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AEROSPACE SENSOR COMPONENT AND SUBSYSTEM INVESTIGATION AND INNOVATION-2 COMPONENT EXPLORATION AND DEVELOPMENT (ASCSII-2 CED)

Delivery Order 0003: Hermetically Sealed Cavities in 3-D GaAs-Silicon and Silicon-Silicon Packages for Microelectromechanical System (MEMS) Devices Using Selective and Large-Scale Bonding

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14. ABSTRACT

Chip-scale bonding of GaAs-to-silicon and silicon-to-silicon to produce cavities for 3-D assembly of MEMS devices has been demonstrated using SnAgCu and eutectic SnPb solders. Laser and furnace reflow were used for region-selective and fast bonding of the chips, respectively, for 3-D assembly. For example, for GaAs-to-silicon bonding, lines of solder paste, 150 mm in width, were screen-printed onto silicon wafers to form square-shaped sealing rings as small as 2 by 2 mm. The solder line width was optimized to provide the smallest width, yet sufficient to ensure a hermetic seal. The solder was reflowed, and the wafer was diced into individual chips of various die sizes. The chips were then flipped onto gold-coated GaAs chips and again placed in the reflow oven at a temperature of up to 250 °C for a total reflow time of 7 minutes. The bonded chips were then tested for hermeticity using MIL-STD-883E and by examining the sealed area after the separation of the chips using a pull test. For the case of selectively laser-bonded silicon-to-silicon chips, the structures exhibited excellent hermeticity and adhesion strength with a uniform microcavity and uniform reflow of the solder.

15. SUBJECT TERMS
MEMS, GaAs, silicon, packaging, gold-coating, solder, laser bonding, reflow oven bonding

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TABLE OF CONTENTS

List of Figures

List of Tables

Preface

This research project was conducted under Systran Grant 3118, sponsored by Air Force Research Laboratory, Sensors Directorate (AFRL/SNDI), Wright-Patterson AFB, Ohio. The Air Force Program Manager was Charles Stevens. The Air Force Technical Manager was Dr. Richard Strawser. The Principal Investigator was Dr. Ajay P. Malshe of University of Arkansas. The Systran Federal Program Manager was Dr. V. “Nagu” Nagarajan.

1. Summary

The overall goal of this project is to design, develop, and test a novel but simple wafer-level and chip-scale packaging and integration scheme (Figure 1) at the University of Arkansas for gold radio frequency (RF) MEMS switches on gallium arsenide (GaAs) substrates provided by AFRL/SNDI at Wright-Patterson AFB. This packaging scheme would allow wafer-level packaging; thereby overcoming typical packaging-related issues such as die handling, packaging-induced stress modification, and interconnection length.

In Phase I of the program, the initial goals were (1) completing the application-specific design of the package and laying out the process model, (2) starting RF simulation of the package using ANSOFT™, and (3) developing a reliable chip-to-chip bonding process, which will have potential to further apply to the wafer-to-wafer bonding process. During the course of the project it became evident that goals one and three are crucial for the further success of the program, and hence a student named Mr. Kelly, who was working on this project, focused on these goals. However, for the first 3 months of this project, another student (in a trial period) named Ms. Cragan, spent time acquiring and learning ANSOFT™, which was aimed for goal number two.

Both of the goals have been successfully met, and the details are described in the following text. A key innovation is made on the previous design, which will completely bypass the step of back-polishing of the GaAs device wafer after wafer-to-wafer bonding for exposing through-wafer electrical interconnects. The innovation is being prepared as a patent disclosure.

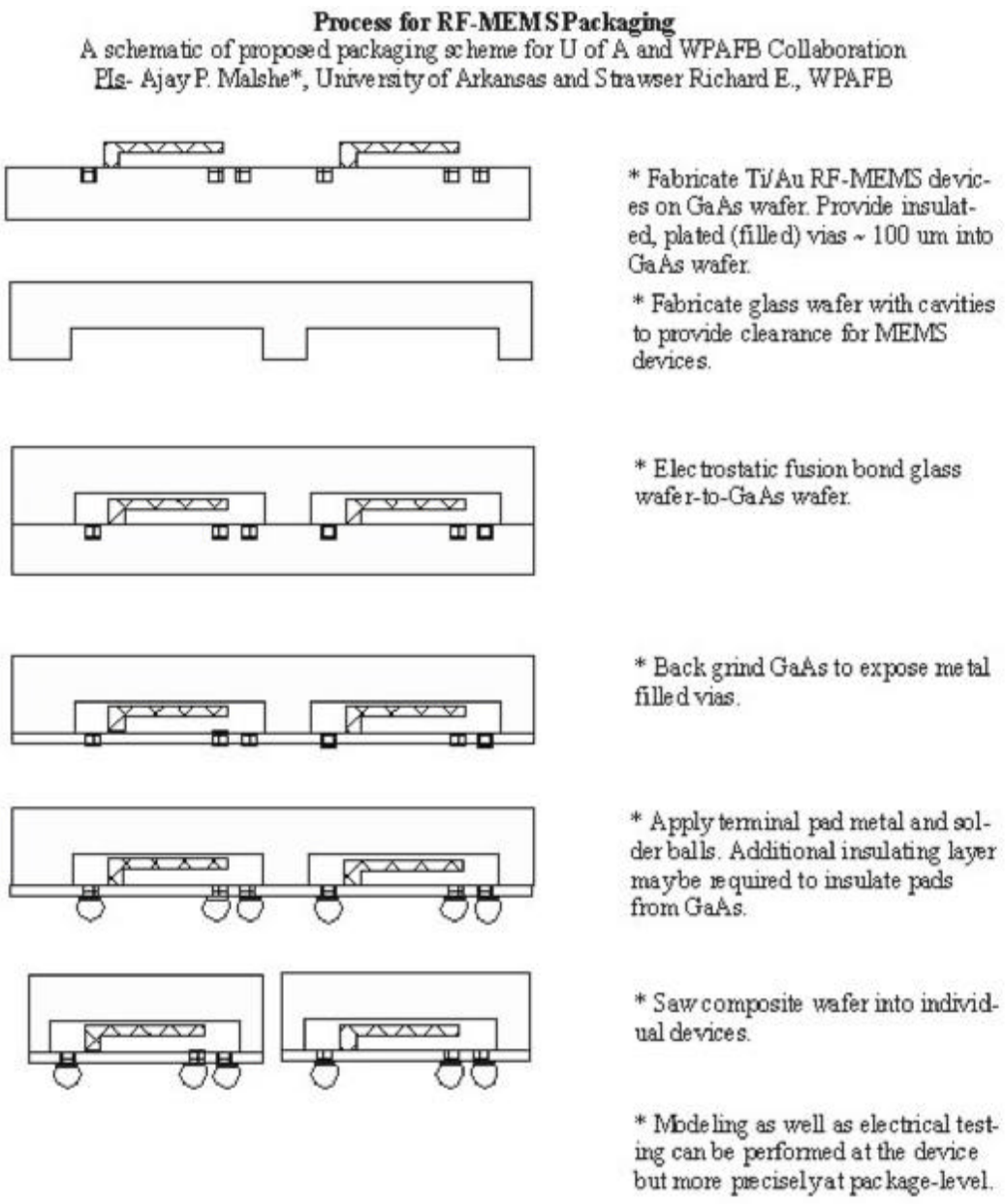


Figure 1. Wafer-Level and Chip-Scale Packaging Design That Was Proposed in 2001 (from the proposal)

2. Introduction and Background

MEMS devices hold great promise for miniaturization, cost reduction, and performance enhancement over their macroscopic counterparts [1]. They are a diverse array of products and are known to be very sensitive to device packaging and assembly techniques [2,3]. Typically, because of their varied sensing and actuation functionality, MEMS devices require application-specific packaging schemes [3]. MEMS-based microsensors and microactuators must simultaneously be able to interact with, and be protected from their environment. In addition to an electrical interface required by microelectronics, MEMS also require mechanical and/or optical, and/or pneumatic interfaces. So far, little attention has been provided to systematically investigate the effect of packaging and assembly parameters on the functionality of MEMS, which is a major challenge for application implementation and market realization [3]. Despite the diversity of MEMS devices and requirements, to achieve reliable MEMS operation and reproducible performance, it will be necessary to understand the influence of major packaging factors, such as die handling, die attachment, and outgassing during die attach cure. Typically, the effect of these parameters is magnified, when dealing with surface micromachined MEMS structures rather than the bulk micromachined ones. For example, RF MEMS switches, which are surface micromachined MEMS, can be degraded due to die attach stress and outgassing during die attach cure. Currently, prepackage yield is typically in the range of 80 to 98 percent, while postpackage yield can be in the range of 40 to 60 percent. This low yield occurs as a result of incorrect die-handling and/or stress-induced fracture and/or redeposition of organic and water vapors on the die during die attach cure process. In Phase I of the research program, the Principal Investigators (PIs) addressed these problems by systematically developing a novel wafer-level and chip-scale packaging design, and thus, successfully developing a key chip-to-chip selective bonding process.

2.1. Technical Approach

Many RF devices use GaAs due to its electrical properties as opposed to silicon. RF MEMS devices are no exception. A design for an RF MEMS capacitive switch on a GaAs substrate was provided for which a packaging scheme was to be developed. A packaging scheme was

devised that involves using a capping chip or wafer with cavities etched to house the device to be hermetically bonded to the device wafer using solder reflowed by CO_2 laser.

Primarily, chip-scale bonding of GaAs-to-silicon and silicon-to-silicon to produce cavities for 3-D assembly of MEMS devices has been demonstrated using SnAgCu and euctectic SnPb solders. Laser and furnace reflow processes were used for region-selective and fast bonding of the chips, respectively, for 3-D assembly. Cavity dimensions as small as 2 by 2 mm^2 with bonding ring linewidth as small as 150 μm were achieved successfully. A manuscript for the IMAPS conference and journal is being prepared and will be published.

Initially, it was planned to bond chips of GaAs-to-silicon, silicon-to-silicon, GaAs-to-glass, glass-to-glass, and GaAs-to-GaAs. Selective laser and reference furnace reflow processes were preferred means for the bonding. During the course of the project experiments, predominantly GaAs-silicon and silicon-to-silicon bonding were pursued for multiple technical and nontechnical reasons:

- GaAs substrates are much more expensive and more fragile than silicon substrates. Therefore, it was decided not to pursue GaAs-to-GaAs bonding and that silicon could be used, and initial experiments were performed to demonstrate feasibility.
- Partial optical transmittance of laser through the lid chip, in this case either silicon or glass, where the device chip is GaAs is critical for the bonding. Currently, we have used an IR (10.6 μm, source of heat) CO_2 laser, which is partially transparent to silicon but opaque to the borosilicate glass. Near Infra-Red (NIR) or Visual (VIS) wavelengths using Nd-YAG or diode laser are suitable for bonding GaAs-to-glass. Glass is transparent to these wavelengths. At the same time, it is important to note that it is mechanically very sensitive and fragile to realize mechanical bonding of GaAs-to-glass. Considering the above realities and the following facts, the decision was made to focus on the first priority, GaAs-to-silicon and study silicon-to-silicon bonding as a reference: (1) 1 year duration of the project, (2) limited financial resource to set up both CO_2 and Nd-YAG or diode laser bonding systems, and (3) available graduate student human resource to complete the task.

- Additionally, the PI's group is modifying the design of Figure 1 for packaging vertical cavity-emitting diodes at wafer-scale. In this project, a process for optical quality glass-to-glass wafer attachment is being developed. Thus, in the future, if desired this knowledge base can be further used to develop GaAs-to-glass bonding.

Also, the success of this project is also due to technical know-how and contribution of another Ph.D. student, Mr. Yi Tao from PI's group, who is not supported by this project. He is working toward vacuum packaging of surface micromachined MEMS devices using gettering structures, sponsored by National Science Foundation (NSF).

3. Experimentation: Sample Preparation and Testing

In the initial experiments, test structures were prepared using 750 µm, 1.0 mm, 1.5 mm, and 2.0 mm line widths with a 1 cm^2 footprint. The experiments produced successful and promising results. However, these line widths were much larger than desired, and further experiments using these structures were abandoned. Smaller test structures were created.

Test structures were developed with combinations of 2 by 2, 3 by 3, 4 by 4, and 5 by 5 mm^2 footprints and 150, 250, 350, 450, and 750 µm line widths for the sealing ring. The substrates were sputtered with 500 Å of Ti, 1 µm of Cu, and 500 Å of Ti. The substrates were patterned with photoresist, and the top layer of Ti was removed. A 2-µm layer of Ni was plated onto the surface, followed by a thin layer of Ni-strike, and then gold. The photoresist was removed, and the remaining areas Ti and Cu were etched away.

3.1 Solder Screen Printing

An 80-mesh screen with 2-mil wires at a 90º pitch and 2-mil emulsion thickness was used to print the solder paste onto the substrate using a AMI Presco MSP-485 screen printer. A 90-durometer squeegee was used at a 3-mil screen snapoff and at a squeegee pressure of 5.65 mm. In the teststructure design, the sealing rings with the thinnest widths were at one end, while the thickest were at the other. When printing in the direction of thinnest to thickest lines, the thinner lines had poor solder coverage, and this resulted in solder beads forming at corners of the 150-µm-wide structures. However, when the solder paste was printed in the direction of thickest lines to thinnest, the solder lines were more uniform and defined, and fewer solder beads formed after reflow.

To improve the yield and solder resolution, a finer mesh screen, such as a 120 or 180 mesh, can be used. While this would increase the resolution of the solder, the print area would decrease due to the presence of more wires per square inch. To accommodate for this change, the screen can be designed with print areas larger than the metal areas. Since the solder only wets to the metal, any excess solder on the substrate will move toward the metal areas, providing the volume needed for uniform solder lines.

For images related to the above test structure and process research, please visit http://intra.engr.uark.edu/~mwkelle/research_images/

3.2 Solder Reflow

The reflow profile for SnAgCu solder was developed on the Sikama convection/ conduction reflow oven using a continuous chain-speed setting of 5, 90 ºC for Zone 1, 140 ºC for Zone 2, 210 ºC for Zone 3, and 240 ºC for Zone 4. Test samples were sent through the oven before any sealing structures were reflowed. These were examined after a microetch process was used to reveal the grain structure. The grain structures were examined using an optical microscope and scanning electron microscope (SEM). The first substrate was then sent through the reflow oven, cleaned using acetone to remove remaining flux, and diced into chips. After examination under SEM, incomplete reflow and dendrite formation was noticed. The sealing structures were reflowed once more and reexamined. The surface now appeared smooth and free of dendrites. For consistency, each additional substrate was reflowed twice.

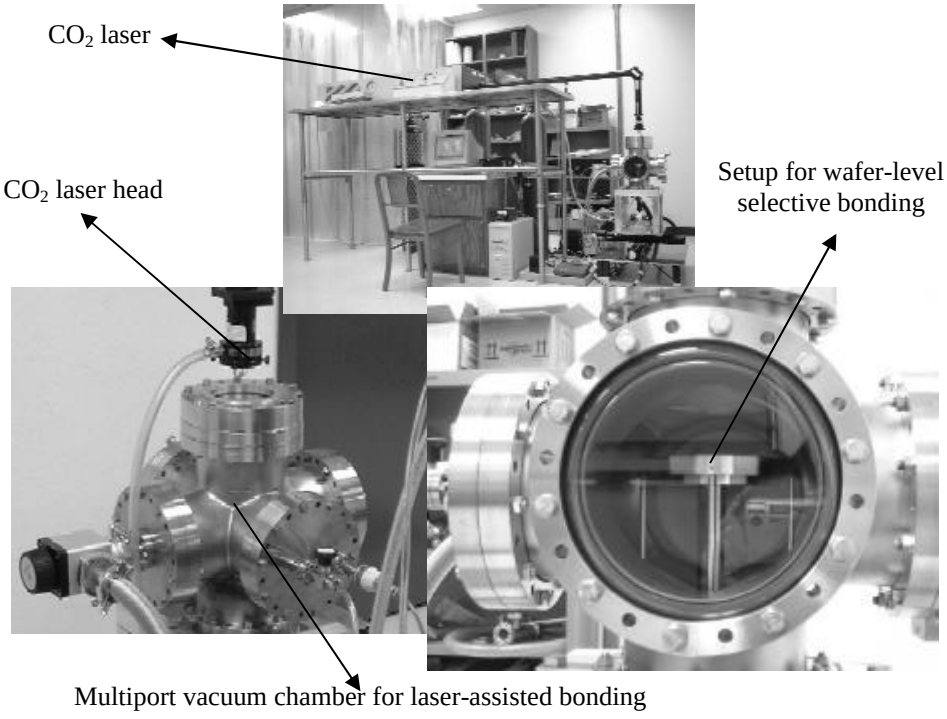


Figure 2: Laser-Assisted Selective Bonding Set Up For Wafer-Level And Chip-Scale Packaging In Selective Vacuum Environment

3.3 Laser Bonding

A mount to position the samples for bonding was constructed. They consisted of a bottom piece that rests in a 5 inch wafer-sized plate and holds 7.5 by 7.5 mm^2 gold-plated GaAs chips, and an interchangeable top piece that holds diced silicon capping chips. The mount, plate, and samples were then placed into the laser-bonding chamber (see figure 2). The x-y stage was aligned so that the laser beam was focused onto the center of the sample. Since in the second test structure, with combinations of 2 by 2, 3 by 3, 4 by 4, and 5 by 5 mm^2 footprints and 150, 250, 350, 450, and 750 μm line widths for the sealing ring, chips were so small, the temperature at the center of the chips would be close to the temperature at the sealing area. Therefore, rastering across the chips with the laser was considered to be secondary. Laser (CW CO_2 laser with λ=10.6 μm) power output was varied from 5 mA to 15 mA, and the time was varied from 5 to 15 seconds. The bond depends on the chip size, power output, and time. Initially, the samples were checked for incomplete bonding by attempting to separate the chips manually. Incompletely bonded samples were discarded, and the remaining samples were analyzed using the acoustic scanning microscope (ASM). Since the bond lines were so thin, completely bonded regions could not be distinguished indisputably from the partially bonded or even unbonded regions. The bonds have to be analyzed using cross-sectioning or by examining the bonded areas after separation by pull test.

Testing using a 1-cm^2 silicon chip was performed to determine the temperature of the chip during bonding. The temperature was measured simultaneously using a thermocouple mounted to the bottom of the chip and by IR camera. The temperatures recorded by both methods coincided closely. However, the IR camera used has a temperature limit of 450 ºC.

3.4 Reflow Oven Bonding

Considering the fact that temperature at the center of the chips would be closer to the temperature at the sealing area and to reduce the variables inherent in laser bonding in the given setup, the capping chips and gold-plated GaAs chips were assembled and reflowed using the same profile as before. Several chips were cross-sectioned, and the height of the cavity formed from the thickness of the capping-wafer metal and solder was 30 to 50 μm.

This resulted in cavity volumes of 0.008 mm^3 for the smallest possible volume (30 µm cavity height, 2 by 2 mm^2 footprint, 750 µm line width) to 0.024 mm^3 for the largest possible volume (50 µm cavity height, 5 by 5 mm^2 footprint, 750 µm line width). Hermeticity was tested using the MIL-STD-883E fine leak test. According to the requirements of the test, volumes of 0.01 cm^3 or less are to be placed in the helium bomb for 2 hours at 75 psi. Each sample was placed in the bomb for the required time, removed from the bombing chamber, placed in the leak test apparatus located in a separate room to reduce helium contamination, and then connected to the vacuum pump and helium detector. The strength of the bond was tested using mechanical pull testing.

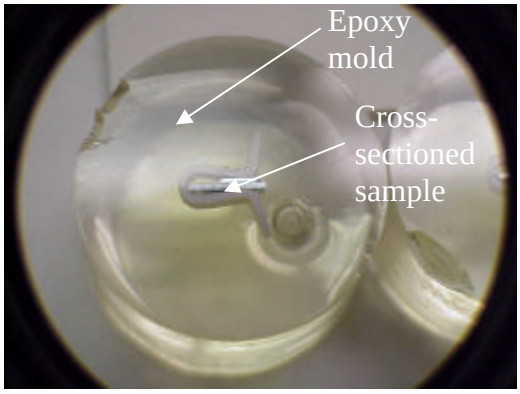


Figure 3: Cross-Sectioned Epoxy Mold Containing Bonded Chip

4. Results and Discussion

The following discussion highlights the findings of this project through (1) optical analysis of the cross section of the bonded cavity, (2) results of the mechanical pull tests, and (3) results of the vacuum testing using MIL-STD-883E criteria.

4.1 Optical Analysis of the Cross-Sectioned Cavity

Metallography sample preparation technique has been used for the sample preparation, where a typical bonded cavity is placed in an epoxy mold (see figure 3) and then lapped and polished using abrasive media. Then the sample is cleaned and used for optical observation.

Figure 4 demonstrates the optical micrographs of the various portions of the GaAs-to-silicon bonded chips. Figure 4(a) demonstrates the uniform solder bonding at the silicon-solder ring-GaAs interface. Figure 4(b) shows uniform cavity where the thickness of the cavity is about 10 microns. Figure 4(c) shows the uniform and well-developed microstructure in the soldering area. These optical micrographs collectively demonstrate uniform bonding at the GaAs-solder-silicon interfaces and uniform cavity formation at the chip-scale, which is important for the proposed design (Figure 1).

4.2 Pull Testing for Bond Adhesion Strength Measurement

Figures 5(a) and (b) demonstrate the findings of the pull test experiments. As evident from both of the figures, during the pull test we did not see any de-lamination, and the parts broke apart at the interface and show excellent mechanical bonding adequate for the purpose of the capping during chip-scale packaging.

4.3 Vacuum Testing for Measuring the Hermetic Performance Measurement

Table 1 shows the data for the vacuum leak testing. On an average, the data indicates lower leak rate (10^{-8} atm.cm^3/sec of beyond), except in a few cases. It is important to point out that further process parameter optimization is essential using a larger selection of samples to reproduce the process for manufacturing purposes. Also, currently the PI's lab is developing systematic procedures for vacuum testing of fine cavities for wafer-level and chip-scale testing, which is an evolving area, and will benefit the program further.

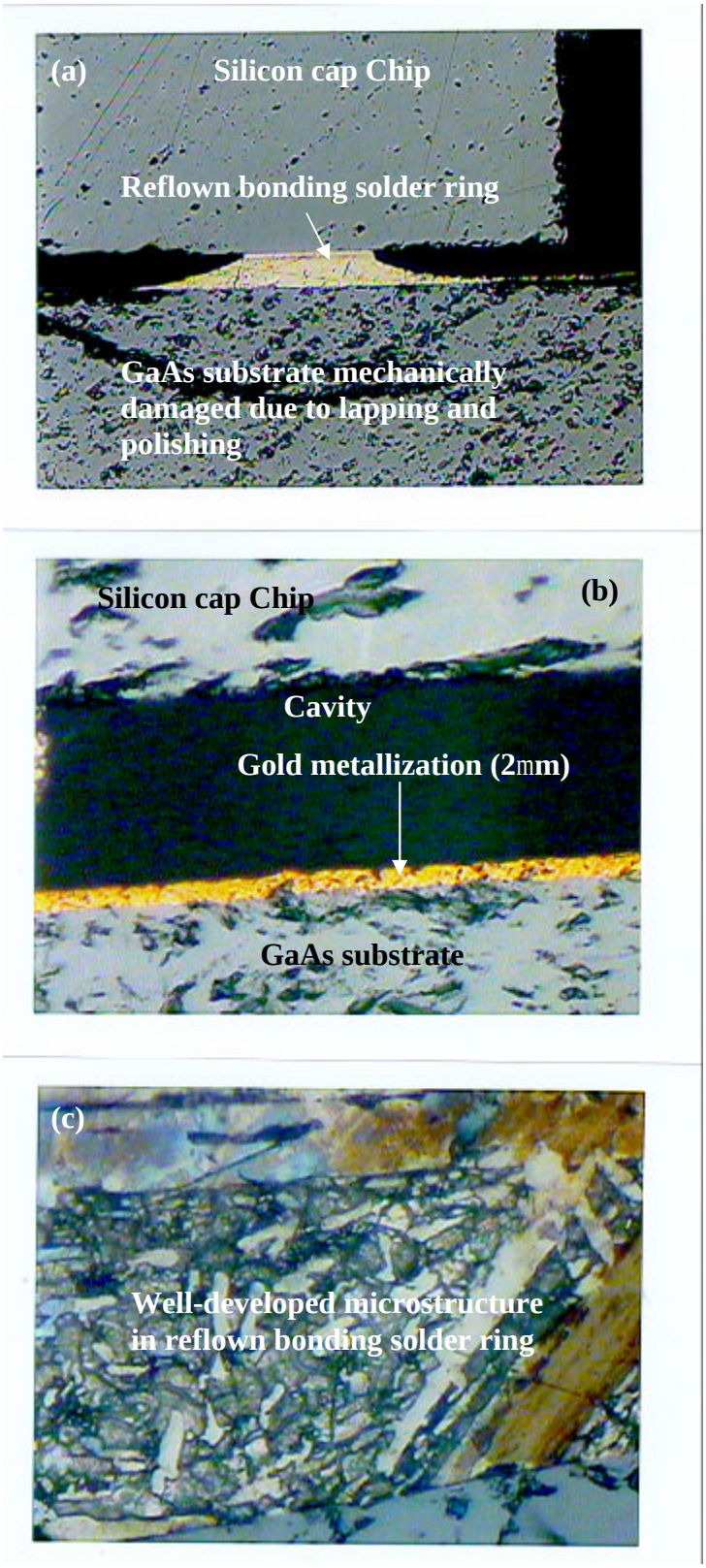
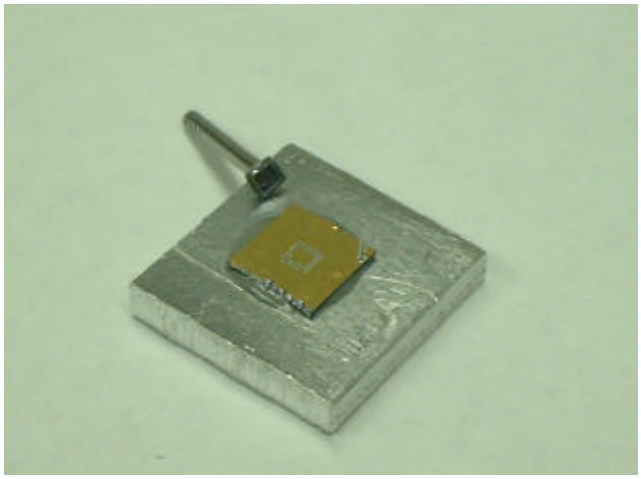
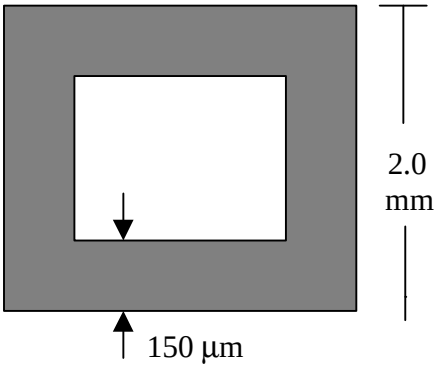


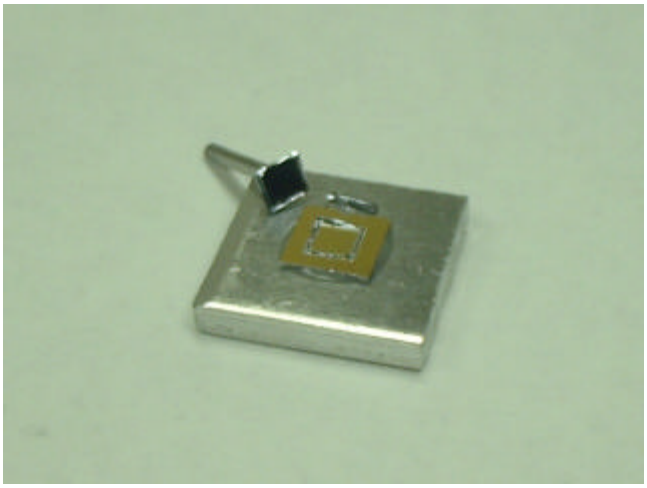
Figure 4: Optical Micrographs Of The Interface Of GaAs-To-Silicon Bonded Chips

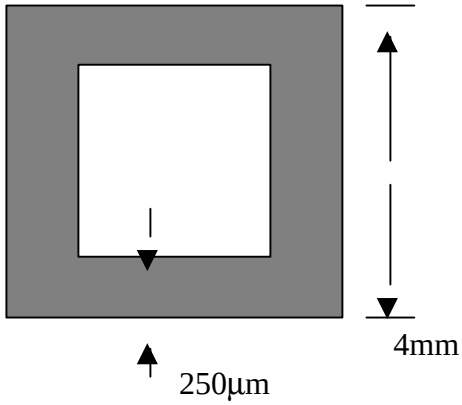




- Feature Size- 150µm
- Die Size- 2×2 mm
- Pull Force- 1.70 kgf - 16.72N
- Bonding Area- 1.11×10-6 m^2
- Pull Strength- 16.72 / 1.11×10-6 = **15.1 Mpa**.

Figure 5(a): Pull Test Result On Sample - 1





- Feature Size- 250µm
- Die Size- 4×4 mm
- Pull Force- 3.14 kgf – 30.88N
- Bonding Area- 3.75×10-6 m^2
- Pull Strength- 30.88 / 3.75×10-6 = **8.23Mpa.**

Figure 5(b): Pull Test Result On Sample - 2

Table 1. Vacuum Leak Testing Data on Sealed Cavities

Sample Description		Readings after I minute (Atm.cm3/sec)	Readings after 5 minutes (Atm.cm3/sec)
FSx(µm)	Die Size (mm)		
150	2x2	1.6×10–8	0.8×10–8
	3x3	0.2×10–8	0.2×10–8
	4x4	1.8×10–9	1.5×10–9
	5x5	1.1×10–9	0.9×10–9
250	2x2	2.8×10–7	0.4×10–7
	3x3	1.6×10–9	1.4×10–9
	4x4	1.4×10–9	1.2×10–9
	5x5	1.0×10–9	0.8×10–9
350	2x2	1.6×10–7	1.7×10–7
	3x3	1.6×10–9	1.8×10–9
	4x4	2.1×10–9	3.1×10–9
	5x5	2.3×10–9	3.0×10–9
450	2x2	2.1×10–9	2.2×10–9
	3x3	2.0×10–8	2.2×10–8
	4x4	1.1×10–7	1.0×10–7
	5x5	3.6×10–9	7.6×10–9
750	2x2	3.8×10–8	4.3×10–8
	3x3	1.4×10–8	1.7×10–8
	4x4	0.6×10–8	0.7×10–8
	5x5	0.3×10–8	0.3×10–8

5. Conclusion

It is demonstrated that bonding of GaAs and silicon at chip scale can be successfully achieved using metal solder rings by IR oven reflow on the test structures at the smaller dimensions and by IR laser selective reflow on the test structures at the larger dimensions. The optical micrograph analysis shows consistent bonding at the interface and uniform cavity formation. Die attachment pull test data demonstrate adequate bonding strength, and vacuum testing confirms uniform and consistent sealing of the cavities with good hermeticity. These bonding processes are insertable in current manufacturing processes. Further systematic developments, described in the next section on Future Directions, for packaging processes at wafer-level and chip scale are essential for reliable packaging of RF MEMS devices.

6. Future Directions

Please see figure 6(a) and 6(b) for schematics of assembled products.

- Reduce sealing ring footprint/line width.
    - Modify screen parameters.
        - Increase mesh size.
        - "Overprint" or increase emulsion thickness for necessary wet-print thickness to line width ratio.
    - Use of "Indent Reflow Sealing (IRS)" Technique.
        - Solder sealing ring is reflowed.
        - Groove or "indent" is created by mechanical means to function as a vent.
        - Sealing ring is subjected to dry fluor-based plasma pretreatment to improve solderability and pre-bond strength.
        - Capping wafer is diced into chips.
        - Capping chip is assembled onto device wafer using a flip-chip aligner and bonder using a thermo-compressing pre-bonding technique.
        - The oven chamber is evacuated, filled with inert gas, and temperature is increased to melt and reflow solder.
        - Wafer/chip assemblies are diced into individual chips.
- Signal routing with through-hole vias
    - GaAs
    - Possibility on silicon (modeling)
- Testing of switches before and after packaging.

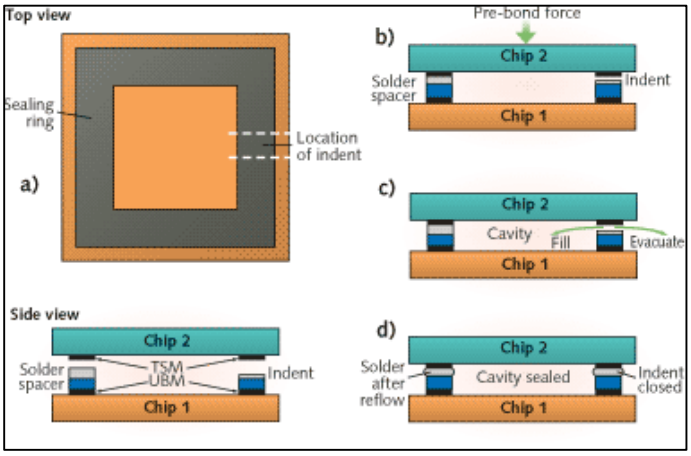


Figure 6(a): Schematic of Bonding and Encapsulation Scheme
TSM: Top Solder Metalization
UBM: Under Bottom Metalization

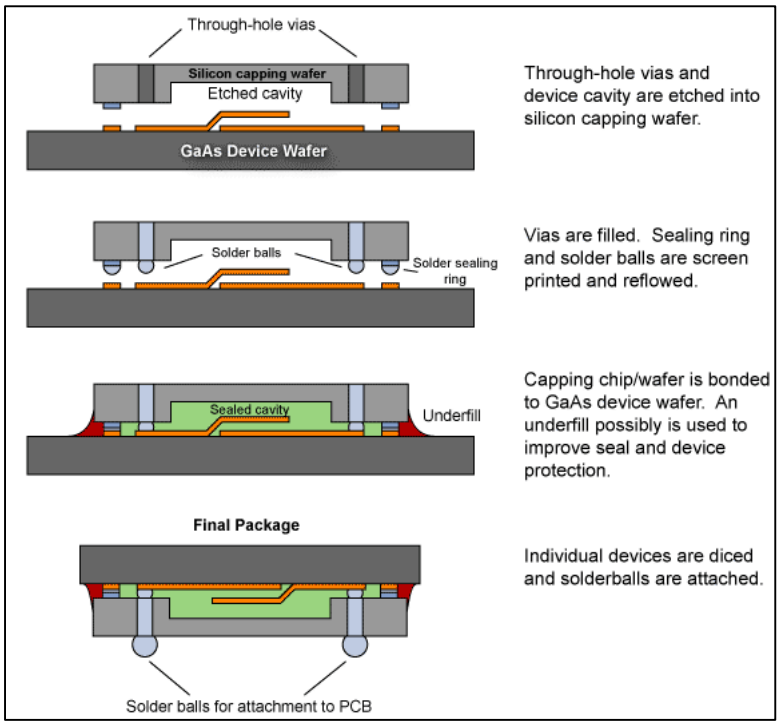


Figure 6(b): A Schematic of Modified Approach for Wafer Level Chipscale Packaging of RF-MEMS and Related Microdevices for Attachment to Printed Circuit Board (PCB)

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