REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Washington Headquarters Service, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington, DC 20503.

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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT DATE	3. DATES COVERED *(From - To)*
	01/22/2004	03/01/02-06/30/03

4. TITLE AND SUBTITLE
The IEEE Lester Eastman Conference on High Performance Devices, 2002

5a. CONTRACT NUMBER

5b. GRANT NUMBER
N00014-02-1-0407

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Robert E. Leoni, Proceedings
Kolodzey, James, Proposal and Program Treasurer

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
James Kolodzey
Department of Electrical and Computer Engineering,
University of Delaware, Newark DE, USA 19716-3130

8. PERFORMING ORGANIZATION REPORT NUMBER
03-3-43-3130-01

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Harry Dietrich, ONR 312
Office of Naval Research
Ballston Centre Tower One
800 North Quincy Street
Arlington, VA 22217-5660

10. SPONSOR/MONITOR'S ACRONYM(S)
ONR

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT

DISTRIBUTION STATEMENT A
Approved for Public Release
Distribution Unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

This grant supported the registration and travel expenses for 20 students.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPONE NUMBER (*Include area code*)

PROCEEDINGS
IEEE LESTER EASTMAN CONFERENCE ON HIGH PERFORMANCE DEVICES

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AIXTRON CORPORATION





IEEE Catalog Number: 02CH37365

Proceedings
IEEE Lester Eastman Conference on High Performance Devices

Leda Lunardi
GENERAL CHAIR

John C. Zolper	Robert E. Leoni III	James Kolodzey
PROGRAM	**PROCEEDINGS**	**TREASURER**

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IEEE Microwave Theory and Techniques Society
Office of Naval Research
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Aixtron Corporation

IEEE ISBN Number: 0-7803-7478-9

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IEEE Catalog Number: 02CH37365
ISBN: 0-7803-7478-9
Library of Congress: 2002103842

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Professor Lester F. Eastman

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Abstract

Professor Eastman is one of the world leaders in the physics and technology of compound semiconductor materials and devices. He has invented, fabricated, and investigated many novel semiconductor materials and devices, and his work on so many occasions has resulted in breakthroughs enabling important practical applications. The best solid-state device groups have followed his ideas with great success, and his former students and associates work in leadership positions in hundreds of leading companies, research laboratories and Universities in the United States and around the globe.

I. Short Biography

The entire professional life of Professor Eastman is closely linked to Cornell University. He received his B.S. in 1953, his M.S. in 1955 and his Ph.D. degree in 1957 from Cornell University. Ever since, he has been doing research on compound semiconductor materials, high speed devices, and circuits, and has been active in organizing workshops and conferences on these subjects at Cornell and world wide. He was an exchange faculty member in Sweden in 1960/61, and a researcher at Sarnoff Laboratory in 1964/65. In 1977 he joined other Cornell faculty members in obtaining funding and founded the National Research and Resource Sub Micron Facility at Cornell (now Cornell Nanofabrication Facility). He initiated the Joint Services Electronics Program at Cornell in 1977 and directed it for ten years. During the 1978-1979 year he was on leave at MIT's Lincoln Laboratory. During the 1985-86 year he worked at IBM Watson Research Laboratory. During 1983 he was the IEEE Electron Device Society National Lecturer. He was a member of the U.S. Government Advisory Group on Electron Devices from 1978-1988, and serves as a consultant for several industries. He has been a Fellow of IEEE since 1969 and has been a member of the Electromagnetics Academy since 1990. In 1986, he was elected to the National Academy of Engineering for pioneering and continuing contributions to communications technology resulting from the development of high-speed and high-frequency gallium arsenide devices. He was appointed the John L. Given Foundation Professor of Engineering at Cornell in January 1985. In 1991 he was awarded the Welker Medal and Annual Award of the International Symposium on Gallium Arsenide and Related Compounds. He was awarded the Alexander von Humboldt Senior Fellowship in 1994, and the Aldert van der Ziel Award in 1995. The IEEE honored him with their 1999 Graduate Teaching Award and Third Millennium Medal 2000. He received the Wisdom Award of Honor in 2000. In 2001, he was elected Fellow of the American Physical Society. Professor Eastman and has supervised a record 110 PhD theses, and, over the years, his students and former students have made significant contributions and won national and international

0-7803-7478/02/$17.00 © 2002 IEEE

prizes by advancing the state of the art of molecular beam epitaxy, microwave transistors, and optoelectronic devices.

Professor Eastman established Cayuga Associates (a research and development firm in Ithaca, New York). He is a Co-Founder and Scientific Advisory Board Chairman of Nova Crystals, an optical communications company, and an active and sought after consultant to industry and US and foreign governments.



Fig. 1 Professor Lester F. Eastman. January 2002.

II. Personal Notes

Professor Eastman's achievements are truly impressive and too numerous to list in a short paper. He was the first to propose and then develop the concept of ballistic transport in ultra small (deep sub-micron) devices, based on both compound and elemental semiconductor materials. This work has started a whole new field of solid state research, and literally changed the way people approach energy band engineering of semiconductor devices. His other achievements include developing a new generation of modulation-doped structures, contributing to the physics of hot electron transport and to the physics of the Gunn effect, developing and implementing the concept of wide band gap piezoelectric field effect transistors, developing delta-doping by MBE, discovering new features of electron transport in wide band gap modulation structures, and contributing to the physics of semiconductor lasers.

To this remarkable list of personal scientific contributions, we must add Professor Eastman's great contribution to educating several generations of materials scientists, device physicists and engineers. So many recognized international leaders in materials physics, device physics and technology have come from his group. In fact, I think that there are probably very few prominent device physics labs in this country that do not include his former doctoral or post-doctoral students. Professor Eastman graduated over 110 Ph. Ds and

mentored several tens of post-doctoral researchers. I was one of them joining his group in 1976, and, in a way, always remaining a part of his group, no matter where I worked, always seeking his input, listening to his ideas, cherishing an opportunity to work with him and his students and associates. As I wrote in the Preface to my book on GaAs devices and circuits, I have greatly benefited from the spirit of the pursuit of excellence that exists in his group. [1] His vision, his generosity, his dedication to engineering, physics, science, and technology, his modesty, his concern for his colleagues and students, present and former, his hard work, his pursuit of excellence made him my role model.

III. Lester Eastman Conference

Professor Eastman served with great distinction as Session Chair, Program Committee Member, Chair, and Organizer of many prestigious national and international conferences. He has given a countless number of plenary, keynote, and invited talks. In 1967, Professor Eastman originated the biennial IEEE-Cornell Conference on Microwave Semiconductors, which later became Biennial IEEE/Cornell University Conference on High Performance Devices. Many new breakthroughs and key developments were first announced at this conference, including the first paper on the ballistic transport. [2] In 2002, IEEE -Cornell Conference on Microwave Semiconductors was renamed IEEE Lester Eastman Conference on High Performance Devices, and all of us, *Eastmanites* – his present and former students and associates, feel very much pleased and honored by this change.

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THREE DECADES OF OUR GRADUATE RESEARCH AND EDUCATION IN COMPOUND SEMICONDUCTOR MATERIALS AND DEVICES

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Introduction

Research on compound semiconductors, beginning with Gallium Arsenide, started at Cornell in 1965. Emphasis has been on pure device-quality material, abrupt heterojunctions, and novel structures for microwave transistors and lasers. There have been 111 PhD and 41 MS degrees granted, and the effort of several senior staff members, and 81 visiting scientists were involved. Most are in U.S. industry and universities, with some in Europe and in the Far East. A substantial fraction of these participants have been involved in the industrial developments leading to the $15-20 Billion annual business in the compound semiconductor areas. This paper covers selected technical results from this early and extended Cornell program in this field.

Technical Results

Initial effort involved n-type GaAs operated in the transferred-electron (Gunn effect) mode of oscillation. Commercial bulk GaAs was given ohmic contacts and operated in the pulsed mode to limit over-heating. Peak power of ~ 6KW in L band [1], and > 1 KW at X band were achieved using thick samples operating in the limited space-charge accumulation (LSA) mode in special cavities. Liquid phase epitaxy was then developed, allowing controlled doping of thick layers of n-type GaAs. In the course of this effort, the first buffer layer was invented and named, to separate the substantial impurities and defects in the substrate from the active layer. The use of electric current through the layered stack of the GaAs source crystal, the melt, and the seed crystal, to control growth rate was made [2]. As part of the early liquid phase epitaxy, abrupt heterojunctions of lightly-doped n-type AlGaAs/GaAs were grown. At the urging of Prof. Herbert Kroemer, these were tested for I (V) across the heterojunction. They were the first strongly rectifying [3] such heterojunctions, experimentally proving his concept of carrier confinement at such interfaces. Next, pure InP [4] and $In_{.53}Ga_{.47}As$ [5] were grown by LPE to show their interesting properties. The current-controlled growth method was also used later, to control the growth of InP.

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As part of the initial national submicron (nanofabrication) facility, established at Cornell in 1977, molecular beam epitaxy effort was started. Dr.Colin Wood joined Cornell to build up this MBE effort. The initial achievement was the lowering of electron trap densities, caused by arsenic anti-site defects, by three orders of magnitude, as determined by DLTS [6], [7]. Others later reversed this effect to cause higher trap densities for high resistivity and fast photo response. The first GaAs HEMT to outperform MESFET's was fabricated. The concept of atomic-planar doping (later renamed δ-doping) was initiated. Such atomic-layer doping of HEMT's, with a spacer layer between the doping plane and the 2DEG, was then initiated [8]. Using a 90 Å GaAs quantum well channel, between AlGaAs barriers, the first quantum well HEMT was made, limiting short-channel effects. Former students conceived of the use of a pseudomorphic quantum well on GaAs for improving these HEMT's. The first $Al_{.48}In_{.52}As$ barrier, for $Ga_{.47}In_{.53}As$ channels, both lattice-matched to InP substrates, was then conceived and grown [9]. This generic structure is now widely used in microwave transistors and in lasers for fiber-optical communication.

In order to achieve high performance transistors at high frequencies, the mushroom-cross-section gate was initiated, using tri-level resist in electron-beam lithography [10]. This method of making short gates, with low resistance along the gate, replaced the initial T-gate studied jointly with Hughes Research Laboratory, and formed with two layered metals, with a selective undercut etch of the bottom metal. It also involved self-aligned, ion-implanted ohmic contacts [11]. The latter T-gate transistor had established a record switching time of 15 PS. The former established record of 150 GHz = f_t, and 250 GHz f_{max}, for a .15 μm footprint gate on a GaAs HEMT.

The concept of ballistic electrons in compound semiconductors was initiated and named, with .25 eV electrons predicted to travel .18 μm at room temperature in GaAs , and 10's of microns at low temperature, when phonons are absent [12]. There have been several fundamental physical measurements, as well as novel quantum electron devices, that depend on these ballistic electrons. Direct measurements of this effect was made by Dr. M. Heiblum at IBM Research Laboratory, using a heterojunction potential step to launch the electrons [13]. Another of our innovative structures, the atomic-planar-doped barrier, also has interesting I(V) characteristics and can also be used to launch ballistic electrons. A ballistic injection HBT was also conceived [14].

Organo metallic vapor phase epitaxy OMVPE was also developed, initially for phosphide-related layers on GaAs substrates [15]. The initial AlGaInP red laser was fabricated. This laser is in wide use today. The InGaP/InGaAs/GaAs HEMT was then also studied, to show that it had higher current density and much less $1/f$ noise. The InGaP has a wide bandgap, and has no deep donors from the DX centers that occur in $Al_xGa_{1-x}As$ when (X) > (.22).

The initial pseudomorphic InGaAs quantum well laser was then grown and tested [16]. It had $In_{.37}Ga_{.63}As$ in the ~ 40 Å quantum well, yielding .99 μm wave length. This device was further developed elsewhere to provide .98 μm wave length pump light for Erbium-doped fiber amplifiers. The pseudomorphic quantum well laser had low threshold current density, because the light hole states in the valence band were raised up to the band edge by the strain. These states have a lower density due to the lighter hole effective mass, so lower current density was required to fill them. By going to 3 or 4 pseudomorphic quantum wells, it was possible to achieve direct modulation at higher frequencies with short laser cavities. A new state-of-the-art of 28 GHz for the 3db bandwidth of modulation was achieved at Cornell [17]. Later, a former student working with others at the Fraunhofer Applied Physics Laboratory in Freiburg, Germany, achieved a world record: 40 GHz bandwidth by the same technique.

For more than six years lately, Gallium Nitride and related alloys and compounds have been the emphasis. Both OMVPE [18] and MBE have been used to grow GaN and AlGaN/GaN and lately InN has been grown on sapphire as a substrate. AlGaN/GaN has also been grown on SiC for improved heat removal. Monte Carlo calculations were done to obtain the dependence of electron velocity on electric field. For GaN [19] it showed a peak electron velocity of ~ 2.8 $x10^7$cm/s at room temperature at 150,000 V/cm, and reduced velocity at higher electric field. For non-uniform electric fields, an average transit velocity of 2.0 – 2.5 x 10^7 cm/s was predicted, higher than obtained for most other compound semiconductors. In HEMT experiments to date, no more than 1.3 x 10^7 cm/s has been gotten. One unexpected experimental result was that for lower electron concentration, the electron mobility dropped, unlike the situation in other compound semiconductors. Because foreign substrates are not lattice-matched to the GaN epitaxial material, dislocations thread up through the latter. The dislocation density is ~ 5 x 10^8/cm^2 on SiC, and ~ 2 x 10^9/cm^2 on sapphire. A model was developed, with the dislocation representing a line of acceptors [20] with a band centered at ~ 2.15 eV below the conduction band. The electrons from the n-type background material are depleted around the dislocation, causing a potential rise. These potential rises scatter the electrons, lowering their mobility. This becomes dominant at lower (<10^{17}/cm^3) donor densities, where virtually all electrons are trapped at the dislocations, yielding > 1 x 10^8 Ω -cm resistivity in the undoped GaN.

There is a dominant electrical polarization in the nitrides, yielding a net positive bound electrical charge at the heterojunction of AlGaN/GaN when it is grown along the c-axis, of this Wurtzite crystal, on the Ga-face [21]. A one-year visit to Cornell, by Dr. Oliver Ambacher, on an Alexander von Humboldt Fellowship, transferred this technology. Undoped, polarization-induced 2DEG in these $Al_xGa_{1-x}N$/GaN HEMT structures were then developed, with .30 < x < .35. These yielded 1 – 1.3 x 10^{13}/cm^2 electron sheet density, with up to 1,700 cm^2/V-s electron mobility,

using the OMVPE reactor developed by Prof. J. Richard Shealy. This reactor used a single flow, single pressure, single temperature method, unlike the much more complex method developed earlier in Japan. Optimized ohmic contacts, usually .3 - .5 Ω-mm, were developed using Ti/Al/Ti/Au annealed at 800°C for .5 – 1.0 minute. A substantial slump in drain current, power, and efficiency occurred when high drain bias was applied. This slump was eliminated by our invention of the PECVD Si_3N_4 passivation of the surface, which stabilized the charge in the surface states of exposed AlGaN. The state-of-the-art of power density was then established in 10 GHz class B operation of these polarization-induced AlGaN/GaN HEMT's [23]. It was 11-12 W/mm CW for .3 μm gates, and 100 μm wide channels biased to 45 V_{ds}, at 31%. power-added efficiency. It was 10 W CW for 10 channels, 150 μm wide, with 50 μm pitch, at 30 V_{ds}, at 40% power-added efficiency. These results are approximately an order of magnitude higher than GaAs HEMT's can deliver at the same frequency.

MBE growth of nitrides with Dr. William J. Schaff has recently come up with two important discoveries. One is that the MBE InN has ~ .85 eV bandgap at 300°K, not the value of 1.89 eV in the literature for many years. It has over 2,000 cm^2/V-s mobility at 300 °K, even with $10^{10}/cm^2$ dislocations and ~ 4 x $10^{17}/cm^3$ electron density. This mobility does not drop with reduced electron density, as is the case of GaN, but rises monotonically. Another is that MBE $Al_xGa_{1-x}N$, with X up to .80 μm(?), can yield $10^{20}/cm^3$ electrons when doped with Silicon. This latter result will allow improved performance of U.V. sources down to .28 μm wavelength. Together with the former result, InGaAlN can now be used over a very wide range of optical devices, from IR to U.V. wavelength.

Summary

In the 37 years of activity in this group's research on compound semiconductor materials and devices, much has been discovered, and many students have been educated. The materials include GaAs, AlGaAs, InGaAs, InAlAs, InGaP, GaN, AlGaN, and InN. The devices have included microwave MESFET's, HEMT's, and HBT's, as well as semiconductor lasers for high speed modulation. The students and results have been hired and transferred to industry, where they have made strong contributions to devices for radar and communication.

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LESSONS IN COMPOUND SEMICONDUCTOR DEVICE DEVELOPMENT

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ABSTRACT:

This paper is a mixture of personal opinion and technical fact merged to serve as a general guideline for compound semiconductor device choices. It may be construed as opinionated and contain several generalizations, but it is a result of the path taken by the author and results learned. The crucial importance of materials research in device development is the most important theme in the paper. Also, the need to minimize the complexity of device fabrication is also emphasized.

The main lesson that I learned from being part of the Eastman-group was that "Materials were the engine that drove revolutionary advances in devices." This was especially true in compound semiconductors where the lack of a compatible oxide (native or deposited) made it crucial to harness the full potential of heterostructures. This way, the devices with the potential impact of MOSFETS could be potentially invented (Note the repeated use of "potential"; a recognition that the probability of such success would still be low). To form heterostructures epitaxial techniques such as Liquid Phase Epitaxy (LPE), Molecular Bean Epitaxy (MBE), and Metalorganic Chemical Vapor Disposition (MOCVD) were sequentially invented and perfected. In my opinion, one of the great decisions of Les was to invest heavily first in MBE and subsequently in MOCVD.

Another lesson that I learned was "Do not attempt to do yourself that others can do vastly better." In these early days, the greatness of the group came substantially from the unique expertise provided by Colin Wood (MBE), Dave Woodard (Device Processing) and Gary Wicks (Characterization). With the ability to control composition, doping and thickness provided by MBE, several device advances were proposed and pursued. The driving force behind several of the projects was the attempt to harness the potential of ballistic transport in transistors. In essence, the objective was to move electrons from a source (emitter) to a drain (collector), which was placed ideally a distance less than a mean free path from the source. The goal was to minimize scattering and thereby enhance electron velocities decreasing transit times and increasing operating frequencies. This led to the next question, "Should these devices be vertical or horizontal devices?" Several groups were proposing these Extra High Frequency (EHF) devices using the Permeable Base Transistor (PBT; a vertical device at MIT Lincoln Laboratories), the Planar Doped Barrier Transistor (Cornell; vertical device), the Vertical FET (Cornell and Westinghouse), the Opposed Gate Source Transistor (OGST; Cornell and TRW, a merged vertical and lateral device) and the AlGaAs/GaAs HEMT (Cornell, GE...; a lateral device).

The seduction of vertical devices was that critical dimensions could be controlled precisely by epitaxial growth. Furthermore, techniques such as Hot Electron Launching

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using wide band gap sources to enhance electron velocities in the channel could be readily incorporated. This was indeed true. The drawbacks however turned out to be very difficult to overcome.

1. *The need to precisely define a gate on the sidewall of the conducting channel.*
   The multiple processing steps required to achieve this, primarily by planarization and deposition methods) was more difficult and progressively more expensive than improvements in linewidth and cost afforded by planar fine-line lithography.

2. *The difficulty in achieving the advantages of a recess technology.*
   A recess technology is extremely important in the non-self aligned technologies that dominate compound semiconductor FETs/HEMTs even today. The more obvious reason is the decrease in access resistance afforded by the recess for a desired threshold voltage as illustrated in figure 1.The less obvious though equally important, is the ability to design the gate to drain region such that parasitic Gunn oscillations were quenched. Such oscillations have plagued devices from GaAs MESFETs to AlInAs/GaInAs HEMTs. Figure 2 best illustrates how difficult it would be to achieve such a structure in a vertical configuration.

3. *The parasitic capacitance between the gate and drain (in a source-up device configuration).*
   This problem also plagues bipolar transistors. A gate defined via planarization and etch-back of low dielectric materials mitigate this problem as shown in figure 3. A technology such as angle evaporation is used to define a gate with the gate length a function of the pillar undercut, d_u, the evaporation angle θ, and the depth of the planarized low dielectric constant material. To remove the last variable, buried implant isolation is also a potential solution. The biggest limitation of such an approach is the lateral straggle of the implanted species (typically $\frac{1}{3} R_p$ in cubic materials in the absence of channeling). Since the doping in the channel tends to be orders of magnitude less than the $n^+ -$ region that one is trying to compensate, the implantation process can substantially raise the drain resistance of devices by compensating a fraction of the drain finger. It is easy to imagine that the entire channel can be compensated if the figures are scaled down to dimensions typical of FET channels.

So are the vertical devices really worth the bother? The answer is "Only if they offer something that lateral devices cannot." In other words in my opinion (often wrong), the de-facto choice is a lateral device. Vertical devices have been preferred in applications where

1. Maximizing current density or minimizing device area for certain on-resistance and breakdown voltage specifications is important such as in devices for power switching applications. A related advantage is in the ability to bury high field regions in a well designed vertical device which renders them less susceptible to surface phenomena.

2. When vertical devices offer functionality advantages such as
   a) Threshold uniformity afforded by bipolar transistors for critical analog operations.
   b) The ease of designing and biasing mixed-signal circuits in the zero-threshold, high g_m, f_T and f_{max} space afforded by bipolar transistors.
   c) Linearity promised by Bipolar and Static Induction Transistors (SITs).

Bipolar transistors have thrived especially in mixed signal applications because the layer structures allowed simultaneously scaling of both the vertical and lateral dimensions of the device. The problem of defining the controlling electrode (so difficult in a Vertical FET) is minor in the bipolar transistor as access to the p-type base could be achieved either through doping or etching with isolation from the emitter only an issue for self-aligned base approaches, as shown in figure 4. The use of selective etches to reveal the base accurately has enabled the thickness of the base to be scaled down to $10s$ of nm. The advances in high p-type doping of base materials such as GaAs, GaInAs and GaAsSb using C has allowed this scaling to occur without a penalty in sheet resistance and reduction in contact resistance. Further advances with regrown extrinsic base regions and low resistance emitter regions promise high performance, high levels of integration and reliability in the future.

My experiences guided me to primarily pursue lateral devices and concentrate on trying to incorporate the advantages of vertical devices. The first was the ability to engineer peak electric fields away from the surface in vertical devices. This led to either mimic this advantage (as in the development of the CAVET) or to mitigate electric fields on surfaces (as in FETs passivated by materials grown at low temperatures; LTG-materials or Non-Stoichiometric materials). The CAVET (Current Apertured Vertical Electron Transistor) is shown in figure 5. Here the current flows laterally along a two-dimensional electron gas channel (as in a regular HEMT) but then is collected in the bulk of the device which serves as the drain. An insulating medium prevents a direct short from the source to the drain and forms the aperture through which the drain current flows. The closest analog to this device is the DMOS in Silicon. The peak field in these devices is indeed in the bulk (as shown in the figure) and problems associated with large surface fields such as dispersion in GaN HEMTs were eliminated. In the case of LTG-GaAs passivated MESFETs the intent was to reduce surface fields by providing states close to the edge of the gate into which electrons could tunnel under high field conditions. This relieved the peaking of the field at the edge of the gate and enabled the breakdown voltage to be increased substantially. It is understandable that the nature of the states (energy level, frequency response, and density) which is controlled by the growth

conditions in MBE would impact the device performance. GaAs MESFETs with power density of over $1W/mm$ were achieved using this technique using optimal LTG-GaAs overlayers.

As a final example of the indelible link between materials advances and device enhancements it is worthwhile presenting our experience in the development of AlGaN/GaN HEMTs. In contrast to conventional materials, the wurtzite phase of GaN (the more stable and currently technologically important phase) is highly polar. Figure 7 shows the schematic of Ga-face GaN, the crystal orientation obtained by MOCVD growth. The associated crystal polarization is shown in figure 8 and the nature of polarization at an AlGaN-GaN interface is shown in figure 9. The resulting two dimensional electron gas in this system screens the difference polarization, $P(x)$, and studies have shown that the source of the electrons are surface donor states and active donors in the AlGaN layer are not required for channel formation. The lack of a lattice matched substrate requires heteroepitaxy and hence, point defects, dislocations, thermal management and surface state management all combine to determine device performance. Figure 10 charts the history of HEMT performance enhancement and links it to crucial materials advances. These are in chronological order:

1) Growing a HEMT structure with a thin GaN buffer layer on sapphire (so as to remain insulating) and demonstrating the first microwave output power from AlGaN/GaN HEMTs.

2) Improving the output power via improved thermal management, achieved by growing thick thermally conductive GaN buffer layers. This required developing a technique of growing high quality insulating buffer layers on sapphire.

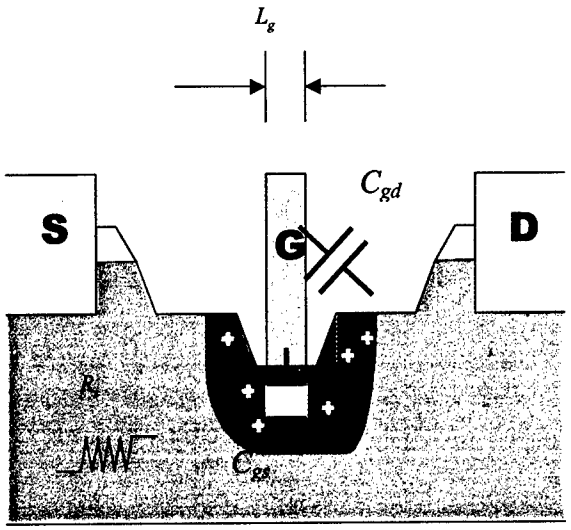
3) Next, a substantial enhancement in output power was achieved by reducing point defects close to the channel by modifying the growth conditions.

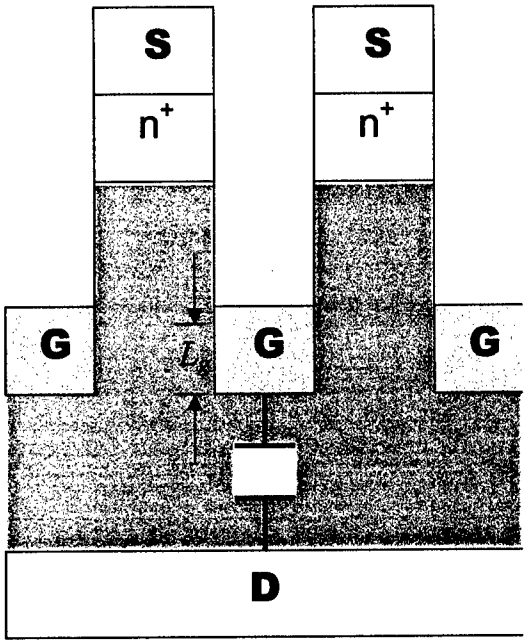
4) The last advance on sapphire substrates was achieved by applying a SiN passivating layer to the device resulting in an output power of $6.6W/mm$ on sapphire, which remains the state of the art.

5) Applying an AlN interlayer between AlGaN and GaN to reduce alloy scattering and implementing the structure on thermally conductive SiC allowed the development of devices with over $8.4W/mm$.

CONCLUSIONS:

I hope that the attempt to generalize classes of devices in this paper has not resulted in any gross misstatements. It represents my attempt to weave my experiences into a story than firm scientific fact.





FEATURES:

- +/- GATE LENGTH Lg DETERMINES DEVICE PERFOMANCE
- + ABILITY TO RECESS DECREASES SOURCE AND DRAIN RESISTANCE AND PREVENTS GUNN-DOMAIN RELATED INSTABILITIES
- + ACTIVE DEVICE CAPACITANCE IS PARALLEL-PLATE WHEREAS PARASITIC/FEEDBACK CAPACITANCE ARE FRINGE.

- + VERTICAL DIMENSIONS ARE EASILY AND ACCURATELY CONTROLLED BY MBE/MOCVD
- + MAXIMUM FIELD CAN BE ENGINEERED TO BE IN THE BULK
- + BAND ENGINEERING IN THE DIRECTION OF CURRENT FLOW IS READILY REALIZED
- - DEFINITION OF THE GATE IS DIFFICULT
- -PARASITIC AND FEEDBACK CAPACITANCES ARE PARALLEL PLATE IN NATURE.

Figure 1 Comparison of lateral and vertical devices.

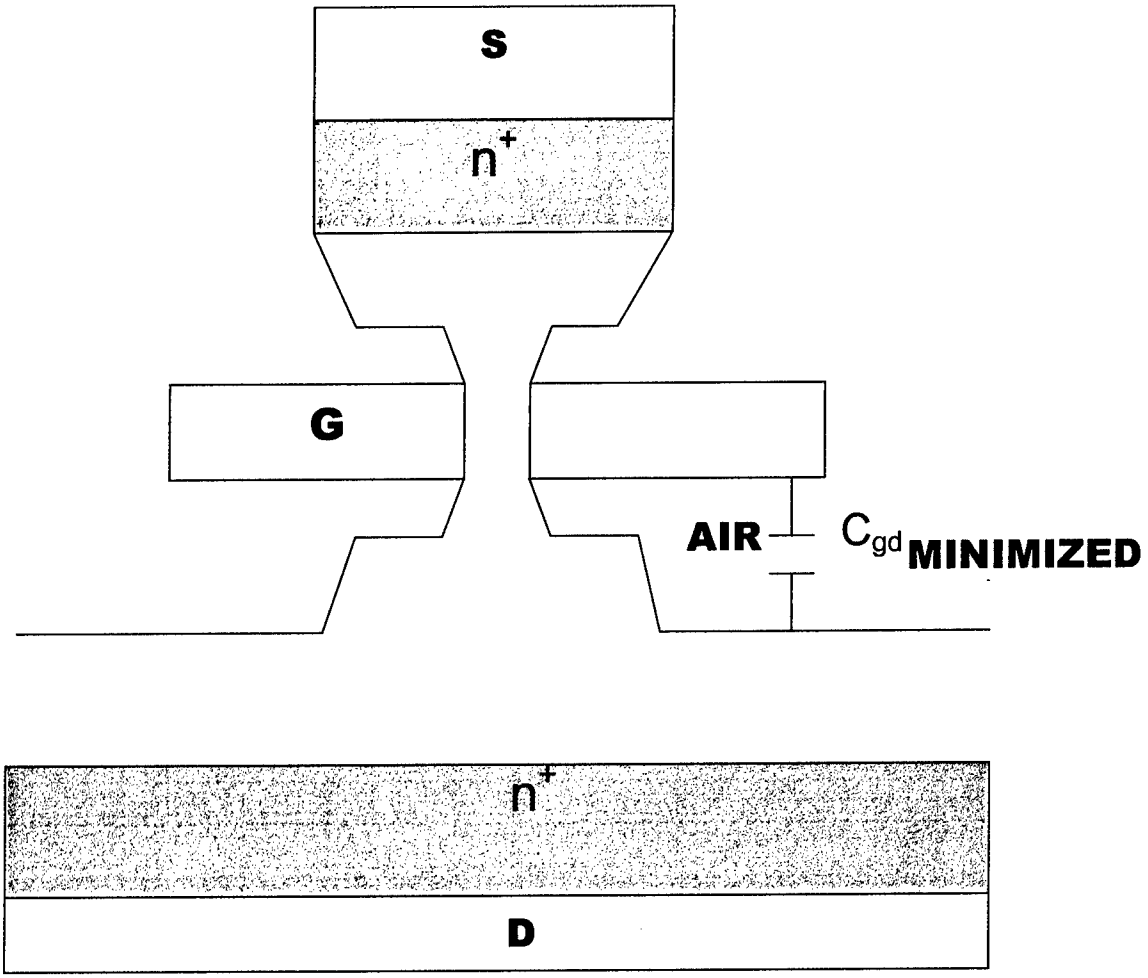
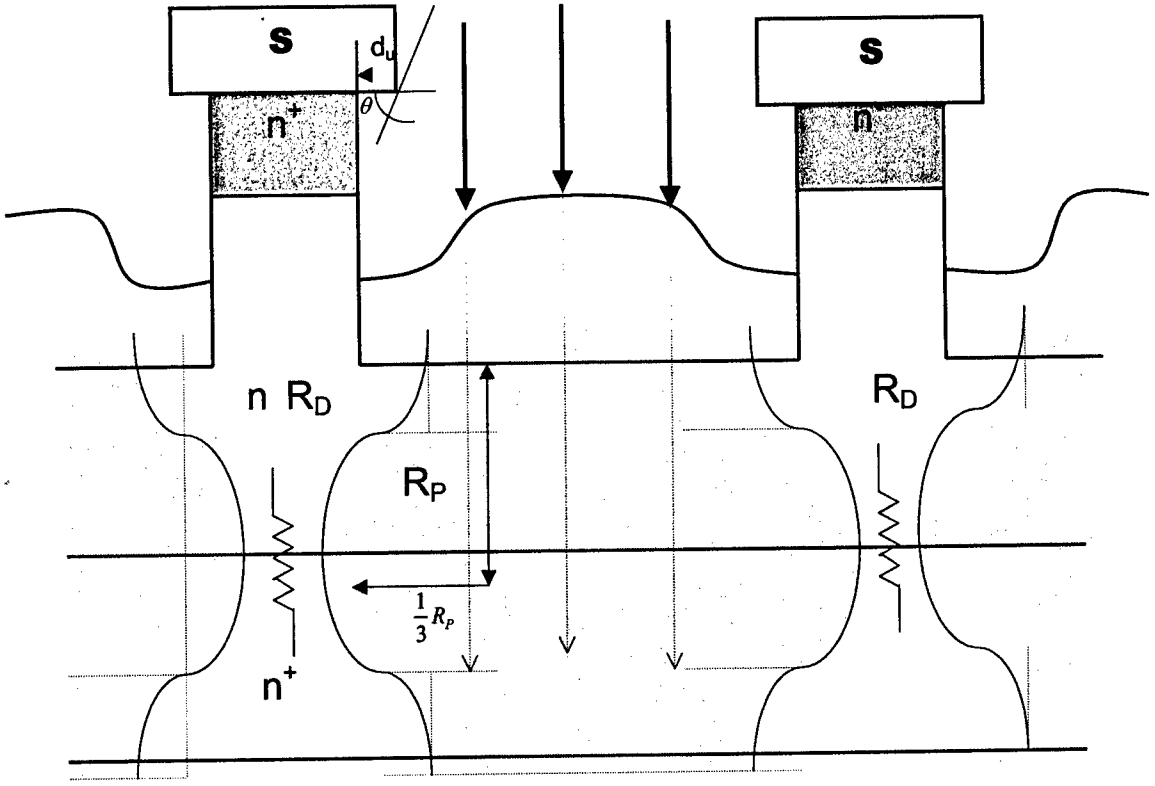


Figure 2 An ideal vertical FET with the complexity of its fabrication pictorially apparent.

ISOLATION IMPLANTATION



+RELIEVES SENSITIVITY TO PLANARIZATION.
- THE LATERAL STRAGGLE OF THE IMPLANTED SPECIES CAN CAUSE AN INCREASE IN THE DRAIN RESISTANCE AND RELIEVES SENSITIVITY TO PLANARIZATION (IN EXTREME CASES CAN PINCH-OFF THE CHANNEL).

Figure 3 Schematic of method of gate definition in vertical FETs using implant isolation for reduction of parasitic gate-drain capacitance.

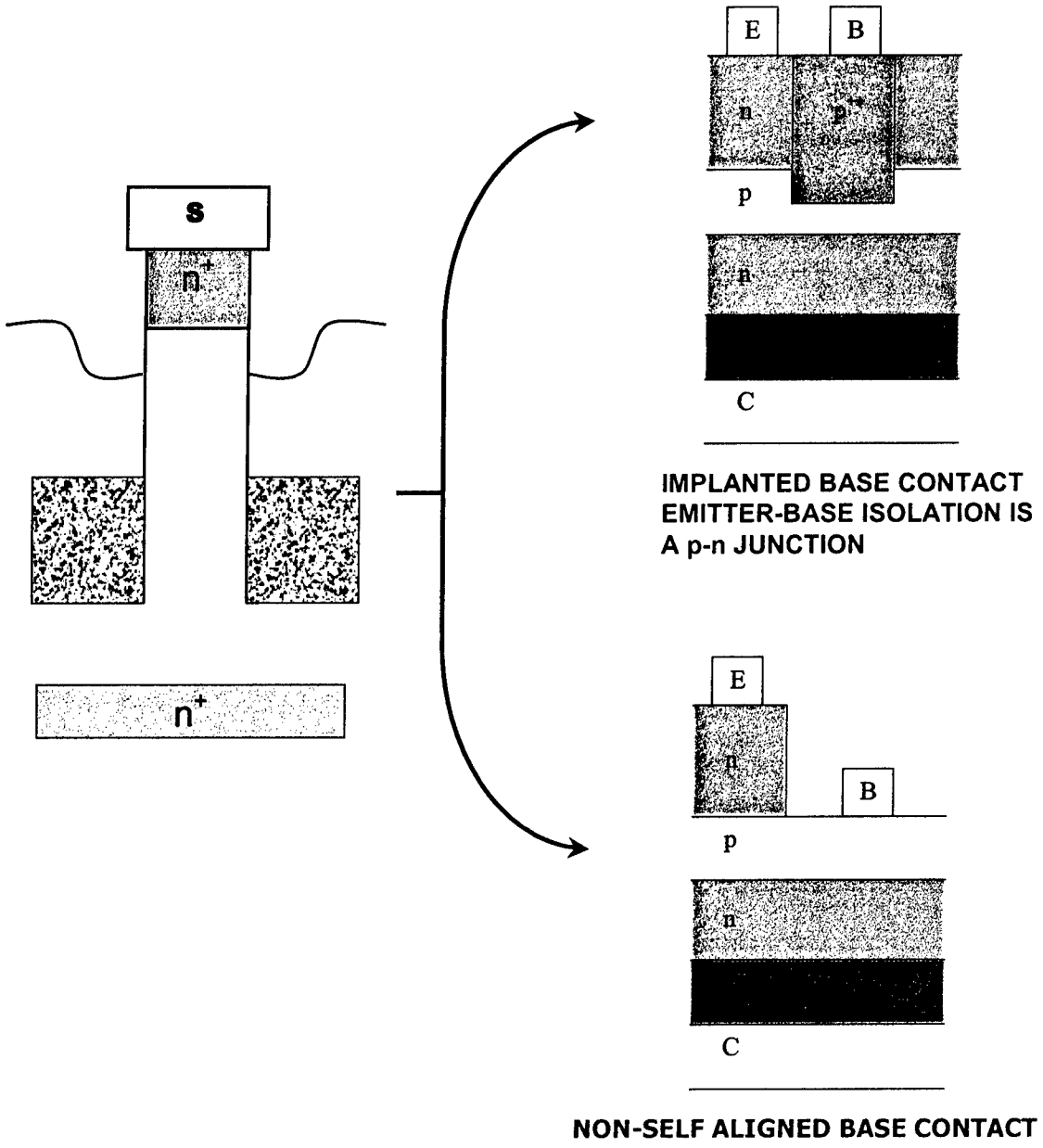
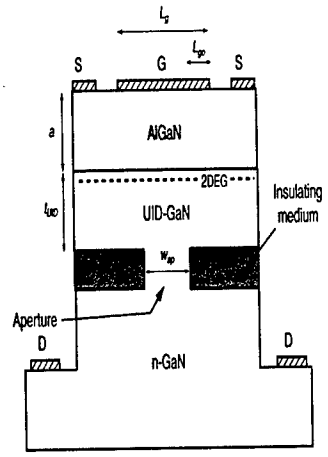
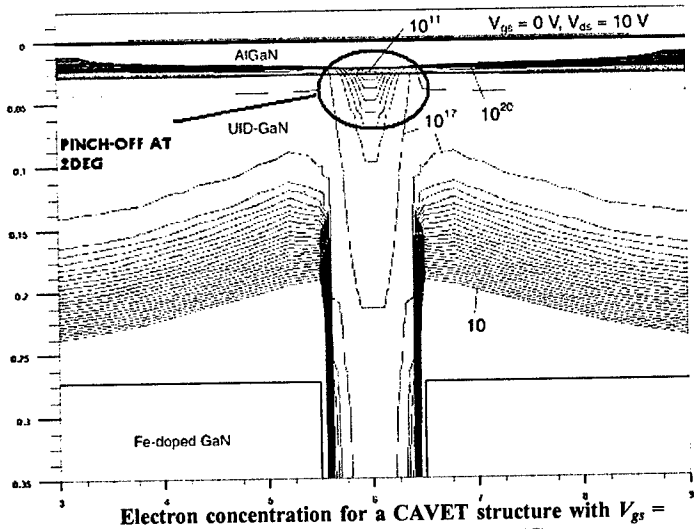


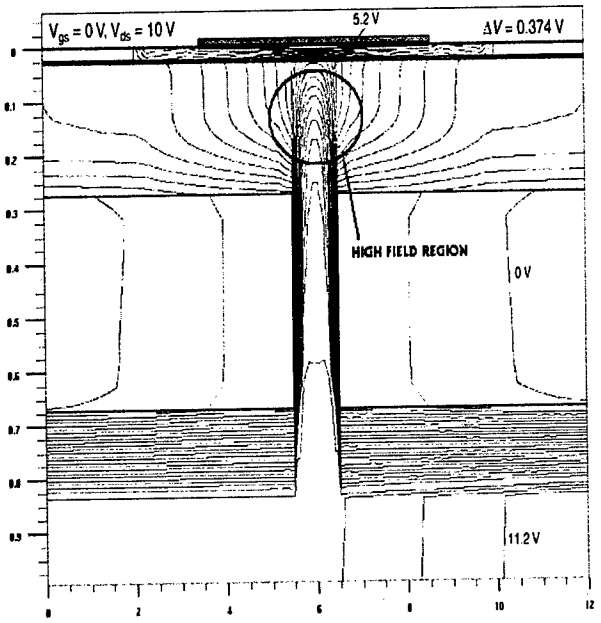
Figure 4 Advantages of bipolar transistors required for success in vertical configurations.



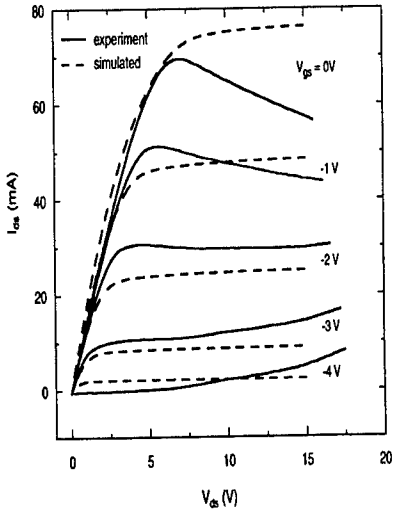
Cavet Structure



Electron concentration for a CAVET structure with V_{gs} = 0V, V_{ds} = 10 V, showing pinch-off of the 2DEG.



Equipotential lines of a CAVET structure with V_{gs} = 0V, V_{ds} = 8 V.



Experimental and simulated *I-V* characteristic of CAVET

Figure 5 The Current Apertured Vertical Electron Transistor (CAVET) demonstrating buried high field regions.

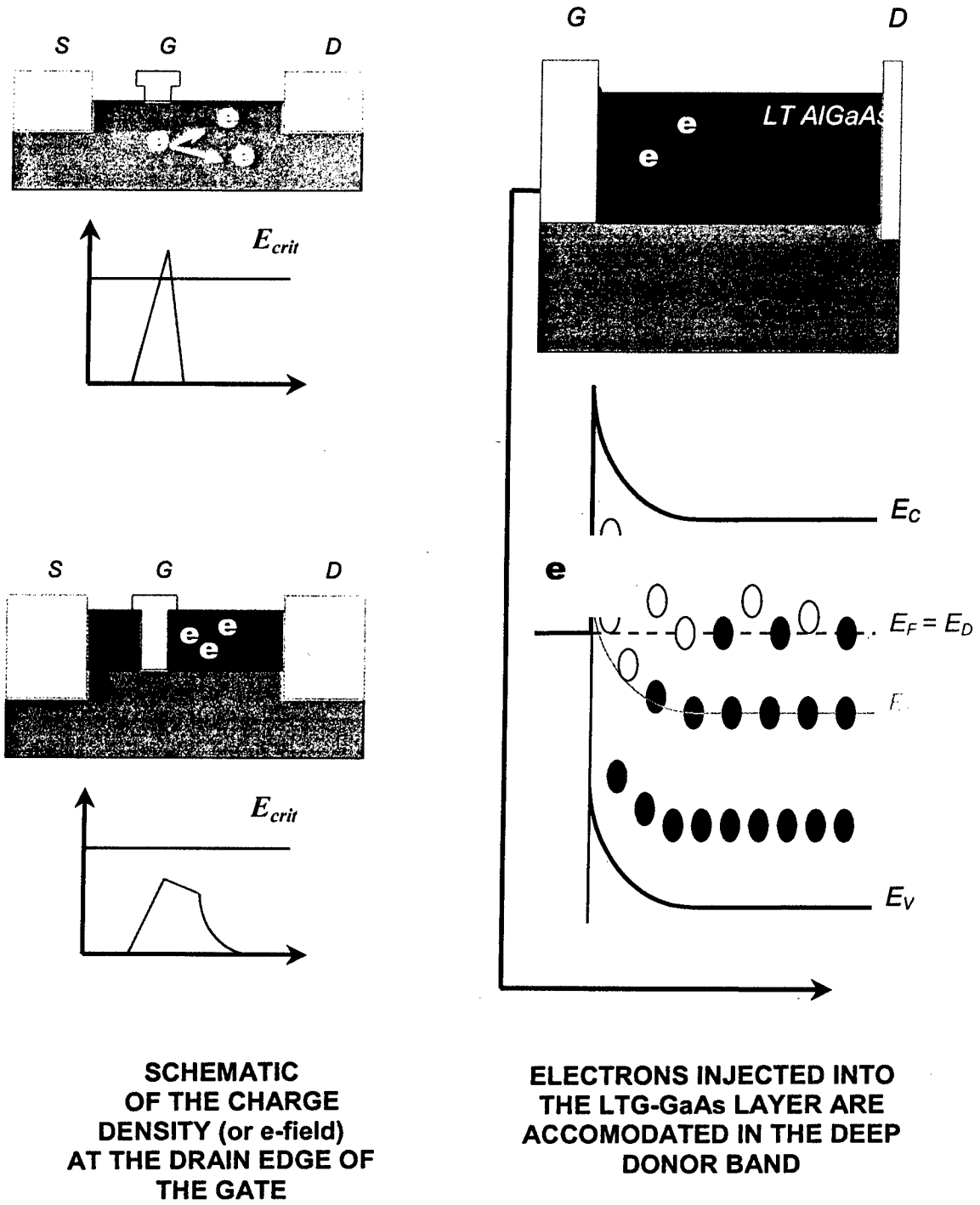


Figure 6 LTG-GaAs overlapping gate schematically illustrating surface electric field alleviation.

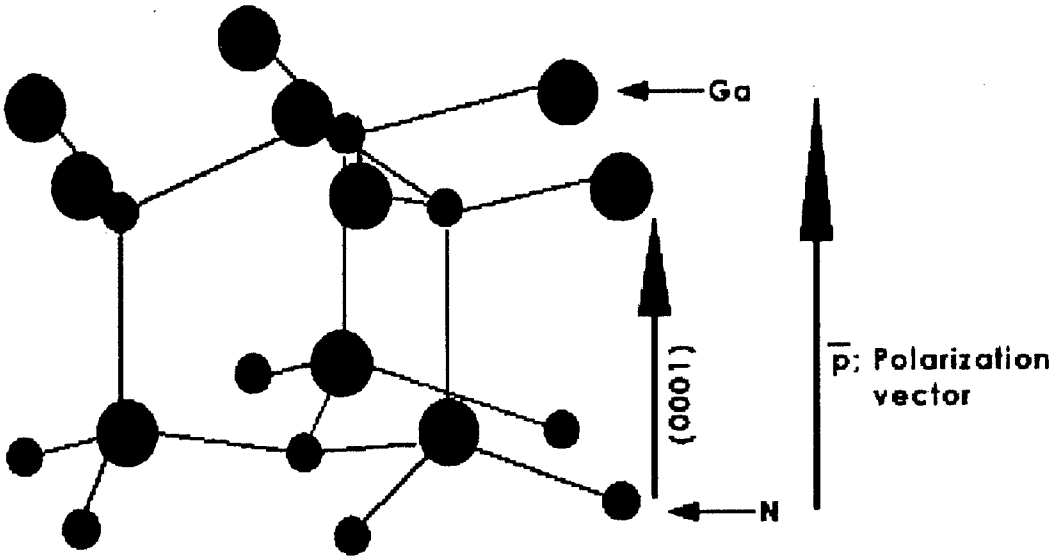
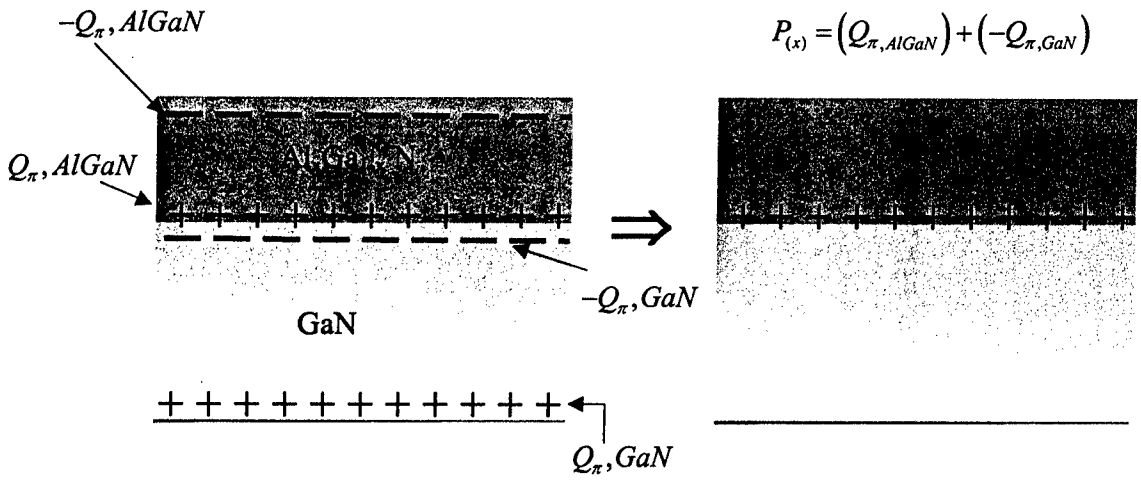


Figure 7 Ga-face GaN wurtzite crystal.



Q_π includes the contribution of spontaneous and piezo-electric contributions

Figure 8 Polarization in bulk GaN and at AlGaN/GaN interfaces.

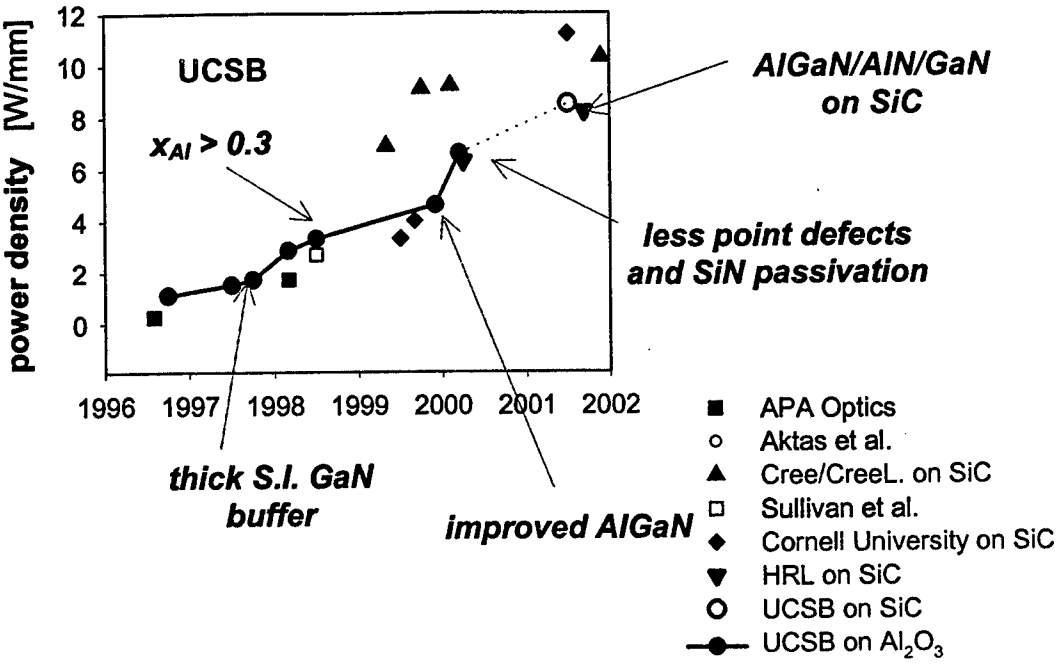


Figure 9 The direct relationship between materials improvements and AlGaN/GaN HEMT device performance as evidenced at UCSB.

The Status of Fiber Optics

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The past decade has witnessed dramatic changes in the communications industry and specifically the fiber optics industry. The markets, technology, and manufacturing infrastructure have gone through what may be one of the greatest expansion phases and the corresponding consolidations. Companies like Worldcom were formed, grew to be comparable to AT&T and have now filed for protection under bankruptcy law. In this paper, I will discuss some of the issues from a market and technology perspective that lead to these changes.

The single greatest enabling technology of the fiber optics industry was the erbium doped fiber amplifier (EDFA). The EDFA was developed in the 1990 time frame and with its development came a technology that was able to amplify 100's of optical channels simultaneously at a cost structure orders of magnitude below that of regeneration. Two technologies were necessary to realize the EDFA, the Er doped fiber and the high power semiconductor lasers used for pumping of the fiber. Initially the fiber was pumped exclusively by 1480 nm lasers as they were more reliable in the early 1990's, however through process improvements, reliable 980 nm lasers became the dominant pump source for EDFAs as 980 nm lasers enable high channel count, low noise EDFAs.

These initial innovations resulted in the deployment of EDFA technology in both undersea and terrestrial systems. Their benefits of cost structure far outweighed the downside of only being a 1R device. In the 1995-6 timeframe companies like Ciena, Lucent and Pirelli started aggressively deploying dense wavelength division multiplexed (DWDM) systems operating at 2.5 Gbits/sec/channel. Nortel subsequently pushed the data rate to 10 Gbits/sec and became the dominant supplier of DWDM transport equipment.

Also, in the 1995-6 timeframe, the fiber plant was dominated by SMF fiber and the transition from the regeneration systems to the EDFA based systems, in conjunction with the expansion of the internet, caused a massive buildout of networks. Key dynamic changes happened in the pre and post 1995 timeframe including the deployment of high fiber count cables. Prior to 1995 most deployed cables had less than 24 fibers in them, after the 1995 timeframe most newly deployed fibers had channel counts of 144 fibers, and in the metro networks fiber counts of 900 fibers were being deployed. This was economical as the cost of deployment was dominated by construction costs and not the cable itself. As a result, the problem of maximizing the capacity in the fiber, which existed in 1995, does not exist now.

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Several key technologies, other than the EDFA, were also critical to the development of the fiber optics business. These included LiNbO based modulators for controlled chirp 10 Gbit/sec transmission, dispersion management via dispersion compensating fibers to manage the analog characteristics of the EDFA based system, and optical muxing technologies. Second generation advances included the demonstration of Raman amplification, which was the enabler of ultra long haul networks, and 40 Gbit transmission technologies for even greater capacity benefits.

In the 2000-2001 timeframe, the economic infrastructure of the fiber optics industry began to unravel. With over $700B invested into communications in the second half of the decade, it became apparent that much of the build out was financed by investors and not through consumer spending. The consumer demand, although growing at 100% per year, was not sufficient to justify the level of capital infrastructure that was implemented. The current state of the market is such that the highest order bit is cost reduction. The market can no-longer support the cost infrastructure and is therefore dramatically limiting the expansion of the networks.

The challenge of the network in the future will be to drive dramatic cost reductions through both better manufacturing infrastructures and better technology choices. It is my opinion that the next phase of the fiber optics industry will be one where the advantages of Si electronics contribute to a lower cost structure. The first areas where Si will impact will be in the incorporation of FEC and electronic equalization. These two technologies can solve as much as 12-15 dB of the link budget. This will enable the optical manufacturer to choose technologies that are lower in performance and therefore lower in cost. The net result will be a resurgence in the industry as the cost infrastructure will become commensurate with the elasticity of the market.

In conclusion, the fiber optics industry has been driven by innovation. Much of this innovation was based on basic materials and device development. The interplay of materials science and device design has resulted in this technology revolution. I would like to thank my thesis advisor, Lester Eastman for his insight into this relationship between materials and devices and his undaunted enthusiasm for innovation.

Three-Dimensional Integration in Silicon Electronics

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Abstract:
As silicon electronics reaches length scales of 100 to 10 nm, device densities of 10^9 to 10^{11} cm^{-2}, interconnect densities of 10^{10} to 10^{12} cm^{-2}, and applications across the spectrum of digital, analog, and mixed-signal domain, a number of key issues arise related to maintaining the improvement in performance, cost, power, and designability. Three-dimensional integration incorporating planar transistors offers interesting new directions for continuing improvements. Adaptive modifications of the planar transistors offer higher scalability and functionality, higher vertical interconnectivity in between device planes can reduce interconnect delays, higher programmability using configurable elements can provide efficient signal and energy flow, higher digital-analog isolation using ground-planes can provide cross-talk improvements for mixed-signal applications, and a power-aware design can allow control of temperature and power dissipation.

Introduction:
There is considerable discussion these days of end of scaling[1-3] and the search for solutions[4-8] beyond the perceived limits of silicon devices. These proposed solutions extend from the use of molecules, DNA, quantum, as well as others that extend the nanostructures-oriented technologies. With this advent of dimensional limits, silicon electronics is entering an interesting era requiring unusual solutions. Underlying this discussion is the question: Why do we need this near-infinite electronics? We do, because, if at a reasonable cost, electronics can continue to help make our life more fun, make chores easier, help us communicate far and wide, make information gathering and dissemination easier, help governments govern and protect, help citizens maintain their freedom and express their opinions, and help scientists and engineers solve fascinating problems, etc., than there is need for it and use for it. One of the important aspect of this high integration and technology complexity is that it allows for an enormous amount of complex information processing, which in turn make the instruments easy to use for the human being, thus producing the demand that drives this industry. High integration, excellent human interface, and high speed information processing is key to success in all these areas, and silicon electronics is the base for the general-purpose solution.

The issues of the high integration are, however, multi-faceted because they are based on interrelated questions of technology development, circuit and architecture development for performance and power, and of systems implementation, all within the criteria of affordability. In technology, these questions relate to the variety of device technologies that can now be found in silicon electronics. Multiple threshold voltage transistors as well as off-chip drivers, transistors for analog or high frequency operation, memory structures for non-volatile(NVRAM) or low power with high density (DRAM) or fast (SRAM), all require quite different practice of silicon technology adding up the costs of the

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processing. To usefully employ the electronics, one needs to mix many of these technologies. Almost all integrated chips with any digital processing require at the least a fast memory with logic with the microprocessor being a very common example. However, many of the newer applications – the video games and digital cameras, the mobile phones, the networking equipment for data transmission, the controllers in automotives to printers, etc., all require mixing of multitudes of these technologies, and in order to design in an acceptable time, require reuse of functional elements of the design. This system-on-chip approach has allowed inexpensive design, and electronics affordable, but with technological complexity inherent in implementing different structures on planar silicon. Interconnections and devices need to scale together in order to truly benefit from the scaling of dimensions. Interconnect for short paths lead to RC delays, while for longer path lengths transmission line delays occur. The increase in interconnect density, the reduction in cross-section area and hence an increase in resistance, and limits in reduction of the capacitance, has led to increasing difficulties with reducing interconnect delays. Long paths typically have a reach of 0.15 mm/ps. For clocked designs, such as microprocessors, this means that ~100 ps latency exists in the longest interconnects of a chip. Clearly, there are a number of ways, either separately or together, that electronics can employ to chip away at these issues. Three-dimensional(3D) integration is one of these as it provides ways by which different technologies can be integrated together, ways by which it can provide higher interconnectivity through the use of vertical interconnections, ways by which it reduce signal path lengths and provides compactness, and ways by which it allows non-silicon technologies (passives, polymer-based, other inorganics: III-V, chalcogenides, etc.) and structures to be integrated.

Looking from the perspective of applications, there are multitudes of ways in which the evolution of electronics usage is likely to occur that three-dimensional integration can help with. Consider the large usage of RF in mixed-signal applications. Cross-talk, i.e., coupling of digital signal to analog elements and the need to employ a largely digital transistor design for a high frequency element are two such issues. 3D addresses these by allowing the use of ground planes to isolate electric coupling and allows freedom in design of the analog elements, such as a transistor with a metal gate to reduce gate resistance, by placing these devices on a separate device plane. In computing, embedding memory, use of large caches to reduce cache-miss penalties, use of specialized embedded DRAM processors with large data manipulation capability, reducing the longest and the average interconnect lengths, use of high interconnection grid in a symmetrically-multiprocessor with a cellular architecture, are few of the ways by which systems can be improved in performance while taking advantage of their density.

In this paper, we will discuss some specific examples of technology and structures that benefit from the 3D integration.

Silicon Layering[9]:

Figure 1 shows a simplified diagram of the two possible ways by which one may implement silicon or silicon device layering. There are two paths to layering of wafers. In sequential processing, a silicon layer is formed on top of a processed wafer. While there are a number of processes that are being researched for this (laser recrystallization, nickel-based crystallization, epitaxial layer overgrowth), the way we implement our structures is by exfoliation. In exfoliation, a large dose of hydrogen and co-implanted species are placed inside the silicon wafer (~μm underneath the surface by implantation), and smooth surfaces of wafers attached by room temperature bonding. After strengthening of this bond, when the temperature is raised again, due to the low solubility of implanted species in silicon, the crust of silicon delaminates from the rest of the wafer and remains attached to the bonded surface. This allows, quite remarkably, an entire surface of wafer to be transferred to another wafer. The parallel processing does not allow such a process to be implemented easily because large doses of hydrogen will have unacceptable effects on reliability as well as operation of the devices. So, the preferred method in this case would be to fabricate devices in silicon-on-oxide (SOI) wafers and then use the oxide as the back-stop for the etching and layering process using a handle wafer. The first technique allows us to use our traditional lithography and processing with its similar resolution and registration. This means that the sequential processing technique allows us to achieve very high density interconnectivity in between planes at a pitch similar to that of the first level metal. The trade-off is that during the processing of the second layer, the first layer sees high temperature processing. The second process involving layering processed wafers, and hence has mechanical limitations of alignment for bonding as well as across-wafer registration effects. But, these techniques together allow us to develop and demonstrate interesting new structures.

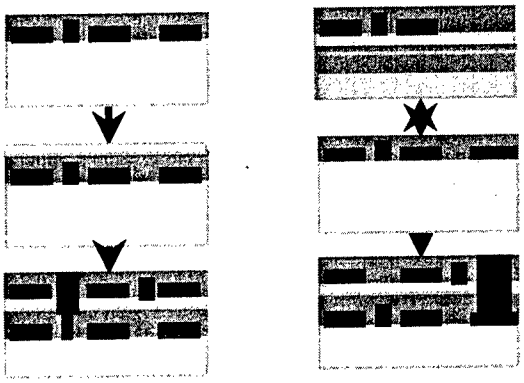
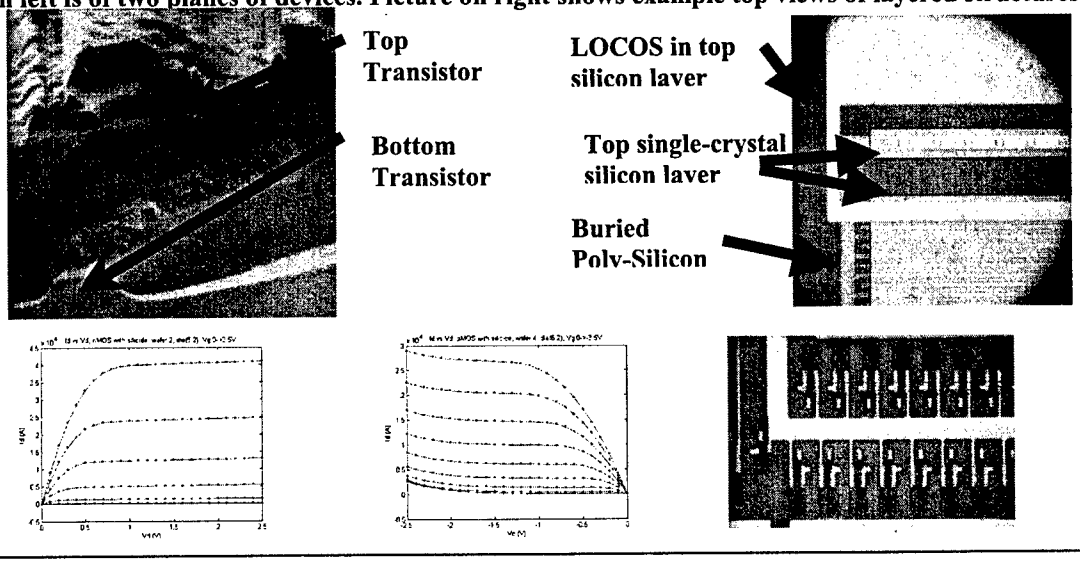


Figure 1: Sequential (left) and parallel (right) silicon layering. In the former, thin film of silicon is layered on top of a processed wafer, while in the latter processed silicon device layers are stacked.

Layered CMOS[9]:

The ability to place the single-crystal silicon on top allows us to therefore continue a CMOS fabrication process. In the devices, the bottom silicon – silicon dioxide interface is a thermally grown interface, and hence the CMOS structures maintain a good interface-state density. Critical to reproducible and high-performance fabrication using this technique is the ability to obtain a reproducible silicon layer thickness. The silicon structure following exfoliation is rough (10's of nm) and needs to be chemically-mechanically polished, an essential part of reproducible bonding because of the emphasis on requiring smooth interfaces. Fig. 2 shows examples and characteristics of structures fabricated using the sequential processing described.

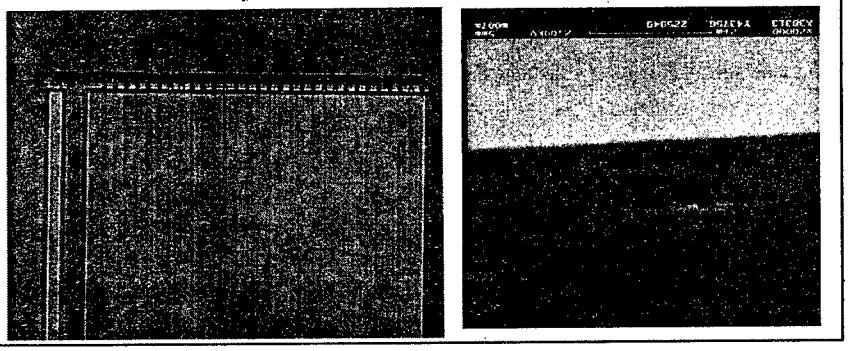
Figure 2: 3D planar CMOS structures fabricated using the single crystal layering technique. Picture on left is of two planes of devices. Picture on right shows example top views of layered structures.



Layered CMOS with Buried Metal[10]:

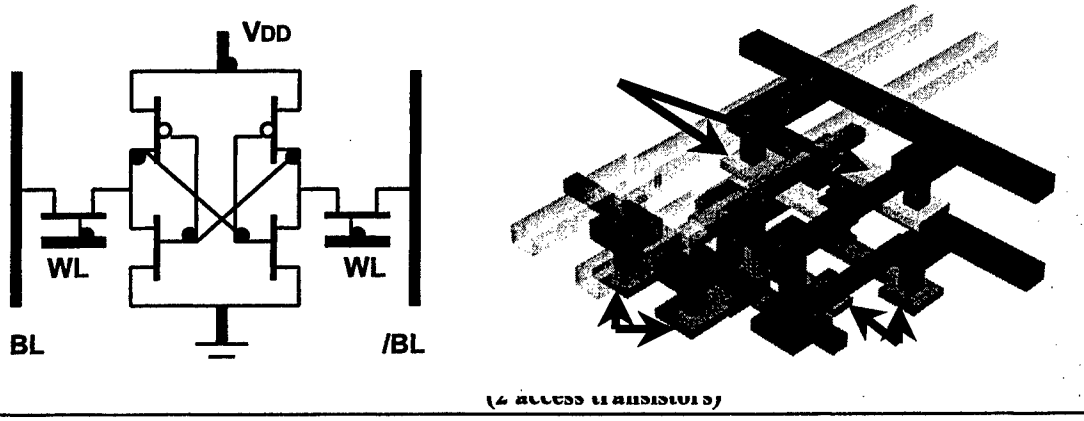
Resistance of the interconnections is extremely important because of the resultant RC effects. Planar CMOS today, e.g., employs 8 levels of metal interconnects in order to achieve interconnectivity with the appropriate delay. In silicon technology, one usually does not introduce metals required for obtaining low resistances in the front-end of device processing. There is currently considerable research in metal gates in order to appropriate threshold voltage control with acceptable gate resistance at the smallest dimensions. Usually with these structures, high temperature processing is minimized and restricted to temperatures below those needed for gate oxides. We have been utilizing tungsten, deposited from tungsten hexacarbonyl, as a high temperature layering and CMOS processing compatible material in our 3D technology. While tungsten does oxidize, the W-Si-O system is highly stable, so the processing must protect the tungsten through encapsulation in order to take advantage of the stability of the ternary system. A cross-section of such buried tungsten is shown in Fig. 3.

Figure 3: Buried-tungsten 3D structures. On the left is a capacitor structure with oxidation-isolated silicon region on top. On the right is a cross-section of such layered structures.



Applications: SRAMs [11]:
Static random access memories are ubiquitous in silicon electronics because of they are fast, based as they are on a simple flip-flop or cross-connected pair of inverters, utilizing CMOS as it exists for the logic. However, SRAMs typically utilize 6 transistors (2 additional for read and write in addition to the flip-flop which consists of 4 transistors) with a fairly elaborate interconnect structure (Fig. 4). There are a total of 14 interconnections and 28 nodes/vias within the cell of the structure.

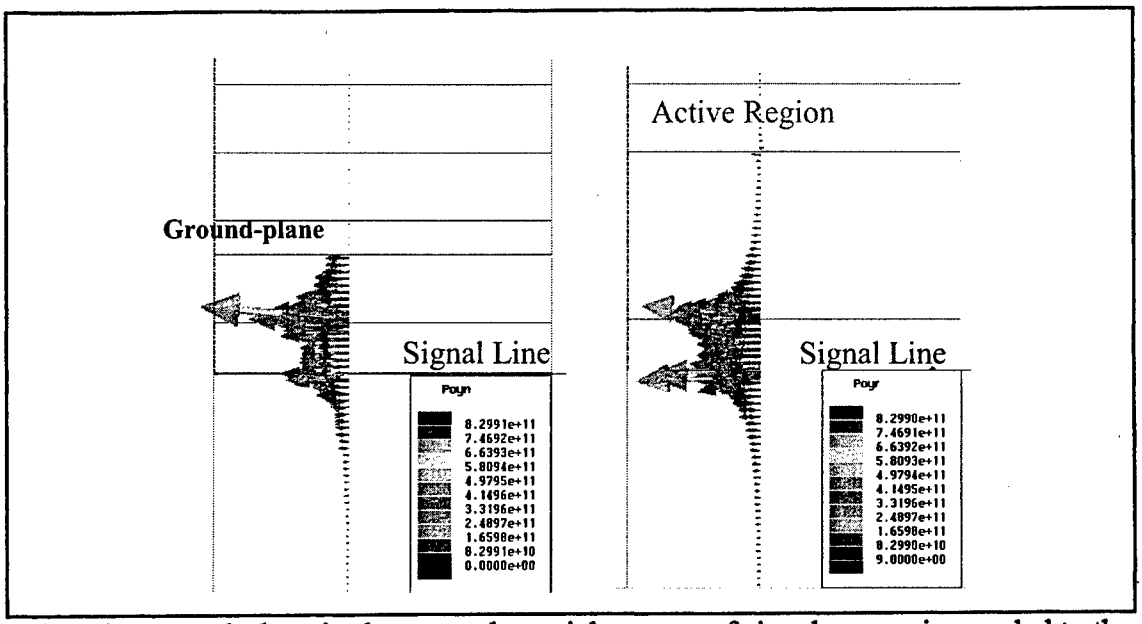
Figure 4: SRAM and one possible layout in 3D. In this layout, the mMOS inverter transistors are placed on the bottom, and the access and p-channel transistors on top.



The consequence of implementing such a structure in planar CMOS technology is that a typical cell uses 80-100 squares of the lithographic feature size. And, much ingenuity in processing goes into collapsing and overlapping the interconnect structure, and cleverly eliminating design constraints in the layout of the cell. Most microprocessors, however, still utilizes half or more of the area for SRAMs that provide the on-chip cache memory hierarchy. Thus, attaining a smaller footprint has significant area-related cost advantages. It also turns out that the smaller area and lower capacitances associated with silicon-on-insulator like technology allows one to maintain good noise margins at low power consistent with achieving high speed. Note, e.g., that in the SRAM cell shown in Fig. 4, there exist CMOS (n- and p-channel) devices simultaneously in the upper device plane, leading, at least in the form as shown in this figure, a two-plane configuration where n-channel devices of the flip-flop to be scalable for a desirable performance feature without sacrificing cell size.

Applications: Mixed-Signal[12]:
We have discussed the partitioning of functions and technology. One interesting example of this is mixed-signal applications where one may wish to design analog and digital functions in separate planes together with changes in the specific implementations of technology. Thus, analog RF structures may specifically address gate resistance issues for obtaining high maximum frequency of oscillations and have a design that provides high linearity. 3D allows one to do this, but also allows added benefits related to the coupling of digital switching noise to analog blocks. Ground planes placed to isolate coupling to the analog elements allow us to achieve this objective. An example of such isolation is shown in Fig. 5 in a simulation that shows the suppression of the energy transfer, using

Poynting vector. In this simulation (implemented using HFSS), the left figure shows a ground plane isolating the active region from a signal line across which the digital signal travels. On the right are the results of the same simulations, but in the absence of the ground plane.

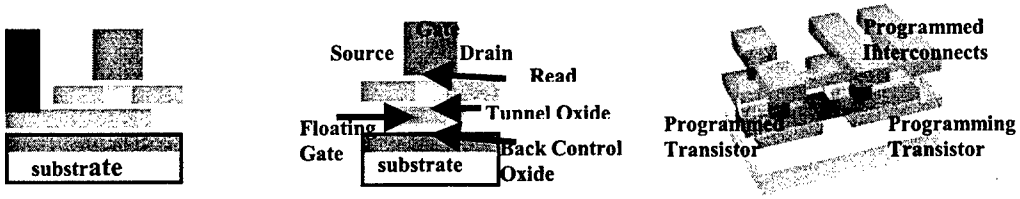


When the ground-plane is absent a substantial amount of signal energy is coupled to the active region, while the presence of a ground plane shadows and isolates the active region. The consequence of an ability to isolate such noise is that very versatile mixed-signal applications can be pursued where analog design plays as large a part as the digital design.

Applications: Adaptive and Configurable Structures[13]:

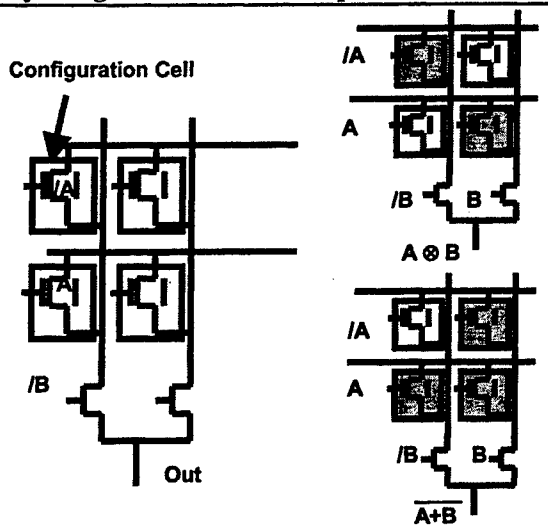
One of the many interesting attributes of three-dimensional structures is the consequence of the availability of the third dimension. An important and significant way that this occurs is the use of a buried gate and a doped substrate. By placing the gate underneath the layered silicon channel, the threshold voltage of the transistor can be modulated, thus providing controllable and adaptive properties to the transistor operation. A floating gate on the back provides a means of storing charge in the floating-gate region, thus achieving a memory using the same transistor technology. This structure also allows us to decouple the constraints of oxide required for reliability and charge retention from the scaling of the transistor for high performance operation.

Figure 5: Buried gate transistor (left), non-volatile memory (center), and configurable switch (right).



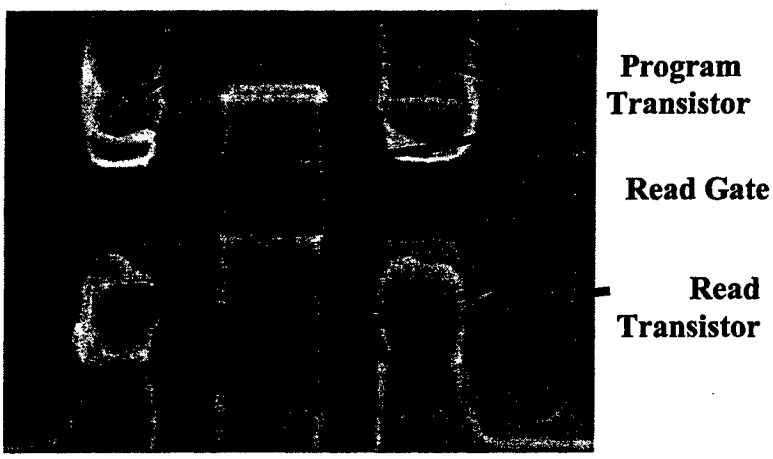
Finally, this same structure with a common floating gate between two transistors provides a method for using one transistor for programming a pass-transistor interconnection using a cross-point switch employing two programming lines. The ability to control the power and speed using the threshold voltage, achieving a non-volatile memory, and programming these properties holds great promise in adaptive power control and configurable designs. Configurable designs that allow functional circuits and tolerance of small defect densities, and designs that allow circuits to perform multiple functions, hold a fruitful area of research and promise in addressing yield and design issues of the large densities. Fig. 6 shows an example for such a back-gated structure implementation where a NOR and XOR functions are implemented using the same 4 transistor circuit using the programmability achieved from the back-gate. Fig. 7 shows an example of a fabricated configurable structure using the 3D approach described.

Figure 6: Configuration cell and programming using back-gate to turn off and on transistor that leads to variety of logic functions to be implemented.



As the device count has increased over the years, and applications have moved from use of few transistors in amplifiers or logic gates, to calculators, servers, and mobile applications, the techniques used in design have shifted from careful hand-crafting to synthesis through automatic tools based on higher definition languages, optimization tools, and a smaller amount of custom manipulation. Extensive use of configurability through software is likely to be an additional step in the continuing evolution towards increasing automation with the integration.

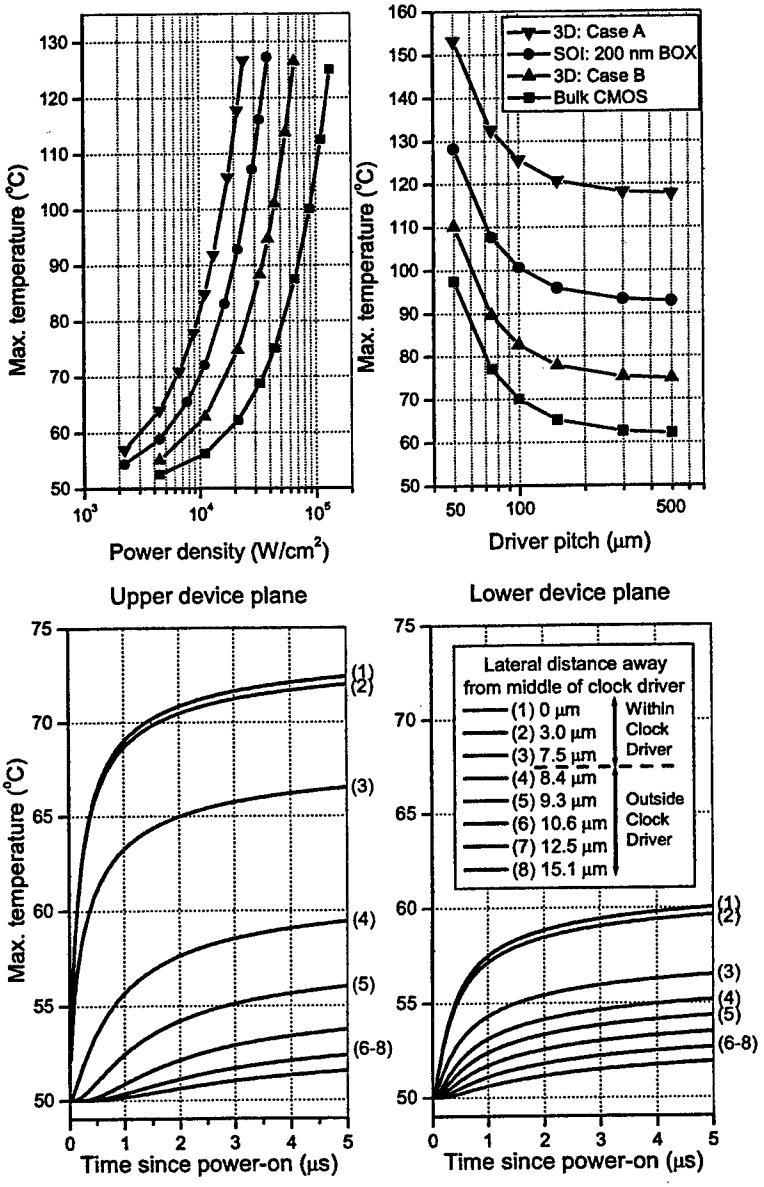
Figure 7: A scanning electron micrograph of a fabricated configurable switch.



Issues with 3D Integration[14]:

That 3D holds much promise is quite clear from the snap-shot provided above. It is quite clearly one possible path to getting beyond the limits set by interconnects and the size limits of field-effect. However, like all research directions, 3D also raises interesting problems that need to be taken care of by design or technology. Besides the development of reproducible technology, two prominent ones are those related to power and yield. These are problems for planar technology too (and silicon-alternatives), but become accentuated in 3D because of limited thermal conductivity of insulators (SiO_2 is nearly factor 100 worse than Si), and the yield limitations of a new technology. It is projected that by the end of this decade, manufacturability would be sufficiently advanced to make 14 cm^2 as the ideal cost-effective size of a chip. Our lithography tools and lateral connectivity delays typically constrain us to work within a foot-print which is at most 2.5 cm on the side, except in specialized applications such as CCDs, etc., where steppers strap the interconnects at the edge of each chip. If these predictions are really true, they seem to indicate that at least 2 or 3 layer 3D circuits should be feasible with reasonable yield within the 2.5 cm x 2.5 cm footprint.

Figure 8: Clock driver related behavior in 3D. Figure on top shows temperature as a function of power density and driver pitch effect in a variety of silicon implementations. The figure on bottom shows the time-transient effect due to heat propagation in 3D structures.



The thermal issue, however, is more bothersome for all electronic designs. In particular, the acuity of this problem arises from synchronous design style that is mainstay of technology today.

Clocks, usually distributed across the chip, consume nearly 70 percent of the power so that the slew is small and the entire chip operates closely in unison. Clock drivers are individual transistor elements with large drive capability, and therefore are the highest power density elements and show the highest temperatures in a chip. Use of SOI technology has led to an increase in these temperatures because the oxide underneath conducts heat poorly. Figure 8 shows a calculation of the temperature rise and time transient effects in clock drivers which is representative of silicon technology at 180 nm dimensions.

These figures show that heat propagation causes unusual effects. Temperatures can be significantly higher because of conductivity effects, and time delays occur because of slow propagation. However, there are interesting advantages also visible in these calculations. Interconnectivity in between planes places elements of high thermal conductivity between the planes. These have the attribute of mitigating the effect of the oxide. Thus, small interconnect lengths, e.g., the case B of Figure 8, actually improves on the SOI case because the small interconnect lengths behave as heat pipes for extracting the heat away from the top plane. The bottom figure shows that the upper device plane with heat propagating laterally due to the oxide heat barrier underneath, shows delay effect in the thermal transient. Thus, one implication of this behavior is that one would have to carefully look at the heat dissipation properties as one partitions the functional and technology design of the 3D implementation.

Other Comments:
We had discussed the two possible pathways to 3D integration – either as sequential with the dense interconnectivity or parallel with lower interconnectivity. Lower interconnectivity clearly has implication from the heat perspective, but it also allows a bus-oriented design such as for system-on-chip applications. The biggest care one has to exercise in such applications is that heat dissipation is controlled and that one designs to take a large advantage of the high interconnectivity bus. Embedded DRAM, or SRAM, integrated to logic, or mixed-signal design combining analog and digital planes, are two examples of such application. The sequential, on the other hand provides wider density-oriented freedom, but at the cost of the higher temperature effects of processing.

Summary:
I hope to have provided a rather diverse view of what 3D technology entails in its promise for devices and circuits and what the limitations of the technology appear to be at this moment in time. The approach to silicon's dimensional limits does not mean that we have reached the end of what we can accomplish with silicon. Higher integrations, low interconnect penalty, new design styles, and high volume and area efficiency that 3D integration will provide is likely to lead to continuing evolution in silicon applications.

Acknowledgements:
This effort has benefited tremendously from the support provided by DARPA (N66001-00-C-8003) through the AME and HGI program and Cornell-IBM (D. J. Frank, K. Guarini, and R. McFeely) collaboration. Additional support from NSF and SRC has been

instrumental in exploring new applications for the 3D approaches developed. Cornell Nanofabrication Facility was vital for the fabrication effort.

Finally, ST wants to express his gratitude to Prof. Les Eastman, in whose honor this conference is named, for being a tremendous example as a teacher and a world citizen, and for his cultivation of science and engineering. The environment, and the research freedom that he provided to his students has been instrumental in our own successes and a guiding example for us in our own development and growth.

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30 Years of Accomplishments in Compound Semiconductor Materials and Devices Attributable to Prof. Lester F. Eastman

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Abstract:

To those that best know him, Prof. Eastman is not only one of the most congenial academicians in the world, but is a walking encyclopedia of knowledge relating to compound semiconductor materials, structures, and devices. Moreover, he is always most willing to enthusiastically share the details of his knowledge. His personal contributions to the field are multitudinous. He has mentored over 110 successful Ph.D. candidates. Eighteen of these have founded new businesses, 19 have become academicians, 16 have become Directors, Managers, CEOs, or VPs in industry, one is currently the associate director of the FBI, and 3 have already retired. Three hundred eighty seven of his over 700 papers have been cited in the Science Citation Index with 9 of them having over 100 citations each. His earliest cited paper was published in 1964.

In this paper several of his traits and accomplishments along with their impact on his students, the DoD, the scientific community, and our standard of living will be highlighted. Projections are also made of future impacts.

I. Introduction

To members of the compound semiconductor community, Professor Eastman and his works hardly need an introduction. The enthusiasm with which he addresses a topic at any workshop, conference, or seminar renders that meeting a memorable event for those in attendance. His contributions span a sizeable number of scientific and engineering fields. Among them are vacuum tubes, transferred electron devices, short gate FETs and associated technology, heterojunction FETs, Ballistic transport devices, planar doped barriers, high speed lasers, wide bandgap semiconductor materials and structures, and the exegesis of various electron device phenomena. Selected areas are highlighted herein.

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II. Transferred Electron Devices

Gunn oscillators were well known by 1976, but they were not noted for generating much output power. Among his first endeavors that actually transitioned into military hardware was the Limited Space charge Accumulation (LSA) high peak power oscillator.[1,2] This device is believed to be the first solid state semiconductor device capable of generating pulse power in excess of one kilowatt in a single device in X-band. Fabricated by his start up company Cayuga Associates, it was deployed during the Vietnam conflict as a beacon permitting the rescue of downed pilots. This device also had what was first believed to be quite a detriment: the frequency was dependent upon the temperature of the device thereby creating a chirp signal. Lemonade, however, was made of this lemon and the first known covert microwave spread spectrum microwave communications system was generated.

III. Short Gate FETS

Prof. Eastman instilled in his students the benefits of teamwork. He was himself one of a team of faculty members receiving the NSF award for the National Resource and Research Facility on Submicron Structures (later to become the Cornell nanofabrication facility after 1977.) The close proximity of this facility and the electrical engineering school and the teamwork among these two groups enabled the demonstration of 0.25 micron gate length HEMTs yielding the lowest value (0.87 pF/mm gate width) ever reported for a HEMT.[3] The cutoff frequency f_T was 45 GHz or 10 GHz higher than for previous 0.5 micron gate length devices – this in spite of mediocre source resistance. Still shorter gate lengths, however, did not substantially improve FET performance as the gate resistance became too large. A new type of gate structure was required and this, in turn, required more sophisticated lithography. Multilayer resist technology and recessed gates proved to be the key.[4] This technique permitted the lift-off of "mushroom" gates with 0.1 μm footprint and > 0.25 μm gate tops for added conductivity and lowest capacitance.[5] This approach yielded the highest unity current gain cutoff frequency f_T ever reported for any FET of any kind to that time: 113 GHz. The basic approach to fabricating this gate is still employed today in several manufacturing lines.

IV. Lamella Doping and Planar Doped Barriers

His concept of lamella doping was first described at a workshop and subsequently published.[6,7] The latter reference was his most-cited paper with 183 citations. This lamella concept vastly increased the sheet density of carriers in field effect transistors and was used by Störmer and Tsui in discovering the fractional quantum Hall effect that led to their Nobel prize. The concept of lamella doping was also used to greatly improve the linearity of microwave field effect transistors and is compatible with other device structures such as modulation doping, superlattices, and heterojunctions. It has even transitioned to silicon:germanium devices.

His paper with 143 citations described an application of the lamella doping concept to achieve a planar doped barrier (PDB).[8] Unlike the Schottky barrier, the PDB is not so sensitive to surface preparation, its barrier height is not fixed by work function, and the

capacitance is rather constant over a wide range of operating parameters. The I-V characteristics of the PDB are largely set by the relative proximities of a thin lamella doping layers in a nominally undoped semiconductor sandwiched between two heavily doped regions.

V. Ballistic Transport and Phenomenon Exegesis

Other concepts pioneered by Prof. Eastman include the concept of ballistic transport in semiconductors. His seminal paper in this field has accumulated 175 citations.[9] Although some overly simplistic assumptions may have been made in this paper (such as including regions where the GaAs band structure was very nonparabolic and the use of steady state Monte Carlo results to obtain characteristic time constants), the paper generated a new field of study that led to better understanding of such concepts as velocity overshoot thus enabling higher performance, very short gate length microwave and millimeter wave transistors.[10,11] A subsequent experiment showed near-ballistic transport in a heterojunction bipolar transistor.[12]

To improve the performance of a transistor, its characteristics must be analyzed and a determination must be made of the phenomena leading to those characteristics. In another seminal paper a comparative analysis of conventional and pseudomorphic MODFETs was made.[13] Until this time, the prevailing assumption was made that the advantage of the pseudomorphic over the conventional MODFET was solely due to a higher saturation velocity in the strained InGaAs channel. This work showed that the advantage in f_T could be equally well explained by the concept of modulation efficiency (ME) wherein a portion of the gate voltage was used to modulate the "parasitic" and comparatively immobile charges in the supply overlayer wherein the saturated velocity was much lower than that in the 2D channel below. ME is the portion of the energy supplied to the gate that modulates only the channel current. They postulate that $\upsilon_{eff} = \upsilon_{sat}$ ME and that by improving ME, the f_T can be improved up to 20%. With this model, variations in f_T can be related to epitaxial layer design.

Prof. Eastman was the first to realize that Hall measurements made on epitaxial layers frequently led to errors in the determination of $(N_D\text{-}N_A)$ because the effects of depletion accruing from free surface and interface charges could partially deplete the layer being measured. The paper addressing this issue and how to correct for it was referenced in 140 different articles.[14]

VI. GaAs-based Heterojunction Devices

$Ga_{0.47}In_{0.53}As$ is known to have a high field drift velocity of 2.2×10^7 cm/sec but a low Schottky barrier height of 0.30 eV thus rendering it difficult to use in FET design and fabrication. The use of a double heterojunction to sandwich the $Ga_{0.47}In_{0.53}As$ overcomes this problem with the low barrier height while permitting the use of a Schottky to the overlying confining barrier of highly insulating $Al_{0.48}In_{0.52}As$ yielding a barrier height of 0.8 eV as described in a conference paper.[15] The performance of such a device utilizing a submicron gate was later published.[16] The structure was later used to demonstrate the highest room

temperature (RT) mobility reported to date for a 2D electron gas structure (12,000 cm^2/V-sec). The RT sheet carrier concentration was 1.4 x 10^{12} cm^{-2}.[17] At lower sheet concentrations, persistent photoconductivity was detected and probably was due to alloy and related impurity scattering. State of the art RT DC transconductance of 440 mS/mm was set for a 1.0 micron gate device.[18]

The first direct evidence of a strain-generated built-in electric field in a (111) oriented strained –layer structure resulted from an ingenious structure. This structure was designed such that the strain generated electric field in a quantum well detector opposes the weaker built-in electric field of the diode. Upon application of a reverse bias, a blue shift of the absorption peak was noted.[19] This paper received 160 reference citations.

VI. High Speed Optics

To design a laser, one requires control of the semiconductor bandgap. While ternary compounds with well-behaved photoluminescence response were routinely grown by organometallic vapor-phase epitaxy and by liquid phase epitaxy, molecular beam epitaxy was seemingly incapable of doing so as recently as 1980. In a paper receiving 111 citations, Eastman showed that the problems were two-fold: 1) too much oxygen was being incorporated and 2) there were too many gallium vacancies. By reducing the CO and H_2O backgrounds and increasing the substrate growth temperature, both problems were overcome.[20] To further increase the spectrum available to semiconductor lasers, pseudomorphic heteroepitaxy is known to provide increased flexibility in bandgap engineering. Strained InGaAs quantum wells grown below 500 Celsius, however, demonstrated rapid degradation of material quality while those grown above 500 Celsius tended to cluster, segregate and desorb. To overcome this dilemma, two approaches were taken. To allow for a smoothing of the heteroepitaxial interfaces, growth was suspended for two minutes immediately prior to the quantum well growth and again for two minutes after growing a 30 Angstrom GaAs layer over the quantum well. Secondly, a 15 second high temperature post anneal dramatically increased the PL efficiency. [21]

VIII. Wide Bandgap Materials and Devices

Until he pioneered the concept of two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures in 1999, the lamella doping concept was the primary means of achieving high sheet charge densities. Nominally undoped III-N heterojunction FETS had been known for their high RF performance but required a better explanation of the source of the electrons in the channel. In a paper receiving 149 citations it was shown that high sheet carrier concentrations and strong confinement at specific interfaces in these structures could be explained by interface charges induced by piezoelectric and spontaneous polarization effects.[22] This pioneering paper has led to a better understanding of GaN HEMT devices which led to microwave FET power densities a factor of 10 higher than had previously been achieved in GaAs and InP technologies. These power densities and the linearity of the

devices engendered thereby, in turn, are expected to engender powerful and versatile new electromagnetic systems characterized by their ability to simultaneously radiate multiple RF beams wherein each beam is provided independent control of its power, frequency, bandwidth, modulation, and beam shape and wherein any beam can perform communications, radar, electronic warfare, or any other conceivable RF function. The upcoming third and fourth generations of cell phone base stations are expected to employ the GaN HEMT concepts he addressed for purposes of improved linearity and power density.

Until recently, charge carrier transport in the III-N materials was both poor and not well understood. A paper by Eastman, et al addressed electron scattering at threading dislocations in GaN. He noted asymmetric electron scattering wherein electrons laterally traversing threading dislocations experienced considerably more scattering than did electrons moving parallel to the dislocations.[23] This paper received 109 citations.

Prof. Eastman, although now semi-retired, has not rested on his laurels. Already in this new century he has published 23 papers cited by others and nearly all of these have been in the wide bandgap semiconductor field. His latest paper shows how to achieve electron sheet carrier densities of ~1 x 10^{20} cm^{-3} in AlGaN with aluminum mole fractions as high as 80%.[24] This work also demonstrated that at these silicon doping densities, the surface roughness in AlGaN was significantly less than in silicon doped GaN. Other interesting features of this work showed that the carrier concentration, the resistivity, and the mobility were all constant over a large range of temperatures. This work is expected to lead to much improved ohmic contacts to N-type AlGaN and possibly to tunnel contacts to P-type GaN. Either could be expected to improve transistor RF performance.

Acknowledgments

This work is supported by the Office of Naval Research under contract N00014-99-D-0506, Task Order # 0001

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Power Amplification in UHF Band using SiC RF Power BJTs

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Abstract

4H-SiC RF Bipolar Junction Transistors (BJTs) have been designed and tested at 425 MHz for the first time. Both epitaxial and implanted emitter structures have been fabricated. It has been established that the implanted emitter structure has very low current gain (~1) due to the implant damage which cannot be totally removed by the high temperature activation anneal. The epitaxial emitter structure with collector and base thickness of 5 μm and 0.1 μm, respectively, shows a maximum current gain of 15 and a common emitter breakdown voltage of 500 V. The f_T of this device was about 1.5 GHz. The epitaxial emitter device, with an emitter width of 2.5 μm and an emitter periphery of 2.62 cm, has demonstrated an output power of 50 W/cell using 80 V power supply in common emitter, Class AB mode. The pulse width was 100 μs and duty cycle was 10%. The collector efficiency at the power output of 50 W was 51% with a power gain of 9.3 dB. The peak large signal power gain was 9.6 dB.

Introduction

Silicon RF BJTs dominate the industry today for power amplification in the UHF band. For high power amplifiers, SiC BJTs have the potential for superior performance due to higher current and voltage handling capability. Recent advances in SiC device technology have realized both implanted emitter and fully epitaxial power BJTs [1,2]. In this paper, we will present the design, fabrication and test results of RF 4H-SiC BJTs suitable for UHF Radar applications. These devices exploit SiC's high saturation velocity, breakdown field strength and thermal conductivity for microwave power amplification. The SiC BJT is particularly attractive because of its ability to achieve 2x higher current density and higher output power during a short pulse as compared to the SiC Static Induction Transistor (SIT).

Device Design

Power gain is one of the most important design considerations in the design of a microwave power transistor. The power gain is basically determined by the f_{MAX}, the maximum frequency of oscillation. Under small signal conditions, the highest power gain a transistor can achieve at frequency f_0 is given by

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$$powergain \approx \left(\frac{f_{MAX}}{f_0} \right)^2$$

Normally, however the above gain cannot be obtained due to parasitics. For large-signal Class C operation, the power gain is further reduced by the current and voltage saturation of the transistor. Therefore it is not unusual for a power transistor to have gain which is 3 to 4 dB lower than the above relation predicts. Assuming that we need a small signal gain of 12 dB at 400 MHz, the above relation dictates a f_{MAX} of 1.6 GHz.

In order to design a transistor with a 1.6 GHz intrinsic f_{MAX}, we should examine the factors, which affect the f_{MAX} of the transistor. A simplified cross-section of the epitaxial emitter structure is shown in Fig. 1. The stripe geometry has been assumed. All microwave transistors are fabricated more or less with this geometry. The intrinsic part, directly under the emitter, is the active part of the transistor. The extrinsic part, which connects the intrinsic base (under the emitter) to the base contacts, is the parasitic part of the transistor. The effects of these two parts on the transistor f_{MAX} can be evaluated by the following formula:

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi \left(r_{con} C_t + \frac{r_{be} C_{be}}{2} + r_b C_i \right)}}$$

where, the various terms are defined below:

f_T: Current gain bandwidth of the transistor
r_{con}: Base contact resistance
r_{be}: Extrinsic base resistance
r_b: Intrinsic base resistance
C_t: Total base-collector capacitance
C_{be}: Collector base capacitance due to the extrinsic part of the base
C_i: Collector base capacitance due to the intrinsic part of the base

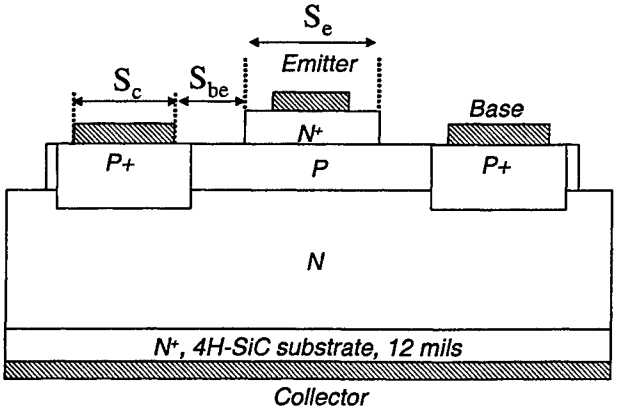


Fig. 1 A simplified cross-section of the BJT structure.

For interdigitated transistor structures, the device parameters in the above formula can be further expressed in terms of the transistor structure parameters [3]. Thus we have,

$$r_{con}C_t = \frac{1}{2}R_c C_{cb}(S_c + 2S_{be} + S_e)$$

$$r_{be}C_{be} = \frac{1}{2}R_{be}C_{cb}S_{be}^2$$

$$r_b C_i = \left(\frac{R_{be}S_{be}}{2} + \frac{R_b S_e}{12}\right)C_{cb}S_c$$

where,

R_c: Base contact resistance per unit length in ohm-cm
R_b: Intrinsic base sheet resistance in ohm/sq
R_{be}: Extrinsic base sheet resistance in ohm/sq
C_{cb}: Collector Base capacitance in F/cm^2
S_e: Emitter width (shown in Fig. 1)
S_c: Base contact width (shown in Fig. 1)
S_{be}: Spacing between emitter mesa and the base contact (shown in Fig. 1)

Assuming $R_c \sim 1$ ohm-cm, $R_b = R_{be} = 100{,}000$ ohm per sq. (for $N_A = 2\text{x}10^{18}$ cm^{-3}), $f_T = 2$ GHz, $S_c = 2$ μm, and W_c, depleted collector thickness of 2 μm ($C_{cb} = \varepsilon_{SiC}/W_c$), the f_{MAX} was calculated for various values of S_e and S_{be}. The results are summarized in Fig. 2. Based on these calculations, it may be concluded that the f_{MAX} is limited by the extrinsic base resistance and not by the emitter width to the first order. Therefore we have chosen the emitter width, $S_e = 2.5$ μm for ease of fabrication. The nominal design uses $S_{be} = 0.5$ μm to assure that we get $f_{MAX} > 1.6$ GHz.

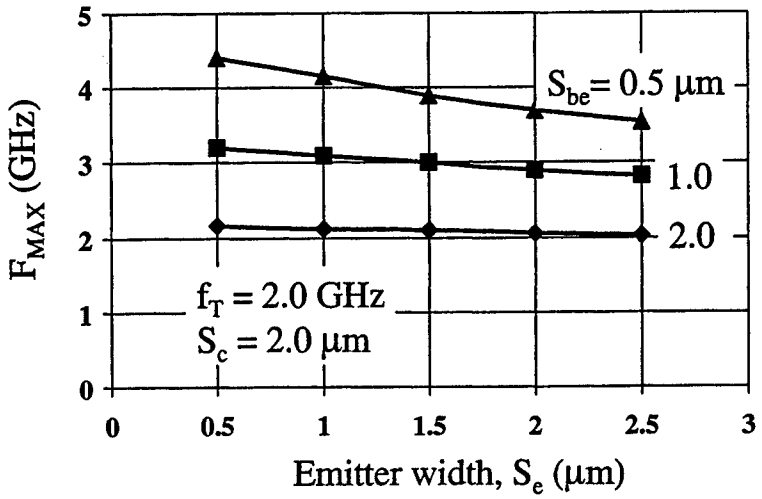


Fig. 2 Calculation of F_{MAX} vs. emitter stripe width, S_e, with a variable spacing between emitter mesa and the base contact, S_{be}.

The f_T may be estimated as follows:

$$\tau_{ec} = \frac{1}{2\pi f_T} = \frac{W_b^2}{2D_n} + \frac{W_C}{2v_s} + \frac{kT/q}{I_C}(C_{BE} + C_t)$$

where,

τ_{ec}: Total delay between emitter to collector
W_b: Base thickness (500 – 2000 Å)
D_n: Diffusion coefficient of electrons in the base (1.95 cm^2/s assuming electron mobility of 75 $cm^2/V\text{-}s$ in the base doped at $2x10^{18}$ cm^{-3})
W_C: Collector thickness (6 μm)
V_s: Velocity of electrons in the collector ($1.5x10^7$ cm/s)
I_C: Collector current (50% of the maximum value at a current density of 6000 A/cm^2)
C_{BE}: Total base-emitter junction capacitance
C_t: Total base-collector capacitance

The calculated values of f_T as a function of W_b at room temperature and 250°C junction temperature are shown in Fig. 3. We have chosen a nominal value of W_b ~ 1000Å to provide a f_T ~ 2 GHz.

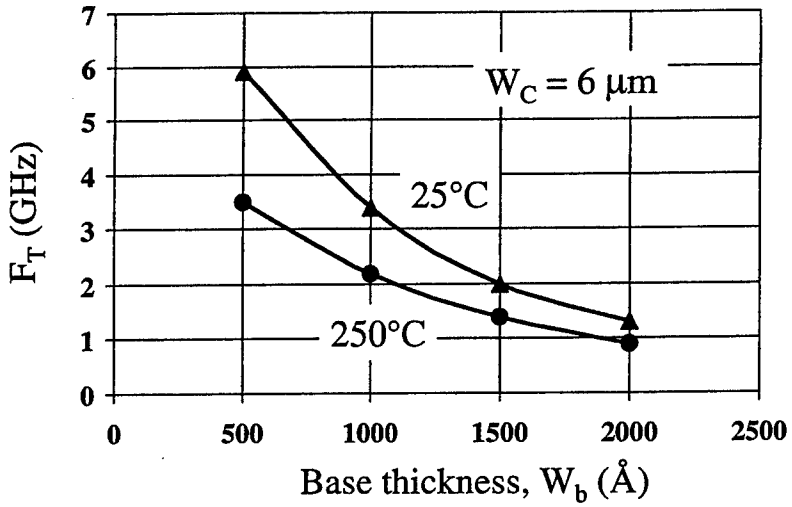


Fig. 3 The calculated values of f_T vs. base thickness.

Two types of transistors were fabricated: (1) Implanted emitter, and (2) Epitaxial emitter.

Implanted Emitter

The implanted emitter structure is shown in Figs. 4-5. A 5 μm n-type collector layer doped at $7x10^{15}$ cm^{-3} is grown on a 4H-SiC, 8° off, n^+ substrate. Next, a 5500 Å thick, p-type

base layer doped at $2x10^{18}$ cm^{-3} is grown. This is followed by a selectively implanted n^+ emitter layer using a 650°C nitrogen implant. The emitter implant energy is adjusted to leave about 1000 Å of p-type base layer (Fig. 4). Next, the p-base is isolated by a mesa etch followed by a p^+ (Al) implantation to simultaneously form the base contact regions and the floating guard rings for edge termination. All the implants were simultaneously activated at 1600°C in Ar ambient. The n and p-contacts were formed with sintered Ni. After contact formation, a 2 μm thick Gold overlayer is applied. A single cell consists of 166 emitter fingers of 75 μm length with a total emitter periphery of 2.62 cm. The cell has a total width of 105 μm excluding the pads and a length of 1019 μm. The total base active area excluding the guard rings is $1.07x10^{-3}$ cm^2.

Epitaxial Emitter

The epitaxial emitter structure is shown in Fig. 6. In this case, only 1000 Å thick, p-type base layer doped at $2x10^{18}$ cm^{-3} is grown. This is followed by an epitaxial growth of 3000 Å thick n^+ emitter layer. The emitter layer is reactive ion etched (RIE) to stop at the base layer. The rest of the design and process details are similar to the implanted emitter structure. The most difficult step in this process is the etching of the emitter layer and stopping at the base layer. The uniformity of the RIE is critical at this step.

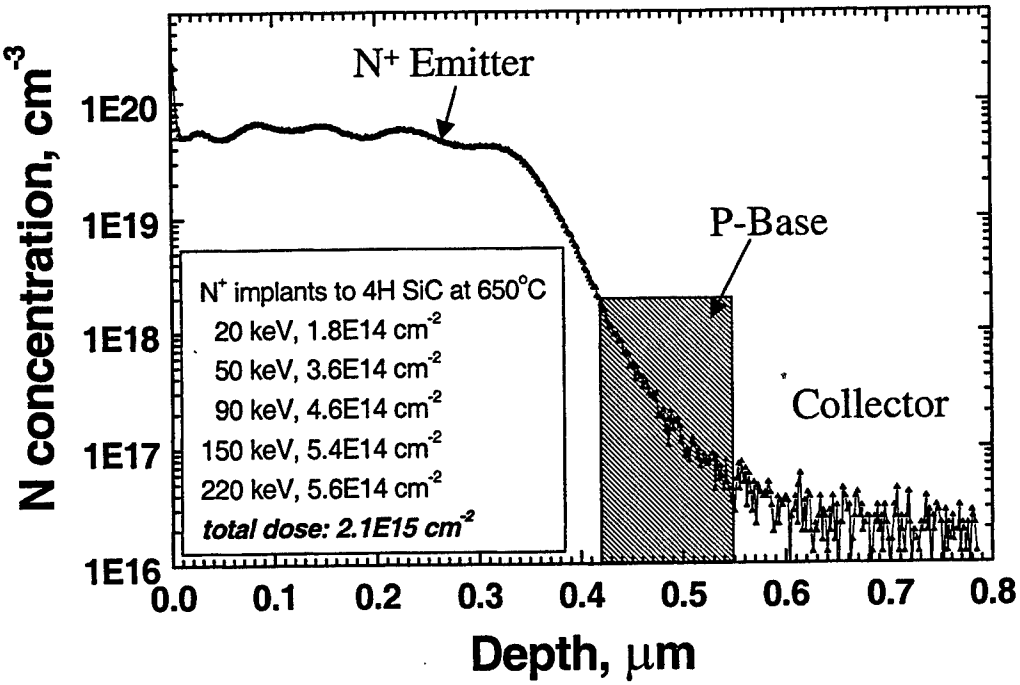


Fig. 4 SIMS profile of the implanted emitter showing that 1000 Å of base layer is remaining.

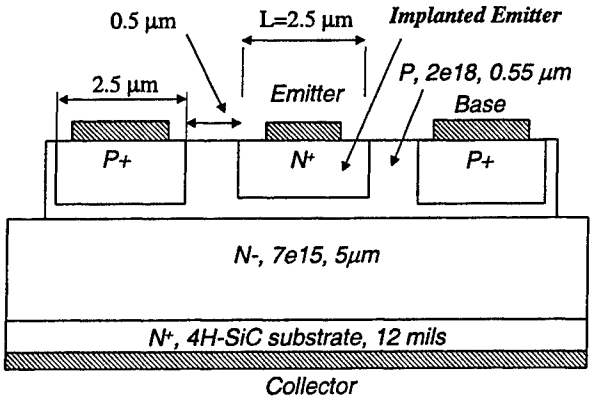


Fig. 5 Simplified cross-section of the implanted emitter structure.

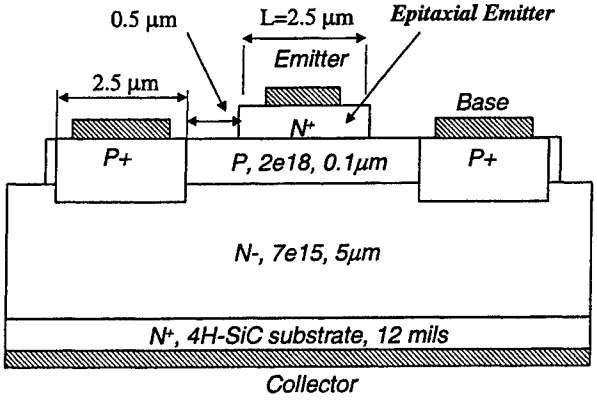


Fig. 6 Idealized cross-section of the epitaxial emitter structure.

Results

It turns out that the current gain in the implanted emitter structure is completely dominated by the recombination in the base layer due to the un-annealed implant damage. Examples of the I-V characteristics are shown in Fig. 7. A current gain of about 1 is obtained in the structure with 2.5 μm wide emitter. The common emitter breakdown voltage is ~500 V as designed. **It is concluded that the implanted emitter approach is not suitable for BJT fabrication in the SiC technology.**

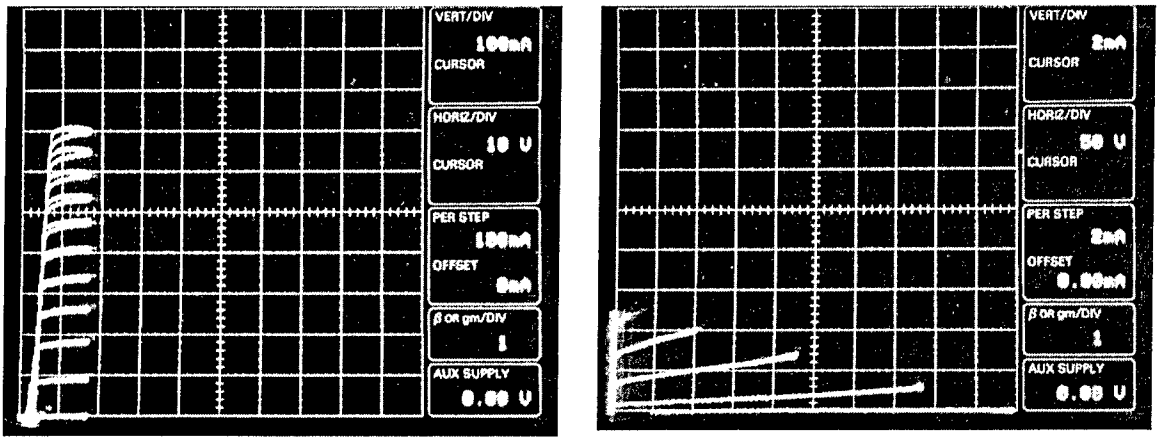


Fig. 7 I-V characteristics of the implanted emitter device with a 2.5 μm wide emitter showing a current gain ~1 and BV_{ceo} > 500 V.

Fig. 8 shows the I-V characteristics of a single epitaxial emitter cell. A maximum current gain of about 15 is obtained. This current gain is extremely sensitive to the base contact implant spacing from the edge of the emitter mesa (in the present design, it is 0.5 μm as shown in Fig. 6). This indicates that the surface recombination is the limiting factor for current gain in the epitaxial emitter structure. Better passivation is needed to suppress the

surface recombination and further improve the current gain. The common emitter breakdown voltage was in excess of 500 V consistent with the 5 μm collector thickness.

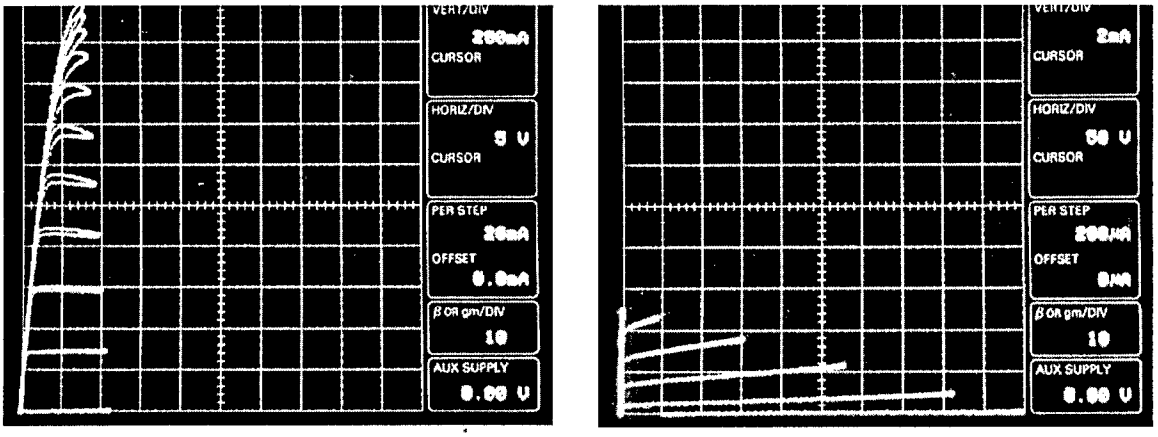


Fig. 8 Common Emitter (CE) I-V characteristics of a single epitaxial emitter cell showing a maximum current of 2 A, β_{max} ~ 15 and a BV_{CEO} = 500 V.

The f_T of the cell was measured as a function of the collector current with different collector supply voltages (Fig. 9). For V_{CC} = 20 V, f_T peaks at about 1.5 GHz whereas for V_{CC} = 30 V, f_T peaks at about 1.3 GHz. This reduction in f_T with collector voltage is expected as the electron transit delay in the collector depletion width increases with increasing collector bias. The sudden drop in f_T at high current for V_{cc}=30 V is attributed to a hot spot on the device.

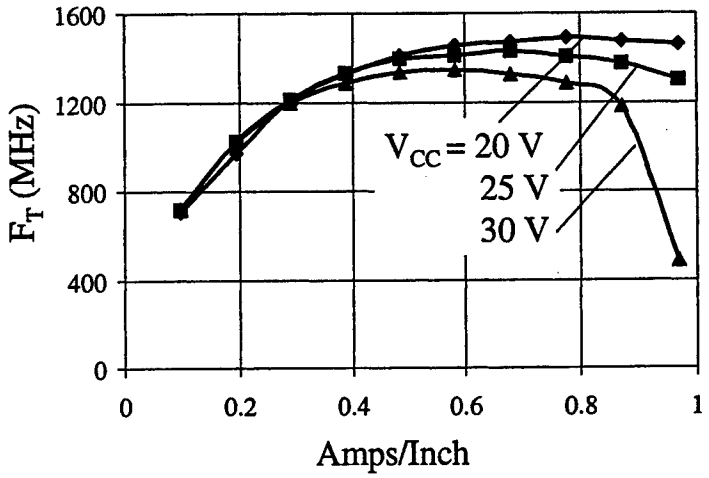


Fig. 9 Measurement of f_T as a function of collector current and the collector voltage.

A single cell was measured in common base (CB), class C mode at 425 MHz using a collector supply voltage of 80 V. The pulse width of 100 μs with a duty cycle of 10% was used. The single measurement yielded a maximum power of 39.8 W with a power gain of

5.1 dB and a collector efficiency of 57.85%. The power gain in class C or class B is expected to be low due to a large input power required to turn-on the input base-emitter junction which has a turn-on voltage of about 3 V due to the wide bandgap of SiC. The output power level is consistent with the power triangle measured under DC conditions [40 W = (160 V x 2 A)/8].

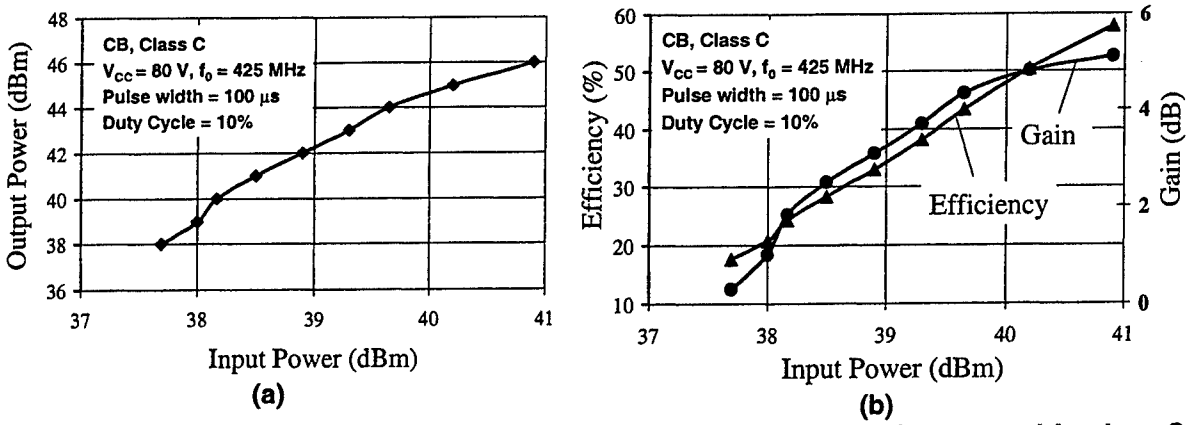


Fig. 10 (a) Output power vs. input power for a single cell in CB mode operated in class C mode at 425 MHz, pulse width 100 μs, duty cycle 10%, and V_{CC} = 80 V; (b) Collector efficiency and power gain vs. output power for conditions stated in (a).

A single cell was also measured in common emitter (CE) mode with a collector supply voltage of 80 V in class AB at 425 MHz. The device was biased in class AB mode with a collector bias current of about 50 mA, just enough to overcome the large 3 V turn-on voltage. A 100 μs pulse width with 10% duty cycle was used. The results are shown in Fig. 11. A maximum output power of 50 W for a single cell was achieved. This represents an output power density of 47 kW/cm^2 when normalized by the active base area. The power density is more than five times higher than that typically obtained with Si BJTs at this frequency. The peak large signal power gain was 9.6 dB. The collector efficiency at the power output of 50 W was 51% with a power gain of 9.3 dB.

This result is highly encouraging as it demonstrates the high power capability of the SiC RF-BJT devices along with acceptable power gain and efficiency. From thermal simulations, it is estimated that the junction temperature may reach a peak value of 171°C for pulse widths of 250 μs and 6% duty cycle without any external cooling. Since SiC junctions can easily sustain a temperature of 250°C, there is room to increase the pulse width even further.

Summary and Conclusion

The design of SiC RF BJTs has been discussed. It is concluded that the implanted emitter structure is not suitable as it yields a very low current gain due to the implant induced

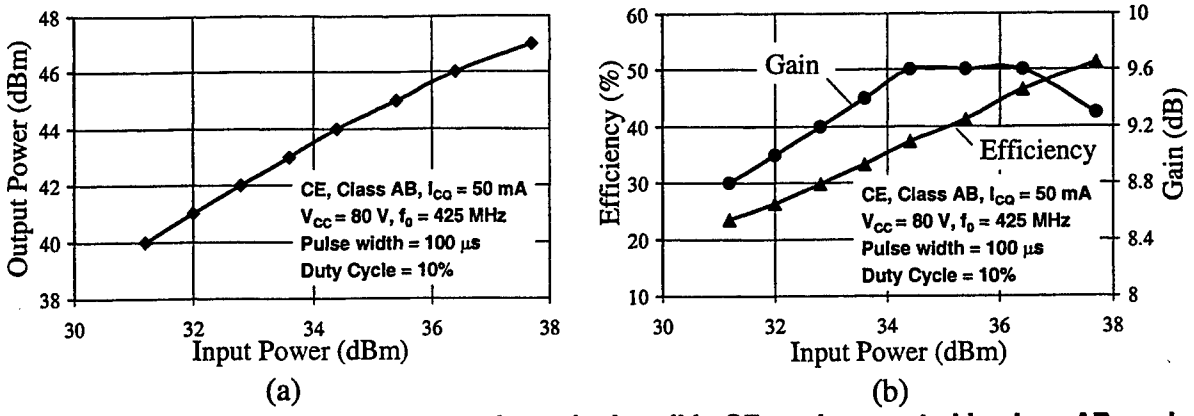


Fig. 11 Output power vs. input power for a single cell in CE mode operated in class AB mode at 425 MHz, pulse width 100 μs, duty cycle 10%, V_{CC} = 80 V and I_{CQ} = 50 mA; (b) Collector efficiency and power gain vs. output power for conditions stated in (a).

damage in the injection region. The fully epitaxial structure was designed and fabricated with approximately 1000 Å thick base layer. This device yielded a maximum current gain of 15, maximum collector current of 2 A at V_{CE} =7 V and a common emitter breakdown voltage of 500 V. A single cell consisted of 166 emitter fingers of 75 μm length with a total emitter periphery of 2.62 cm. The cut-off frequency, f_T was measured to be above 1.4 GHz for I_C in the range of 0.5 to 1.0 A and V_{CC} = 20 V. A single cell has demonstrated an output power of 50 W/cell using an 80 V power supply in common emitter, Class AB mode. The pulse width was 100 μs and duty cycle was 10%. The collector efficiency at the power output of 50 W was 51% with a power gain of 9.3 dB. The peak large signal power gain was 9.6 dB. The common base configuration yielded a maximum power of 39.8 W with a power gain of 5.1 dB and a collector efficiency of 57.85% in class C mode. The power gain was low in class C mode because of the large input RF signal needed to overcome the turn-on voltage of the base-emitter junction. This can be easily overcome by forward biasing the input junction at the threshold of conduction (class AB mode). This was verified in common emitter mode. Since SiC junctions can withstand high junction temperatures, it is possible to increase the pulse width to 250 μs or higher without requiring any external cooling, resulting in significant systems advantages.

Acknowledgement

This work was supported by Dr. John Zolper and Dr. Harry Dietrich of the Office of Naval Research (Contract No. N00014-01-C-0017).

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High-Performance Power BJTs in 4H-SiC

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Abstract

In this paper, we summarize recent progresses in 4H-SiC BJTs at Purdue University. For 50 μm collector devices, BV_{CEO} > 3,200V is achieved. Large devices (active area = 1.05 mm^2) exhibit common emitter current gain β around 15, and specific on-resistance $R_{ON,SP}$ of 78 mΩ-cm^2. Smaller devices (active are = 0.0072mm^2) have β of 20 and $R_{ON,SP}$ of 28 mΩ-cm^2. For 20 μm collector devices, β's greater than 50 and $R_{ON,SP}$ around 26 mΩ-cm^2 are observed. The blocking voltage is low (500 – 700 V) for these devices because of aluminum spiking during the base contact anneal. The observed positive temperature coefficient of $R_{ON,SP}$ and negative coefficient of β show that 4H-SiC BJTs can be safely operated in parallel connections. We also observe that β decreases as the spacing between base contact implant and emitter finger is reduced. We attribute this to recombination at defect sites in the p+ implanted base contact.

I. Introduction

Silicon carbide (SiC) is an attractive material for semiconductor power devices because of its superior physical and electrical properties such as its wide band gap, high breakdown field, high saturation velocity, and high thermal conductivity. Among SiC power switching devices, bipolar junction transistors (BJTs) are projected to have lower $R_{ON,SP}$ than unipolar devices because of conductivity modulation in the collector drift region [1]. BJTs also have lower turn on voltage than other bipolar devices [1]. Previously reported BJTs show excellent on-state characteristics at room temperature, with reverse blocking voltage BV_{CEO} of 1,800V [2].

In this paper, BJTs with different sizes and different collector thickness are reported. Blocking voltage BV_{CEO} as high as 3,200 V and current gain over 50 are achieved. High temperature measurements show that 4H-SiC BJTs are suitable for device paralleling. A separate study indicates that the gap between the p+ base contact implant and the emitter finger has a significant effect on the current gain.

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II. Device Fabrication

An interdigitated finger structure is used for these 4H-SiC BJTs to avoid current crowding due to the lateral resistance of the p-type base layer. BJTs are fabricated in n+/p/n- epilayers on heavily-doped n+ 4H-SiC substrates. The n+ emitter layers are 1 μm, doped above $1x10^{19}$ cm^{-3}. For the high-voltage devices, the base layer is 1 μm thick, doped $2x10^{17}$ cm^{-3}, and the collector is 50 μm, doped $8x10^{14}$ cm^{-3}. For the lower voltage devices, the base is 1 μm, doped $1.2x10^{17}$ cm^{-3}, and the collector is 20 μm, doped $2.4x10^{15}$ cm^{-3}. Emitter and base mesas are defined by reactive ion etching in SF_6. P+ regions are implanted along each base finger to reduce the base contact resistance. In these regions, aluminum is implanted at doses/energies of $6x10^{13}$/40 and $1.6x10^{14}$/130 cm^{-2}/keV. A single-zone junction termination extension (JTE) is used to relieve filed crowding at the junction corners in the blocking state. The JTE ring is formed by a second aluminum implantation at doses/energies of $1x10^{12}$/40, $2x10^{12}$/100, $3x10^{12}$/200, and $5x10^{12}$/350 cm^{-2}/keV. Both implants are performed at 650 °C and activated at 1600 °C for 30 min in argon. The implant activation percentage is estimated to be 70% after annealing. After an RCA clean, an MOS-quality oxide is thermally grown in wet O_2 at 1150 °C for 2.5 hours to passivate the surface. The p-type base ohmic contact is composed of 30 nm titanium followed by 100 nm of aluminum, and n-type contacts to the emitter and back side (collector) are 100 nm of nickel. All contacts are annealed at 1000 °C for 2 min. in argon. A 0.5 μm layer of gold is evaporated on the back side, and 0.8 μm of gold is deposited as the top interconnect metal. A cross sectional view of the device is shown in Fig. 1.

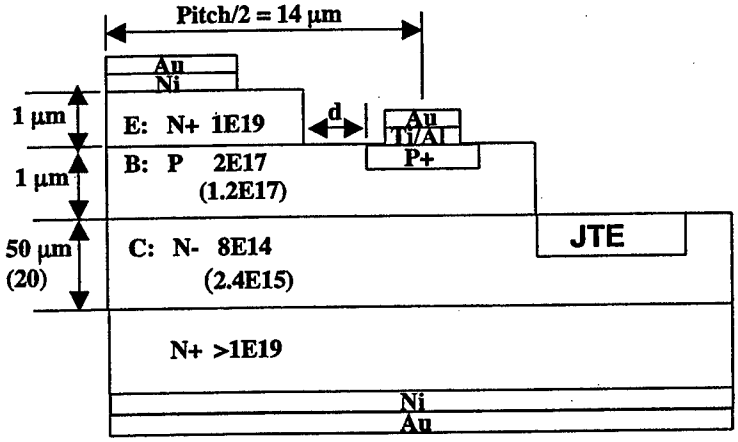


Figure 1. A cross sectional view of a 4H-SiC BJT showing two different designs (low-voltage design parameters in parentheses).

III. Results and Discussion

Current-voltage curves of the fabricated devices are extracted using an HP-4156 semiconductor parameter analyzer and a Tektronix 371A curve tracer. The high voltage performance is measured with samples immersed in flourinert. Elevated temperature measurements are performed on a hot chuck.

The n- and p-type contacts are ohmic after anneal, with specific contact resistivities of $2x10^{-5}$ and $1x10^{-3}$ Ω-cm^2, respectively, at room temperature. These results are extracted from TLM structures. Although the p-type contact resistance is higher than the n-type, the estimated additional voltage due to the contact resistance is less than 0.1 V, which is small compared with the built-in potential of the emitter-base junction. Therefore the effect of the p-type contact resistance on device performance can be neglected.

A. Devices with 50 μm collector layers

Figure 2 shows the room temperature on–state I-V characteristics of a large device with 50 μm thick collector and 1.05 mm^2 active area (finger length = 350 μm). The device carries 1.2A (corresponding to 115 A/cm^2) at a forward voltage drop of 11.5 V with a base current of 80 mA. DC current gain is 15. The specific on-resistance resistance is 78 mΩ-cm^2, about 1.9 times higher than the theoretical unipolar value for this epilayer. Figure 3 shows that BV_{CEO} is greater than 3,200 V, about 40% of the theoretical value. The figure of merit $V_B^2/R_{ON,SP}$ is 131 MW/cm^2, comparable to the best SiC MOSFETs

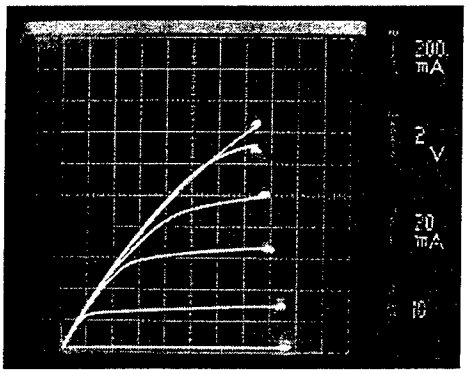


Figure 2. On-state characteristics of a large BJT (active area of 1.05 mm^2 and finger length of 350 μm) on a 50 μm collector drift region.

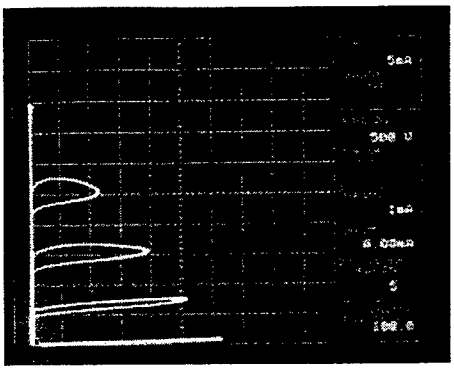


Figure 3. Blocking characteristics of the large BJT of Fig. 2. V_{CEO} is greater than 3,200 V.

Figures 4 - 6 show the on-state characteristics of a small BJT at room temperature. The device maintains a current gain greater than 20 up to collector current densities of 300 A/cm^2 at V_{CE} = 10 V. Above this current density the device enters saturation, and the current gain is dramatically reduced because the base-collector junction is forward biased and base current flows into collector as well as into the emitter. The specific on-resistance $R_{ON,SP}$ obtained from Fig. 4 is 28 mΩ-cm^2, smaller than the theoretical unipolar value. This can be explained by lateral spreading of current in the thick drift region in the small size device, and possibly some conductivity modulation of the drift region. From Fig. 5, the ideality factor for the base current η_B is close to 2, indicating the base current is dominated by recombination. The collector current, on the other hand, is dominated by η_C=1 diffusion current. The power dissipated in driving the base of the small BJT is only about 1.7 % of its total on-state power loss.

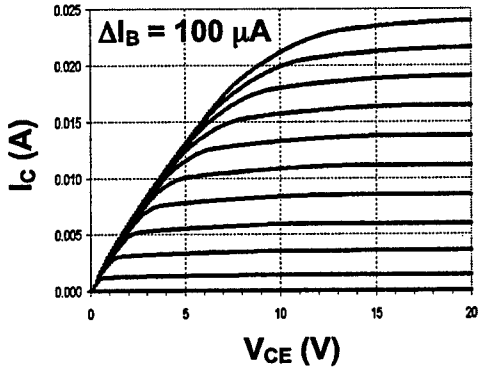


Figure 4. On-state characteristic of a small BJT (active area of 0.0072 mm^2) on a 50 μm collector drift region.

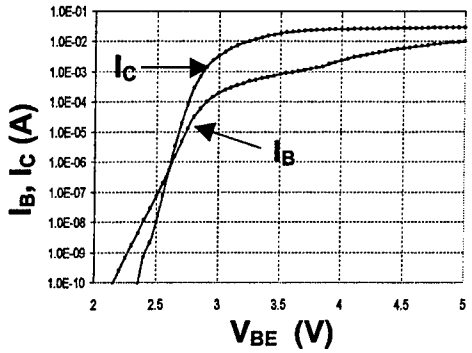


Figure 5. Gummel plot for the small BJT of Fig. 4 at V_{CE} = 10 V.

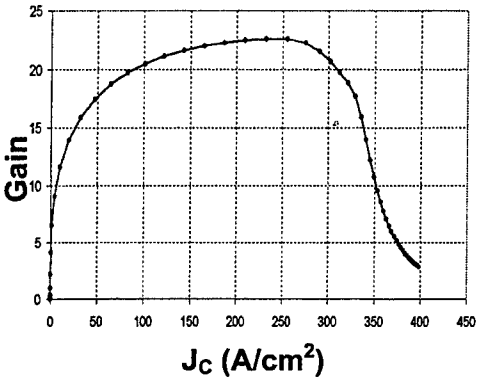


Figure 6. Common-emitter current gain vs. collector current density for the small BJT at V_{CE} = 10 V.

Figure 7 shows how performance varies with temperature. These BJTs exhibit higher $R_{ON,SP}$ and lower β at elevated temperatures, which is desirable because it allows devices to be operated in parallel. This trend is consistent with observations of other groups [2, 3].

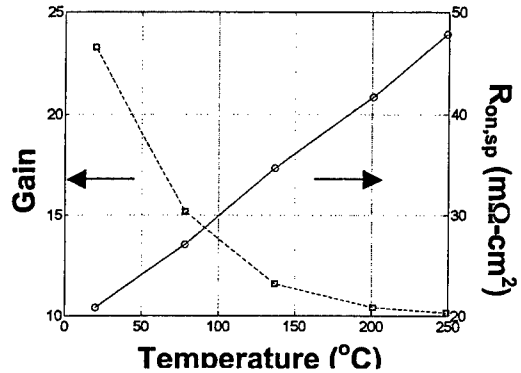


Figure 7. Temperature dependence of current gain and specific on-resistance for the small BJT of Fig. 4.

The dependence of current gain on the spacing between the p+ base contact implant and the emitter edge is shown in Fig. 8. As the p+ base contact implant is brought closer to the emitter edge, the current gain decreases monotonically. It is likely that the p+ base contact implant introduces defects into the SiC that are not completely removed during the implant activation anneal. As the defect sites are brought within one electron diffusion length of the emitter, recombination at these defect sites reduces the current gain.

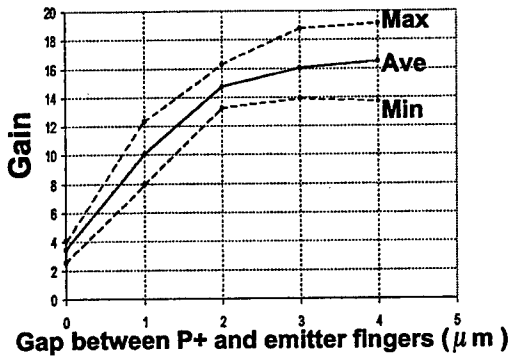


Figure 8. Current gain of the small BJT as a function of spacing between the p-type base contact implant and the edge of the emitter

B. Devices with 20 μm collector layer

Figure 9 shows the on-state characteristics of a large BJT (active area of 1.05 mm^2 and finger length of 350 μm) on a 20 μm collector drift region. This device carries 2 A (190 A/cm^2) at a forward voltage of 5 V and base current of 50 mA. DC current gain is greater than 50, and the specific on-resistance is 26 $m\Omega$-cm^2, about 5-6x higher than the theoretical unipolar value for the collector epilayer. Figures 10 and 11 show that BV_{CEO} is 500 V and BV_{CBO} is around 700 V, only 20% of the theoretical value for this collector epilayer. We attribute the low blocking voltage to punchthrough of the base caused by aluminum spiking from the base ohmic contact during the contact anneal. Prior to the contact anneal, BV_{CBO} was greater than 1,900 V on a test PiN diodes on the same wafer. Elevated temperature measurements and p+ implant studies on the 20 μm epilayer devices show similar results as those on 50 μm epilayer devices.

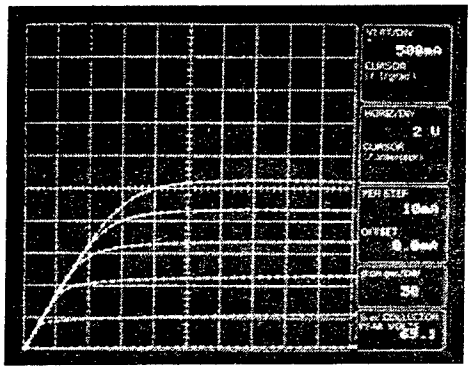


Figure 9. On-state characteristics of a BJT with 1.05 mm² active area (finger length = 350 μm) on a 20 μm collector drift region.

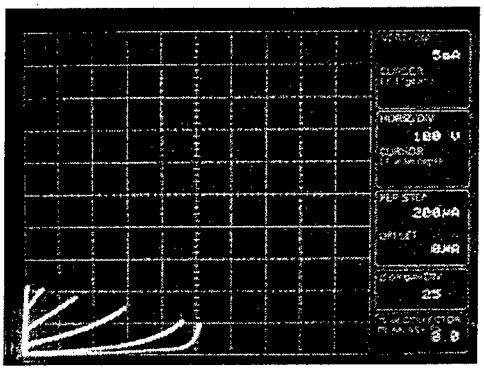


Figure 10. BV_{CEO} of the BJT in Fig. 9 is 500 V after ohmic contact anneal.

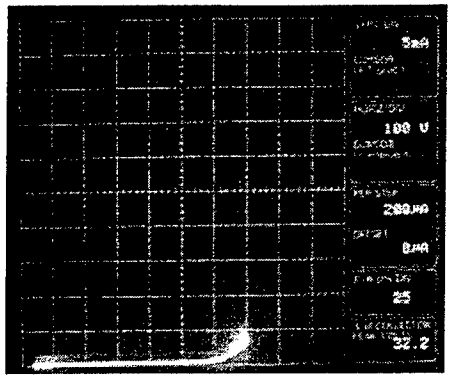


Figure 11. BV_{CBO} of the BJT in Fig. 9 is 700 V after ohmic contact anneal.

IV. Conclusions

4H-SiC npn BJTs of different sizes and different collector layer thickness are reported. For 50 μm collector devices, an open-base blocking voltage BV_{CEO} of 3,200 V is achieved, the highest value reported to date for SiC BJTs. Large devices exhibit a common emitter current gain of 15 and a specific on-state resistance of 78 mΩ-cm^2. Small devices exhibit a current gain of 20. The figure of merit $V_B^2/R_{ON,SP}$ for the large SiC BJT is 131 MW/cm^2, comparable with the best reported for any SiC power switching device. For 20 μm devices, a DC current gain greater than 50 is observed in the forward active region. The lower blocking voltage (500 – 700 V) is due to aluminum spiking during the base ohmic contact anneal. β increases and $R_{ON,SP}$ decreases as temperature increases, which makes 4H-SiC BJTs resistant to thermal runaway. The spacing between the p+ base contact implant and the edge of the emitter has a strong effect on current gain. This is attributed to recombination at implant-introduced defect sites within the p+ base contact implant.

Acknowledgements

This work is supported by the DARPA Megawatt program under grant no. N00014-99-1-0938 and by the Office of Naval Research under grant no. N00014-01-1-0077.

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100 A and 3.1 kV 4H-SiC GTO Thyristors

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Abstract

In this paper we report on asymmetric SiC GTOs (Gate Turn-Off Thyristors), fabricated at Northrop Grumman with the assistance of Silicon Power Co. A module containing six 1 mm x 1mm GTOs connected in parallel has demonstrated 100 Amps of switching current capability. This is the highest current reported to date with GTOs designed for greater than 3 kV forward blocking voltage [1]. GTOs fabricated from the same wafer have achieved a forward blocking voltage of 3.1 kV, which was the testing limit of the instrumentation. This represents a record high breakdown voltage for GTOs with a drift layer thickness of 30 μm [1-4]. These GTOs also demonstrated record low leakage currents of < 5 μA at the forward blocking voltage of 3.1 kV.

Introduction

Silicon Carbides higher breakdown field, higher thermal conductivity, and wide bandgap give SiC and advantage over Si for high power, high speed, and high temperature device operation. The SiC GTO has advantages as a power switch over its counterparts. BJTs suffer from gain reduced breakdown voltage. IGBTs in SiC have not been developed yet. MOS devices suffer from poor channel mobility and poor reliability of the oxide at high temperatures. The conductivity modulated base regions of the GTO will allow high voltages (> 3000 volts) and high current densities while maintaining a low forward voltage. We report on a GTO fabricated to provide the high voltage and the high current density capabilities. The area of the device was limited to avoid defects in the material; therefore the total current that these devices are capable of carrying is limited. However, these GTOs have been packaged and bonded in parallel to achieve high current. Potential use of the GTO would be in electric vehicles, electric ships, and in power utilities. To realize the potential of

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SiC, difficulties with material defects, passivation, and edge termination must be overcome. To realize the benefit of lower on-resistance from a thinner drift region, the edge termination design and execution must be sufficient to allow the device to achieve the maximum theoretical breakdown voltages. It is the novel JTE design and fabrication that makes the GTOs described in this paper stand out among other SiC devices fabricated thus far.

Fabrication

SiC GTOs were fabricated on n-type 8° off-axis 4H-SiC substrates obtained from Cree. Five epitaxial layers were grown at Cree on the 4H substrates to form the body of the devices. The GTO cross-section is shown in Figure 1. The p-type drift layer thickness (30 μm) and doping level ($5x10^{14}$ cm^{-3}) were chosen to support high voltage in punch-through mode under forward biased blocking. The doping of the N+ buffer layer adjacent to the substrate and the doping of the adjacent P layer was chosen to improve injection efficiency into the base

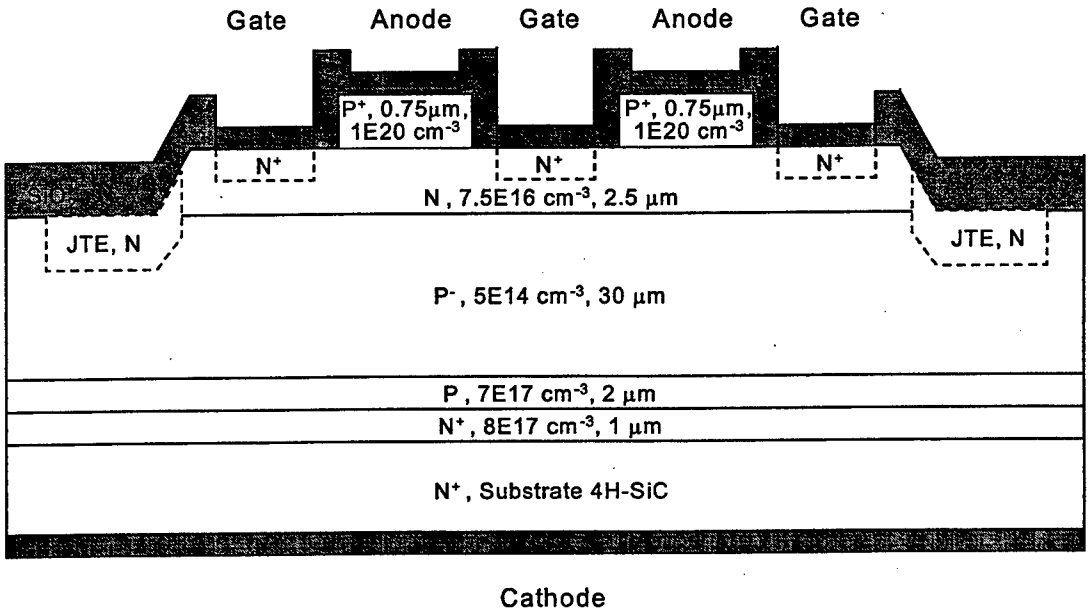


Figure 1: Cross-section of the asymmetrical GTO with 30 μm drift layer.

region. GTOs with nominal dimensions of 1 mm x 1 mm and 2 mm x 2 mm were fabricated using a mesa-etch process for this experiment. These GTOs have a proprietary Junction Termination Extension (JTE), designed to allow a greater realization of the bulk breakdown conditions. The JTE has a laterally graded density profile, with the highest density being on the mesa structure near the device edge and the lowest density on the outermost periphery. This profile was obtained by the masked implantation of Nitrogen at 600 °C, yielding a bulk concentration of approximately $5.4 \times 10^{17} cm^{-3}$. Implants of the JTE, gate, and guard ring

were annealed at 1600 °C in Ar for 10 min. A Nickel-Silicide process was used to form the anode, cathode, and gate contacts. The gate and anode fingers are interdigitated to ensure fast turn-on for inverter applications. The design includes two contact pads of equal area above the interdigitated gate and anode fingers. This design allows double sided cooling of packaged devices. The device surface is passivated with a thick layer of oxide.

Results and Discussion

The turn-off portion of a switching characteristic of a 2 mm x 2 mm GTO is shown in Figure 2. Testing was done in Fluorinert to prevent arcing at the exterior interface of the passivation layer. The forward blocking voltage of 1 kV and a forward current of 2 Amps represents the highest dynamic switching capability currently reported in SiC. During turn-

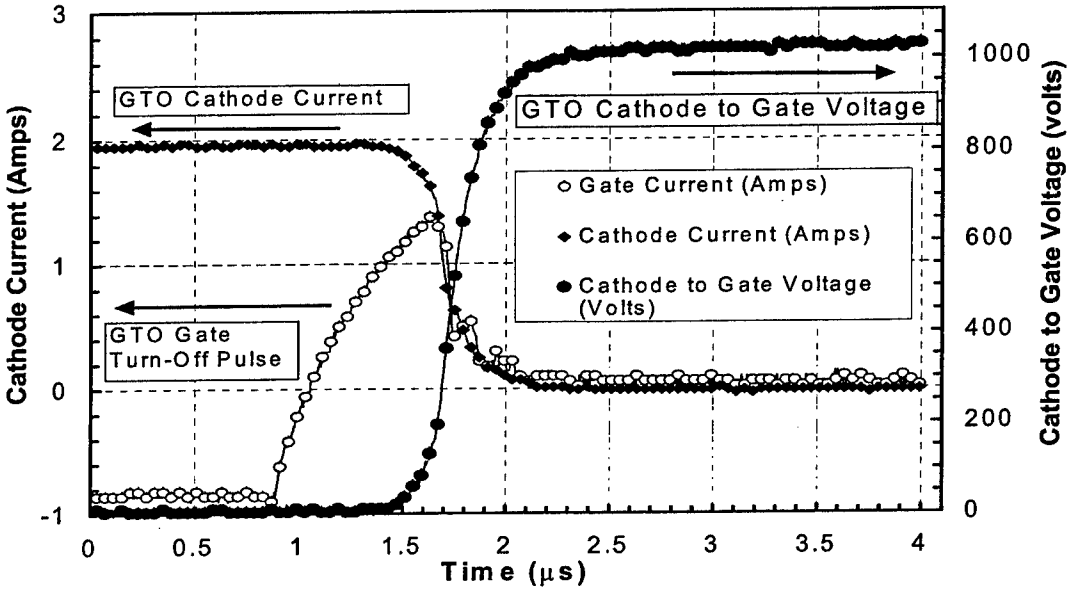


Figure 2: Turn-off portion of a 2 mm x 2 mm GTO switching between a forward conducting current of 2 Amps and a forward blocking voltage of 1 kV.

on and turn-off, the devices handle large currents and large voltages, demonstrating the high instantaneous power achievable in these devices. The turn-off dI/dt of this device was 4.7 A/μs and the dV/dt was 2220 V/μs. It was observed that the 2 mm x 2 mm GTOs yielded lower breakdown voltages than the 1 mm x 1 mm GTOs, which we attribute to area considerations. 1 mm x 1 mm GTOs exhibited forward blocking voltages of up to 3170 volts, as shown in Figure 3.

Figure 4 shows the forward on-state characteristics of a 3.1 kV, 1 mm x 1 mm GTO as a function of temperature. A room temperature on-resistance of 3 $m\Omega$-cm^2 was

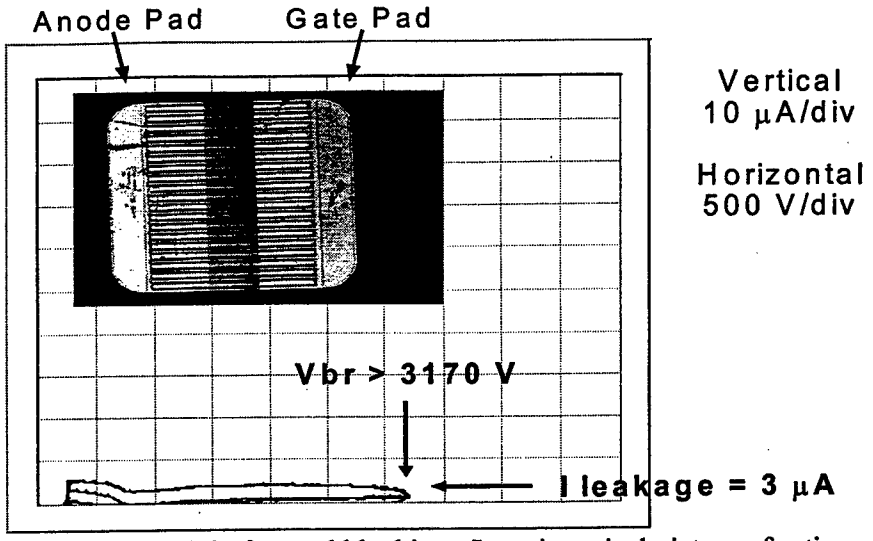


Figure 3: 1 mm x 1mm GTO in forward blocking. Inset is optical picture of active area showing the gate and anode pads.

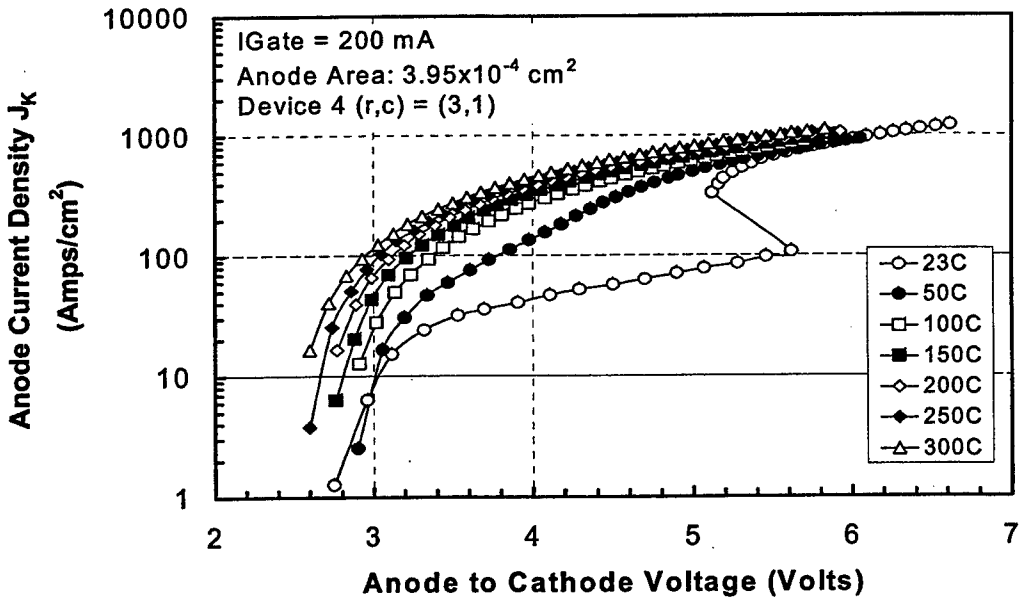


Figure 4: Temperature dependence of the on state I-V Characteristic of a 3.1 kV, 1 mm x 1 mm GTO.

determined from the forward characteristics between current densities of 380 A/cm^2 thru 1140 A/cm^2 and by utilizing the anode area. The on-resistance stays constant with temperature from 50 °C to 300 °C, however, the forward voltage drop did vary, decreasing from 3.73 to 2.93 volts for a current density of 100 A/cm^2. This reduction of on-state voltage with temperature is expected due to the enhanced acceptor ionization in the p+ anode and increased carrier lifetime in the p- drift layer [3]. The maximum turn-off gain was observed to decrease with current density and temperature, and was measured to be 4.0 at a current density of 506 A/cm^2 when measured at room temperature.

Figure 5 displays the turn-off portion of a module consisting of 6-paralleled 1 mm x 1mm GTOs, that is switching 100 Amps. The voltage on this assembly has been kept low since

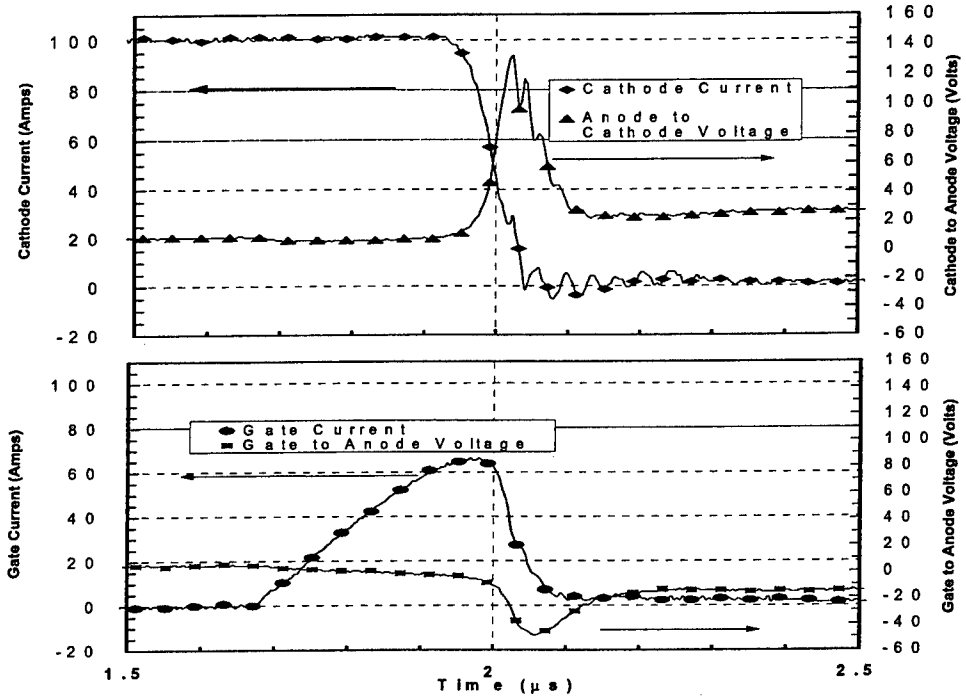


Figure 5: Six parallel GTOs switching 100 Amps for a current density of 1670 A/cm^2.

the GTOs yielding lower breakdown voltages from the same wafer have been utilized first. The GTO Cathode current and Anode to Cathode Voltage are shown in the top most graphs within this figure. The Cathode current is seen to decrease from 100 Amps in under 0.2 μs. The lower graphs within this figure show the Gate current pulse needed to turn this assembly of GTOs off. The peak Gate current was 70 Amps. Figure 6 shows the GTO assembly with the anode and gate bonded to gold foil ribbons, which are subsequently soldered to the substrate. High temperature solder (280 °C) was used to bond the GTO cathodes to the AlN

substrate. The test set up for this circuit minimized the inductance of the leads and had a snubber to account for the voltage overshoot that could cause latch-on.

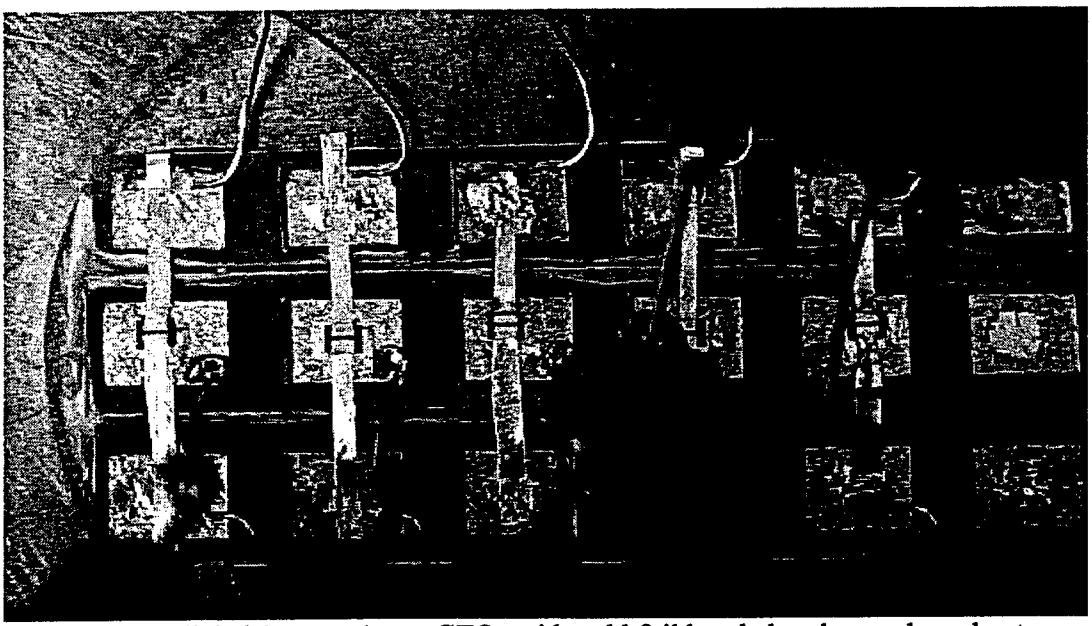


Figure 6: Paralleled 1 mm x 1 mm GTOs with gold foil bonded to the anode and gate contacts.

Conclusion

4H-SiC Asymmetric GTOs have been successfully fabricated with an optimized JTE. The use of this novel JTE leads to the ability of a 30 μm drift layer to support 3 kV breakdown voltages where others have used thicker epi layers to achieve the same. The thinner drift layer leads to a lower on resistance, 3 mΩ-cm^2, for high currents. The forward I-V temperature dependent data reveals the decrease in the forward voltage drop with temperatures as high as 300 °C operation. These GTOs also demonstrated the high current density (> 1600 A/cm^2) that SiC is capable of. The topside contact pads worked sufficiently to allow bonding over the interdigitated fingers. These pads were utilized in the 100 A hybrid GTO assembly and their use should ultimately lead to double sided cooling, enhancing future package performances.

Acknowledgements

The authors gratefully acknowledge support for this work from Ingham Mack of ONR, Dan Radack and John Zolper of DARPA, and Ben Damsky of EPRI (Contract MDA972-98-3-0009).

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Novel Ni-Based Ohmic Contacts To *n*-SiC For High Temperature and High Power Device Applications

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Abstract

Novel Pt/Ti/WSi/Ni composite ohmic contacts to *n*-SiC were investigated as a function of annealing temperatures up to 1000 °C. The onset of ohmic behavior occurred after annealing at 900 °C. Annealing at temperatures between 950 and 1000 °C yielded excellent ohmic behavior. At these temperatures the contact-SiC interface was smooth, defect free and characterized by a narrow Ni_2Si reaction region. The annealed contacts possessed smooth surface morphologies and exhibited minimal contact expansion. The residual carbon, resultant from SiC decomposition, was constrained by reaction with the WSi and Ti metallization layers forming carbide phases of W and Ti. The locations of the carbide phases were spatially distant from the metal semiconductor interface. The anneal optimized (annealed at 950 and 1000 °C for 30 s) Pt/Ti/WSi/Ni ohmic contacts to *n*-SiC were evaluated for thermal stability via pulsed/cyclic thermal fatigue and aging experiments at 650 °C. Negligible changes in the electrical properties, microstructure, and surface morphology/roughness were observed for both annealed ohmic contacts in response to 100 cycles of acute cyclic thermal fatigue. Aging of the 950 °C annealed contact for 75 hours at 650 °C resulted in electrical failure and chemical interdiffusion /reaction between the contact and SiC substrate. The 1000 °C annealed contact retained omicity after 100 h of aging and was found to be chemically and microstructurally stable. These findings indicate that the 1000 °C annealed Pt/Ti/WSi/Ni ohmic contact to *n*-SiC is thermally stable and merits strong potential for utilization in high temperature and pulsed power devices.

I. Introduction

Recently, wide bandgap semiconductors such as SiC have attracted much attention for high power, high temperature, high frequency, and high radiation tolerance device applications. It is the exceptional properties of SiC, such as, high breakdown field, large bandgap, high thermal conductivity and large electron saturation velocity, which are responsible for these device application interests [1, 2]. It has been reported that most SiC based electronic devices, which cannot sustain long-term operation at elevated temperature/power levels, suffered deterioration of their metal/SiC contacts [3]. Thus, an important concern for realization of SiC devices is the formation of low resistance ohmic contacts with good thermal, chemical, and mechanical stability. The development of such ohmic contacts serves to insure enhanced device reliability under the influence of high power and high temperature in-service operational stress.

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To date, many metallizations, namely, Ni, Al/Ni/Al, Cr, Al, Au-Ta, $TaSi_2$, W, Ta, Ti, Ti/Au, $TiSi_2$, Co, Hf, and WSi have been investigated for ohmic contacts to *n*-SiC [2-4]. Ni ohmic contacts have been suggested as superior candidates due to their reproducible low specific contact resistance, less than 5.0×10^{-6} ohms-cm^2, and deemed the industry standard ohmic contact to *n*-SiC [2, 4-6]. Fabrication of Ni ohmic contacts requires a post deposition anneal at temperatures ranging from 950 to 1000 °C. This anneal causes the Ni to react with SiC to form Ni_2Si and is responsible for achieving ohmic behavior [4, 6, 7]. However, the annealing process also causes undesirable features, namely, broadening of the metal SiC interface, a rough interface morphology heavily laden with Kirkendall voids, carbon segregation at the metal-SiC interface and/or throughout the metal layer, and substantial roughening of the contact surface [5-8]. Thus, even though Ni contacts possess excellent electrical properties, the above mentioned features will inhibit long term reliability and ultimately cause device failure via contact degradation and/or wire bond failure after exposure to extensive high power and high temperature device operational stresses.

The goal of this investigation was to eliminate the undesirable features (residual carbon, void formation, and rough surface morphology) associated with Ni ohmic contacts by designing, fabricating, and optimizing an improved ohmic contact, to *n*-SiC for high power and high temperature device applications. Subsequent to contact optimization the contact reliability was evaluated via both static and pulsed thermal stability-reliability testing.

II. Experiment

The Pt/Ti/WSi/Ni (100nm/25nm/80nm/40nm) composite metallization was sputter deposited (WSi) and e-beam evaporated (Ni, Ti, Pt) on research grade (0001) Si-faced 4H *n*-type (8.0×10^{18} cm^{-3}) SiC wafers. The samples were rapid thermally annealed (RTA) in an AG Associates rapid thermal annealing system for 30 s at 900, 950 and 1000 °C in a N_2 atmosphere. Material characterization was performed on the as-deposited and annealed samples. The contacts electrical quality was evaluated via current-voltage (I-V) characteristics using a HP 4140B semiconductor test system. Auger electron spectroscopy (AES) was used to chemically depth profile the different contact elements. The AES data was acquired using a Perkin-Elmer PHI660 scanning Auger microscope. A 5 keV electron beam was used to stimulate Auger transitions within the sample. In addition, a 4 keV Ar^+ ion beam was used to simultaneously sputter-etch the surface with a sputter rate of 10Å/s. In this way, elemental information as a function of depth was collected, that is, an Auger depth profile. Field emission scanning electron microscopy (FESEM) was utilized to assess the contact surface morphology, contact-SiC interface uniformity, and film microstructure. The surface morphology was also examined and quantified by a Digital Instrument's Dimension 3000 atomic force microscope (AFM) using tapping mode with amplitude modulation. The contact structure was analyzed by glancing-angle (5°) x-ray diffraction (GAXRD) via a Siemens D-5005 powder diffractometer using Cu K_α radiation at 50 kV and 40 mA.

The anneal optimized contacts (950 and 1000 °C annealed contacts) were subjected to

continuous thermal stress at 650 °C, referred to as static thermal fatigue or aging, for up to 100 hours in a tube furnace with an ambience of nitrogen. An identical set of contact samples were subjected to pulse or cyclic thermal stress. The pulse thermal fatigue tests were conducted in an AG Associates RTA system with an ambience of nitrogen, for 1, 10, 30 and 100 cycles at 650 °C with a pulse width of 10 s followed by a 60 s cool. In order to evaluate the electrical integrity of the contacts as a function of thermal fatigue duration, I-V measurements were acquired after specified intervals (after 1, 10, 40, and 100 cycles for pulsed thermal fatigue testing and after 1, 24, 50, 75, and 100 h for the aging experiments) of fatigue exposure. The contacts structural, compositional, microstructural, interfacial and surface quality were assessed prior and subsequent to thermal fatigue exposure.

III. Results and Discussion

The electrical, structural, and chemical properties of the Pt/Ti/WSi/Ni ohmic contacts to *n*-SiC were investigated as a function of annealing temperature. The I-V characteristics of the as-deposited and annealed composite contacts to *n*-SiC are displayed in Fig. 1. The as-deposited sample exhibited rectifying behavior suggestive of a large barrier height, typically 1 eV or greater. Annealing at 900 °C caused the I-V characteristics to move toward ohmic behavior. Ohmic behavior is demonstrated by I-V characteristics which posses linear characteristics with small resistance and are symmetric with reversal of voltage polarity. The contacts became fully ohmic after the 950 °C anneal. A slight reduction in resistance, with respect to the 950 °C annealed contact, was achieved after annealing at 1000 °C. Thus, annealing at temperatures between 900 and 1000 °C significantly enhanced the current conduction through the contacts.

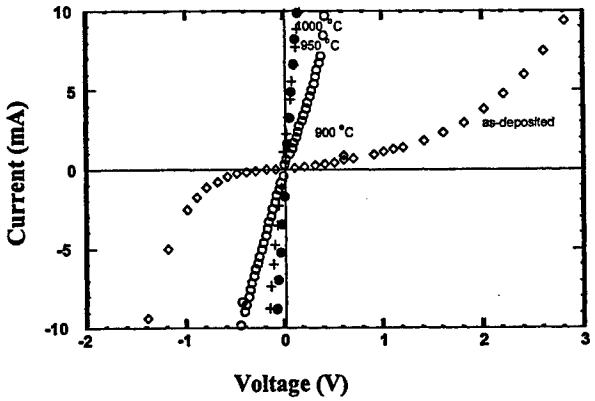


Figure 1: I-V characteristics of the as-deposited (open diamonds), 900 °C (open circles), 950 °C (crosses), and 1000 °C (filled circles) annealed Pt/Ti/WSi/Ni contacts to *n*-SiC.

In order to assess and understand the contacts electrical characteristics AES elemental depth profiles, GAXRD, and FESEM microstructural analyses were performed on the as-deposited and annealed samples. The AES depth profiles for the as-deposited and 1000 °C annealed samples are displayed in Fig. 2. In the case of the as-deposited Pt/Ti/WSi/Ni composite contact the layer structure between each of the contact metallizations remains

distinct. Figure 2a clearly shows that the top surface is composed of pure Pt. Underlying the Pt is a very well resolved Ti layer. The Ti layer shows signs of oxidation as evidenced by the oxygen signal peaking at ~18 at% at a sputter time of 250 s. The WSi and Ni layers are very distinct and show no evidence of mixing. The interface between Ni and SiC substrate is chemically abrupt; that is, there is no evidence of an interfacial oxide or interfacial chemical reactions upon sputter deposition. The AES depth profile of the 1000 °C annealed sample is shown in Fig. 2b. The individual contact metal layers are no longer distinct. Extensive intermixing has occurred in response to the 1000 °C heat treatment. A minimum of four layers are present within the contact metallization. The top or outer most layer is dominated by Pt, Ni, Si, and W signals and most likely consists of several phases or alloys. Underlying the surface alloy zone is a layer composed predominately of tungsten carbide. Beneath the tungsten-based layer is a region where the carbon signal displays a strong peak, 55 at. %, at a sputter time of 750 s. The position of the carbon peak coincides with the maximum in the Ti signal and is suggestive of TiC phase formation.

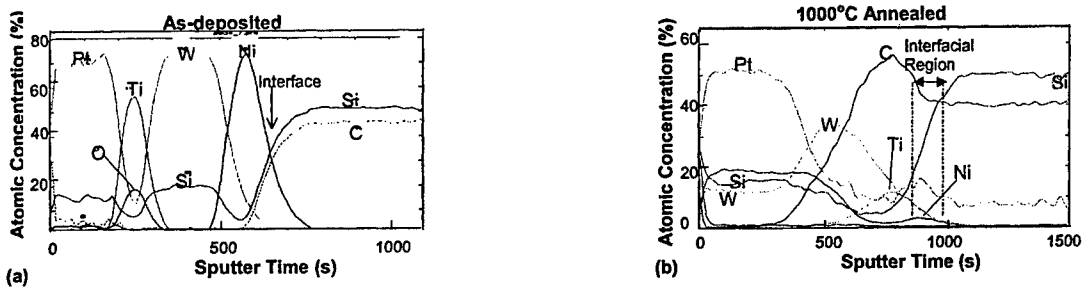


Figure 2: AES depth profile for (a) the as-deposited and (b) the 1000 °C annealed Pt/Ti/WSi/Ni metallization scheme on *n*-SiC.

The presence of TiC was confirmed by the GAXRD analysis. GAXRD analysis on the 1000 °C annealed sample revealed peaks at 41.7°, 72.35°, and 90.8° two theta which correspond to 2.16 Å, 1.30 Å, and 1.09Å d-spacings for TiC. The 20-80 at. % decay of the Si signal, between 850 s and 950 s sputter time, defines the metal-SiC interfacial region. Within this designated interfacial region exists a peak in the Ni signal. We suggest this to be evidence of a limited reaction region between Si and Ni resulting in Ni_2Si phase formation at the metal-SiC interface. Within this same area is a Pt peak, which has, been attributed to noise at the Pt energy level. The GAXRD data also supports the existence of the Ni_2Si phase at all annealing temperatures. The GAXRD analysis (not shown) detected peaks at 32.78°, 33.4°, 36.6°, 43.9°, 50.9 °, and 52.8° two theta which correspond to the d-spacings of 2.73 Å, 2.68 Å, 2.45 Å, 2.06 Å, 1.79 Å, and 1.73 Å matching the (221), (122), (212), (240), (401) and (041) reflections of δNi_2Si. It is well documented for Ni contacts on SiC that the SiC dissociates due to the strong reactivity of nickel above 400 °C, and that at ~900 °C the Ni_2Si stable phase is formed leading to carbon accumulation both at the interface and in the metal layer [2, 4, 5]. Additionally, the 850 °C isothermal section of the Ni-SiC-C ternary phase diagram is characterized by the absence of Ni-C compounds and therefore determined by the nickel-silicide, δNi_2Si (orthorhombic phase), which is in equilibrium with both, C and SiC

[7]. In this ternary phase diagram no Ni-SiC tie line exists, therefore, Ni is not in thermodynamic equilibrium with SiC. Thus, the AES profile data, GAXRD results, and the high temperature Ni-SiC phase equilibria, strongly support the existence of the Ni-Si reaction product, Ni_2Si, spatially adjacent to the SiC substrate. The AES depth profile for the 1000 °C annealed composite contact indicates that both the WSi and the Ti layers served to confine the residual carbon which was released from the dissociation of the SiC during the annealing process. These reactions, W-C and Ti-C, are extremely desirable from the standpoint of device reliability. Carbon inclusions at the metal-SiC interface and within the Ni_2Si contact layer are considered a potential source of electrical instability, especially after prolonged operation of the devices at high temperatures. At elevated temperatures redistribution of carbon inclusions will arise, resulting in significant degradation of the contact's electrical and microstructural properties. Thus, the WSi and Ti layers served to mitigate carbon segregation at the metal-SiC interface.

Carbon inclusions/segregation, are not the only reason for high power and temperature device operation reliability problems. The microstructure of the contact-SiC interface and nature of the contact surface both strongly influence device operational reliability. It has been established that annealing of Ni contacts on SiC causes extensive voiding (Kirkendall voids) at the original metal-SiC interface, a contact thickness which has been substantially expanded, and extreme surface roughness [5, 8]. The voids at the interface will cause internal stress and possible delamination of the contact layer which will compromise device reliability. The internal stress and contact delamination will be significantly amplified under the extreme thermal and electrical stresses typical of the power device operational environment and will ultimately result in device failure. For device applications, ohmic contacts must be wire bonded to a die package. A rough surface morphology will most likely cause wire bonding difficulty and/or failure under the extreme thermal fatigue during high power and high temperature device operation.

Figure 3 displays the FESEM secondary electron cross-sectional images of the as-deposited and 1000 °C annealed contacts to SiC. The metal-SiC interfaces are morphologically abrupt and show no evidence of void formation or contact delamination as a result of the annealing process up to 1000 °C. The distinct metal layers in the as-deposited contact are noted in Fig. 3a. Comparison of the as-deposited and 1000 °C annealed FESEM images in Fig. 3 not only confirms the abrupt void free interface morphology but also reveals that there is minimal increase (<6%) in contact thickness as a result of annealing. Suppression of contact expansion during annealing is due to restricted interfacial contact growth, that is, a narrow Ni-SiC reaction zone. Specifically, deposition of a thin Ni layer, 40 nm, as opposed to the usual 100-200 nm of Ni traditionally employed results in a significantly limited Ni-SiC reaction zone. This mitigated contact growth after heat treatment makes the Pt/Ti/WSi/Ni composite contact an excellent choice for device designs, which possess shallow p-n junctions.

Plan-view FESEM analyses determined that the annealed surfaces remain smooth with evidence of grain growth. Quantitative analysis of surface roughness, an AFM plot of the

average surface roughness (R_{av}) as a function of annealing temperature, is displayed in Fig. 4. The extreme smoothness of the as-deposited contact surface is substantiated by a surface roughness value, R_{av}, of ~0.7 nm. This value remains essentially constant throughout all the heat treatments. Thus, the surface morphology of the annealed composite contact possesses the smoothness required for strong reliable wire bonding and should maintain excellent wire-contact mechanical durability during high power/temperature device operation.

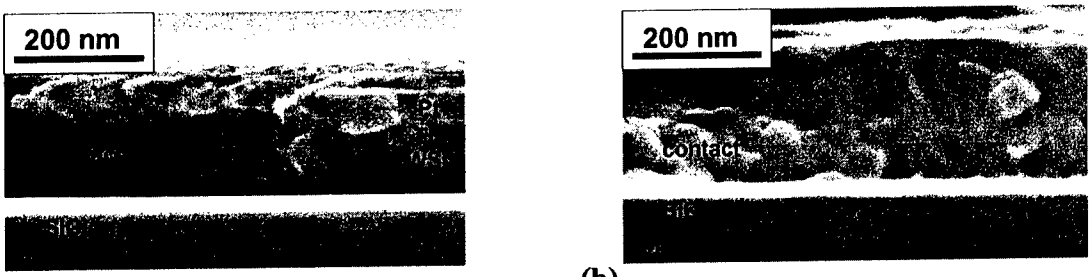


Figure 3: Cross-sectional FESEM micrographs of the (a) as-deposited and (b) 1000 °C annealed Pt/Ti/WSi/Ni composite contact to *n*-SiC.

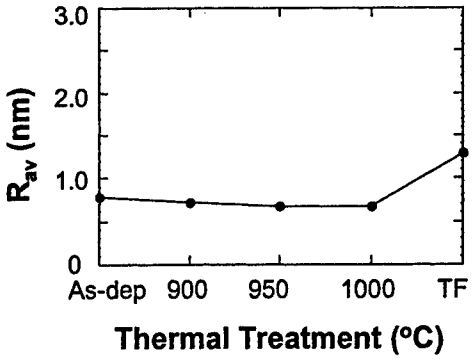


Figure 4: AFM data showing the average surface roughness, R_{av}, of the Pt/Ti/WSi/Ni contact to *n*-SiC as a function of annealing temperatures up to 1000 °C. TF represents the R_{av} of the 1000 °C annealed contact after exposure to 100 cycles of thermal fatigue at 650 °C.

In order to evaluate device component performance-reliability for pulsed power and /or high power device applications the anneal-optimized (RTA at 950 and 1000 °C for 30 s) Pt/Ti/WSi/Ni-SiC ohmic contacts were subjected to pulsed thermal fatigue testing for up to 100 cycles at 650 °C. The current-voltage characteristics were assessed after exposure to 1, 10 and 100 cycles of thermal fatigue and are displayed in Fig. 5. Figure 5 shows that the contacts initially annealed at both temperatures exhibited similar electrical performance in response to the pulsed thermal stress. The I-V characteristics remained stable, showing little deviation from that of the initial annealed ohmic contact, after exposure to 100 cycles of pulsed thermal fatigue at 650 °C. Assessment of the microstructure in response to pulsed thermal fatigue was achieved via cross-sectional FESEM. The microstructure of the ohmic

contact exposed to 100 cycles of thermal fatigue at 650 °C appeared similar in structure to that of the un-fatigued contact. The fatigued contact exhibited no evidence of nanocracks, or other structural defects associated with potential physical-mechanical contact failure. The fact that the electrical integrity and metal-SiC interfacial microstructure were not significantly altered by the pulsed thermal cycling bodes well for the use of this ohmic contact in pulsed high power devices.

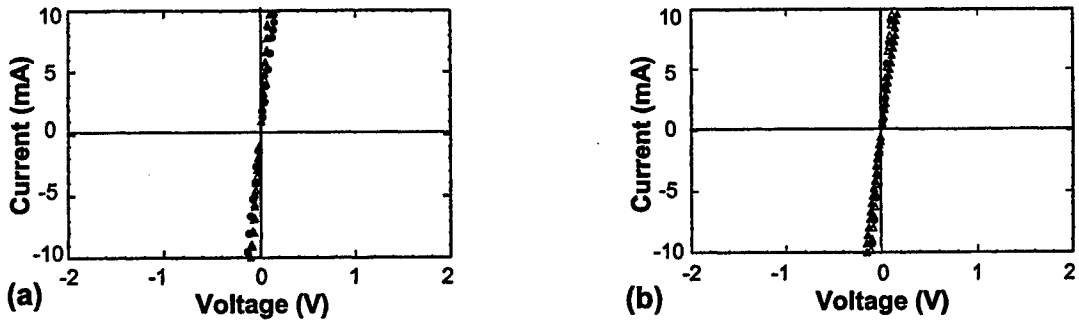


Figure 5: I-V characteristics of the 650 °C pulsed thermal fatigued contact initially annealed at (a) 950 °C and (b) 1000 °C. The initial annealed contacts are represented by filled circles and the samples fatigued for 10 and 100 cycles are represented by open and filled triangles, respectively.

For device applications, ohmic contacts must be wire bonded to a die package. Maintenance of a smooth surface morphology is essential to insure good wire bonding and uniformity of current flow. A post fabrication anneal or fatigue-induced rough surface morphology (tens to hundreds of nanometers) will most likely cause wire bond failure. Temperature-induced surface roughness, indicative of interface roughness, which generates excessive stress in the underlying SiC substrate, can result in a SiC polytype change, which causes modification of the device's electrical properties. Quantitative analysis of surface roughness, via AFM, for both the un-fatigued and pulsed thermal fatigued contacts is shown in Fig. 4. The contacts annealed at both annealing temperatures exhibited extremely smooth surfaces. However, after 100 cycles of pulsed thermal fatigue the contacts surface morphology exhibited an increase in the average surface roughness, from 0.7 nm (initial annealed contact) to 1.3 nm. This increase in surface roughness is minimal with respect to the contact thickness, and the actual value of R_{av} is substantially less that other that of other un-fatigued annealed ohmic contacts cited in the technical literature [3, 5]. Thus, the average surface roughness, before and after exposure to pulsed thermal fatigue, is considered negligible and should not be an influencing factor for wire bond failure and/or electrical degradation. Additionally, the fact that the contact metal did not delaminate as a result of the thermal cycling indicates strong adhesion of the metal contact to the SiC substrate.

Static thermal fatigue/aging experiments were performed on the contacts in order to evaluate their performance for high temperature device applications. Identical contacts to those utilized for pulsed thermal fatigue testing, (initially annealed at both 950 and 1000 °C)

were exposed to static thermal stability/aging tests for various times up to 100 h at 650 °C in an N_2 ambience. The contacts were electrically evaluated after 1, 24, 50, 75, and 100 hrs of aging, and the I-V characteristics of the initially annealed (950 and 1000 °C) and static thermally fatigued contacts are shown in Fig. 6. The I-V characteristics of the 950 °C annealed ohmic contacts aged for up to 50 h maintained good ohmicity, however, an increase in resistance with respect to that of the un-aged contact was noted. This contact became rectifying after 75 h of aging. In contrast, the 1000 °C annealed ohmic contact maintained I-V linearity, with an increase in resistance, after aging for up to 75 h. After 100 h of aging the I-V characteristics exhibited a further increase in resistance, however, the contact did not become rectifying. Thus, the ohmic contact which had been initially annealed at 1000 °C, appears to be more electrically stable in response to long term aging than the 950 °C annealed ohmic contact.

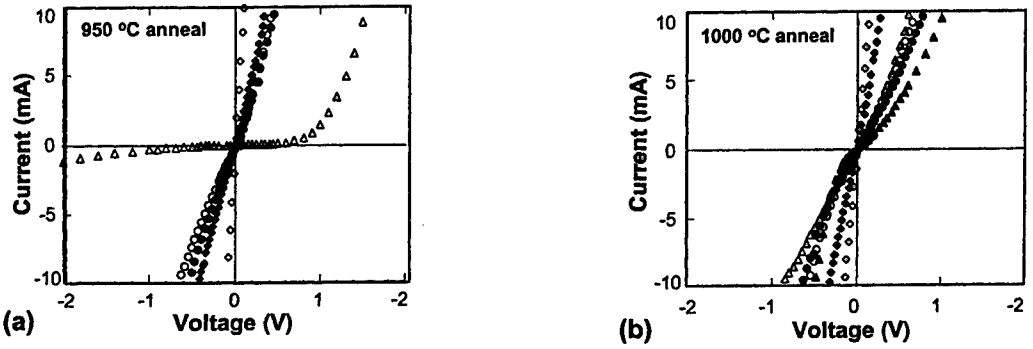


Figure 6: I-V characteristics of the 650 °C aged Pt/Ti/WSi/Ni-*n*SiC ohmic contacts initially annealed at (a) 950 °C for 30 s and (b) 1000 °C for 30 s. The initial annealed samples are represented by open diamonds, and the samples aged for 1, 24, 50, 75 and 100 h are represented by filled diamonds, open circles, filled circles, open triangles, and filled triangles, respectively.

In order to identify the source(s) of degradation of the aged 950 °C annealed ohmic contact, the 950 and 1000 °C annealed contacts were characterized via FESEM and RBS. The cross-sectional microstructure of the 950 and 1000 °C annealed contacts after exposure to 75 h of aging appeared identical. The metal-SiC interface appeared structurally abrupt with no evidence of degradation via metal-SiC interface modification. The surface morphology of both samples also appeared similar, with no evidence of thermally induced surface heterogeneity, roughening, nanocracks or pit formation. The RBS spectra for the annealed contacts (RTA at 950 and 1000 °C for 30 s) before and after aging (650 °C for 75 h) are displayed in Fig. 7. The static thermal fatigue/aging treatment of the 950 °C contact modified the RBS spectrum, with respect to that of the unaged 950 °C annealed contact, by shifting the "back edge" of the RBS peak (around 1440 keV) to a lower energy (Fig. 7a). This shift is indicative of a net movement of the contact material into the SiC substrate in response to the long-term static thermal fatigue/aging. Figure 7b shows that the back edge of

the 1000 °C contact metallization remained relatively unchanged after the same treatment, indicating that the contact-SiC interface experienced little or no reaction/diffusion. This result is in agreement with the electrical measurements which showed rectifying characteristics for the 75 h aged 950 °C annealed contact and ohmic behavior for the 1000 °C annealed contact aged for 100 h. The RBS results suggest that the 1000 °C annealed Pt/Ti/WSi/Ni contact must have undergone a more complete interfacial reaction with the SiC during the initial annealing process such that the driving force for any further interfacial reaction was exhausted. In contrast, the fact that the 950 °C annealed contact experienced elemental diffusion and/or interfacial reactions which resulted in electrical degradation after long term aging suggests that the metal-SiC had not fully reacted at the initial annealing temperature of 950 °C. Thus, even though this contact initially displayed acceptable electrical behavior after annealing at 950 °C, exposure to prolonged thermal aging at 650 °C caused the electrical integrity of the contact to degrade. The results suggest that the 950 °C annealed contact was not in complete thermodynamic equilibrium with SiC, and prolonged exposure at elevated temperature during aging allowed the contact metallization to continue to react with the SiC substrate, resulting in electrical degradation.

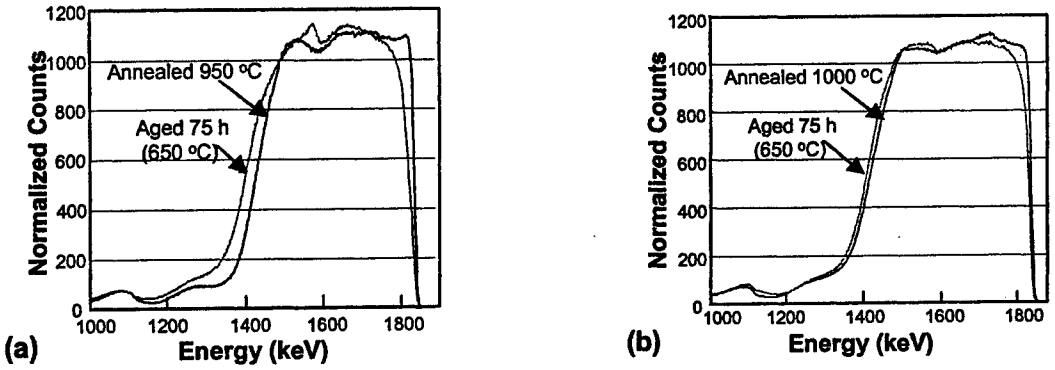


Figure 7: RBS spectra of the Pt/Ti/WSi/Ni ohmic contacts to *n*-SiC aged for 75 h at 650 °C subsequent to the initial anneals at (a) 950 °C and (b) 1000 °C for 30 s.

IV. SUMMARY

We have achieved excellent electrical properties for Pt/Ti/WSi/Ni ohmic contacts to *n*-SiC annealed between 950 and 1000 °C for 30 s. The excellent electrical properties were paralleled by the formation of a narrow Ni_2Si interfacial reaction zone, minimal contact broadening, and a smooth, abrupt, and void free contact-SiC interface. The residual carbon, resultant from the reaction of SiC with the overlying Ni, was confined by Ti-carbide and W-carbide phases spatially distant from the contact-SiC interface. Thus, the detrimental effects of contact delamination due to stress associated with interfacial voiding, and wire bond failure due to extreme surface roughness, have been eliminated for this composite ohmic contact. Additionally, electrical instability associated with carbon inclusions at the contact-SiC interface after prolonged high temperature and high power device operation has also

been eliminated. The thermal stability of Pt/Ti/WSi/Ni ohmic contacts to *n*-SiC was assessed via acute pulsed/cyclic thermal fatigue and long term thermal aging experiments. The 950 and 1000 °C annealed ohmic contacts exhibited excellent electrical and microstructural stability in response to acute pulsed thermal fatigue at 650 °C for up to 100 cycles. The absence of observed surface and metal-SiC interfacial modification in combination with the stable electrical characteristics demonstrates strong potential for application of this contact metallization in pulsed power device applications. Aging at 650 °C resulted in contact failure for the 950 °C annealed contact after 75 hours and ohmic behavior for the 1000 °C annealed contact after 100 hours of exposure. The RBS results indicate that the 1000 °C annealed contact underwent complete interfacial reaction with SiC during the initial anneal, but the 950 °C annealed contact experienced further elemental diffusion and/or interfacial reactions in response to prolonged exposure at elevated temperature, resulting in electrical degradation. It is suggested that oxidation of both contacts contributed to the slight increase in contact resistance observed during aging. Results of this investigation demonstrates that the 1000 °C annealed Pt/Ti/WSi/Ni ohmic contact to *n*-SiC merits beneficial potential for both high temperature and high (pulsed) power device applications.

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Channel Recessed 4H-SiC MESFETs with F_t of 14.5GHz and F_{max} of 40GHz

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Abstract

Channel recessed 4H-SiC MESFETs have demonstrated excellent small signal characteristics and the effect of Si_3N_4 passivation on these devices has been studied in this work. A saturated current of 250-270 mA/mm and a maximum transconductance of 40-45 mS/mm were measured for these devices. The 3-terminal breakdown voltage V_{ds} ranges from 120 V to more than 150 V, depending on gate-drain spacing. 2 x 200 μm devices with 0.45 μm gate length show high F_t of 14.5 GHz and F_{max} of 40 GHz. After Si_3N_4 passivation, the output power and PAE were increased by 40% and 16%, respectively, for CW power measurement. Other measurements, such as, the change in surface potential and the dispersion of the drain current make it clear that the passivation of SiC MESFETs reduces the surface effects and enhances the RF power performance by suppressing the instability in DC characteristics.

I. Introduction

SiC MESFETs have emerged as promising high power microwave devices due to unique material properties, such as, high saturated electron velocity, high breakdown field, and high thermal conductivity. Wide bandgap semiconductor devices, such as, GaN HEMTs and SiC MESFETs have been developed for high power applications and have shown great potentials in comparison to GaAs and other commercially available devices. SiC MESFETs show better linearity than GaN HEMTs but operate at lower frequencies.

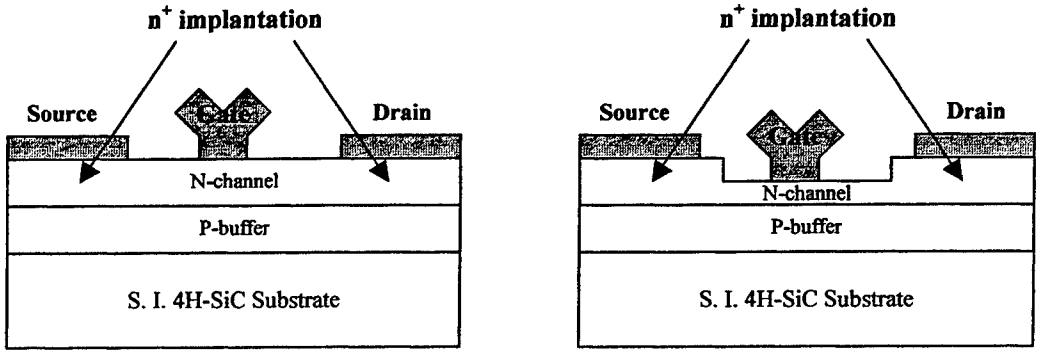
In this work, channel recessed 4H-SiC MESFETs were fabricated and they have demonstrated excellent small signal characteristics, such as, F_t of 14.5GHz and F_{max} of 40GHz. The device performance was compared to the case without channel recess that has also been fabricated on the same material. The improvement in small signal characteristics can be explained by a decrease in feedback capacitance and higher aspect ratio (L_g/a) that can enhance channel modulation and increase the ratio of G_m/G_o.

SiC MESFETs have been reported to have current instability and strong dispersion [1]. We present the effect of Si_3N_4 passivation on 4H-SiC MESFETs by measuring the instability of DC drain current, the dispersion of drain current with input power, the change in surface potential, etc. The Si_3N_4 passivation reduced surface trapping effect and enhanced the power performance. From our measurements, however, we found out that both the surface trapping and deep traps in the substrate can be responsible for the instability in SiC MESFETs.

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II. Device Fabrication

The material structure consisted of a semi-insulating 4H-SiC substrate, a 0.25 μm p-type buffer layer doped < 5 x 10^{15} cm^{-3}, and a 0.26 μm n-type channel layer doped N_d = 2 x 10^{17} cm^{-3}. The cross-sectional device designs are shown in Figure 1. Type I has no recess but type II has a channel recess region between source and drain. Source and drain regions were implanted with phosphorous. Ni deposition followed by annealing at 980°C resulted in a specific contact resistance of 1.5 x 10^{-6} Ω-cm^2. ECR etching with a $Cl_2/CH_4/Ar$ gas mixture was used to define the mesa and etch the channel region. The channel region between source and drain was etched 0.06 μm for the channel recessed device (Type II). The T-shaped gates were fabricated by multi-layer e-beam lithography process using a Cambridge EBMF10.5. The gates consisted of Ni/Pt/Au metal structure. A 1 μm thick Au layer was deposited as a pad and an ohmic overlay metal. PECVD Si_3N_4 passivation was done before the air-bridge step. The gate length was 0.4 μm and 0.45 μm for type I and type II, respectively. The source-to-gate spacing is fixed at 0.5 μm and the gate-to-drain spacings varied from 1.0 μm to 1.5 μm.



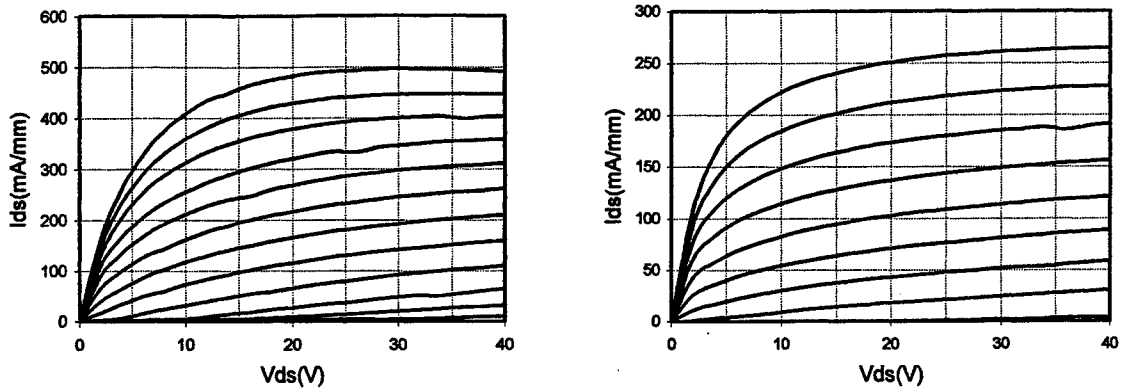
(a) Normal 4H-SiC MESFET without recess (Type I) (b) Channel recessed 4H-SiC MESFET (Type II)

Fig. 1. Cross-sectional design of 4H-SiC MESFETs utilizing phosphorus n^+ implantation

III. Results and Discussion

A. DC and Small Signal Characteristics

Figure 2 shows typical I-V characteristics of each type. Type I (Figure 2 (a)) showed higher current density but lower transconductance and lower breakdown voltage, as expected from no recess. A saturated current of 500 mA/mm and a maximum transconductance of 30 mS/mm were measured. According to the measurement, the pinch-off voltage, V_{gs}, is estimated to be less than -20V but the devices still showed a gate leakage of a few mA/mm for drain voltages greater than ~50V. The 3-terminal on-state breakdown voltage of 90V was observed. Type II, which had a channel recess, showed higher transconductance and breakdown voltage compared to type I. A saturated current of 250-270mA/mm and a maxium transconductance of 40-45mS/mm were measured. Negligible gate leakage (< nA/mm) was observed and a pinch-off voltage, V_{gs} ~ -8V was measured. The off-state 3-terminal breakdown voltage, V_{ds}, range from 120 V to more than 150 V at V_{gs} =-14V, depending on gate-drain spacing.



(a) Type I, Top trace is for V_{gs} = 0V, ΔV = -2V (b) Type II, Top trace is for V_{gs} = 0V, ΔV= -1 V

Fig. 2. I-V characteristics of each type of devices

The unit current gain cut-off frequency (F_t) and maximun oscillation frequency (F_{max}) were extracted from s-parameters measured on-wafer using HP8510 network analyzer. This small signal measurement was done at V_{ds} = 20V and V_{gs} = -2V. Table I shows the values of F_t and F_{max} for each type of devices.

Table I. Small signal characteristics

	Cutt-off frequency (F_t)		Maximun oscillation frequency (F_{max})	
	Type I	Type II	Type I	Type II
2 x 100 μm	12.6 GHz	13.8 GHz	28 GHz	41 GHz
2 x 200 μm	N.A.	14.5 GHz	N.A.	40 GHz
2 x 300 μm	15.0 GHz	15.4 GHz	23 GHz	33 GHz
2 x 500 μm	18 GHz	16.0 GHz	17 GHz	18 GHz

We observed a trend in the small signal measurements with different unit gate width. The cut-off frequency increases with unit gate width due to higher gate capacitance. It is more significant on type I than type II. The highest F_t of 18GHz was obtained for 2 x 500 μm type I devices. As for shorter gate widths, higher F_t and F_{max} were obtained for type II devices. 2 x 200 μm type II devices demonstrated excellent F_t and F_{max} of 14.5 GHz and 40 GHz, respectively. Especially, F_{max} was significantly improved compared to type I (with F_{max} of 28 GHz). The improvement in small signal characteristics can be explained by considering the aspect ratio and feedback capacitance. The F_t and F_{max} of the device can be expressed by,

$$F_t = \frac{G_m}{2 \cdot \pi \cdot \left(C_{gs} + C_{gd}\right)} \quad (1)$$

$$F_{max} = \frac{F_t}{\sqrt{4\frac{Go}{Gm}\left(G_m \cdot R_i + \frac{Rs+Rg}{1/Gm+Rs}\right) + \frac{4}{5}\frac{Cgd}{Cgs}\left(1+\frac{2.5Cgd}{Cgs}\right)}(1+G_m \cdot R_s)^2} \quad (2)$$

The behavior of f_{max} is considerably more complicated since its value depends on the device resistances and feedback capacitance. The channel recess makes the depletion region between gate and drain extend more toward the edge of the drain, which can contribute to the decrease in the feedback capacitance. The channel recess also leads to higher aspect ratio (L_g/a), which improves channel modulation and increases the ratio of G_m/G_o. Therefore, the combination of high F_t, C_{gs}/C_{gd}, and G_m/G_o is a possible explanation for this dramatic improvement of F_{max}.

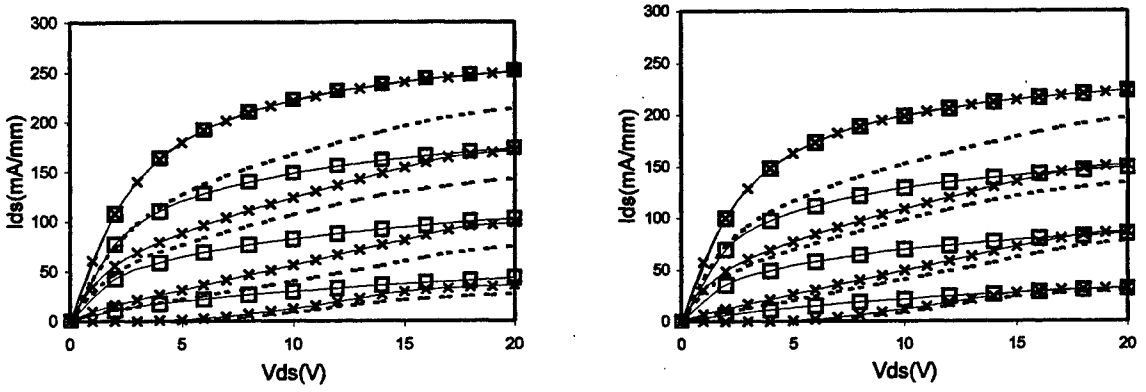
B. Current Instability and Passivation

SiC MESFETs have been reported to have current instability and strong dispersion. This phenomenon has been reported using a pulse IV measurement [1]. In this work, we illustrate this phenomenon by measuring IV characteristics using different bias sweeping method and surface potential using surface probing technique. These measurements were repeated under the same conditions after Si_3N_4 passivation. Figure 3 (a) shows the current instability of type II before passivation. Three different voltage sweeping were performed as followings.

(1) Case I (-□-) : From V_{gs} = 0V to V_{gs} = -10V with 100sec time interval between sweeps
From V_{ds} = 0V to V_{ds} = 20V (forward) at each gate bias
(2) Case II (-×-) : From V_{gs} = 0V to V_{gs} = -10V, No time interval
From V_{ds} = 0V to V_{ds} = 20V (forward) at each gate bias
(1) Case III (----) : From V_{gs} = -10V to V_{gs} = 0V, No time interval
From V_{ds} = 20V to V_{ds} = 0V (backward) at each gate bias

The gate voltage step was 1V, but only the cases of V_{gs} = 0V, -2V, -4V, and –6V were plotted for better understanding. The measurement for case I (-□-) was done with the time interval of 100sec between each gate voltage sweep while the others were done continuously. The time interval of 100sec is assumed to be enough to recover the state. Top two traces in Figure 3 are consistent with each other because of the same initial condition. We found discrepancy among different sweeping methods. For case II (-×-), current lag was observed and it was more significant at low drain voltages. The current recovers after reaching higher drain voltages. We speculate that trapping of electrons at the surface states and deep states in the substrate affect current lag phenomenon. With applied high drain bias, electrons can tunnel from the gate and move across the surface depletion region getting trapped at the surface states. In addition, electrons in the channel can pass through thin p-type buffer layer which is fully depleted under the high reverse bias condition and get trapped in the deep states present in the substrate [2]. Even after the drain voltage is disconnected (after the first sweep), the trapped electrons remain until they are slowly detrapped from the states. Consequently, unintentional depletion region is formed near the surface and lower channel region by the remaining electrons. Now, the channel area becomes thinner compared to the initial condition so that the channel current becomes lower. In the next sweep, this unintentional depletion region becomes covered by the extension of the gate-to-drain depletion and the p-n junction depletion as the applied drain voltage becomes higher again. Therefore, the current level recovers at higher drain bias region. Reasonably, this lag phenomenon is more serious for case III (----) because the higher field was applied between gate and drain at the previous sweep. Figure 3 (b) shows the same measurement result after passivation. Similar trends were observed but with noticeable improvement after passivation. This improvement was observed more significantly for the normal devices without channel recess.

To verify the effect of passivation on the surface, we also measured surface potential by using Kelvin probe technique. Detailed measurement procedures have been described elsewhere [3]. After stressing the device for 2 minutes with the drain voltage of 20V under the pinch-off condition, surface potential was measured versus time. Figure 4 shows the recovery of surface current versus time before and after passivation. Much faster recovery was observed after passivation, which proves that passivation reduces surface effect. In Figure 3 (b), however, current instability was not improved significantly. Surface treatment reduces instability, but not completely. We propose that current instability is caused not only by surface traps but also by deep traps in the substrate.



(a) Before passivation (b) After passivation

Fig. 3. Current instability before and after passivation (—□— : Forward drain voltage sweep with the time interval of 100sec for each gate bias, —x—: Forward drain voltage sweep from V_{gs} = 0 V toward –10 V without time interval, ——— : Backward drain voltage sweep from V_{gs} = –10 V toward 0 V without time interval)

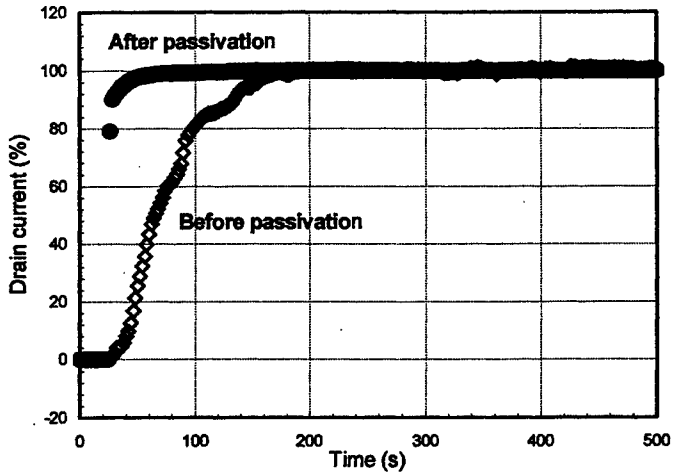


Fig. 4. The recovery of the surface current before and after passivation

Figure 5 shows the gate leakage current measured before and after passivation. Lower leakage current was observed after passivation for lower drain bias. However, it increases rapidly for higher drain bias in comparison to those before passivation. Passivation seems to prevent electrons from tunneling from the gate for lower drain bias but accelerate the tunneling mechanism for higher drain bias. The tunneling mechanism is closely related to temperature. Increased temperature on the surface around the gate in the high field region produces a decreased threshold voltage for the tunnel leakage so that thermally induced electrons can easily tunnel from the gate. [4] We speculate that it is more difficult to eliminate the increased surface temperature after passivation because the surface is blocked by passivation film. The thermal conductivity of Si_3N_4 is much less than that of SiC. Therefore, although passivation reduces the surface effect and suppress gate leakage for lower drain bias, more electrons can tunnel from the gate for higher drain bias by obtaining the thermal energy. These electrons flow toward the drain edge for higher drain bias, while most tunneling electrons can't arrive at the drain edge for lower drain bias. Moreover, passivation reduces the number of trapped electrons and therefore induces more electrons to reach the drain edge for higher drain bias. This can explain why the breakdown voltage reduces after passivation although the gate leakage current is lower for lower drain bias.

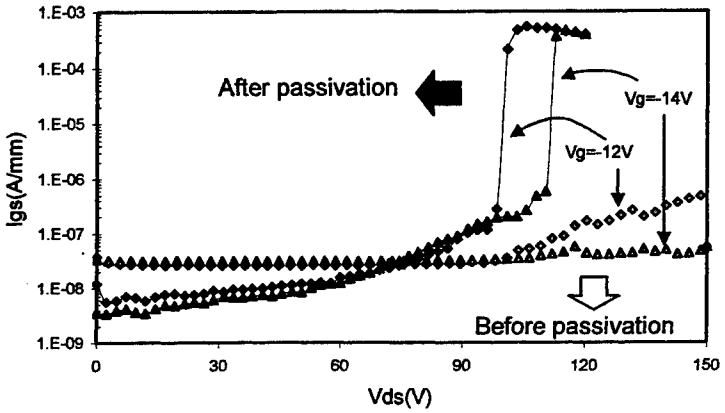
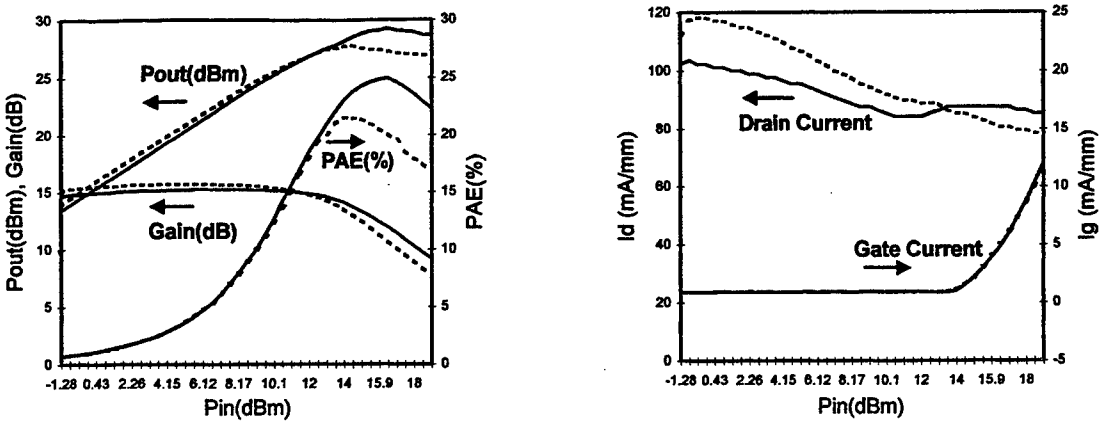


Fig. 5. Gate leakage current before and after passivation.

As shown previously, the channel recess resulted in lower saturation current but higher breakdown voltage. Figure 6 shows CW power measurements before and after passivation. CW power measurement was performed at 4 GHz with V_{ds}=30 V due to our measurement system limitation. The output power, gain, and PAE are plotted in Figure 6 (a) and the drain and gate current are plotted in Figure 6 (b). The unpassivated device showed output power density of 0.6 W/mm with the power gain of 15 dB and PAE of 20 %. Due to insufficient power sweeping at low drain bias, it showed relatively low output power. Compared to normal devices, the output power is a little lower but the power gain and PAE were improved. Especially, as expected from thinner channel region, the power gain was increased significantly, by a factor of 2. After passivation, the output power density of 0.85 W/mm was measured with PAE of 25% and a similar power gain for the channel recessed device. Although, the saturated current became lower after passivation, the output power and PAE were improved. This can be explained by investigating the drain current behavior versus input power in Figure 6 (b). While the drain current decreased continuously by 20-30% with input power before passivation, it decreased much less after passivation. This resulted in higher output power density and PAE compared to the unpassivated device for higher input power levels. The current drop reflects the instability in DC drain current shown in Figure 3.



(a) Output power, Gain, and PAE (b) Drain current dispersion versus input power

Fig. 6. CW power measurement before and after passivation at 4GHz (Vds=30V)
(Dashed lines : Before passivation, Solid lines : After passivation)

IV. Conclusion

Channel recessed 4H-SiC MESFETs have been fabricated and compared to normal devices without channel recess. The channel recess resulted in lower saturated current but higher breakdown voltage and excellent small signal characteristics. The cut-off frequency of 14.5 GHz and the maximum oscillation frequency of 40 GHz were measured on 2 x 200 μm devices with a gate length of 0.45 μm.

The current instability was observed by measuring I-V characteristics and surface potential. Si_3N_4 passivation improved current instability by reducing surface effects but cannot eliminate it completely. From these measurements, we propose that trapped electrons both on the surface and in the substrate modulate channel thickness by producing unintentional depletion region and therefore reducing the drain current.

Passivation reduces the gate leakage current for lower drain bias, but accelerates tunneling mechanism for higher drain bias. We speculate that the passivation film deposited on the surface makes it difficult to eliminate the increased surface temperature due to lower thermal conductivity. Therefore, thermally induced electrons can easily tunnel from the gate in the high field region and flow toward the drain to accelerate breakdown mechanism. Passivation also improves RF performance by suppressing the drain current dispersion with input power.

From our measurements, Si_3N_4 passivation on SiC MESFETs enhances device performance noticeably by the reduction of surface effects. However, it doesn't seem to be enough to completely eliminate the current instability. More study of deep traps in the substrate should be performed.

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Acknowledgements

This work was supported by the GE Corporate Research & Development and was performed in part at the Cornell Nanfabrication Facility (a member of the National Nanofabrication Users Network).

Inversion Channel MOSFETs in 3C-SiC on Silicon

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Abstract

As a substrate material, single crystal SiC wafers are commercially available in diameters up to 75 mm, whereas silicon wafers are available in diameters of 200 – 300 mm. SiC wafers remain quite expensive compared to silicon, and contain troublesome densities of micropipes that limit the yield of large devices. In the past, several groups have attempted to circumvent these problems by fabricating devices in 3C-SiC films grown epitaxially on silicon substrates, with limited success. However, in this paper we report new results demonstrating high quality inversion channel MOSFETs in 3C-SiC films on silicon.

The inversion channel mobility of SiC MOSFETs has been limited to < 50 cm^2/Vs in the 4H polytype and < 100 cm^2/Vs in the 6H polytype by a high density of interface states in the upper half of the bandgap. Because of its narrower bandgap, the 3C polytype of SiC is expected to have lower interface state density, leading to higher channel mobilities.

We fabricated lateral n-channel MOSFETs in 6 μm p-type epilayers of 3C-SiC grown on 2° off-axis Si(001) substrates. The epilayers were subsequently polished to improve surface smoothness, leaving a 3 μm layer. Sacrificial oxidation was then performed to remove damage caused by polishing. Source and drains were formed by implanting phosphorus and activating at 1250 °C for 30 minutes in argon. The gate oxide was formed by wet oxidation at 1150 °C for 30 minutes, followed by re-oxidation in wet O_2 at 950 °C for two hours. A polysilicon gate was deposited by LPCVD and doped by spin-on dopant. Ohmic contacts are unannealed nickel. The resulting MOSFETs show excellent transistor behavior, with good current saturation, a threshold voltage of 1.6 V, and a peak channel mobility of 170 cm^2/Vs.

I. Introduction

Because of its wide band gap (2.2eV-3.2eV depending on polytype) and excellent thermal conductivity, silicon carbide (SiC) is an ideal semiconductor material for high power, high voltage and high temperature applications. While many high performance power devices have been demonstrated on 4H- and 6H-SiC wafers [1-3], far fewer devices on 3C-SiC have been demonstrated. There exists no substrates of 3C polytype, and 3C epilayers are grown heteroepitaxially on large area silicon substrates by chemical vapor deposition (CVD) [4]. Earlier attempts in 1980's to fabricate metal-oxide-semiconductor field-effect transistors (MOSFET) in 3C-SiC showed large drain leakage current [5] or poor current saturation [6].

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These poor results were due to the high defect density in 3C-SiC epilayers and poorly developed process techniques for 3C-SiC devices.

The improvement of 3C-SiC epitaxial growth and the availability of more mature SiC processing technology have lead to a renewed interest in 3C-SiC materials and devices. The inversion channel mobility of SiC MOSFETs has been limited to < 50 cm^2/Vs in the 4H polytype and < 100 cm^2/Vs in the 6H polytype by a high density of interface states in the upper half of the bandgap. In contrast, 3C-SiC MOSFET's have demonstrated an effective channel mobility about 100 cm^2/Vs [6]. The potential for integrating SiC with Si technology has also become feasible with the improvements made in SiC processing. In this paper, we report inversion-type n-channel 3C-SiC MOSFET's fabricated on Si(001) substrates which show excellent transistor behavior and a channel mobility of 170 cm^2/Vs. Subthreshold characteristics and gate oxide integrity are also evaluated.

II. Device fabrication

A 6-μm-thick, p-type 3C-SiC (2×10^{17} cm^{-3}) epilayer was grown on a 2° off-axis p-type Si(001) substrate by CVD, with silane and propane as precursors. The epilayer was subsequently polished by a chemical mechanic polishing (CMP) process to improve surface smoothness, leaving a 3 μm layer. Sacrificial oxidation was performed to remove lattice damage caused by polishing. A carefully-designed phosphorus implantation scheme, including four implantations, with energies and doses of 360 keV/1.5×10^{15} cm^{-2}, 220 keV/1.1×10^{15} cm^{-2}, 100 keV/8×10^{14} cm^{-2} and 30 keV/6×10^{14} cm^{-2}, respectively, was employed to form a uniform doping profile in the source and drain regions of the MOSFET. The resulting source/drain junction depth was about 500 nm. The implantation mask was a Ti(10 nm)/Au(80 nm) metal bilayer. Following implantation, the sample was annealed at 1250 °C for 30 minutes in argon to activate the implanted dopants. An RCA cleaning procedure was performed immediately before the sample was loaded into a pyrogenic oxidation system. An oxidation procedure optimized for 4H-SiC was used, which consisted of wet oxidation at 1150 °C for 2.5 hours, argon annealing at 1150 °C for 30 minutes, and reoxidation at 950 °C for 2 hours. The oxidation rate of 3C-SiC is about 2-3 times higher than that of 4H-SiC and, therefore, the oxidation time was reduced to 40 minutes to produce an 80-nm-thick gate oxide. A poly-silicon gate (400 nm thick) was deposited by LPCVD and was subsequently doped by spin-on phosphorus dopant. The gate was defined using wet etching (HNO_3:HF:H_2O=55:3:30). Finally, contact windows were opened in the source and drain regions by wet etching the oxide, and a 200 nm-thick nickel layer was evaporated to form ohmic contacts. Aluminum was deposited on the backside of the sample to form an ohmic contact to the p-type silicon substrate. Due to processing constraints, alloying of ohmic contacts was not performed yet.

Figure 1 shows a schematic cross-section of the 3C-SiC MOSFET device. Devices with a gate width of 110 μm and various gate lengths of 3, 5, 10, 20, 50, 80, 110 and 140 μm were fabricated. All devices were a planar structure with a strip gate layout. Transmission line

method (TLM) test structures were also fabricated to monitor contact resistance and sheet resistance of the implanted regions. Circular MOS capacitors with a diameter of 450 μm were designed in front-to-front configuration for MOS C-V measurements.

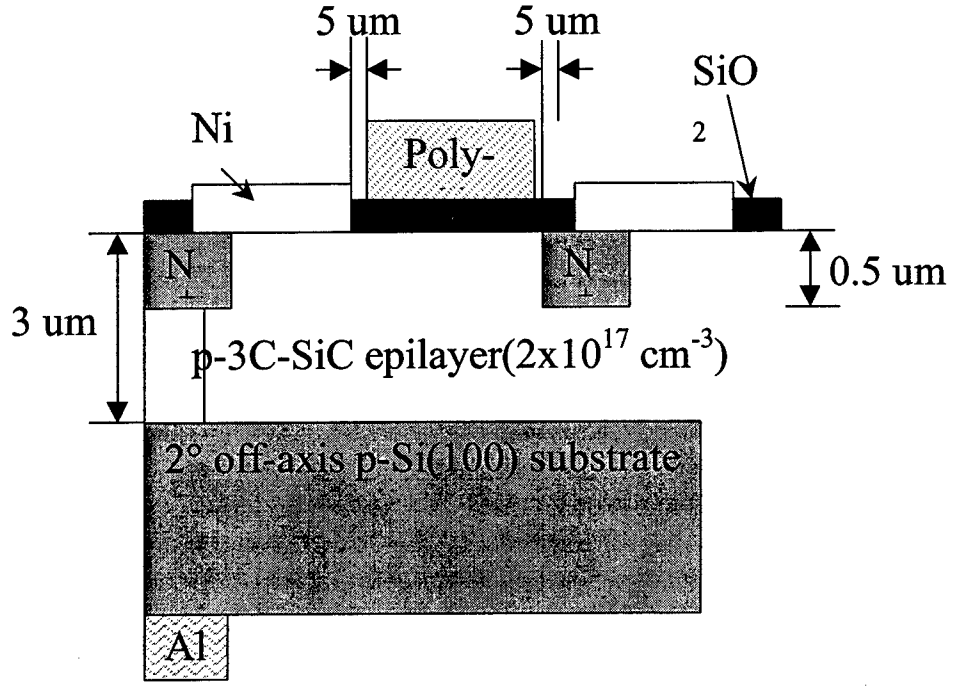


Figure 1: The schematic cross section of a 3C-SiC MOSFET

III. Results and discussion

As-deposited Ni contacts on the implanted SiC layer exhibit an ohmic characteristic with contact resistivity of 4.2 x 10^{-3} ohm-cm^2 measured from TLM structures. The sheet resistance of the implanted regions is about 70 Ω per square, which is nearly equivalent to previously reported data [7].

The drain characteristics of MOSFETs were measured by a HP4156 semiconductor parameter analyzer. Figure 2 shows the drain current (I_D) versus drain voltage (V_{ds}) curves, with gate voltage (V_{gs}) from 0 to 20 V in steps of 2 V, for a device with a gate length of 3 μm. Current saturation is observed for positive gate biases while the device can be properly turned off at zero gate bias.

The subthreshold characteristics were examined by measuring drain current (I_D) versus gate voltage (V_{gs}) at a fixed drain voltage (V_{ds}). Figure 3 shows I_{ds} versus V_{gs} curves at three different V_{ds} bias of 0.1, 5, 10 V, respectively, for a device with a gate length of 5 μm. At

V_{ds} =0.1 V, the device has a small leakage current and the subthreshold slope is about 391 mV/decade. At higher V_{ds}, the leakage current is increased significantly. Defects in 3C-SiC epilayer are responsible for the leakage current and further improvement in crystal quality are needed to alleviate this problem. From the linear plot of I_D versus V_{gs}, the threshold voltage of this device is 1.6 V.

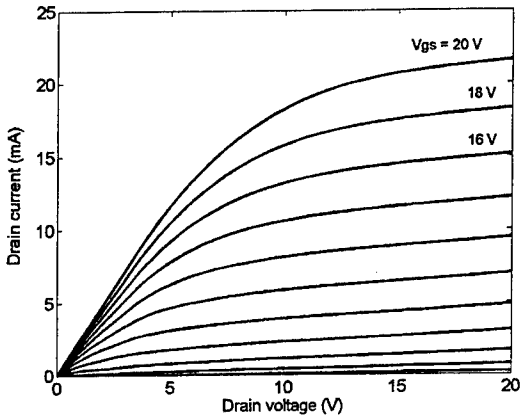


Figure 2: Drain characteristics of a 3C-SiC MOSFET with a gate length of 3 μm (V_{GS} varied from 0 to 20 V in steps of 2V)

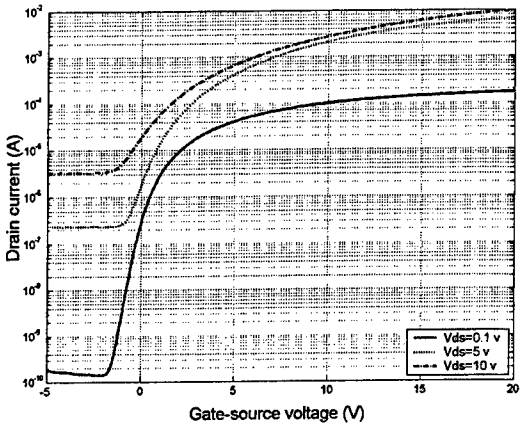


Figure 3: Subthreshold characteristics of a 3C-SiC MOSFET with a gate length of 5 μm (V_{DS} values of 0.1 V, 5 V, and 10 V).

The channel mobility was estimated by differentiating I_D with regard to V_{gs} in the linear region (V_{ds} = 0.1 V) using equation (1).

$$\mu = \frac{L}{WC_{ox}V_{ds}} \frac{\partial I_d}{\partial V_{gs}} \qquad (1)$$

where L and W are gate length and width, respectively, C_{ox} is the gate oxide capacitance for unit area. Figure 4 shows the dependence of channel mobility on gate voltage for a device with a gate length of 140 μm. A peak mobility of 170 cm^2/Vs was observed at a gate voltage of about 12 V, while the channel mobility gradually decreased at a higher gate voltage.

MOS capacitors were measured using a HP4284 LCR meter. Figure 5 shows a capacitance-voltage curve of a 3C-SiC MOS structure at 10 KHz taken in the dark. It is interesting to note that inversion was observed even without illumination and the C-V curve exhibited a peculiar "hook and ledge" characteristics similar to previously reported 6H-SiC results [8]. To understand this strange C-V curve, both fixed charges and interface traps should be taken into account together with the particular configuration of the MOS capacitor structures. The measured circular MOS capacitor is surrounded by a large area capacitor. From the C-V curve in figure 5, we can see a large negative shift in the flat band voltage (close to –20 V). This suggests a large number of positive fixed charges in the oxide.

Because of these fixed charges, the 3C-SiC surface underneath the large area capacitor could be inverted into n-type, serving as an electron supply for the small area capacitor. When the gate bias on the measured capacitor was swept from –20 V (point A) to 0 V (point B), this MOS capacitor was pushed into deep depletion because electrons supplied from large area MOS capacitor were trapped by interface traps located at the gap between the two capacitors. During this process, the interface traps of the small capacitor were empty. Once the interface traps between the gap were completely filled, electrons were able to begin filling the interface traps underneath the small capacitor and bring the MOS capacitor into inversion (point D). Inversion under the small capacitor always occurs at zero volt, because this is the point where the voltage polarity between the small and large capacitors reverses. When the gate bias was swept back from 10V to –20V, the MOS capacitor went from inversion into accumulation. However, the interface traps of the MOS capacitor were filled during this reverse sweep, which caused a parallel shift of C-V curves with respect to the forward sweep curve at the region from 0 V to -5 V. The voltage shift ΔV_g between forward and reverse C-V curves can be used to estimate the interface trap density by equation (2)

$$N_{IT} = \frac{C_{ox}}{q} \times \Delta V_g \qquad (2)$$

Where N_{IT} is the total interface trap density across the bandgap and Cox is the oxide capacitance for unit area. According to this calculation, the total interface trap density across 3C-SiC bandgap is about 1.2×10^{12} cm^{-2}.

Gate oxide leakage current and breakdown field were also characterized by MOS structures and a typical current-voltage curve is shown in Figure 6. A very low leakage current is observed at electric fields below 3 MV/cm, and breakdown occurs at an electric field of 3.5 MV/cm. This breakdown field is lower than that of the 4H or 6H-SiC oxide (~10 MV/cm) probably due to higher defect density in 3C-SiC. However, this value is higher than the previously reported value of 2.5 MV/cm [9].

IV. Conclusions

Inversion-mode, n-channel 3C-SiC MOSFETs have been fabricated on 3C-SiC epilayer on silicon substrate. These devices exhibit excellent transistor characteristics and a channel mobility of 170 cm^2/Vs. Capacitance-voltage characteristics of 3C-SiC MOS structures were measured and the interface trap density was estimated to be 1.2×10^{12} cm^{-2}. The gate oxide breakdown field is 3.5 MV/cm.

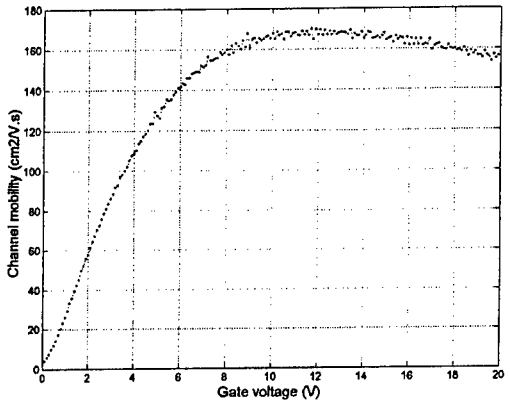


Figure 4: Dependence of channel mobility on gate voltage for a device with a gate length of 140 μm

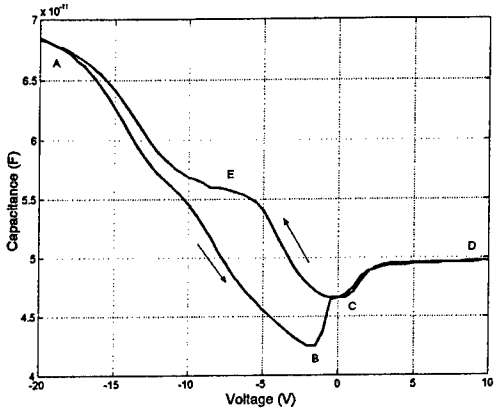


Figure 5: Capacitance-Voltage curve of a p-3C-SiC MOS capacitor with a diameter of 450 μm

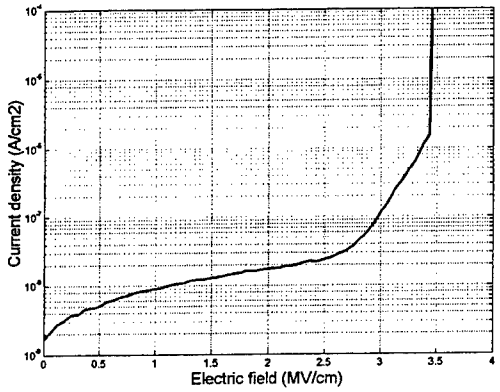


Figure 6: The leakage current and breakdown Field of the gate oxide

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Acknowledgements

This work is supported by a grant from Agere Systems, Inc. The 3C-SiC epilayer was grown at LETI, Grenoble, France, and polished by NovaSiC Inc., Moûtiers, France.

Advances in diamond surface channel FET technology with focus on large signal properties

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Abstract

Field effect transistors based on a hydrogen induced p-type surface channel (surface channel FETs) have shown steady progress in the past. Devices with sub-μm gatelength have been fabricated and cut-off frequencies up to the mm-wave range could be extracted. However, large signal and power performance could only be reported recently. This is due to severe stability and degradation problems. These phenomena are largely related to the highly polar H-terminated diamond surface, although details are still in discussion. This contribution describes these instabilities and the recent progress obtained. To some extent this may also shine some light onto the nature of instabilities observed in GaN based devices.

1. Introduction

The hydrogen terminated diamond surface induces a p-type channel of high carrier density (with an $N_{s,p}$ in the range of 10^{13} cm^{-2}) in close proximity to the surface [1]. This channel has been analyzed in detail down to low temperatures and identified as hole accumulation layer and 2DHG with activation energy below 23 meV [2]. The nature of the related acceptor is still in discussion and several models have been put forward either proposing acceptor surface states or doping transfer from adsorbates [3, 4]. The surface itself is highly polar due to the strong dipole moment of the surfacial H-C bond (fig. 1) and un-pinned in respect to the Schottky barrier of metal contacts [5]. Thus, ohmic and Schottky contact behavior can be realized using metals of different work function. This configuration has been used for the fabrication of Schottky-gate FETs [6, 7] and metal-insulator-gate FETs with various insulators like SiO_x, CaF_2 and BaF_2 [8-12].

On the other hand, terminating the diamond surface by oxygen, results in a highly insulating surface due to a surface potential pinning at 1.7 eV above the valence band [13]. This property has been used to obtain localized active device areas (by employing an oxygen plasma treatment).

The characteristics of the Schottky-gate FETs can well be fitted to HFET or MOSFET models, based on a gate barrier separation layer of 5 to 10 nm [14-17]. This leads to the hypothesis of a hydrogen induced sub-surface channel, a surface barrier layer and a high surface state density acting as surface acceptor (see fig. 2). The surface hydrogen is positively charged, with most of its electronic charge being transferred to the carbon atom below. This will attract negative charges to the surface, change the overall vertical charge balance and influence the 2DHG channel density.

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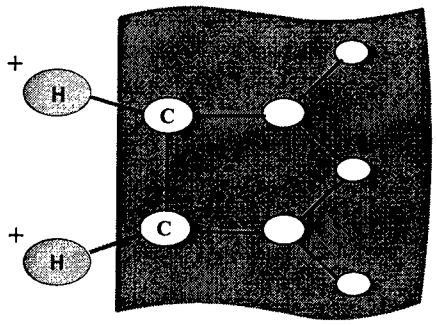


Fig. 1. Surface H^+C^- dipole on (100) diamond surface.

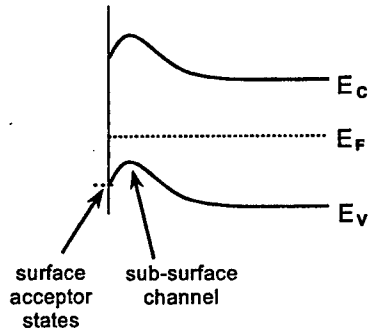


Fig. 2. Proposed energy band diagram of H-terminated diamond surface.

Sub-μm technologies have been developed for both, Schottky-gate FETs and MISFETs with self-aligned T-gates. The Schottky-gate FET devices were unpassivated, MISFET devices used CaF_2 as gate dielectric and an overlapping gate configuration. These technologies were applied to single crystal synthetic HTHP substrates of chip size approx. 4 mm x 4 mm. Equivalent circuit models have been developed and cut-off frequencies in the GHz-range extracted [16, 18, 19]. The high-speed small signal performance could be scaled down to 0.2 μm gatelength (see fig. 3) [18]. However, attempts to measure the large signal properties have failed largely. The devices degraded during the measurement at high current and bias levels. Only one attempt of operation in class B has been published [16].

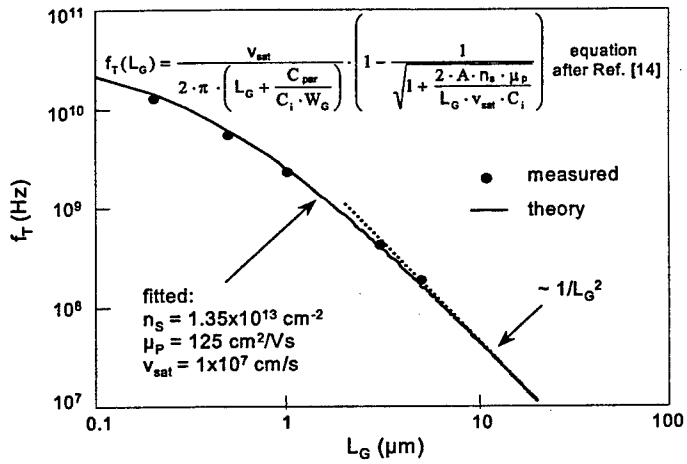


Fig. 3. Measured and calculated f_T dependence on L_G, after Ref. [12].

At the same time, it was found that the hydrogen terminated diamond surface is pH-sensitive in the liquid environment [20], where the pH-value defines the electrochemical potential of the solution. This again was expected since the surface is un-pinned. Thus, it seemed not unexpected that the surface of planar FET devices was unstable. Nevertheless, a number of investigations published in the literature, claimed surface conditions insensitive to pH-values or sensitive to only few ionic species [21]. It seemed therefore, that it may be possible to

in-situ passivate the surface during device processing. Such a treatment was found in connection with the newly developed self-aligned gate fabrication process described below involving an Au-etchback by a KI/I_2 solution.

2. Experimental

The devices were fabricated on nominally undoped homoepitaxial films on single crystals. The homoepitaxial layer had a thickness of 100 nm, and was grown in microwave plasma CVD reactor in a H_2 atmosphere containing 1.5% of CH_4 at 650 °C and pressure of 15 Torr. Subsequently, the layer was treated in hydrogen plasma and cooled down to R.T. in hydrogen atmosphere to obtain the hydrogen terminated diamond surface. Device isolation was obtained by using low energy oxygen plasma. Thus, the conducting active device areas were as-grown hydrogen terminated and the surrounding passive areas were isolating by oxygen termination.

Due to the un-pinned nature of the hydrogen-terminated diamond surface, the barrier height of metal to diamond contacts depends strongly on the metal work function as mentioned above. E-beam evaporated Au has been used for ohmic contacts and Al for Schottky contacts, respectively. The contact fabrication sequence is illustrated in fig. 4. Firstly, the Au-layer covering the entire active area is patterned by etching. Next, a three-layer e-beam lithography process has been used for the definition of the sub-μm gate patterns. The footprint of the gate has then been opened by etching back the Au layer in a KI/I_2 solution and was therefore self-aligned in respect to the Au contacts. Subsequently the gate metal (Al) has been deposited and patterned by lift-off. FETs have been fabricated both on HTHP type Ib substrates and on a diamond quasi-substrate (a single crystal substrate detached from an $Ir/SrTiO_3$ substrate [22]).

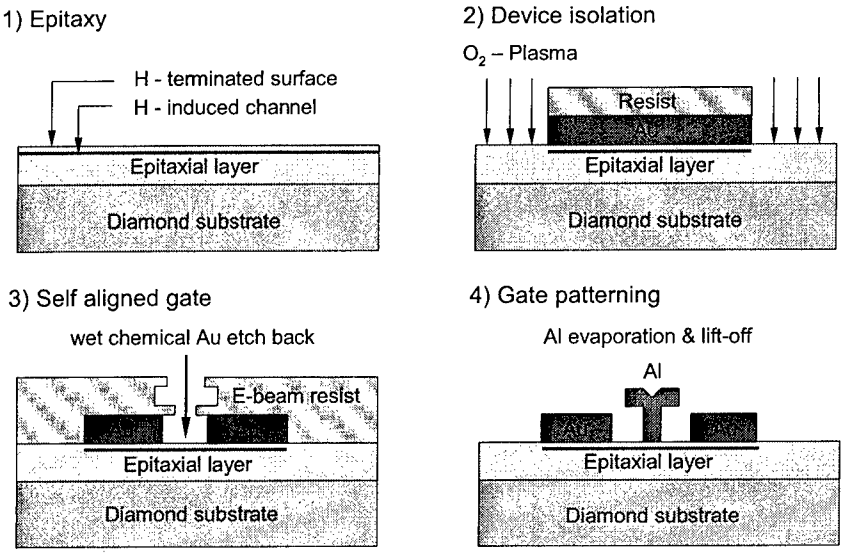


Fig. 4. Processing sequence of self aligned gate of diamond Schottky-gate FET technology.

To test the free surface in the liquid environment, diamond surface channel structures were prepared as described in [20] with contacts and leads entirely isolated and protected by epoxy. After various surface treatments these structures were tested in 0.1 M H_2SO_4 acidic and in 0.1 M KOH basic water solutions.

3. Switching and large signal characteristics

In our previous experiments the hydrogen terminated diamond surface has been treated with resist and developer to pattern the contacts. This was generally followed by a rinse in acetone and isopropanol, avoiding oxidizing agents. The characteristics of this surface may be summarized as shown in the following figs. 5 and 6.

Fig. 5 shows the switching response in atmosphere of an ungated channel between source and drain contacts (source to drain spacing is 5 μm). When switching from the quiescent bias point V_{DS} = 0 V to a drain-source bias of 40 V and 80 V, respectively, the current decreases with time. However, it recovers after switching the bias off, as also shown in fig. 5, where the measured points are obtained by short bias pulsing. The bias pulse must be short enough (~ 1 s) to not disturb the recovery. It seems that the channel becomes slowly depleted by surface charges changing the surface potential or acting as virtual gate. The effect is reversible with bias and thus an electronic surface instability.

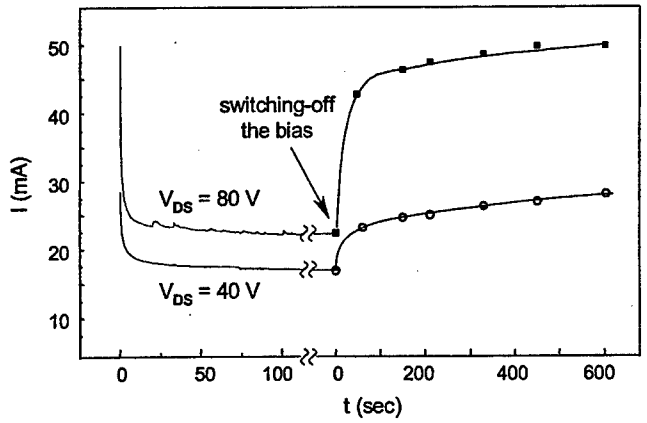


Fig. 5. Previously observed current instability of an ungated channel when switching on the bias between contacts and subsequent current recovery after switching-off the bias (the measured points are obtained after short ~ 1 s bias pulse not disturbing the recovery).

On the other hand, when trying to remeasure the FET output characteristics up to high forward gate bias, the output current is degraded with each trace (see fig. 6) and not recovered. Thus, this effect is not reversible and points towards a permanent degradation of the surface charge state. S-parameter measurements characterizing the high-speed performance, were therefore mostly taken in the lower part of the output characteristics using virgin samples [16].

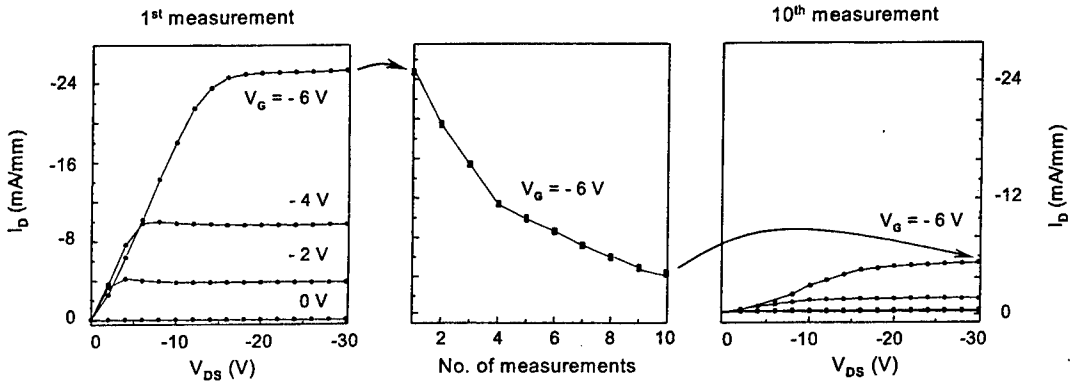


Fig. 6. Previously observed irreversible degradation of MESFET output characteristic after 10 measurements, after Ref. [16].

The characteristics of ungated samples in the liquid environment are shown in fig. 7. Here the sample has been dipped into 0.1 M H_2SO_4 acidic and in 0.1 M KOH basic water solutions with pH values approx. 1 and 11, respectively. The experiment started with pH = 1. After each dip the sample was rinsed in deionized water and then brought into contact with the next solution. The pH sensitivity of the device in the first sequence shows that indeed the surface appears unpinned. The highest current level and thus smallest channel depletion is obtained for pH = 1, the channel being successively depleted with increasing pH. Repeating the sequence reveals that the initial open channel condition cannot be reproduced. In addition, after each sequence a further reduction in open channel current is observed. Thus this effect is not reversible and finally the channel appears depleted at all time. This points towards the build-up of an in-situ passivation layer charging up the surface and depleting the channel. The driving force can be expected to be the highly polar surface. It seems that this passivation layer due to adsorption cannot be removed anymore or may even react with the surface resulting in a change of its termination.

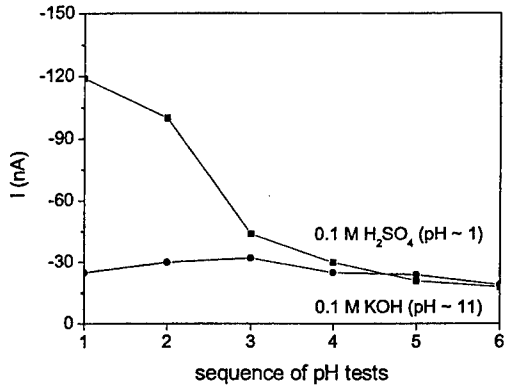


Fig. 7. Degradation of an ungated channel in aqueous solution of different pH values of as-fabricated samples.

In the new experiment the surface was treated with a KI/I_2 Au-etch solution, then rinsed in deionized water and dried before deposition of the Al-gate (in case of the FET) or before immersing into the liquid (in case of the ungated structures). Thus, in the case of the FET the surface treatment was effective to the open surface as well as to the Schottky gate interface.

At first, the response of ungated structures to the liquid environment shall be discussed. The same sequences were performed as described above, in fact on the same device after KI/I_2 treatment. The result is shown in fig. 8. The starting current level is about 5 times higher than before. This means that this time the current more than recovered after the first series of sequences, which showed degradation. This means also that indeed an adsorbed passivation layer had caused the degradation in the first case and not a non-reversible chemical reaction. Furthermore, in the first case the surface conduction (for an open channel) had already been degraded and depleted the channel partially by the previous resist deposition and development routine. Now, even after 6 sequences going through the full cycle of pH-treatments, still 90% of the current level is seen. The surface has been essentially stabilized without loosing its property of being un-pinned. It seems important to identify the chemical mechanisms behind. This is still under investigation and will however need to involve a full electrochemical analysis.

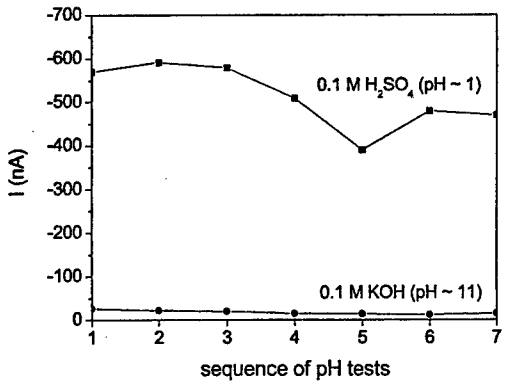


Fig. 8. An ungated channel in aqueous solution of different pH values after KI/I_2 treatment.

In respect to the Schottky-gate FETs, repeatedly large signal measurements were performed using a parameter tester and a power bench at 1 GHz. In fig. 9 is shown the IV-output characteristics of a virgin device with 0.8 μm gatelength. Stressing the device for 10 minutes in the open channel condition (V_{GS} = - 3.5 V and V_{DS} = - 20 V) shows an increase of the maximum current by approx. 20% (see fig. 10). This is mainly related to a stabilization of the Schottky barrier characteristics, resulting in a decrease of (forward) pinch-off voltage of this enhancement mode device. No external current limiter is visible stemming from the open channel areas between the contacts. Power measurements in class A were first performed with a 50 Ω load scanning the drain bias up to - 40 V. The level of power saturation could be obtained for each scan and thus the maximum peak in RF-current. Adding up the different scans will then result in an RF current envelope of the output characteristics. As expected, it surpasses the DC output current levels obtained from the curve tracer measurement. Thus no

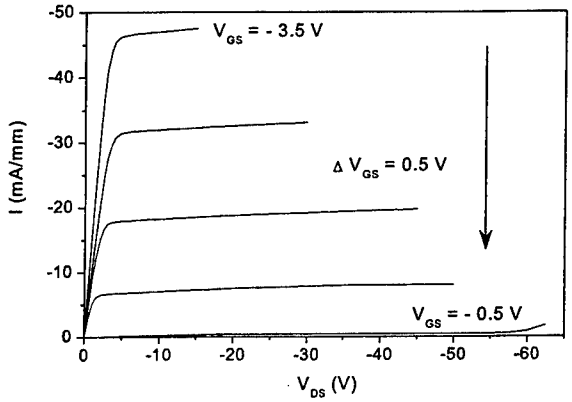


Fig. 9. I-V output characteristic of surface channel FET with 0.8 μm gate length. This graph is constructed of 2 measurements. The breakdown curve is added.

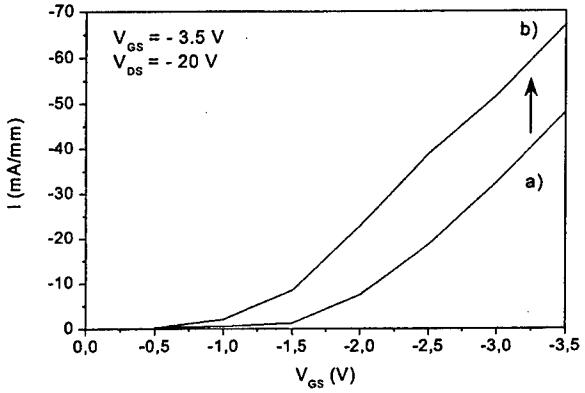


Fig. 10. Transfer characteristics
a) measured on a virgin device b) after bias stress at V_{GS} = - 3.5 V and V_{DS} = - 20 V for 10 min.

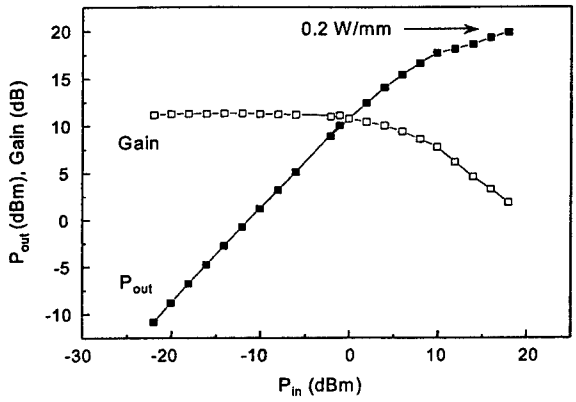


Fig. 11. Large-signal measurements at 1GHz for class-A bias point V_{DS} = - 40 V, V_{GS} = - 2.2 V, after Ref. [23].

current clipping or RF current degradation is observed. Using the optimum available load on the tuner system (approx. 400 Ω) has then resulted in the first diamond FET power measurement of 0.2 W/mm at V_{DS} = - 40 V (see fig. 11) with an associated linear gain of 12 dB as recently reported at the 60th DRC [23].

4. Conclusions

Although the diamond crystal does not contain a spontaneous polarization, the surface becomes highly polar upon termination. After growth in a hydrogen rich environment, this is the H-termination with a highly positively charged surface. This surface is un-pinned, indicating a high bondstrength of this atomic surface layer and no (noticeable) surface states within the bandgap. This is very similar to other polar materials like hexagonal GaN. Therefore, it is not surprising that surface adsorbates can charge the surface, resulting in effects similar to the virtual gate effect in GaN based FET structures. Thus, the H-terminated diamond surface will behave electronically highly unstable, which will in turn affect the stability of FET channel sheet charge densities. In the case of diamond the surface conditions can change and deteriorate irreversibly, causing permanent current degradation. Thus, in-situ passivation by adsorbates plays an important role.

These instability and degradation phenomena have been severe enough to prevent large signal operation. However our recent results indicate, that the instability and degradation mechanisms can be influenced by specific surface treatments. The present understanding is, that the surface dipole layer is stabilized by an in-situ passivation of specific ionic adsorbates. However, this picture is still highly speculative. Nevertheless the stabilization of the FET large signal characteristics have by now been observed in devices fabricated with various gatelengths and on various substrates, namely a diamond quasi-substrate and also on HTHP synthetic crystals with homoepitaxial active layers.

Eventually it is hoped that a refined surface treatment may allow to further improve of the power handling capability of diamond surface channel FETs, which is still approx. 2 orders of magnitude below expectations [24].

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Simulations of High Linearity and High Efficiency of Class B Power Amplifiers in GaN HEMT Technology

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Abstract

We describe the design and simulation of highly linear and highly efficient common source Class B power amplifiers. Efficient broadband Class B Push-Pull amplifiers are not feasible at microwave frequencies as baluns with desired broadband even-mode impedance are unavailable. We find, however, that single-ended Class B amplifier with bandpass filtering has equivalent efficiency and linearity. Simulations of Class B designs predict a power added efficiency (PAE) of 48% with 40 dBc of third order intermodulation product (IMD3) performance when biased close to the pinch-off voltage.

I. Introduction

Simultaneously achieving high efficiency and low distortion is a major challenge in microwave power amplifier design. Class A amplifiers exhibit low distortion but exhibit power added efficiency well below 50%[4]. Improved efficiency is obtained with switched mode power amplifiers [5]. These, unfortunately, exhibit high intermodulation distortion in multi-tone applications. Push-Pull Class B amplifiers offer the potential for improved efficiency, at a theoretical limit of 78.6%[2], combined with distortion as low as Class A.

II. Single-ended Class B Power Amplifier

Efficient broadband Class B amplification is unfortunately not feasible at microwave frequencies due to the lack of available baluns with the required zero ohm *even-mode* impedance. With non-zero even-mode impedance, the transistor drain voltage waveform contains 2^{nd} harmonic Fourier component, and power is dissipated in the 2^{nd} harmonic, degrading efficiency. Additionally, microwave baluns are physically large (of the order $\lambda/2$), which results both in large excess consumed expensive IC die area and in large excess line losses with resulting degradation in efficiency.

We must emphasize that Push-Pull operation, through its symmetry, suppresses only even-order (2^{nd} harmonic) distortion [1]. Odd-order component in the circuit transfer function, and the resulting two-tone 3^{rd} order intermodulation distortion are not suppressed.

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Third-order distortion characteristics of Class B Push-Pull circuits, therefore, do not differ from that of a single-ended Class B amplifier. Consequently, for power amplifier applications requiring less than 2:1 frequency coverage, Push-Pull operation is entirely unnecessary. Instead, 2nd harmonic Fourier components of the transistor drain current waveform can be supplied (provided with the required zero ohm impedance) through use of an output bandpass filter, centered at the signal fundamental, and a single transistor stage can be employed. Third-order intermodulation characteristics are identical for both Push-Pull and the single-ended configurations. Therefore, given an operating bandwidth requirement of less than an octave, a single-ended Class B amplifier can provide both high linearity and efficiency approaching 78.6%.

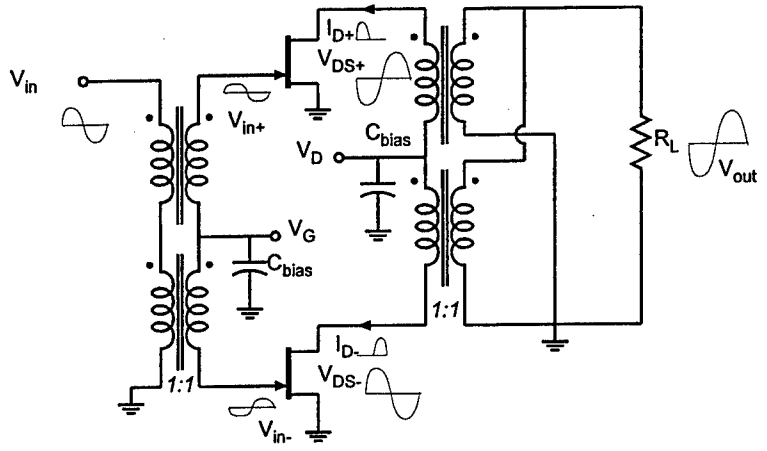


Fig. 1. Circuit Schematic of Push-Pull Class B

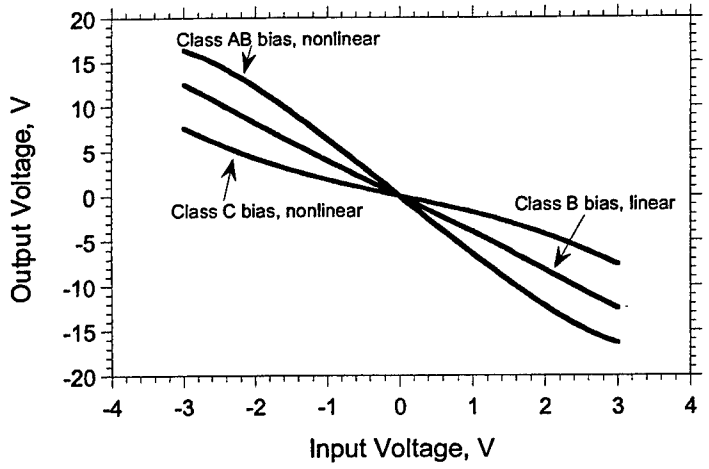


Fig. 2. Transfer function of Common Source Amplifier as a function of bias

Two-tone third order distortion characteristics depend critically upon the Class B bias point, whether for single-ended or for the equivalent Push-Pull configuration. Bias

design is, however, most easily discussed in the framework of the Push-Pull stage (Fig.1), with drain current $I_d(V_{in})$, the Push-Pull output current is $I_o=I_d(V_{in})-I_d(-V_{in})$. Given the threshold characteristic typical in HEMT (Fig. 4), third-order distortion is strongly reduced for Class B biased precisely at the HEMT threshold voltage (Fig. 3), and degrades as the bias is set either above (Class AB) or below (Class C) the threshold voltage. Transfer characteristics with Curtice GaN HEMT model are shown in Fig. 2 for Classes AB, B and C.

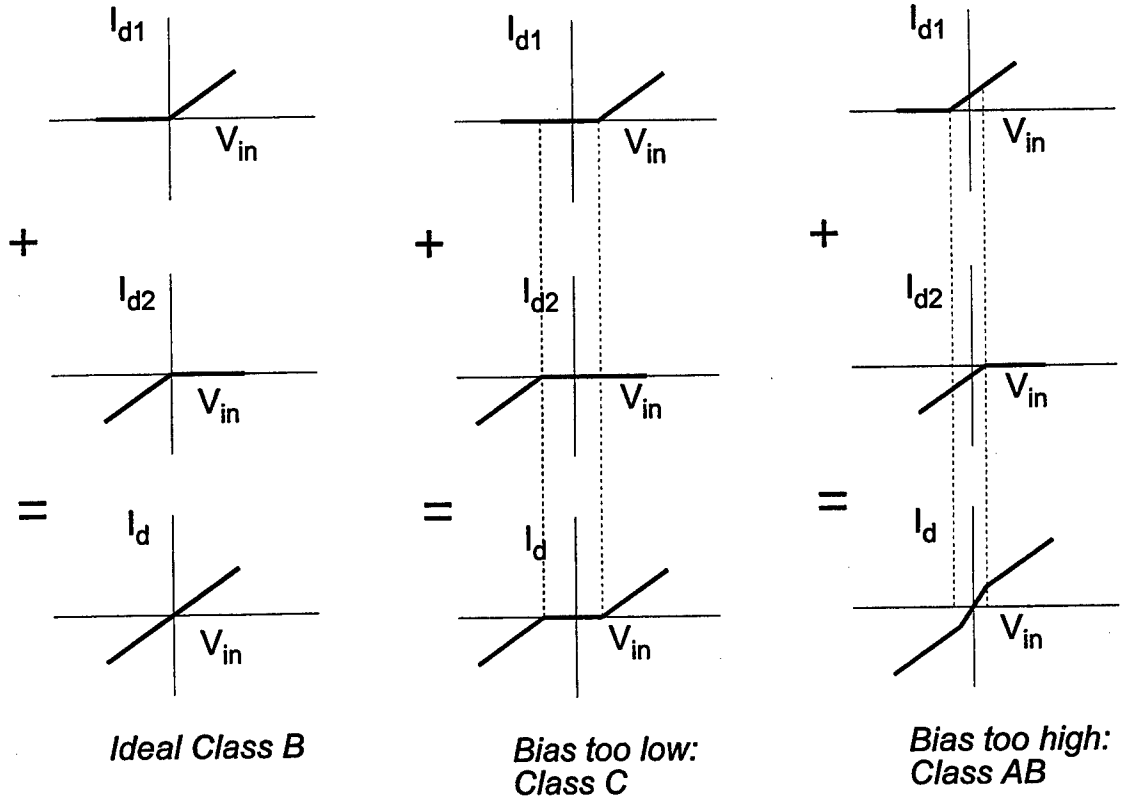


Fig. 3. Bias design for good linearity performance

III. Design and Simulations

Designs have been developed for UCSB's GaN HEMT MIMIC process. Designs were developed using the model of a 0.2μm L_g device, resulting in 50 GHz f_t and 100 GHz f_{max} [3]. The modeled devices have 50V breakdown and I_{dss} is 650mA/mm. These device parameters are representative of better GaN HEMTs fabricated at UCSB.

The circuit is simulated using Agilent ADS and the Curtice HEMT model. The measured HEMT drain current-gate bias characteristics (Fig. 4) and input capacitance characteristics (Fig. 5) are precisely modeled, as those parameters are crucial for linearity simulations. In particular, IMD3 is generated if the input capacitance C_{gs} is not purely anti-

symmetric about the gate bias voltage. The GaN HEMT on SiC has very nearly linear current-voltage characteristic if biased at the pinch-off voltage, a bias condition which is also desirable for high efficiency.

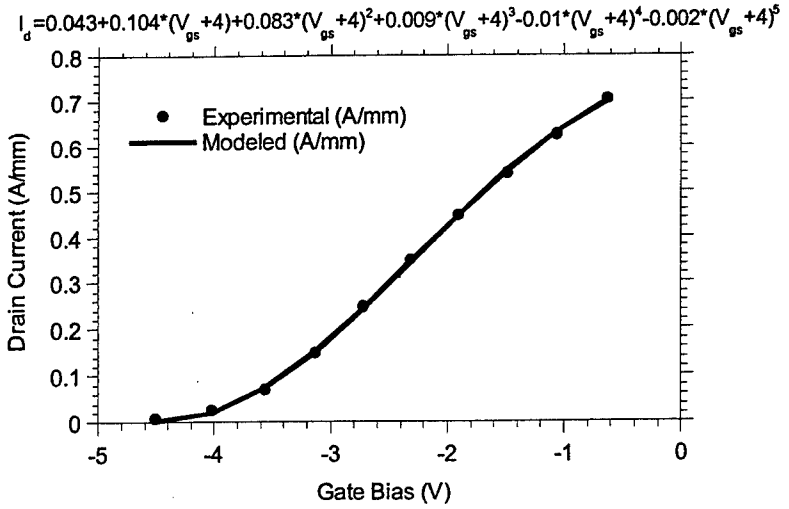


Fig 4. I_d-V_{gs} characteristic of GaN HEMT on SiC

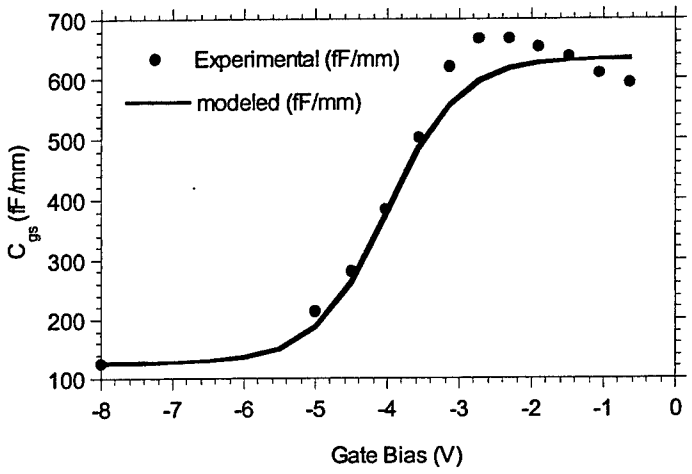


Fig. 5. Input Capacitance characteristic of GaN HEMT

Circuit simulations (Fig. 6, Fig. 7, Fig. 8, Fig. 9, Fig. 10) predict 36dBm output power with a saturated efficiency of 48 percent. Two-tone circuit simulations predict IMD3 levels of -40dBc when the output power is 3dB below the 1-dB gain compression point. The zero-input-signal dissipation is low, which will result in high PAE, when a broadband amplifier is constructed by frequency-multiplexing an array of class-B amplifiers. A systematic study of the influence of bias point on PAE and linearity was performed (Fig.

10). The optimum operating point is found to be very close to pinch off confirming the theoretical predictions. The cascode version of this circuit is being fabricated in GaN HEMT technology at UCSB.

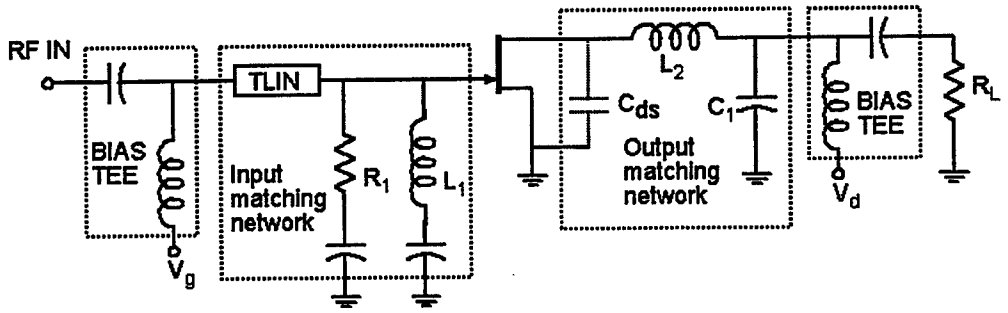


Fig. 6. Circuit Schematic for Single-ended Class B

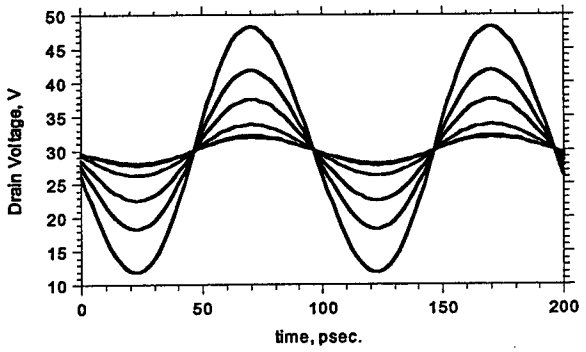


Fig. 7. Drain voltage waveform

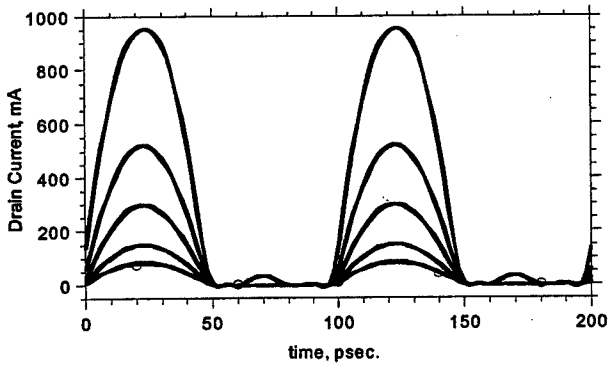


Fig. 8. Drain current waveform

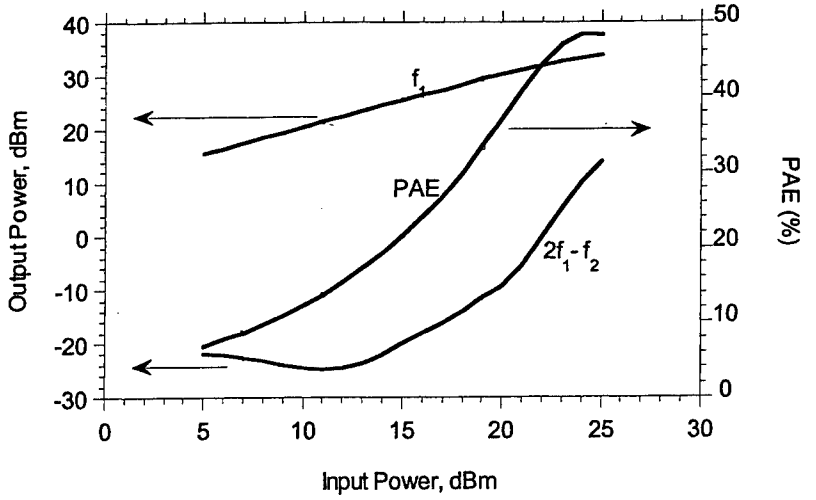


Fig. 9. PAE and IMD3 performance of Class B power amplifier

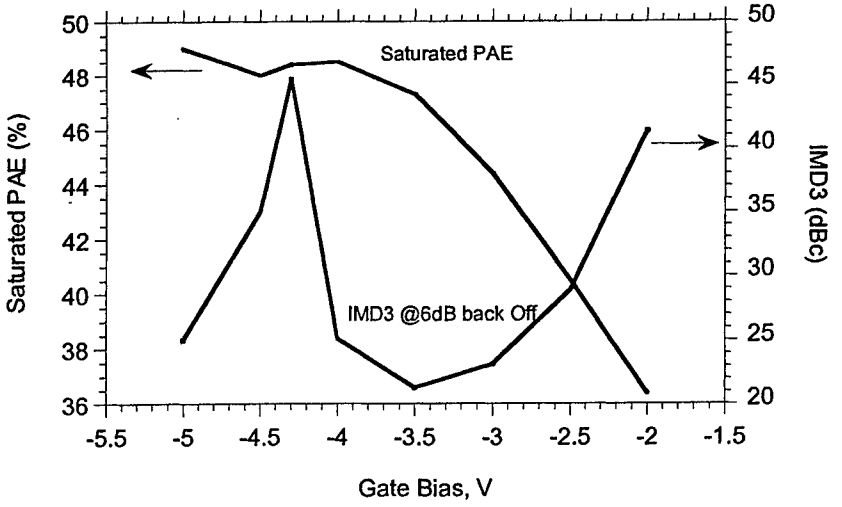


Fig. 10. Bias dependence of PAE and IMD3

IV. Conclusions

The Push-Pull configuration is unnecessary and can be replaced by a single ended configuration with adequate filtering. The common source Class B can be linear if the transfer characteristics are linear. This configuration has shown ~40dBc of linearity at 10GHz with approximately 48% PAE.

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Acknowledgment

This work is supported by the Office of Naval Research (ONR) under ONR Class D/E (N00014-00-1-0653). The authors thank Dr. W. Curtice (Curtice Counseling) for providing his HEMT model.

Thermal and Trapping Effects in GaN-Based MESFETs

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Abstract

RF power performances of GaN-MESFETs are reported using a physics-based model that incorporates dispersion in the output resistance and transconductance due to traps and thermal effects. Calculated *I-V* characteristics are in excellent agreement with the measured results. Taking thermal effects into account the maximum output power of a 0.3μm × 100μm GaN MESFET is 22dBm at a power gain of 4.2dB at 4GHz. The corresponding quantities are 27dBm and 6.4dB, respectively if a constant channel temperature of 300K is assumed. At elevated temperatures compression in output power, gain and PAE is less in MESFETs with longer gate lengths.

Introduction

Currently, power transistors used in applications involving phased array radar and wireless base stations are Si-LDMOS which operates around 1W/mm power density range. Recently, GaN-based FETs have successfully demonstrated their usefulness in circuits operating at high temperatures, high power and high frequencies [1-4]. GaN with bandgap of 3.4eV, saturation velocity of 3×10^7 cm/s and low parasitics is suitable for high power and high frequency applications compared to Si-LDMOS and SiC-based transistors. Moreover, GaN grown on SiC offers a thermal conductivity of 4.5 W/cm/K making the system suitable for applications at high temperatures and high power. GaN HEMTs with output power of 11.7 W/mm at 10GHz with 43% power added efficiency [1], f_T = 107 GHz [2] and f_{max} = 155 GHz [3], and operating temperature of 750C [4] have been reported. However, the inability to dissipate the generated heat leads to self-heating effects [5-7]. For a GaN HFET grown on SiC, with gate width of 250μm, Nuttinck *et al.* [5] estimated the maximum temperature to be 96C in the active channel with the device operating under a continuous wave dissipation power density of 5W/mm. Due to thermal effects a 25% reduction in drain current was observed as the drain pulse width increased from 1% to 100% for the same 250μm wide GaN HFET grown on SiC [6]. Using Raman spectroscopy Kuball *et al.* [7] estimated the temperature at the gate-drain opening to be as high as 180C for a 4μm × 200μm GaN HFET grown on Sapphire at drain and gate bias of 20V and 0V, respectively.

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Self-heating effects at large drain bias increase the device lattice temperature and reduce the transport parameters such as mobility and carrier saturation velocity by increasing the carrier-phonon scattering [8,9]. Besides, GaN based devices are plagued by traps that results in performance deteriorating gate- and drain-lag transients and current collapse in the *I-V* characteristics [10, 11]. Trapping effects are dependent upon the applied signal frequency and their effect is more pronounced for frequencies less than the transconductance and output resistance dispersion frequencies [12,13]. The dispersion frequencies are related to the detrapping time constants, which are critically dependent upon the junction temperature. Therefore, an exact simulation of GaN based devices should proceed by determining the appropriate junction temperature to update the transport and detrapping parameters.

In this paper, a physics-based model is reported to determine the power performance of GaN-MESFETs by considering dispersion in the output resistance and transconductance due to traps while accounting for the thermal effects. The present treatment will allow the optimization of GaN-based MESFETs used in high power and high frequency applications.

Analysis

In the present analysis, the intrinsic and the trap related circuit parameters, as shown in Fig. 1, are obtained from a physics based analysis. Temperature and field dependent transport parameters are obtained from an ensemble Monte Carlo simulation [8, 9]. Following the treatment reported by Golio *et al.* [12] the effects of traps are incorporated through the parameters C_{ss}, $g_m^{"}$ and $R_{ds}^{"}$. These parameters are obtained once the underlying physical processes governing trap dynamics are formulated. Intrinsic circuit parameters: C_{gs}, C_{gd}, $g_m^{'}$, R_i and $R_{ds}^{'}$ are obtained from conventional small-signal MESFET analysis in the absence of traps and considering the effects of velocity saturation. The other circuit parameters are obtained from the reported experimental data and are as follows: $R_g = 6\ \Omega$, $L_g = 0.055$ nH, $R_d = 70\ \Omega$, $L_d = 0.307$ nH, $R_s = 90\ \Omega$, $L_s = 0.027$ nH and $C_{ds} = 0.040$ pF [11, 12].

A thermal simulator is incorporated to calculate the operating temperature for a given power level by solving Laplace's equation. The analysis proceeds with the initial guess of junction temperature to estimate mobility, carrier velocity and critical electric field for a given channel electric field to determine the drain current for given drain and gate bias. Estimating the dissipated power which is related to the product of drain voltage and current Laplace's equation is solved to obtain the updated temperature. Transport parameters and critical electric field are updated to determine the drain current and the process continues till a consistent solution in terms of drain current and temperature is obtained. The temperature

dependent transconductance and output resistance dispersion frequencies are obtained once self-consistency is achieved.

At any given frequency the overall intrinsic output conductance, g_{ds}, and transconductance, g_m, are obtained by analyzing the output subcircuit of Fig.1. For large-signal analysis, g_m, g_{ds} and C_{gs} are considered nonlinear functions of v_g while C_{gd} is nonlinear function of v_{dg}. The nonlinear functions are approximated up to second order term, $p = p_0 + p_1 v + p_2 v^2$, where p represents g_m, g_{ds}, C_{gs} or C_{gd} and v represents v_g or v_{dg}.

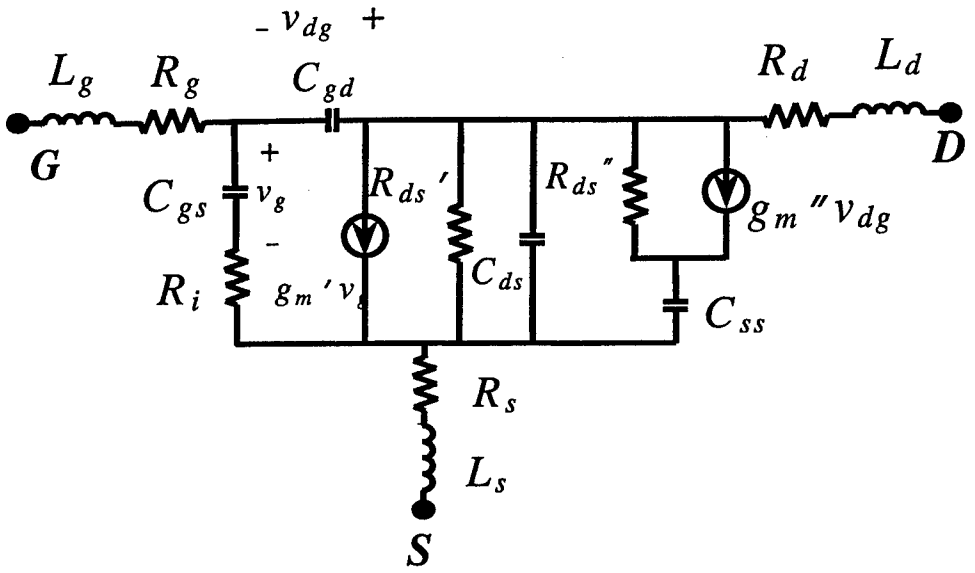


Fig.1. GaN MESFET model.

Volterra series technique is used to compute output power and nonlinearities at RF. For Volterra series analysis, the circuit shown in Fig.1 is terminated in source impedance Z_S and load impedance Z_L across the gate-source and drain-source terminals, respectively. Defining ports 1 through 5 across nonlinear elements C_{gs}, g_m and g_{ds}, C_{gd}, load and source respectively, the elements of 5×5 system matrix Y are expressed as follows:

$$Y_{1,1}(\omega) = 1/R_i + j\omega C_{gs0}\,, \tag{1}$$

$$Y_{1,2}(\omega) = Y_{1,3}(\omega) = Y_{3,1}(\omega) = -1/R_i\,, \tag{2}$$

$$Y_{2,1}(\omega) = -1/R_i + g_{m0}\,, \tag{3}$$

$$Y_{1,4}(\omega) = Y_{4,1}(\omega) = Y_{1,5}(\omega) = Y_{5,1}(\omega) = 0\,, \tag{4}$$

$$Y_{2,2}(\omega) = 1/R_i + \left[\{1/(R_d + j\omega L_d) + 1/(Z_s(\omega) + R_g + j\omega L_g)\}^{-1} + R_s + j\omega L_s\right]^{-1} + j\omega C_{ds} + g_{ds0}\,, \tag{5}$$

$$Y_{4,4}(\omega)=\left[\left\{1/\left(Z_s(\omega)+R_g+j\omega L_g\right)+1/\left(R_s+j\omega L_s\right)\right\}^{-1}+R_d+j\omega L_d\right]^{-1}+1/Z_L(\omega), \tag{6}$$

$$Y_{5,5}(\omega)=\left[\left\{1/\left(R_s+j\omega L_s\right)+1/\left(R_d+j\omega L_d\right)\right\}^{-1} + Z_s(\omega)+R_g+j\omega L_g\right]^{-1}, \tag{7}$$

$$Y_{2,5}(\omega)=Y_{5,2}(\omega)=-Y_{5,5}(\omega) \left[\left(R_d+j\omega L_d\right)/\left(R_s+j\omega L_s+R_d+j\omega L_d\right)\right], \tag{8}$$

$$Y_{2,4}(\omega)=Y_{4,2}(\omega)=\left[1/Z_L(\omega)-Y_{4,4}(\omega)\right] \left[\frac{Z_s(\omega)+R_g+j\omega L_g}{R_s+j\omega L_s+Z_s(\omega)+R_g+j\omega L_g}\right], \tag{9}$$

$$Y_{3,4}(\omega)=Y_{4,3}(\omega)=\left[Y_{4,4}(\omega)-1/Z_L(\omega)\right] \left[\frac{R_s+j\omega L_s}{R_s+j\omega L_s+Z_s(\omega)+R_g+j\omega L_g}\right], \tag{10}$$

$$Y_{2,3}(\omega)=Y_{3,2}(\omega)=1/R_i-Y_{2,5}(\omega), \tag{11}$$

$$Y_{3,3}(\omega)=Y_{5,5}(\omega)+1/R_i+j\omega C_{dg0}, \tag{12}$$

$$Y_{3,5}(\omega)=Y_{5,3}(\omega)=-Y_{5,5}(\omega), \text{ and} \tag{13}$$

$$Y_{5,4}(\omega)=Y_{4,5}(\omega)=-Y_{3,4}(\omega). \tag{14}$$

With an applied signal of amplitude V_{s1} at frequency ω_1, voltages across ports 1 through 4 are determined using [14]:

$$\left[V_p(\omega_1)\right]=-\left[Y_{i=p,\,j=1,\cdots,4}\right]^{-1}\left[Y_{i=p,\,j=5}\right]^{T}\left[V_{5,1,q}=V_{s1}\right] \tag{15}$$

where $p = 1,\ldots,4$. The second-order voltages appear across ports at mixing frequencies, $\omega_{2,k} = \omega_1 + \omega_2$ when two tones are applied with amplitudes V_{s1} and V_{s2} at frequencies ω_1 and ω_2, respectively. Second-order port voltages are calculated by applying nonlinear currents through each nonlinear port. The nonlinear currents are evaluated using first-order port voltages due to individual tones and p_1 coefficients of nonlinear elements [14]. With Y matrix evaluated at mixing frequencies, the second-order port voltages are given by,

$$\left[V_p(\omega_1,\omega_2)\right]=-\left[Y_{i=p,\,j=1,\cdots,4}\right]^{-1}\left[I_{i=p,2,k}\right]^{T},\ p=1,\cdots,4. \tag{16}$$

Similarly, third-order port voltages due to tone amplitudes V_{s1}, V_{s2} and V_{s3} and frequencies ω_1, ω_2 and ω_3 are calculated by applying current sources due to nonlinear

coefficients p_1 and p_2 and first and second-order port voltages. The fundamental component of the output power is given by,

$$P_{out} = 0.5|V_4(\omega_1)/Z_L(\omega_1)|^2 \,\mathrm{Re}[Z_L(\omega_1)]. \tag{17}$$

Results and Discussion

Fig.2 shows calculated DC and pulsed *I-V* characteristics incorporating thermal and trapping effects for a 0.3μm × 100μm GaN MESFET [10]. Experimental results are plotted on the same figure to show good agreement [10]. The MESFET structure was grown on sapphire with a 2000 Å n-GaN active layer with doping concentration of 2.7 x 10^{17} cm^{-3} [10]. In the presence of light, the DC *I-V* measurements do not show any current collapse as the electrons captured by traps located at the channel-buffer interface and the surface (between gate-drain region) have sufficient time to be released. With pulsed input signals electrons captured by the buffer traps form a depletion region in the channel at the channel-buffer interface. Besides, surface traps also capture electrons and form a virtual gate [15] which causes drain current to decrease for a given drain bias. The effect of surface traps is incorporated by considering an additional negative gate potential due to the trapped electrons in the region between gate and drain.

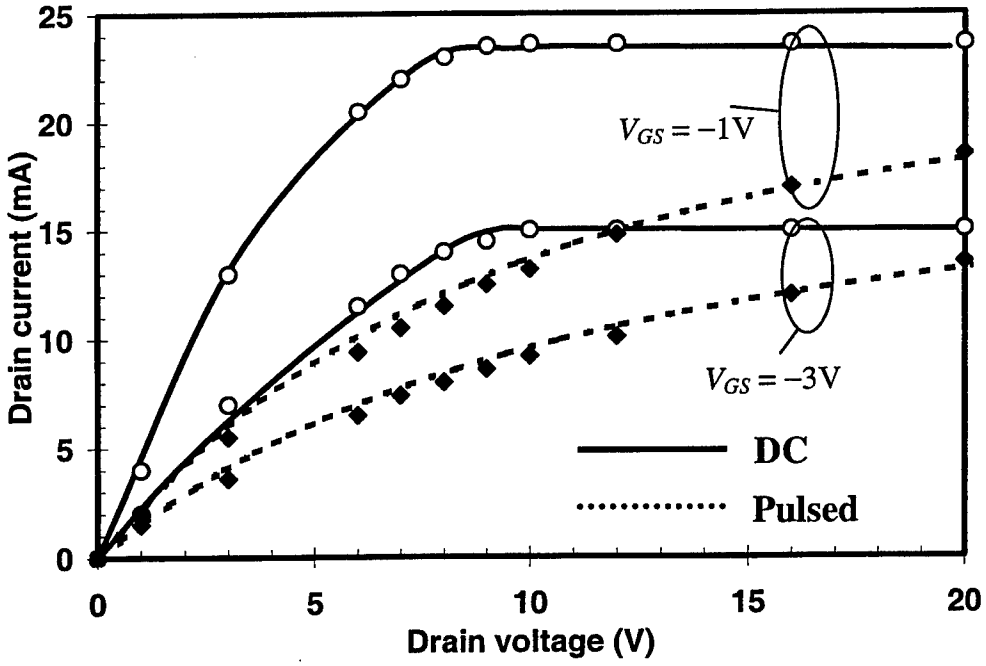


Fig.2. Calculated (solid lines) and measured (symbols) *I-V* characteristics for 0.3μm × 100μm GaN MESFET [10].

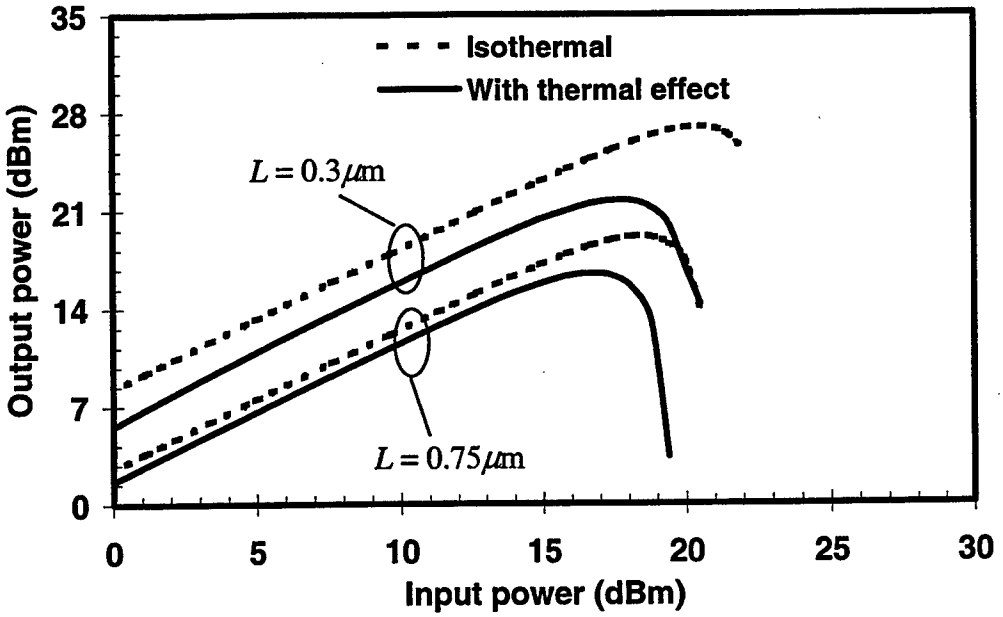


Fig.3. Variation of output power as a function of input power for $L\times100\mu m$ GaN MESFET at 4GHz.

Fig.3 shows the variation of the output power as a function of input power for $0.3\mu m$ and $0.75\mu m$ gate length devices operating at 4GHz. The bias voltages are V_{GS} = -2V and V_{DS} = 30V. Using isothermal (300K) calculations maximum output powers of 27dBm and 19dBm are obtained with $0.3\mu m$ and $0.75\mu m$ gate length devices, respectively. For the same gate lengths by taking into account thermal effects the maximum output powers decrease to 22dBm and 17dBm, respectively. Higher output power is obtained for a given input power in shorter gate length devices due to higher transconductance resulting from higher differential mobility. The temperature and electric field dependent differential mobility, defined as the ratio of velocity to electric field, for the $0.3\mu m$ gate length device is given by, $\mu_n(E,T) = (1705.2 - 30.91E + 0.1564E^2) + (-3.35 + 0.075E - 4\times10^{-4}E^2)T + (0.0015 - 4\times10^{-5}E + 2\times10^{-7}E^2)T^2$, where temperature T is in K and channel electric field E is in kV/cm. Mobility expression for the $0.75\mu m$ gate length device is, $\mu_n(E,T) = (1914.4 - 36.18E + 0.1855E^2) + (-4.30 + 0.09E - 0.00053E^2)T + (0.0032 - 8\times10^{-5}E + 5\times10^{-7}E^2)T^2$. The determination of the temperature, electric field and size dependence of mobility proceeds by carrying out an ensemble Monte Carlo simulation by taking into account scatterings due to polar optical phonon, acoustic phonon, equivalent and non-equivalent intervalley scattering, impact ionization, ionized impurity, alloy, interface and self-scattering [8, 9]. For a given power

dissipation, shorter gate length devices operate at higher temperatures and their mobility and saturation velocity are greatly reduced from their corresponding room temperature values. Though, at a given temperature and electric field shorter gate length devices have a higher differential mobility as compared to devices with longer gate lengths. The higher temperature in shorter structures is due to higher dissipation power density. As a result, output power decreases significantly due to device heating in shorter structures.

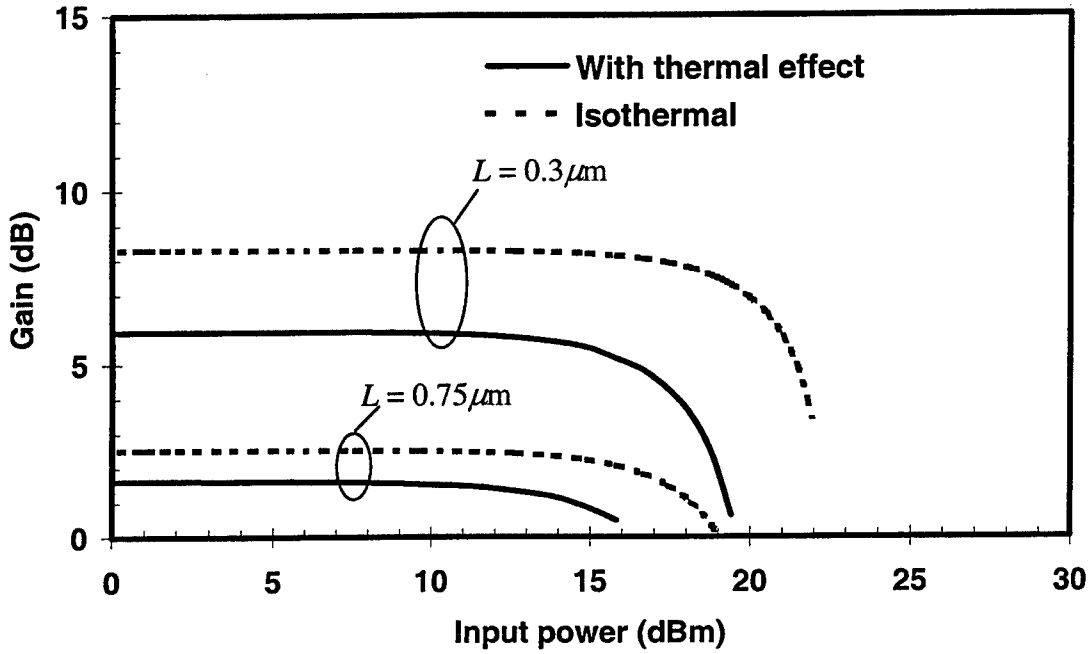


Fig.4. Variation of power gain as a function of input power for $L\times100\mu$m GaN MESFET at 4GHz.

In Fig. 4, a similar result showing gain compression due to device heating is depicted. The gain compression due to thermal effects for the 0.75μm gate length device is 0.75dB. Due to higher operating temperature the gain compression for the 0.3μm gate length device is 2.2dB. Similar effects in power added efficiency (PAE) is shown in Fig.5. Shorter gate length devices have better PAE due to higher power gain. PAE compression due to thermal effects is less in longer gate length devices and follows the trend observed in output power and gain compression.

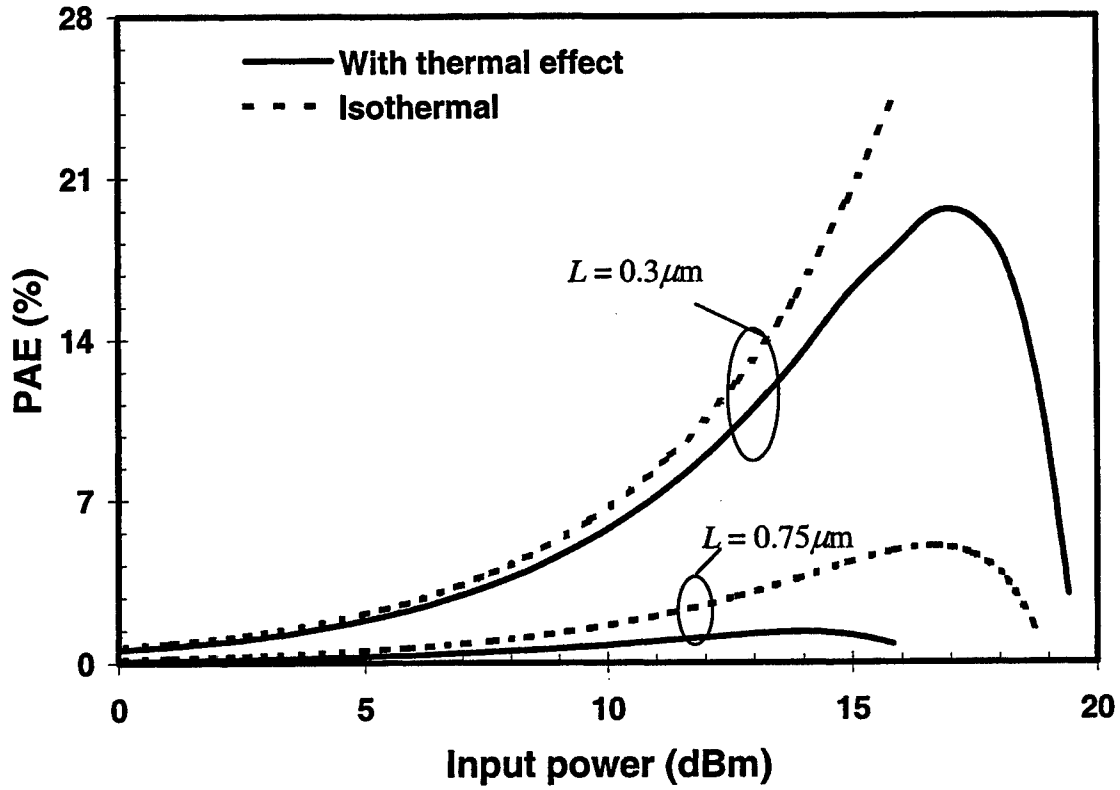


Fig.5. Variation of power added efficiency (PAE) as a function of input power for $L\times100\mu$m GaN MESFET at 4GHz.

Conclusions

RF power performances of GaN MESFETs are analyzed considering trapping and thermal effects. The DC to RF dispersions of transconductance and output resistance due to detrapping effects and transport parameter variations with channel temperature are incorporated. Volterra series technique is used to analyze device power performance and nonlinearities. Short channel devices demonstrate higher output power, power gain and PAE, however, better thermal stability is obtained in long channel devices.

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Dependence of Power and Efficiency of AlGaN/GaN HEMT's on the Load Resistance for Class B Bias

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The material properties of GaN and the AlGaN/GaN heterostructure such as high breakdown field and high sheet charge density, allow AlGaN/GaN HEMTs to be operated at significantly higher drain bias voltages as compared to other III-V compound semiconductor FETs [1]. As expected, larger RF voltage and current swings result in higher normalized output power at microwave frequencies. AlGaN/GaN HEMT's are capable of generating output power density in excess of 10W/mm [2], [3] in X-band, which is at least an order of magnitude larger than what is obtainable with GaAs FETs. In this paper, we will discuss the effect of the load impedance on measured output power (P_{out}) and efficiency (η) at various drain bias conditions in Class B mode. Dynamic loadlines extracted at the device's output are used for analysis of the trade-off between voltage and current swings at different load resistances and its effect on output power and efficiency.

I. Theoretical Background

Load impedance is related to the reflection coefficient at the device's output plane as

$$Z_{load} = R_{series} + jX_{series} = Z_0 \frac{1+\Gamma_{load}}{1-\Gamma_{load}} \qquad (1)$$

Load admittance can be represented as

$$Y_{load} = \frac{1}{R_{load}} - j\frac{1}{X_{load}} = \frac{R_{series}}{R_{series}^2 + X_{series}^2} - j\frac{X_{series}}{R_{series}^2 + X_{series}^2} \qquad (2)$$

For the purpose of direct correlation between the load resistance and the complex reflection coefficient, it is more illustrative to represent device loading conditions in terms of parallel combination of load conductance and load susceptance. The inverse of load conductance (real part of load admittance) in equation (2) is the actual load resistance connected in parallelel accross the drain-source junction of a FET.

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The same value of the load resistance R_{load} appears as a negative slope of a symmetry axis of measured dynamic loadlines (see Figures 4 and 5). On the other hand, loadline looping is caused by series reactance X_{series}, which makes the output current lag behind the output voltage waveform (in a case of inductive reactance). When series reactance becomes zero, voltage and current waveforms are exactly in antiphase, the loadline becomes purely resistive and collapses onto a line with the slope equal to the negative of the load resistance.

To extract maximum possible microwave output power from an active semiconductor device, a specific load impedance has to be presented at the output device plane. Usually, the load impedance corresponding to the maximum output power is not the same as the ones corresponding to the maximum transducer gain (G_t), drain efficiency (η).

Optimum load impedances for optimum power and efficiency will be analyzed for Class B bias, when the device is biased at pinch-off. In the absence of RF current slump, this bias mode is preferable for high drain voltage operation of AlGaN/GaN HEMT's due to minimization of the adverse thermal effects. Also, we will make the following assumptions: 1) breakdown voltage is infinity; 2) second and higher harmonics are properly terminated such that microwave voltage waveform is sinusoidal and microwave current waveform is a half-wave rectifier. Under these assumptions the power of a Class B signal is equal to

$$P_{out} = \frac{V_{\max} - V_{\min}}{2\sqrt{2}} \frac{I_{peak}}{2\sqrt{2}} = \frac{(V_{ds(bias)} - V_{\min}) I_{peak}}{4}, \qquad (3)$$

where V_{min} and V_{max} are the two extrema of the voltage waveform and I_{peak} is the peak of the current waveform with zero being the minimum.

Drain efficiency is defined as the ratio of output power to dissipated DC power

$$\eta = \frac{P_{out}}{V_{ds(bias)} I_{ds(bias)}} \qquad (4)$$

For Class B bias, DC (average) value of the drain current can be shown to be equal to

$$I_{ds(bias)} = \frac{I_{peak}}{\pi} \qquad (5)$$

Power and drain efficiency will be analyzed for the three types of loadlines shown in Figure 1.

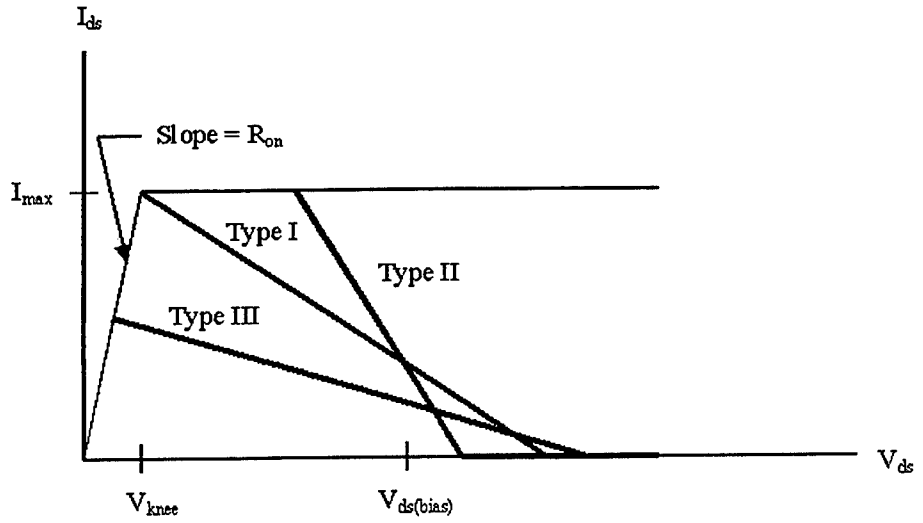


Figure 1. Three Types of Analyzed Loadlines

If we neglect the effect of reflection from the load, optimal load impedance resulting in maximum P_{out} (loadline of Type I in Figure 1), i.e. in simultaneous maximization of microwave voltage and current swings, is purely resistive and equal to

$$Z_{load(Pout)} = \frac{\pi}{\pi - 1} \frac{V_{ds(bias)} - V_{knee}}{I_{max}} + j0, \tag{6a}$$

where I_{max} is the open-channel current and V_{knee} is the minimum drain-source voltage at which I_{max} is attainable.

The maximum output power and drain efficiency corresponding to the load impedance $Z_{load(Pout)}$ are equal to

$$P_{out\,max} = \frac{(V_{ds(bias)} - V_{knee}) I_{max}}{4} \tag{6b}$$

$$\eta = \frac{\pi}{4} \frac{V_{ds(bias)} - V_{knee}}{V_{ds(bias)}} \tag{6c}$$

For an ideal case of V_{knee} being 0V, drain efficiency for Class B is equal to $\pi/4$=78.5%.

Load resistance smaller than $Re(Z_{load(Pout)})$, corresponding to the loadline of Type II in Figure 1, results in the maximum RF current swing and reduced RF voltage swing. I_{peak} is equal to the open-channel current I_{max}, the minimum RF voltage is larger than the knee voltage and is limited to

$$V_{min} = V_{ds(bias)} - \frac{\pi - 1}{\pi} I_{max} R_{load} > V_{knee} \tag{7a}$$

The resulting output power and corresponding drain efficiency are proportional to load resistance. Output power does not depend on drain bias voltage, while drain efficiency is inversely proportional to drain bias voltage

$$P_{out} = \frac{\pi - 1}{\pi} \frac{I_{\max}^2 R_{load}}{4} < P_{out\max} \tag{7b}$$

$$\eta = \frac{\pi - 1}{4} \frac{I_{\max} R_{load}}{V_{ds(bias)}} < 78.5\% \ . \tag{7c}$$

Load resistance larger than $Re(Z_{load(Pout)})$, corresponding to the loadline of Type III, results in reduced RF current swing but increased RF voltage swing. Both peak RF current and minimum RF voltage are functions of load resistance, on-resistance R_{on} and drain bias voltage:

$$I_{peak} = \frac{\pi}{(\pi - 1)R_{load} + \pi R_{on}} V_{ds(bias)} < I_{\max} \tag{8a}$$

$$V_{\min} = \frac{\pi R_{on}}{(\pi - 1)R_{load} + \pi R_{on}} V_{ds(bias)} < V_{knee} \tag{8b}$$

and the corresponding output power and drain efficiency are

$$P_{out} = \frac{V_{ds(bias)}^2}{4} \frac{\pi(\pi - 1)R_{load}}{\left[(\pi - 1)R_{load} + \pi R_{on}\right]^2} < P_{out\max} \tag{8c}$$

$$\eta = \frac{\pi}{4} \frac{(\pi - 1)R_{load}}{(\pi - 1)R_{load} + \pi R_{on}} \rightarrow 78.5\% \,|_{R_{load} >> R_{on}} \tag{8d}$$

In this case, an increase in load resistance leads to an increase in drain efficiency up to 78.5% for $R_{load} >> R_{on}$, and causes a decrease in the output power. Formula (8d) indicates that as long as the load resistance is larger than the optimum power load resistance defined in formula (6a), drain efficiency should be ideally independent of drain bias voltage. This observation is confirmed by experimental results presented below. Also, similar conclusions were reached by Y.-F. Wu [3] for class A bias-dependent operation of AlGaN/GaN HEMT's.

Theoretical dependence of output power and drain efficiency on load resistance, derived assuming a finite on-resistance and using formulas (6b-c), (7b-c), (8c-d) are plotted in Figures 2 and 3. The optimum power load resistance results in the maximum efficiency only for zero on-resistance case. For a real device with some finite on-resistance, optimum efficiency load resistance will always be larger than the optimum power load resistance.

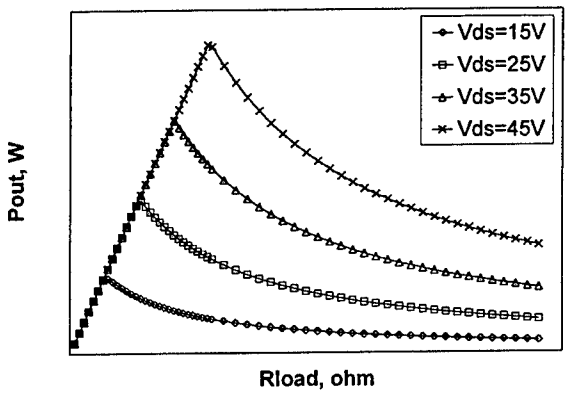


Figure 2. Theoretical Dependence of Output Power on Load Resistance

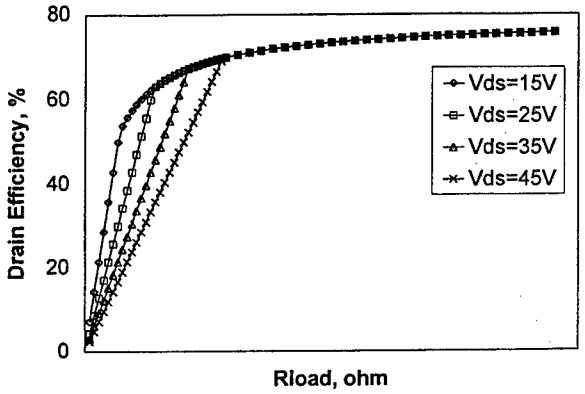


Figure 3. Theoretical Dependence of Drain Efficiency on Load Resistance

The load impedance, corresponding to the maximum small-signal transducer gain, is equal to the complex conjugate of the device output impedance in order to minimize reflection from the load

$$Z_{load(Gt)} = Z_{out}^{*} \tag{9}$$

For optimum large-signal performance, some load reflection is inevitable due to the fact that optimum power and efficiency load resistances in most cases are going to be smaller than the device's output resistance. To compensate for the drain-source and drain pad capacitances, load impedance should contain some inductive reactance. This load reactance introduces a delay between microwave output current and output voltage waveforms. On the extreme, if the load reactance becomes infinitely larger than the load resistance, output current waveform lags the voltage waveform by 90°, and the active power at the fundamental frequency goes to zero.

In order to include the effect of reflection from the load, formula (3) for maximum output power has to be modified as follows

$$P_{out} = \frac{(V_{ds(bias)} - V_{\min})I_{peak}}{4} \frac{1-|\Gamma_{load}|^2}{|1-\Gamma_{load}\Gamma_{out}|^2} \tag{10}$$

II. Continuous Wave Power Measurements with 2nd Harmonic Termination

Power performance of AlGaN/GaN HEMTs on SiC has been characterized using a harmonic load-pull system, in which fundamental source and load reflection coefficients can be varied from 0 to 0.8 in magnitude and from 0 to 180° in phase. 2nd harmonic load reflection coefficient has a range from 0 to 0.6 in magnitude and 0 to 180° in phase.

Continuous wave (CW) power measurements were made on a 0.25μm x 1.5mm device at 10 GHz. The gate bias was set very near pinch-off for class B operation. The source impedance was set to be the complex conjugate of the device input impedance to maximize power transfer between the signal source and the device. Then, two

fundamental load reflection coefficients of interest were determined and set. A second harmonic load pull was used to determine optimum 2nd harmonic load impedance. This allows one to approximate the microwave voltage waveform as an ideal sinusoid and microwave current waveform as half-wave rectifier.

Input power sweeps were taken at drain voltages from 15V to 40V with 5V steps at two load reflection coefficients. Reactive parts of load admittance (impedance) are attempted to be kept equal within the accuracy of the load-pull setup, and real parts differ to explore the effect of load resistance on bias-dependent large-signal device performance:

1) Γ_{load1}=0.703∠132°, which corresponds to R_{load1}=53.4ohm and X_{load1}=26ohm as calculated based on formulas (1) and (2);

2) Γ_{load2}=0.695∠124°, which corresponds to R_{load2}=79.8ohm and X_{load2}=34.4ohm.

1dB and 3dB compression output powers as functions of the drain bias voltage for both load reflection coefficients are shown in Figure 4. Drain efficiencies are shown in Figure 5.

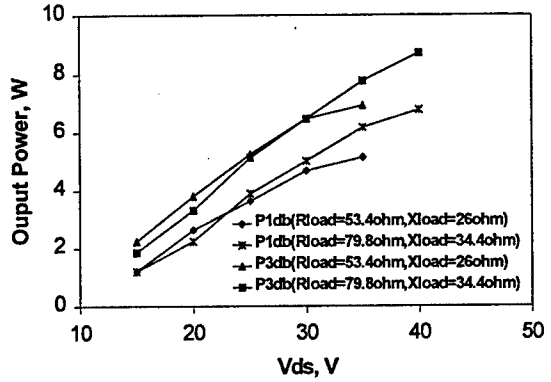


Figure 4. CW Linear and Maximum Output Powers Measured at 10GHz and Various Drain Bias Voltages for the two load impedances

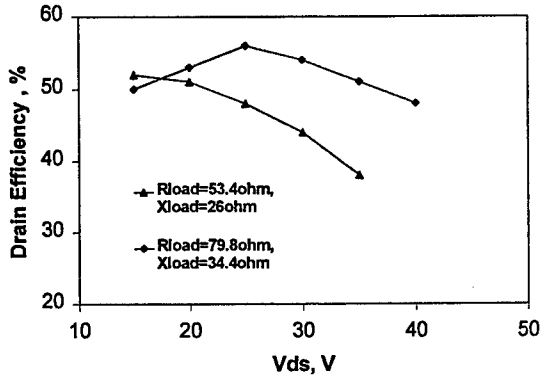


Figure 5. CW Drain Efficiency Measured at 10GHz and Various Drain Bias Voltages for the two load impedances

Loading the device with the load reflection coefficient Γ_{load1} results in slightly higher power and efficiency at low drain biases. However, at bias voltages above 20V, the load resistance R_{load1}=53.4ohm apparently becomes smaller than the optimum power load resistance as defined in formula (6a). As a result, efficiency starts to decrease with increase in the bias voltage as predicted by formula (7c). The continuous increase in the output power above 20V, contradicts formula (7b), according to which for a Type II loadline, P_{out} should be independent of the drain bias voltage. We attribute this phenomena to increase in I_{max} due to some finite output conductance and the floating-body effect, found by Nuttinck et al [4] in AlGaN/GaN HEMT's on SiC substrates.

On the other hand, the load resistance R_{load2}=79.8ohm remains larger than the optimum power load resistance, meaning it stays the Type III loadline, up to drain bias voltage of 40V. Thus, drain efficiency is almost independent of the bias voltage as predicted by formula (8d). Also, R_{load2} yields more linear device response at large drain bias voltages as evidenced by higher 1dB compression power data in Figure 4.

III. Pulsed Power Measurements with Dynamic Loadline Extraction

To visualize the effect of load resistance on RF output voltage and current waveforms, pulsed power measurements were performed at 8 GHz on Maury™ load pull system with HP Microwave Transition Analyzer (MTA) being used in place of input, reflected and output power meters. MTA allows to accurately measure power waveforms at its own calibration planes. The RF voltage and current waveforms at the device planes are then extracted by using the known load tuner's scattering parameter matrices at fundamental, second and third harmonics [5]. The RF loadlines, expressed as functions Iout = f(Vout) are then plotted.

To minimize thermal effects and alleviate reduced device performance due to rise in the channel temperature, the pulse width was set to 500 ns with 1% duty cycle.
Loadlines for two load impedances:
1) R_{load}=53.1ohm, X_{load}=35.8ohm;
2) R_{load}=78.2ohm, X_{load}=48.5ohm
for drain voltages from 15 to 35V are plotted in Figures 6 and 7.

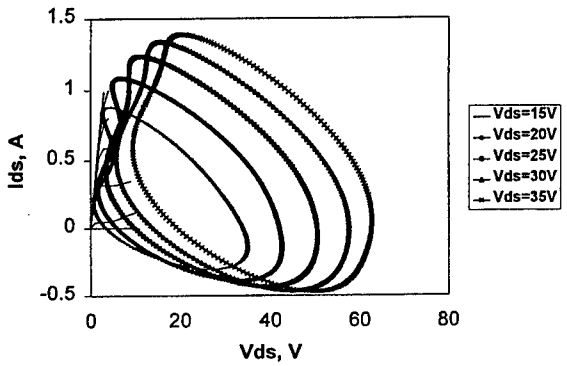


Figure 6. Pulsed Dynamic Loadlines Measured at 8GHz and Various Drain Bias Voltages for R_{load}=53.1ohm X_{load}=35.8ohm

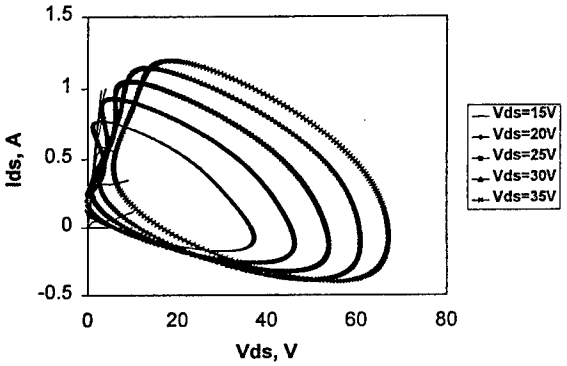


Figure 7. Pulsed Dynamic Loadlines Measured at 8GHz and Various Drain Bias Voltages for R_{load}=78.2.1ohm X_{load}=48.5ohm

Similarly to the 10 GHz CW results, drain efficiency, as shown in Figure 8, for the larger load resistance varies insignificantly with drain bias voltage, and the minimum RF voltage is only limited by the DC knee voltage, which helps to maximize RF voltage swing. On the other hand, smaller load resistance becomes less than the optimum power load resistance at approximately 25V drain bias voltage. At this point, minimum RF voltage becomes limited by the open-channel current and starts to increase with the bias voltage, which causes the drain efficiency to drop.

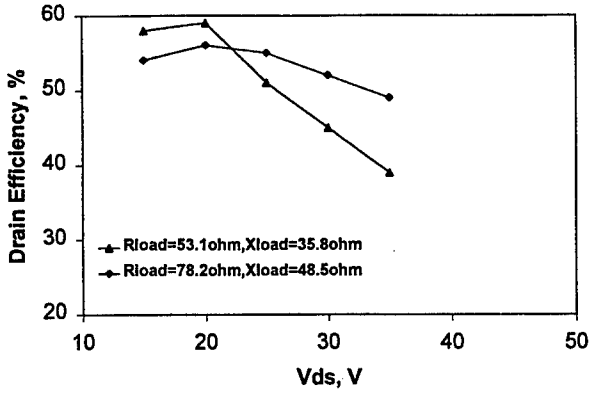


Figure 8. Drain Efficiency Measured Under Pulsed Conditions at 8GHz and Various Drain Bias Voltages for the two load impedances

III. Conclusions

We investigated the effects of the load resistance on large-signal performance of discrete AlGaN/GaN HEMT's. Observed functional dependencies of output power and drain efficiency at various load resistances and drain bias voltages are explained analytically in terms of device's DC I-V metrics: the open-channel current, knee voltage and on-resistance.

Measured dynamic loadlines for the two load resitances of interest at different bias voltages allowed visualization of the limiting mechanisms and trade-offs between RF voltage and current swings and their effect on output power and efficiency.

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AlGaN/GaN HEMTs grown by Molecular Beam Epitaxy on sapphire, SiC, and HVPE GaN templates

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ABSTRACT

Molecular Beam Epitaxy of GaN and related alloys is becoming a rival to the more established Metalorganic Vapor Phase Epitaxy. Excellent control of impurity, interface abruptness, and in-situ monitoring of the growth are driving the increase in quality of MBE epilayers. We have developed nucleation schemes with plasma-assisted MBE on three types of substrates, consisting of sapphire, semi-insulating (SI-) SiC, and HVPE SI-GaN templates on sapphire. While sapphire and SI-SiC are established substrates for the growth of AlGaN/GaN HEMT epilayers, HVPE GaN templates may provide a path to low-cost large-diameter substrates for electronic devices.

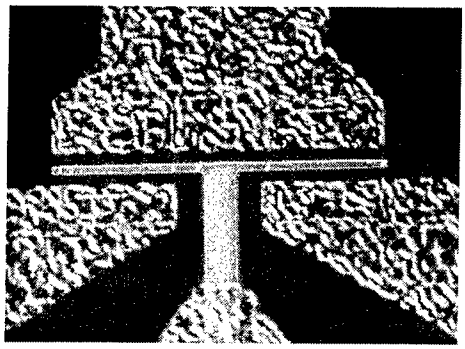


Figure 1: Micrograph of finished HEMT device, 2 fingers of 2μm x 25μm gates each

We compare device results of HEMTs fabricated on these substrates. As a metric for device performance, the saturated RF power output in class A operation is measured at 2 GHz. We achieved a saturated power density of 2.2 W/mm from HEMTs on sapphire, 1.1 W/mm from HEMTs on HVPE GaN templates on sapphire, and 6.3 W/mm from HEMTs on semi-insulating 6H-SiC substrates. The difference in output power can be attributed to self-heating due to insufficient thermal conductivity of the sapphire substrate, and to trapping in the compensation-doped HVPE template.

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INTRODUCTION

AlGaN/GaN HEMT devices have delivered extremely high RF output power densities at microwave frequency. Up to 11 W/mm have been demonstrated on MOCVD-grown AlGaN/GaN layers [1, 2], and up to 8 W/mm with layers grown by plasma-assisted MBE [3]. In the recent past, growth of AlGaN/GaN layers by MBE has received increased attention with the demonstration of high quality epilayer films. MBE growth offers certain advantages over MOCVD, such as very low background impurities, in-situ growth monitoring via RHEED, and the ability to produce atomically sharp interfaces. Epitaxy of GaN films is currently done mostly on foreign substrates, notably sapphire and SiC. The substantial lattice mismatch needs to be taken up in a dislocated buffer layer. The quality of the 2DEG, as measured by the Hall low field mobility, is largely dependent on the growth conditions at nucleation on the substrate, and during growth of the buffer layer.

We have developed nucleation layer schemes on both sapphire and SiC, involving a thin AlN layer deposited at the beginning of the growth. In both cases, the nucleation and subsequent growth of GaN result in films with Ga-face polarity, suitable for high-mobility AlGaN/GaN 2DEGs.

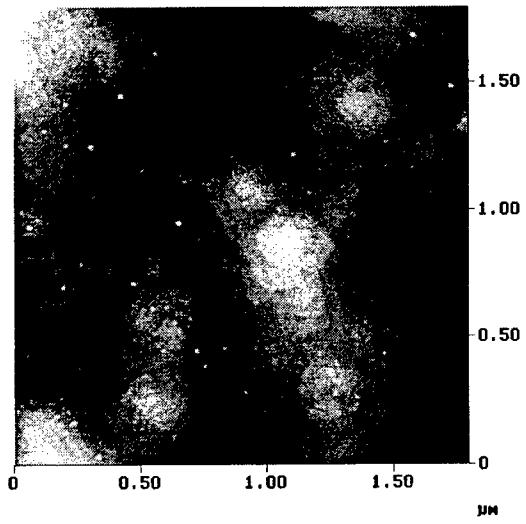


Figure 2: AFM image of MBE GaN/AlGaN heterostructure grown directly on sapphire

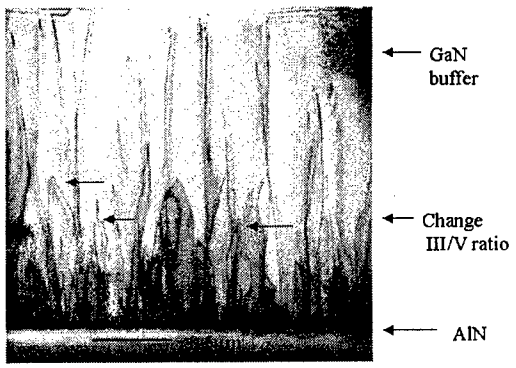


Figure 3: cross-sectional TEM of two-step GaN buffer on sapphire

The 2DEG properties can be further enhanced through buffer layer engineering. We developed a two-step growth process to reduce the number of extended defects present at the AlGaN/GaN interface, while keeping the surface smooth. A Ga/N ratio close to unity is chosen in the first half of the buffer growth. The slightly roughened surface leads to enhanced defect interaction due to the spatial proximity of neighboring defects. During the second half of the buffer growth, a Ga/N ratio greater than one is adjusted to smooth out the growth front (Figure 3). Only minimal defect interaction occurs in this regime, but the AlGaN/GaN interface is smooth (Figure 2), which minimizes interface roughness scattering.

GROWTH ON HVPE GAN TEMPLATES

Thick GaN templates grown by HVPE on sapphire substrates are used as a quasi-homoepitaxial substrate for the GaN MBE growth [4]. The threading dislocation at the surface of these templates is reduced to the 10^8 cm^{-2} range. We grow the MBE layer stack directly on top of the HVPE template without additional nucleation layers as in the case of growth on sapphire and SiC. As grown HVPE GaN is residually *n*-type due to Si and O impurities in the range of 10^{16} cm^{-3}.

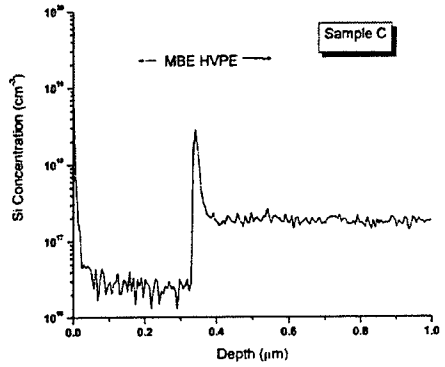


Figure 4: SIMS profile of MBE GaN on HVPE GaN template

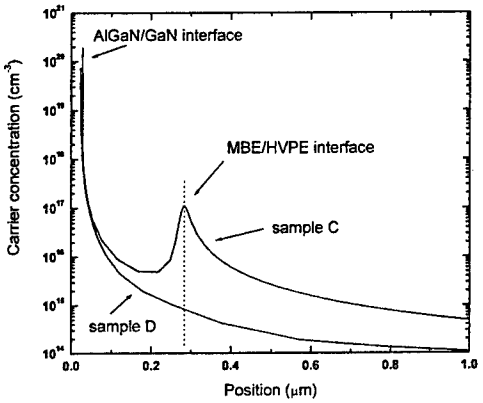


Figure 5: CV profile before (C) and after (D) correction of the compensation doping

To obtain semi-insulating layers, Zn is used as a compensating deep acceptor. A concentration of 10^{17} cm^{-3} Zn yields semi-insulating HVPE GaN layers. SIMS (Figure 4) and CV (Figure 5) profiling shows the absence of net dopants and charge at the HVPE/MBE interface. However, the buried HVPE nucleation layer is degenerately *n*-type. Thermal considerations are paramount for high-power microwave devices. Sapphire with its thermal conductivity of only 0.30 W/cmK limits the device output power severely.

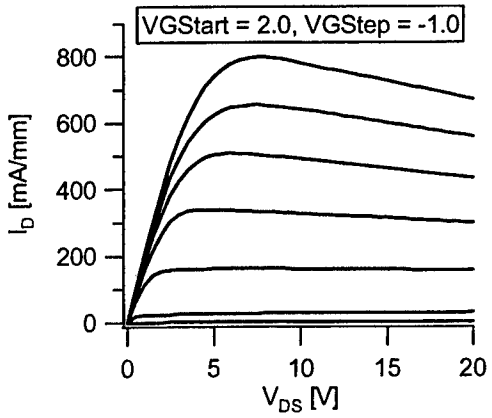


Figure 6: IV curve of HEMT on HVPE GaN

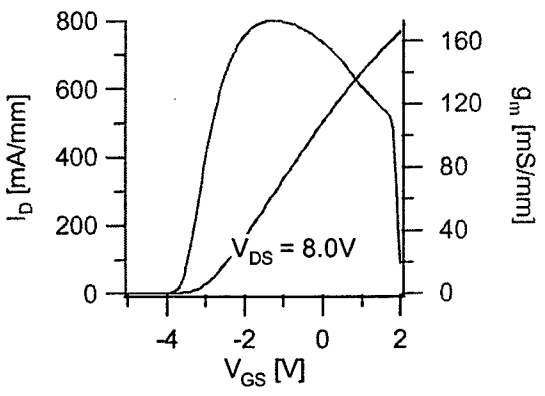


Figure 7: transfer characteristics of HEMT on HVPE GaN

A thick GaN layer helps spreading the heat conically under the active area of the power device, effectively decreasing the thermal impedance of the sapphire/GaN combination. Further enhancement may be reached with flip-chip package designs.
We were able to produce HEMT devices on these layers that show good pinch-off behavior, proving the absence of a parasitic channel in the HVPE template (Figure 6). Due to the low defect concentration in MBE layers grown on HVPE templates, we were able to measure record low-temperature mobilities for low-density 2DEGs up to 75,000 cm^2/Vs at 4K.

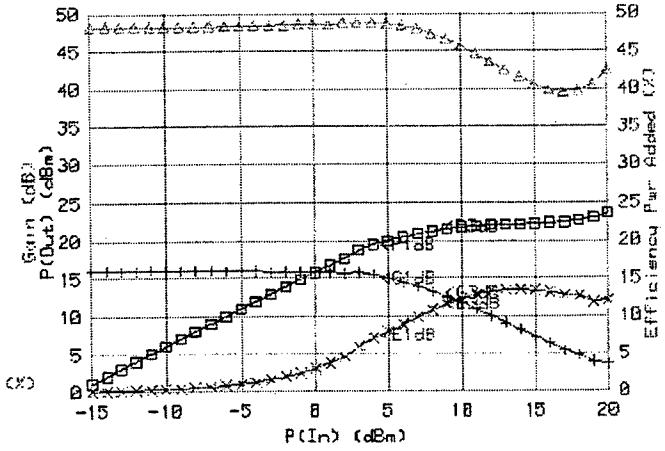


Figure 8: load-pull data of 200 µm wide HEMT on HVPE GaN

GROWTH DIRECTLY ON SAPPHIRE

Sapphire is still widely used as a substrate for GaN growth due to its low cost as compared to SiC, allowing for cost-effective development of device processing steps such as ohmic contact metallization. Using a thin AlN nucleation layer, we reproducibly yielded Ga-face AlGaN/GaN heterostructures [5] with mobilities higher than 1,200 cm^2/Vs at a carrier concentration of approximately 10^{13} cm^{-2}.

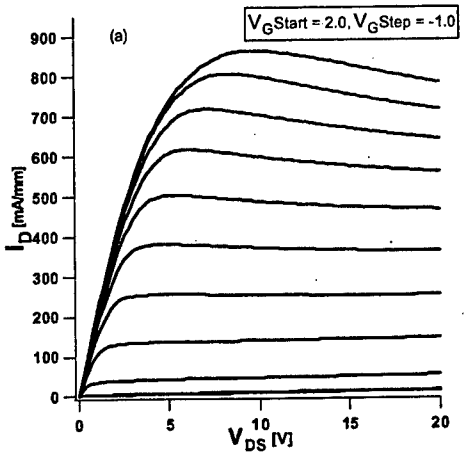


Figure 9: IV curve of 100 µm wide HEMT on sapphire

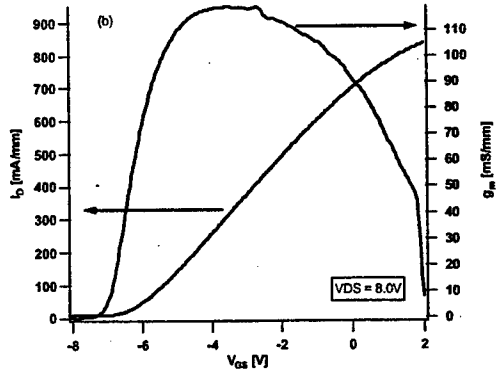


Figure 10: transfer characteristics of 100 µm wide HEMT on sapphire

We fabricated HEMTs from these layers, DC data are shown in Figure 9 and Figure 10. The RF output power is limited by the thermal properties of the substrate. We obtained 2.2 W/mm at 2 GHz from a 100µm wide HEMT on sapphire (Figure 11) in class A device operation.

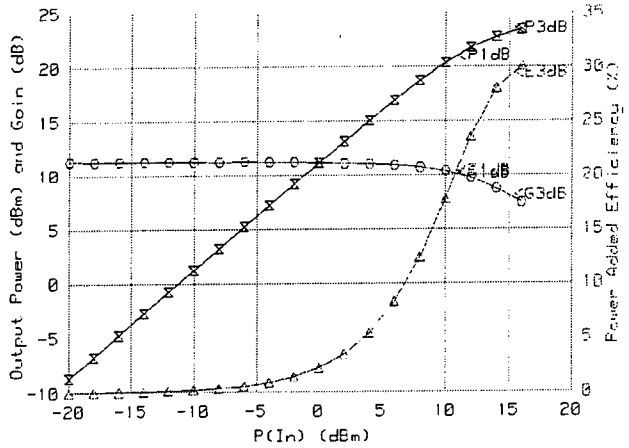


Figure 11: class A load-pull data of 100 µm wide HEMT on sapphire, V_{DS} = 20V, I_{DS} = 266 mA/mm

GROWTH ON SEMI-INSULATING 6H-SIC

SiC currently provides the best compromise in thermal management and lattice mismatch for epitaxial growth of GaN. We used semi-insulating 6H-SiC substrates from Sterling Semiconductor for our AlGaN/GaN HEMTs on SiC. Prior to MBE growth, the substrates receive an additional chemical mechanical polish.

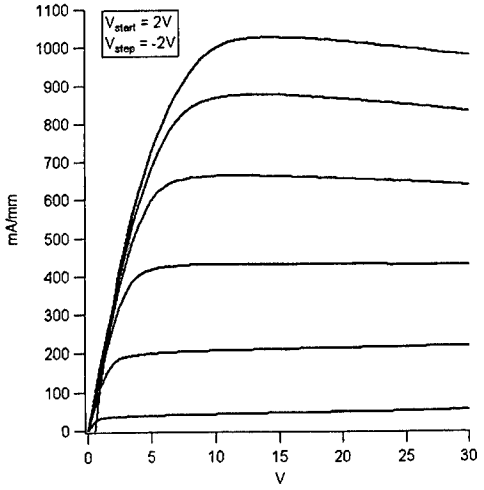


Figure 12: IV curve of 25 µm wide HEMT on 6H-SiC

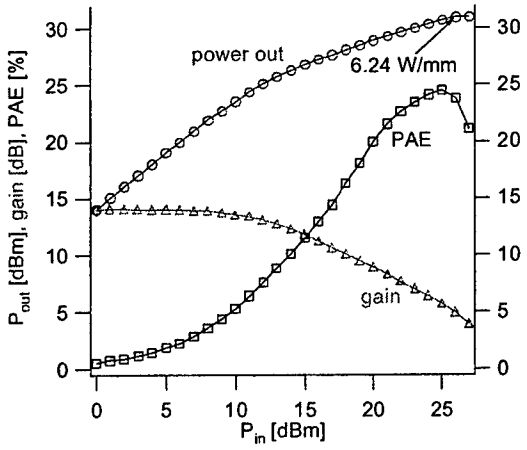


Figure 13: class A load pull data, 200 µm wide HEMT on 6H-SiC; VDS = 40V

A thin AlN film serves as a nucleation layer. Our standard AlGaN/GaN layer structure consists of approximately 2 µm of GaN, followed by a 25 nm thick $Al_{0.30}Ga_{0.70}N$ barrier, and a 5 nm thick undoped GaN cap. Part of the barrier is doped with silicon ($8 \cdot 10^{17}$ cm^{-3}) to reduce the

resistance of the ohmic contacts. At room temperature, we measure Hall mobilities higher than 1,300 cm^2/Vs and a sheet carrier concentration of $1.2 \cdot 10^{13}$ cm^{-2}, resulting in a sheet resistance approximately 350 Ω/□. We were able to reproducibly process HEMTs from these layers, with a saturated drain current of more than 1 A/mm. Most devices yielded a saturated output power of around 4.5 W/mm at 2 GHz. The best device showed a saturated output power of 6.2 W/mm with an associated gain of 5 dB. The power added efficiency was measured to 24%. All values were obtained from unpassivated devices in class A operating condition [6].

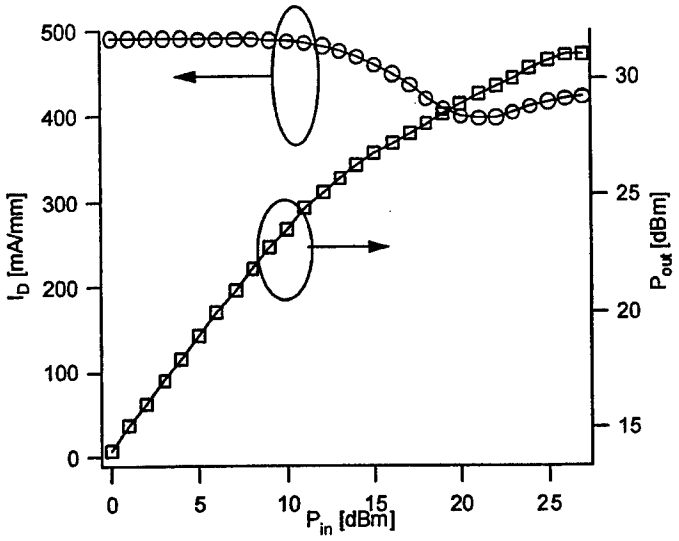


Figure 14: drain current dispersion of same device as shown in Figure 13

It is noteworthy that the drain current dispersion in these devices is very low, given the absence of a passivating layer. From Figure 14, a decrease of the DC drain current of only 17% from the small-signal regime towards saturation was recorded. At first, the drain current drops, until the drive signal voltage is large enough to bias the gate-source Schottky diode in forward direction, leading to rectification of the input signal and a positive shift of the internal gate bias, which increases the drain current.

HEMT DEVICE FABRICATION AND MEASUREMENT

HEMT devices are fabricated with optical lithography (Figure 1). The short turn-around time of our robust device process enables quick feedback to the epilayer growth. The devices are mesa-isolated in an ICP Chlorine etch step. Ohmic contacts are deposited by e-beam and thermal (Al) evaporation. We use Ti/Al/Ni/Au or Ti/Al/Ti/Au for our ohmic contact metallization. Transfer resistances as low as 0.3 Ω-mm have been realized, routinely we obtain 0.5 Ω-mm after rapid thermal annealing in nitrogen at 850°C. Finally, Schottky gates are deposited by e-beam evaporation of Ni followed by a thick Au layer. Presently, all our devices are *unpassivated* when measured.

The DC characteristics of the HEMTs are measured with an HP4145B semiconductor parameter analyzer. We measure saturated drain current densities of more than 1 A/mm on SiC and on HVPE GaN templates. On sapphire, we achieved a maximum drain current of 880 mA/mm. The gate leakage current is typically around 150 μA/mm in pinch-off at 20 V_{DS}. We obtained a

maximum transconductance of 180 mS/mm; in addition, the transconductance is relatively flat across a wide rage of gate voltages. Pinch-off occurs between –4 and –10 V_{GS}, depending on sheet charge and barrier structure. The devices break down at 95 V_{DS} (three-terminal breakdown). The RF power output is measured with an ATN LP1 automated load-pull measurement setup at 2 GHz. Small-signal *S*-parameters are recorded with an HP8510C network analyzer and an HP8516A test set in the passband of the tuners between 2 and 8 GHz. We extrapolated f_t/f_{max} of 6 and 16 GHz, respectively, for our devices with a gate length between 1 and 2 μm. We tested devices on all three substrates on various wafers. The highest saturated power densities we found at 2 GHz were 2.2 W/mm on sapphire, 1.1 W/mm on HVPE templates, and 6.2 W/mm on SiC for a device periphery of 200 μm, with a drain voltage between 35 and 45 V.

DISCUSSION

The power density on SiC is limited in part by the large drain-source separation of 6 μm in our simple test mask, limiting the power-added efficiency as well. On sapphire, the power density is limited by the thermal impedance of the substrate, as evidenced by the negative output conductance visible in the IV curve. We expected the output power of devices on HVPE GaN templates between sapphire and SiC; however, we recorded only 1.1 W/mm. The unionized excess Zn acceptors in the HVPE GaN may act as trapping centers, which can be charged and act as a backgate on the 2DEG. Drain dispersion defined as the variation of the DC drain current with RF input power at constant gate and drain bias voltage is measured for all three substrates. On SI-SiC substrates, we observed as little as 7% drop in drain current with input power. On HVPE GaN templates, the drain current drops by 20%, indicating trapping in the substrate. Additionally, the gain compresses prematurely. The 1dB compression point is reached at 19 dBm output power and 4 dBm input power for a device with 200 μm periphery. The maximum power-added efficiency is only 14% on HVPE templates in class A operation, compared to 25% on SI-SiC.

CONCLUSION

We have grown high-quality AlGaN/GaN HEMT device layers by plasma-assisted MBE on various substrates. The highest saturated output power of 6.2 W/mm was measured from unpassivated HEMT devices on SI 6H-SiC at 2 GHz in class A operation. Record low-field mobilities up to 75,000 cm^2/Vs were measured from AlGaN/GaN MBE films grown on GaN templates prepared by Hydride Vapor Phase Epitaxy.

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PS-5

REDUCTION OF BUFFER LAYER LEAKAGE CURRENT IN AlGaN/GaN HEMTs GROWN BY PLASMA MBE

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E.R. Glaser,
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PAPER UNAVAILABLE FOR PUBLICATION

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Subterahertz Detection by High Electron Mobility Transistors at Large Forward Gate Bias

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Abstract

The electron delay time associated with the electron propagation across the FET gate barrier layer under high positive gate bias is expected to induce a dynamic negative differential conductance and enhance the growth of plasma waves in the channel [1]. This dynamic negative conductance is related to the phase shift between the current and voltage waveforms caused by the electron time delay during the electron tunneling through the gate barrier. We present experimental investigations of the plasma wave detector responsivity at 200 GHz and 600 GHz radiation for long channel AlGaAs/GaAs and AlGaInN/GaN based HEMTs at 8 K and 300 K. The appearance of detector response correlated with an increase of the injected gate current under the forward gate bias is reported for both types of the investigated devices. Our results confirm that a large gate current can enhance the excitation of plasma waves.

I. Introduction

Excitation of plasma waves in a channel of a high electron mobility transistor (HEMT) can be used for emission and detection of terahertz radiation [2-13]. When the electron mobility is sufficiently high, the HEMT channel serves as a resonant cavity for the plasma waves, and the detectivity has a maximum at the fundamental frequency of the plasma waves in the channel and its harmonics. When the electron mobility is relatively small, the plasma waves are overdamped, and the detection is nonresonant. Both types of the detection (resonant and nonresonant) have been observed [6, 8, 12, 13]. Recently, we analyzed dynamic behavior of the electron system in high-electron mobility transistors (HEMTs) associated with tunneling injection from the two-dimensional channel into the gate under forward bias. We showed that the propagation of the injected electrons across the barrier layer could result in the self-excitation of plasma oscillations in the HEMT [1]. This self-excitation is caused by the dynamic negative conductance that comes from the phase shift between the current and voltage waveforms resulting from the electron time delay. As another consequence of the same effect, we expect that the detectivity should have a peak at high

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gate bias when the gate current becomes large. In this paper, we report on the first observation of such detectivity peaks at large forward gate bias in GaAs and GaN-based HEMTs.

II. Experimental Results and Discussion

The detectors used in our experiments are long-channel AlGaAs/GaAs and AlGaN/GaN based High Electron Mobility Transistors (HEMTs). The gate length of GaAs HEMT is 2.5 μm. The separation between the gate and the source of GaAs HEMT is 2 μm, and the separation between the gate and the drain is 7 μm. The gate length of GaN HEMT is about 1.5 μm. For low temperature measurements we used a closed cycle compressor based cryostat with a temperature controller. The detector temperature was stabilized in the temperature range from 8 K to 300 K. The detectors were exposed to the 200 and 600 GHz radiation from two different Gunn oscillator systems.

The current voltage characteristics of the GaAs and GaN devices at $T = 8$ K are shown in Fig.1 a and Fig.1 b, respectively.

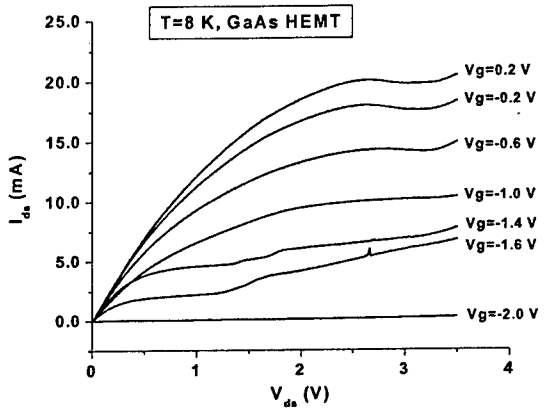


Fig.1 (a) The current-voltage characteristics of GaAs HEMT at 8K

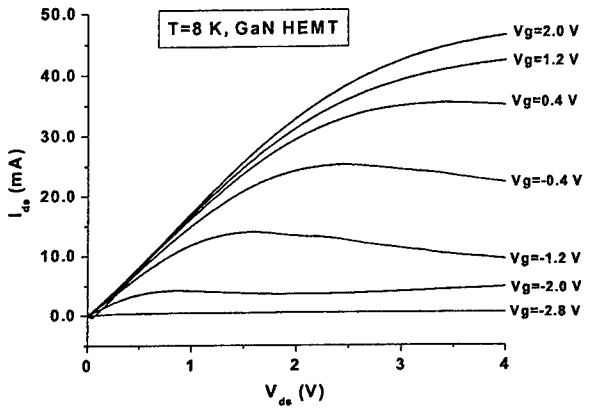


Fig.1. (b) The current-voltage characteristics of GaN HEMT at 8K

The transfer characteristics of the GaN-based and GaAs-based devices are shown in Fig.2.

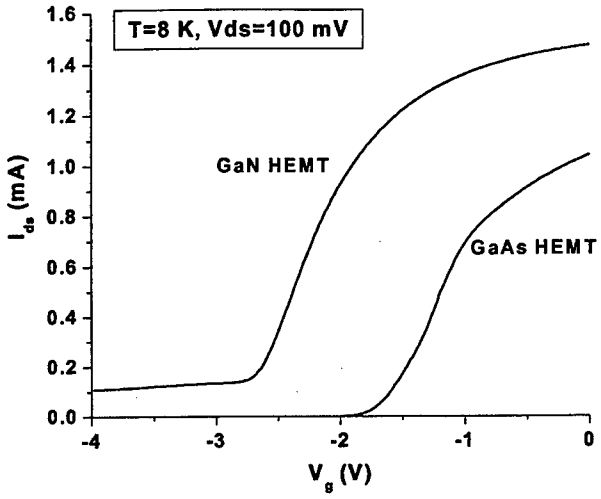


Fig.2. Transfer characteristics of GaAs and GaN HEMTs at 8K

As seen from Fig. 2, the threshold voltages of the devices are V_T=-2.8V for GaN HEMT and V_T=-1.7V for GaAs HEMT.

Fig. 3a shows the detector response of GaN HEMT detector exposed to 201 GHz radiation at 8 K.

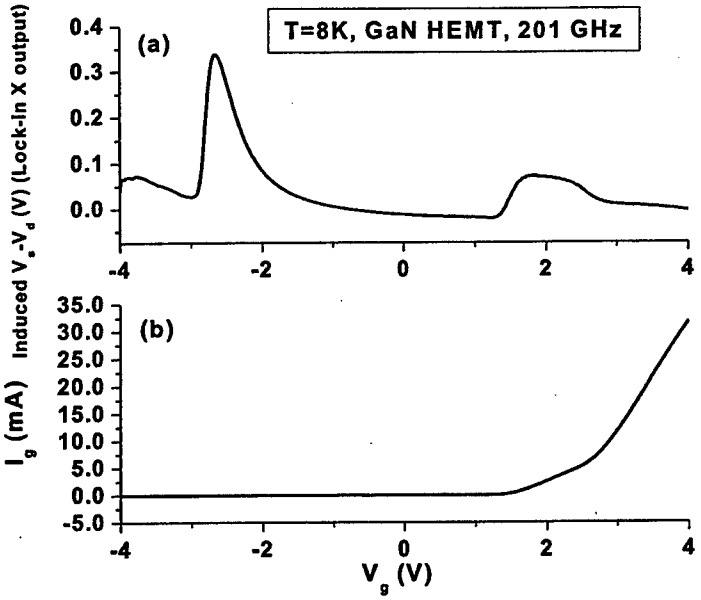


Fig. 3. (a) The GaN HEMT detector response to 201 GHz radiation at T=8 K and (b) Gate current versus gate voltage for the positive (forward) gate bias at 8 K.

One can observe two pronounced maxima. The first one near the transistor threshold –2.6V is due to non-resonant detection, which was extensively discussed in Ref. [12]. We attribute the second peak at V_g=2V to the new mechanism associated with tunneling or thermionic-field electron injection from the two-dimensional channel into the gate under the forward bias [1]. The current voltage characteristic of the gate barrier is shown in Fig.3 b. As can be seen from Fig.3 b the maximum of the detector signal under positive gate bias is correlated with the increase of the gate current.

Similar correlation between the detectivity increase and the gate current was observed for the GaAs-based transistor. The detector response for a few frequencies ranging between 188 GHz and 212 GHz is shown in Fig. 4.

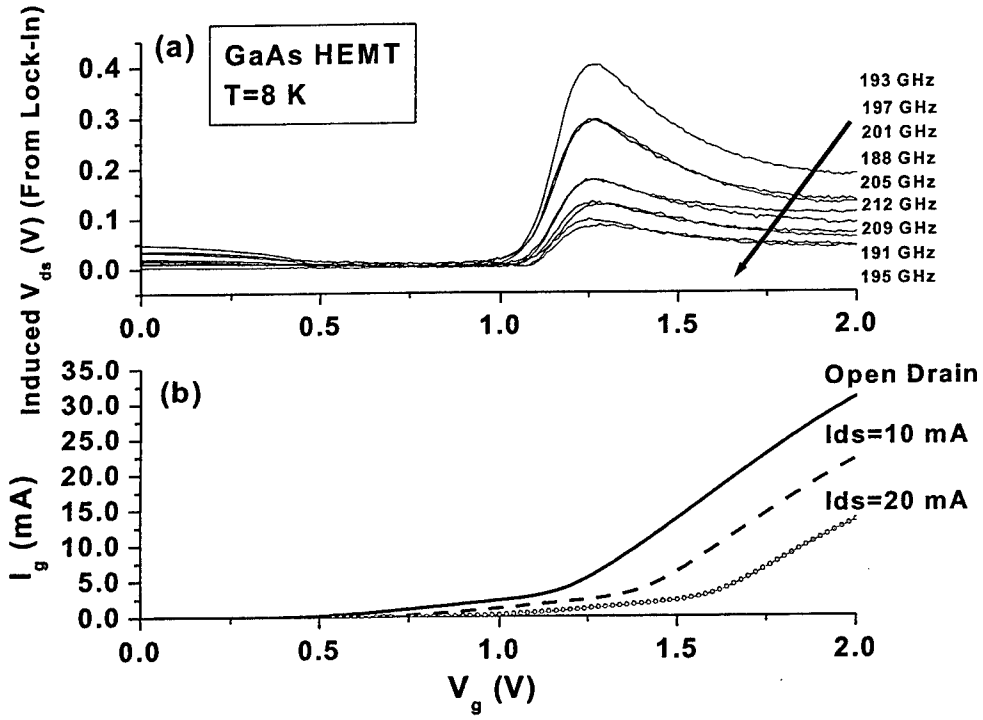


Fig. 4. (a) 188 GHz to 212 GHz radiation response of GaAs HEMT under large positive gate bias at 8 K and (b) Positive bias gate current voltage characteristics for GaAs HEMT.

The gate current voltage characteristic is shown in Fig. 4 b. From comparison of figures 4 a and 4 b, one can see that both the detector signal and the gate current start to increase (simultaneously) when the gate bias reaches +1V.

The GaAs detector response was also investigated as a function of the source drain current. The results are shown in Fig.5

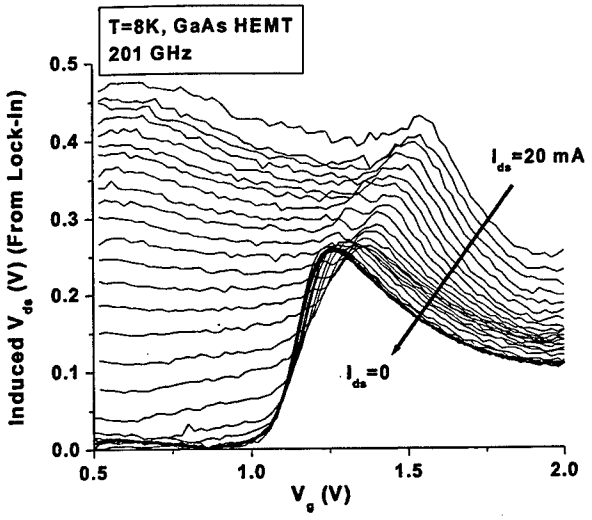


Fig. 5. 201 GHz radiation response of GaAs HEMT under large gate bias with DC drain current at 8K. I_{ds} increases from 0 to 20mA. The drain current step for I_{ds} in the range between 1mA and 20mA is equal to 1mA.

As seen from the Fig. 5, the higher is the drain current, the less pronounced is the maximum at positive gate bias (but the higher is the overall response). The gate current decreases with the increase of the drain current (see Fig. 4 b.). Therefore, the decrease at the maximum in Fig. 5 confirms the suggestion that it is related to the gate current [1].

We also performed the detection experiments for 600 GHz radiation. The results are shown in Fig 6a for GaAs HEMT and in Fig.6 b for GaN HEMT. For this frequency, only detection for negative gate voltages close to the threshold voltage was observed (see Ref. [12]). For positive gate voltages only noisy broadband signals were registered.

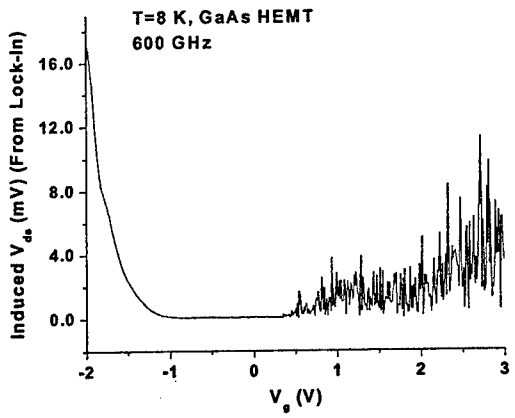


Fig. 6. (a) 600 GHz radiation response of GaAs HEMT at 8 K

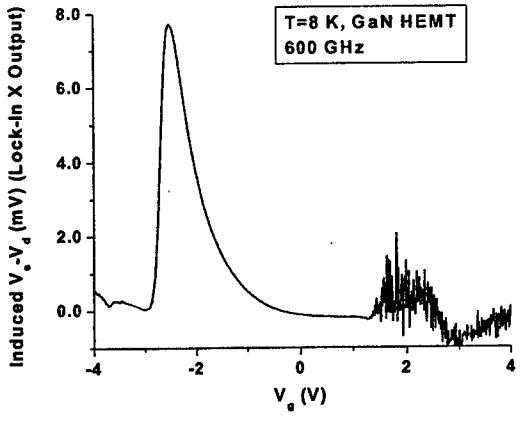


Fig. 6. (b) 600 GHz radiation response of GaN HEMT at 8 K

One of the possible reasons can be that the resonant frequency of the plasma oscillations is much smaller than 600 GHz.

The fundamental frequency of the plasma oscillations is given by [3]:

$$f_0 = \frac{1}{4L}\sqrt{\frac{qU_0}{m}} \tag{1}$$

where m is the effective mass, L is the gate length, and $U_o = V_g - V_T$ is the gate voltage swing. The calculated dependence f_o versus U_o is shown in Fig. 7. The gate lengths for GaAs and GaN HEMTs in calculation are 2.5 μm and 1.5 μm, respectively. One can see that the 200 GHz resonant frequency lies well in our measurement range (V_g=0 to 4V) while 600 GHz is out of this range.

Two big dots in Fig. 7 are the measured peak positions of radiation responsivity for GaAs and GaN HEMTs at large gate bias, respectively. They are closer to the resonant frequency of 200 GHz than that of 600 GHz. The large width of the maximum at large gate bias means that the measurement frequency does not correspond to the resonant frequency and that the response (if it exists) is fairly broad.

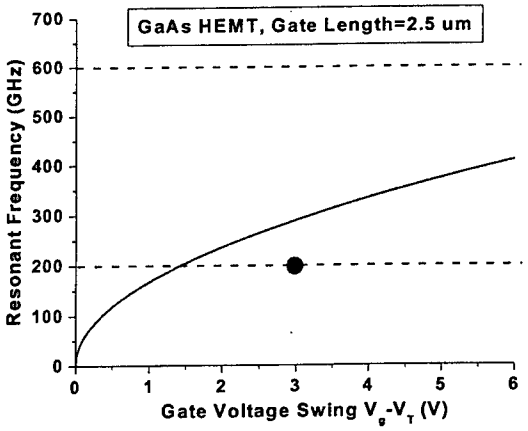


Fig. 7. (a) Resonant frequency f_0 versus U_o for GaAs HEMTs

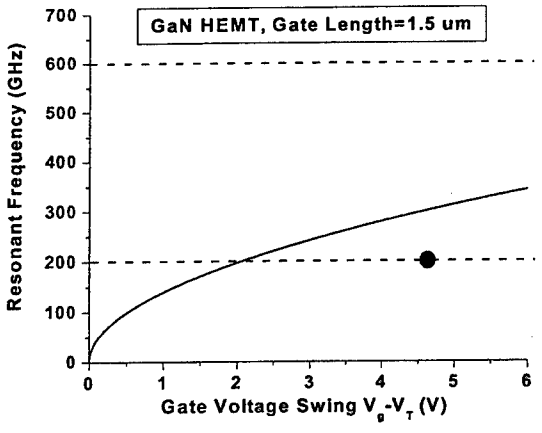


Fig. 7. (b) Resonant frequency f_0 versus U_o for GaN HEMTs

As shown in Fig.8, no response peaks at positive gate bias were observed at room temperature. Only the small non-resonant response (nearly 10 times smaller than that at 8K in Fig. 3 a) for negative gate bias close to the threshold voltage was observed. This decrease can be related to the decrease of the electron mobility (momentum relaxation time) at higher temperatures due to increased polar optical phonon scattering. However, our calculations using the theory developed in [3] indicate that the

change of the electron mobility from 8,000 $cm^2/V\text{-}s$ to 2,000 $cm^2/V\text{-}s$ could only explain the decrease in response on order of factor of 2.

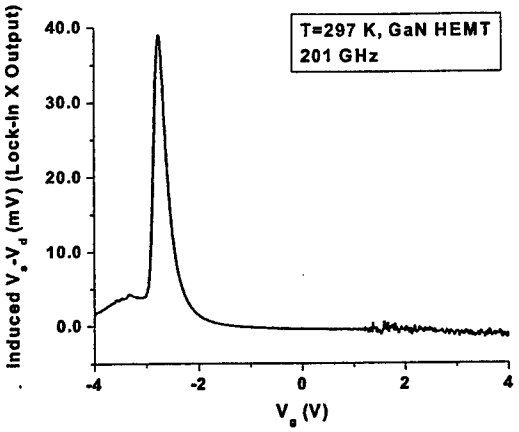


Fig. 8. 201 GHz radiation response of GaN HEMT at room temperature

III. Conclusion

We presented experimental investigations of the plasma wave detector responsivity at 200GHz and 600GHz radiation for long channel AlGaAs/GaAs and AlGaN/GaN based HEMTs at 8K and 300K. The enhancement of the responsivity at high positive gate bias was observed. We found that this enhancement, in both types of the devices, is correlated with the increase of the gate current under the forward gate bias. These results can be explained on the basis of the new theoretical model in which the plasma self-excitation can appear under condition of the high gate current.

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Acknowledgments

The authors gratefully acknowledge the DARPA support of (project monitors, Dr. Edgar Martinez and Dr. Dwight Woolard). The authors also thank Dr. A. Sereika for his help in our experiments.

Compact Circuit Model of GaN HFETs for Mixed Signal Circuits

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Abstract

This work presents a comprehensive compact circuit model of GaN HFETs for mixed signal applications. Self-heating and trapping effects are included in the model. Model parameters can be determined by fitting measured data, or estimated analytically based on geometrical dimensions and layer structure. Good agreement has been found with measured characteristics from DC to RF.

Introduction

GaN-based HFETs offer a unique combination of high current density with large breakdown voltage, making them attractive for a variety of microwave and mm-wave power applications. High performance mixed-signal circuits capable of handling large analog voltages may also be possible with scaled GaN HFET structures. For comprehensive circuit simulation, accurate models are needed. Models should describe self-heating behavior, since with the high power density of GaN, thermal management is an important issue. Also, models should include the trapping effects present in many GaN HFETs, to alert the designer about the possible consequences of trapping for circuit behavior. Modeling of AlGaN/GaN HFETs including self-heating and trapping effects is the subject of this work.

Model

The compact circuit model is based on the BSIM3v3.3 MOSFET model with subcircuit elements added to represent the Schottky gate, gate resistance, parasitic inductances and capacitances, self-heating and transient phenomena as shown in figure 1. BSIM3 was chosen as the base model for this work because it is physically based, scalable, and includes short channel effects and velocity saturation. The BSIM3 model, however, contains a multitude of parameters, many of which do not have physical significance in an HFET; accordingly, the parameter set was reduced from 128 to 24 parameters.

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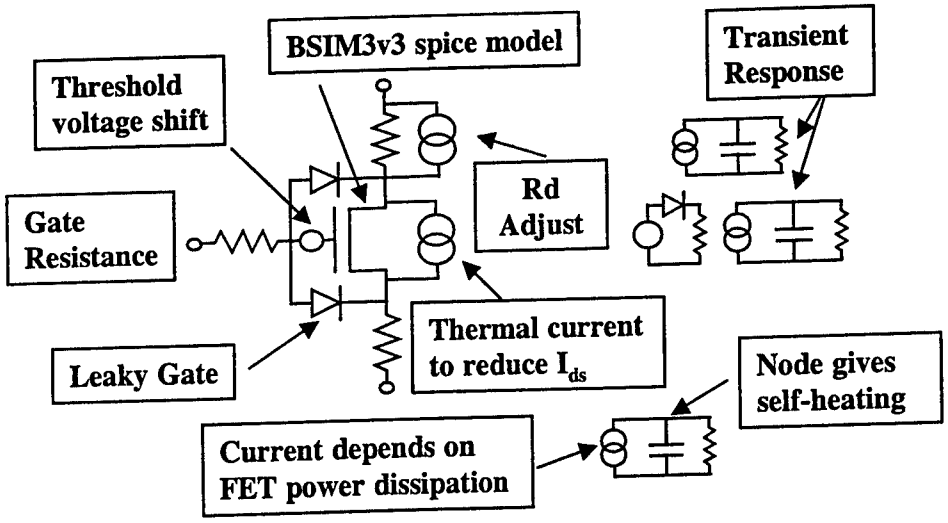


Figure 1. Model Schematic

A spreadsheet was developed to estimate model parameters including the parasitics, from the device geometry and layer structure. A self-heating subcircuit was added, which calculates the power dissipated in the device and the corresponding temperature increase at a given bias condition. The increase in temperature leads to a decrease in drain current due to a reduction of mobility from phonon scattering. This is represented in the model as a dependent current source opposing the drain source current. Transient effects including gate lag and drain lag are also represented as subcircuits. Gate lag is modeled as a threshold voltage shift dependent on the history of the transistor bias. Drain lag is represented by an increase in drain resistance and a threshold voltage shift. The model was compared with a suite of DC and RF measurements on HFETs fabricated with MBE material, on substrates of sapphire and SiC. Figures 2, 3, 4, and 5 show a representative comparison of measured and modeled results.

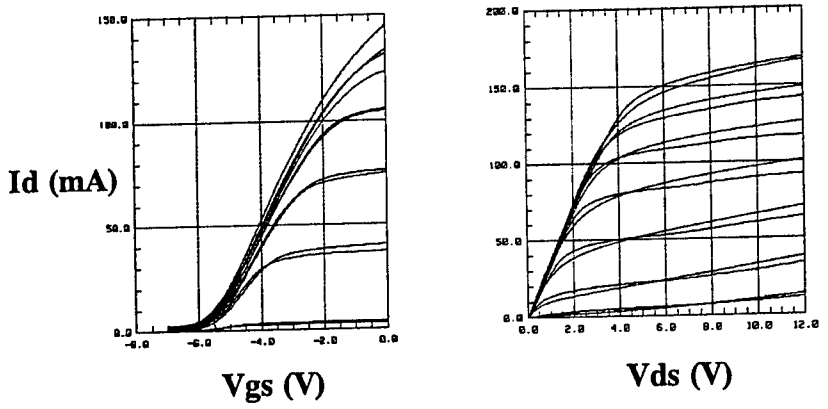


Figure 2. DC current vs. voltage curves for a 0.25 um by 200um device on a SiC substrate, measured and modeled.

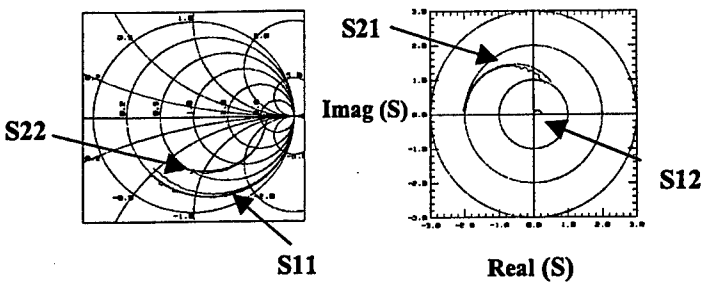


Figure 3. S-parameter data, measured vs. modeled from 0.5 to 26.5 GHz.

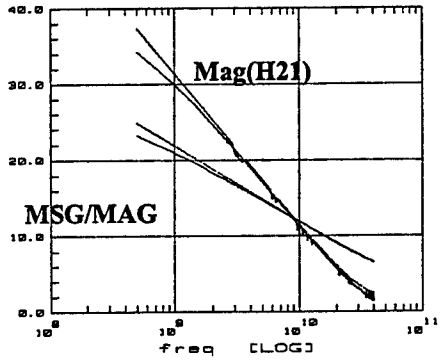


Figure 4. Comparison of mag(H21) and MSG/MAG vs. frequency for model and measurement.

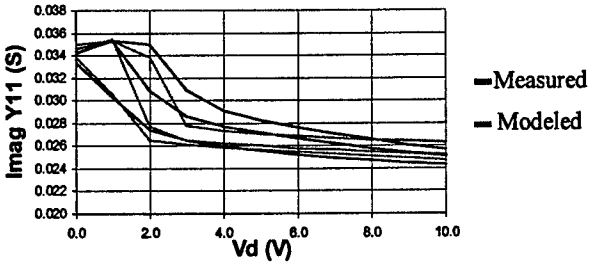


Figure 5. Imag Y11 vs. bias at 5 GHz for GaN HFET on SiC substrate.

Self Heating

Self-heating is an important issue for GaN based transistors due to the high power densities the devices are capable of handling. To model the temperature rise caused by power dissipation and thus the drop in drain current, the thermal resistance of the layer structure must be determined. The approach taken in this work was to use a three - dimensional thermal simulator to model the device and also to measure the thermal resistance using a novel electrical technique. In the simulations, thermal conductivities of 0.48 °C/W, 3.5°C/W and 1.7°C/W were used for sapphire, SiC and GaN respectively. The simulations were performed for varying gate dimension for devices on both sapphire and SiC substrates as shown in figure 6.

To corroborate the simulations, measurement of the thermal resistance was desired. This was accomplished using the ac conductance technique[3]. The premise behind this technique is to compare the DC current – voltage characteristics with the current voltage curves of the device without self-heating. This is accomplished by measuring s-parameters over the entire bias range of the DC I-V curve. Then converting the s-parameters to y-parameters and integrating the real part of y22, one can reconstruct the I-V curves as shown in figure 7. Next the relationship between the decrease in current and the increase in

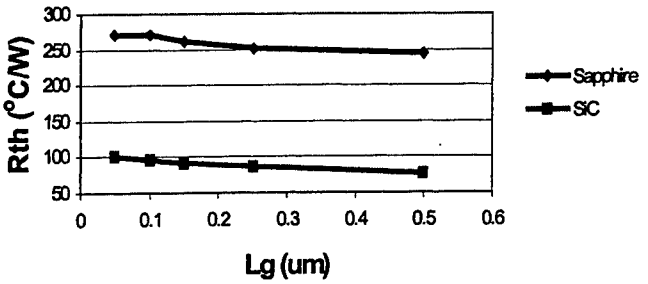


Figure 6. Simulated thermal resistance vs. gate length.

temperature needs to be determined. This was accomplished by measuring the low voltage I-V characteristics vs. temperature as shown in figure 8. By relating the ratio of the dc drain current to the reconstructed drain current to the temperature dependence of current, the temperature at a given power level can be estimated. By plotting temperature versus power dissipated, the thermal resistance can be extracted. The thermal resistance calculated for this technique is 15% lower than the simulation. Some of this difference may be accounted for by the absence of metalization in the simulation, which would act as a heat sink.

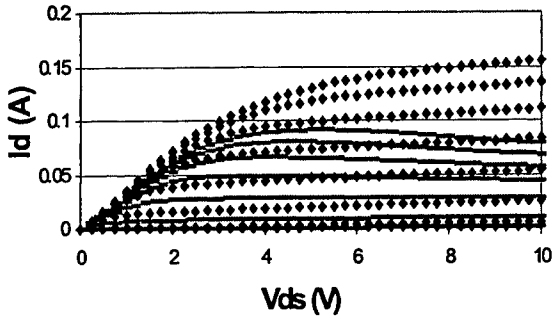


Figure 7. Reconstructed I-V cures, with and without self-heating for a 0.25 um by 100um device on sapphire.

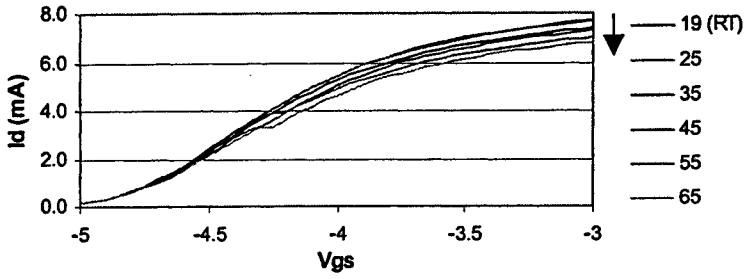


Figure 8. Low drain voltage I -V curves vs. increasing temperature.

Transient Effects

To accurately predict the output characteristics of AlGaN/GaN HFETs, the response to pulsed excitation must be considered. Anomalous transients are commonly observed known as gate lag and drain lag, in accordance with the terminal to which the pulse is applied. Charging and discharging of surface states, traps in the AlGaN layer and traps in the GaN buffer can cause changes in the I-V characteristics related to the time scale of the measurement, as shown in the data of figure 9; they are accounted for in the model by a history dependent threshold voltage shift. Similarly, charging and discharging of traps at the surface and in the AlGaN layer between the gate and the drain can cause an increase in series resistance. Such an effect is accounted for in the model with a history dependent current nonlinear source.

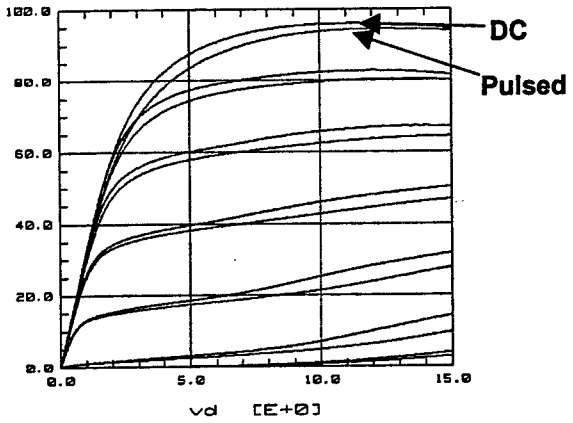


Figure 9. DC and pulsed I vs. V curves for a gate pulse of period 10ms and pulse width 0.5ms.

Conclusion

A model has been developed for AlGaN/GaN HFETs by adapting the BSIM3v3 MOSFET model with subciruits to include self-heating and the effects of traps in the device. The thermal resistance was modeled, measured and added as a subcircuit. The effects of pulsed excitation, in the form of gate lag and drain lag, were also included as subcircuits in the model. The model accurately represents device characteristics from DC to RF over a wide bias range.

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Acknowledgements

This work was sponsored in part by SPAWAR/DARPA contract # N66001-01-C-8028, entitled "Application of GaN HFET Technology for Advanced Mixed Signal Circuits".

Comparison Between Si-LDMOS and GaN-Based Microwave Power Transistors

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Abstract

We present in this paper a performance comparison between Si-LDMOSTs with an optimized structure for high breakdown voltage, and AlGaN/GaN power HFETs, based on DC-IV, small-signal and RF power measurement results.

I. Introduction

The large and rapidly growing market for wireless telecommunication has a great need for low cost, high performance microwave solutions. Both GaN-based and Si-LDMOS transistors are of great interest because they offer high power capabilities at RF frequencies.

AlGaN/GaN HFETs offer important advantages for high power applications [1,2]: the high saturated electron velocity of the GaN material combined with an hetero-structure design enables devices to operate at microwave frequencies, also, the devices high breakdown voltage resulting from the GaN wide-bandgap makes high voltage operations possible, and the high output impedances of GaN-based FETs is beneficial for wide bandwidth power amplifiers. The use of this technology will ultimately result in reduced circuit complexity, improved linearity, gain, efficiency, and reliability. However parasitic effects like self-heating, floating-body and trapping still reduce the device performance and reliability [3-6]. In addition integrating these parasitic effects in nonlinear models is crucial for accurate device simulation, but lead to more complex modeling procedures.

On the other hand Si-based technologies benefit from the past extensive work done in micro-electronic, leading to reliable and low cost technology for RF applications. However, because of the Si intrinsic material properties, the typical breakdown voltage in Si MOSFET is in the few V range, and frequency of operation above a few Ghz requires a drastic reduction of the gate length leading to new parastic effects such as short channel effects. New Si-LDMOS device concepts allow the breakdown voltage to be above 80V while maintaining good frequency performance, opening the door of high power and high frequency operation to bulk-Si technology. Also, ultimately such devices could be integrated in conventional Si-CMOS process.

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We present in this paper a performance comparison of Si-LDMOSTs and AlGaN/GaN HFETs based on DC-IV, small-signal and RF power measurement results. The studied AlGaN/GaN HFETs are 2-finger devices grown on a SiC substrate, with a total gate width (W_G) of 250μm, and a gate length (L_G) of 0.35μm. The measured Si LDMOSTs exhibit a 850μm gate width and a channel length of 0.3μm.

II. Studied Devices

A. AlGaN/GaN HFET

The AlGaN/GaN HFETs used in this investigation are provided by and Cree, N.C. They are 2-finger devices grown on a SiC substrate, with a total gate width (W_G) of 250μm, and a gate length (L_G) of 0.35μm. Fig.1a and Fig.1b show a photograph and a cross section of the device structure, respectively.

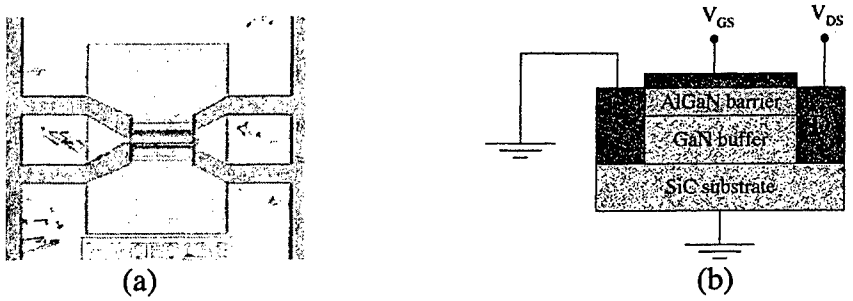


FIG.1: (A) Photograph of a 2-finger AlGaN/GaN HFET. (B)AlGaN/GaN HFET layer structure.

B. Si LDMOST

The (lateral double-diffused) LDMOS structure in this work is schematically shown in Fig.2. A double RESURF (REduced SURface Field) structure of the drift region has increased the breakdown voltage to around 90V, resulting in a large increase in output power density, compared to the commercial available Si LDMOS devices that are conventionally biased around 25V. Detailed information about the device structure can be found in [7]. The device measured has a gate width of 850μm, a gate length of 1.5μm, and a channel length of 0.30μm [8].

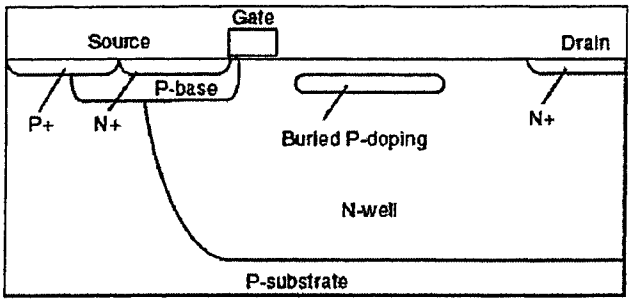


FIG. 2: Schematic cross-section of the LDMOS transistor showing the buried p-doping.

III. Measurement Results

A. DC-IV Characteristics

Fig.3a and Fig.3b show the drain-to-source current characteristics of a Si LDMOST, and an AlGaN/GaN HFET, respectively.

The breakdown voltage is in the 80V range for both device technologies, enabling high drain-to-source voltage operation beneficial for high power applications. A peak transconductance of 52mS/mm is extracted in the Si-based devices whereas it reaches 200mS/mm in the GaN-based FETs. This result will translate into higher cutoff frequency (f_T) and higher RF-gain for the GaN-based devices. Finally, the drain-to-source current saturation (I_{DSS}) is measured to be in the 800mA/mm for the AlGaN/GaN HFET, while it is around 160mA/mm in the measured Si-LDMOST, resulting in higher device power performances for the GaN based devices.

Also, it is noteworthy that the current characteristics of the AlGaN/GaN HFETs exhibits a kink at low V_{DS} and a negative slope under high bias conditions. The first parasitic effect is attributed to deep trap levels in the GaN buffer, and is commonly referred to as current collapse. Using a device with such a kink in the IV characteristics would increase the harmonic generation under large signal conditions when the load trajectory traverses this region. Also, this kink leads to more complex nonlinear current modeling necessary for accurate device simulation, where the load trajectory traverses the linear region [9]. Improvement in the buffer crystal structure would reduce this effect. The second effect is due to the excess of power that cannot be dissipated in the device, and is referred to as self-heating. This affects the device RF power performance and the device reliability [10]. Improving the device design from a thermal and efficiency point of view would reduce this effect. Both parasitic effects are not present when performing measurement under pulsed mode of operation, and none of them appear in the current characteristics of the measured Si-LDMOS transistors, traducing a more mature technology.

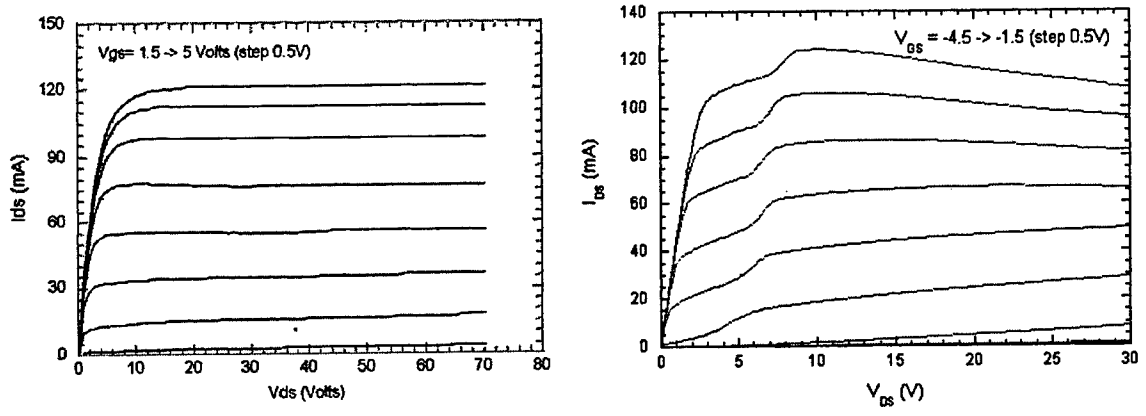


FIG.3: (A)S i LDMOST (W_g=850μm) drain-to-source current characteristics. (B)AlGaN/GaN HFET (W_g=250μm) drain-to-source current characteristics.

B. Small-Signal Characteristics

The cutoff frequency (f_T) of the devices is extracted from small-signal measurements. Fig.4 illustrates the short circuit current gain for both devices. f_Ts of 2.3GHz and 31GHz are extracted for Si LDMOST and AlGaN/GaN HFET, respectively. Very high frequency of operation can be achieved when using GaN-based devices, making these transistors more versatile than Si LDMOSTs. This result confirms the higher frequency performance of GaN-based devices obtained from the DC-transconductances.

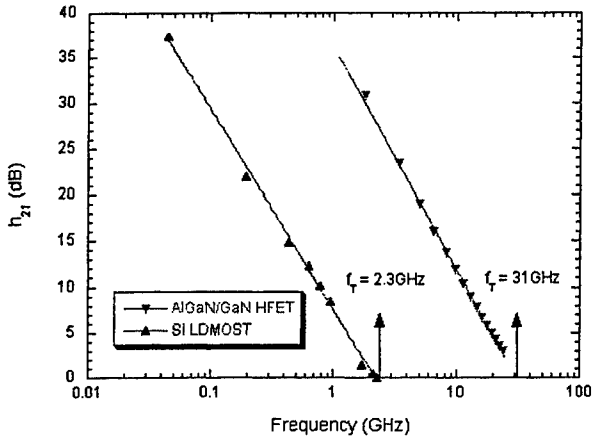


FIG. 4: AlGaN/GaN HFET and Si LDMOST short circuit current gain.

C. Large-Signal Characteristics

Finally, Fig.5a and Fig.5b present RF power measurement results of Si-based and GaN-based devices. Si LDMOSTs exhibit a power density in saturation of 1.4W/mm and a peak power added efficiency (PAE) of 51% at 1GHz, while the AlGaN/GaN HFETs present a 4W/mm power density with a peak PAE of 27% at 8GHz. power densities above 10W/mm have been recently reported for AlGAN/GaN HFET in the X-band [11]

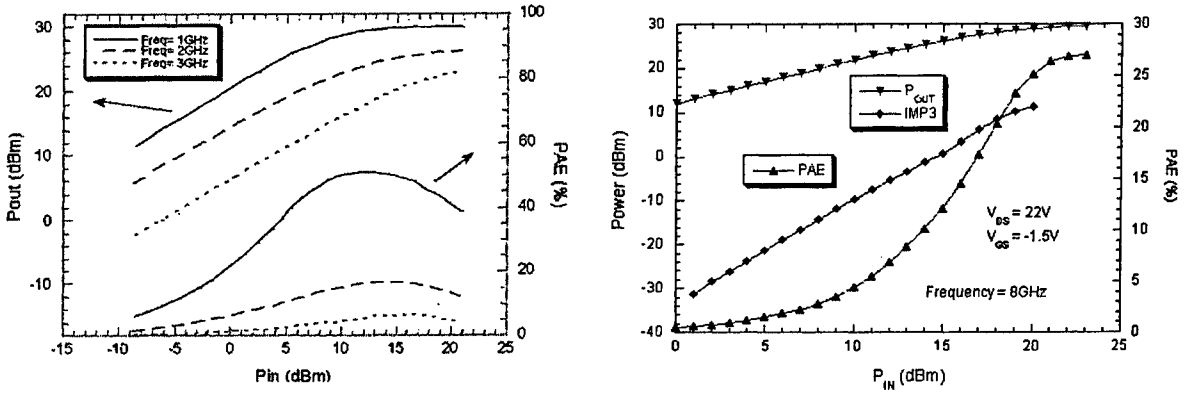


FIG. 5: (A)Si LDMOST (W_g = 850mm) output power and power added efficiency versus input power tuned for maximum output power at three different frequencies 1, 2 and 3 GHz (V_{DS}= 50V, V_{GS}= 1.5V). (B)Power results of an AlGaN/GaN HEMT with W_G=250μm at 8GHz, and at (V_{DS} = 22V; V_{GS} = 1.5V).

Finally, Fig.5a illustrates the degradation of the power characteristics in Si LDMOSTs when increasing the frequency of operation, and the linearity of the AlGaN/GaN HFETs is presented through 3rd order intermodulation measurement results in Fig.5b.

IV. Conclusion

GaN-based transistors exhibit high power capabilities at high frequency of operations but the technology still suffer from parasitic effects like self-heating, and trapping, limiting the reliability, and the reproducibility of the devices. On the other hand Si-LDMOSTs offer advantages in terms of thermal stability, and process maturity, but lack the frequency bandwidth.

Acknowledgments

The authors wish to acknowledge J. Zolper from the Office of Naval Research, CREE Inc. for providing the devices, and J. Milligan and W. Pribble from CREE Inc. for their support. The authors are grateful to the clean-room staff at Mitel Semiconductor AB for processing the Si LDMOSTs.

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Design of GaN/AlGaN HEMT Class-E Power Amplifier Considering Trapping and Thermal Effects

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Abstract

A microwave class-E power amplifier using AlGaN/GaN HEMT as the switching device is reported by incorporating trapping and thermal effects in the large-signal device model. The load network of the class-E amplifier is designed by considering more realistic exponential decay of the drain current during fall time and finite quality factor of the resonant circuit to incorporate the nonidealities of the active device and passive components. With 9V supply voltage, calculated output power and power conversion efficiency are 89mW and 58% at 1GHz which decrease to 84mW and 54% at 3.8GHz, respectively for a GaN/$Al_{0.30}Ga_{0.70}N$ HEMT with gate width of 50μm.

Introduction

Class-E amplifiers [1-3] are suitable for nonlinear modulation schemes used by cellular and cordless standards like GSM and DECT and are popular for their higher power conversion efficiencies. Using GaAs MESFETs as the active device, Sowlati *et al.* [2] have reported a class-E amplifier with power added efficiency (PAE) of 50%, output power of 250mW at a supply voltage of 2.5 V at 835 MHz. Tsai *et al.* [3] have demonstrated operation of a class-E amplifier up to 1.9 GHz using 0.35 μm CMOS technology with PAE of 48% at a supply voltage of 2 V.

In recent years, GaN based HEMTs are pursued extensively for applications in high power microwave amplifiers operating at high temperature. GaN with a band gap of 3.4eV has a breakdown field of 2MV/cm. With SiC as the substrate, GaN offers an overall thermal conductivity of 4.5 W/cm-K allowing the devices to be operated at elevated temperatures as high as 750C reported by Daumiller *et al.* [4]. Eastman [5] has demonstrated an output power density of 11.7 W/mm at 10GHz with a 0.3μm × 100μm AlGaN/GaN HEMT. A low field mobility of 1500 $cm^2\ V^{-1}s^{-1}$ along with a saturation velocity of 3×10^7 cm/s allows the realization of high frequency devices as demonstrated by Lu *et al.* [6] where f_T = 101 GHz and f_{max} = 155 GHz have been reported with a 0.12μm ×100μm GaN/AlGaN HEMT. In

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class-E amplifiers, efficiency decreases at elevated frequencies due to the higher power loss in the active device that forces the driving transistor to operate at elevated temperatures. Due to superior power performances at elevated frequencies and temperatures, GaN based devices can be more suitable in class-E power amplifiers.

The superb performances of GaN based devices are hindered by the trapping effects [7]. The presence of traps in the buffer layer causes current collapse that may lead to DC to RF dispersion of transconductance and output resistance thereby degrading device performances at elevated frequencies requiring device models to incorporate the trapping effects for accurate analysis of RF/analog circuits [8]. In our previous effort [1], we have reported a GaN-based class-E amplifier operating up to 11GHz neglecting the trapping effects in the large-signal device model. In this paper, a class-E power amplifier using AlGaN/GaN HEMT as the switching device is reported for possible applications in microwave and wireless circuits by incorporating trapping effects in the large-signal device model.

Analysis

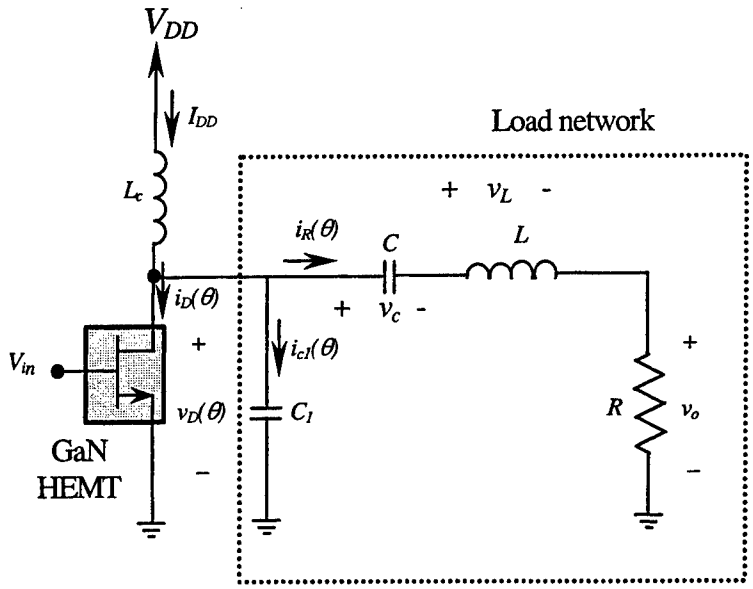


Fig.1. Basic class-E power amplifier circuit.

Fig.1 shows the basic class-E power amplifier circuit. The active device operates as a switch and the load network ensures minimum switching loss. A large-signal HEMT model,

as shown in Fig.2, is used to realize the functional dependence of drain current upon applied gate and drain voltages. In Fig. 3, the dashed curve shows the measured *I-V* characteristics [7]. The negative slope of the modeled AC *I-V* characteristics, as shown in Fig. 3, is due to thermal effects. Surface traps located at the surface in the region between gate and drain were passivated by a layer of Si_3N_4. Current collapse and subsequent recovery at high drain bias have been correlated to the trapping and detrapping of carriers by the trapping centers located in the buffer layer [7]. Current collapse is dependent upon the applied signal frequency and causes the device transconductance and output resistance measured at DC to decrease significantly at RF [8]. Using drain-lag measurement data for AlGaN/GaN HEMTs, we have estimated detrapping time constants to be 58.42 seconds and 1.55 seconds that correspond to trap states located at 0.79eV and 0.69eV below the bottom of the conduction band, respectively. At room temperature, the transconductance and output resistance dispersion frequencies are less than 1Hz due to the trap levels mentioned above. However, with increasing temperature the dispersion frequencies increase and can be of the order of MHz at 600K. For applied signal frequencies greater than the output resistance and transconductance dispersion frequencies, traps are unable to respond and recovery of collapsed drain current is not possible. This necessitates the determination of the model parameters from the AC *I-V* characteristics as shown by the solid lines in Fig. 3. The AC drain current as function drain-source and gate-source voltages are given by,

$$I_{ds} = \left[f_o(V_{gs}) + f_1(V_{gs})V_{ds} + f_2(V_{gs})V_{ds}^2 + f_3(V_{gs})V_{ds}^3\right]\tanh\left[f_\alpha(V_{gs})V_{ds}\right] \tag{1}$$

where

$$f_\alpha(V_{gs}) = a_{\alpha o} + a_{\alpha 1}V_{gs} + a_{\alpha 2}V_{gs}^2 + a_{\alpha 3}V_{gs}^3, \tag{2}$$

$$f_i(V_{gs}) = a_{io} + a_{i1}V_{gs} + a_{i2}V_{gs}^2 + a_{i3}V_{gs}^3, \quad i = 0,\ldots,3, \tag{3}$$

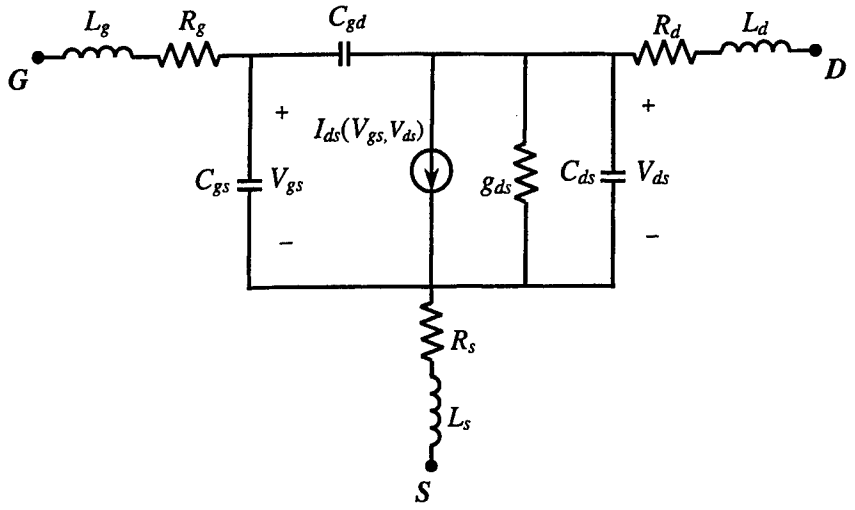
the constants a's are given in Table 1. The intrinsic model parameters are given by,

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}} \tag{4}$$

$$g_{ds} = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}} \tag{5}$$

$$C_{gs,gd} = C_{gs0,gd0}\left(1 - \frac{V_{gs,gd}}{V_{bi}}\right)^{-\frac{1}{2}} \tag{6}$$

where, $C_{gs0,\ gd0}$ are zero-bias gate-source and gate-drain capacitances and V_{bi} is the built-in potential. The rest of the model parameters are obtained from reported experimental data [9,10] that are listed in Fig.2.



R_g	L_g	R_s	L_s	C_{ds}	R_d	L_d
0.5 Ω	0.09 nH	0.7 Ω	0.1 nH	0.44 pF/mm	0.5 Ω	0.07 nH

Fig.2. Equivalent circuit model of the GaN HEMT.

Table 1: Coefficients used in eqns. (2) - (3) defining GaN/$Al_{0.30}Ga_{0.70}N$ HEMT (width is 50μm, I_{ds} in milliamperes and V_{ds} and V_{gs} are in Volts) [7].

i	a_{i0}	a_{i1}	a_{i2}	a_{i3}
0	72.75	53.25	15.61	1.89
1	–6.51	–6.44	–1.64	–0.08
2	0.34	0.26	0.01	–0.01
3	–0.006	–0.002	0.002	0.0006
α	0.236	–0.270	–0.185	–0.090

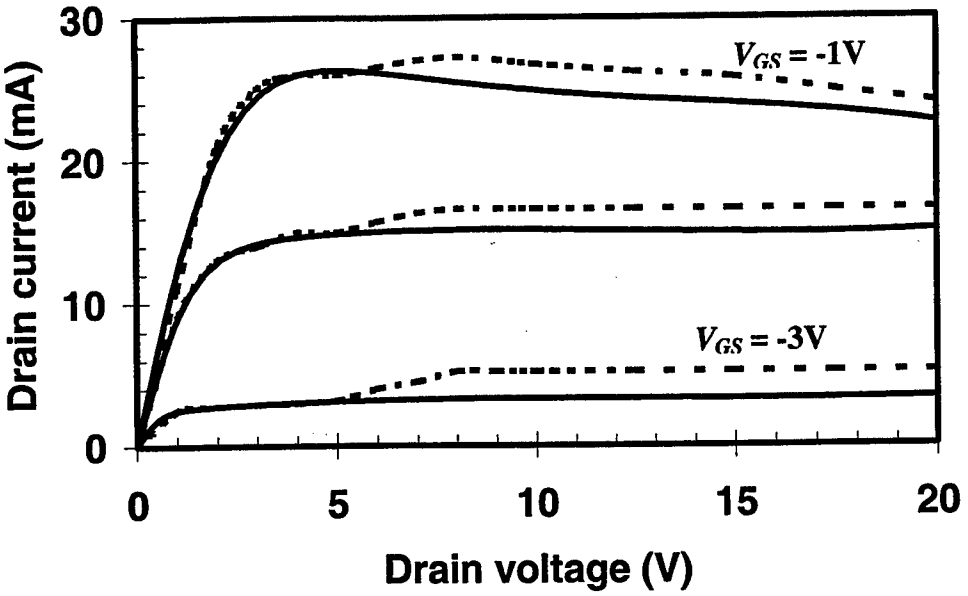


Fig.3. Simulated AC *I-V* characteristics of a GaN/AlGaN HEMT of 50μm gate width (solid lines). Experimental results are shown by dashed lines (DC *I-V*).

In the present analysis, the load network is designed by considering finite loaded quality factor of the inductor and exponential decay of the drain current during fall time. The load network components are as follows [1]:

$$C_1 = \frac{P_{out}\sin\phi\left[2+\frac{\pi^2}{2}+\pi\tan\phi+2\tau^2\left(1-e^{-\frac{t_f}{\tau}}\right)-2\tau\theta_f e^{-\frac{t_f}{\tau}}\right]^2}{2\pi\omega V_{dd}{}^2 k_1}, \tag{7}$$

$$R = \frac{k_1\sin\phi}{\pi\omega C_1}, \tag{8}$$

$$L = \frac{Q_L R}{\omega}, \tag{9}$$

and

$$C = \frac{1}{\omega^2\left(L-\frac{k_2\sin\phi}{\pi\omega^2 C_1}\right)}. \tag{10}$$

Here,

$$k_1 = \left[2\sin\phi + \cos\phi(4\omega\tau - \pi) - 2\cos\phi\cot\phi - 2\omega\tau e^{-\frac{t_f}{\tau}}\{\cos\phi + \cos(\theta_f + \phi)\} + \right.$$
$$\left. \frac{2\omega^3\tau^3}{1+\omega^2\tau^2}\left\{\cos\phi - \cos(\theta_f + \phi)e^{-\frac{t_f}{\tau}} - \frac{1}{\omega\tau}\sin(\theta_f + \phi)e^{-\frac{t_f}{\tau}} + \frac{1}{\omega\tau}\sin\phi\right\}\right], \quad (11)$$

$$k_2 = \left[\frac{\pi}{2\sin\phi} - (4\omega\tau - \pi)\sin\phi - 2\omega\tau e^{-\frac{t_f}{\tau}}\{\sin\phi + \sin(\theta_f + \phi)\} + \right.$$
$$\left. \frac{2\omega^3\tau^3}{1+\omega^2\tau^2}\left\{\sin\phi - \sin(\theta_f + \phi)e^{-\frac{t_f}{\tau}} + \frac{1}{\omega\tau}\cos(\theta_f + \phi)e^{-\frac{t_f}{\tau}} - \frac{1}{\omega\tau}\cos\phi\right\}\right], \quad (12)$$

$\theta_f = \omega\, t_f$ is the drain current fall angle, ϕ is the initial phase angle of the load current with respect to the load voltage at operating frequency ω, τ is the decay lifetime, P_{out} is the output power and Q_L is the loaded quality factor. ϕ is calculated by solving-

$$\frac{1}{\sin\phi} + \frac{\pi + \omega\tau\left(e^{-\frac{t_f}{\tau}} - 1\right)}{2\cos\phi + \omega\tau\sin\phi\left(e^{-\frac{t_f}{\tau}} - 1\right)} = 0, \quad (13)$$

which is obtained by applying the optimal switching conditions, namely, $v_D = 0$ and $dv_D(\omega t)/d(\omega t) = 0$ at $\omega t = 2\pi$ to the drain current and voltage equations.

Results and Discussion

The GaN/$Al_{0.30}Ga_{0.70}N$ HEMT reported by Binari *et al.* [7] is used to calculate the power and frequency performances of the class-E amplifier. The gate width is 50μm. The load network parameters are calculated considering a loaded quality factor of 10 and decay lifetime τ of the order of nanoseconds [1]. Fig.4 shows the calculated output power and efficiency of the class-E amplifier as a function of DC supply voltage at 3.8GHz that corresponds to the frequency at which peak pulsed power density of 6.7W/mm is reported [7]. Here, input signal has rectangular waveform which can be generated using a class-F driver [2]. As observed, with increasing DC supply voltage output power increases. Efficiency initially increases and eventually saturates due to the increase in DC power dissipation in the device. With a supply voltage of 9V, calculated output power of the class-E amplifier is 84mW and the power conversion efficiency is 54%. A similar variation in output power and efficiency was observed in the class-E power amplifier designed with GaAs MESFETs [2]. As GaN based devices are suitable for high voltage operation, higher output

power can be obtained for given device dimensions using higher supply voltage. Besides, transient analysis shows that the drain voltage can be as high as 20V which can be sustained by the GaN HEMT without causing breakdown. As reported by Binari *et al.* [7], the application of a drain bias exceeding 20V caused current collapse in subsequent *I-V* measurements which necessities the incorporation of current collapse in the device model.

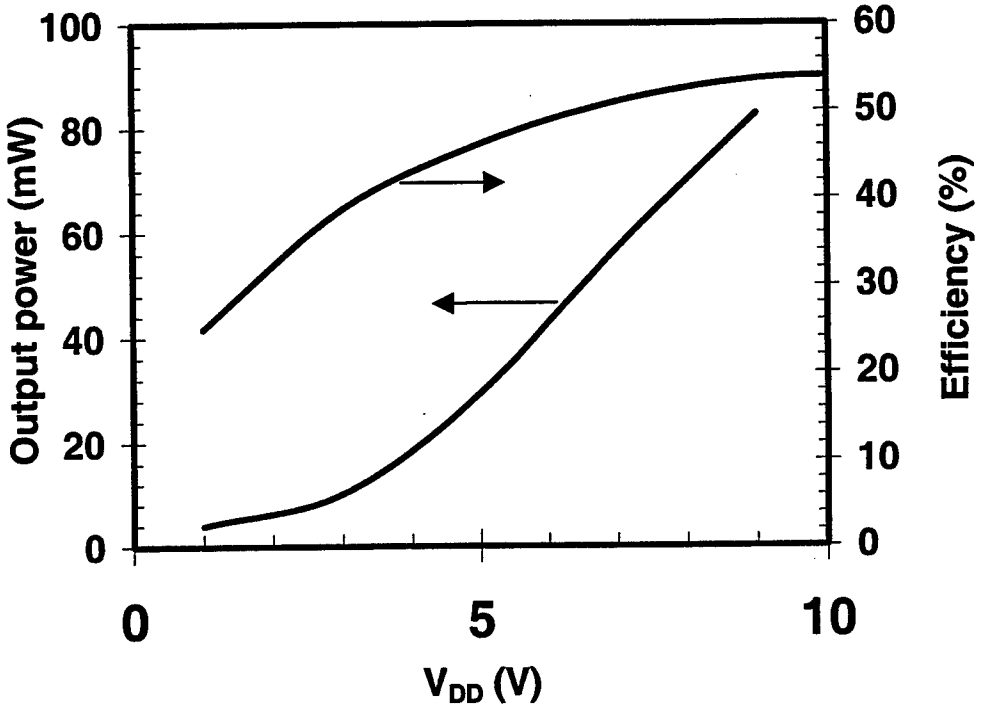


Fig.4. Calculated output power and efficiency as a function of DC supply voltage at 3.8GHz.

Output power and efficiency as a function of operating frequency are shown in Fig.5. Here supply voltage is 9V. At 1GHz, calculated efficiency and output power are 58% and 89mW, respectively. Output power and efficiency decrease monotonically with increasing frequency due to higher power loss at elevated frequencies [1].

To further investigate the effect of traps on the power performance of class-E amplifiers, simulations were carried out without accounting for current collapse in the device model. In the absence of current collapse, at 1GHz and with 9V supply voltage, output power increased to 114mW and efficiency increased to 60%. Similar results were obtained for output power and efficiency at elevated frequencies.

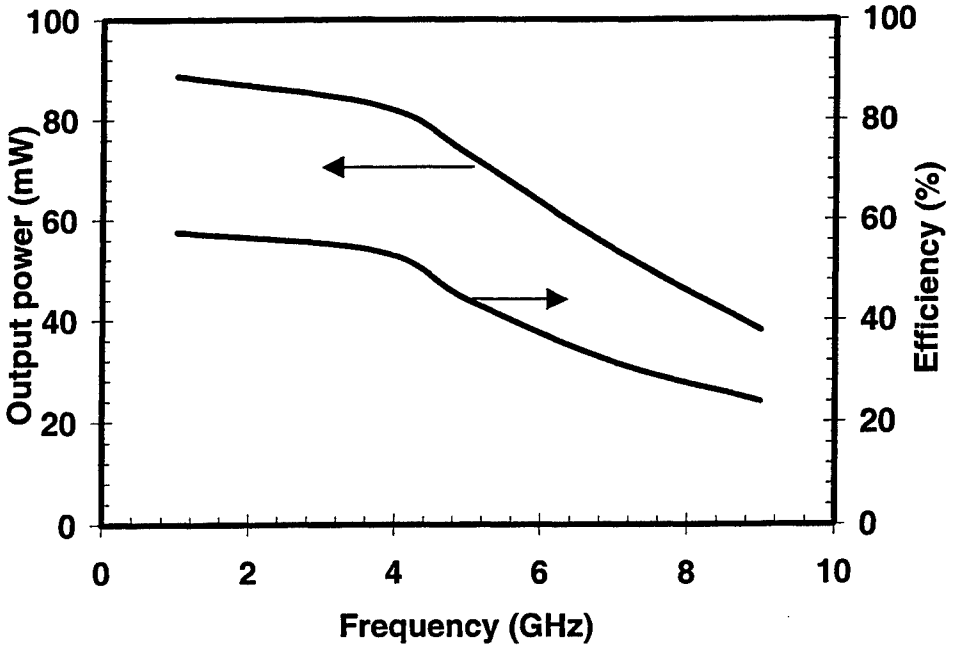


Fig.5. Calculated output power and efficiency as a function of frequency at 9V supply voltage.

Conclusions

A class-E power amplifier with AlGaN/GaN HEMT as the active device is reported. The large-signal model used in the simulation incorporates current collapse and DC to RF dispersions of transconductance and output resistance. A significant increase in operating frequency and efficiency of class-E power amplifier is obtained with GaN HEMT as the active device compared to that was reported with Si CMOS or GaAs MESFETs. Output power is significantly overestimated when current collapse is neglected in the device model.

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Low Frequency Noise in $Al_{0.4}Ga_{0.6}N$ Thin Films

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ABSTRACT

Low-frequency noise in $Al_{0.4}GaN_{0.6}$ thin films (50 nm) was measured at room and elevated temperatures as function of gate and drain voltages. Both $1/f$ noise and generation-recombination (g-r) noise were observed. Hooge parameter, α, was estimated to be about 7. The activation energy for observed g-r noise was found to be $E_a \sim 1.0$ eV. This activation energy is consistent with the activation energy observed for g-r noise in AlGaN/GaN HFETs.

I. INTRODUCTION

Group-III Nitride Heterostructure Filed Effect Transistors (HFETs) have demonstrated impressive results in high frequency and high power electronics. These HFETs, metal-oxide HFETs (MOSHFETs) and metal-insulator HFETs (MISHFETs) have employed AlGaN layers with different Al molar fractions [1,2,3].

Low frequency noise (LFN) is one of the most important characteristics of FETs, which determines the suitability of devices for microwave communication systems. The LFN properties of GaN layers and AlGaN HFETs have been studied in numerous papers [4,5,6,7]. Therefore the study of low frequency noise in AlGaN films is important for establishing the location of the noise sources in these devices.

In this paper, we present experimental data on the low-frequency noise ($1/f$ and generation-recombination noise) in thin Si-doped n-type AlGaN films and compare the results with the results of low frequency noise studies for AlGaN/GaN HFETs

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II. EXPERIMENTAL DETAILS

$Al_{0.4}Ga_{0.6}N$ thin films were grown at 1000 °C and 76 torr by low pressure Metal Organic Chemical Vapor Deposition (MOCVD) on sapphire substrate. A 50 nm AlN buffer layer was followed by the deposition of a 1 μm insulating AlGaN layer and a 50 nm n-AlGaN layer with the doping level of 5×10^{18} cm^{-3}. The measured room temperature Hall mobility was 100 cm^2/Vs. We used e-beam deposited Ti/Al/Ti/Au (100 Å /300 Å /200 Å /1000 Å) layers for ohmic contacts. These contacts were annealed at 850 °C for 60 s using Rapid Thermal Annealing (RTA) in nitrogen ambient. Helium ion implantation was used to isolate devices.

Low-frequency noise was measured in the frequency range from 1 Hz to 100 kHz in the temperature interval from 300 K to 550 K. The voltage fluctuations were measured using the Transmission Line Model structures (TLMs) with 200 μm width and distance, *L*, between the TLM pads ranging from 2μm to 20μm. The probe station with the tungsten probes of 10-μm diameter and controlled pressure on the probes provided contacts to the sample pads.

III. RESULTS AND DISCUSSION

In order to find thickness and doping level of the $Al_{0.4}Ga_{0.6}N$ layers the capacitance - voltage measurements were performed at frequencies from 1 kHz to 10KHz on the test Schottky diodes with the area of 4×10^{-4} cm^2. Fig.1 shows the doping profile extracted from measurements at two frequencies. Those values are in agreement with the estimated values from growth parameters.

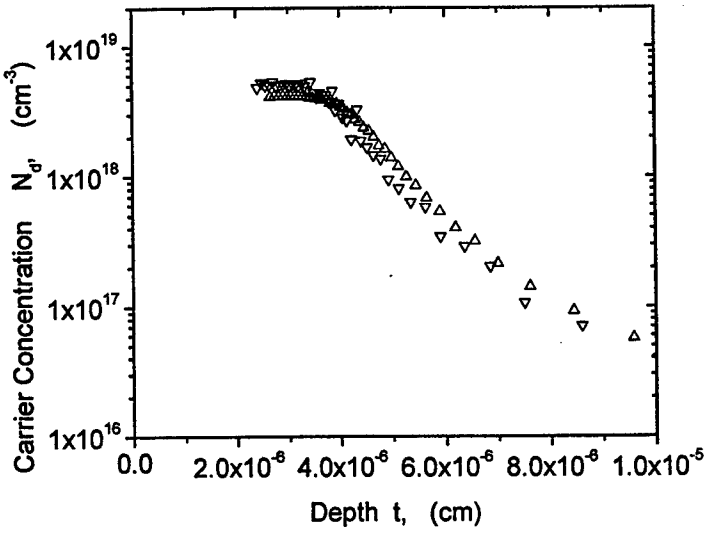


Fig. 1. Doping profile extracted from capacitance-voltage measurements at 10 and 100kHz.

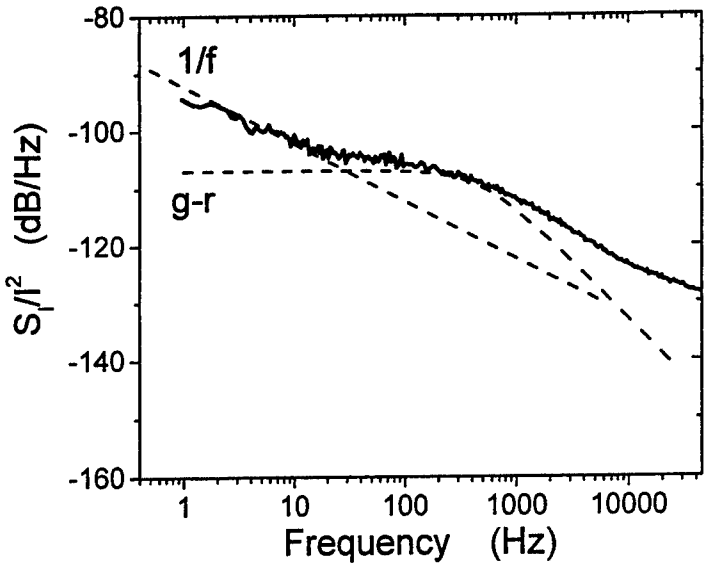


Fig. 2. Spectral density of low frequency noise at room temperature.

Measurements of the current-voltage characteristics on the TLM structures revealed a high contact resistance R_c=250 Ωmm and sheet resistance R_s=1.5×10^{4}Ω/square. Therefore even for the biggest distance of W=20μm between pads in TLM structures the resistance of the layer was comparable with the contact resistance.

Fig. 2 shows the noise spectrum for W=20μm at room temperature. As seen, both $1/f$ noise and generation-recombination (g-r) noise were observed. The $1/f$ noise level in different semiconductor materials and structures is usually characterized by the dimensionless Hooge parameter, α [8]:

$$\alpha = \frac{S_I}{I^2} fN \qquad (1)$$

where N is the total number of the conduction electrons in the sample, f is the frequency of the analysis, S_I/I^2 is the relative spectral density of noise. Using the value of N extracted from capacitance voltage measurements, we found $\alpha \approx 7$. This value of α is several orders of magnitude larger than the one observed in thin n-GaN films and GaN based transistors. Such high values of α are usually observed in highly disordered materials, such as polycrystalline semiconductors and conducting polymers [9].

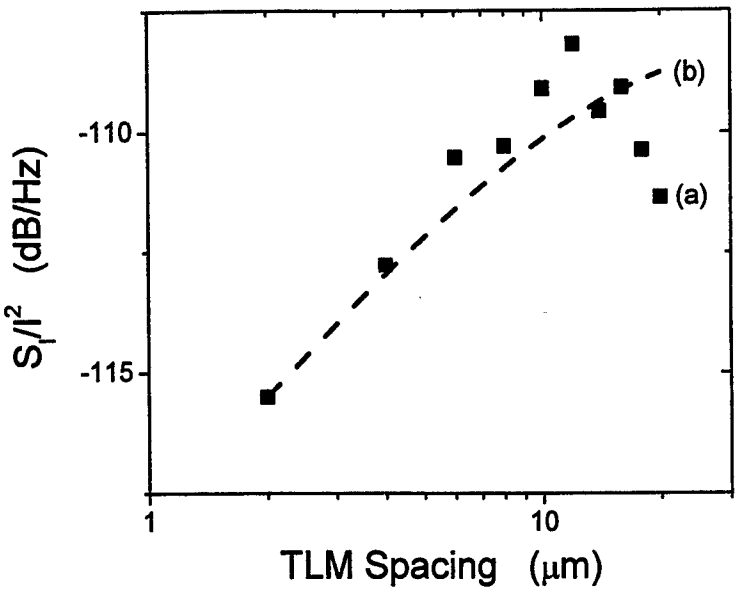


Fig. 3. The dependence of the relative spectral noise density S_I/I^2 on the distance L between the pads of TLM structure. Dots (a) represent measured data; curve (b) represents calculated noise with the assumption that the channel noise is dominant. Frequency of analysis f= 100 Hz.

Symbols in Fig.3 show experimental dependence of noise measured at frequency f=100Hz as a function of the distance between contact pads in the TLM structure.

Assuming that the noise sources are not correlated and located in the contacts and in the channel, the spectral noise density of the current fluctuations can be expressed as follows:

$$\frac{S_{Id}}{I_d^2} = \frac{S_{RAlGaN}}{R_{AlGaN}^2}\frac{R_{AlGaN}^2}{(R_{AlGaN}+R_C)^2} + \frac{S_{Rc}}{R_C{}^2}\frac{R_C{}^2}{(R_{AlGaN}+R_C)^2} \qquad (2)$$

where S_{AlGaN}, and S_{Rc} are spectral densities of channel resistance R_{AlGaN} between contact pads, and contact resistance R_C fluctuations, respectively. In Eq. (2) first and second terms give increase and decrease of the noise as function of R_{AlGaN} and represent contribution from AlGaN layer and contacts respectively. The contribution from the AlGaN layer increases with the distance L between contacts pads, while contribution from the contacts decreases with L increase.

The dashed curve in Fig.3 represents the calculated noise density using Eq. (2) and assuming only AlGaN layer as a source of noise (first term). The values of resistances were taken from the dc TLM measurements. We assumed also that in accordance with Eq. (1) (S_{AlGaN}/R^2_{AlGaN}) decreases as $1/L$.

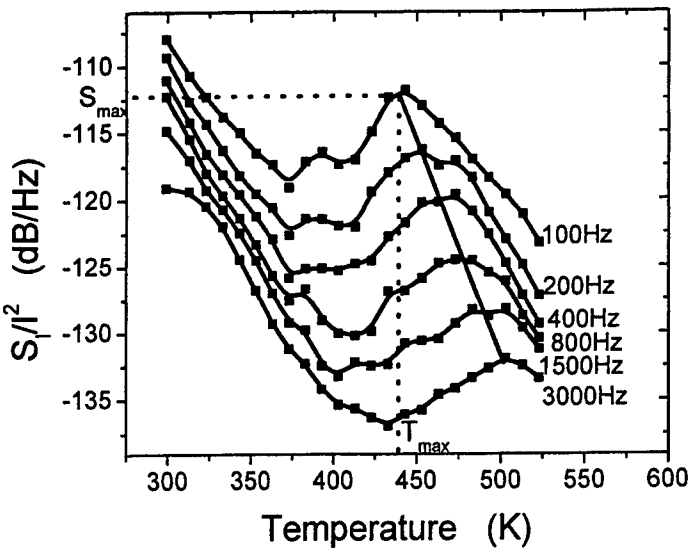


Fig. 4. Temperature dependence of low frequency noise.

Since there is qualitative agreement between measured data and the results calculations we can conclude that in spite of the large resistance contacts do not contribute much to noise.

Figure 4 shows the temperature dependence of the noise spectral density S_I/I^2 at a series of frequencies. In the temperature interval between 400 and 450K these dependences exhibit a clear maximum. The temperature T_{max} corresponding to the maximum noise increases with frequency. This dependence is typical for the generation-recombination noise caused by a local level [10,11,12]. The sharp decrease of the noise at temperatures 300-350K indicates contribution to noise from another local level.

Figure 5 shows the dependencies of $1/kT_{max}$ versus $ln\,(f)$ (the Arrhenius plots). The slope of this dependence gives the activation energy E_a=1eV. This is the same value with the one found for g-r noise in AlGaN/GaN HFETs [7]. As discussed in Ref [12] the activation energy of g-r noise is the sum of level energy position E_0 and activation energy E_1 of temperature dependence of level capture cross section. Following the procedure, described in Ref. [12] we plotted the dependence of the noise at maximum $log(S_{max})$ versus $log(f)$ and found the slope of this dependence equal to unity. This indicates that $E_1 >> E_0$. This is the most unfavorable situation for estimation of the level parameters.

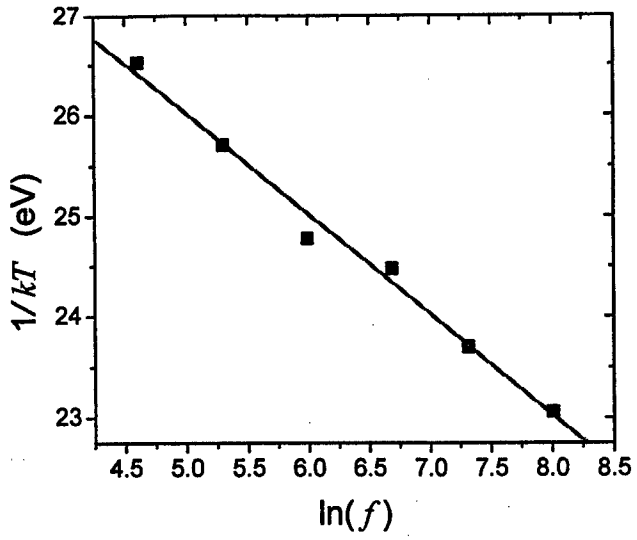


Fig. 5. Arrhenius plot for low frequency noise. Slope gives the activation energy as 1 eV.

For thin layers the contribution to noise of the surface levels might be important. Assuming a level with the concentration N_{ts} that exceeds the total concentration of all other levels at the surface and therefore determines the position of the Fermi level at the surface, we attribute the value of energy E_a to the surface level position relative to the conduction band [13]. Following the procedure described in Ref. [13], lower limit for the level concentration N_{ts} was estimated to be 3×10^{13} cm^{-2}.

IV. CONCLUSION

Low frequency noise in thin $Al_{0.4}Ga_{0.6}N$ layers was studied within the temperature range from 300 to 520K. In spite of the high contacts resistance comparable with layer resistance contacts do not contribute much to noise. Both, $1/f$ and generation recombination noise were found. Generation recombination noise with activation energy of 1 eV might be attributed to the surface level. The same activation energy was found before for g-r noise in AlGaN/GaN HFETs. This confirms the suggestion made in Ref. [7] that sources of g-r noise in AlGaN/GaN HFETs are related to AlGaN barrier layer. High value of the Hooge parameter $\alpha \approx 7$ typical for disordered materials indicates low structural perfection of the layer.

ACKNOWLEDGEMENT

The work at RPI was supported by the Office of Naval Research, and the project was monitored by J. Zolper. The work at SET, Inc. was supported by ONR under contract N00014-01-C-0195 and monitored by Y.-S. Park. The work at USC was supported by the

Ballistic Missile Defense Organization (BMDO) under Army SMDC contract DASG60-98-1-0004, monitored by Dr. Brian Strickland and Dr. Kepi Wu.

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ADVANCED LARGE-SIGNAL MODELING OF GaN-HEMTs

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Abstract

For improved non-linear modeling of AlGaN/GaN high electron mobility transistors, a large-signal model originally developed for GaAs-based devices has been extended by introduction of a thermal sub-circuit to account for self-heating. Thereby, DC output characteristics which typically show negative output conductance at a high dissipating power level are well reproduced. Since self-heating also effects the transconductance, which is related to S_{21} at RF conditions, the comparison of broadband S-parameter simulations and measurements revealed significant improvement when using the extended model. First experimental and theoretical investigations on the transient behavior at pulsed conditions are finally presented.

I. Introduction

In recent years, AlGaN/GaN high electron mobility transistors (HEMTs) have been developed and investigated in detail due to the high potential of this materials system for high power, high frequency and high temperature electronics (see, e.g., [1]). It is expected that for many applications, e.g. base-station amplifiers or radar, nitride-based transistors and circuitry play an important role in the near future. Power amplifier and circuit design requires adequate modeling of the transistor behavior at its various operating conditions such as DC, cw-RF and pulsed mode. Under each operating condition, the responding behavior of the transistor is differently influenced by thermal effects introduced by poor thermal conductivity of the adjacent substrate. This in particular shows up when sapphire having a thermal conductivity of 0.4 W/cmK is used as a substrate instead of SiC (4.5 W/cmK). The SiC substrate appears to be the substrate of choice (moreover due to better lattice constants match), however, its significantly higher price might prevent from use for mass products. Therefore, consideration of substrate-induced thermal effects is required for comprehensive modeling of the transistor (note that although in use of SiC substrates thermal effects appear at high dissipating power levels [2]). In nitride-based HEMTs, beside thermal effects, trap-related dispersion may also give rise to discrepancies between static and dynamic characteristics [3]. So far, to the best of our knowledge, papers reporting on large-signal modeling of AlGaN/GaN-HEMTs are scarce [4, 5]. This paper presents non-linear modeling

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results obtained by an extension of an existing large-signal model [6-8] to account for self-heating effects. Simulations are compared with DC and broadband S-parameter measurements for validation purposes. Finally, first experimental investigations under pulsed stimulus are presented and discussed in regard to further verification of the improved model.

II. Theoretical description of the large-signal model

As a starting point for GaN HEMT modeling including self-heating, the analytical large-signal transistor model developed for GaAs HEMTs [6-8] has been chosen because of its simple model equations yet excellent non-linear modelling capabilities. This original model was implemented as a user-defined model in Agilent Advanced Design System (ADS) and has already been applied for AlGaN/GaN-HEMTs. Although dynamic output characteristics were used for the parameter extraction, the first attempt shows the necessity of the self-heating correction [9]. The original large-signal equivalent circuit is divided into two parts – the internal transistor with its non-linear elements and the parasitic network. The parameters of the parasitic network are determined from "Cold" S-parameter measurements [10]. For the internal transistor, a drain current source and two current sources representing the gate current as well as two non-linear capacitances are used to model its non-linear behavior.

According to Wei et al. [11], the large-signal equivalent circuit is extended by an additional thermal sub-circuit (see Figure 1). The thermal sub-circuit consists of the parallel connection of the current source, i_{th}, the thermal resistance, R_{th}, and the thermal capacitance, C_{th}, which describe the self-heating-related decrease of the current. In the simulation procedure, both the thermal sub-circuit and the transistor equivalent circuit are jointly considered.

As follows, the basic model equations are summarized:

The thermal current source represents dissipating power in the device

$$i_{th} = I_{ds}\, V_{dsi} \tag{1}$$

and the voltage drop on the thermal resistance gives the channel temperature rise

$$\Delta T = R_{th} i_{th} = R_{th}\, I_{ds}\, V_{dsi}\,. \tag{2}$$

This channel temperature rise ΔT leading to the drain current decrease at high dissipated power level gives an additional term (f_4) in the basic drain current source equation:

$$I_{ds}\left(V_{gsi}, V_{dsi}\right) = f_1\left(V_{gsi}\right)\cdot f_2\left(V_{gsi}, V_{dsi}\right)\cdot f_3\left(V_{dsi}\right)\cdot f_4\left(\Delta T\right) \tag{3}$$

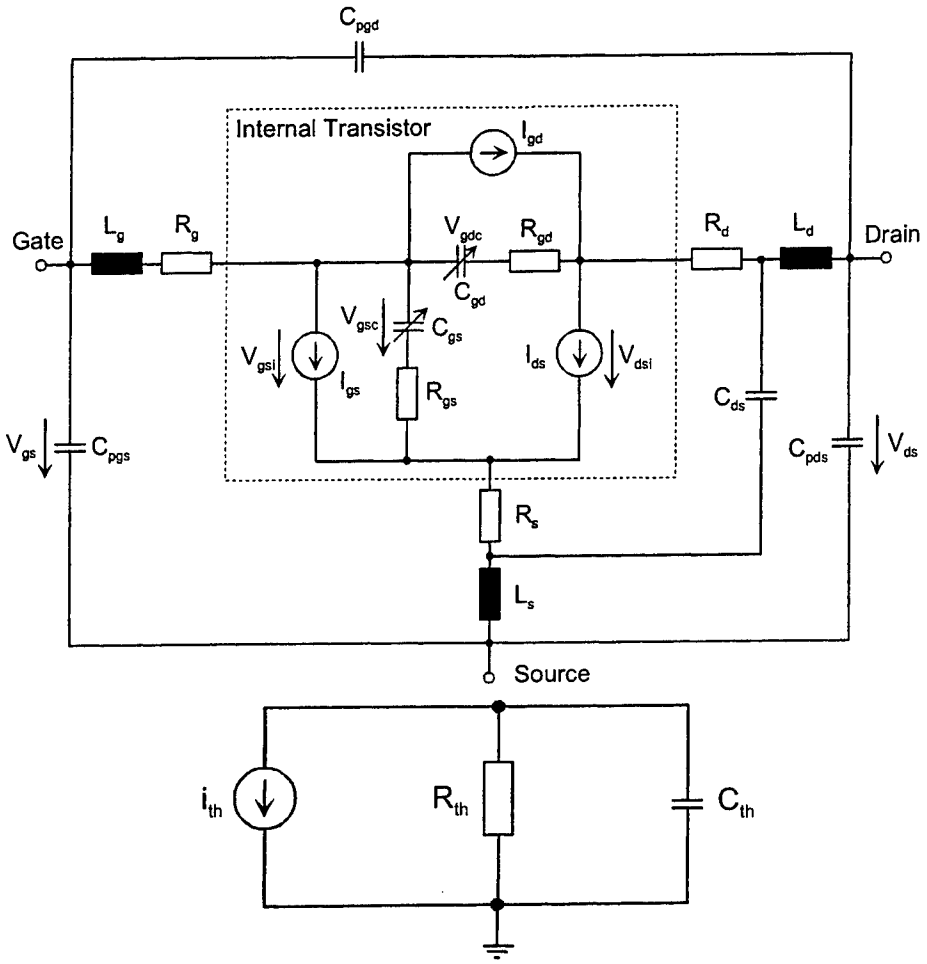


Figure 1: Large-signal equivalent circuit of the GaN HEMT with thermal sub-circuit

$$f_4(\Delta T) = 1 - \kappa \frac{\Delta T}{T_0} \tag{4}$$

where T_0 is the ambient temperature; κ parameter.

The basic terms of the original model are

$$f_1\left(V_{gsi}\right) = CD_{vc} \cdot \left(1 + \tanh\left[\beta \cdot \left(V_{gsi} - V_c\right) + \gamma \cdot \left(V_{gsi} - V_c\right)^3\right]\right) + CD_{vsb} \cdot \left(1 + \tanh\left[\delta \cdot \left(V_{gsi} - V_{sb}\right)\right]\right) \quad , \qquad (5)$$

$$f_2\left(V_{gsi}, V_{dsi}\right) = 1 + \frac{\lambda}{1 + \Delta_\lambda \cdot \left(V_{gsi} - V_{to}\right)^2} \cdot V_{dsi}, \quad \text{with} \quad V_{to} = V_c - \frac{2}{\beta}, \qquad (6)$$

and

$$f_3\left(V_{dsi}\right) = \tanh\left(\alpha \cdot V_{dsi}\right), \quad \text{with} \quad \alpha = \frac{\alpha_0}{1 + K V_{gs}} \quad . \qquad (7)$$

f_1 describes the transfer behavior of the transistor, f_2 models the RF output conductance and f_3 the triode region.

The part of the original model responsible for the triode region of the transistor output characteristics (f_3) is also modified by an additional parameter K to include the dependence of the slope on the gate voltage.

Note that the low-pass characteristic of the thermal sub-circuit reflects the frequency dependence of the self-heating (i.e., current reduction). It means that the transition to high frequency stimulus, where self-heating cannot follow anymore, is considered. For transient behavior, the respective time constant is

$$\tau = R_{th} C_{th} \quad . \qquad (8)$$

III. Experiment

The transistor structures were grown by metal organic vapor phase epitaxy on sapphire substrate and consisted of a AlN-nucleation / GaN-buffer / Al(0.24)Ga(0.76)N-barrier / GaN-cap layer sequence (5 nm/1,6 µm/24 nm/3 nm) (Figure 2). A composition of Ti/Al/Au (20 nm/120 nm/200 nm) is used for the ohmic contacts, which has been alloyed at 870 °C for 45 s by RTA. The gate consists of a standard Ni/Au (100 nm/150 nm) Schottky diode without any temperature treatment after the metalization process. The herein presented

results have been obtained from a device with a gate length and width of 1,5 μm and 2×100 μm, respectively. Standard bias-dependent broad-band S-parameter measurements up to 40 GHz have been performed at room temperature. For pulsed measurements, a LeCroy LC 584A digital oscilloscope has been used.

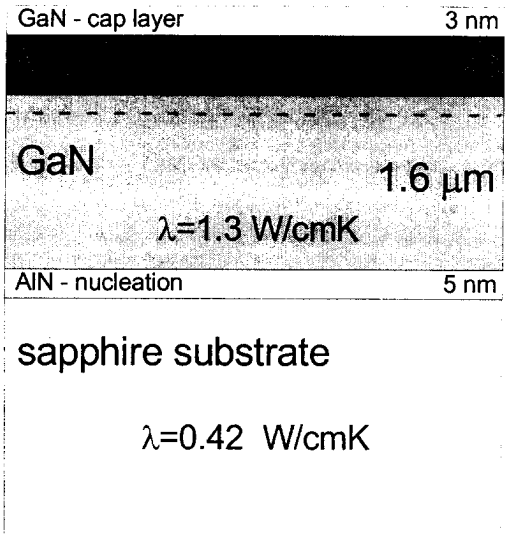


Figure 2: Sketch of a typical AlGaN/GaN/sapphire-substrate-HEMT structure indicating thermal properties

IV. Results

Figure 3 depicts measured and simulated DC output characteristics of the HEMT. Experimentally, a negative output conductance is clearly observed at increased dissipating power (i.e. at increased $I_{ds}V_{ds}$) as a direct consequence of the elevated channel temperature. Simulations by the original model (Figure 3a.) do not allow to reproduce the negative slope. Instead, by applying the improved model equations described in section II, a very good agreement of measured and simulated characteristics has been achieved. The average error of 5% validates the improved approach.

Respective advances have been achieved in S-parameter simulations including the thermal sub-circuit as shown in Figure 4. For S_{21}, discrepancies of measured and simulated data at low frequencies which arise due to self-heating-related reduction of the transconduction have been overcome in the improved approach. Here, the average errors of measured and simulated S-parameters of about 10% are satisfactorily low.

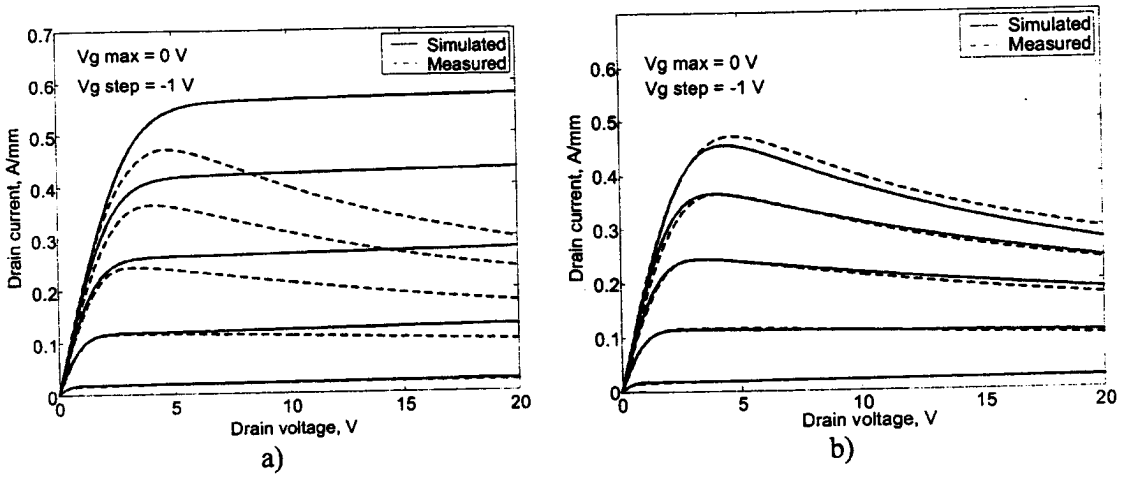


Figure 3: Measured and simulated output characteristics using the large-signal model without (a) and with (b) thermal effect

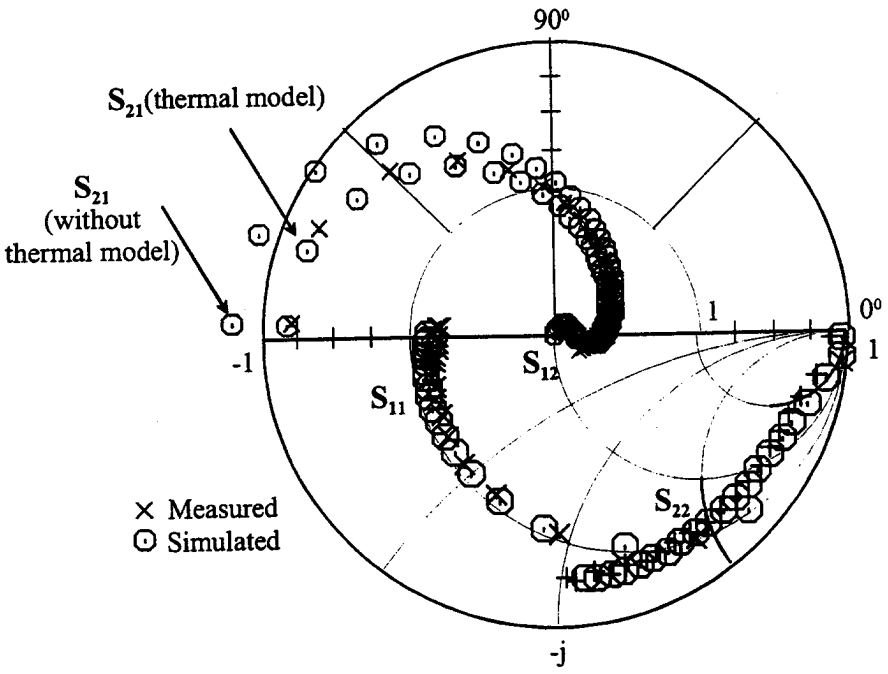
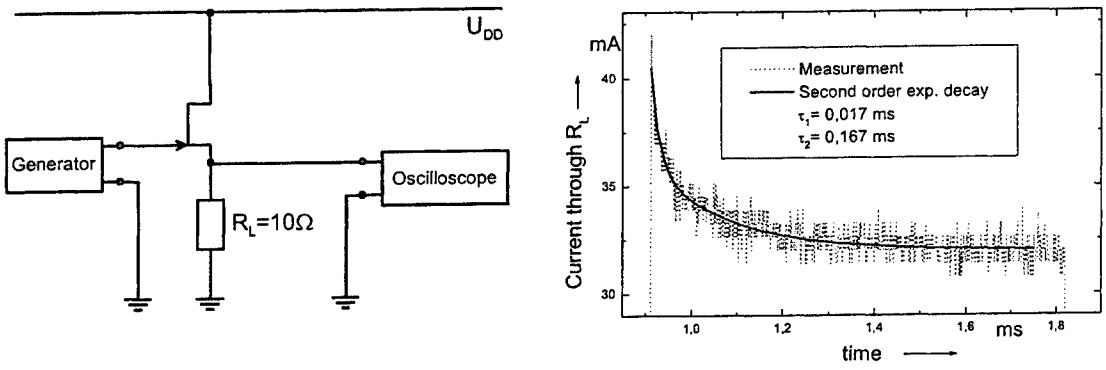


Figure 4: Measured and simulated S-parameters (S_{21} simulated without thermal effect is also shown).

The improved model has finally been examined for predictions of the transient behavior under pulsed stimulus. For this, rectangular shaped gate-source-voltage-pulses from pinch-off (-8 V) to open-channel condition (0 V) at a 0.55 kHz repetition rate have been applied at constant drain-source-voltage. The voltage drop over a R_L = 10 Ω resistance, connected to the source, was measured. Connection of the resistor in the source line of the transistor (Figure 5a) instead of connection in the drain line was used in order to simplify the measurement technique (no differential measurements were necessary). We note that the respective current through R_L is therefore not the drain-current, but the sum of drain-current and gate-current. Since the transient time of the gate-current is much smaller than the thermal transient time (ps vs. ms), the influence of the gate-current is negligible. Detailed inspection of the experimental traces shows that two thermal time constants govern the fall of the drain current (Figure 5b). This is explained by the layered structure of the device where the layers of dominant thickness (2 µm GaN buffer and 500 µm sapphire substrate) have various thermal conductivities (see Figure 2). This explanation is sustained by similar investigations which have been published recently [12].



a) b)

Figure 5: Experimental setup (a) and drain-current transient at pulsed stimulus (V_{gs} from –8 V to 0 V at constant V_{ds} = 20 V), including second order exponential decay fitting (b)

V. Conclusion

An adequate extension of a large-signal model to account for self-heating related deterioration of the transistor behavior has been presented. Both DC and S-parameter simulations compare very well with experimental data, thus validating that the advanced model is capable to comprehensively describe the transistor behavior under such conditions. By using the improved model, experimental results obtained under pulsed conditions have

additionally been compared to simulations. It turned out that two different time constants, most likely originating from the different thermal conductivities of the GaN buffer layer and the sapphire substrate, govern the transient behavior of the device. A second pair of thermal resistance and capacitance has to be connected to the thermal sub-circuit, to reflect two measured time constants. The advanced large-signal model will sufficiently provide improved predictions of broadband amplifier performance and nitride-based circuit design.

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Microwave Power SiC MESFETs and GaN HEMTs

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ABSTRACT

We have fabricated SiC MESFETs with more than 60 watts of output power at 450 MHz from single 21.6mm gate periphery devices (2.9 W/mm) and 27 watts of output power at 3 GHz from single 14.4mm SiC MESFET devices (1.9 W/mm). We have also demonstrated more than 6.7 W/mm CW power from 400 μm GaN/AlGaN HEMT devices for X band (10 GHz) applications. These excellent device performances have been attributed to the improved substrate and epitaxial films quality, optimized device thermal management, and enhanced device fabrication technologies. The substrates and epitaxial films from different sources were compared and some showed significant less SiC substrate micropipes confirmed by X-ray topography and epitaxial defects characterized by optical defect mapping.

INTRODUCTION

Wide bandgap semiconductors, SiC and GaN, have been viewed as highly promising for microwave power generation at UHF, L/S and X bands [1]. The advantages of wide bandgap materials over the conventional Si and GaAs include high breakdown field, high saturation electron velocity, and high thermal conductivity. For SiC Metal Semiconductor Field Effect Transistors (MESFETs), 250 μm-periphery devices have demonstrated a record power density of 5.6 W/mm at 3 GHz [2]. GaN/AlGaN High Electron Mobility Transistors (HEMTs) can offer even higher power performance due to the higher carrier sheet density and saturation velocity of 2DEG compared to SiC, and record power density of 10 W/mm has been demonstrated from 50μm or 150 μm gate periphery devices [3-4]. With the increased device gate periphery, the power performance will be degraded due to the significant device self-heating and trapping effects. The largest SiC MESFETs were 48 mm gate periphery with 80 watts CW power (1.67 W/mm) at 3GHz [2]. For SiC MESFETs operated at lower frequencies, small gate periphery devices were reported [5-6], but no large gate periphery devices have been reported for UHF band applications.

DEVICE FABRICATION

The SiC MESFET process starts with epitaxial SiC layers grown on either semi-insulating or conductive 4H-SiC substrates. The fabrication process includes mesa isolation, ion implantation for source/drain, ohmic metal sputtering and annealing, recess gate etching, overlay metals, e-beam patterned T-shaped gate with 0.5 μm footprint, airbridge crossovers, and backside vias (not applied yet). The devices were fabricated in house at General Electric global research center. The 14.4mm and 21.6 mm gate periphery devices normally have more than 50% yield. The completed device with airbridges is shown in Fig. 1.

The GaN/AlGaN HEMTs process starts with epitaxial GaN and AlGaN layers grown on 4H-

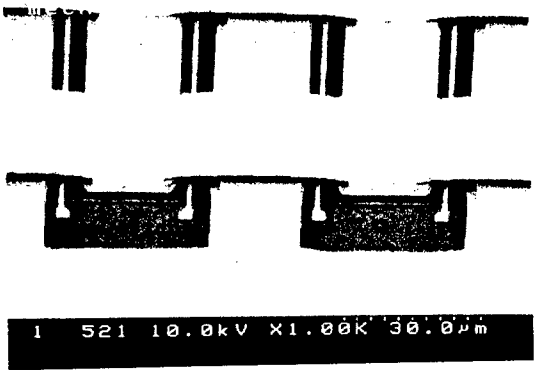


Fig. 1 SiC MESFETs with completed airbridges.

SiC semi-insulating substrates. The fabrication process includes mesa isolation, ohmic metal evaporation and annealing, overlay metals, e-beam patterned T-gate with 0.2~0.3 μm footprint, SiNx surface passivation, airbridge crossovers, and backside vias (not applied yet). The GaN/AlGaN HEMT devices were fabricated in house at General Electric global research center as well.

3-DIMENSIONAL THERMAL SIMULATIONS

For the microwave power devices made from wide bandgap semiconductor materials, the output power can be 5X to 10X more than the conventional microwave power devices made from Si or GaAs. Although SiC substrates offer a thermal conductivity of 4 W/cm·K compared to 1.5 W/cm·K of Si and 0.5 W/cm·K of GaAs, the potentials of device performance will be significantly compromised if the heat dissipation is not properly managed. Wide bandgap semiconductor materials are able to operate at higher temperatures; however, the drain current will be significantly lowered at high temperatures as shown in Fig. 2. For both SiC MESFETs and GaN/AlGaN HEMTs, the full channel current at 300 °C is only about 55% of that at room temperature mainly due to the electron mobility reduction at higher temperatures. To lower

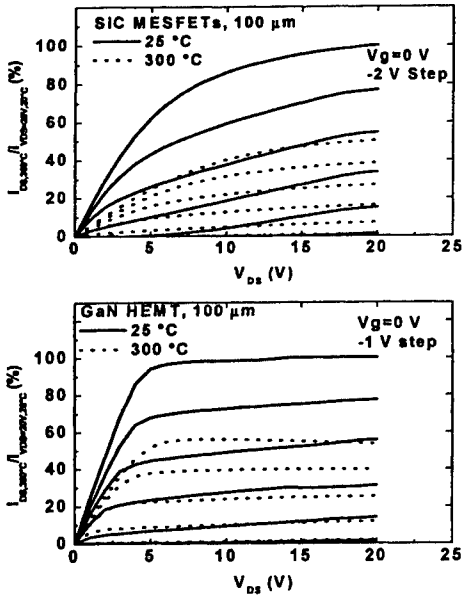


Fig. 2 High temperature DC performance of SiC MESFETs (top) and GaN HEMTs (bottom)

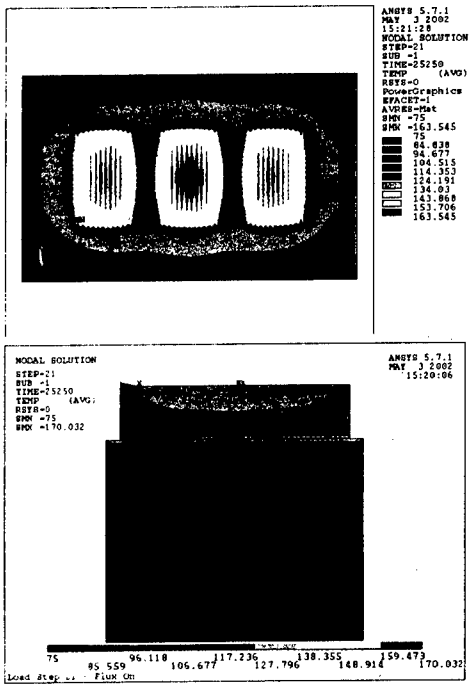


Fig. 3 Three-dimensional thermal simulations: top view (top) and cross-sectional view (bottom).

the junction temperatures, we have developed a 3-dimensional thermal simulation model to optimize the device gate layout designs. Different device gate layouts and package layer buildups were simulated. One example of the simulation results is shown in Fig. 3. The junction temperatures of optimized devices could be lowered by 50~100 °C with negligent phase delays.

SiC MESFETs POWER RESULTS

SiC MESFETs for UHF band applications use either conductive or semi-insulating 4H-SiC substrates. The 21.6 mm gate periphery devices typically have more than 50% yield. The devices were DC screened on-wafer and then diced for packaging. The packaged dies were tested at 450 MHz without matching networks. The power performance from 21.6 mm gate periphery devices is shown in Fig. 4. The devices delivered about 62 watts output power with 1% duty cycle and 250 μs pulse width. This is the highest output power reported for single SiC MESFETs at UHF band. The typical power added efficiency (PAE) was

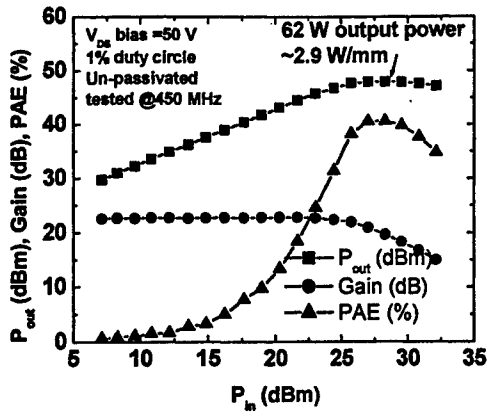


Fig. 4 Power performance of SiC MESFETs at UHF band.

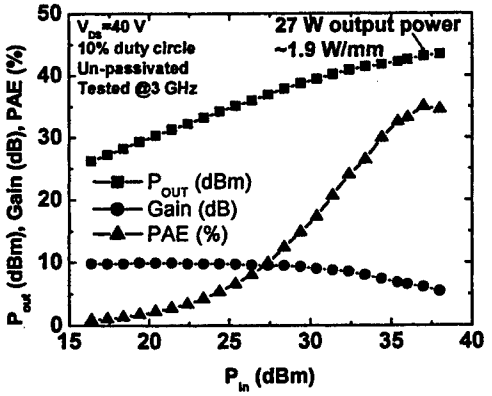


Fig. 5 Power performance of SiC MESFETs at L/S band.

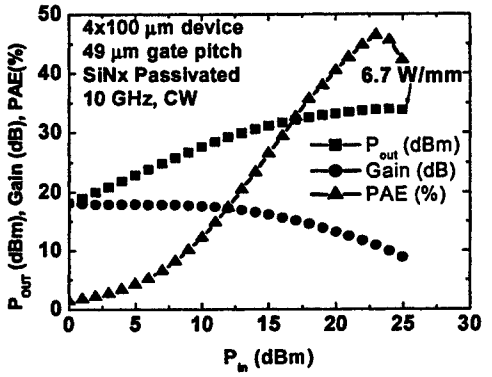


Fig. 6 Power performance of GaN/AlGaN HEMTs at X band.

~40%. The gain was high due to the use of semi insulating substrates. The devices were not passivated and still have the current dispersion effect that will be dealt with later. From the small signal S-parameter measurements, the typical values for frequency response using semi-insulating substrates was ft=7 GHz and fmax=25 GHz and ft=2 GHz and fmax=8 GHz for using conductive substrates (n-type).

Another application window for SiC MESFETs is at L/S band. The devices were fabricated on semi-insulating substrates. The large gate periphery devices were screened on-wafer for DC characteristics using the automated tester. The devices then were diced and packaged. These devices were tested at 3 GHz without matching networks. One typical device power performance is shown in Fig. 5. The device gate periphery was 14.4mm and tested with 10% duty cycle and 250 µs pulsed width at 40 volts drain bias. The total output power was 27 watts which translates to a power density of 1.9 W/mm From the small-signal S-parameters, the values for frequency response were ft=15 GHz and fmax=30 GHz.

GaN/AlGaN HEMTs POWER RESULTS

Due to the superior electron transport properties, such as high mobility, high electrical field and high saturation velocity, GaN/AlGaN high electron mobility transistors (HEMTs) have been the choice for higher frequencies (10 GHz and above) microwave power applications. The unavailability of large bulk GaN crystals has fostered the use of either sapphire or SiC as substrates. Although the highest power density has been obtained from very small gate periphery devices [2-3], the power performance of larger devices has been significantly compromised due to increased junction temperatures and deteriorating defect trapping effects. We have fabricated the devices with gate periphery from 100 µm to more than 10 mm. The power performance of one typical 400 µm gate periphery device on SiC substrates is shown in Fig. 6. The device has 4 gates with 100 µm gate width. The gate pitch was 49 µm to facilitate the good heat dissipation. The gate length was 0.2 µm determined from cross-sectional SEM images. The device was biased at class A with 30 volts drain bias and tested at CW mode at 10 GHz

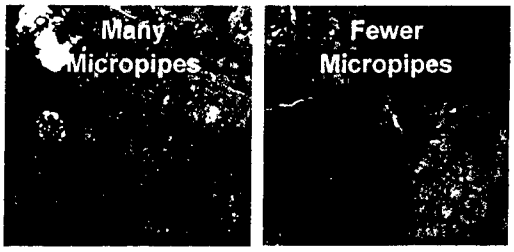


Fig. 7 X-ray topography of SiC semi-insulating substrates.

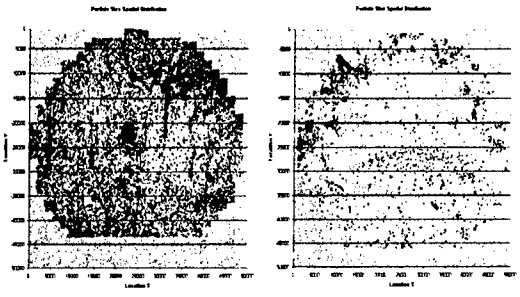


Fig. 8 Optical defect mapping of GaN/AlGaN HEMTs .

without active cooling. The output power density was 6.7 W/mm and power added efficiency was 47%. When the device was biased towards class AB, the PAE increased to more than 57%. The PAE was not pushed to the maximum due to the input power limitations. The large gate periphery devices are being packaged and currently tested.

TRAPPING EFFECTS

The early development of SiC MESFETs and GaN/AlGaN HEMTs has seen very low power densities compared to what can be expected from the DC current-voltage characteristics. This has been attributed to the trapping effects. Traps influence the power performance through the formation of quasi-static charge distributions, most notably on the wafer surface, in the buffer layers underlying the active channel or from the substrates. This parasitic charge acts to limit the drain-current and voltage swings, thereby limiting the high-frequency power output [6-8]. Great efforts have been dedicated to reduce the micropipe density and defects in SiC substrates, to improve the SiC epitaxial film quality, and to improve the epitaxial GaN and AlGaN quality. Surface passivation has

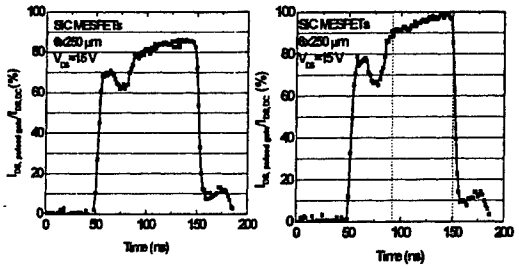


Fig. 9 Pulsed gate I-V characteristics of SiC MESFETs: less trapping (left), more trapping (right).

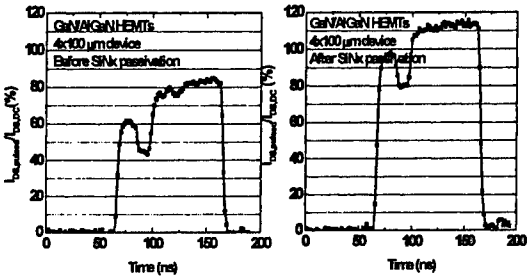


Fig. 10 Pulsed gate I-V characteristics of GaN/AlGaN HEMTs: before passivation (left), after SiNx passivation (right).

also been proven to be critical to stabilize the surface states especially for GaN/AlGaN HEMTs. We used X-ray topography to characterize the micropipes and defects in SiC substrates. Fig. 7 shows the x-ray topography images from two different SiC substrates. One was conventional semi-insulating SiC substrate with Vanadium as compensating doping and another one was Vanadium-free semi-insulating substrate. It is noted that the Vanadium- free substrates have significant fewer micropipes and low angle grain boundaries. Fig. 8 shows the optical defect mapping of GaN/AlGaN HEMTs wafers. The wafer on the right shows significant less defects than the wafer on the left. These micropipes and defects may not only account for the DC to RF current dispersion but also raise the questions for device long-term reliability.

The surface trapping generally can be identified through the gate lag measurements and buffer layer trapping can be characterized by drain lag measurements. Fig. 9 shows gate lag measurements from two SiC MESFET devices. The device gate periphery was 1.5 mm and there is no surface passivation applied. The drain bias was 15

volts while gate baseline was –12 volts. The gate voltage was pulsed from the baseline to +1 volt. The drain current was normalized to the DC drain current under the same conditions. The first device showed significant drain current slump under pulse mode while the devices from another wafer showed less drain current dispersion effects.

Fig. 10 shows the gate lag measurements of GaN/AlGaN HEMTs. The device gate periphery was 400 μm. The drain bias was 15 volts and the gate baseline was –8 volts. The gate was pulsed from the baseline to +1 volt. The drain current was normalized to DC drain current under the same conditions. The device without surface passivation only obtained ~80% of the drain current at DC. In contrast the SiNx passivated devices showed almost no current dispersion. The pulsed drain current over 100% of that at DC under the same condition was due to the reduced DC drain current by device self-heating. These results proved that the surface passivation was effective to stabilize the surface states and therefore almost fully recover the surface trapping effects in GaN/AlGaN HEMTs.

CONCLUSION

SiC MESFETs and GaN/AlGaN HEMTs have been fabricated and characterized. 3-dimensional thermal simulations were critical to fully exploit the device potentials especially for large gate periphery devices. For SiC MESFETs operated at UHF band (450 MHz), 62 watts output power has been obtained from single 21.6 mm gate periphery devices, which is the highest power from single device at UHF band. SiC MESFETs operated at 3 GHz have delivered 27 watts output power from single 14.4 mm gate periphery devices, while GaN/AlGaN HEMTs have demonstrated more than 6.7 W/mm from a 400 μm device tested at 10 GHz. X-ray topography and optical defect mapping have revealed the improvements of micropipes density in SiC semi-insulating substrates and defect density in AlGaN and GaN epitaxial films. Surface passivation on GaN/AlGaN HEMTs showed almost the full recovery of DC drain current dispersion from surface states. The surface passivation is needed for SiC MESFETs to eliminate the surface trapping effects.

ACKNOWLEDGMENTS

This work was supported by Lockheed Martin Corporation. The authors would like to thank M.E. Lazzeri, P.P. Gipp, P.L. Mowers, B. Joleyn, A.A. Johnson at GE global research center for device fabrication and mask layout, K. Chu at BAE systems for assistance with T-gate processing, C. Lee at TriQuint Texas for assistance with SiNx passivation, and V. Kaper at Cornell University for assistance with GaN/AlGaN HEMTs load-pull measurements.

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Simulation, Characterization and Design of Epitaxial Emitter NPN 4H-SiC BJTs for Amplifier Applications

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Abstract

We have analyzed the implementation of a 4H-SiC NPN high voltage BJT as a small signal amplifier transistor. From experimental characterization and intrinsic device modeling we determined that the factors limiting performance are base transport considerations and an inefficient layout for high frequency applications. Approaches such as improving base transport and base series resistance are suggested in order to achieve 4H-SiC BJTs with UHF and lower microwave frequency capabilities. Using two-dimensional numerical simulations, we present an improvement on the existing design wherein the intrinsic device modeling suggests a unity gain frequency f_T of approximately 5 GHz.

I. Introduction

SiC is a promising material for a wide variety of applications, with high voltage MOSFETs, rectifiers and bipolar junction transistors (BJTs) having been reported in recent years [1]. During the same time, SiC MOSFETs and MESFETs with RF capabilities have been demonstrated [2], [3]. The 4H polytype of SiC with a room temperature energy gap of 3.26 eV, saturated drift velocity of ~$2x10^7$ cm/s, critical breakdown field of ~2.5 MV/cm and a thermal conductivity of 4.9 W/cm-K is attractive for RF devices.

For applications such as amplifier output stages, BJTs are advantageous due to their high power density stemming from their current handling abilities. However, this power density capability comes at a cost of more complex bias circuitry, higher feedback capacitance and diminishing input impedance with frequency. Advances in the quality of SiC epi-layers have made the realization of SiC BJTs possible, with both implanted emitter and completely epitaxial vertical power 4H-SiC BJTs having been demonstrated [1], [4]. S-H. Ryu et al. presented a high voltage NPN 4H-SiC BJT fabricated with epitaxially grown collector, base and emitter layers [1]. The devices exhibited a blocking capability of 1800 V and common emitter current gain (β) of more than 20.

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In this paper, we analyze the performance of the aforementioned epitaxial emitter 4H-SiC high voltage BJT as a small signal amplifier transistor and describe design approaches to achieve devices with higher frequency performance capability. Important parameters for high frequency SiC BJT design are explored using numerical simulations.

II. Device Analysis and Characterization

Fig. 1 shows a two-dimensional schematic cross section of the SiC BJT presented in reference [1]. Vertically, the device is made up of N^+ emitter, P base and N^- collector layers epitaxially grown on top of an N^+ 4H-SiC substrate. Since the device was fabricated for high voltage (switching) applications, a 1 μm base width is used to prevent punchthrough breakdown. P^+ implantations are used to create lower resistance ohmic base contacts. The die includes three lateral cell pitches as shown in Fig. 1. As is typical with power switching devices, a single collector contact is made at the bottom of the die, common to all devices. The emitter and base stripes are interdigitated, and a single metal layer is used.

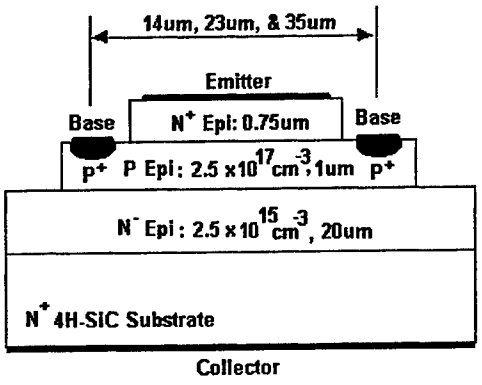


Fig. 1 2-D schematic cross section of devices reported by S-H. Ryu et al. [1]

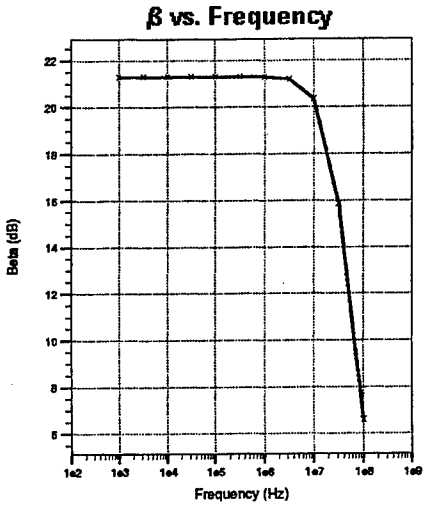


Fig. 2 Simulated frequency response of intrinsic device reported by S-H. Ryu et al. [1]

The device structure shown in Fig. 1 was simulated using MEDICI and ATLAS two-dimensional numerical simulators. Included within the 4H-SiC material parameters used are donor and acceptor levels of 0.1 eV and 0.2 eV, which are typical of n and p-type dopants. Due to the deep acceptor levels in SiC, incomplete ionization was modeled in all simulations, resulting in approximately 10% of acceptors being active at room temperature. The incomplete ionization of acceptors is significant to the common emitter current gain β as well as the base series resistance of the device.

Fig. 2 shows the simulated common emitter current gain β versus frequency for the structure as fabricated. For this simulation, the 35 μm cell pitch device was used. The bias conditions were such that V_{BE}=3 V, V_{CE}=10 V. Shockley-Read-Hall (SRH) lifetime

parameters τ_{p0} and τ_{n0} of 0.4 μs and 2.0 μs, respectively result in good agreement between simulated and experimental static I-V characteristics and were used in this simulation. Since parasitics associated with packaging and layout are not included, the results correspond to the *intrinsic* device performance. The results show an *intrinsic* limit on f_T for the device as fabricated to be approximately 400 MHz.

The device designed for high voltage / high power switching applications was not optimized for amplifier applications. The large base width (1 μm) results in base transport limited current gain and a high base diffusion capacitance, which limit the frequency response of the device. The low ambipolar diffusion constant (estimated at 4 to 8 cm^2/Vs) under high-level injection in the base plays a significant role. Here the base transit time is estimated to be on the order of 0.5 to 1 ns, resulting in a cutoff frequency in the hundreds of MHz. Simulations show that the device gain is indeed base transport limited with the base transport factor (α_T) and emitter injection efficiency (γ_E) calculated to be 0.94 and 0.98, respectively at the aforementioned bias conditions.

The devices originally reported in reference [1] underwent dc and ac characterization as part of this effort, with dc test results in general agreement with reference [1]. The 35 μm cell pitch devices exhibited the highest current gain of β_0=25 and were used in the subsequent amplifier testing. From the dc performance, bias conditions were set at $V_{CE|Q}$=10 V and $V_{BE|Q}$=3 V, $I_{C|Q}$=60-70 mA, $I_{B|Q}$=3-4 mA.

As stated earlier, the device was originally fabricated for power switching applications. Here, the collector contact was common to the entire (1.5 cm x 1.5 cm) die while the individual device areas were 800 μm x 660 μm. This introduced extraneous collector-base capacitance as well as parasitic capacitance from the collector to ground. Also, the layout of the devices was not aggressive, which results in extra base resistance as well as capacitance. The effects of these issues are clearly evident in the performance of the device as a small signal amplifier.

The device was biased in both common emitter amplifier and common collector emitter follower configurations. The common collector configuration was used in order to eliminate the parasitic fixture capacitance from collector to ground. Fig 3 (a) and (b) illustrate the circuits used for ac testing. In each case, the input signal of 10 mV_{RMS} or less or was supplied.

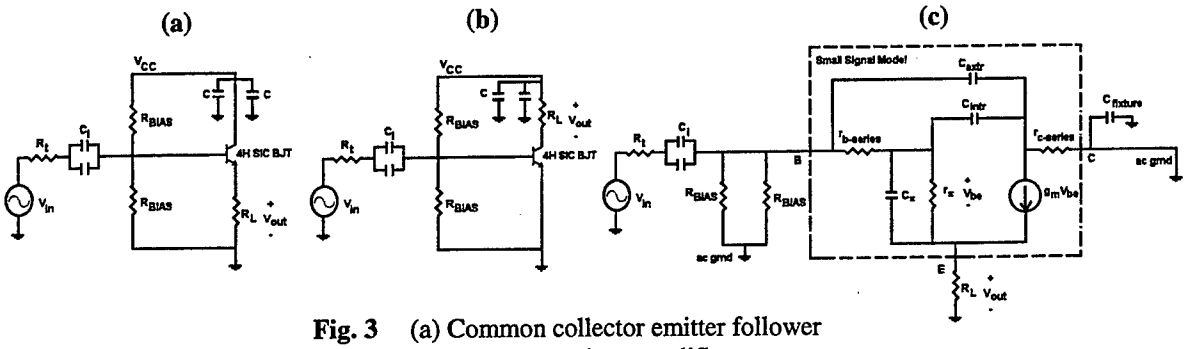


Fig. 3 (a) Common collector emitter follower
(b) Common emitter amplifier
(c) Small signal equivalent circuit of emitter follower

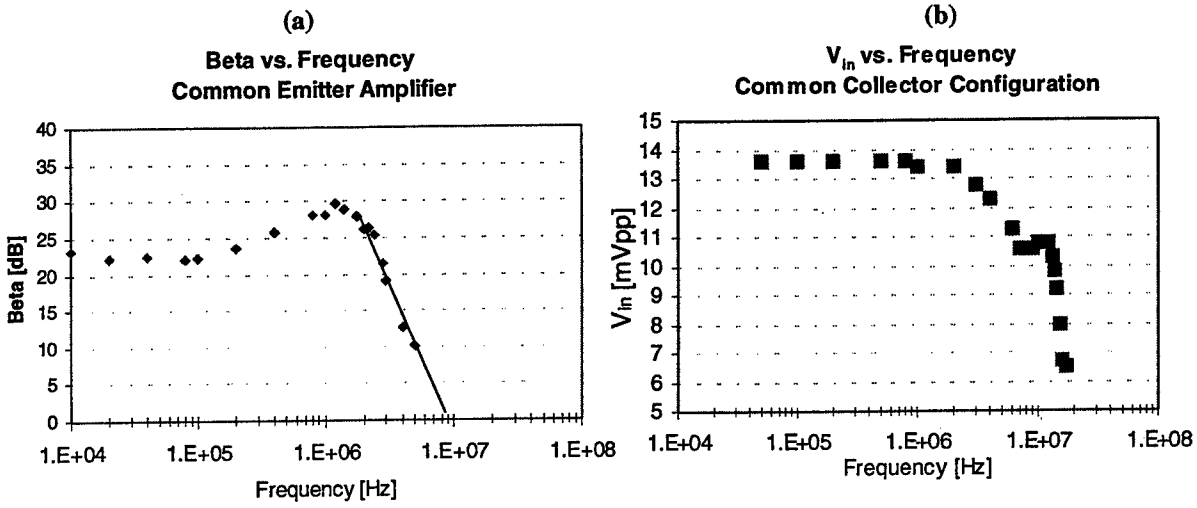


Fig. 4 4H-SiC BJT device testing results
(a) β vs. frequency in common emitter amplifier
(b) V_{in} vs. frequency in common collector circuit

In the common emitter amplifier shown, the device exhibited a cutoff frequency of only several MHz, attributed to the Miller effect in which the extraneous base-collector capacitance is multiplied by the voltage gain of the circuit. Here, SPICE modeling shows that in the presence of significant base series resistance (~100 Ω), a feedback capacitance as low as 100 pF can cause a reduction in gain at such low frequencies.

Placing the device in the common collector circuit allowed us to gain insight into the magnitude of the base series resistance as well as the collector-base feedback capacitance. The results of the amplifier testing are shown in Fig. 4 (a) and (b). Fig. 4 (b) depicts the magnitude of the voltage observed across at the base terminal of the device (denoted as V_{in}). Using Fig. 3(c) as a model, at high enough frequencies the feedback capacitance effectively shorts out the "π" components along with the load, leaving only the base and collector series

resistance as well as the front end bias circuitry in the ac path to ground. The magnitude of the series resistance can be estimated from the base voltage to source voltage ratio. The value is approximately 150 Ω, in agreement with first order calculations when an average mobility of 50 cm^2/V-s is assumed. The two distinct pole locations also suggest that the parasitic feedback can be modeled as a network in which a portion of the capacitance is located under the base contact regions and a portion which is under the emitter stripe.

III. Amplifier Device Design

From the simulation and characterization results shown the design of the base width, doping and layout of the SiC BJTs in section II must be addressed. The base width must be decreased from 1 μm to ~200 nm while decreasing the base series resistance associated with device layout. More aggressive lithography should be used in order to realize microwave or UHF devices. Fig. 5 illustrates simulated potential drop under the emitter for 12 μm and 2 μm stripe widths. The 12 μm stripe exhibits almost a six times larger potential drop across the stripe than does the 2 μm stripe at the same current. This results in significantly more current injection at the edges, which in turn means less area of the device is being used for current gain.

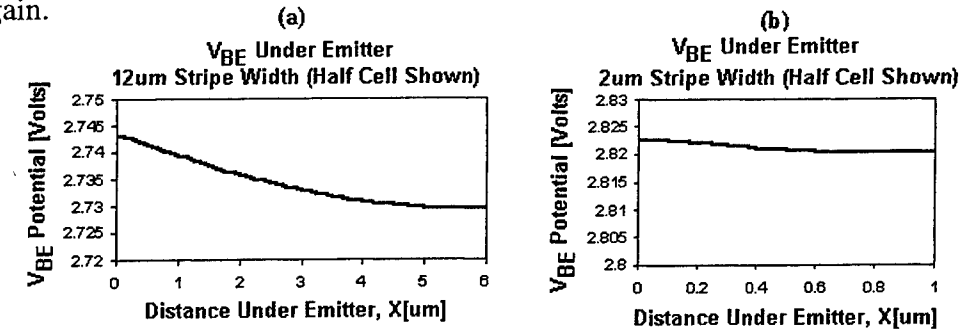


Fig. 5 Base-Emitter potential drop vs. distance under emitter
Base spreading resistance causes the wider stripe width
to suffer from additional current crowding

Since simulations show that the present device gain is base transport limited, improvement of the frequency response requires decreasing the base width while increasing the base doping concentration to minimize the increase in base spreading resistance. A new structure was designed in which the base width was decreased to 200 nm, with the base doping concentration increased to $5x10^{17}$ cm^{-3}. The base series resistance per area increased by almost 2.5 times. However, the low frequency current gain increased by a factor of 8. The emitter injection efficiency and the base transport factor of the new design are closer (α_T,γ_E >0.99), which suggests that the base width is more optimum for current gain (versus blocking voltage in previous design). The width of the lightly doped collector was also reduced to 3μm. MEDICI simulation results indicate that the *intrinsic* device cutoff frequency has increased to approximately 5 GHz. Fig. 6 illustrates forward I-V characteristics of the reduced base width design up to a collector bias of 100 V.

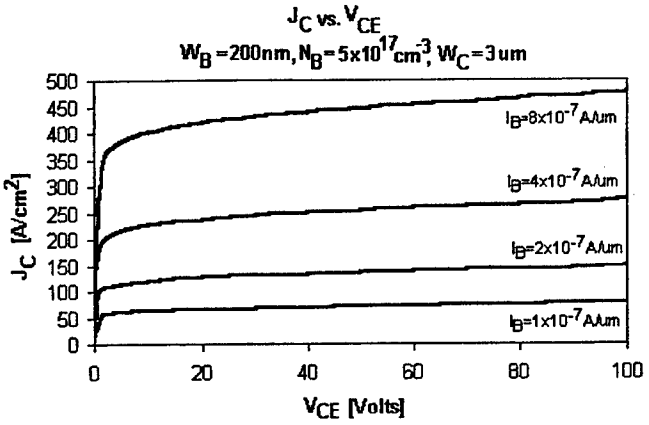


Fig. 6 Simulation results of forward I-V characteristics for 200nm base width design

IV. Summary and Conclusion

We have analyzed the use of an existing high voltage power BJT design as a small signal amplifier. The simulation results show that the *intrinsic* device is limited by the 1 μm base width, which results in low current gain as well as large diffusion capacitance. Although the test fixture primarily limited the ac testing presented within, insight into the device *intrinsic* response was obtained. The effects of the extraneous capacitance and resistances associated with the test fixture and inefficient device design (for high frequency) are heightened by the large base series resistance of SiC NPN BJTs. In order to realize useful vertical UHF and lower microwave frequency BJTs for power applications, reduced base widths and more aggressive layout dimensions should be incorporated. Although SiC BJTs may not outperform SiC MOSFETs or MESFETs at high frequencies, they offer the potential for high output power density at lower frequencies since they do not suffer from the poor inversion mobility or drain to gate breakdown.

Acknowledgement

This work was performed in part by the MURI program, supported by the Office of Naval Research, Contract N00014-95-1-1302.

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RF 4H-SiC Bipolar Junction Transistors

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Abstract.

We report on the progress towards a silicon carbide (SiC) bipolar transistor aimed at operation at RF frequencies up to 3GHz. Devices with a 5μm emitter stripe width were fabricated and tested on-chip with cascade probes and an HP8510C network analyzer. These devices have an f_t/f_{max} of 0.6/0.2GHz. To best of our knowledge the devices represent a first demonstration of an RF 4H-SiC BJT.

I. Introduction

Silicon carbide is a wide band gap semiconductor that has been identified as a potential candidate for use in high power and high frequency devices due to its superior material parameters. SiC has a breakdown field almost ten times higher than that of silicon or six times that of gallium arsenide resulting in a higher attainable power density. The higher breakdown field results in a shorter electron transit time through a depletion layer with the same blocking voltage. SiC has a larger thermal conductivity, 3 times that of Si and 6 times that of GaAs, translating into a smaller chip size and, therefore, more efficient systems. The higher thermal conductivity and higher temperature operation due to the wider band gap of SiC result in a higher maximum power dissipation density compared to Si and GaAs-base devices. Together these material properties provide the basis for the potential of SiC-based power RF devices at L and S-band.

We have chosen a 4H-SiC BJT structure because of its potential to yield a device with short transit time and high power density. We designed and fabricated a typical RF device structure with narrow emitter stripes, a thin base and an ion-implanted base contact layer.

II. Material characterization.

The device fabrication starts with a 0.02Ωcm n-type 4H-SiC substrate. A 3μm thick $2x10^{16}cm^{-3}$ nitrogen-doped collector layer is grown first followed by a 100nm thick $2x10^{18}cm^{-3}$ aluminum-doped base layer and a 200nm thick $1x10^{19}cm^{-3}$ nitrogen-doped emitter layer. This material was purchased from Cree Inc. The Secondary Ion Mass Spectroscopy profile is shown on Figure 1.

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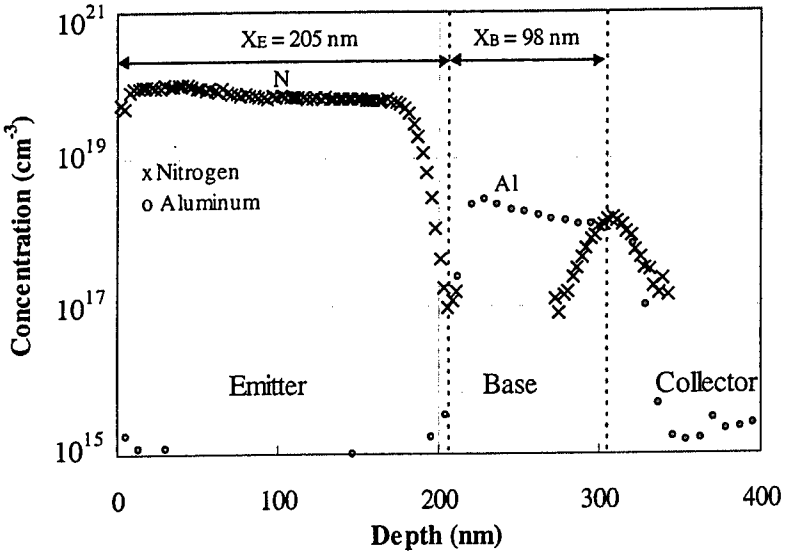


Figure 1 SIMS profile of the BJT epilayer structure

The average nitrogen doping of the emitter obtained from Figure 1 is $6.7x10^{19}$ cm^{-3}. The average aluminum doping of the base is $1.45x10^{18}$ cm^{-3}. Because of the 191meV activation energy [1] of aluminum in SiC, and the lower 65meV activation energy of nitrogen [1], the nitrogen peak observed at the base-collector junction effectively reduces the width of the base layer to 66nm. The reduction of the base width, the low ionization of aluminum, and probably nitrogen compensation of aluminum throughout the base, result in a high base sheet resistance. For this material, the sheet resistance of the base was found to be 195kΩ per square. The collector doping could not be determined from SIMS due to the nitrogen detection limit of $10^{17}cm^{-3}$. The doping was obtained from capacitance-voltage measurements and was found to be $2.5x10^{16}$ cm^{-3}.

III. Fabrication procedure.

The device is fabricated by etching a double-mesa structure using CF_4/O_2 RIE. A base contact layer is then formed by ion-implantation of $10^{15}cm^{-2}$ aluminum with 50 keV at 600°C. A 30 min anneal at 1630°C in a SiC CVD reactor in silane was done at Acreo AB to remove the implantation damage and to activate the implanted species. The structure is then passivated with a 300nm SiO_2 layer. Via holes are etched for the emitter, base and collector layer, followed by the deposition of the Ni/Cr emitter and front collector contact metal and the Ti/Al base contact metal. Nickel was evaporated on the back to provide a back collector contact to allow the DC testing of large devices. All the metals were evaporated in a resistively heated evaporator at a base pressure of $2x10^{-6}$ Torr. The contacts are annealed at 1000°C for 2 minutes in vacuum, resulting in a p-type contact resistivity of $4.2x10^{-5}\Omega cm^2$ and an n-type contact resistivity of $3.9x10^{-6}\Omega cm^2$ both characterized with a linear Transmission Line Method structure. The devices where then completed by adding a Cr/Au wiring metal. A cross section of the device is shown in Figure 2.

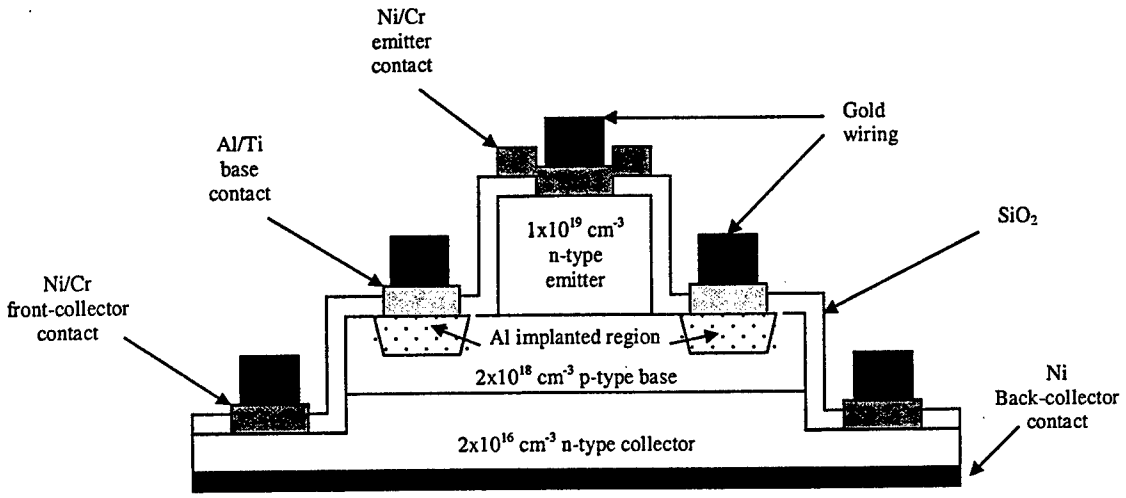


Figure 2 Cross section of the a double mesa BJT structure

IV. DC and RF characterization.

The devices were DC tested using an HP4145B semiconductor parameter analyzer. The characteristics of a 5x50μm^2 emitter transistor are shown in Figure 3 and Figure 4.

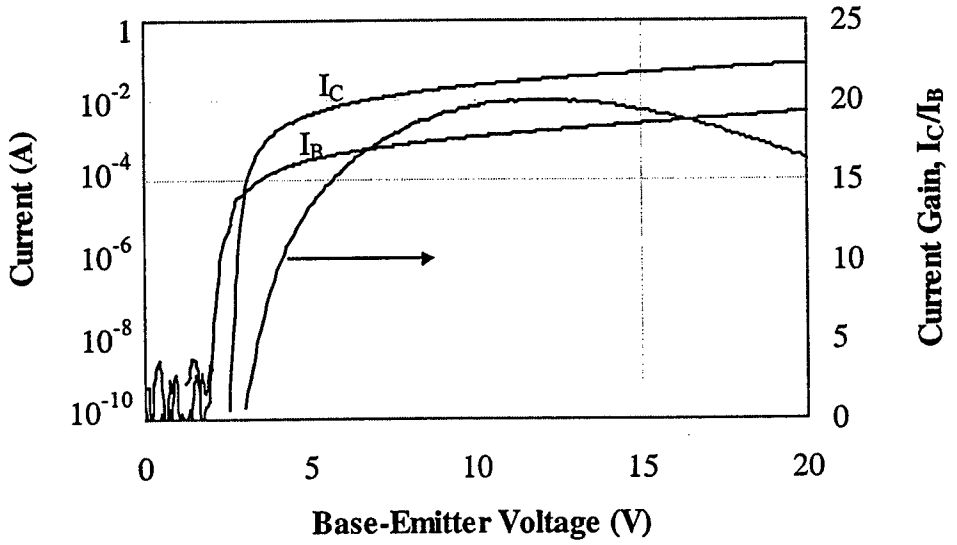


Figure 3 Gummel plot of a 5x50μm^2 emitter BJT measured at room temperature. The base and collector were kept at the same potential during the measurement.

Figure 3 shows that the maximum DC current gain of this transistor is 20. It can be seen that the base current appears to have a turn on voltage lower than that of the collector current. We believe that the base current seen at these lower voltages is due to base-emitter leakage current caused by the incomplete removal of the emitter epilayer on top of the

extrinsic base. At higher current levels the base current flattens due to the high resistance of the base consistent with the measured high base sheet resistance.

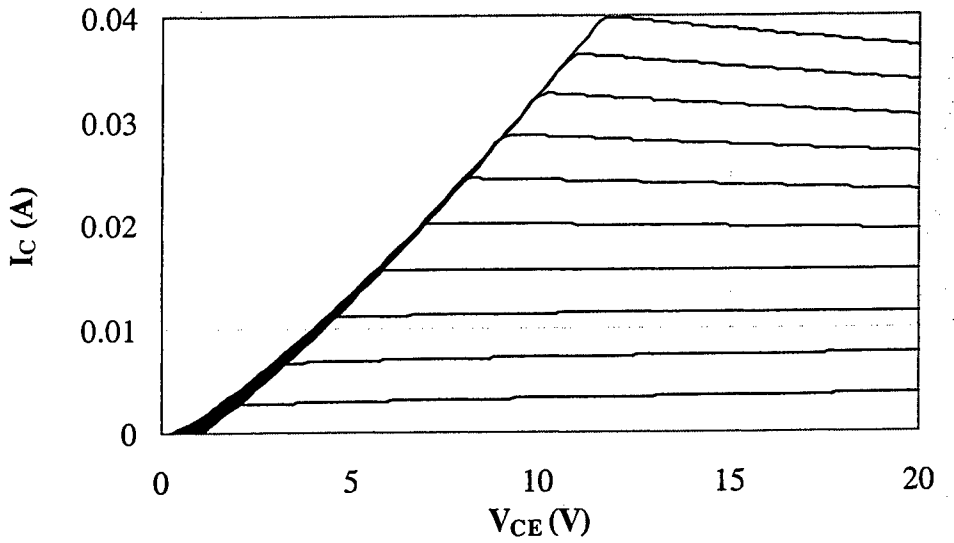


Figure 4 Common-emitter I-V characteristics of a 4H-SiC bipolar junction transistor with a 5x50μm² emitter. The applied base current is 0.2mA (bottom trace), 0.4mA, 0.6mA, 0.8mA, 1.0mA, 1.2mA, 1.4mA, 1.6mA, 1.8mA and 2mA (top trace).

The common emitter I-V characteristics on Figure 4 show a characteristic slope of the collector current before it reaches its maximum value for a given base current. This can be explained as follows. As the base current flows laterally through the extrinsic base from the base contact to the emitter, a voltage drop is observed across the extrinsic portion of the base. This in turn causes the base-collector voltage to have a significant lateral variation across the extrinsic base. Part of the extrinsic base-collector junction will then be forward biased even if the base-collector junction is reversed biased in the intrinsic base region. The applied base current will then be divided between the portion of the forward biased base-collector junction and the forward biased base-emitter junction. Only the current that flows through the base-emitter diode gets amplified and has a significant impact on the collector current. As the collector-emitter voltage is increased, the forward bias across the base-collector is reduced causing less of the applied base current to flow to the collector and more current is then injected from the base into the emitter. Eventually, the base-collector voltage across the whole base is equal or less than zero so than no base current is injected across this junction. Beyond this point the collector current reaches a fairly constant value.

At collector currents larger than 20mA the current decrease as the collector-emitter voltage increases. We believe this is due to heating effects. Notice that the maximum current density of this device is 16kA/cm^2 at 12V V_{CE}. The maximum dissipated power density is 300kW/cm^2 at 20V V_{CE}. We have demonstrated devices with a current density capability of 42kA/cm^2 [2] but the current density handling ability shown by the device presented here is sufficient to achieve a high frequency performance.

The RF characteristic of the transistor were obtained with on-chip measurements using cascade probes and an HP8510C network analyzer. The RF contact pad footprint used for these measurements is shown on Figure 5.

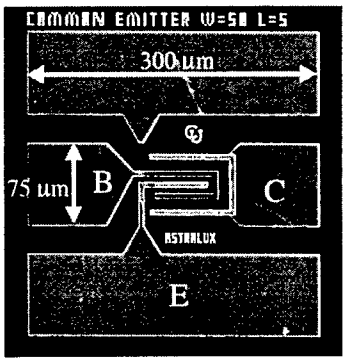


Figure 5 RF characterization contact pads with a 5x50µm^2 emitter BJT

The high frequency measurements were performed using a Short -Open- Load-Through calibration technique. A commercial load standard was used in conjunction with on-chip open, short and through structures consistent with the contact pads shown on Figure 5. The cutoff frequency, f_t, and the maximum oscillation frequency, f_{max}, were obtained from the measured s-parameters using the following formulae[3][4]:

$$h_{21} = \frac{2s_{21}}{s_{12}s_{21} + (1 - s_{11})(1 + s_{22})} \tag{1}$$

$$U = \frac{\left|s_{21}/s_{12} - 1\right|^2}{2k\left|s_{21}/s_{12}\right| - 2\mathrm{Re}(s_{21}/s_{12})} \tag{2}$$

$$k = \frac{1 - \left|s_{11}\right|^2 - \left|s_{22}\right|^2 + \left|s_{11}s_{22} - s_{12}s_{21}\right|^2}{2\left|s_{12}s_{21}\right|} \tag{3}$$

Figure 6 and Figure 7 show the frequency dependence of the AC common emitter current gain and the unilateral power gain, respectively, calculated with equations (1) and (2). The expected behavior of 10dB/decade decrement of $|h_{21}|$ and 20dB/decade for U are plotted with a solid line on the corresponding figure.

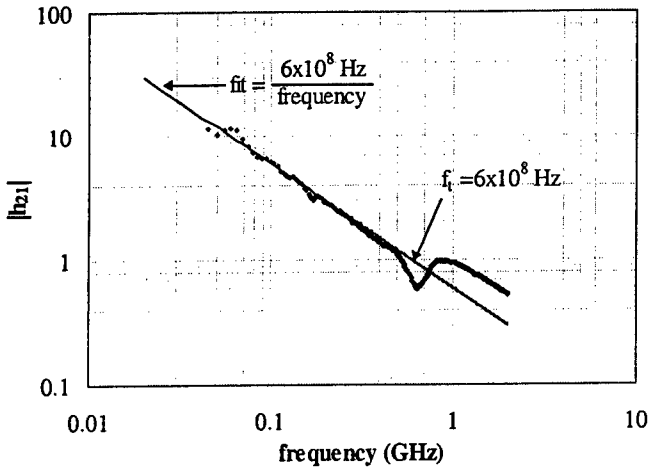


Figure 6 $|h_{21}|$ for a 5x50μm^2 emitter calculated from the measured s-parameters. J_E=10kA/cm^2, V_{CE}=20V

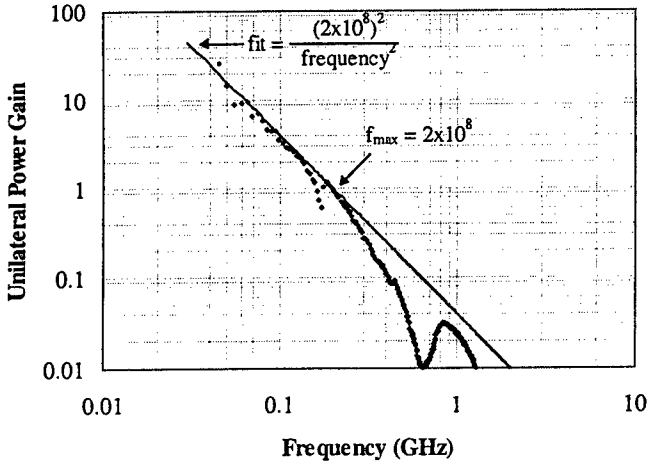


Figure 7 Unilateral power gain for a 5x50μm^2 emitter calculated from the measured s-parameters. J_E=10kA/cm^2, V_{CE}=20V.

These measurements indicate an f_t of 600MHz and an f_{max} of 200MHz. The value of f_t is significantly lower than the theoretical cutoff frequency of 22.15GHz calculated using the following expression:

$$f_t = \frac{1}{2\pi\left(\frac{\eta_i V_t}{I_E}\left(C_{je}+C_{jc}\right)+\frac{X_{Bi}^2}{\eta V_t \mu_{nB}}+\frac{X_{bc}}{2v_s}+(R_E+R_C)C_{jc}\right)} \qquad (4)$$

This discrepancy is due to the high base resistance. The applied AC base current is divided between the base-collector and the base-emitter impedances. At low frequencies, the base-emitter impedance is significantly lower than the base-collector impedance. In this case, most of the applied AC base current is injected into the emitter and the transistor behaves normally. As the frequency of the applied base current increases, the base-collector impedance, mostly capacitive, decreases and eventually becomes smaller than the base-emitter impedance. With increasing frequency more of the applied base current is injected directly into the collector and the current amplification is lost. The result is a lower transit frequency, f_t, than that obtained from equation (4).

It is also important to mention that the use of the on-chip open structure during the calibration can result in a calibration error when the substrate is conductive. One way to completely remove the effect of the pads from the transistor of interest is by using probes that are not connected as the open condition during the calibration [5]. The s-parameters measured for the on-chip open structure are used to de-embed the impedance related to the contact pads from the s-parameters measured on an actual device. With this technique one expects an f_t in the order of 1GHz for the device discussed in this paper. The performance would be limited by the base-collector impedance determined only by the device structure.

V. Summary.

The DC and RF characteristics of a 4H-SiC have been presented. A maximum DC common emitter current gain of 20 was measured on a device with a $5x50\mu m^2$ emitter. The s-parameters obtained for this device indicate and f_t/f_{max} of 600/200 MHz. The RF performance is limited by the high base resistance as well as the base-collector impedance that includes the capacitance of the contact pads as well as the capacitance of the base-collector junction. To the best of our knowledge this is the first report of the high frequency performance of a SiC bipolar junction transistor and it demonstrates the potential of this device for their use in RF applications.

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Acknowledgments

We would like to thank Jan Van Zeghbroeck for the automation of the DC measurements and Jim Smith for the help provided in the device fabrication.

This work was sponsored in part by OSD/AFRL monitored by John King (WPAFB).

Ge Incorporation in SiC and the Effects on Device Performance

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Abstract

Silicon carbide has been given much attention as a promising material for use in high-voltage and high-power devices. The absence of closely lattice-matched materials precludes the existence of heterostructure devices with good properties. The availability of a lattice-matched heterojunction partner should allow for new SiC-based devices that can exploit the heterojunction band offsets to enhance device properties.

Silicon-carbide:Germanium (SiC:Ge) alloys were formed by ion implantation of Ge into 4H-SiC wafers at 1000 °C. We have observed the resultant SiC:Ge material to have favorable properties, such as nice crystal structure, interface quality and good electrical characteristics.

Diodes and bipolar transistors have been fabricated using these layers. These devices have been characterized for properties including forward current density and transistor gain. In this paper we report on the effects of Ge incorporation on devices formed using SiC:Ge layers.

SiC:Ge Alloy

The concept of Ge incorporation into SiC is illustrated in Figure 1. The SiC:Ge alloy was fabricated by low-energy ion implantation. Ge^+ ions were implanted at 140KeV and 50KeV into a 4H-SiC wafer heated to 1000 °C. SiC wafers were purchased from Cree <0001>, N-type and ρ=0.059 Ω-cm. This results in a step-like Ge profile starting at the surface and extending 1200 Å into the substrate, as shown in Figure 2. The composition profile was later checked with Rutherford Backscattering Spectrometry (RBS), which verified the presence of Ge in the substrate. High Resolution X-Ray Diffraction (HRXRD) spectra were measured with a Phillips X'Pert diffractometer equipped with a four-crystal Ge (220) monochromator and Ge channel-cut analyzer on the primary and detector optical arms repectively. Figure 3 displays the (0004) HRXRD spectra from as-implanted SiC:Ge with 0.4% Ge incorporation together with a non-implanted 4H-SiC control sample. The

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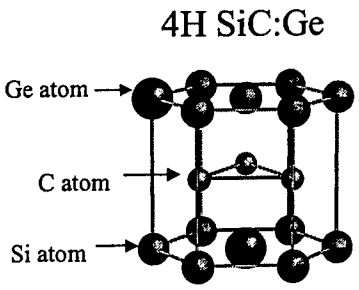


Figure 1. SiC lattice with substitutional Ge atoms, forming a SiC:Ge alloy solid solution.

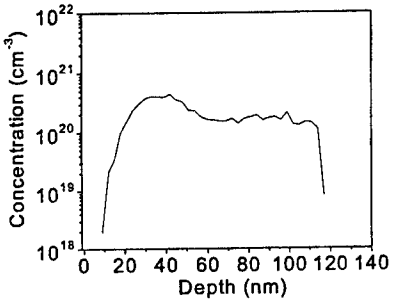


Figure 2. Implanted Ge projected profile simulated by SRIM 2000.

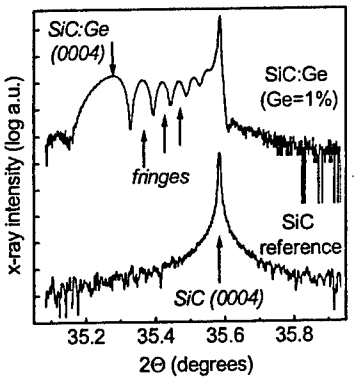


Figure 3. (0004) HRXRD spectra from as-implanted SiC:Ge with 0.4% Ge incorporation together with non-implanted 4H-SiC samples as a reference.

Pendellösung (thickness) fringes of SiC:Ge in Figure 3 indicate good crystalline quality and a coherent interface [1]. No such fringes have previously been noted in implanted SiC substrates, presumably due to heavy lattice damage [2, 7]. The strained layer thickness (t) can be calculated from the fringe period ($\Delta\Theta$), X-Ray wavelength (λ=1.54 Å) and the Bragg angle (Θ_B) with the equation:

$$t = \frac{\lambda \sin \Theta_B}{\Delta\Theta \sin 2\Theta_B}$$

From the data in Figure 3 the strained layer thickness, t, is calculated as 140 ± 20 nm, in good agreement with the projected Ge depth profile simulated by SRIM 2000.

Optical properties of the SiC:Ge material were studied using Raman Spectroscopy and UV-Visible spectrometry techniques. Raman Spectroscopy measurements were performed using a green laser system (λ = 532 nm). The presence of the characteristic (796 cm^{-1} and 972 cm^{-1}) peaks in the Ge implanted areas confirmed that the 4H-SiC structure was reconstructed after the high-temperature anneals. UV-visible measurements were performed in transmission mode over the 190 –1100 cm^{-1} wavelength region. Analysis of the absorption spectra using the MacFarlane-Roberts equations yielded a decrease in the optical bandgap of 100 meV for a layer with 2.2 atomic % of Ge.

These results suggest that low energy implantation can form SiC:Ge alloy with good crystal and interface quality and lower optical bandgap, thus crediting the potential for fabricating SiC:Ge/SiC heterostructures.

TLM Measurements on SiC:Ge layer

To do the contact studies, TLM (Transfer Length Method) patterns were fabricated on both n-type and p-type SiC:Ge samples together with SiC ones for comparison [5]. Both the p-type and n-type SiC:Ge samples were used with approximately two atomic percent of Ge.

The TLM measurements showed a significant reduction in contact resistivity: from 5.3×10^{-4} Ω-cm^2 to 6.0×10^{-5} Ω-cm^2 for n-type SiC:Ge; and from 1.2×10^{-3} Ω-cm^2 to 8.3×10^{-5} Ω-cm^2 for p-type case. And calculations showed a reduction in the effective barrier height by 57 mV and 70 mV, respectively for n-type and p-type SiC:Ge. Table I summarizes the TLM measurement results. These results suggest the potential of Ge containing layers to become an important processing technique to lower the contact resistance with SiC.

Material Type	Contact Resistance R_c (Ohms)	Transfer Length L_t (microns)	Contact Resistivity (Ohms-cm^2)	Barrier Height Reduction (mV)
n-SiC:Ge	35.3	1.71	6.0×10^{-5}	57
n-SiC	196.2	2.70	5.3×10^{-4}	--
p-SiC:Ge	29.7	2.80	8.3×10^{-5}	70
p-SiC	551.8	2.18	1.2×10^{-3}	--

Table I. Summary of the TLM measurements of SiC:Ge alloy compared with SiC.

SiC:Ge/SiC Heterojunction Diodes

SiC:Ge/SiC heterojunction diodes and reference SiC p-n junction ones were fabricated using Ti/Au metal as electrical contacts[3]. The current-voltage characteristics on the SiC:Ge/SiC diodes were measured and summarized in Table II. The data was found to fit well to a simple theory of injection over a heterojunction barrier, as shown in Figure 4. A typical current voltage plot of the SiC:Ge heterojunction and SiC homojunction diodes is given in Figure 5. The incorporation of Ge was found to increase the diode current density and decrease the heterojunction ideality factor from 1.88 to 1.48. The greater asymmetry between forward and reverse current (larger rectification ratio) for the SiC:Ge devices suggests the presence of band offsets. Capacitance-voltage measurements show that that the Ge also reduced the measured built-in voltage. This result was found to be consistent with the observed difference in layer contact resistances [5].

Diode Material	Rectification Ratio (4V)	η	Current Density (@5V) [mA/cm^2]	Specific Contact Resistance [Ω-cm^2]
SiC:Ge	2.79	1.48	650	1×10^{-3}
SiC	1.60	1.88	400	4×10^{-3}

Table II. Summary of the electrical properties of SiC:Ge and SiC diodes, where η is the effective heterojunction ideality factor. The SiC:Ge diodes have a larger current density and rectification ratio, as expected with a heterojunction band offset.

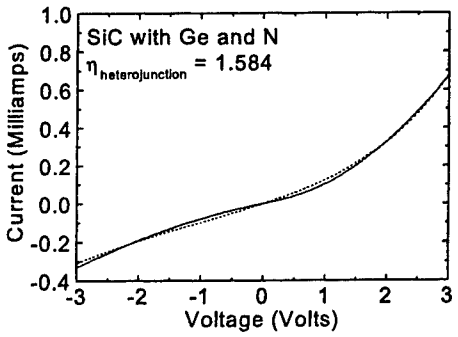


Figure 4. Measured I-V data of a typical SiC:Ge p-n diode (solid line). The dashed curve is a fit of the data with the heterojunction current model that takes into account the heterostructure band offsets as described in the text.

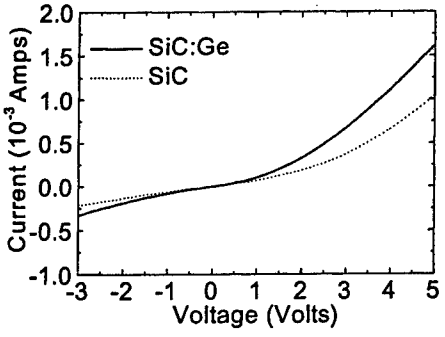


Figure 5. Measured Current-voltage plot of SiC:Ge and SiC diodes. Note the large increase in current density with the presence of Ge.

SiC/SiC:Ge/SiC p-n-p heterojunction bipolar junction transistors (HBTs)

SiC/SiC:Ge/SiC p-n-p heterojunction and SiC p-n-p homojunction bipolar junction transistors (BJTs) were fabricated by ion implantation and annealing[4]. The collector regions were the bulk of a 4H-SiC p-type (approximately 2 x 10^{16} cm^{-3}) wafer. The p+-emitter regions were formed by the implantation of Ga. The SiC:Ge base region was formed by the co-implantation of Ge and N. A two-step implant anneal was performed at 1050 °C for 30 minutes and then 1600 °C for 30 minutes. Simple mesa transistors were then fabricated with RIE etching.

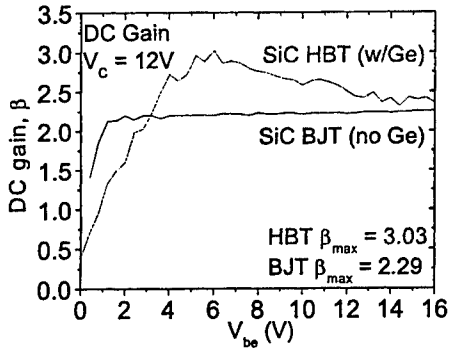


Figure 6. DC current gain, β, versus base-emitter voltage for the SiC:Ge HBT and SiC BJT. Note the larger gain with Ge as expected for a HBT with a heterojunction offset in the base region.

The electrical properties of the SiC/SiC:Ge/SiC p-n-p heterojunction and SiC p-n-p homojunction bipolar junction transistors are summarized in Table III. The SiC:Ge devices exhibited higher maximum gain (3.02 vs. 2.21) and larger Early voltage (605 V vs. 321 V) than the SiC BJT counterparts. Figure 6 shows the typical HBT and BJT common emitter current gain versus base-emitter voltage from the respective Gummel Plots. In each case, the breakdown voltage (BV_{CEO}) of the devices exceeded 50 V. The existence of heterojunction offsets should be manifested in the gain and early voltage properties of the devices, similar to effects seen in Si/SiGe/Si transistors [8].

For a transistor with a lower bandgap material in the base, an increase in the gain β, by a factor of exp ($\Delta E_g / k_B T$) is expected, where ΔE_g is the bandgap reduction. Based on this and the β increase, ΔE_g is calculated to be 8.1 meV. Also, assuming the bandgap of SiC:Ge alloy is linear with Ge percentage between SiC and Ge, together with the predicted 0.34% of average Ge concentration from SRIM simulations, SiC:Ge alloy should have a ΔE_g of 8.6 meV lower than the bandgap of SiC. These two predicted values agree with each other very well.

For a transistor with a gradient in Ge concentration from the base to collector junction (provided here by the Gaussian nature of the Ge-implant profile), there will also be an increase in the Early Voltage, V_A, by a factor of exp ($\Delta E / k_B T$), where ΔE is the bandgap reduction at the collector side of the base compared to the emitter side. From SRIM implantation simulations, we expect the predicted base to collector fraction gradient to be 0.70 atomic percent. This gradient should result in an ΔE of 17.8 meV. From our typical measured Early voltage values, we calculated an ΔE of 16.4 meV, which once again exhibits excellent agreement. These two measurements again indicate heterostructure device behavior.

Sample	Common Base Current Gain (α)	Maximum Measured DC gain (β)	Calculated Band offset, ΔEg [meV]	Early Voltage [V]	Calculated Base Bandgap Gradient [meV]
SiC:Ge HBT	0.850	3.02	8	605	16.4
SiC BJT	0.812	2.21	0	321	0

Table III. Summary of the electrical properties of SiC/SiC:Ge/SiC HBT and SiC BJT devices. The calculated average band offset and total band gradient data calculated from the measured device properties are indicated.

Conclusion

In conclusion, we have fabricated and characterized SiC:Ge alloy layers. The presence of Ge has proven to lower electrical contact resistances to devices up to a factor of 10. SiC-based heterostructure devices have been fabricated and demonstrated based on these layers. Heterostructure diodes with varying current density and rectification ratio were observed. We have made the first SiC-based HBT devices, and noted that the presence of Ge in the base increases the gain and the Early voltage by as much as 33% over a homojunction BJT fabricated without Ge but otherwise with an identical process. A common-emitter current gain for the HBT of greater than 3 has been achieved. These results show that SiC:Ge is a promising material for a range of SiC-based heterostructure devices.

Acknowledgements

The authors would like to thank G.C. DeSalvo, J. R. Gigante and R.C. Clarke from Northrop Grumman Corp., Baltimore, MD for their assistance with this work. The authors

gratefully acknowledge Thomas Adam for assistance with device processing and Dr. George Watson for assistance with the UV-Visible measurements. Special thanks to C. Wood, M. Yoder, and J. Zolper for technical discussions, and to D.C. Tsui for suggesting the heterojunction diode model. This research is supported by ONR contract no. N00014-00-1-0834 and ARO AASERT contract no. DAAG55-97-1-0249

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Molecular Beam Deposition of Low-Resistance Polycrystalline InAs

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Abstract

We report low-resistance Si-doped polycrystalline InAs (poly-InAs:Si) using molecular beam deposition. We believe this to be the first report of low resistance in poly-InAs. The poly-InAs:Si was deposited using conventional molecular beam epitaxy (MBE) onto SiN_x coated GaAs substrates at various growth temperatures and deposition rates. Poly-InAs samples with thicknesses of 2000Å and 1000Å were grown for Hall and TLM measurements, respectively. We have observed electron concentrations from 8.8×10^{18} to 1.5×10^{19} cm^{-3} and respective mobilities from 886 to 441 cm^2/Vs. This range of values suggests that the poly-InAs:Si has a doping-mobility product, and hence bulk conductivity, that is only 3-4 times lower than that of similarly doped InGaAs lattice-matched to InP. The typical bulk resistivity determined by TLM measurements is approximately 1.4×10^{-3} Ω-cm. Contact resistance to the poly-InAs with a Ti/Pt/Au metal stack less than 1.6×10^{-7} Ω-cm^2. The combined low contact access resistance and low junction capacitance found in poly-InAs:Si may be useful in a variety of III-V device applications.

1. Introduction

Heavily doped polycrystalline silicon (polysilicon) is commonly used in the fabrication of Si- and SiGe-based bipolar junction transistors (BJTs) and heterojunction bipolar transistors (HBTs). Polysilicon is used in the extrinsic base contact of Si-based transistors to obtain reduced base contact resistance and lower base-collector capacitance (C_{bc}). Heavily doped polysilicon is used to form the diffused, self-aligned emitter and an extrinsic emitter contact that is much wider than the active base-emitter junction [1,2]. Low-resistance, p-type polycrystalline GaAs (poly-GaAs) has been reported as an analogous extrinsic base contact material for use in III-V HBTs [3,4]. In this application, low-resistance poly-GaAs might been used with a dielectric buried in the extrinsic base-collector area to reduce C_{bc} while maintaining a low base contact resistance [5], as analogous to established SiGe HBT processes [2]. The poly-GaAs work achieved a lowest resistivity of approximately 5×10^{-3} Ω-cm with a hole concentration of 8.4×10^{20} cm^{-3} [4].

This work is meant to demonstrate a low-resistance polycrystalline material that may be suitable for use as an extrinsic emitter contact that is much wider than the active base-emitter junction. N-type poly-InAs:Si has been found to have resistivities as low as 1.4×10^{-3} Ω-cm and contact resistance to a Ti/Pt/Au metal stack of less than 1.6×10^{-7} Ω-cm^2. We have used the low-resistance poly-InAs in an HBT utilizing non-selective-area regrowth in the

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formation of the emitter-base heterojuction [6]. In general, combined low contact access resistance and low junction capacitance may also be useful in a variety of III-V device applications through the formation of a wide, extrinsic n-type contact layer deposited over a narrow semiconductor mesa and planarized by a buried dielectric.

2. Experimental Procedure

Poly-InAs:Si was grown in a modified Varian GenII solid-source MBE system. The poly-InAs was deposited on (100) semi-insulating GaAs substrates coated by PECVD with 3000Å of SiN_x. The deposition temperature of the substrate was determined by pyrometer and was typically maintained at approximately 480°C. The deposition rates varied from 0.21-0.77 μm/h. The SiN_x coated wafers were first raised to a temperature above 550°C in the MBE growth chamber. Hydrogen was allowed to escape from the SiN_x coated wafers until the baseline pressure of the growth chamber was achieved. The wafer temperature was then lowered to the desired growth temperature, and the Si-doped InAs was deposited. For studies of the bulk material, 2000Å of poly-InAs:Si was deposited directly onto the SiN_x coated wafers. For studies of the electrical characteristics, 1000Å of poly-InAs was grown on top of approximately 2000Å of polycrystalline InAlAs. The polycrystalline InAlAs is assumed to be highly resistive and of low mobility similar to that shown in published work on polycrystalline InGaAs [7] and our own experience with polycrystalline ternaries. Electron concentration and mobility were determined by room temperature Hall measurements. Resistance data were determined by TLM measurements using a Ti/Pt/Au metal stack. The grain size of the poly-InAs was examined by scanning electron microscopy (SEM).

3. Results and Discussion

The dependence of electron concentration and mobility of the doped poly-InAs:Si on the doping cell temperature is shown in Fig. 1. The substrate growth temperature was 480°C, and the growth rate was 0.71 μm/h. The Si cell temperature was varied between 965-995°C in these growths. As expected, the electron concentration increases with the doping cell temperature, and the mobility decreases with increased carrier concentration. In this range of increasing doping cell temperature, the electron concentration increases from 8.8×10^{18} to 1.5×10^{19} cm^{-3} and the mobility decreases from 886 to 441 cm^2/Vs. For comparison, InGaAs lattice matched to InP and grown at similar conditions has electron concentrations ranging from 1.2×10^{19} to 4.3×10^{19} cm^{-3} and mobility less than 2500 cm^2/Vs in this range of doping cell temperatures. This comparison suggests that the poly-InAs:Si has a doping-mobility product, and hence bulk conductivity, that is only 3-4 times lower than that of the lattice-matched InGaAs typically used as the capping layer in InP-based HBTs. This demonstrates that poly-InAs:Si may be a suitable material for use as an extrinsic emitter contact.

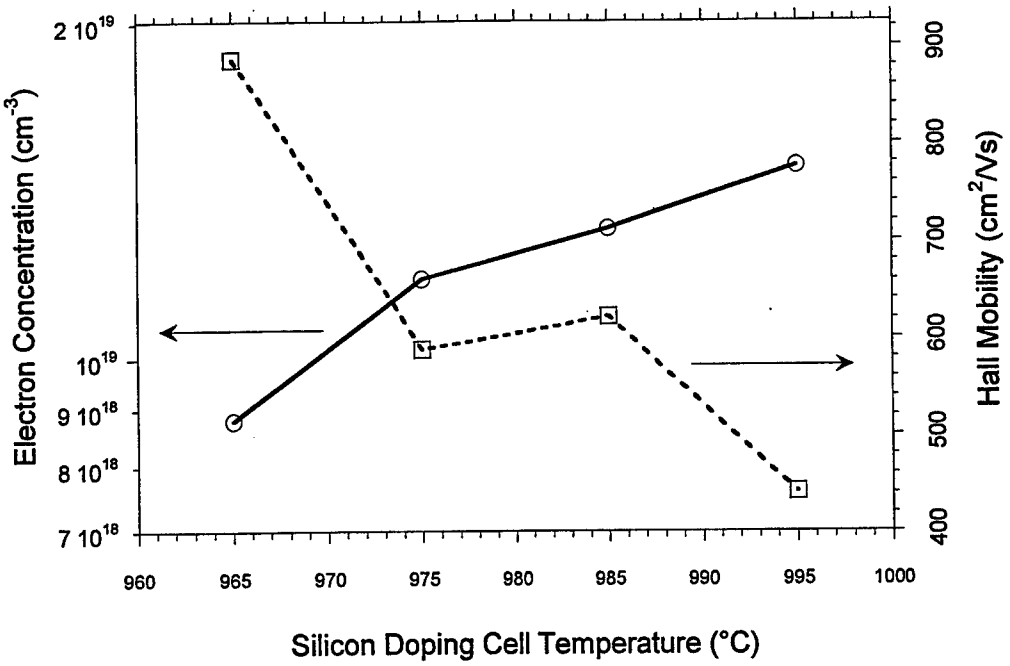


Figure 1. Doping cell temperature dependence of electron concentration and Hall mobility.

The dependence of electron concentration and mobility of the doped poly-InAs:Si on the substrate growth temperature is shown in Fig. 2. The substrate temperature was varied from 400-490°C while the Si doping cell temperature was maintained at 980°C for all of these growths. The growth rate was lowered to 0.21 μm/h for this series of growths to determine the effect of growth rate on the poly-InAs:Si material. As substrate temperature increases from 400-490°C, the doping decreases from 1.8×10^{18} to 8.1×10^{17} cm^{-3} and the mobility increases from 793 to 476 cm^2/Vs. This data suggests that the bulk conductivity is slightly higher for the lower growth temperatures.

Studies in poly-GaAs:Be report observations of increased resistivity with increased polycrystalline grain size [4,8]. The polycrystalline grain size was increased in the poly-GaAs studies by increasing the substrate growth temperature. The observed increase in resistivity was unexpected, as mobility is expected to increase with larger polycrystalline grain size and resistivity is expected to decrease. Although the mobility was found to increase with grain size in these reports, the hole concentration simultaneously decreased and lead to an overall decrease in the resistivity. To date, similar trends have not been observed in our poly-InAs:Si data. Increasing the growth rate from 0.21 to 0.71 μm/h is observed to strongly impact polycrystalline grain size and doping while having a minimal effect on the Hall mobility. The electron concentration shown in Fig. 1 (growth rate of 0.71 μm/h) is an order of magnitude higher than that shown in Fig. 2 (growth rate of 0.21 μm/h) at similar

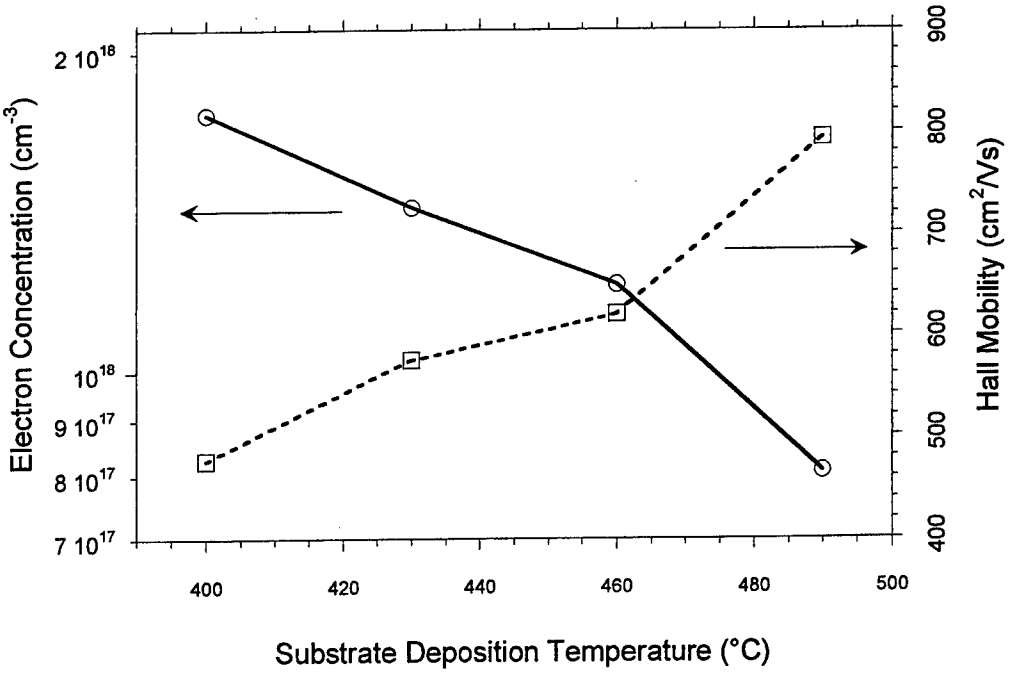
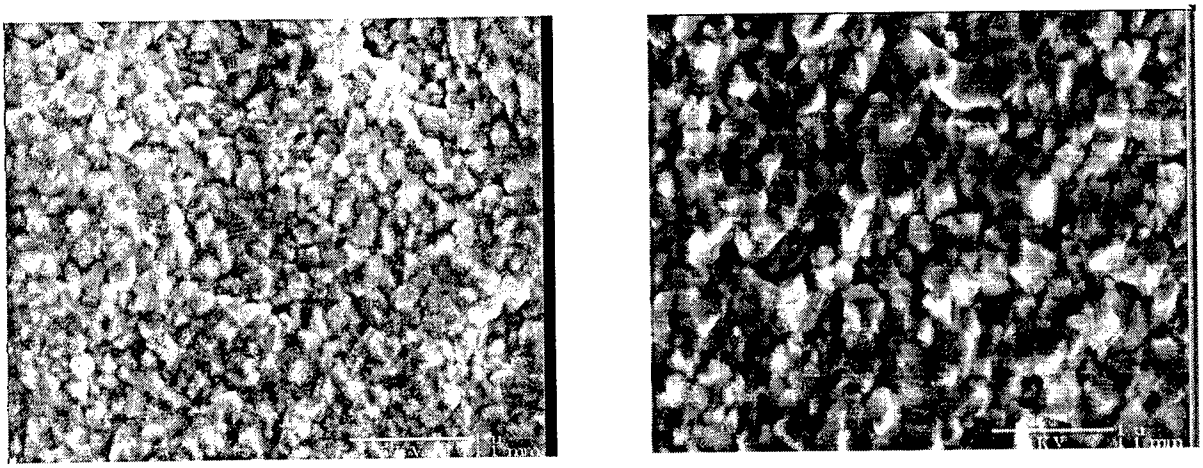


Figure 2. Substrate temperature dependence of electron concentration and Hall mobility.

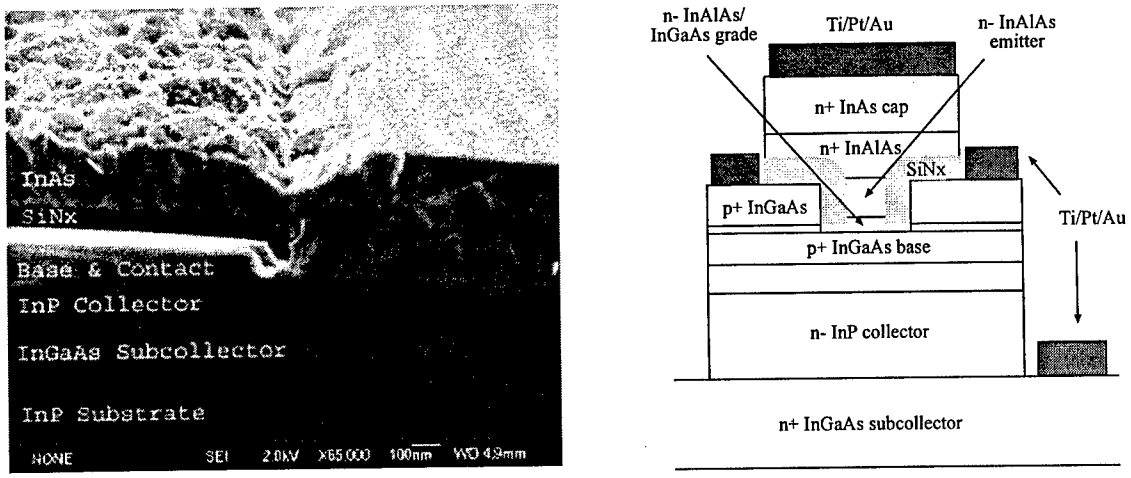
substrate and dopant cell temperatures. Figure 3 shows the typical surface morphology of the poly-InAs:Si at these growth rates. The SEM images show the material at the same magnification so the difference in the polycrystalline grain size and density may be compared. Figure 3(a) shows poly-InAs:Si deposited at a rate of 0.71 μm/h. The grain sizes in Fig. 3(a) are smaller than those grown at the lower rate, as shown in Fig. 3(b). A grain size of approximately 130 nm is obtained at the higher deposition rate, and the polycrystalline grains for the lower growth rate average about 190 nm in size. The poly-InAs:Si grain size is not observed to vary significantly in our data with variations in growth temperature.

TLM structures have been used to determine the bulk resistivity and contact resistance of the poly-InAs:Si. We have used the poly-InAs:Si as the emitter cap and extrinsic emitter contact in an HBT utilizing non-selective-area regrowth in the formation of the emitter-base heterojuction [6]. The HBT utilizes the poly-InAs as a low-resistivity emitter contact with an area larger than that of the base-emitter junction, allowing for low emitter resistance while shrinking the active base-emitter junction area. A cross-section of the base-emitter junction with the poly-InAs cap and a schematic of the transistor are shown in Fig. 4. The substrate temperature is set to 480°C during the poly-InAs:Si growth of the HBTs, and the growth rate is typically about 0.70 μm/h. The typical bulk resistivity is approximately 1.4×10^{-3} Ω-cm. Contact resistance to the poly-InAs with a Ti/Pt/Au metal stack less than 1.6×10^{-7} Ω-cm^2.



(a) (b)

Figure 3. SEM images of typical poly-InAs morphology when grown at (a) 0.71 μm/h and (b) 0.21 μm/h.



(a) (b)

Figure 4. (a) SEM cross-section of the regrown emitter HBT showing the polycrystalline regrowth (left) and the regrowth on crystalline material (right). (b) HBT schematic with poly-InAs emitter cap.

4. Conclusion

We report, for the first time, that low-resistance poly-InAs:Si can be achieved. The low-resistance polycrystalline material may be suitable in III-V HBTs for use as an extrinsic emitter contact in the non-selective regrowth of the emitter-base heterojuction. In addition, the material may also be useful in other III-V devices where low contact access resistance and low junction capacitance are desired.

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Acknowledgements

This work is supported by the Office of Naval Research (Contract No. N0014-99-1-0041)

EPITAXIAL TERNARY AND QUATERNARY III-V ANTIMONIDE SUBSTRATES

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Abstract: Modified liquid-phase epitaxy (LPE) techniques can be adapted for the growth of relatively thick (50 to 500 micron) epitaxial layers of ternary and quaternary III-V antimonide alloys, including InAsSb, InGaSb, AlGaAsSb, InGaAsSb, and InAsSbP. These structures can function as 'virtual' substrates with adjustable lattice constants for epitaxy of various optoelectronic devices such as mid-infrared photodiodes. A variety of substrate structures can be realized either by effecting gradual, continuous compositional grading of thick epilayers, or by growing multilayers with abrupt but incremental compositional changes between adjacent layers. Both approaches can be combined with selective removal of the seeding substrate and wafer bonding techniques. Low-defect alloy substrates with increased functionality, and with lattice constants and bandgaps significantly different than available with binary compound wafers (e.g., InAs or GaSb), appear feasible.

1. Introduction and Background

'Customized' substrates comprised of ternary and quaternary III-V compound alloys—in the form of either thick, self-supporting structures or else as epilayers transferred from the seeding substrate and bonded to a surrogate substrate—would enable much new device technology for mid-infrared optoelectronics. Such alloy substrates may also be useful for high-speed electronics. In particular, the III-V antimonide-based compound semiconductors (ABCS) have a wide range of band-gaps and valence or conduction band offsets in their heterojunctions, and extremely high electron mobilities. Consequently, the low-bandgap III-V antimonides are of increasing interest for infrared (2- to 12-micron wavelength) detectors, LEDs, and laser diodes; high-frequency (>100 GHz) analog, digital, and mixed analog / digital circuits with extremely low power consumption (< 1 fJ per operation) and low power supply voltage levels (< 1 V); and novel devices that operate in the THz to IR frequency range [1]. There is an acute need for improvements in substrate technology to facilitate epitaxial growth of these materials.

Compared to conventional elemental or binary compound substrates such as silicon or GaAs wafers—which are of invariant lattice constant and bandgap for a given temperature, alternative substrates made of ternary or quaternary alloys provide one or two extra degrees of freedom for 'tuning' the lattice constant and/or bandgap. The additional latitude in selecting the lattice constant and bandgap of the substrate would open up new device designs and applications that until now have been severely hindered by certain materials limitations. For example, the performance ranges of semiconductor detectors based on III-V antimonide alloys (e.g., InAsSbP, InGaAsSb, and AlGaAsSb) are limited by lattice-matching constraints, as epitaxial device layers should generally be closely lattice-matched (< 1%) to their substrate in order to avoid excessive defect levels. Thus, epilayer compositions that would nominally satisfy bandgap specifications for particular wavelength bands of operation are eschewed due to the inavailability of a substrate with the desired lattice constant. Lattice matching considerations are one of the most important criteria in formulating an epitaxy process, especially with regard to reducing threading dislocation concentrations; maintaining smoothness, thickness uniformity, and homogeniety of epilayers and avoiding corrugated surface morphologies; and controlling or exploiting strain effects that influence optical and electrical properties. The lattice mismatch between substrate and epilayer determines the critical thickness that delimits whether the epilayer is relaxed (with dislocations) or coherent (strained or pseudo-morphic), an aspect of growth which is especially important in quantum well or superlattice structures.

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In epitaxy of many III-V alloys, lattice matching constraints are further exacerbated by miscibility gaps that can preclude alloys with compositions (and bandgaps) prone to spinodal decomposition. Consequently, miscibility considerations may impose additional restraints on alloy compositions suitable for lattice-matched III-V semiconductor device designs. To a certain degree, lattice-matched epitaxial layers with compositions inside the miscibility gap can be stabilized against decomposition; the strain energy that a homogeneous layer incurs by separating into lattice-mismatched phases impedes decomposition. In many instances, a wider selection of substrate lattice constants would help circumvent limitations associated with miscibility gaps.

Semi-insulating substrates are useful for device isolation and for reducing substrate capacitance effects that can limit device speed. A significant drawback of the low-bandgap III-V antimonides is the lack of semi-insulating substrates, such as are available with GaAs and InP. The low bandgaps of InAs, InSb, and GaSb result in relatively high room-temperature thermal carrier generation, and consequent high substrate conductivity. On the other hand, substrates with wide bandgaps (>approx.1.3 eV) can be rendered semi-insulating provided the residual doping and certain background impurities are kept sufficiently low such that conductivity is dominated by intrinsic carriers. Close donor-acceptor compensation, control of electrically active defects and impurities such as oxygen, and/or the introduction of deep donor or acceptor levels can also increase resistivity. Nevertheless, the techniques used to produce very high resistivity in GaAs, InP, and GaP substrates have not been effective with GaSb, InAs, or InSb—or with Ge or Si for that matter. Thus, the growth of wide-bandgap antimonide alloy layers, especially compositions rich in AlSb (E_g = 1.5 eV), in combination with techniques for inducing semi-insulating behavior, may present a route for producing semi-insulating wafers suitable for lattice-matched growth of III-V antimonides. Some caution is warranted here, however, since the more complex field of defects in ternary and quaternaries may contribute to electrical conduction mechanisms that are difficult to control. A more promising approach for achieving substrate isolation is perhaps provided by wafer bonding techniques whereby an epilayer is transferred to an insulating surrogate substrate.

2. Some Prior Relevant Work on Alloy Substrates

As a general rule, the only readily available substrates are wafers sliced from ingots of bulk-grown elemental semiconductors (Ge and Si) or congruently melting, stoichiometric binary compounds (e.g., InAs, InSb, GaSb, GaAs, ZnSe, and SiC). The potential advantages of ternary and quaternary alloy substrates as discussed above have been appreciated for quite some time, and the production of new alloy semiconductor wafers has been an area of long standing interest with considerable potential applications [2-13]. "Bulk" photon or particle detectors with tunable bandgaps and optical absorption edges can be directly fabricated in such alloy substrates. Still, of much greater interest is the use of such alloy substrates for epitaxial growth of semiconductor device structures. As an example of a purely optical application, 2- to 3-mm thick plates of ternary and quaternary III-V antimonide alloys can be used as window materials with tunable optical absorption edges in mid-infrared laser protection schemes.

We note some limited successes in growing bulk ternary crystals of InAsSb, HgZnTe, and HgMnTe for certain composition ranges using the Bridgman-Stockbarger technique (directional melt freezing); or through solid-state recrystallization or zone melting growth of quenched or sintered charges [14]. Nevertheless, growth of ternary and alloy semiconductor is typically hampered by severe segregation effects, sensitivity of solid composition to fluctuations in growth temperature, and the high vapor-pressure of components resulting in evaporative losses and changes in melt composition. In spite of these difficulties, much effort has been directed toward making alloy substrates using adaptations of bulk crystal growth, such as Czochralski crystal pulling or horizontal boat directional solidification, from three-component melts to produce boules or ingots of the ternary alloy. This is reasonable since crystallization rates from the melt are sufficiently fast enough to grow large crystals that can be cut into free-standing wafers with thickness of 100 to 1000 microns. In contrast, vapor-phase or vacuum growth (e.g., CVD or MBE) is usually considered much too slow to achieve crystals with millimeter thicknesses. (However, there are some notable exceptions such as vapor-phase growth of bulk AlSb [15] and ZnS.)

While most semiconductor substrates are made by slicing wafers from boules grown from congruently-solidifying stoichiometric melts, the *epitaxial growth* of substrate wafers, either from the vapor-phase or from non-stoichiometric liquid solutions as will be described shortly, is not unprecedented. For example, commercial ultrabright light-emitting diodes utilize a 100-micron thick AlGaAs "transparent substrate" grown by liquid-phase epitaxy [16]. Moreover, SiC substrates are grown by what is essentially a vapor-phase sublimation process. Sumitomo, Inc. (Japan) is producing ZnSe wafers made by vapor-phase transport processes, and Crystal Photonics, Inc. (Sanford, FL) is developing a GaN substrate made by vapor-phase epitaxy. In general, however, the application of epitaxial growth methods for substrate production would normally be considered uneconomic due to the slow growth rates (< 0.1 to 1 microns /min) resulting in very low throughput. (Evidently, in the instances cited above the advantages gained by epitaxial growth with respect to material quality are so compelling that the slow growth rates are acceptable, and that at least for certain materials, a premium will be paid for high-quality substrates made by unconventional or specialized techniques.) Solution growth methods, specifically liquid-phase epitaxy (LPE), might also be dismissed as too slow for the practical growth of bulk crystals. LPE is usually effected by precipitation from a molten metal solution that is dilute in at least one component of the crystallized material. For instance, the LPE growth of AlGaAs occurs from Ga-rich solutions with As and Al concentrations on the order of 1 atomic-% and 0.01 atomic-%, respectively; and growth rates are typically in the 0.1 micron / min range. Nevertheless, there are at least several III-V antimonide alloy semiconductors where the LPE melt is relatively rich in all components. For example, for GaInSb solidified at ~550 °C the liquid-phase atomic fractions are X_{Ga} ~0.3, X_{In} ~0.5 and X_{Sb} ~0.2. These ternaries generally exhibit fast LPE growth rates (1 to 5 microns / min), and in such cases, the distinction between melt growth and solution growth is not sharp.

Thick (> 50 micron), low-defect, compositionally-graded epitaxial layers of ternary and quaternary alloys, termed "virtual substrates" by MAO and KRIER [17], would effectively satisfy many of the same specification objectives that are sought in substrate wafers sawed from ternary ingots. Assessment and applications of thick LPE layers, and specifically, the use of a thick continuously compositionally-graded single layer or step-graded multilayers, often in for low-bandgap III-V antimonide alloy detector or LED structures have been reported by several groups [18-23]. As mentioned, the seeding substrate can be selectively removed and/or the epitaxial layer can be transferred to an insulating surrogate superstrate, thus increasing its functionality for device applications benefiting from a transparent or electrically isolating substrate.

3. Technical Approach

Our approach is based on adaptations of liquid-phase epitaxy (LPE) technology for the production of so-called *virtual substrates*. These virtual substrates are essentially thick (> 100 micron), potentially self-supporting epitaxial structures of ternary or quaternary III-V antimonides grown from liquid-metal solutions by a modified LPE process. Multiple growths; i.e., separate LPE steps where the epitaxial structure is cooled to room temperature, removed from the LPE system, and used as a substrate for another LPE growth; are feasible. Each LPE step adds a layer and increases the total thickness of the stack. The associated compositional step-gradings at each growth interface contributes to the total lattice constant deviation from the binary substrate upon which the stack is seeded and supported. Epilayers are added until the desired lattice constant targeted for the ultimate top layer is achieved.

An overview of two basic but closely related options is shown in FIGURE **1**. A III-V binary compound substrate (e.g., InAs, GaSb, or GaAs) is used to seed the epitaxial growth of the virtual substrate. The epitaxial virtual substrate layer(s) can be transferred to a surrogate substrate, such as a semi-insulating GaAs wafer, using bonding and etching techniques already demonstrated or currently in development for silicon and other III-V semiconductors. Alternatively, if foregoing a bonded surrogate substrate, then the epitaxial layers of the virtual substrate are made sufficiently thick to be self-supporting and do not need the binary seeding substrate for mechanical support. In either case, the binary seeding substrate can be removed by post-growth selective or controlled etching, yielding a free-standing wafer of a ternary or quaternary alloy.

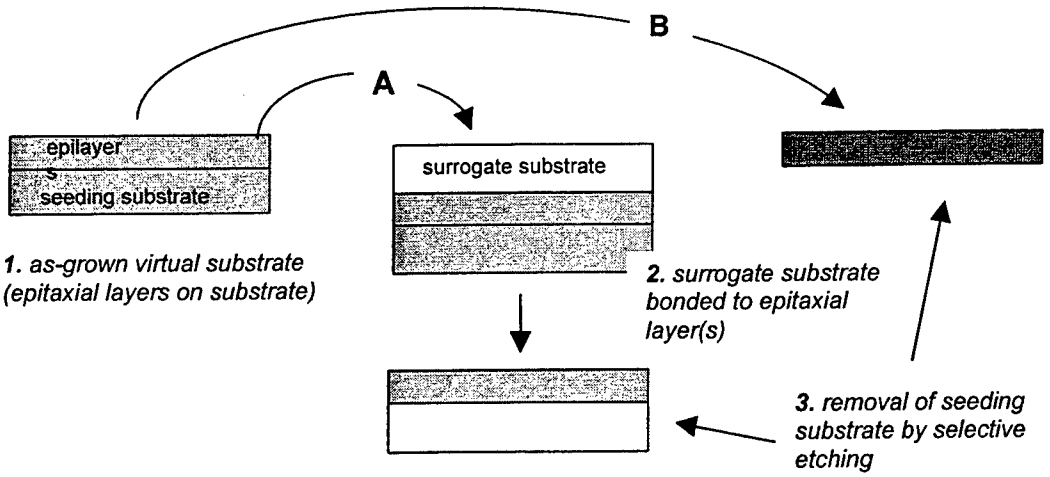


FIGURE 1: Options for virtual substrates: 1. epitaxial growth of thick multilayers on a binary compound seeding substrate (e.g., GaSb, InAs, InSb, or GaAs); Option **A**: 2. a surrogate substrate (e.g., semi-insulating GaAs, oxide-coated silicon, or a thermal-expansion matched insulating material is bonded to the exposed surface of the epitaxial layers, 3. which is then removed by selective etching. Option **B**: the epitaxial virtual substrate is grown sufficiently thick to be self-supporting, in which case, 3. the seeding substrate can be removed by etching.

4. Experiments and Results

An important advantage of the proposed work is the ability to make ternary and quaternary substrates with lattice constants significantly different than that currently available with the wafers of binary compound such as GaSb, InAs, InSb, and GaAs. By growing multiple layers with a small composition change and related lattice constant change (0.1 to 0.3 %) at each interface, the cumulative effect is an top layer alloy with a lattice constant significantly different than that of the binary seeding substrate. Thus, the bandgap in which a device is fabricated, or the lattice constant of the surface upon which a device structure is grown in a subsequent MBE or MOCVD epitaxy step can be parameterized over some range, hopefully without generating excessive defects. The change in lattice constant at each interface must be sufficiently small to maintain low densities of misfit dislocations [24]. Additionally, such thick LPE layers tend to "anneal-out" defects [25], which is an important advantage gained by the high growth rates inherent in LPE. Details of III-V antimonide LPE processes can be found in ref. [26] and references contained therein.

For the LPE we use a graphite slideboat technique in a horizontal, three-zone, resistively heated, 55-mm diameter fused-silica tube furnace. All of the systems are microprocessor-controlled and can be programmed with elaborate time-temperature schedules. The growth ambient is 1-atm pressure, Pd-membrane purified hydrogen with a flow rate of 30 ml/min. Growth temperatures are in the range of 400 to 650 °C. Upon contact with the melt, the substrate is ramp-cooled at a rate of 1 °C / min. Our research epitaxy normally uses 1 cm x 1 cm substrates, but substrate sizes up to 5 x 5 cm can also be used. Typically, such an LPE system is used for one epitaxy run per day, although two or three epitaxy experiments per system per day is feasible. One technician can operate as many as four systems simultaneously, and various heterostructures based on InGaAsSb, AlGaAsSb, InAsSbP alloys are routinely grown. Substrates are polished wafers of (100) oriented GaSb:Te and InAs:S and are obtained from a number of vendors including Firebird Semiconductor (British Columbia), MCP Wafer Technology (Milton Keynes, UK), Galaxy Compound Semiconductors, Inc. (Spokane, WA) and Princeton Scientific (Princeton, NJ). (111)-oriented GaSb wafers were used in some experiments. Pieces of these wafers were also used as source materials for the melts. All metals are six-9's purity obtained from Alfa Aesar (Ward Hill, MA) or Atlantic Metals & Alloys, Inc. (Stratford, CT). Prior to growth, metals are baked out for sixteen hours at a temperature of 100 °C above the highest growth temperature in flowing hydrogen to remove residual impurities and reduce oxides. In the

following, we present results for thick epilayer growths of several antimonide-based III-V alloys. The top surface(s) and cross sections of the epitaxial structures are characterized by optical, scanning electron, and atomic force microscopy, defect etching, energy-dispersive x-ray analysis, electron microprobe analysis, Raman spectroscopy, photoluminescence, and high-resolution x-ray diffraction.

4.1 Thick InAsSb LPE Layers

We first studied the characteristics of liquid-phase epitaxy of thick InAsSb layers on InAs substrates. The substrates are polished (100) oriented InAs wafers diced into 1-cm x 1-cm rectangles. We start with melt compositions (i.e., indium saturated with InAs) and growth temperatures that produce thick (> 200 micron) layers of InAs on InAs substrates, followed by experiments wherein the relative antimony content of the melt is increased incrementally with the objective to empirically determine the effect of increasing antimony content on growth characteristics. Although lattice mismatch is perhaps most important in determining the quality of growth, substrate dissolution, solute mass transfer in the melt, and effective supercooling are also contributing factors. We are able to grow InAsSb layers of several hundred microns on InAs substrates in a single LPE step by cooling In-As-Sb melts from 650 °C to 530 °C over a course of 2 hours.

4.2 Thick LPE Layers of InGaSb and AlGaAsSb

We have developed modified LPE techniques for the growth of thick, closely-lattice matched epilayers of InGaSb and AlGaAsSb. FIGURES **2** and **3** show cross-sections of >100-micron thick epilayers of $In_{0.04}Ga_{0.96}Sb$ on GaSb and AlGaAsSb on GaSb. This demonstrates that very thick layers of these III-V antimonide alloys can be grown by conventional methods of LPE. In many cases, LPE of alloy epilayers appears straightforward, however, in general such growth of a ternary or quaternary epilayer on a binary substrate is a complex process involving initial dissolution of the substrate (a binary substrate can never be in equilibrium with a 3- or 4-component melt), formation of an interlayer, solid-state diffusion, or changes in the saturation of the solution [27,28]. FIGURE **4** indicates an example of this behavior, showing a plot of growth thickness for several growth times (separate epitaxy experiments with varying growth times) for a ramp-cooling mode of growth (1 °C /min). Initially, there is melt back of the substrate ("negative" growth thickness) as the non-equilibrium conditions are relieved by dissolution of the GaSb substrate. After sufficiently long times, there is a net growth of quaternary alloy on the substrate. The growth rate then diminishes, and the epilayer attains an ultimate thickness. Such melt back and regrowth invariably results in rough interfaces. These effects are not inevitable and can be minimized by proper selection of melt composition and growth parameters (temperature, initial supersaturation, and ramp cooling rates). As Figure **3** demonstrates, a thick AlGaAsSb epilayer on a GaSb substrate with a smooth interface is attainable.

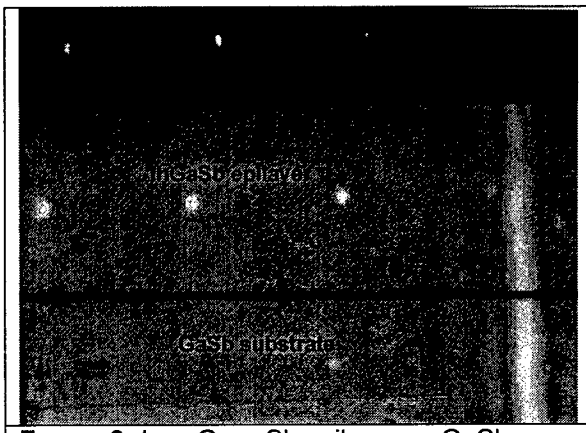


FIGURE 2: $In_{0.04}Ga_{0.96}Sb$ epilayer on GaSb substrate cross-section. Thickness of epilayer is 160 microns.

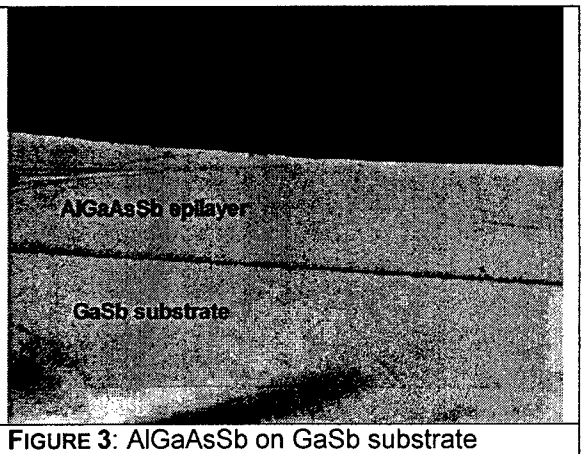


FIGURE 3: AlGaAsSb on GaSb substrate cross-section. (Epilayer is 200 microns thick. Ramp-cooling mode of growth).

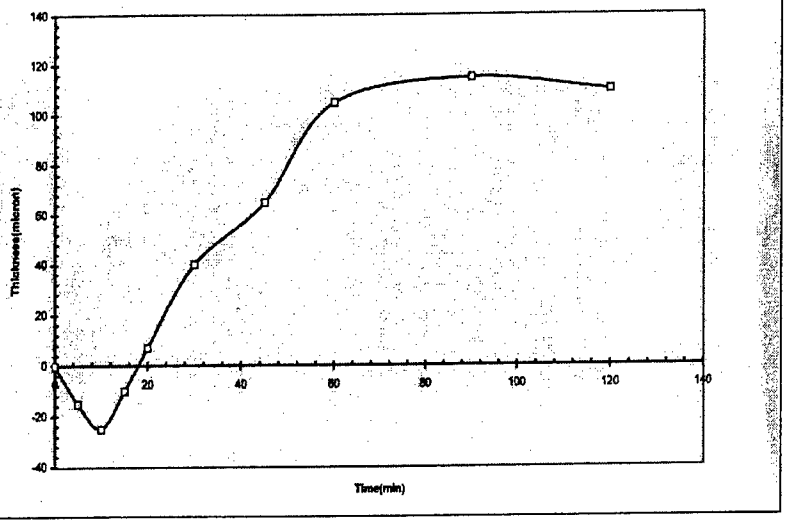


Figure 4: AlGaAsSb epilayer thickness as a function of contact time for growth on a (100)GaSb substrate. Growth solution is ramp-cooled at a rate of 1 °C/min from an initial temperature of 515 °C. Negative thickness corresponds to dissolution of the substrate ("melt back'). After sufficiently long times (≈20 mins), there is a net growth of the AlGaAsSb quaternary alloy.

4.3 Thick LPE Multilayers of InAsSb

Stacks of thick (> 50 μm) compositionally step-graded $InAs_{1-x}Sb_x$ layers on (100) InAs substrates, where x increases with each layer, are also feasible. To make such and similar structures, we found it was feasible and convenient to growth each thick ternary (or quaternary) layer in separate, successive LPE steps. For LPE of III-V antimonides, cleaning and surface preparation are evidently not overly critical for the success of these multi-step LPE processes: we can routinely and consistently use samples with epitaxial layers as substrates for subsequent LPE growth without surface cleaning or etching between growths. FIGURES **5a** and **5b** are cross-sections after the three-step growth of three InAsSb epilayers. Each layer has a successively higher antimony fraction. This is effected by increasing the relative proportion of antimony in the In-Sb-As melt. The melt compositions for the two samples for which stained cross-sections are shown in FIGURES **5a** and **5b** are summarized in TABLE **1**. All layers were grown at 650 °C for 120 minutes. Excess InAs in the form of a wafer floating on the melt was used as the source of arsenic. The step grading is dictated by the maximum abrupt lattice change at each growth interface that can be tolerated to maintain epitaxial growth and thus single-crystal layers (see refs. 24-26 for elaboration). If the difference in lattice constants of adjacent layers is too large, non-optimum nucleation is likely. On the other hand, higher antimony in the melt probably inhibits melt back of the underlying layer. This then suggests an optimum antimony fraction for each layer.

Each layer is approximately 100 microns thick so that the thickness of the composite structure (not including the substrate) is about 0.3 mm. The interfaces are smooth and abrupt. In the sample shown in FIGURE **5a**, the top layer is rough and polycrystalline. We interpreted this as due to excessive lattice mismatch between the second and third layer. We then reduced the amount of antimony in the melt used to grow the third layer (from 1.6 g to 1.53 grams). This resulted in a smooth third layer. Energy-dispersive x-ray spectroscopy (EDS) indicates the composition of the top layer is $InAs_{0.8}Sb_{0.2}$. X-ray diffraction indicates the layers are completely relaxed. The lattice constant difference between the top $InAs_{0.8}Sb_{0.2}$ and the InAs substrate is ≈1.5%.

The desired change in composition in step-graded LPE-grown structures raises the issue of lattice *pulling* or *latching*. In some systems, there is a tendency for a lattice-matched composition of the ternary or quaternary to grow in preference to the composition predicted by the phase diagram [25-27]. The stabilization of lattice-matched compositions against small changes in melt composition is advantageous in some applications. On the other hand, for step-graded, multilayer virtual substrates this phenomena might imply a minimum supersaturation and associated composition/lattice-constant step is required to overcome the tendencies of lattice pulling.



FIGURE 5a: Cross-sectional view of three layers of InAsSb on InAs substrate. Total thickness of three epilayers is ~0.3 mm.

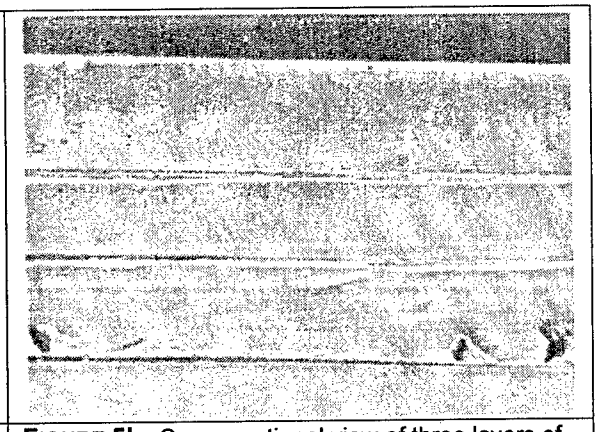


FIGURE 5b: Cross-sectional view of three layers of InAsSb on InAs substrate. Total thickness of three epilayers is ~0.3 mm.

TABLE 1: SUMMARY OF STEP-GRADED THREE-LAYER InAsSb GROWTHS (SHOWN IN FIGURES 5a AND 5b)

		Composite structure shown in FIGURE 5a	Composite structure shown in FIGURE 5b
top layer	indium in melt (g)	4.40	4.47
	antimony in melt (g)	1.60	1.53
	epilayer composition	$InAs_{0.8}Sb_{0.2}$	$InAs_{0.8}Sb_{0.2}$
	lattice mismatch	approx 1.5%	approx 1.5%
middle layer	indium in melt (g)	4.60	4.60
	antimony in melt (g)	1.40	1.40
	epilayer composition	$InAs_{0.85}Sb_{0.15}$	$InAs_{0.85}Sb_{0.15}$
	lattice mismatch	approx. 1.0%	approx. 1.0%
bottom layer (next to substrate)	indium in melt (g)	4.80	4.80
	antimony in melt (g)	1.20	1.20
	epilayer composition	$InAs_{0.93}Sb_{0..07}$	$InAs_{0.93}Sb_{0.07}$
	lattice mismatch	approx. 0.5%	approx. 0.5%

notes: melts are saturated with an InAs source; epilayer compositions determined by EDS or electron microprobe to approx. ±2 atomic percent resolution.

4.4 Multi-Layer LPE Growth of InGaSb, InGaAs, and InAsSbP

The cross-section of a two-layer $In_xGa_{1-x}Sb$ ($x \approx 0.05$) structure grown on a (100) GaSb substrate is shown in FIGURE 6. The InGaSb layers are grown in two separate LPE steps each at a starting ramp temperature of 500 °C. Similarly, two-layer InGaAs structures with a total epitaixal layer thickness of 0.25 mm were grown in two LPE steps both with starting ramp temperatures of 600 °C. Layers with thicknesses on the order of 100 microns require about 1 to 1.5 hours growth time. A cross-section of a three-layer stack of InAsSbP on an InAs substrate is shown in FIGURE 7. In this case, for each of the three LPE steps, the melt atomic fractions are $X_{In} = 0.589$, $X_{Sb} = 0.40$, $X_{As} = 0.01$ and $X_P = 0.00088$ and the growth temperature is 565 °C which yields an epitaxial layer with a composition of $InAs_{0.6}Sb_{0.2}P_{0.2}$. As before, in each successive LPE step we change the melt composition to effect a small lattice change at each interface, and again, in principle multiple LPE steps can be performed several times to achieve a desired lattice constant substantially different than the binary seeding substrate wafer (GaSb or InAs). The defect density of the last-grown epilayer of the stack will depend on the lattice constant steps and epilayer thicknesses.

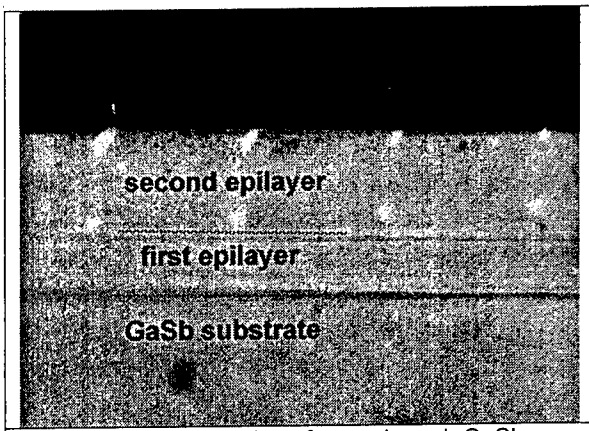


FIGURE 6: Cross-section of a two-layer InGaSb structure on a GaSb substrate. The total thickness of the layers is 250 microns.

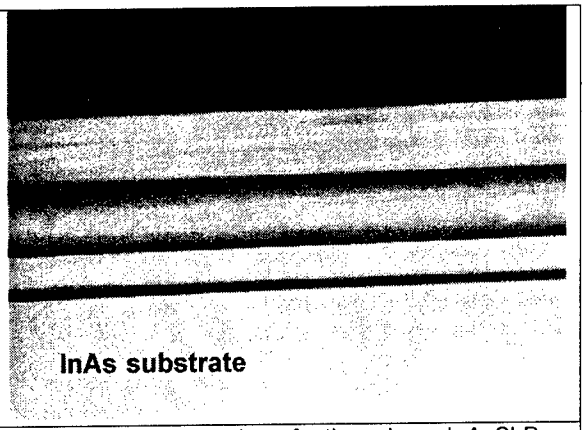


FIGURE 7: Cross-section of a three-layer InAsSbP structure on an InAs substrate. The total thickness of the layers is 150 microns.

The utility of step-graded ternary and quaternary alloy multilayers ofor virtual substrates is contingent upon the simultaneous achievement of two objectives: **1.** the lattice constant of the top layer should be significantly different than the underlying binary substrate upon which the first layer was seeded and this needs to be achieved in a reproducible and consistent manner with negligible variation over the entire area of the top layer, and **2.** the defect density due to misfit and threading dislocations must be sufficiently low (<< 10^3 or 10^4 cm^{-2}), preferably comparable to that of GaAs wafers. FIGURE **8** shows the high-resolution x-ray diffraction for a composite structure of two InAsSbP layers, each approximately 40 microns thick, on an (100) InAs substrate. The compositions of the LPE layers are adjusted to effect a modest lattice mismatch at each interface. Modeling indicates an approximate 2% lattice mismatch between the top InAsSbP epilayer and InAs substrate. FIGURE **9** is an atomic force microscope scan showing the exceptionally smooth surfaces produced by this LPE process: the root mean square roughness is ~0.2 nm. Defect etching studies on these layers indicate an etch pit density of less than 10^4 cm^{-2}.

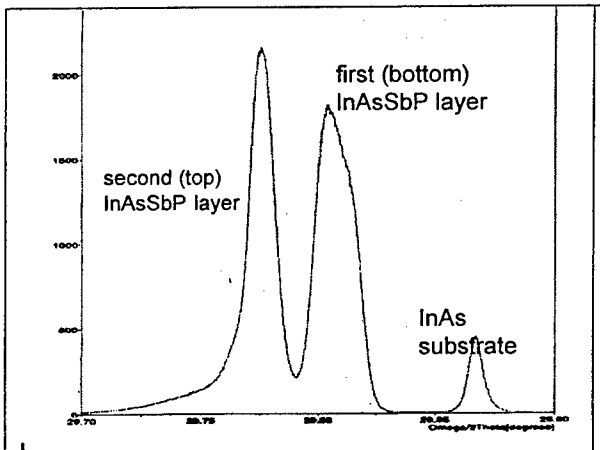


FIGURE 8: High-resolution double crystal x-ray diffraction peaks for a two layers of InAsSbP on InAs substrate, (004) peaks shown.

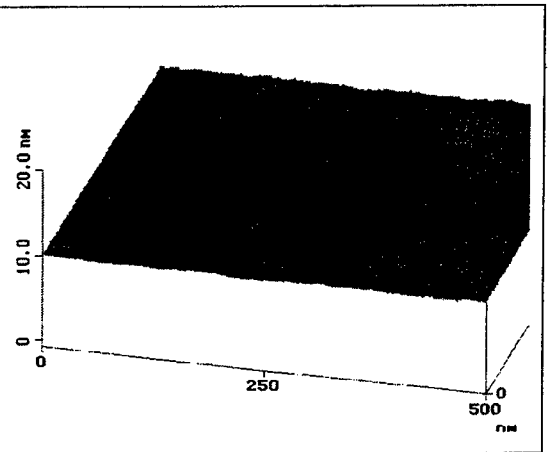


FIGURE 8: AFM suface profile of three layer InAsSbP/InAs structure similar to that shown in FIGURE **7**.

LPE-grown layers can be bonded to a superstrate such as, for example, a metal sheet, a glass slide, an oxidized silicon wafer, a semi-insulating GaAs substate, or a GaSb wafer coated with an insulating dielectric film. The binary seeding substrate can be removed by controlled and/or selective wet etching, and the resulting epilayer/surrogate substrate composite can be polished as needed. FIGURE **10** shows a top-view of a 20-micron thick InAsSbP epilayer bonded to a glass slide after the GaSb has been etched away. As an indication of the potential for a scaled-up implementation of these ideas, but demonstrated for AlGaAs rather than III-V antimonides, FIGURE **11** shows a 3-inch (75-mm) diameter, 50-micron thick, LPE-grown $Al_{0.5}Ga_{0.5}As$ epilayer (which is semitransparent) epoxied to a glass superstrate after the GaAs seeding substrate was removed by wet chemical etching. More sophisticated wafer bonding techniques could be applied to the structures described here. Some relevant related work in this area includes the demonstration of 100-GHz InGaAsP photodiodes formed on sapphire substrates [30]. A spin-on sodium silicate glass was used to bond InGaAsP /InP epitaxial structures to sapphire followed by removal of the InP substrate by wet etching.

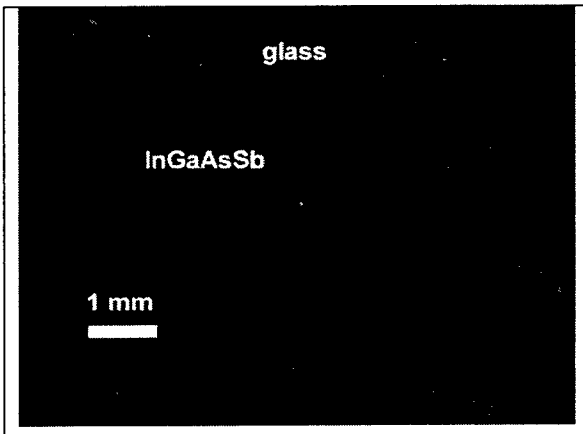


FIGURE **10:** 20-micron thick InGaAsSb epilayer bonded to a glass superstrate with GaSb substrate removed by wet etching. (See text for description).

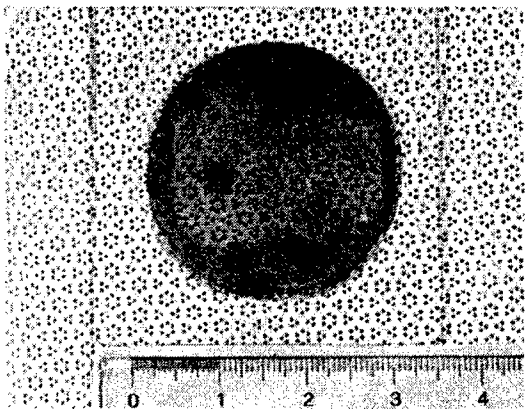


FIGURE **11:** 75-mm diameter, 50-micron thick $Al_{0.5}Ga_{0.5}As$ epilayer bonded to glass superstrate. (GaAs seeding substrate removed.)

5. Summary and Discussion

Liquid-phase epitaxy techniques can be used to produce thick (50 to 500 micron) layers of ternary and quaternary alloys including InAsSb, InGaSb, AlGaAsSb, InGaAsSb, and InAsSbP. LPE of the III-V antimonides exhibits remarkably high growth rates (1 to 10 microns / min), thus making very thick layers feasible. Using gradual- or step-compositional grading, low-defect layers with lattice constants and bandgaps significantly different from the binary substrate on which the thick layer(s) are seeded can be achieved. Additionally, the thick epitaxial layer can be bonded to a surrogate (insulating) substrate and the seeding binary compound substrate can then be removed by selective etching, yielding a semiconductor-on-insulator structure. These techniques are applicable to a practically all III-V compound alloys that can be grown by LPE and are sufficiently versatile to enable a wide assortment of structures suited for various device applications. The most profitable near-term applications appear to be mid-infrared detectors. These devices will also serve as excellent test structures to evaluate material quality. We are currently exploring alternative LPE methods, such as piston-boat techniques [31] for making virtual substrates. Although the customized substrates described here will cost more than commercially available wafers, e.g. GaSb or InAs, we believe they will be considerably less expensive than some recently developed niche substates such as SiC or GaN wafers, and further, the added cost of III-V antimonide virtual substrates will be justified by improved performance and new regimes of device operation for mid-infrared optoelectronics.

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Evaluation of Interfaces in Narrow InAs/AlSb Quantum Wells

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Abstract. InAs/AlSb quantum wells may be grown with two types of interfaces: InSb-like and AlAs-like. The interface type refers to the half-monolayer of the well material and half-monolayer of barrier which are in contact. The type and quality of the quantum well interface is critical to the ISBT intensity and lineshape and, to a lesser extent, position. In addition to FTIR spectroscopy of the ISBT, we have performed transmission electron microscopy (TEM) to directly evaluate the quality of the interfaces at the atomic level. In order to evaluate the effects of interface type and quality on ISBT intensity, lineshape, and linewidth, we studied the TEM of a 10 nm QW sample with InSb-InSb interfaces and a 3 nm QW sample with InSb-AlAs interfaces.

1. Introduction

Quantum structures made from the 6.1-Å family of III-V compounds – InAs, GaSb, and AlSb – provide an ideal playground for the quantum engineering of electronic energy levels and wavefunctions due to their interesting band-edge alignment. In particular, the extremely large conduction band offset between InAs and AlSb (~2 eV) is promising for highly sophisticated architecture of multi-level systems with tailored transition energies and matrix elements. We are investigating the short-wavelength limit of intersubband transitions (ISBTs) achievable in InAs/AlSb quantum wells.

We have investigated ISBTs and photoluminescence (PL) in InAs/AlSb multiple quantum wells (MQWs) of 20 periods with well widths ranging from 2.1 nm to 10.5 nm. The ISBT absorption energy increased with decreasing well width and ISBTs disappeared in wells narrower than 7 nm; the PL energy decreased with increasing well width and PL disappeared in wells wider than 6 nm. In other words, PL and ISBTs are mutually exclusive. Also, we found that the ISBT absorption linewidth of the 10 nm InSb-AlAs interfaces QW sample is much wider than the 10 nm InSb-InSb interfaces one.

Since one of our goals is to explore the short-wavelength limit of intersubband transitions, which is expected in narrow InAs wells, finding out the reason for the disappearance of ISBTs in the narrower wells is extremely important. There are three possibilities:

- The ISBT absorption intensity in narrower wells is too small to be observed. This is unlikely to be the cause because we compared the absorption intensity of 7, 8, 9 and 10 nm wells and found that the absorption intensity of the narrower wells was not significantly smaller than the wider wells.

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• The ISBT absorption is masked by another type of absorption, for example, interband absorption. This situation is possible for the 6 nm QW, in which PL and ISBTs are predicted at about the same energy. But for even narrower QWs, the intersubband transition energies should be significantly larger than the interband transition energies, therefore they should not overlap and mask each other.
• The ISBT absorption peak is so broad that the peak height is too small to be observed. It is well known that interface roughness is the major contributor to ISBT linewidth, and broadening due to interface roughness is more pronounced in narrower wells. In order to test the hypothesis that the ISBT is too broad to be observed in narrow wells due to interface roughness, we have made TEM images of wide and narrow wells.

2. Sample growth

The samples were grown by molecular beam epitaxy (MBE). Before growth, the GaAs substrates were thermally cleaned at 630 °C for 30 minutes in an As_4 atmosphere. Buffer layers consisting of 10 nm AlAs, 1000 nm AlSb and 15 periods of GaSb (6 nm) / AlSb (6 nm) superlattices were grown at 550 °C. These buffer layers are used to change from the lattice constant of GaAs (0.56 nm) to that of GaSb (0.60 nm). After the growth of buffer layers, InAs/AlSb MQWs were grown at 420 °C. Finally, GaSb was grown as a cap layer.

The InAs/AlSb MQW interface types can be controlled by the growth sequence and are expected to affect the band structure [1]. Two types of interface are possible: InSb-like and AlAs-like. Yano et al. have reported that the low temperature PL intensities of InAs/AlSb QWs with InSb-type interfaces were much stronger than those with AlAs-type [2]. For comparison, two types of interfaces were grown: InSb-like on both sides of the QW, and AlAs-like from InAs to AlSb and InSb-like from AlSb to InAs (Figure 1).

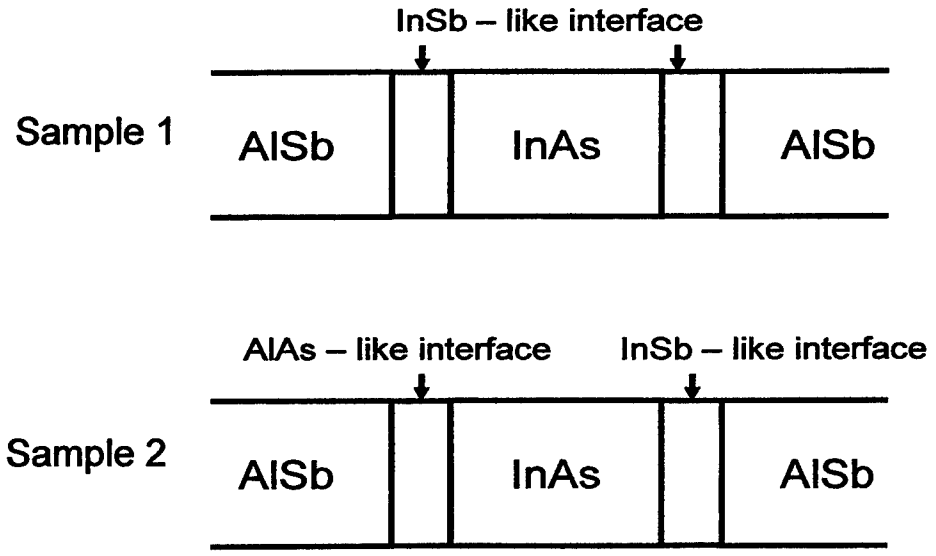


Figure 1. Two samples studied: InSb-InSb interfaces and InSb-AlAs interfaces

3. TEM sample preparation

To evaluate QW interfaces using TEM, the sample must be less than 10 nm thick (the penetration distance of electrons). The sample preparation process will be described in detail in this section.

The first step is to build a stack. Two InAs/AlSb MQW samples are glued face to face using M-bond 600/610 to increase the viewable quantum well area, and two silicon dummy pieces are attached to make the stack stronger. Then the stack is cured at 170°C for an hour. The stack is thinned to 100 μm using a hand polisher. An optical microscope is used to check the stack thickness.

The second step is to reduce the sample thickness to 10 μm using a dimple grinder. The dimple grinder has two major parts: a diamond dimpling wheel and a thickness measuring system. The effect of dimpling is to produce a thin central region on the sample stack while leaving a thick, supporting rim which protects the sample stack from damage.

The last step of sample preparation is ion-milling, which further reduces the sample thickness. The sample is glued on a copper grid and put in an ion mill. Argon ion guns, tilted at 15° to reduce sputter damage, hit the center of the sample. The rate of thickness reduction with ion-milling is much slower than with mechanical processes. Ion milling is continued until a hole appears at the QW edges and the region around the hole has a thickness of approximately 10 nm, which is good for TEM analysis.

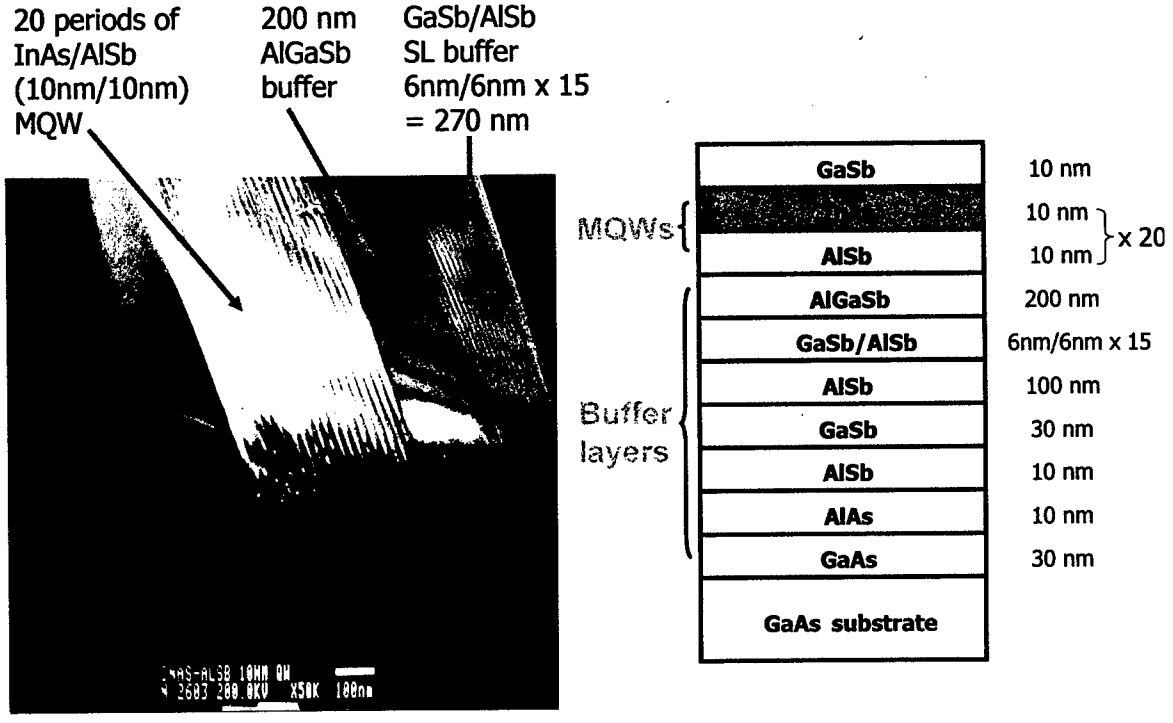


Figure 2. Left: micrograph of sample cross-section taken at 50K magnification. Right: Detailed 10 nm QW sample structure.

4. TEM analysis

We studied the TEM of a 10 nm InSb-InSb interfaces sample (Sample 1) and a 3 nm InSb-AlAs interfaces sample (Sample 2). Figure 2 shows a micrograph of the cross-section of the 10 nm InSb-InSb interfaces sample. It was taken at relatively low magnification (x 50K) to see the entire sample cross-section. The MQW region is clearly visible, along with the AlGaSb and GaSb/AlSb superlattice buffer layers. Then we looked at the QW regions using a higher magnification.

Figure 3 shows a micrograph of 10 nm InSb-InSb interfaces sample taken at 1M magnification. We can see that the interfaces are flat, parallel to each other and in good shape. The dark material is InAs and the bright material is AlAs. Figure 4 shows a micrograph of 3 nm InSb-AlAs interfaces sample taken at 1M magnification. We can tell that the interfaces are not flat and the InAs layers have different thicknesses. The InSb-InSb interfaces sample has better interface quality than InSb-AlSb interfaces sample. This finding is in agreement with our ISBT results: the ISBT absorption linewidth of InSb-AlAs interfaces sample is much wider than the absorption linewidth of InSb-InSb interfaces sample of the same well width.

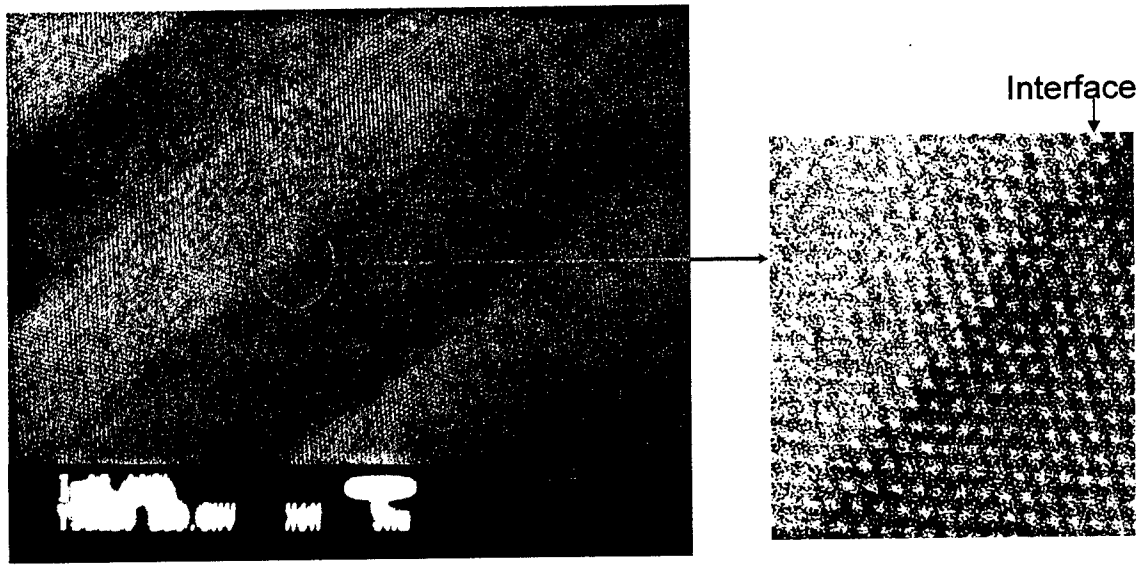


Figure 3. Left: Micrograph of 10 nm InSb-InSb interface sample taken at 1M magnification. Right: Detail of micrograph on the left at 8 times magnification.

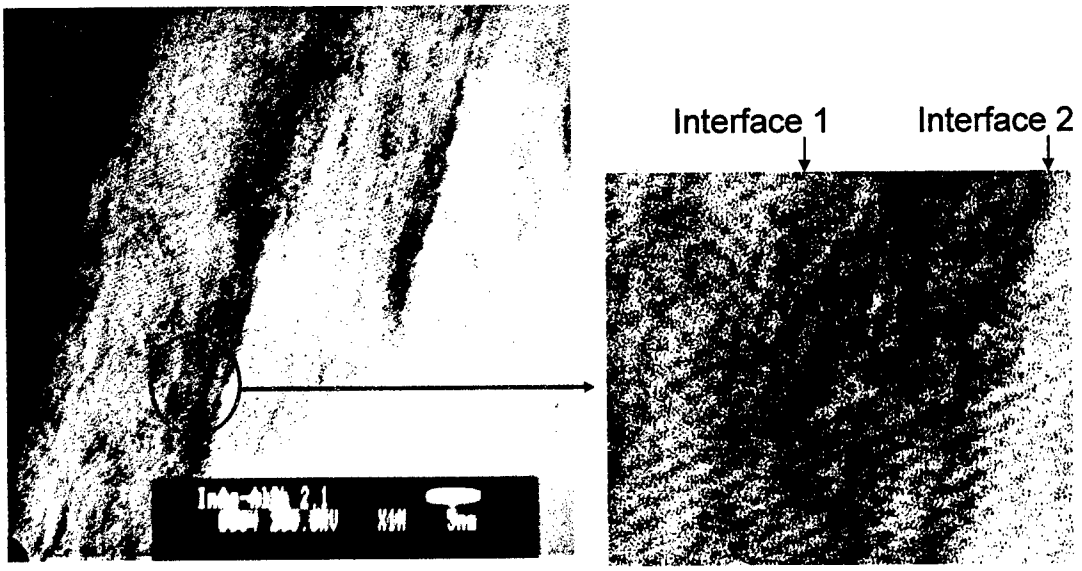


Figure 4. Left: Micrograph of 3 nm alternating interfaces sample taken at 1M magnification. Right: Deatail of the micrograph on the left at 8 times magnification.

5. Conclusion

We have taken TEM micrographs of InAs/AlSb quantum well samples with both interfaces InSb-like and with one interface InSb-like, one AlAs-like. The interface quality of the InSb-InSb sample is much better than the InSb-AlAs sample, which is in agreement with the wider ISBT absorption linewidth of InSb-AlAs samples.

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Picosecond Time-Resolved Cyclotron Resonance Study of InSb Quantum Wells in a Quantizing Magnetic Field

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Using two-color pump-probe spectroscopy in a magnetic field, we have measured the time-resolved cyclotron resonance of photogenerated transient carriers in undoped and doped InSb quantum wells. We used an intense femtosecond pulse of near-infrared (NIR) radiation from a Ti:Sapphire-based regenerative amplifier to create a large density of non-equilibrium carriers, which modifies the transmission of a delayed pulse of far-infrared (FIR) radiation from a free-electron laser. We monitored the dynamics of FIR transmission while varying the magnetic field and the time delay between the NIR and FIR pulses. Our data clearly show that the average electron cyclotron mass decreases as the electrons relax towards the band edge, as expected from the strong nonparabolicity of the InSb conduction band. Detailed lineshape analysis combined with Landau level calculations allowed us to determine the time evolution of the Fermi-Dirac distribution function of non-equilibrium two-dimensional carriers in a quantizing magnetic field.

Two-dimensional electron gases (2DEGs) in narrow-gap semiconductors in high magnetic fields show a rich varieity of quantum phenomena due to their small effective masses and large g-factors, which lead to extremely large Landau and Zeeman quantization. These quantized, atomic-like energy levels not only give rise to pronounced quantum oscillations in electron transport properties but also provide a tunable, multi-level system in which to investigate the quantum dynamics of charge and spin carriers [1]. However, there have been very few studies that directly probe carrier dynamics in a 2DEG in the time domain [2–4] with ultrashort and/or intense terahertz (THz) or far-infrared (FIR) pulses.

We have studied the picosecond time-resolved cyclotron resonance (TRCR) of photogenerated electrons in undoped and modulation-doped InSb quantum wells (QWs). TRCR is a new spectroscopic method for studying intraband carrier relaxation in a magnetic field [3, 5] which allows us to monitor directly the effective mass of relaxing carriers as a function of time. In our two-color experiement, high energy transient carriers are created using an ultrashort near-infrared (NIR) pulse, and the subsequent dynamics are probed by a delayed FIR pulse.

InSb, with its small effective mass and large g-factor, is a natural candidate for TRCR measurments. InSb's strongly energy-dependent mass and g-factor provide a mechanism for CR to expose the electron energy distribution, which evolves in time. Unlike earlier TRCR work [3, 5], which studied bulk semiconductors, carrier diffusion in the light propagation direction can be ignored in QWs due to confinement.

We studied two samples, undoped and doped InSb QWs. The undoped sample was a multiple QW structure, containing 25 periods of 35 nm InSb wells separated by 50 nm thick $Al_{0.09}In_{0.91}Sb$ barriers, grown by molecular beam epitaxy on a semi-insulating (001) GaAs substrate. In order to eliminate any effects of photoexcited carriers in the substrate, it was etched away. The doped sample consisted of a single 30 nm InSb QW with $Al_{0.09}In_{0.91}Sb$ barriers.

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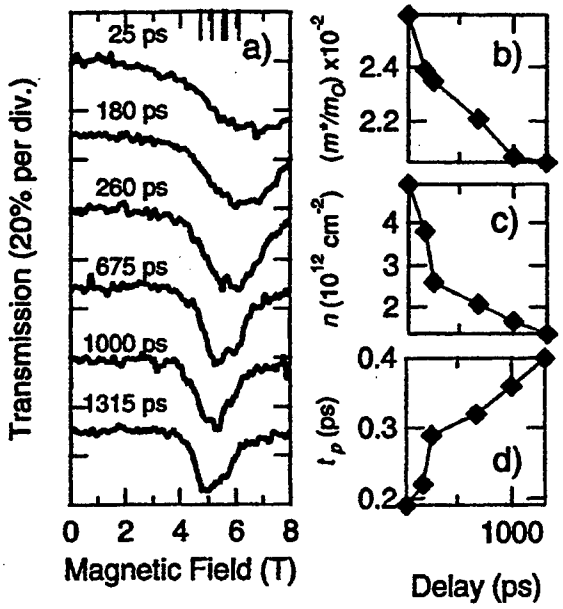


FIG. 1: (a) Transmission change of the FIR probe pulse for the undoped sample at 1.5K as a function of magnetic field at different time delays. The probe wavelength was 42 μm and the NIR fluence was $\sim$1.3 mJ/cm^2. (b) Carrier density vs. time delay. (c) Average cyclotron mass vs. time delay. (d) Average scattering time vs. time delay.

The sample had an electron density of 2×10^{11} cm^{-2} and a mobility of 100,000 cm^{-2} at 4.2 K. The sample growth procedures and basic sample characteristics have been described previously [6]. Because of the lattice mismatch between the well and the barrier materials ($\sim$0.5%), the wells were under compressive strain.

The experimental setup for the two-color TRCR spectroscopy of this work was similar to what was used in [3, 5, 7]. The FIR source was the Stanford Picosecond Free Electron Laser (FEL), which was tunable from 3 to 80 μm and emitted a transform-limited and diffraction-limited pulsed beam with durations between 600 fs to 2 ps and energies as high as 1 μJ. The NIR source was a Spectra Physics Tsunami Ti:Sapphire laser seeding a regenerative amplifier (Positive Light Spitfire) with the wavelength fixed at 800 nm during the experiment. The FIR and NIR beams were combined by a Pellicle plate and then focused onto the sample, which was placed in an 8 Tesla Oxford Instrument Spectromag 4000 with sapphire cold windows and polypropylene room temperature windows. The measurements were performed in the Faraday geometry at three FIR wavelengths (46, 42 and 38.5 μm). The FEL produced millisecond macropulses at 10 Hz, which contained picosecond micropulses at 11.8 MHz. The Ti:Sapphire oscillator was locked at the 7th harmonic of the FEL micropulse repetition rate, i.e., 82.6 MHz, and our synchronization electronics allowed us to obtain one NIR pulse from the regenerative amplifier for every FIR macropulse. A liquid-helium-cooled Ge:Ga photoconductive detector was used to collect the FIR beam transmitted through the sample.

Typical B-scan data for the undoped sample are shown in Fig. 1(a) for six different fixed delays and a NIR pump fluence of $\sim$1.3 mJ/cm^2. These traces show the evolution of CR over time scales much shorter than the interband lifetime which suggests the effects seen here are the result of intraband processes. At 25 ps after excitation, the CR line is significantly broadened to higher B, i.e., to heavier effective mass. At longer delay time, the electrons relax towards the band edge, resulting in a lighter mass with a more or less symmetric lineshape at 1.3 ns. The average cyclotron mass, carrier density, and average scattering time, obtained through Lorentzian fits [8] to the traces in (a), are plotted against delay in Figs. 1(b), 1(c), and 1(d), presenting the CR dynamics stated above more quantitatively. The fits take into account the presence of multiple sharp CR lines within the broad resonance observed. This approach is justified by the Landau level calculation and confirmed by the TRCR simulation (see later). In Fig. 2, TRCR spectra at different time delays are shown for three different NIR fluences. We should mention that the magnetic field width corresponding to the finite spectral width of the FEL pulse ($\Delta B \approx 0.087$ T, using $0.025m_0$) is much smaller than the width of any of the resonances we observe.

In order to predict the positions of the CR transitions, we modeled the system with a magnetic field applied along the growth direction [001] using a modified Pidgeon-Brown model [9, 10]. In this model, the bulk energy gap is

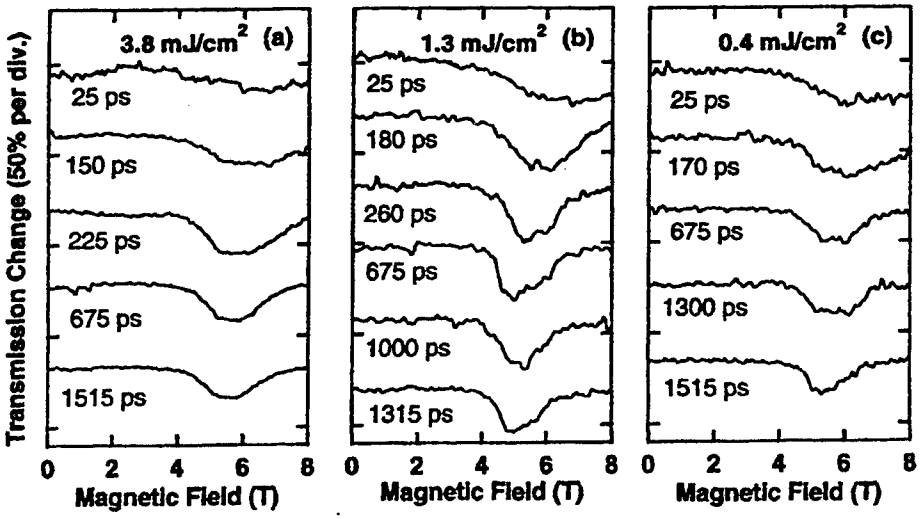


FIG. 2: Transmission change of the FIR probe pulse as a function of magnetic field for different NIR powers and time delays. The probe wavelength was 42 μm.

replaced by the effective band gap in the quasi-2D structure, i.e., the energy separation between the lowest subband in the conduction band and the highest subband in the valence band. Several calculated low-lying conduction band Landau level transitions for an FIR wavelength of 42 μm are shown in Fig. 1 as black bars. The calculated energy levels strongly suggest that the TRCR lines we observe consist of multiple transitions.

Based on the above considerations, we performed a detailed simulation of the TRCR spectra obtained for 42 μm probe light and a NIR fluence of $\sim$1.3 mJ/cm^2, as shown in Fig. 3. The fixed parameters in the simulation were the calculated B positions of the CR transitions and, at each time delay, the carrier density, which accounts for carrier recombination, and scattering time, both taken from fits as in Fig. 1. The variable parameter was the temperature of the Fermi-Dirac distribution of the excited carriers. We neglected continuum states above the barrier energy and many-body effects such as band gap renormalization. We took into account the reduction in CR-active population that occurs when the upper level of a transition is populated. The results accurately reproduced the main observed features, which arise from the strong nonparabolicity of the InSb conduction band. Namely, the initially excited carriers, having a Boltzmann-like distribution with a high carrier temperature, populate some states with high Landau indices, where the cyclotron masses are higher than that of the lowest electron Landau level. This is the main cause for the significant initial broadening (inhomogeneous broadening). As time progresses, the electrons relax towards the lowest Landau level, and, as a result, the number of transitions contributing to the observed linewidth decreases in time. At the same time, the linewidth of individual CR transitions decreases with time, as is obvious from the simulation. This indicates that each energy level is initially broadened due to the high scattering rate in the high density and high temperature regime (homogeneous broadening). As time progresses, both the electron temperature and density decrease, making individual transitions narrower.

TRCR spectra for the doped sample as a function of magnetic field at different time delays are shown in Fig. 4. The CR peak position is significantly shifted to higher magnetic fields compared to the undoped sample, which we believe is due to the Pauli blocking of the low-lying Landau levels by the carriers provided by the donors as opposed to the photogenerated carriers. The expected CR transitions inside the 30 nm QW are indicated as black arrows in Fig. 4. The intense NIR pulse, in this case, is expected to not only create additional photogenerated carriers but also raise the temperature of the 2DEG. We thus believe that the subsequent dynamics is mostly domonated by the change of the carrier distribution (i.e., cooling) rather than carrier density decrease due to recombination. Our preliminary calculations suggest that the relevant Landau levels in the first subband are fully populated and the CR peak we are seeing is probably due to CR in the second subband. In addition, we found that at these resonance magnetic fields the final states of the CR transitions in the second subband are out of the well, i.e., bulk like. We are currently performing more detailed calculations and analyses to understand this intriguing physical situation better.

In summary, we performed picosecond two-color (NIR and FIR) TRCR spectroscopy on undoped and doped InSb quantum wells. We monitored the dynamics of FIR transmission while we varied the magnetic field and the time delay between the NIR and FIR pulses. Our data clearly showed that the average electron cyclotron mass decreases as the

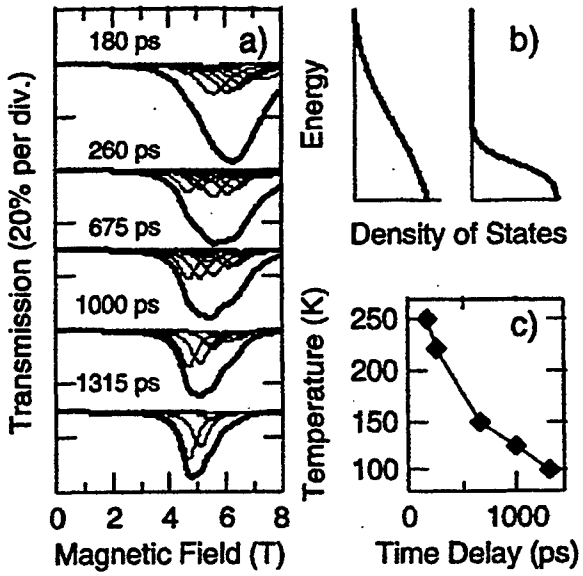


FIG. 3: (a) Simulated transmission change of the FIR probe pulse as a function of magnetic field at different time delays. The thin traces are the single-particle CR transitions and the thick traces are their sum. (b) Cartoon of (left) hot, high density Fermi distribution and (right) cold, low density Fermi distribution. (c) Simulated carrier temperature as a function of time delay.

electrons relax towards the band edge, which behavior is due to the strong nonparabolicity of the InSb conduction band.

J.K. gratefully acknowledges support from NSF DMR-0049024, DMR-0134058 (CAREER), DARPA MDA972-00-1-0034, ONR N00014-94-1-1024, the Japan Science and Technology Corporation PRESTO Program, and the NEDO International Joint Research Grant Program. M.B.S. thanks NSF for support through DMR-9973167 and DMR-0080054. We are grateful to H. A. Schwettman, T. I. Smith, R. L. Swent, T. Kimura and G. A. Marcus for their technical support during this work at the Stanford Picosecond Free Electron Laser Center.

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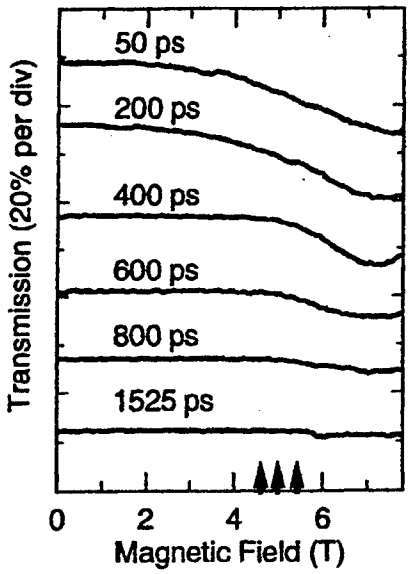


FIG. 4: Transmission change of the FIR probe pulse for the doped sample at 1.5K as a function of magnetic field at different time delays. The probe wavelength was 42 μm and the NIR fluence was $\sim$3 mJ/cm^2.

Monte Carlo Simulation of InGaAs/InAlAs HEMTs with a Quantum Correction Potential

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Abstract

In Monte Carlo simulation of high electron mobility transistors (HEMTs), how to position the source and drain contacts will significantly affect the drain current. Unlike many Monte Carlo (MC) simulations of HEMTs in the past, in this work, the source and drain contacts are placed on the top of the caps as in the real device instead of on the side adjacent to the channel. In addition, to take quantum effects into consideration, the effective potential approach of quantum correction has been incorporated into our MC simulator. We have found that the simulated drain current is substantially increased compared to that of using the classical potential.

I. Introduction

HEMTs have been extensively used in high-frequency applications, such as high power and low noise amplifiers. Due to expensive cost of processing HEMTs, it is desirable to predict their performance by simulation and by doing so to improve their design parameters. However, most existing simulators which use drift-diffusion (DD) or hydrodynamic (HD) model are not able to simulate complicated heterostructures with sufficient accuracy. Although some HD simulators [1][2] are capable of producing results which agree with the experimental data well, often a silicon-like mobility model is used in the simulation and extensive parameter adjustment is required. The alternate simulation tool is the ensemble Monte Carlo (EMC) method which does not require assumption of the mobility model. This approach is employed in this work for the simulation of HEMTs.

In most reported Monte Carlo (MC) simulations of HEMTs [3][4], the drain and source contacts are extended down to the channel as shown in Fig.1 (a). In this case, most electrons drift from the source end of the channel to the drain end and are collected by the extended drain contact without crossing the heterojunction, as indicated by the dotted line. However, in a real device, the Ohmic contact is placed on the top of the cap layers as shown in Fig. 1(b) where the typical electron flow path is indicated by the dotted line. Our two

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dimensional self-consistent MC simulation shows that if the top contacts are used, the drain current I_D predicted by the MC method is much smaller than the experimentally measured data. This observation is also confirmed by Simlinger et al. using the DD model [5]. The

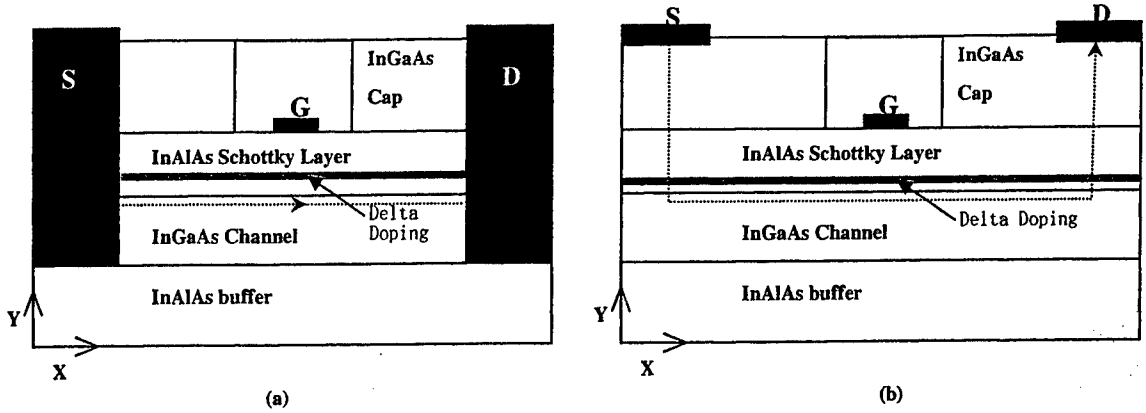


Fig. 1 The structure of HEMT (a) with contacts extended into the channel. (b) with contacts on top of the caps.

main reason for this is that the particle injection scheme at the contacts plays an important role in the simulation. We have found that if particles are injected into the device in order to maintain the charge neutrality near the Ohmic contacts, use of an injection scheme according to the weighted Maxwellian distribution [6] rather than the hemi-Maxwellian distribution [7] will increase the drain current by approximately 20 percent. In addition, in the classical transport model, only the thermionic emission is considered for the real space transfer. It is well known that the quantization effect in the channel and the tunneling effect across the Schottky layer must be taken into account for realistic HEMT simulation. This is usually implemented by solving the Shrödinger equation coupled with the Poisson equation. However, this approach is very time consuming, especially for self-consistent ensemble MC simulation. Therefore, some alternative methods are adopted by many researchers, such as the field assisted barrier lowering [1][5] and the non-local Schottky contact model [2].

II The Effective Potential Method of Quantum Correction

In recent years, the effective potential (EP) approach has been established as a viable alternative to the solution of Schrödinger equation for incorporating certain quantum effects. In the original paper by Feynman and Kleinert [8], the EP was used to study bounded carriers in a symmetric anharmonic oscillator and a double-well potential. Subsequently the EP approach has been applied to semiconductor devices [9][10][11][12], which has advantage of easy numerical implementation and almost guaranteed convergence. The EP model is based on the following integral transformation from the classical potential (CP), $V(x)$, to the EP, $V_{eff}(x)$ [8]:

$$V_{eff} = \frac{1}{\sqrt{2\pi}a}\int_{-\infty}^{\infty} V(x+\xi)exp(-\frac{\xi^2}{2a^2})d\xi. \quad (1)$$

The idea of proposing the EP for device simulation originates in part from the consideration of the finite-size effect of charge carriers [8][13]. When the electric potential produced by a point charge (represented by a delta function) is replaced by a finite-size wave packet (represented by a Gaussian function), the CP is smoothed out and it results in an EP as given by (1).The integral form of V_{eff} as given in (1) suggests that V_{eff} is a convolution of $V(x)$ with a Gaussian function with the standard deviation a.

In this work, we modify the EMC simulation code to account for the quantum effects by smoothing the classical potential V to obtain the effective potential V_{eff} by (1).

III Simulation Experiments

The structure of a HEMT we simulated is as shown in Fig.1 (b). The gate length is 150 nm, the cap doping is 10^{18} cm^{-3} and the δ-doping is 1.5×10^{19} cm^{-3}. The thickness of the channel is 20 nm and that of the Schottky layer is 18 nm. The length of the recess is 0.5 μm and the total length of the device is 3.5 μm. A uniform rectangular mesh is used to avoid the self-force effect [14] and 40,000 particles are used in the simulation. Our EMC simulator adopts a non-parabolic 3-valley energy band structure and uses a synchronous scheme [14] with a constant time step dt equal to 2fs. We advance the particle's position by the equation (taking the y-direction as example)

$$y^{(i+1)} = y^{(i)} + \frac{1}{2}(v_i + v_f)\cdot\Delta t \quad (2)$$

rather than by the one suggested in [3]:

$$y^{(i+1)} = y^{(i)} + v_i\cdot\Delta t + \frac{1}{2}\frac{qE_y}{m^*}(\Delta t)^2 \quad (3)$$

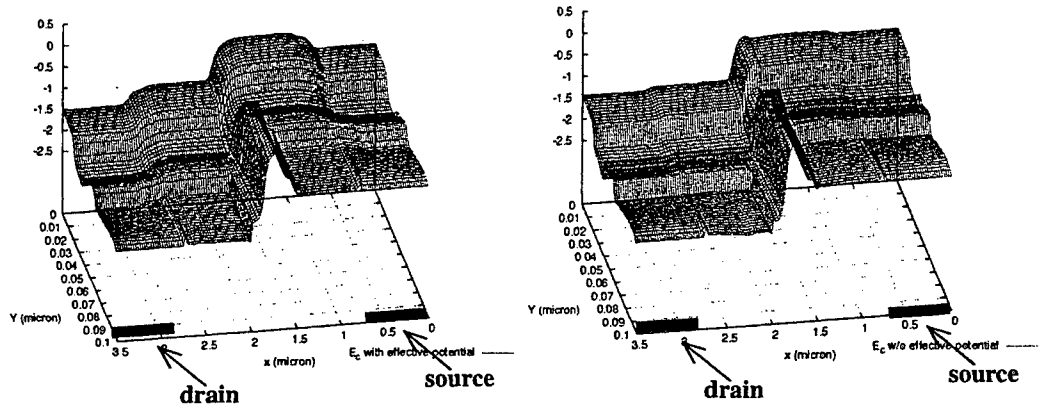
where, v_i and v_f are the y-components of initial velocity and final velocity, respectively, and E_y is the y-component of the electric field. When a particle crosses a hetero-interface, the time step dt is split into dt1 and dt2 which are respectively the times the particle spends during this time step before and after crossing the hetero-interface. The time intervals dt1 and dt2 are solved by (2) implicitly by an iteration scheme rather than by (3) explicitly. We have found that the former approach makes the simulation result less sensitive to the size of time step when the top drain and source contacts are usesd and when the electric field is very high.

At the beginning of each time step dt, the Poisson equation is solved and the effective potential V_{eff} is evaluated by (1). We choose the parameter a in (1) to be 1.92 nm, three times the theoretical value

$$a_0 = \hbar / \sqrt{8mk_B T} \tag{4}$$

which is often treated as an adjusting parameter. The effective mass m* of the Schottky layer material is 0.083m; thus if we substitute m by m* into (4), we will obtain a value roughly three times a_0. The force exerted on the particles is then calculated by the effective potential V_{eff} rather than by the classical potential. Only carriers in the Gamma valley are subject to the effective potential in our simulation since we consider that most of the carriers reside in the Gamma valley.

In Fig.2, we show the conduction band edge obtained from the simulation under the bias condition of V_g = -0.2V and V_d = 1.0V. From Fig.2 (a) and (b) we can see that the



(a) (b)

Fig.2 Conduction band edge for applied bias Vg=-0.2V and Vd = 1.0V
(a) with the effective potential (b) without the effective potential.

abrupt conduction band discontinuities have been smoothed out by the EP. Fig.3, Fig.5 and Fig.7 show the conduction band edge along the y-direction on the source side, under the gate and on the drain side, respectively. We find that the band edge in the channel is lifted and the barrier between the channel and the cap is lowered. Therefore more carriers can go over the Schottky layer and flow into the drain cap. In Fig.4, Fig.6 and Fig.8, we plot the corresponding electron density along the same line in the y-direction. A significant increase of electron density in Schottky layer can be observed. This means that the tunneling effect has been effectively included in the EP. In addition, the conduction band edge in the cap layer (see Fig. 3) with the EP becomes flat compared to that with the classical result. With the EP, it is easier for the carriers to move to the top of the cap layer and be collected by the drain contact. The output characteristic is shown in Fig.9. As expected, under the same bias condition, the drain current is increased by about 20 percent compared to that of the classical result.

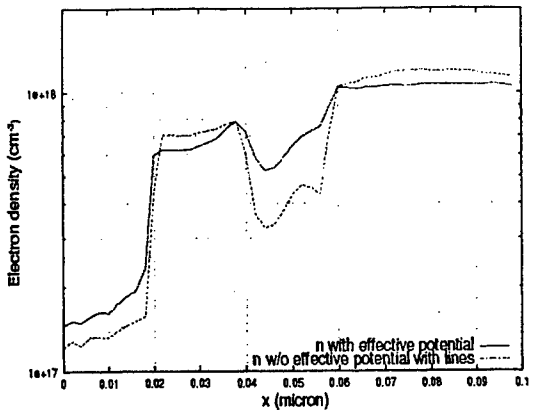


Fig.3 Conduction band edge along Y direction at the source side.

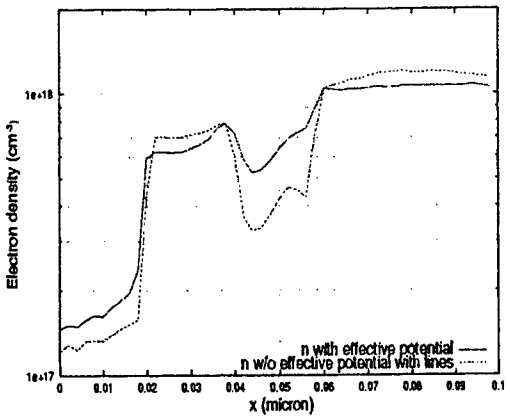


Fig.4 Electron density along Y direction at the source side.

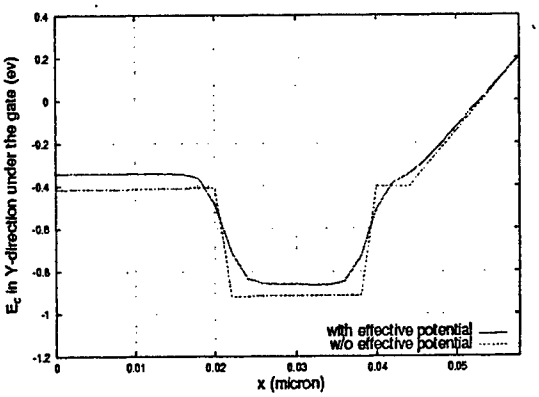


Fig.5 Conduction band edge along Y direction under the gate.

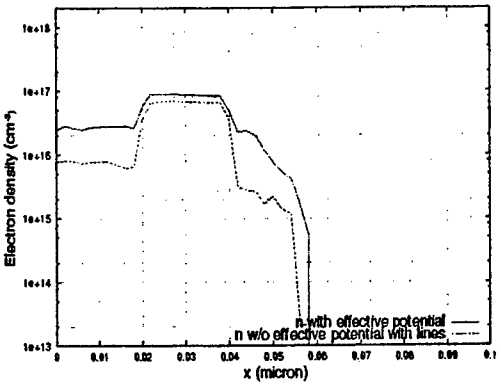


Fig.6 Electron density along Y direction under the gate

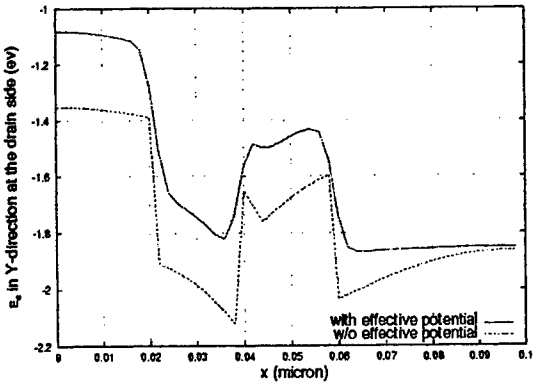


Fig.7 Conduction band edge along Y direction at the drain side.

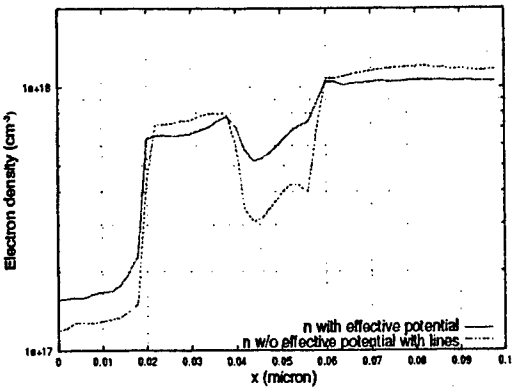


Fig.8 Electron density along Y direction at the drain side.

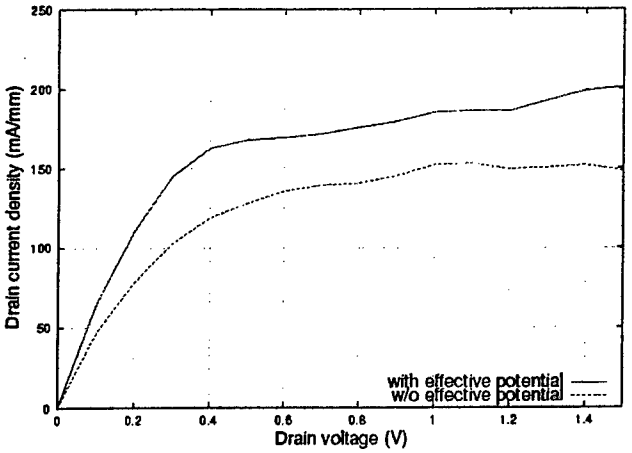


Fig. 9 Drain current vs. Drain voltage under the bias condition V_G = -0.2V and V_D=1.0V.

III Conclusion

In summary, when the contact is placed on top of the cap layer, the classical transport scheme gives very low I_D because the carriers cannot easily get out from the channel to the Schottky layer and be collected by the drain. However, when the effective potential is utilized to incorporate the quantum effects, the result is substantially improved and is much closer to the experimental data. We find that the particle injection scheme at Ohmic contacts also affects the drain current, and we expect a even larger current if a weighted displaced Maxwellian distribution [15] is used for the particle injection.

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An Ebers-Moll Model for Heterostructure Bipolar Transistors with Tunnel Junctions

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Abstract

This paper presents an Ebers-Moll model for HBTs and DHBTs in which tunnelling transport plays an important role at the base-emitter (BE) and/or base-collector (BC) junction. Devices of this type include GaAs or InP-based HBTs with abrupt heterojunctions, as well as a number of devices designed intentionally with thin tunnel layers at the B-E or B-C junctions [1,2]. For these structures, the conventional drift-diffusion formalisms (and numerical simulators based on them) are inadequate. The present model allows a quasi-analytical description of the device characteristics, assuming one dimensional structure. The model is applied here to the study of tunnel emitter [1] and tunnel collector InGaP-HBTs [2]. Forward and reverse Gummel plots can be analysed in relation to the tunnelling characteristics of the junction barriers.

I. Introduction

To relate measured I-V bipolar device characteristics and material parameters, Ebers-Moll models find wide applications. Lundstrom [3] proposed that carrier flow across the interface could be modeled by a generalized interface transport velocity; using such a velocity he derived an Ebers-Moll-like model that would be valid for abrupt or graded, and single- or double-heterojunction transistors. Using the same topology, in this paper, we have developed a simple Ebers-Moll model for heterostructure bipolar transistor with tunnel junctions.

The model presented can be implemented using simple numerical calculations based on analytical expressions. It should also be easy to implement in commercial software using CAD tools to compute the tunnel factors. The analytical form of the model is also useful to extract material or device parameters from simple DC measurements.

II. Device Model

A simplified band diagram of a base-emitter or base-collector junction containing a tunnel layer is shown in fig.1. In this work, electron and hole transport by thermionic-field emission across the barrier is calculated and related to carrier concentrations and other band diagram parameters [4]. Balancing the currents inside the device provides one set equations which can be solved to obtain an Ebers-Moll model of the form:

$$I_{ES} = qA\left[\frac{S_{EN}\left(S_{DNE}^2 + S_{DNE}S_{CN} - S_{DNC}^2\right)n_{BE}^o}{\left[\left(S_{EN} + S_{DNE}\right)\left(S_{CN} + S_{DNE}\right) - S_{DNC}^2\right]} + \frac{S_{DPE}S_{EP}p_E^o}{S_{DPE} + S_{EP}}\right] \quad (1)$$

$$I_{CS} = qA\left[\frac{S_{CN}\left(S_{DNE}^2 + S_{DNE}S_{EN} - S_{DNC}^2\right)n_{BC}^o}{\left[\left(S_{EN}+S_{DNE}\right)\left(S_{CN}+S_{DNE}\right)-S_{DNC}^2\right]} + \frac{S_{DPC}S_{CP}p_C^o}{\left(-S_{DPC}+S_{CP}\right)}\right] \tag{2}$$

$$\alpha_F = \frac{\left[\frac{S_{DNC}S_{EN}S_{CN}n_{BE}^o}{\left[\left(S_{EN}+S_{DNE}\right)\left(S_{CN}+S_{DNE}\right)-S_{DNC}^2\right]}\right]}{\left[\frac{S_{EN}\left(S_{DNE}^2 + S_{DNE}S_{CN} - S_{DNC}^2\right)n_{BE}^o}{\left[\left(S_{EN}+S_{DNE}\right)\left(S_{CN}+S_{DNE}\right)-S_{DNC}^2\right]} + \frac{S_{DPE}S_{EP}p_E^o}{S_{DPE}+S_{EP}}\right]} \tag{3}$$

$$\alpha_R = \frac{\left[\frac{S_{CN}\left(S_{DNE}^2 + S_{DNE}S_{EN} - S_{DNC}^2\right)n_{BC}^o}{\left[\left(S_{EN}+S_{DNE}\right)\left(S_{CN}+S_{DNE}\right)-S_{DNC}^2\right]}\right]}{\left[\frac{S_{CN}\left(S_{DNE}^2 + S_{DNE}S_{EN} - S_{DNC}^2\right)n_{BC}^o}{\left[\left(S_{EN}+S_{DNE}\right)\left(S_{CN}+S_{DNE}\right)-S_{DNC}^2\right]} + \frac{S_{DPC}S_{CP}p_C^o}{\left(-S_{DPC}+S_{CP}\right)}\right]} \tag{4}$$

where, for tunnel junction in the emitter, see fig. 1,

$$S_{EN} = \frac{v_{n2}\left(1+p_{n2}\right)\exp\left(\frac{qV_{pE}}{KT}+\frac{qV_{n3}}{KT}\right)\exp\left(\frac{-\Delta E_C}{KT}\right)}{\left[1+\frac{v_{n2}\left(1+p_{n2}\right)N_{C3}}{v_{n1}\left(1+p_{n1}\right)N_{C1}}\times\exp\left(\frac{-qV_{n2}}{KT}\right)\right]} \tag{5}$$

$$S_{EP} = \frac{v_{p2}\left(1+p_{p2}\right)\frac{N_{V2}}{N_{V1}}\exp\left(\frac{qV_{n1}}{KT}+\frac{qV_{n2}}{KT}\right)\exp\left(\frac{-\Delta E_V}{KT}\right)}{\left[1+\frac{v_{p2}\left(1+p_{p2}\right)}{v_{p1}\left(1+p_{p1}\right)}\times\exp\left(\frac{qV_{n2}}{KT}\right)\right]} \tag{6}$$

$$S_{DNE} = \frac{D_{nB}}{L_{nB}\tanh\left(\frac{W_B}{L_{nB}}\right)} \tag{7}$$

$$S_{DNC} = \frac{D_{nB}}{L_{nB}\sinh\left(\frac{W_B}{L_{nB}}\right)} \tag{8}$$

$$S_{DPE} = \frac{D_{PE1}}{L_{pE1}\tanh\left(\frac{W_{E1}}{L_{pE1}}\right)} \tag{9}$$

$$v_{n1} = \left(\frac{KT}{h}\right)\left(\frac{2}{N_{CE1}}\right)^{1/3} \tag{10}$$

$$v_{n2} = \left(\frac{KT}{h}\right)\left(\frac{2}{N_{CE3}}\right)^{1/3} \tag{11}$$

Similar equations can be written for the base-collector junction.

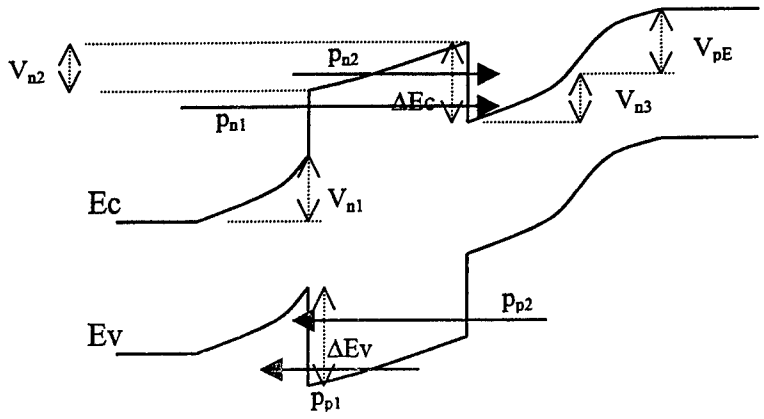


Figure 1: Band diagram of the emitter-base region of a heterostructure bipolar transistor with one tunnel junction. The emitter is composed of three layers, for example GaAs(1)/InGaP(2)/GaAs(3).

III. Results

The model was applied to InGaP/GaAs HBTs. Fig. 2 shows a measured Gummel plot for a InGaP-HBT whose doping profile is shown in the Table 1, compared with the results obtained from the Ebers-Moll model.

Table 1: Basic layer structure for NPN HBT with tunnel junction

MATERIAL	THICKNESS(A)	DOPING (CM-3)
InGaAs (In=0.5)	500	N=>1e19
InGaAs (In=.5 to 0)	500	N=>1e19
GaAs	1000	N=5e18
InGaP (In=.5)	300	N=3e17
GaAs	500	P=4e19
GaAs	4000	N=3e16
GaAs	7000	N=5e18

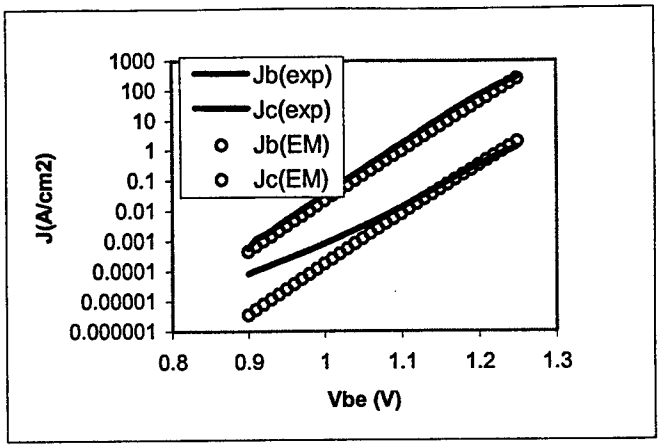


Figure 2: InGaP/GaAs tunnel HBT Gummel-plot.

The reverse Gummel plot, Ie(Vec), is particularly sensitive to the barrier characteristics. Experimental results, shown in fig. 3, can be fit assuming a 60A undoped layer between InGaP emitter and GaAs base.

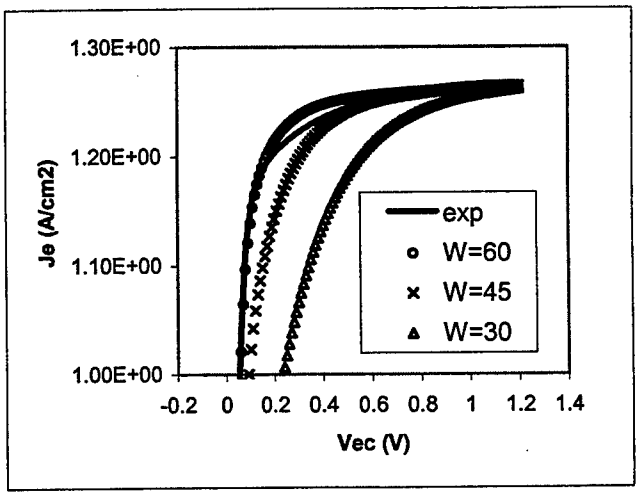


Figure 3: Ie(Vec) with undoped layer width as parameter

Fig. 4 shows the Ie(Vec) performance when ΔEc is varied. The model can thus be useful to determine barrier heights at the emitter heterojunction.

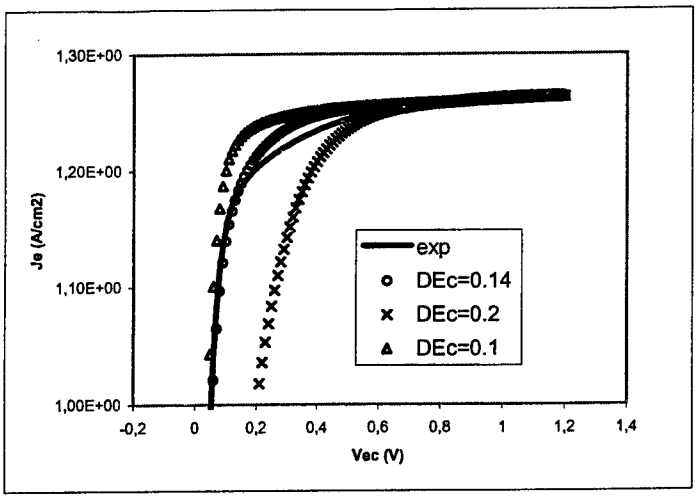


Figure 4: Ie(Vec) with ΔEc of InGaP/GaAs heterojunction as parameter

IV. Conclusions

This paper presents an Ebers-Moll model for heterostructure bipolar transistors with tunnel junctions. The present model allows a quasi-analytical description of the device characteristics, assuming one dimensional structure. The model can be useful to determine barrier heights at the emitter or collector heterojunctions.

Acknowledgements

The work described in this paper was supported in part by the Secretary of State of Education and Universities of Spain.

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InP/InGaAs Heterojunction Bipolar Transistors Grown on Ge/P Co-implanted InP Substrates by Metal-Organic Molecular Beam Epitaxy

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Abstract

InP/InGaAs Heterojunction Bipolar Transistors (HBTs) have demonstrated excellent high-frequency performance [1-4] and are widely used for optical fiber transmission [5-7]. However, the current mesa HBT structure utilizes a very thick, highly doped n^+InGaAs layer for the subcollector contact. This added mesa height makes multi-level interconnection processes more difficult, which impedes the capability of fabricating compact integrated circuits. In addition, InP has a much higher thermal conductivity than InGaAs, so heat dissipation may be a problem for densely packed circuits with the above structure. This paper reports on InP/InGaAs HBTs grown on Ge/P co-implanted substrates by Metal-Organic Molecular Beam Epitaxy (MOMBE). This embedded subcollector HBT structure offers several advantages for the fabrication of large-scale integrated circuits on InP substrates.

I. Ion-Implantation Conditions

Various elements have been reported for n-type implantation species into InP [8-10]. However, presently there is no obvious evidence to judge which species is better. In this paper, an embedded subcollector layer was formed by co-implanted Ge/P into Fe-doped InP substrates. Multi-energy and multi-dose implantation has been used to optimize the doping profile of both the bulk and surface doping densities. The latter is extremely important to form a good ohmic contact. The conditions are shown in Table I. After ion implantation, the substrates were annealed at 750°C by rapid thermal annealing (RTA). Hall measurements showed low sheet resistance of 54Ω/□, and a very good X-ray diffraction spectrum with a FWHM of 15 arc-secs. This was almost the same as InP substrates without implantation.

Table I. The Ge/P ion-implantation energy and dose for forming embedded subcollector layers.

	Energy (keV)	Dose (10^{14}/cm^2)
Ge	100	0.2
	275	0.5
	550	1.3
P	50	0.2
	120	0.5
	250	1.3

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II. Device Performance

Figure 1 shows the cross section of the InP/ InGaAs HBT with an embedded, ion-implanted subcollector layer. A 3500Å undoped InGaAs collector layer, followed by 500Å C-doped InGaAs base layer, 850Å n-type InP emitter layer and 1150 Å emitter contact layer were grown on ion-implanted and annealed InP substrates by MOMBE. Figures 2, 3 and 4 illustrate the dc performance of the HBT, including common-emitter dc characteristics, Gummel plots, and beta gain versus V_{BE}, respectively. A low turn on voltage of <0.25V, high breakdown voltage BV_{CEO} of >3V, and high beta current gain of >60 are achieved. These results are very similar to a reference InP/InGaAs HBT grown directly on a regular Fe-doped InP substrate with an n^+InGaAs layer for the subcollector contact. In summary, this experiment demonstrates that InP/InGaAs HBTs can be successfully grown on implanted InP substrates with excellent dc characteristics.

Figure 1 Cross section of HBTs with an embedded subcollector

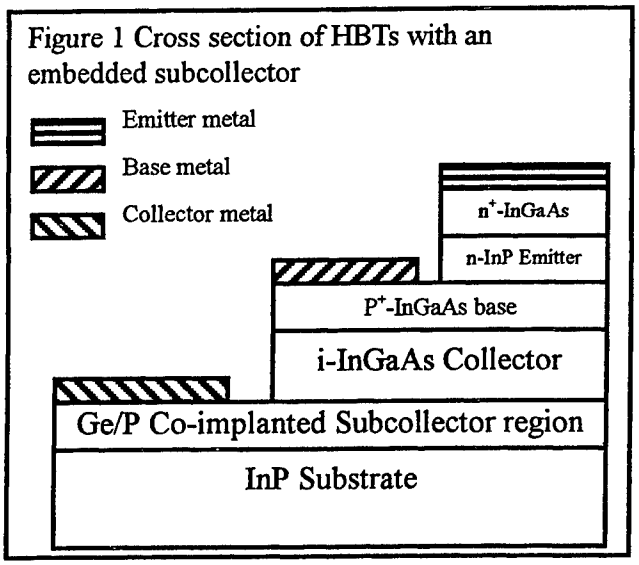


Figure2 Common emitter behavior for HBTs grown on Ge/P co-implanted InP substrates

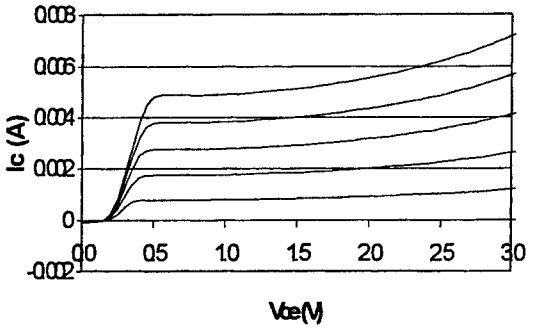


Figure 3 Gummel plot for HBTs grown on Ge/P co-implanted InP substrates

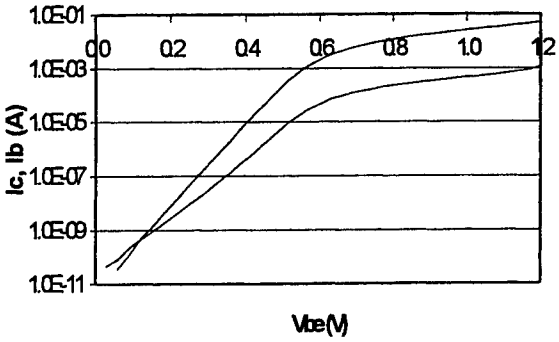
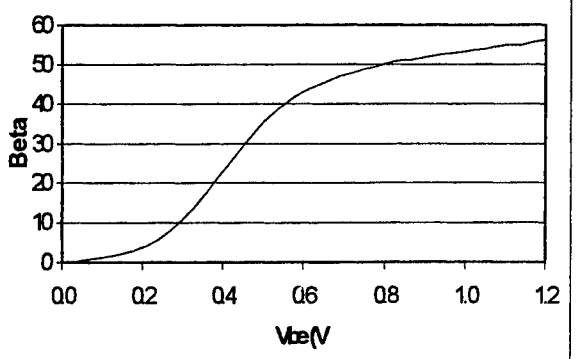


Figure 4 Beta gain vs V_{be} for HBTs grown on Ge/P co-implanted InP substrates



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CCD MEASUREMENTS OF GUIDED OPTICAL MODE ATTENUATION IN GaN LAYERS

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Abstract

Wide band gap and strong piezoelectric effect make GaN-based materials attractive for visible and ultraviolet optoelectronic applications, especially optical integration devices. The optical waveguide is a fundamental component of integrated optical devices. The measurement of the propagation loss is essential for waveguide characterization, where the loss is due to absorption and scattering. The conventional methods require the measurement of the absolute optical power, polishing of sample edges, and, sometimes, the sliding of coupling prism. Therefore, the conventional techniques are not very convenient or controllable. In this paper, a straightforward method has been proposed to characterize the attenuation of guided modes in GaN layer by employing a CCD system. As an optical mode propagates in the waveguide, the light is scattered and a characteristic light track appears on the waveguide surface. It is assumed that the scattered light is proportional to the guided mode intensity. By taking a digital picture of the track for each guided mode, the light intensity variation along the track is obtained. We used this technique to measure the attenuation of guided optical modes in multi-mode GaN layers grown by MOCVD on (0001) sapphire substrates. In accordance with theoretical predictions, the attenuation increased with mode order. For example, in 1 μm thick GaN layer, the attenuation of TE modes at 633 nm was 9.5dB/cm, 18.5dB/cm and 28.5dB/cm for m = 0, 1 and 2 respectively. These results demonstrate that the CCD technique is a fast, convenient and reliable method to characterize attenuation in optical waveguides.

1. Introduction

GaN-based materials are emerging as attractive materials for visible and ultraviolet optoelectronic applications and optical integrated circuits due to their wide band gap and strong piezoelectric effect. The optical waveguide is a fundamental component of optical devices. Therefore the characterization of GaN-based waveguides is essential for device and system design and performance improvement. This paper concentrates on the characterization of GaN waveguide propagation loss.

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When a light beam travels in a waveguide, it is subjected to attenuation due to absorption and scattering. Various methods have been used to determine the light intensity versus distance relationship. From the viewpoint of light intensity, the methods can be classified as direct and indirect measurements. The direct measurement includes the waveguide edge coupling (cutback [1]), prism coupling (sliding-prism [2], three-prism [3]), higher refractive index liquid coupling [4], and out-of-plane scattering measurement (optical-fiber probe [5], video camera [6]). The indirect measurement includes the measurement of the light-induced temperature change (direct temperature measurements [7], pyroelectric absorption measurement [8] and photothermal deflection [9]). In general, direct measurement methods are commonly used due to their simplicity.

From the viewpoint of distance variation, the loss measurement methods can be classified as cutback method [1], sliding-prism [2] (or coupling liquid [4]) method, Fabry-Perot resonance method [10], and light streak method (which corresponds to out-of-plane scattering method). The light streak method is the most commonly used method because the cutback method is destructive, the sliding-prism method has repeatability problem, and the Fabry-Perot resonance method is not very straightforward.

A light streak due to the light scattering can be observed when light travels along a thin-film dielectric waveguide. It is assumed that the scattered light is proportional to the coupled light. Therefore the variation of the scattered light along the light path can be viewed as the variation of coupled light intensity. The optical fiber probe is commonly used to detect the scattered light intensity variation by moving the probe along the light streak. However, since the amount of light collected by the probe depends strongly on the separation between the probe and the streak, it is important to keep the probe a constant distance from the waveguide when it moves along the streak, which is not a simple task. This alignment problem can be avoided by video camera method [6] proposed by Okamura et al. in 1983, in which the entire streak can be recorded by a video camera and digitized by an A/D converter. However, limited by the technologies of those times, their system was cumbersome. This method also has been employed by E. Dogheche et al [10][11] to investigate the propagation loss in GaN based waveguides in recent years, but no detailed description of their system has been given.

In this paper, a compact version of the video camera method has been realized by employing the InstaSpec IV CCD system of Oriel Instruments, which integrates the functions of video camera, A/D converter, and plotter. Using this system we measured the attenuation of guided modes in GaN layers grown by MOCVD on (0001) sapphire substrates.

2. System description

A schematic of the attenuation measurement setup is shown in Fig.1. The GaN waveguide sample and the prism are pressed together by a test fixture, and the test fixture is mounted on a turntable. By adjusting the laser incident angle, a particular propagation mode can be excited in the waveguide.

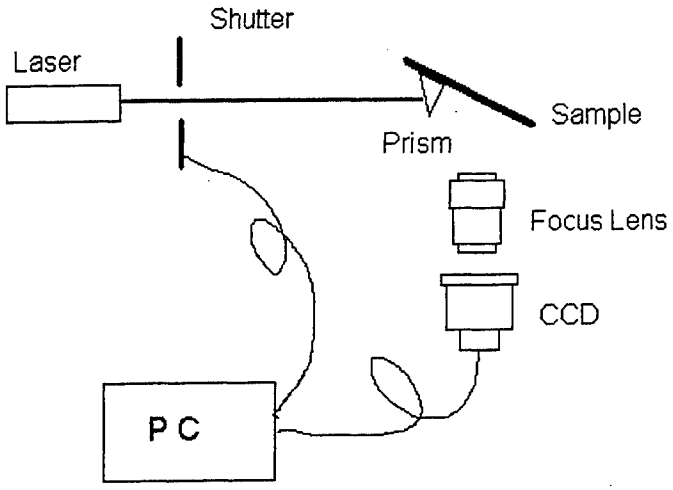
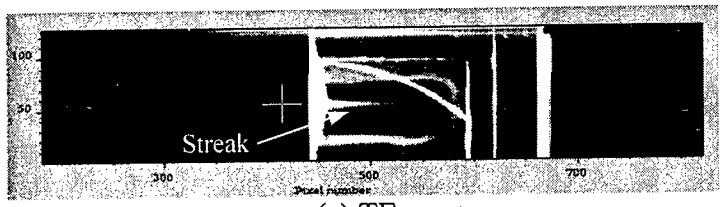


Fig. 1 Schematic of attenuation measurement setup

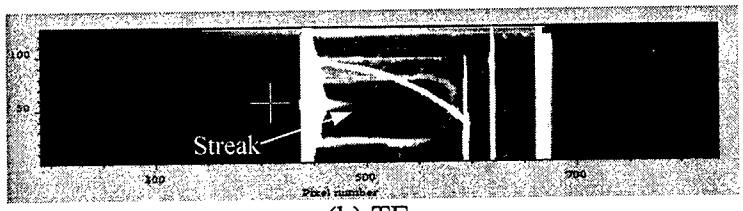
To take digital pictures of the light streak on the sample, an electrical shutter and a focus lens have been used. The shutter model was Oriel Instruments' 76994 with exposure time as short as 2 milliseconds and exposure frequency of 40 Hz. The focus lens (Edmund Industrial Optics' Model #52-274) had 6:1 zoom ratio and 145-330 mm working distance. The Oriel Instruments' IntaSpec IV model 78451 CCD system has 1024×128 pixels, with the size of each pixel being $26\times26um^2$. The embedded A/D converter had 16 bits resolution with linearity better than 1%. The software provided by the Oriel Instrument integrates the functions of the shutter and CCD control, image acquisition, display and analysis. The acquired image data can also be exported as ASCII data file to facilitate analysis with other tools.

3. Results

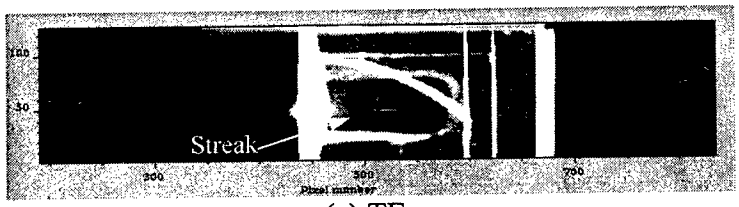
The laser source was a 25mW HeNe laser with 633nm wavelength. The waveguide was a 1 μm thick GaN layer grown by MOCVD on (0001) sapphire substrate. The images of the TE modes are shown in Fig. 2. The horizontal light track at the center of each image is the scattered streak of each mode, and the bright vertical line on the left of the image is the prism edge where the light is coupled into the waveguide. Other lines are the edges of sample and of the test fixture. The higher the mode order, the shorter the light streak, hence the larger the attenuation. The reason is that a higher order mode travels at a larger angle (with respect to the waveguide surface) in the waveguide; thus for unit waveguide length, it has a longer path than lower order mode. Therefore, the higher order mode is subjected to a larger attenuation.



(a) TE_0



(b) TE_1



(c) TE_2

Fig.2 Images of guided modes in GaN layer taken by CCD

In finding the attenuation of each propagation mode, the data of the corresponding light streaks have been extracted and then integrated vertically (normal to the propagation direction). After the integrated light intensity being plotted as a function of propagating distance, the curve was fitted to the exponential decay function

$$I(x) = C + I_0 e^{-\alpha x} \quad , \tag{1}$$

where C corresponds to background light, I_0 is the light intensity of the streak (other than the background) at x=0, and α is the attenuation coefficient. Fig. 3 shows the fitting results, where the y-axis is $(I(x)-C)/I_0$. The extracted attenuation values of TE0, TE1 and TE2 modes are 9.5dB/cm, 18.5dB/cm and 28.5dB/cm, respectively.

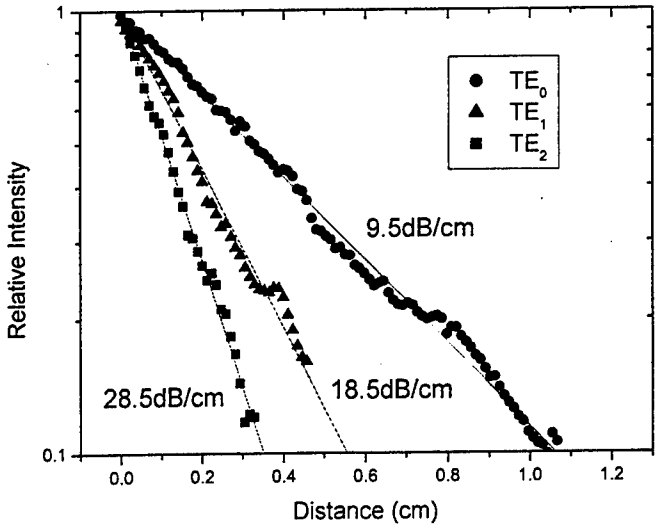


Fig.3 Attenuation of guided optical modes in GaN layer

4. Conclusion

By using CCD system of Oriel Instruments' InstaSpec IV, a setup of taking digital pictures of the streaks of guided modes has been built to evaluate the attenuation of waveguides. With this setup, the attenuation values of guided optical modes in 1 μm thick GaN layer grown by MOCVD on (0001) sapphire substrate have been measured to be 9.5dB/cm, 18.5dB/cm and 28.5dB/cm for TE0, TE1 and TE2 modes, with 633 nm HeNe as laser source. The results demonstrate that the CCD technique is a fast, convenient and reliable method to characterize attenuation in optical waveguides.

Acknowledgment

The work at SET and RPI was supported by the Office of Naval Research (Dr. Y.-S. Park).

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Physics of GaN-based High-Power Lasers

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Abstract

Advanced device simulation is used to analyze performance and device physics of milestone nitride laser diodes. These lasers exhibit the highest room-temperature continuous-wave output power measured thus far. The laser model self-consistently combines band structure and free-carrier gain calculations with two-dimensional simulations of wave guiding, carrier transport, and heat flux. Material parameters used in the model are carefully evaluated. Excellent agreement between simulations and measurements is achieved. The maximum output power is limited by electron leakage into the p-doped ridge. Leakage escalation is caused by strong self-heating, gain reduction, and elevated carrier density within the quantum wells. Improved heat-sinking is predicted to allow for a significant increase of the maximum output power.

Introduction

Fabry-Perot laser diodes emitting at 400 nm wavelength are investigated which exhibit the highest output power measured thus far (420 mW) [1]. The active region includes two InGaN quantum wells, an AlGaN electron stopper layer, GaN waveguide layers, and superlattice cladding layers (Fig. 1). Advanced laser simulation is used to analyze internal physical processes, to reveal performance limitations, and to explore optimization options. The laser model self-consistently combines 6x6 **kp** band structure and gain calculations with two-dimensional simulations of wave guiding, carrier transport, and heat flux [2]. However, the optical gain mechanism in InGaN quantum wells of real lasers is still not fully understood. It may be strongly affected by a non-uniform Indium distribution. Internal polarization fields tend to separate quantum confined electrons and holes, thereby reducing optical gain and spontaneous emission. However, screening by electrons and holes is expected to suppress quantum well polarization fields at high power operation. The high carrier density also eliminates excitons. On the other hand, many-body models predict significant gain enhancement at high carrier densities. Considering all the uncertainties in calculating the gain of real InGaN quantum wells, we here start with a simple free carrier gain model, including a Lorentzian broadening function with 0.1ps scattering time. The resulting gain characteristics are plotted in Fig. 2 for different temperatures.

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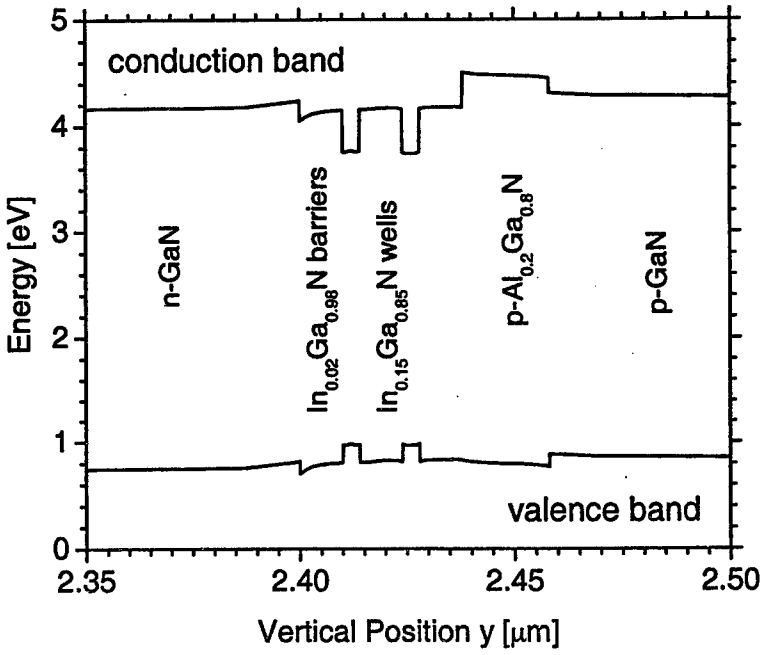


Fig. 1: Energy band diagram of the active region near lasing threshold.

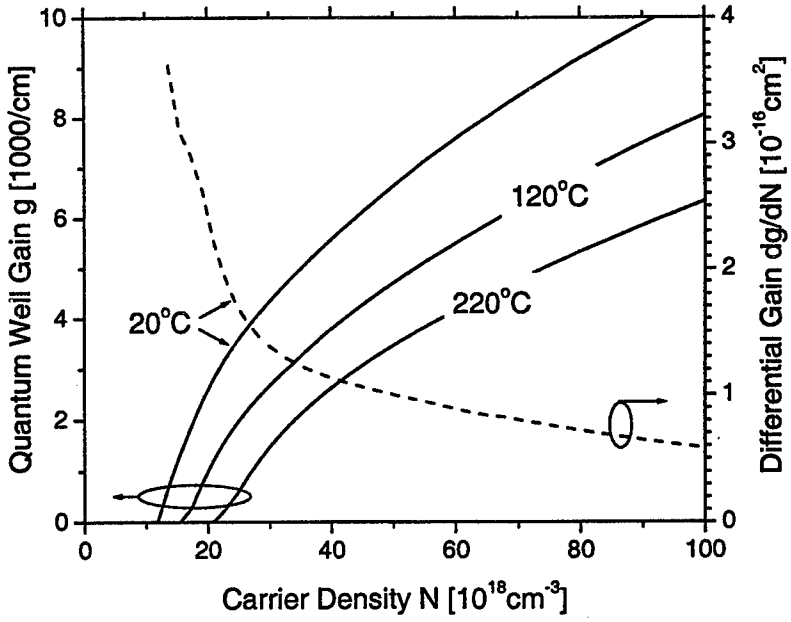


Fig. 2: Gain vs. carrier density at different temperatures (solid) and differential gain vs. carrier density at room temperature (dashed).

Comparison to Measurements

All material parameters used in the model are carefully evaluated. Excellent agreement with measured current-voltage (IV) and light-current (LI) characteristics is achieved (Fig. 3). The IV fit indicates a low p-contact resistance in these devices. The LI fit leads to the following internal device parameters: 12 /cm internal modal loss, 0.5 ns defect recombination lifetime within the quantum wells, and 75 K/W thermal resistance. All three numbers are within the expected range which confirms the accuracy of the laser model.

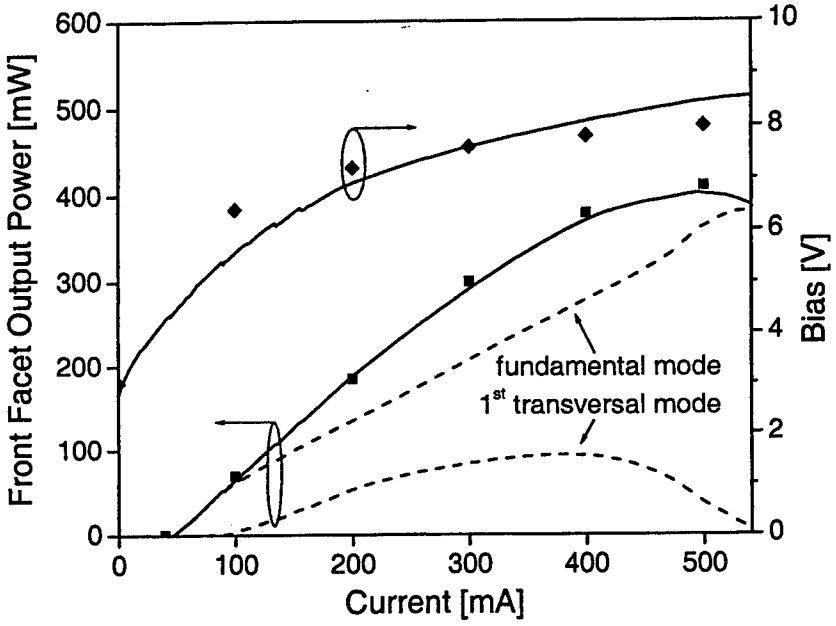


Fig. 3: Current-voltage and light-current characteristics (dots – measurement, lines – simulation).

Power Limiting Mechanisms

The output power roll-off of laser diodes is typically attributed to the self-heating in continuous-wave operation. The data in Fig. 3 indicate the generation of about 4 W heat power at the lasing power maximum. Considering 75 K/W thermal resistance, it is not surprising that a strong internal heating is calculated of about ΔT=300 K. The different heat sources are illustrated in Fig. 4. Joule heat in the highly resistive p-doped regions dominates the power budget by far. The much smaller contribution from phonons generated by defect recombination is partially compensated for by Thomson cooling, which represents the phonon absorption by carriers. Photon absorption is of minor importance. The strong self-heating reduces the optical gain (cf. Fig. 2) which leads to a substantial increase in quantum well carrier density. This triggers an escalation of electron leakage from the quantum wells into the p-doped side of the laser (Fig. 5) causing the measured power roll-off. Polarization charges are found to hardly affect the maximum power as they are screened by the high carrier density in the quantum wells.

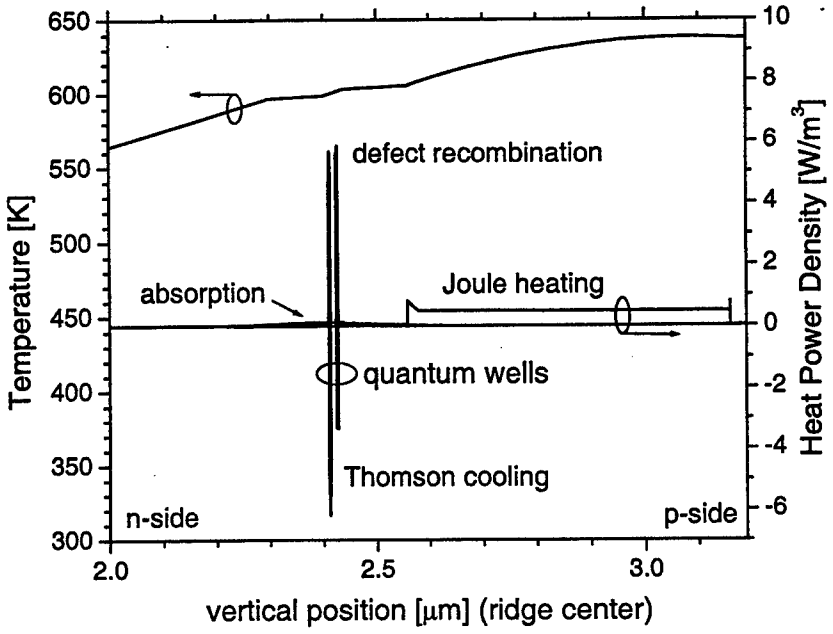


Fig. 4: Vertical profile of internal temperature and heat sources at maximum power.

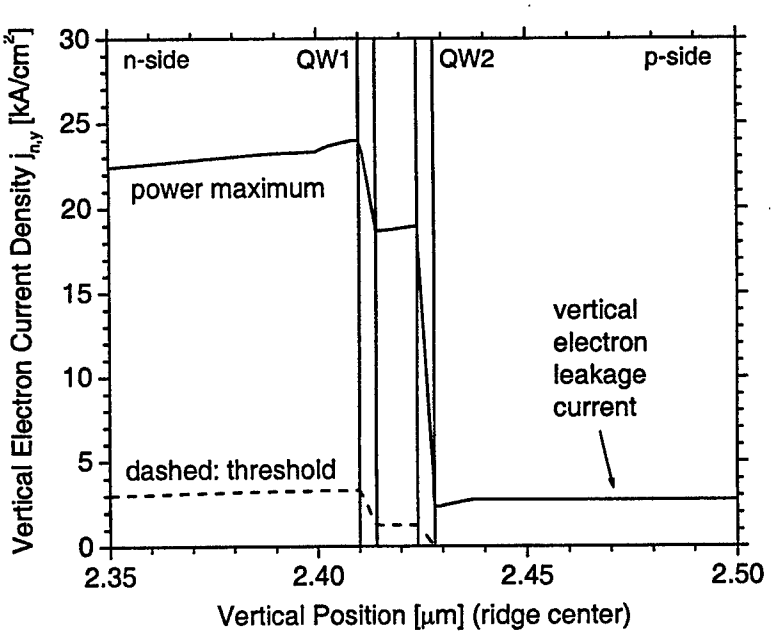


Fig. 5: Vertical profile of electron current density showing electron leakage into the p-side at the power maximum.

Laser Optimization

Reduction of the self-heating is the key to higher lasing power. This can be achieved by lowering the heat power generation or by improved heat dissipation. The electrical resistance of the p-doped layers constitutes the main heat source but it cannot be easily reduced since higher p-doping causes a lower hole mobility. Improved heat sinking has recently been demonstrated by replacing the sapphire substrate with copper [3]. In our simulation, we simply eliminate the external thermal resistance of 30K/W, which reduces the total thermal resistance to 45 K/W. The resulting LI characteristic exhibits almost double the maximum output power (Fig. 6).

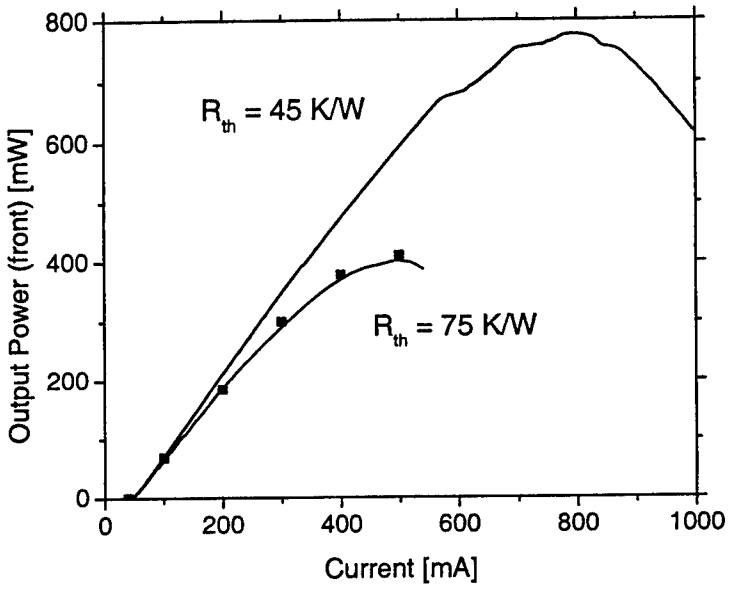


Fig. 6: Simulation of the light-current characteristic with reduced thermal resistance R_{th} in comparison to original curve from Fig. 3.

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The Electrical Effects of DNA as the Gate Electrode of MOS transistors

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Abstract

The gate conductor material affects the threshold voltage of metal-oxide-semiconductor (MOS) transistors through the influence of the electrochemical work function and electric charge. Measurements of the threshold voltage from current voltage characteristics may therefore provide a method to estimate the electronic properties of biomolecules located on the gate electrode. We have deposited DNA from the corn genome onto the gate oxide of Si nMOS transistors and measured the effects on the current-voltage characteristics. We found that the DNA decreased the drain-source current compared to devices with clean gate oxides and pure buffer solutions. The threshold voltage was extracted by current-voltage measurements in the linear operating region and was found to increase by +1.9 volts after application of the DNA specimen, a value consistent with the expected negative charge density. This large change suggests that MOS devices may be useful as sensitive bioelectronic detectors.

Introduction

Currently there is interest in the development of high-speed, integrated techniques for rapid processing of biologically important molecules and neurological cells [1-3]. The industrial maturity of high-speed and high-density CMOS technology makes the silicon field effect transistor (FET) a natural contender for applications in this relatively new field. The

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purpose of our investigation was to analyze the response of Si FETs to the presence of DNA samples suspended in solution, which is placed directly upon the transistor gate oxide. The DNA-solution acts as the transistor gate electrode, replacing the conventional metal electrode which is anticipated to interfere with direct coupling of the bio-material with the Si channel [4]. Figure 1 shows the conceptual design of our bio-FET design. Our approach was to measure the transistor characteristics and to extract device parameters including the threshold voltage, which depends on the electrochemical work function and electric charge of the DNA sample. We offer preliminary results illustrating the effects of biomolecular modification of the gate area on the transistor characteristics. We provide support that further investigation is warranted if this effect can be reliably used as a rational basis for detecting biomolecule specificity.

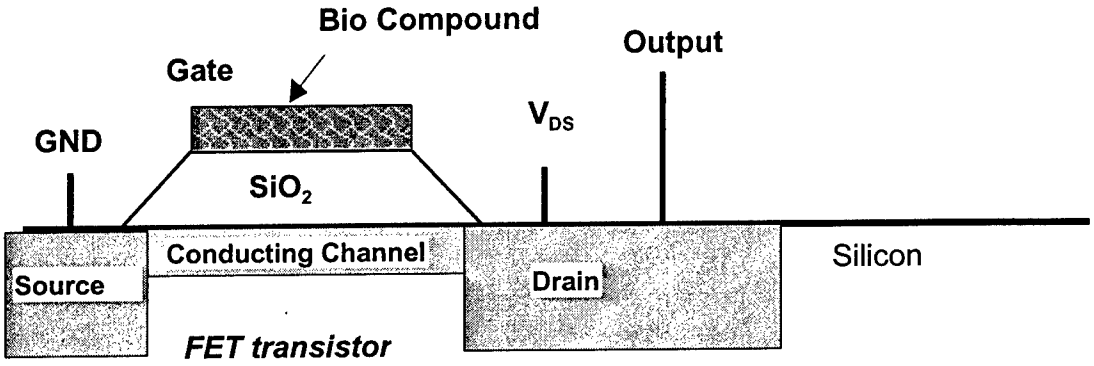


Figure 1. Cross sectional illustration of the bio-transistor with a biocompound (e.g. DNA) deposited on the gate oxide. The purpose of this device is to measure the effect of biological molecules and compounds located near the gate dielectric on the transistor characteristics. Electrode designations: GND (ground), V_{DS} (drain voltage).

Experimental

N-MOS transistors were fabricated starting with 1-10 Ω-cm p-type Si substrates and using a standard planar N-channel enhancement MOSFET process. Source and Drain regions were formed via phosphorus diffusion through a pre-patterned 500nm thick SiO_2 diffusion mask (bubbling O_2 carrier gas through $POCL_3$ for pre-deposition, followed by drive-in in an N_2 ambient). The gate insulator was formed by dry-oxidation involving bubbling high purity O_2 gas through semiconductor grade TCE forming a 50nm thick SiO_2 gate insulator. The biosensor FETs had an active area of 50 x 200 (length×width) square micrometers and the gate oxide capacitance per unit area was: $C_{OX} = 69nFcm^{-2}$.

During this work we used single stranded corn DNA (a 20 base oligomer, from Synthetic Genetics) in a phosphate buffer solution with a pH of 7. The DNA-solution and the reference material (buffer without DNA) were applied with a dropper on the gate insulator during electrical testing. We measured the current-voltage (I-V) characteristics of equivalent transistor structures with floating gates prior to application of solution and also for gate configurations consisting of the phosphate buffer only and the DNA suspended within the buffer. Figure 2 shows the I-V curves of the transistor (i) prior to application of solution, (ii) after application of the phosphate buffer solution, (iii) after application of the DNA in the buffer solution and (iv) after the DNA solution remained on the gate for 3 hours. It is immediately obvious that the drain to source current changes significantly for equivalent driving voltages (V_{DS}) after application of the buffer and DNA/buffer solutions. We observed that the transistor characteristics were not stable with time for both the buffer solutions and the DNA solutions, an effect which has also been observed for neurological cells suspended in an electrolyte solution on the gates of p-channel Si FETs-probably due to chemical interaction between the SiO_2 insulator and ions within the buffer solution[4]. It has been suggested that a silicon nitride cap on the gate and use of n-type Si will alleviate the problem of ionic diffusion from the buffer solution into the Si/SiO_2 interface region.

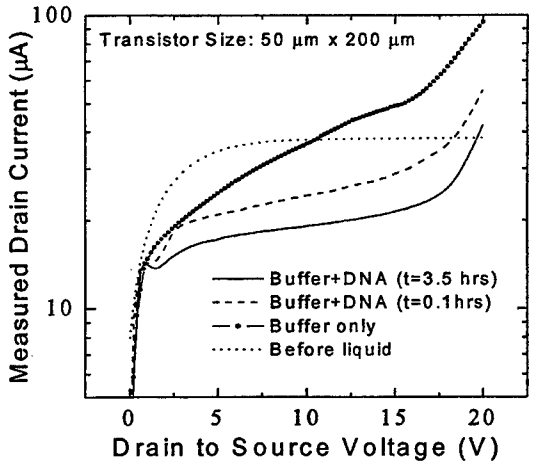


Figure 2. The current-voltage characteristics of biosensor transistor fabricated using silicon MOS circuit technology. The data show the drain-to-source current I_{DS} versus the drain-to-source voltage V_{DS}, for different gate conditions including the presence of DNA. No external bias was applied to the gate, and the substrate was grounded (V=0). The variations in current traces may indicate differences in the electrochemical potentials of the gate molecules. A solution of DNA decreased the output current by 20 µA compared to the buffer solution, indicating that the DNA had a negative charge.

Effect of gate-electrode (DNA) on the FET threshold voltage

The threshold voltage (V_T) is an important figure of merit for Si FETs which dependent on Si doping, oxide thickness, the electrochemical work function of the gate electrode, and the charges in the vicinity of the Si/SiO_2 interface. V_T can be extracted from the transistor IV characteristics, operating in the linear region, by the following well known equation for drain current:

$$I_D = (\beta_n/2)[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (1)$$

Our experiments indicated that DNA shifted the threshold voltage parameter (V_T) by about + 1.92 volts compared to that of the FET using the buffer solution alone as gate electrode. The experimental I-V and curve fit using equation (1) are shown in figure 3. Such large threshold shifts indicated a strong sensitivity to DNA, and the positive direction (less negative) corroborated the well known negative charge of DNA molecules. Table I summarizes the result of the V_T extraction for several gate electrode conditions and with a grounded substrate.

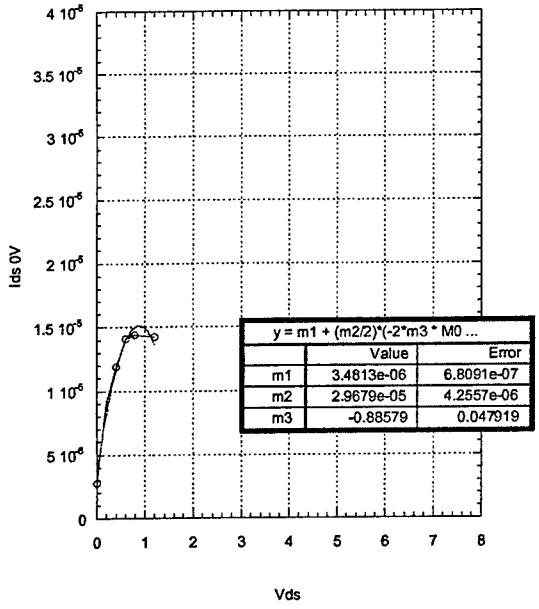


Figure 3. Curve fit of the transistor I-V in the linear operating region to equation (1).

The measured V_T shift corresponded to a net negative charge Q per area which we attribute to the addition of DNA into the buffer solution:

$$Q = CV = (69nF \cdot cm^{-2}) \times (-1.92V) = -(1.3 \times 10^{-7}\ Coulomb \cdot cm^{-2}). \quad (2)$$

This value of charge density reasonably agrees (within one order of magnitude) with that of DNA, which is reported in the micro-Coulomb range [5].

Data for the threshold voltage, V_{TO}, with zero substrate bias, are summarized in Table 1. It is important to note that the phosphate buffer solution itself strongly affects the transistor characteristics, even more so than the effect of the DNA. It is not clear yet if the strong change in threshold voltage after application of the buffer is due solely to its electrochemical potential, or if there is also diffusion of charged ions from the buffer solution into the SiO_2. We believe that phosphate buffer solution itself affects the integrity of the oxide insulator; this is supported from our observation that the V_T does not return to its value prior to application of the buffer, even after thorough washing and rinsing in DI water and that the transistor characteristics are not stable over periods of time (hours). This effect was also observed in the work of reference [4] for neurological cells suspended in an electrolytic solution.

Table 1. Table of extracted threshold voltages using the curve fitting technique described in the text.

Gate Condition	V_{T0}
Clean gate oxide	-6.57 V
oxide with buffer solution	-2.81 V
with DNA+buffer	-0.89 V
DNA+buffer (3.5 Hours Later)	-0.80 V
DNA+buffer (3 Days Later)	-3.36 V
Cleaned (4 Days Later)	-5.15 V

Conclusions

We have found that DNA molecules suspended in solution placed on the gate insulator produce a significant shift in the threshold voltage, which may be attributed to the workfunction and/or electric charge of the material. This effect may be usable for bioelectronic device applications such as sensing and identification. Future work involves

developing an optimized process in which the degradation effects of the buffer solution are eliminated or at least completely understood, so that any effect of charged ion interactions with the SiO_2 insulator can be taken into account in the analysis.

In conclusion we designed, built and tested a novel prototype biomolecular- sensitive FET transistor that varies its output current in response to the presence of DNA on its gate electrode. Our electrochemical potential biosensor transistor was fabricated using standard MOS processing. The array density of these sensor transistors can be equivalent to the densities of transistors in integrated circuits: above 10^7 cm^{-2}. The bio-electrochemical sensor transistors may be capable of yielding the time dependent behavior of bio-molecules, and could be used to explore the possibilities of semiconductor-biological hybrid circuits. Possible applications include sensing and identifying proteins and DNA.

Research sponsored by NSF under SGER grant ECS-0129535. Thanks to T. N. Adam and R.T. Troeger for processing assistance.

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SiGe Diffusion Barriers for P-doped Si/SiGe Resonant Interband Tunnel Diodes

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Abstract

Si/SiGe resonant interband tunnel diodes (RITD) employing δ-doping spikes of P and B that demonstrate negative differential resistance (NDR) at room temperature are presented. Thin SiGe layers sandwiching the B δ-doping spike used to suppress B out-diffusion are discussed. Three structures were investigated in this study. Structure A, which employed a symmetrical 1nm Si / 4nm $Si_{0.6}Ge_{0.4}$ / 1nm Si (1/4/1) spacer, showed a peak-to-valley current ratio (PVCR) of 2.7 after 1 minute annealing at 725°C. Structure B with an asymmetrical 0nm Si / 4nm $Si_{0.6}Ge_{0.4}$ / 2nm Si (0/4/2) spacer configuration showed a PVCR of 3.2 after 1 minute annealing at 800°C. Structure C, which is the same as Structure B, except that a 1nm $Si_{0.6}Ge_{0.4}$ cladding layer was grown below the B δ-layer, further improved PVCR to 3.6 after 1 minute annealing at 825°C. Results clearly show that, by introducing SiGe layers to clad the B delta-doping layer, the B diffusion is suppressed during the post growth annealing, which raises the thermal budget. A higher RTA temperature appears to be more effective in eliminating defects and results in a lower valley current and higher PVCR

I. Introduction

Since the development of Si-based resonant interband tunneling diodes (RITD) [1] that can potentially be integrated with CMOS or HBT for highly functional tunnel diode-transistor circuits [2], numerous experimental attempts have been made to improve RITD performance, especially the peak-to-valley current ratio (PVCR) [3,4]. To maximize the PVCR, a higher peak current density and a lower valley current density are desired. For Si-based RITD, the peak current density is determined by the electron tunneling probability through the tunneling barrier, which depends on the dopant profile of both sides of the p-n junction. Sharper dopant profiles will lead to higher tunneling current, thus higher peak current density. Valley current density becomes elevated by the defects within the tunneling barrier created during the low temperature molecular beam epitaxy (LT-MBE) growth process. LT-MBE is needed to minimize dopant diffusion and segregation during epitaxy. Post growth annealing can reduce

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the point defect density, thus lowering the valley current density, but concurrently it unfavorably broadens the dopant profiles, especially B, which is a fast interstitial diffuser, thus the peak current density can also be reduced if over-annealed. Given that SiGe can act as an effective diffusion barrier for B in a Si matrix [5], structures with SiGe layers cladding the B δ-doping layer were grown in order to preserve the sharp B profile during high temperature post growth annealing to reduce the point defect density. In this manner, the aim of this work is to raise the thermal budget of the RITDs in order to maximize the PVCR.

II. Experimental

Three structures were designed to study the effect of the SiGe cladding layer. Structure A, the control device, employed a symmetrical 1nm Si / 4nm $Si_{0.6}Ge_{0.4}$ / 1nm Si (1/4/1) spacer as shown in Figure 1. Figure 2 shows Structure B with an asymmetrical 0nm Si / 4nm $Si_{0.6}Ge_{0.4}$ / 2nm Si (0/4/2) spacer. Note, the SiGe layer was directly grown atop the B δ-layer without the thin Si offset layer. Figure 3 shows structure C, which is the same as structure B, except that a 1nm $Si_{0.6}Ge_{0.4}$ cladding layer was also grown below the B δ-layer. In this structure, the B δ-layer was essentially clad by thin SiGe on both sides. For all these 3 structures, the nominal n-type and p-type bulk doping levels in the injectors are $5\times10^{19}cm^{-3}$, while the nominal n-type and p-type δ-doping levels are $1\times10^{14}cm^{-2}$.

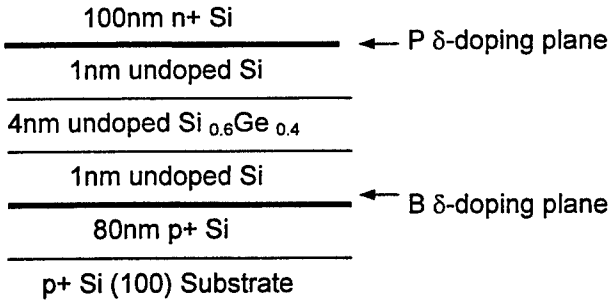


Fig. 1. Schematic diagram of structure A, the Si / $Si_{0.6}Ge_{0.4}$ / Si (1/4/1) RITD.

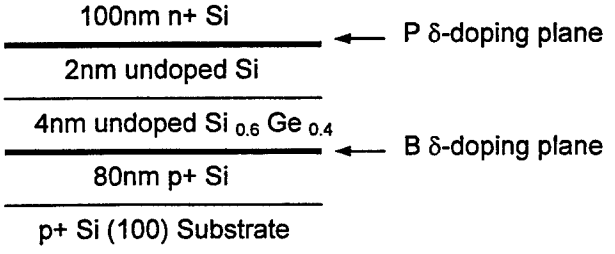


Fig. 2. Schematic diagram of structure B, the $Si_{0.6}Ge_{0.4}$ / Si (0/4/2) RITD.

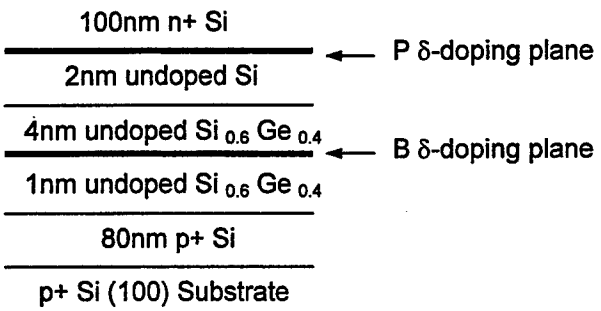


Fig. 3. Schematic diagram of structure C, the $Si_{0.6}Ge_{0.4}$ / Si (0/4/2) RITD with cladding layer.

Epitaxial growth was achieved with a specially designed MBE growth system using elemental Si with an electron-beam source. The structures were grown on 75mm B-doped (ρ = 0.015-0.04 Ω·cm) Si (100) wafers. Prior to device fabrication, portions of the wafers were rapid thermal annealed (RTA) using a forming gas ambient in a Modular Process Technology Corporation RTP-600S furnace at various temperatures for 1 minute. Ti/Au dots with 18 μm diameters were patterned on the surface of the wafers via standard contact lithography. A buffered oxide etch was used prior to metallization. Using the Ti/Au dots as a self-aligned mask, HF/HNO_3 wet etching was performed to define the diode mesa. Finally, a Ti/Au backside contact was thermally evaporated on all of the samples.

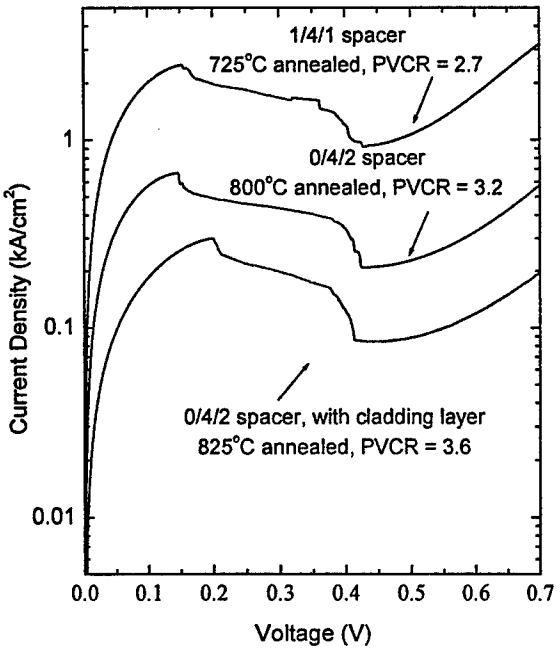


Fig. 4. I-V characteristics of RITDs showing highest PVCR for these 3 different structures Note, the annealing temperatures are differer

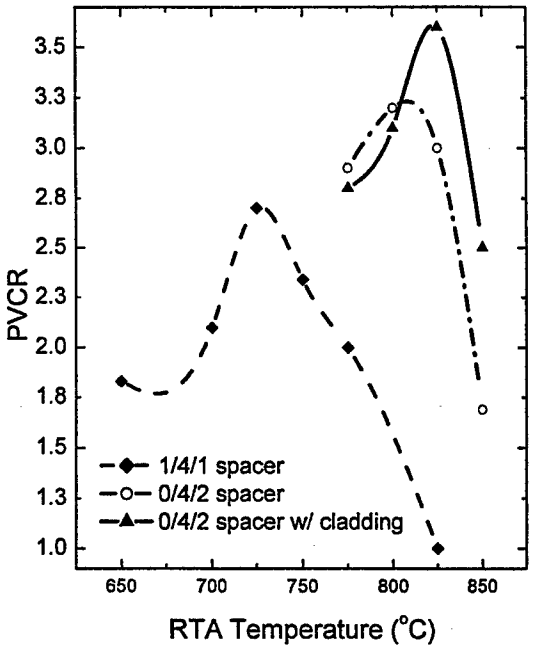


Fig. 5. Comparison of PVCR vs. annealing temperature for these 3 different structures.

III. Results and Discussions

Figure 4 shows the I-V characteristics of these 3 structures with the highest PVCR. Structure A demonstrates a PVCR of 2.7 with 1 minute annealing at 725°C. Structure B obtained a PVCR of 3.2 using 1 minute annealing at 800°C. Whereas, Structure C further improved its PVCR to 3.6 with 1 minute annealing at 825°C.

Post-growth RTA processing has been shown to remove point defects that contribute to elevated valley current, but deleteriously broaden the B δ-doping [6]. Consequently, an optimal RTA temperature exists that maximizes PVCR, which is clearly shown in Fig. 5. Note the optimal annealing temperatures for these 3 structures are different, Structure C shows the highest optimal annealing temperature, while Structure A shows the lowest optimal annealing temperature. These results illustrate that insertion of the SiGe cladding layers suppresses B outdiffusion, so that higher RTA temperatures can be employed to more effectively remove point defects, while preserving the B peak to ensure a high peak current density. Consequently, Structure C demonstrates the highest PVCR among these 3 structures.

The effect of the SiGe cladding layer can also be demonstrated by Fig. 6, which shows a comparison of the isothermal I-V characteristics of these 3 structures all annealed at 825°C for 1 minute. All of these 3 structures show similar valley current density, while structure C shows the highest peak current density.

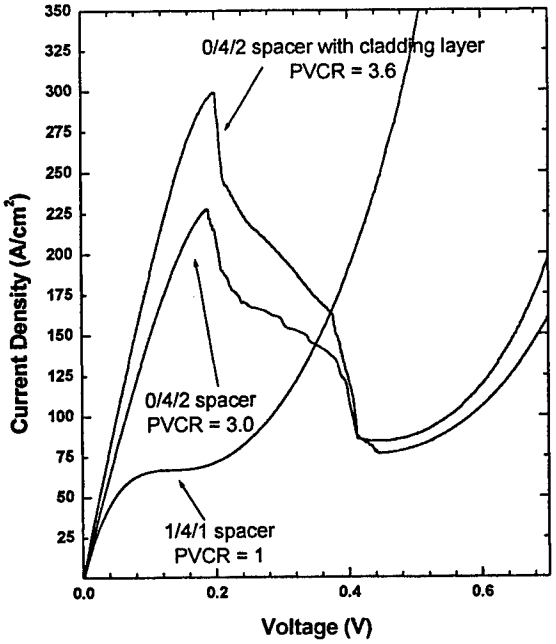


Fig. 6. Comparison of I-V characteristics of 3 structures annealed at 825°C.

IV. Conclusions

By introducing SiGe layers cladding the B δ-doping layer, the B diffusion is suppressed during the post growth annealing, which raises the thermal budget. A higher RTA temperature appears to be more effective in eliminating defects and results in a lower valley current and higher PVCR.

Acknowledgements

The authors which to acknowledge useful technical discussions with Roger Lake. This work was supported by the NSF (ECS-0196208 and ECS-0196054).

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SILICON-GERMANIUM POWER DEVICES AT LOW TEMPERATURES FOR DEEP-SPACE APPLICATIONS

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ABSTRACT

Silicon-germanium heterostructure based 1-watt n-channel metal-oxide-semiconductor modulation-doped field effect transistors (MOS-MODFETs) with 6 μm gate lengths and 1 mm total gate widths have been designed, fabricated and tested from 300 K to 90 K. The devices were fabricated by an ion-implanted process and employ a low-temperature thermal oxide and PECVD deposited oxide as the gate insulator. The devices showed a saturation current of approximately 77 mA at V_{DS}=14 V, V_{GS}=5V at 90 K, corresponding to a power dissipation of 1W. Because they employ oxide as a gate dielectric, the devices have a low gate leakage current of < 1nA at V_{GS}=10 V.

1. INTRODUCTION

As space probes move away from the sun, average temperatures experienced by them decrease from an average of about 280 K near earth, to an average of about 40 K near Pluto. Convention silicon-based electronic devices often suffer from carrier freeze-out at low temperatures, and must be heated by radio-isotope heater units (RHUs) to keep them at normal operating temperatures. RHUs suffer from the following disadvantages: uncontrollable heat output, added weight, and risk of environmental damage from the radioactive material. Devices capable of operation at cryogenic temperatures would therefore be useful in circuitry aboard spacecraft.

The silicon-germanium MODFET has been proven to operate at cryogenic temperatures [1]. P-channel SiGe MOS-MODFETs have also been fabricated and characterised at cryogenic temperatures [2]. Fabrication and characterisation of n-channel MODFETs using Schottky gates has been reported by Ismail et al. in 1994 [3]. N-channel modulation doped MOSFETs were reported in 1999 by O'Neill et al.[4] This paper describes the design, fabrication and cryogenic characterization of a 6 μm gate length x 1mm gate width n-channel SiGe-based MOS-MODFET capable of dissipating 1 watt. The current-voltage characteristics and the variation of drain current with temperature are presented.

2. SIMULATION

One-dimensional Poisson solvers [5, 6] were used to obtain the band structure of the silicon-germanium heterostructure and electron densities in the conducting channel

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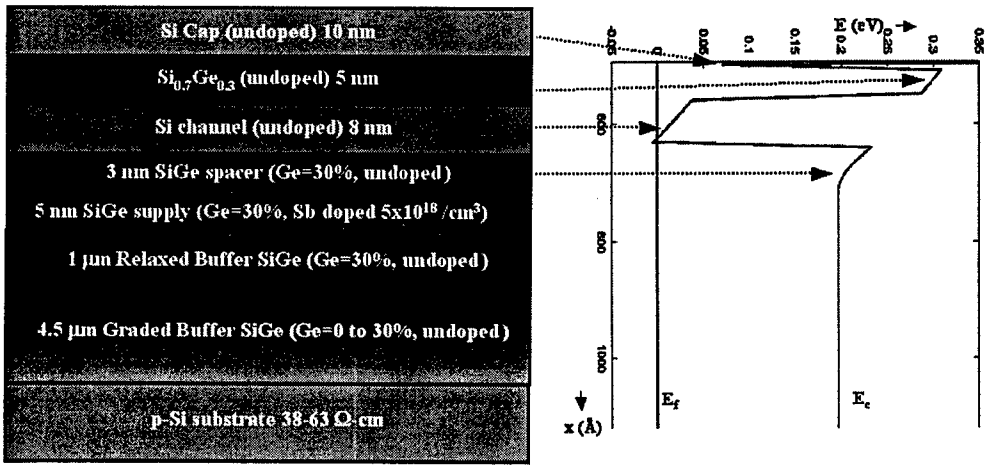


Fig 1: N-channel heterostructure and band shape

were obtained for varying gate biases. Material parameters for silicon-germanium and strained silicon were supplied to the programs along with the layer thicknesses and doping concentrations. The structure chosen for growth is shown in figure 1 along with the conduction band edge as obtained from the simulation. The substrate is a 38-63 ohm-cm boron doped P-type silicon substrate. The first layer is a graded SiGe buffer in which the Ge concentration is increased from 0 to 30%. Next is a 1mm thick relaxed $Si_{0.7}Ge_{0.3}$ layer. Together these layers form the virtual substrate on which a strained Si layer may be grown. This is followed by a 5 nm thick $Si_{0.7}Ge_{0.3}$ supply layer doped with Sb to $5x10^{18}/cm^3$. The 3 nm thick undoped $Si_{0.7}Ge_{0.3}$ is a spacer and prevents electrons in the following 8 nm undoped strained Si channel from interacting with the ionised impurities in the supply layer. The channel is followed by a 5 nm thick undoped $Si_{0.7}Ge_{0.3}$ barrier layer which prevents electrons from the supply layer from accumulating in the cap. The cap itself is a 10 nm thick undoped Si layer which was almost completely consumed during thermal gate oxidation.

Figure 2 shows the electron density in the channel region. It is clear that the electrons are confined to the channel region, and not present in the cap in high concentrations. Changing the amount of applied gate bias produced a change in the electron density in the channel, which indicated the ability of the gate to modulate drain-source current.

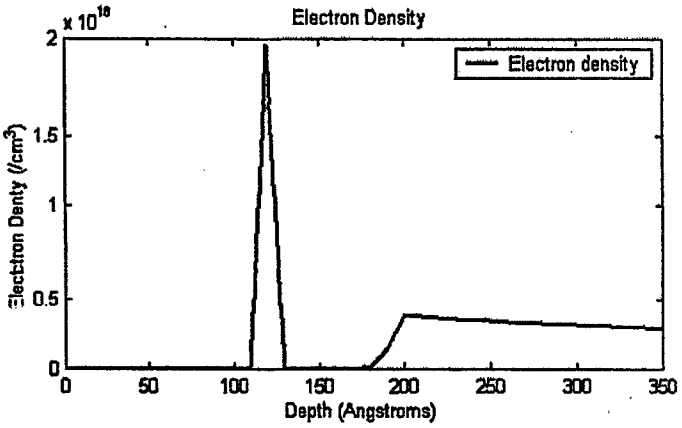


Fig 2: Electron density in the Si channel

3. DESIGN

The device was designed to be an interdigitated structure, with eight fingers of 125 μm width each, for a total width of 1 mm (see figure 1(b)). Figure 3 shows the Autocad layout of the device where the gate structure consists of eight 125 mm wide fingers for a total gate width of 1 mm. The source and drain ohmic regions are 125 x 125 μm. The large pad areas aid in wirebonding. The total device area is 350 μm x 1050 μm, while the total gate area is 6000 μm^2.

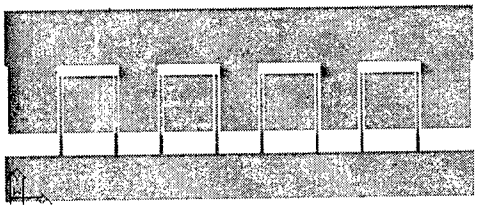


Fig 3: Device Layout

4. FABRICATION

During fabrication of silicon-germanium based heterostructure devices, care must be exercised to limit exposure of the wafer to high temperatures in order to prevent strain relaxation and germanium diffusion. Accordingly, the maximum temperature that was used in device fabrication was 750° C.

The silicon-germanium heterostructures was grown by molecular-beam epitaxy in a Perkin-Elmer 430S MBE system on a 4-inch 38-63 Ω-cm B-doped wafer. Except for the supply layer, all epitaxial layers were nominally undoped. However, the background doping of this MBE system is in the high 1e15/cm3 range, n-type. A 4.5 μm thick graded buffer was first grown, with the germanium concentration increasing from 0 to 30 % over this range. A 1 μm $Si_{0.7}Ge_{0.3}$ relaxed buffer was grown next. Next, a 5 nm thick layer of $Si_{0.7}Ge_{0.3}$ was grown; this layer was Sb-doped to 3e18/cm3. This was followed by an undoped 3 nm thick $Si_{0.7}Ge_{0.3}$ spacer and the 8 nm undoped strained Si channel. A 5 nm thick $Si_{0.7}Ge_{0.3}$ barrier layer and 10 nm thick silicon cap completed the epitaxy.

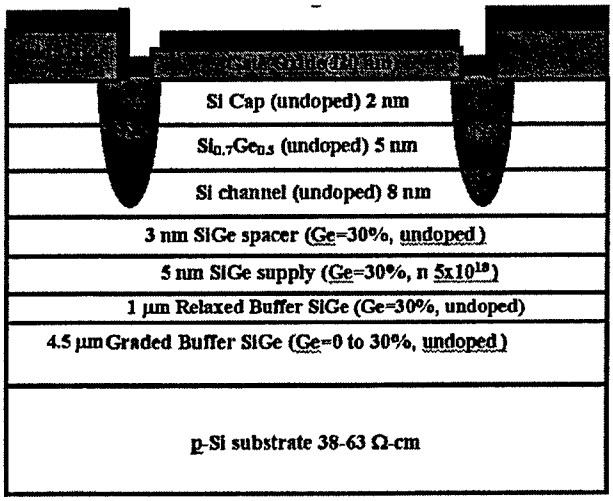
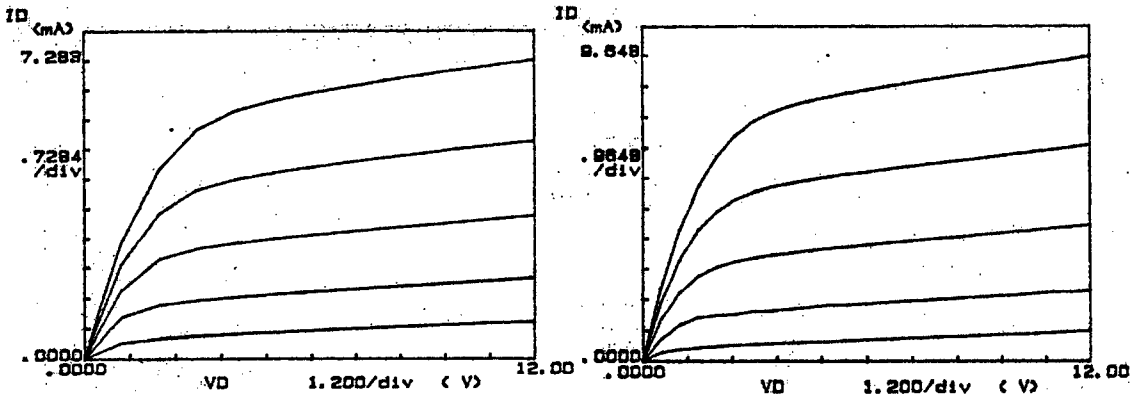


Fig 4: Device cross-section

The cross section of the device is shown in figure 4. The MBE grown structure was cleaned with hot isopropanol, acetone and methanol. No HF dip was performed to protect the thin Si (10 nm) cap layer. Device fabrication was started with a RIE mesa etch to isolate individual devices. The RIE was performed with CF4 at 80 sccm, O2 at 6 sccm, 100 millitorrs and 50 W for 30 seconds. After the mesa etch, a 5000 Å field oxide was deposited by PECVD at 275° C. The parameters for this deposition were SiH_4 at 15 sccm, N2O at 33 sccm, RF power 100 W for 16 minutes. Measured oxide thickness was 5100 Å. Windows were then etched in the field oxide with buffered HF (BHF) to define the source and drain regions. Ion-implantation simulations performed by using the SRIM program [7] to determine dose and energy for the formation of suitable ohmic contacts. The source and drain were formed by ion-implantation with phosphorus at 25 keV at a dose of 3e15/cm2, with a tilt angle of 7 degrees. The gate region was then opened by etching with BHF and the wafer was subjected to thermal oxidation at 750° C: 45 minutes in dry O_2, 45 minutes in steam, then 1 hour in dry O_2. The three oxidation times were obtained from SUPREM simulations. This thermal oxidation step also serves to activate the phosphorus implant. Measured oxide thickness was 200 Å. This gate oxide was then thickened to 1200 Å by plasma enhanced chemical vapor deposition (PECVD) (SiH_4@15 sccm:N_2O@33 sccm, RF power 100 W) at 275° C. The wafer was then annealed in H_2 at 350° C for 30 minutes to improve the oxide quality. A lift-off process was used for metallization. Contact cuts were etched with BHF and metal evaporated to form the drain, source and gate contacts. 500 Å of Al/2%Si were deposited, followed by 3500 Å of Au, without breaking vacuum. The thick Au layer facilitates wirebonding. Excess metal was lifted off in warm acetone with slight ultrasonic agitation.

5. RESULTS

The finished device was mounted on a 24 pin metal DIP package with conductive adhesive. The pads on the device were bonded to the package pins with 25 μm gold wire. The packaged device was mounted on the cold head of a CTI-Cryogenics Model 22 helium refrigerator. A HP 4145B semiconductor parameter analyser was used to obtain current-voltage characteristics.



(a) (b)

Figure 5: (a) Current-voltage characteristics of 6 μm x 125 μm device at 190K and (b) at 90K

The devices worked throughout the 300 K – 90 K temperature range. Figure 5(a) and figure 5(b) show the current-voltage characteristics of finger of the 6 μm x 1mm device at 190 K and at 90 K. The drain-source voltage is swept from 0 V to 12 V, which the gate-source voltage is increased from 0 V to 4 V in steps of 1 V. Figure 6 shows the relation of maximum drain current to temperature for this device, at a drain bias of 14 V and a gate bias of 5 V. At 300 K, the drain current was 7.2 mA. The current rises steadily with decreasing temperature to a maximum value of 9.6 mA at 90 K, an increase of approximately 40 %. The increase in current is due to an increased electron mobility, which in turn is due to reduced phonon scattering at lower temperatures.

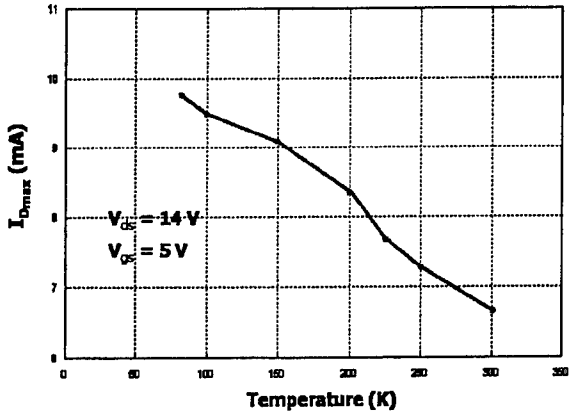
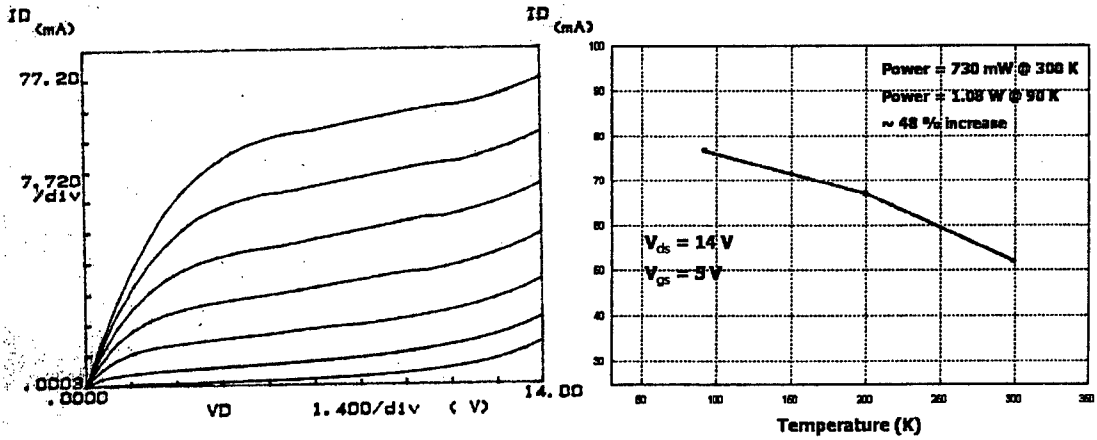


Fig 6: I_D vs. Temperature, 6 μm x 125 μm

Figure 7(a) shows the current-voltage characteristics of the complete 1 mm device at 90 K. The drain-source bias is swept from 0 to 14 V, and the gate-source voltage is increased from -1 V to 5 V in 1 V steps. Figure 7(b) shows the relation of maximum drain current to temperature, at a drain bias of 14 V and a gate bias of 5 V. At 300 K, the drain current was 52 mA, corresponding to a power of 0.7 W. The current rises steadily with decreasing temperature to a maximum value of 77 mA at 90 K, corresponding to 1.08 watts. Thus the current increases by approximately 48 % as the temperature is reduced from 300 K to 90 K. The devices exhibited a threshold voltage of -1 V. The maximum transconductance was found to be 13 mS/mm.



(a) (b)

Figure 7: (a) Current-voltage characteristics of 6μm x 1 mm device at 90K and (b) Variation of drain current vs. temperature for the same device

The drain-source breakdown voltages were 14 V, while gate breakdown voltages were greater than 30 V. The gate leakage current at V_{GS}=10 V was found to be less than 1 nA. The gate-to-body capacitance C_{GB} was found to be 1.4 pF.

The devices were then tested in a simple class-A amplifier circuit, where they produced an output of 9 mA p-p at 3 V for an input of 3 V, 1 μA p-p, indicating significant power gain.

6. CONCLUSION

6 μm x 1 mm silicon-germanium based n-channel MOS-MODFETs were fabricated and tested from 300 K down to 90 K. The devices were found to produce superior I-V characteristics throughout this temperature range. The viability of using n-channel silicon-germanium heterostructure based MOS-MODFETs for higher-power applications at cryogenic temperatures have been demonstrated. The lower leakage current of the MOS-MODFET structure as compared to MODFETs is invaluable at the relatively high gate biases that a 1-watt transistor may frequently be subject to.

Research funded by NASA grant.

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MMIC Compatible AlSb/InAs HEMT with Stable AlGaSb Buffer Layers

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Abstract

In this paper, we present state-of-the-art f_T and f_{max} results of 130 GHz, and 110 GHz for AlSb/InAs HEMTs with AlGaSb/AlSb metamorphic buffer layers that demonstrate InAs-channel HEMTs that are stable with exposure to air and are compatible with standard MMIC production processes.

I. Introduction

Monolithic Millimeter-wave Integrated Circuits (MMIC) based upon InAs-channel HEMTs have the potential to enable revolutionary low-noise, low-power, and high-speed applications due to higher electron mobility and velocity that can be achieved in InAs, compared to those of current state-of-the-art $In_XGa_{1-X}As$-channel HEMTs. However, InAs-HEMT growth is complicated by the lack of viable 6.05 Å substrates for lattice-matched growth. Metamorphic growth on GaAs substrates using the $Al_XGa_{1-X}Sb_YAs_{1-Y}$/InAs material system, which has a near 6.1 Å lattice constant, has proven to be a viable alternative for state-of-the-art AlSb/InAs HEMTs [1-5]. However, many of these AlSb/InAs HEMTs [1-4] had employed relaxed AlSb buffers that gradually disintegrate in air, due to the reactivity of AlSb with water. Because of this, previous devices required a deep mesa isolation step to etch away the AlSb buffer outside of the active device regions. This step must be performed after gate and ohmic formation, making the integration of standard MMIC components very difficult because of the non-planar topography after deep mesa etching.

In this paper, we report DC and RF device performance of AlSb/InAs HEMTs that employ a stable $Al_{0.7}Ga_{0.3}Sb$ insert on top of the AlSb buffer. The new insert enables a shallow 1000 Å mesa isolation etch before gate and ohmic formation and provides a method of device formation that is completely compatible with our existing space-flight qualified production MMIC processes. Furthermore, the AlGaSb surface remains stable in air.

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II. Device Fabrication

The AlSb/InAs structure was grown by molecular beam epitaxy (MBE) on semi-insulating 2" GaAs substrates. Hall measurements on the as-grown wafer revealed a 300 K mobility of 12,500 cm^2/Vs and an electron sheet density of 1.45 x 10^{12} cm^{-2}. The structure was designed to achieve high transconductance while mitigating the effect of impact ionization at higher drain biases; a requirement for taking full advantage of the electron velocity vs electric field characteristics of InAs for high-speed devices. This is achieved through a combination of an InAs subchannel, and a lightly p-doped GaSb hole drain layer [3-4]. A schematic of the layer structure is shown in Figure 1 that illustrates the incorporation of these features.

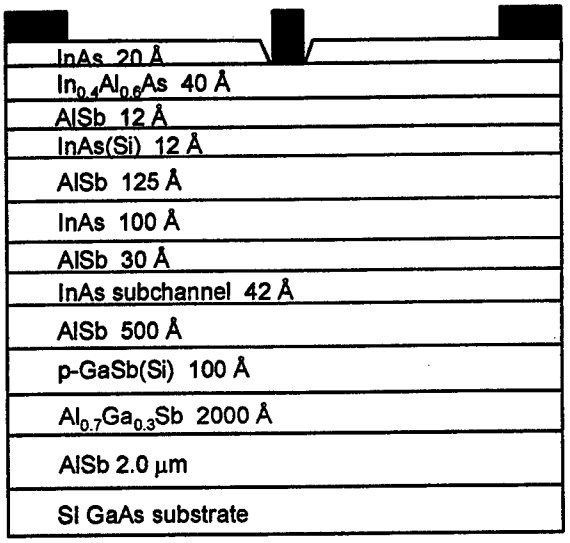


Figure 1. Schematic of the AlSb/InAs HEMT structure.

Active device mesas were formed by using a hydrofluoric acid based non-selective etch to remove ~1000 Å of the structure. The mesa isolation process was designed to end in the $Al_{0.7}Ga_{0.3}Sb$ layer, and has achieved 670 KΩ/sq of electrical isolation resistance without the need for implant isolation. This level of isolation is comparable to TRW's space-qualified, production InAlAs/InGaAs HEMTs on InP substrates that employ both mesa isolation and implant isolation. Pd/Pt/Au ohmics alloyed at 175°C in a nitrogen atmosphere formed contacts with a resistance of 0.14 Ω-mm. Electron beam lithography was utilized to fabricate 0.15 μm Pt/Au T-gates in a 2 μm source-drain region. The source to gate distance was 0.8 μm. A tilted-view SEM of a completed device is shown in Figure 2, which shows the shallow step of the 0.15 μm gate length T-gate down to the AlGaSb mesa floor.



Figure 2. Scanning electron microscope photo showing a tilted-view of 0.15-μm T-gate over shallow mesa isolation etch step.

The devices were passivated with PECVD SiN and two levels of interconnect metal including airbridges were used for external connections. The AlSb/InAs HEMTs had a peak transconductance of 820 mS/mm with a drain bias of 0.75 V and a drain current of 100 mA/mm; 600 mS/mm with a drain bias of 0.5V, 120 mA/mm. Figure 3 shows the drain current vs drain voltage, and gate voltage, as well as the transconductance vs gate voltage.

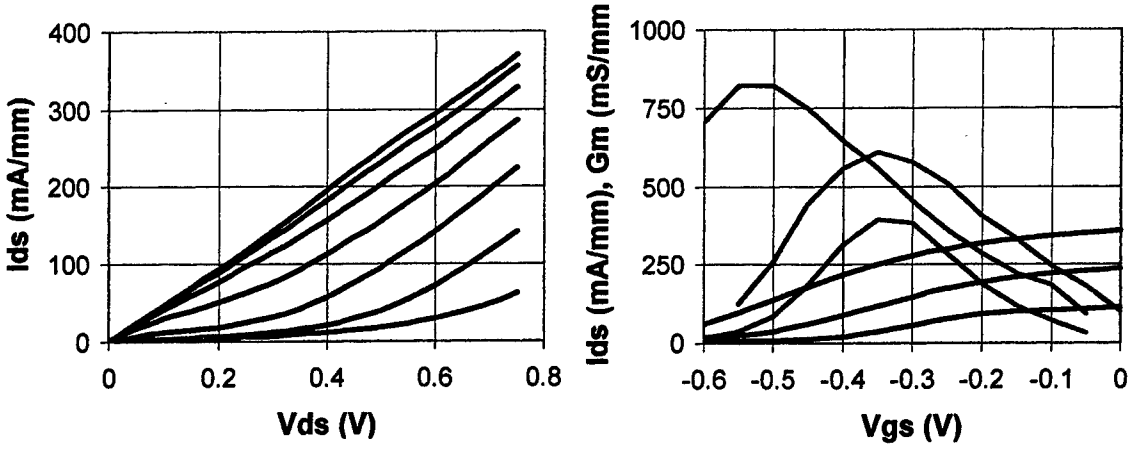


Figure 3. (Left) Ids vs Vds: top curve Vgs = 0V, steps of –0.1 V
(Right) Ids (Blue) and Gm (Red) vs Vgs: top curve Vds = 0.75 V, steps of –0.25 V.

III. Microwave Results

The two gate finger, 80 μm wide InAs HEMTs were measured for small-signal S-parameters up to 50 GHz. These devices achieved an extrinsic f_T of 130 GHz, and f_{max} of 110 GHz with a drain bias of 0.75 V and a drain current of 9.6 mA. At a drain bias of 0.5 V and a drain current of 12 mA, the devices achieved extrinsic f_T of 110 GHz, and f_{max} of 105 GHz. Figure 4 shows the measured h21, and unilateral gain versus frequency with the extrapolated roll-off to extrinsic f_T and f_{max}, for both bias conditions. The measured roll-off of h21 for the higher drain bias exhibits a slight deviation from ideal –6dB/octave behavior at lower frequencies because of the presence of gate-source and gate-drain conductance, caused by the onset of impact ionization.

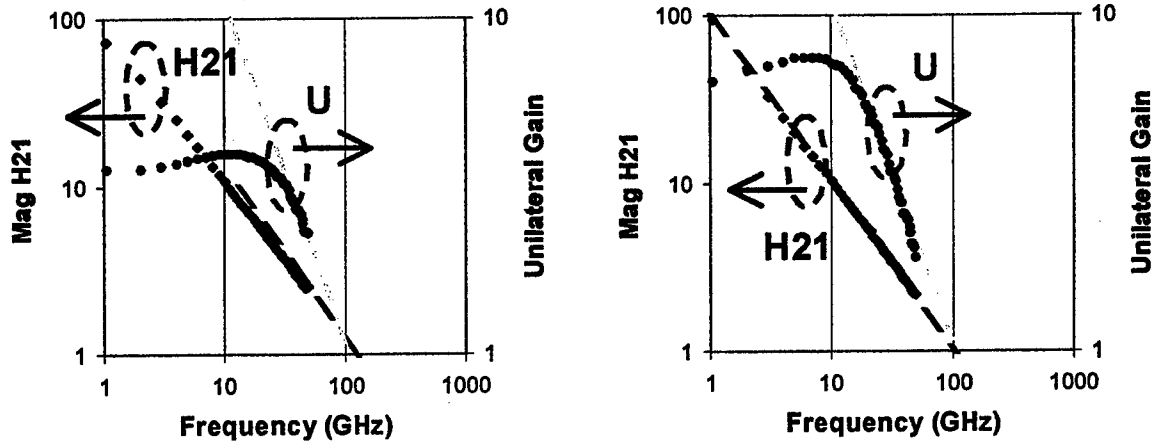


Figure 4. Magnitude of h21 and unilateral gain as a function of frequency, for:
(Left) device biased at Vds=0.75 V, Ids of 120 mA/mm. Extrapolated extrinsic f_T = 130 GHz, f_{max} = 110 GHz;
(Right) device biased at Vds=0.5 V, Ids of 150 mA/mm. Extrapolated extrinsic f_T = 110 GHz, f_{max} = 105 GHz.

The decrease in measured unilateral gain below 10 GHz is also caused by impact ionization current. At these frequencies, the impact ionization current adds to the drain current, but lags the gate-drain voltage waveform in phase. This results in a small-signal output resistance that has a complex impedance that is inductive, instead of capacitive, and has a reduced resistive component. This effect, coupled with other changes in S_{21} and S_{12}, cause the gain decrease.

By fitting equivalent circuit models to the measured s-parameter, we were able to estimate that the intrinsic f_T and f_{max} of these devices to be 160 GHz, and 190 GHz at the 0.75 V drain bias, and 135 GHz and 240 GHz at the 0.5 V drain bias. The small-signal model and topology for the 0.5 V drain bias data are shown in Figure 5. In these results, f_{max} is clearly limited by the sheet resistance of the starting material, which was ~340 Ω/sq. Lower sheet resistance

obtained either through higher electron sheet density or mobility, will reduce the extrinsic access resistances, R_s and R_d, and provide up to a two-fold improvement in f_{max}.

Linear Model		
Parameter	Value	Units
Cgs	0.05	pF
Cgd	0.015	pF
Cds	0.0107	pF
Gm	55	mS
Rds	75	Ω
Tau	0.1	pS
Rg	4	Ω
Rs	3	Ω
Rd	4.5	Ω
Ri	10	Ω
Rj	0	Ω
Lg	0.0041	nH
Ls	0.0006	nH
Ld	0.0105	nH

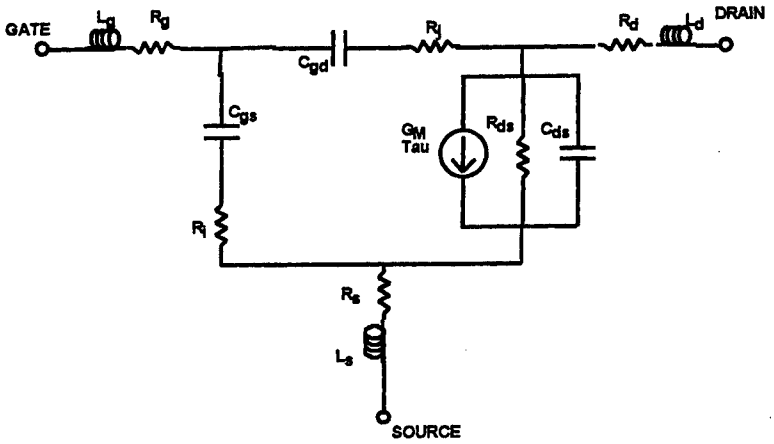


Figure 5. Small-signal model and topology for 2x40 μm device biased at 0.5 V, 150 mA/mm

Acknowledgements

This work was supported by ONR Cooperative Agreement No.: N00014-01-2-0014, DARPA ABCS Program

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DC and RF Performance of InAs-Based Bipolar Transistors at Very Low Bias

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Abstract

We fabricated metamorphic InAs bipolar junction transistors (BJTs) with a narrow bandgap in the base to reduce operating voltages, and we report RF results that we believe to be the first published for InAs-based bipolar transistors. InAs BJTs were grown by molecular beam epitaxy on InP substrates using strain-relief graded InAlAs buffer layers and optimized graded emitter-base and collector-base junctions. Large area devices (75×75 μm^2 emitter) exhibit DC current gain β of 85. Higher β exceeding 100 was observed from tunneling-emitter bipolar transistors with various InAlAs barrier designs, indicating lower holes injection from the base to the emitter. Small-area devices have been fabricated using the standard front-side process from our InP HBT line. Microwave properties measured from devices with emitter size of 1.5×10 μm^2 were very promising, showing a cutoff frequency over 50 GHz in devices with thick base and collector layers. An extremely low base-emitter voltage of 0.3 V was measured at peak frequency. These InAs-based bipolar transistors on InP substrates with good DC and RF performance demonstrate the viability of future narrow bandgap heterojunction bipolar transistors with state-of-the-art speed performance at low operating voltage.

I. Introduction

The indium arsenide (InAs) material system with lattice parameters that range from 6.0 to 6.058 Å has several unique advantages, including one of the highest electron mobilities of all III-V semiconductors, a low electron effective mass, a high peak velocity, and a narrow energy bandgap less than 0.5 eV. These properties indicate a great potential for future bipolar electronic devices and circuits with very high frequency operation and very low power dissipation.

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InAs and GaSb substrates are available for growing 6.058 and 6.096 Å epitaxial materials, respectively, and InAs-based bipolar transistors including InAs Bipolar Junction Transistors (BJTs) and InAlAs/InAs Heterojunction Bipolar Transistors (HBTs) have been previously demonstrated on InAs substrates with excellent DC characteristics [1,2]. However, the very high conductivity associated with these substrates prevents their use for microwave applications. Motivated by lower cost and greater mechanical robustness, metamorphic *InP*-based bipolar transistors grown on GaAs substrates have been developed in the past few years with continuous improvement of DC and RF performance [3-5]. The approach selected in this work uses similar metamorphic strain-relief compositionally graded buffer layers (GBLs) grown on semi-insulating InP substrates to produce virtual substrates with desired lattice parameters for subsequent fully-relaxed device epilayer growth, opening the possibility of high-frequency operation with good device isolation and low parasitic capacitance for 6.0 to 6.058 Å bipolar transistors. In this paper, we report the fabrication of metamorphic InAs-based bipolar transistors grown by molecular beam epitaxy on InP substrates, with promising DC and RF characteristics observed from InAs BJTs and InAlAs/InAs Tunneling-Emitter Bipolar Transistors (TEBTs).

II. Growth Optimization and Device Fabrication

The initial effort of this work has focused on fabricating high quality InAlAs metamorphic GBLs to create suitable substrates (6.058 Å lattice constant) for subsequent device epitaxial growth with minimal surface roughness and dislocation density. The metamorphic buffers and device layers were grown using a GEN II molecular beam epitaxy system. This virtual substrate technique allows the use of readily available, high quality, semi-insulating InP substrates for relaxed InAs-based devices. InAlAs was chosen over InGaAs for the buffer grade because its larger band gap creates a less conductive substrate. The metamorphic epitaxial layer growth of compositionally Al graded buffer layer slowly changes the lattice parameter with increasing layer thickness by fostering elongation of strain-relieving misfit dislocation segments. The substrate temperature and the grading profile were optimized to reduce the surface roughness associated with subsequent growth over strain relieving defects. The total InAlAs buffer layer was 1.2 μm thick, subdivided by three step-graded segments (with equal compositional grades in each segment) to accommodate the lattice-mismatch between InP and InAs. Then, a 3000 Å InAs layer was grown to terminate the buffer layer structure. The surface morphologies of the metamorphic structure exhibited the characteristic cross hatch pattern of relaxed metamorphic growth. Typical root-mean-square roughness of 6.5 nm was observed from atomic force microscopy images with GBL optimal growth conditions, as shown in Figure 1. The growth optimization of the GBL results in bending most of the dislocations in the buffer, as confirmed by the cross-sectional scanning transmission electron microscopy (STEM) image in Figure 2, which shows only few threading dislocations propagating through the active device.

The remaining InAs bipolar transistor layers were grown on top of the optimized GBL structure during the same growth cycle. Lattice-matched InAs bipolar junction transistors (BJTs) were investigated first. The epitaxial structure of the InAs BJTs begins with a 5000 Å (n^+ 1×10^{19} cm^{-3}) sub-collector, a 5000 Å unintentionally doped collector, and a 1000 Å (p^+ 1×10^{19} cm^{-3}) base layer with graded setback layers on both ends to reduce dopant diffusion. The device structure is terminated by an 800 Å (n^- 5×10^{17} cm^{-3}) emitter layer followed by a 1000 Å n^+ emitter cap. In addition to the baseline InAs BJT structure, InAlAs barrier layers with various combinations of Al composition and thickness have been introduced at the emitter-base junction forming InAlAs/InAs Tunneling-Emitter bipolar transistor structures. Inserting a thin tunneling barrier in a normal homojunction bipolar transistors will enhance the emitter injection efficiency by taking advantage of a large difference in the tunneling probabilities for electrons and holes in the barrier layer [6]. Two TEBT structures were grown with the exact same InAlAs barrier thickness of 35 Å but different aluminum compositions (8 and 30 %) while a third structure had a thicker InAlAs barrier of 100 Å with only 8 % aluminum content.

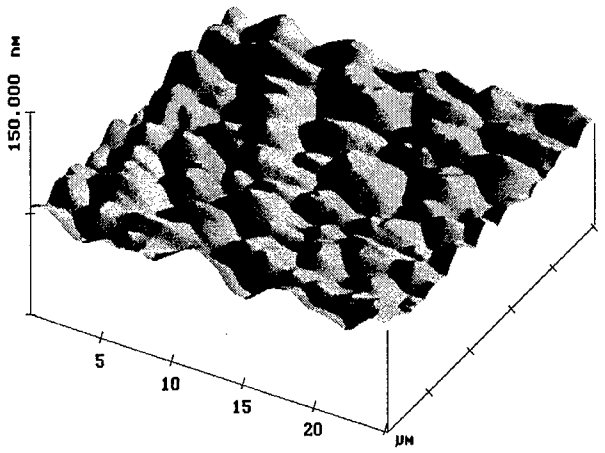


Figure 1: AFM surface map (25×25 µm) of the 1.5 µm undoped InAlAs graded buffer layer, with 6.5 nm RMS.

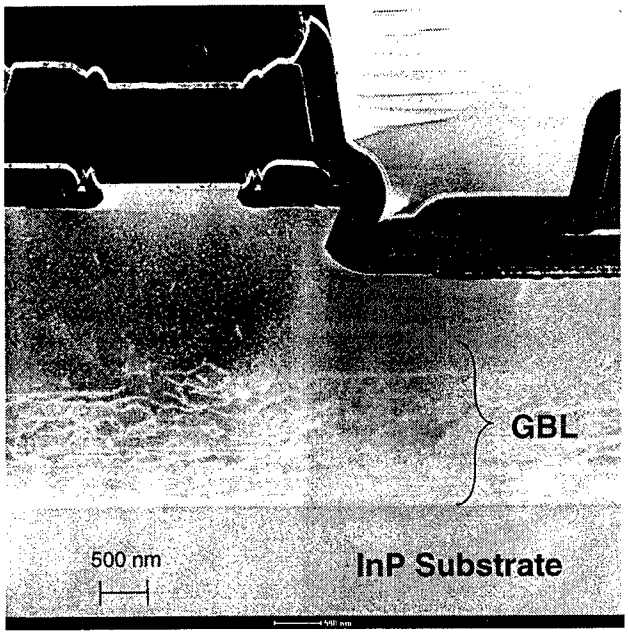


Figure 2: Cross-sectional STEM image of a processed InAs BJT grown on top the InAlAs graded buffer layer. Very few dislocations are present at the surface of the GBL.

Small-area devices with emitter dimension varying from 1.5×4 to 1.5×20 μm^2 were fabricated using our standard robust high-yield InP HBT front side process that was described in detail previously [7], with some differences in wet etch chemistry. Process highlights include a self-aligned base metal, wet-etched mesas, silicon nitride passivation, and two layers of gold interconnect metal with airbridge crossovers. In order to

ensure a good isolation for the metamorphic bipolar transistors, the isolation etch was required to extend into the InAlAs graded buffer layer, resulting in a much taller isolation mesa compared to traditional InP technology. Large-area devices (with active emitter area of 75×75 μm^2) were also fabricated to evaluate the metamorphic device quality.

III. Device Results

A room temperature DC current gain β of 85 was observed from the baseline InAs BJT device (with emitter size of 75×75 μm^2), which is excellent for such a homojunction structure with a relatively thick (1000 Å) InAs base layer. The graded profile present in the setback layer at the emitter-base junction helped reducing the hole injection to the emitter for a better emitter carrier injection efficiency. The use of a narrow band gap InAs collector layer results in excess leakage at the base-collector junction and limited breakdown characteristics are reported from common emitter I-V measurements. Improved breakdown properties have been recently observed by replacing the InAs collector by ternary $In_{0.9}Al_{0.1}As$ that shows a breakdown voltage exceeding 2 V. The DC gain versus the base-emitter voltage V_{BE} observed from the baseline transistor is compared in Figure 3 with the various TEBT structures with identical emitter size. The TEBT structure with an $In_{0.70}Al_{0.30}As$ barrier exhibits a maximum gain below 40. This limitation could suggest that the InAlAs barrier has exceeded the pseudomorphic critical thickness of InAlAs on InAs, resulting in inferior growth quality. Values of β approaching 100 are reported from TEBT structures with less aluminum in the barrier layers (8%), demonstrating the benefit of the wide band gap barrier in reducing holes injection into the emitter. This moderate improvement over homojunction structures indicates that the current gain is mostly dominated by transport base rather than emitter injection efficiency.

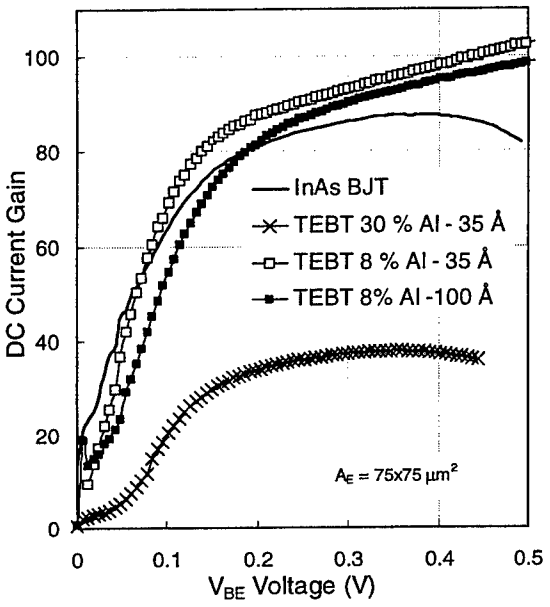


Figure 3: DC current gain versus V_{BE} measured from a baseline InAs BJT and various Tunnel Emitter Bipolar transistor (TEBT) structures.

Figure 4 shows the common-emitter I_C-V_{CE} characteristics of the baseline InAs BJT with an emitter size of 1.5×10 μm^2. The breakdown properties slightly improve compared to that observed from a large area device. The Gummel plot is displayed in Figure 5 with a maximum gain of 25 at V_{BE} = 0.4 V. On-wafer microwave measurements have been performed. The peak cutoff frequency f_T and the maximum oscillation

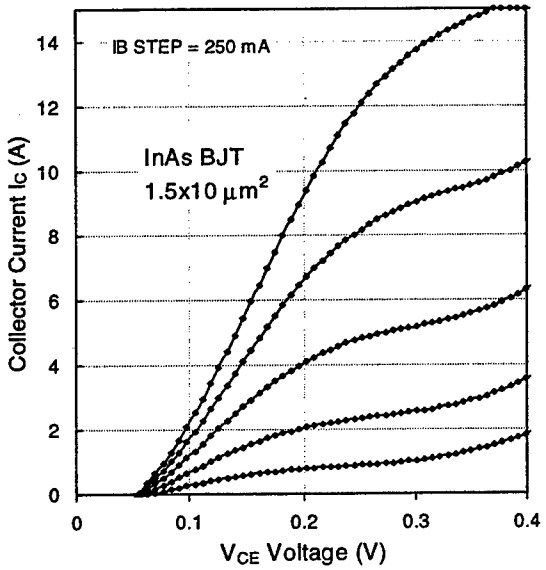


Figure 4: Common-Emitter I-V measurements for the InAs BJT (A_E = 1.5×10 μm^2).

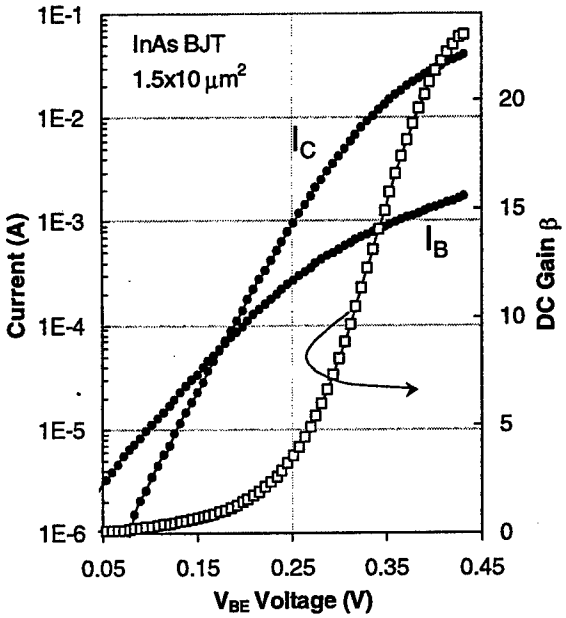


Figure 5: Gummel plot characteristics for the InAs BJT (A_E = 1.5×10 μm^2).

frequency f_{max}, extrapolated from measured small signal gains h_{21} and U, respectively, are plotted in Figure 6 as a function of the collector current and the base-emitter voltage. Preliminary microwave measurements reveal a peak f_T of 50 GHz and a peak f_{max} of 35 GHz. The f_{max} value is currently limited by the low doping concentration in the base used in this initial experiment. An extremely low base-emitter voltage V_{BE} of 0.3 V was measured at peak frequency, demonstrating the great potential of the InAs technology for reduced power dissipation of high-frequency circuits. This first microwave performance measured at very low operating voltage from a device that is not optimized for high-speed demonstrates the promise of this technology for efficiently reducing power consumption. Higher speed together with higher breakdown is predicted by using a more aggressive vertical epitaxial design for the base and collector layers and by introduction a large band gap material for the emitter and the collector.

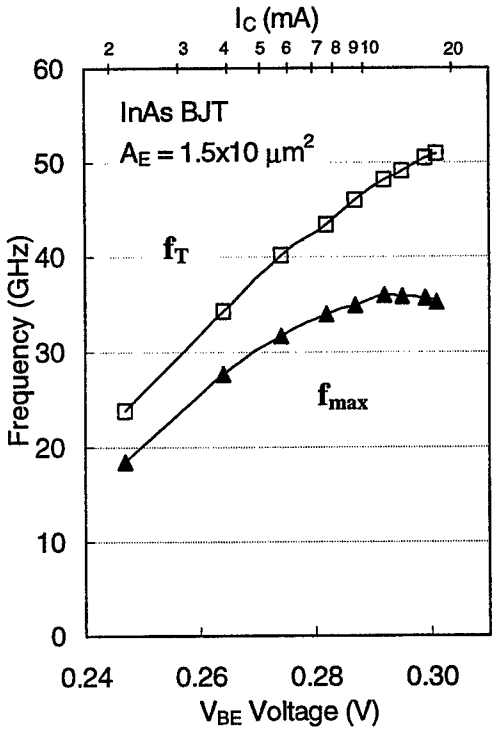


Figure 6: f_T and f_{max} as a function of the collector current and the base-emitter voltage for a 1.5×10 μm^2 InAs BJT.

IV. Conclusion

In conclusion, InAs-based bipolar junction transistors have been grown by molecular beam epitaxy on InP substrates. High quality InAlAs metamorphic grade buffer layers were used to create suitable substrates with 6.058 Å lattice constant. The substrate temperature and the grading profile were optimized to confine dislocations in the graded buffer, with limited surface roughness and reduced dislocation density. Large DC current gain values approaching 100 were measured from pure InAs bipolar junction transistors and InAlAs/InAs tunneling emitter bipolar transistors. Promising microwave performance with peak cutoff frequency of 50 GHz measured at very low operating voltage from InAs BJT structures not optimized for high-speed demonstrates the potential of this technology for reducing power consumption in next generation low power digital and microwave circuits.

Acknowledgments

This work is supported by ONR Contract No. N00014-01-2-0014, DARPA ABCS Program.

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AN InAs BASED TRANSISTOR APPROACH TO TERA-HERTZ ELECTRONICS: CONCEPTS AND MATERIALS SCIENCE

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0-7803-7478/02/$17.00 © 2002 IEEE

Antimony-based Quaternary Alloys for High-Speed Low-Power Electronic Devices

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Abstract

Heterojunction bipolar transistors using $In_zGa_{1-z}Sb$ for the base and $In_xAl_{1-x}As_ySb_{1-y}$ alloys for the collector and emitter have been explored. Modeling of the DC current-voltage characteristics indicate that current gain in excess of 500 may be obtained. The calculations show that the gain is a function of the base-collector conduction band offset. Molecular beam epitaxy (MBE) procedures for growing suitable alloys with a 6.2 Å lattice constant are under development. Double crystal X-ray diffraction, photoluminescence, Hall effect, and atomic force microscopy have been used to determine the quality of the materials grown. To minimize stress-induced defects, the $In_xAl_{1-x}As_ySb_{1-y}$ alloys were grown on undoped GaSb substrates with an AlSb buffer layer. The photoluminescence data indicate that good quality $In_xAl_{1-x}As_ySb_{1-y}$ (x=0.52 and y=0.3) with a band gap near 1 eV, is obtained using growth temperatures between 350 and 400 °C. Superior surface morphology is also found for growths in this temperature range. Te has been used to dope $In_xAl_{1-x}As_ySb_{1-y}$ n-type in the 10^{17} cm^{-3} range. Good diode characteristics with an ideality factor of 1.1 have been obtained for $In_xAl_{1-x}As_ySb_{1-y}$ p-n junctions grown using Te for the n-type dopant and Be for the p-type.

Introduction

InAs, AlSb, and GaSb are a group of binary semiconductors that are nearly lattice matched at 6.1 Å with a wide range of bandgaps and band offsets, as well as high electron and hole mobilities that make them desirable for use in high-speed low-power electronic devices. High electron mobility transistors[1,2] and resonant tunneling diodes[3-5] made with these binary alloys have been shown to have good operating characteristics. As part of an effort to enhance the performance of these devices and to make heterojunction bipolar transistors (HBT) in this system we have been developing MBE procedures to grow ternary and quaternary alloys with a lattice constant near 6.2 Å.[6] In addition, we have begun to use a two dimensional model to investigate possible HBT structures.

This report focuses on the effort to develop an npn HBT with superior high-speed operating characteristics at low collector-emitter voltages to minimize power dissipation. Based on a survey of materials and band offsets a material system with a lattice constant near 6.2 Å has been chosen as a starting point. InGaSb has been chosen for the base because of its small bandgap and to exploit the good hole transport characteristics of these alloys. In

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addition, it should be easy to form low-resistance ohmic contacts to InGaSb. These properties are important factors in minimizing the base resistance. Equally important is the fact that a narrow bandgap InGaSb base can be used with a collector and an emitter made from a variety of InAlAsSb alloys. While little is known about the details of the band offsets and bandgaps of these materials, extrapolations from known binary and ternary alloys indicate that it should be possible to have a large valence band offset of 300 mV or more over

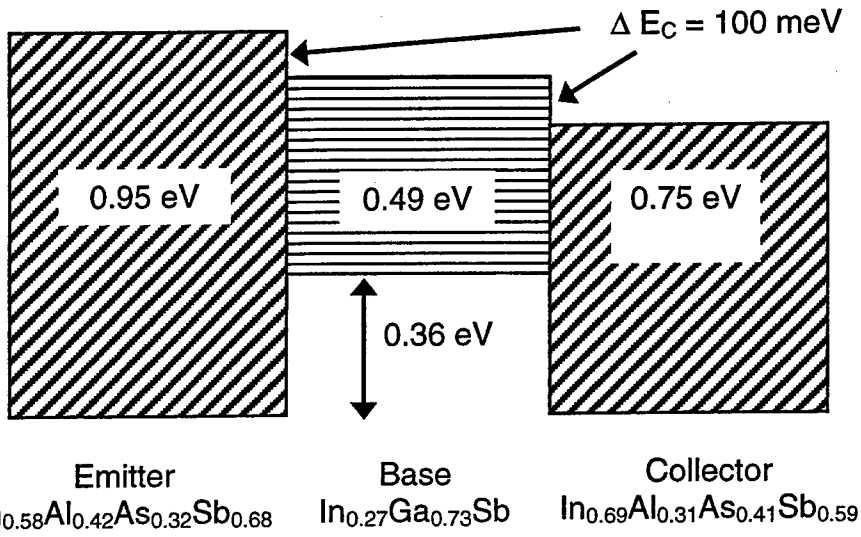


Fig. 1. An example of a possible npn HBT with an InGaSb alloy base and different InAlAsSb alloys for the emitter and collector in order to tailor the conduction band offsets at both the emitter-base and collector-base junctions.

a wide range of InAlAsSb alloys, particularly with alloys having a 6.2 Å lattice constant.[7,8] This is important in minimizing the parasitic hole current flow from the InGaSb base to the emitter. The InAlAsSb alloys are predicted to be a direct bandgap semiconductor over a range of bandgaps from 0.2 to 1.4 eV. This leads to a wide range of possible conduction band offsets with the InGaSb base because the valence band offset is almost insensitive to the InAlAsSb composition. The above listed properties allow a great deal of latitude in using band structure engineering to optimize HBT performance. An example of the core emitter-base-collector structure of a possible HBT is illustrated in Fig. 1. A more complete picture would include other layers outside the emitter and collector region shown here. These layers would be used to obtain low resistance contacts to the emitter and collector and not considered here as this paper deals with the development of emitter-base-collector heterostructure.

Silvaco's ATLAS device simulator has been used to model HBTs composed of a variety of possible alloy combinations with the material combinations illustrated in Fig. 1 chosen as a starting point. Because of uncertainties in the material properties these calculations should be regarded as preliminary in nature and most useful for understanding the device physics and the dependences of the device characteristics on the various material

parameters. To keep things simple, a drift-diffusion model was employed with mobility

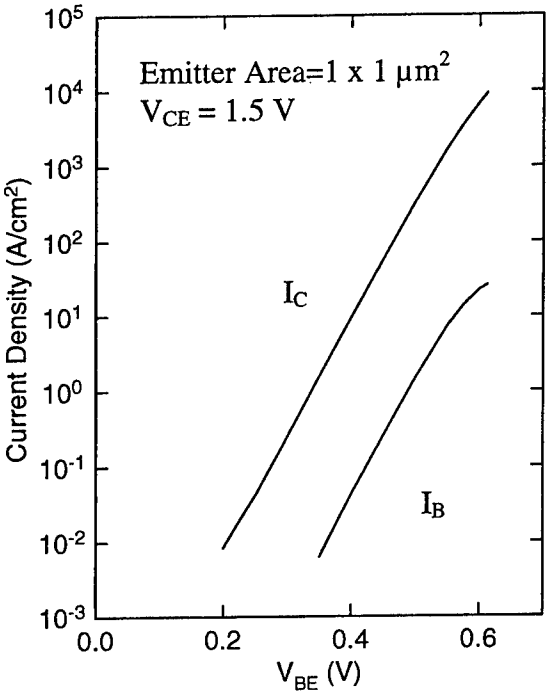


Fig. 2. Gummel characteristics for the layer structure in Fig. 1.

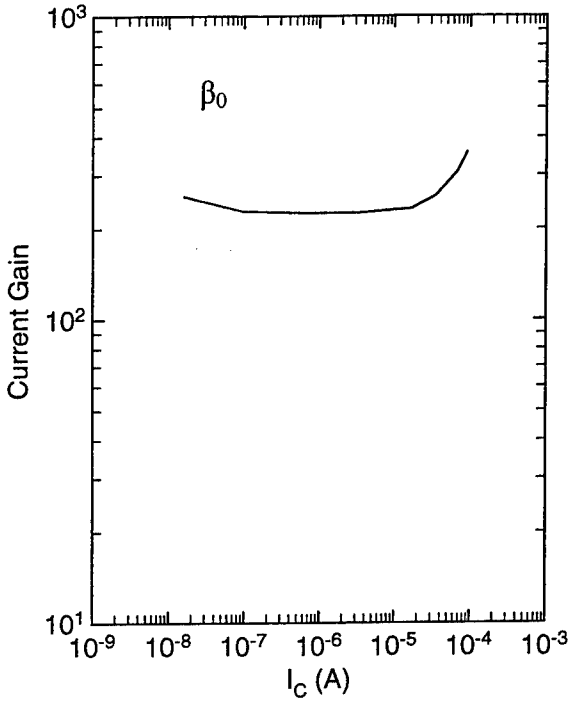


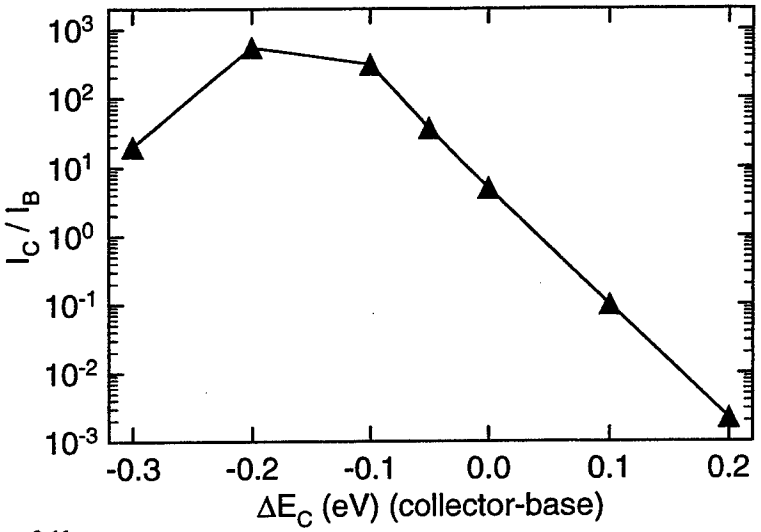
Fig. 3. DC gain obtained from I_C and I_B in Fig. 2.

models appropriate for III-V materials. Non-stationary transport effects are undoubtedly important in these devices and will be included in the future in the hydrodynamic approximation. The Gummel characteristics illustrated in Fig. 2 and the DC current gain in Fig. 3 were generated with this model for the alloy combinations in Fig. 1. The collector current in Fig. 2 is found to depend exponentially over many orders of magnitude on the emitter-base bias, and to reach a peak value over $2x10^4$ A/cm^2. As the development of this HBT is in its infancy we consider this to be a good start as it is near $1x10^5$ A/cm^2, the current density desirable for high frequency operation. The DC current gain found from Fig. 2 is shown in Fig. 3 to be greater than 200 and nearly constant over 4 orders of magnitude of the collector current. Fig. 4 illustrates that a DC gain greater than 500 may be obtained with the collector conduction band chosen to be 200 mV below the base conduction band. This result emphasizes that the conduction band offset between the base and collector plays a significant role in determining the DC gain, and the advantage of being able to tailor it in this material system.

The possibility of having high-performance HBTs in the antimonide materials system has led to the development of MBE methods for growing alloys like those illustrated in Fig. 1. This material system offers a vast parameter space to investigate, including the use of alloys at lattice constants other than those at 6.2 Å being investigated here. A number of problems need to be resolved in the development of the MBE growth of InAlAsSb with the

compositions of interest here. Miscibility gaps are believed to exist for these alloys that

Fig. 4. The model prediction for the dependence of the DC current gain, I_C / I_B, on the collector-base conduction band offset.

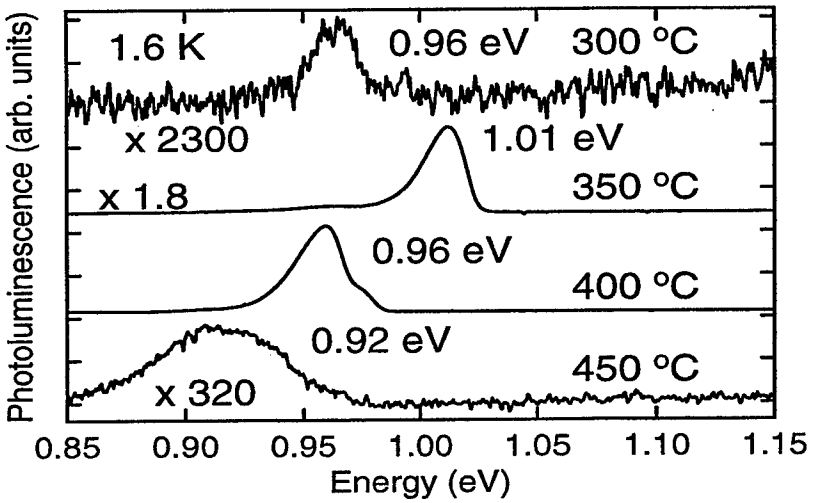


would make them difficult to grow.[9-11] If reasonable materials can be grown then methods need to be developed to dope them. A semi-insulating substrate is required for complex circuits, and none exist with a lattice constant near 6.2 Å. Therefore an effort needs to be made to produce either metamorphic growth procedures on semi-insulating substrates, or wafer bonding techniques.

Materials Growth

The MBE growth effort has focused on determining methods for growing good

Fig. 5. Photoluminescence measured at 1.6 K for samples grown at 300, 350, 400, and 450 °C. Each spectrum was scaled to have the same amplitude in the above plot.



quality $In_{0.52}Al_{0.48}As_{0.25}Sb_{0.75}$ that is an alloy close to that suggested for the emitter in Fig. 1. The growth temperature, As to Sb ratio and total As plus Sb flux are parameters of concern. GaSb with a lattice constant of 6.0954 Å has been chosen as the substrate as it is

commercially available. An effort is under way to develop methods for the metamorphic growth of the desired alloys on semi-insulating InP. The growths shown below were done with a 2 μm AlSb buffer, lattice constant 6.1355 Å, grown on an unintentionally doped GaSb substrate to accommodate part of the lattice mismatch between GaSb and the alloy at 6.2 Å. Part of the reason for choosing a 6.2 Å lattice constant was to minimize the mismatch with the available substrates while trying to use a narrow bandgap InGaSb base with a large valence band offset with the InAlAsSb alloys.

The growth temperature study consisted of investigating a series of $In_{0.52}Al_{0.48}As_{0.25}Sb_{0.75}$ samples at substrate temperatures of 300, 350, 400 and 450 °C while keeping the other parameters fixed. The temperature was determined by using RHEED to monitor the 5x to 3x reconstruction transition[12] after growing a few nm of GaSb on the GaSb substrate at the start of a growth. The $In_{0.52}Al_{0.48}As_{0.25}Sb_{0.75}$ layer was 2 μm thick with the first 1 μm doped with Te at $5x10^{16}$ cm^{-3} and the top 1 μm doped with Be at $1x10^{18}$ cm^{-3} to form a p-n junction. Photoluminescence (PL) measurements at 1.6 K were used to examine

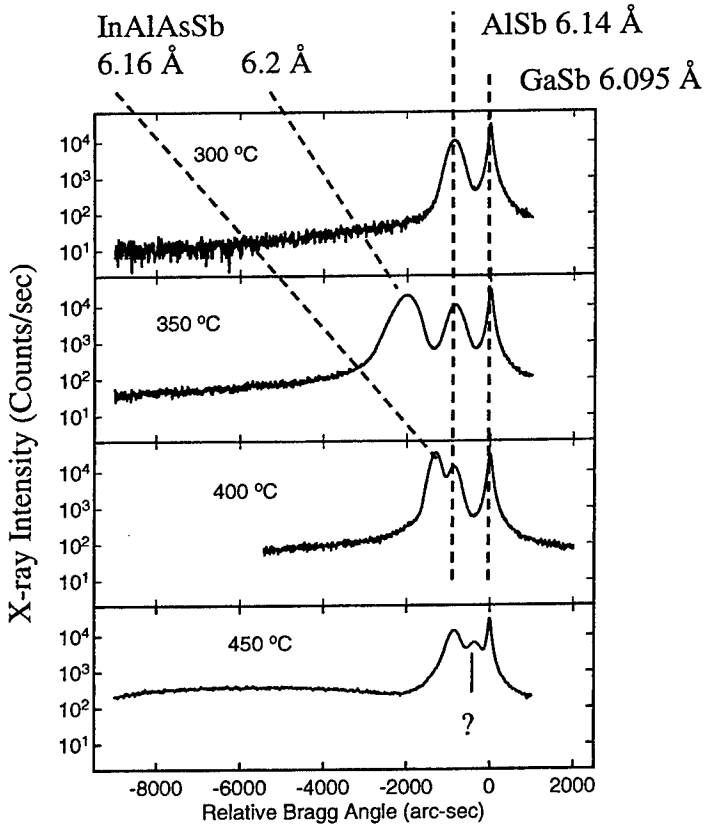


Fig. 6. Double crystal X-ray diffraction for samples grown at 300, 350, 400, and 450 °C.

the quality of the material and to determine the bandgap. The samples grown with substrate temperatures of 300 and 450 °C exhibited poor material quality as illustrated by the weak PL intensities in Fig. 5. Significantly more intense PL spectra are illustrated in Fig. 5 for the

samples grown at 350 and 400 °C indicating that much higher quality material is grown in this temperature range. The spread in peak energies is an indication of the variation in composition from growth to growth. Additional work needs to be done to determine whether the variations in peak energies reflect differences in the group III or V composition or a combination of both. Weak shoulders similar to the one on the high-energy side of the 400 °C spectra are often found though sometimes they are on the low energy side of the dominant peak.

The double crystal X-ray diffraction data illustrated in Fig. 6 for these samples also indicates that the best material is grown at temperatures between 350 and 400 °C. For these temperatures there are peaks in the spectra at 6.2 Å and 6.16 Å respectively due to the InAlAsSb layer. To account for both the difference in PL energy and lattice constant for the 350 and 400 °C samples requires slight differences in the Al to In ratio and the As to Sb ratio based on the predicted bandgap dependence on composition. The spectra for the 450 °C sample has a broad feature in the region corresponding to lattice constants longer than 6.2 Å, and a line near 6.1 Å that has not been found in any other samples. The X-ray data for the 300 °C sample lacks any sign of an InAlAsSb layer.

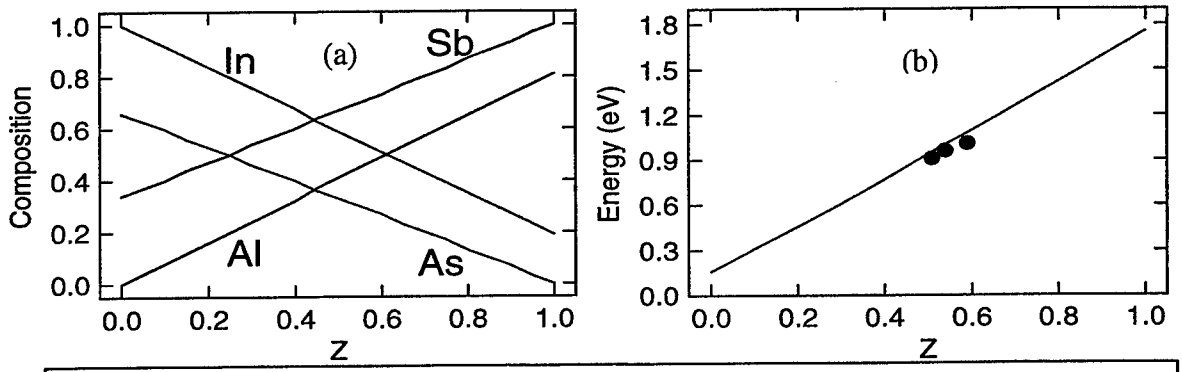


Fig. 7. (a) Dependence of composition for 6.2 Å InAlAsSb alloys on parameter, Z. (b) Comparison of the predicted dependence of the bandgap on Z, solid line, with experimental data, solid circles.

PL and X-ray measurements are not sufficient to determine the composition of these alloys. It is particularly important to know the composition in order to determine the factors controlling the incorporation of Sb and As. SIMS measurements have been performed on several samples to aid in understanding this problem, and to use with the PL data to compare the available predictions for the bandgap as a function of composition. The SIMS data gave $In_{0.53}Al_{0.47}As_{0.27}Sb_{0.73}$ for the 350 °C sample while the growth parameters were set for $In_{0.52}Al_{0.48}As_{0.25}Sb_{0.75}$. Similar variations in composition have been found for other growths. The predictions of Glisson et al.[7] for the bandgap dependence on the composition of alloys with a 6.2 Å lattice constant have been compared with our data. To make this comparison, Glisson's composition and bandgap data have been parameterized in terms of Z as shown in

Fig. 7a, for the composition and in Fig. 7b by the solid line for the bandgap. The three black dots in Fig. 7b are experimentally determined from our data. A value of Z was found for each sample using Fig. 7a and the compositions determined by SIMS. The corresponding PL peak energies were used as a measure of the bandgaps. These three points are in reasonable agreement with the prediction represented by the solid line. Additional work needs to be done to better understand the PL mechanisms. The PL may not be due to a band-to-band recombination process, but to another process such as donor-to-acceptor, that would under estimate the bandgap energy.

Atomic force microcopy was used to measure the topography of the samples, as surface roughness is an important consideration in determining the usefulness of the material in device applications. The RMS roughness for 5x5 μm^2 areas is 2 nm for the 350 and 400 °C samples and 12 nm and 33 nm for the 450 and 300 °C samples, respectively. These results further support the observation that the growth window for the best quality material is between 350 and 400 °C. The surface features for the samples with 2 nm RMS were elongated and mainly aligned in one direction. Additional work needs to done to understand the implications of this in terms of growth mechanisms and residual strain in the layers.

An npn HBT in this system requires an n-type dopant for the InAlAsSb alloys. Si is an amphoteric dopant in III-V compounds, yielding n-type conductivity in (In, Ga, Al)As but p-type in GaSb and AlSb. It was tried, but did not yield n-type material for the alloys of interest. A GaTe source was installed in the MBE to use Te for the n-type dopant.[13] Hall effect measurements on two InAlAsSb layers indicated an electron concentration of $4x10^{17}$ cm^{-3} when grown with the GaTe cell temperature of 450 °C. This is somewhat higher than the $2x10^{17}$ cm^{-3} found for GaAs doped using the same GaTe cell temperature. The GaAs

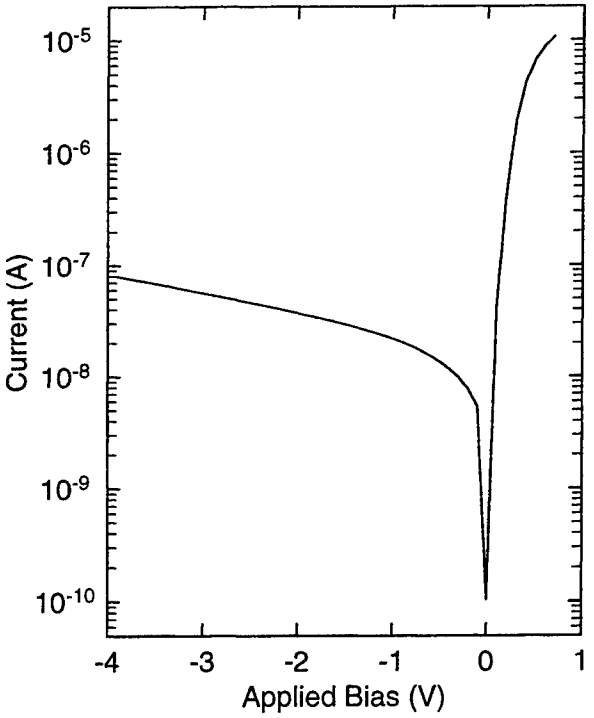


Fig. 8. Current-voltage characteristics for a mesa diode with an area of 80x125 μm^2 on the layer grown at 400 °C.

(Te) calibration data and the one InAlAsSb (Te) point were used to estimate the GaTe cell temperature used to dope the top layer of these samples to $5x10^{16}$ cm^{-3} to form p-n junctions.

Optical lithography and wet chemical etching were used to define mesa diodes on the at 400 °C is illustrated in Fig. 8. The ideality factor of 1.1 found for this data indicates a good quality diode. The slight turn over at high currents for positive bias is due to series resistance effects, due in part to the poor ohmic contact to the InAlAsSb layer. I-V probe measurements of the Be doped top layer indicate that the contacts to this layer have a low resistance and is not a significant problem here. At a reverse bias of 4 V, the leakage current density of $1x10^{-11}$ A/cm^2 also indicates a good quality p-n junction, particularly considering it has a very large area.

Summary

An effort to develop an InAlAsSb/InGaSb HBT for low-power, high-speed operation has been described. Preliminary simulations indicate that the DC current gain is a function of the base-collector conduction band offset, and that gains as high as 500 are possible. Present knowledge of the bandgaps and band offsets indicate that the alloy compositions can be tuned to obtain the desired offsets and bandgaps. MBE techniques for growing the desired alloys are being developed. The substrate temperature during growth is an important factor, and a growth window has been found. SIMS data indicate that the compositions are close to those intended by the growth parameters. They are also proving to be useful in determining the limits in variation of the composition that can be tolerated in order to obtain reproducible lattice constants and bandgaps. The SIMS composition and PL data are in reasonable agreement with predictions made by extrapolating from known binary and ternary data. AFM topography measurements have found the RMS surface roughness to be 2 nm. This is another measure of the good quality of the material. Understanding the details of the surface morphology is expected to be a useful tool in understanding the growth mechanisms and the amount of residual strain at the surface.

InAlAsSb p-n junctions have been formed using Te as the n-type dopant and Be as the p-type dopant. Lithographic and wet etch procedures are under development, and have been successfully applied to form mesa diodes for I-V tests. The best I-V characteristics with an ideality factor of 1.1 and low reverse-bias leakage current have been found for material grown near 400 °C.

Future work toward improving the quality of the InAlAsSb will involve investigating the dependence on the As and Sb fluxes and flux ratios. Preliminary work also indicates that there are better buffer layers than the AlSb when growing on GaSb substrates. InGaSb layers are being grown in an effort to improve the quality of the material needed for the HBT base. As soon as the InGaSb growth has been optimized, p-n heterojunctions will be formed, and an effort to determine the band offsets will begin. The modeling has demonstrated that this is an important parameter in device operation. The segregation and diffusion of dopants at the interfaces may also be a difficulty that needs to be addressed.

Acknowledgement

This work was supported by the Defense Advanced Research Projects Agency, and the Office of Naval Research.

The authors would like to thank Donald Sawdai, Cedric Monier, and Mike Wojtowicz for their useful discussions.

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AlGaAsSb-InGaAsSb-GaSb epitaxial heterostructures for uncooled infrared detectors

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Abstract

Lattice matched n-type AlGaAsSb-InGaAsSb-GaSb heterostructures for uncooled infrared detectors including separate absorption and multiplication avalanche photodiodes (SAM-APD) as well as low-voltage InGaAsSb APDs were grown using inexpensive liquid phase epitaxy. Formation of the pn-junction was performed through diffusion of Zn from the vapor phase. Responsivity at $\lambda = 2$ μm as high as 3.5 A/W was achieved in InGaAsSb APD biased at 8 V with the avalanche multiplication starting at 6 V. Our calculations have shown that the above parameters can result in a NEP value as low as $1x10^{-12}$ W or D* value as high as $2x10^{10}$ cm·Hz$^{1/2}$/W at room temperature for 400 μm diameter (200 μm diameter photoactive area) APD diodes.

Introduction

AlGaAsSb-InGaAsSb heterostructures lattice matched to GaSb are of great interest for use in high-performance photodetectors, LEDs and lasers in the mid-infrared wavelength region as well as for thermophotovoltaic devices. AstroPower has accumulated considerable experience in the development of inexpensive liquid phase epitaxy (LPE) for fabrication of AlGaAsSb-InGaAsSb photodetectors [1-3].

LPE inherently provides high material quality, both with respect to defect density and purity. This may be attributed to the preferential segregation of impurities to the liquid phase, the high mobility of atoms in the liquid phase (as compared to surface diffusion upon which vapor phase techniques depend), and near-equilibrium growth conditions.

In this work, we continued to study LPE growth of AlGaAsSb-InGaAsSb heterostructures. Additionally, a technically uncomplicated and productive method of Zn diffusion from the vapor phase was used to simplify and improve the fabrication technology of photodetectors including SAM-APDs and low-voltage APDs.

APDs are widely used for optical fiber communication. However, commercially available Si APDs require high voltage (several hundreds of Volts) that limits their application. In this work, low-voltage (6-8 Volts) APDs were developed. Moreover, in comparison with Si, the long wavelength sensitivity of the developed devices was extended to 2 μm.

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Experimental

Epitaxial growth

A standard horizontal slide boat technique is used for the LPE growth of the InGaAsSb and AlGaAsSb layers. The graphite slide boat is situated in a sealed quartz tube placed in a microprocessor-controlled, programmable, three-zone tube furnace. The growth ambient is palladium-diffused hydrogen at atmospheric pressure with a flow rate of 300 ml/min. The substrates with an area of 14x14 mm^2 are polished, (100) oriented, *n*-type GaSb wafers doped to 3-5 x 10^{17} cm^{-3} with tellurium.

The basic growth solution for InGaAsSb is indium (x_{In}=0.59), gallium (x_{Ga}=0.21) and antimony (x_{Sb}=0.20), where x_i is the atomic fraction of the element *i* in the solution. High purity (99.9999%) indium, gallium, and antimony metals are used and no intentional doping of the melt is applied. Prior to growth, the melt is baked out at 700 °C for 15 hours under flowing hydrogen to de-oxidize the metallic melt components and outgas residual impurities. After the baking and cooling, an undoped polycrystalline float InAs wafer is loaded on top of the melt, and the boat is heated again up to 530°C. Arsenic from the float InAs wafer is added to the melt through a partial dissolution of the wafer at this temperature. The melt is equilibrated for 1 hour at 530 °C and then cooled down to the growth temperature. At 515 °C, the substrate is contacted with the melt for 2 minutes to grow a 5 micron thick *n*-type $In_{0.15}Ga_{0.85}As_{0.17}Sb_{0.83}$ base layer with an electron concentration of 2-4x10^{16} cm^{-3}. Afterwards, the melt is wiped from the substrate. Electron probe microanalysis (EPMA) was used to determine the solid composition of the InGaAsSb layer. The electron concentration in InGaAsSb was calculated from CV-measurements performed after a pn-junction was formed in the InGaAsSb layer (see below). It is worth noting that not all samples were tested using CV-measurements. As no intentional and thus controllable doping of InGaAsSb was used in this work, the studied samples could have been doped in a range wider than 2-4x10^{16} cm^{-3}.

The growth of the AlGaAsSb layer is carried out from the growth solution having liquidus composition of gallium (x_{Ga}=0.959), antimony (x_{Sb}=0.013) and aluminium (x_{Al}=0.028). Arsenic is added to this melt from an undoped polycrystalline float GaAs wafer through the partial dissolution of the wafer at the growth temperature. The growth of AlGaAsSb is performed either in the same epitaxial run together with InGaAsSb, or in a separate epitaxial process using an InGaAsSb/GaSb wafer as a substrate. The reason to carry out separate processes is the following. We have found that in some experiments drops of the first melt (In-Ga-As-Sb) were left on the surface of the wafer after its wiping (especially at the edges). These drops when mixed with the second melt (Al-Ga-As-Sb), lead to the local formation of unpredictable melt compositions and hence irreproducible growth. A better reproducibility is achieved when the wafer is removed from the boat after the first layer growth, and the drops (if any) are eliminated. In the case of the separate epitaxies, the above-described procedure of the melt baking is repeated for a Ga-Sb part of the melt prior to growth. Al and GaAs floating wafer are added to the melt after the baking and cooling. The growth is performed at 509°C during a 90-sec long contact of the substrate with the melt resulting in a 2-μm thick $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ layer. AlGaAsSb layers grown without intentional doping are p-type. As we need an n-type layer, some Te-doped GaSb with a doping concentration of 2x10^{18} cm^{-3} was added and partly replaced Ga and Sb in the melt. Fig. 1 shows the carrier concentration in n-type $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ vs. the GaSb:Te amount in the Al-Ga-As-Sb melt. Adding of GaSb:Te into the melt provided an accurate control of the electron concentration down to the n=6-7x10^{16} cm^{-3}.

Diffusion of Zn

Pseudo-closed box diffusion of Zn from the vapour phase was performed into n-AlGaAsSb layers in a H_2 atmosphere purified by a Pd cell. A specially designed graphite boat close to that described in [4] was used. Separated pure Zn and Sb vapor sources were used in more than sufficient quantities to provide the saturation of vapour pressures. The design of the graphite boat ensures the uniformity of the Zn vapor pressure across the wafer surface, and thus the uniformity of the p-AlGaAsSb layer depth.

Fig. 2 shows two as-diffused Zn profiles in $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ obtained by means of a 4-hour diffusion of Zn at 460°C and 470°C. The profiles were measured by Secondary Ion Mass Spectroscopy (SIMS). The part of the profile near the surface has a very high concentration of Zn (about 10^{20} cm^{-3}). This 300 – 400 nm thick "dead" layer (shown hatched in Fig. 2) with a low diffusion length of electrons is removed by means of anodic oxidation and selective oxide etching.

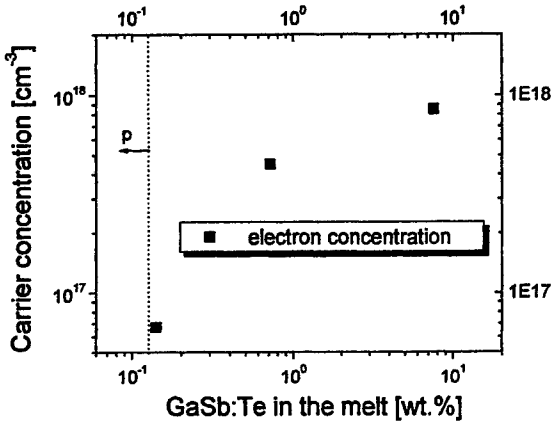


Fig. 1 Carrier concentration in n-$Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ layers vs. the amount of tellurium doped GaSb in Al-Ga-As-Sb melt.

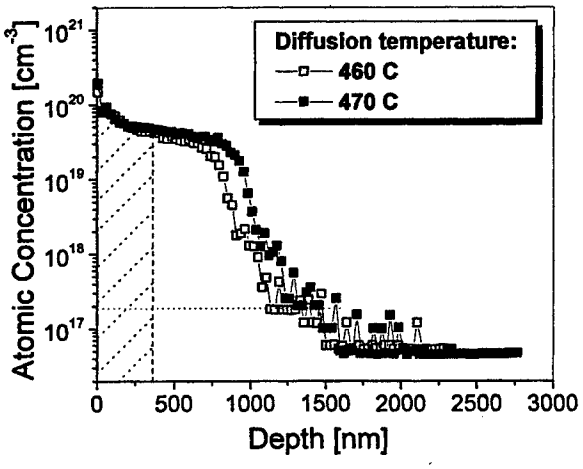


Fig. 2 Zn concentration profiles measured by SIMS in an $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ layer. The hatched part of the profile shows a dead layer that is removed later. The dotted line shows the electron concentration in the n-type $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ layer determined by CV-measurements.

If the AlGaAsSb layer is diffused all the way through, Zn diffusion in InGaAsSb must be considered. To evaluate Zn diffusion in InGaAsSb, data from [5] was used.

Device fabrication

Fig. 3 shows a photodiode mesa structure fabricated and studied in this work. It is composed of a 5-μm thick n-type $In_{0.15}Ga_{0.85}As_{0.17}Sb_{0.83}$ layer with $n=2\text{-}4x10^{16}$ cm^{-3} and a 2-μm thick $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ layer. The n-part of the AlGaAsSb layer is doped at the level of $n=2\text{-}4x10^{16}$ cm^{-3}. In the previous publications of AstroPower [2,3], both p- and n-type AlGaAsSb layers were grown epitaxially. In this work, the p-AlGaAsSb layer was formed by diffusion of Zn from the vapor phase. One can mention the following advantages of this approach:

- Technically, diffusion is simpler than epitaxy
- As only one AlGaAsSb layer is epitaxially grown, a difference in chemical composition between matrices of p- and n-layers is ruled out
- Diffusion of Zn is faster at the places of possible crystal defects in the n-AlGaAsSb layer. Thus, electrical isolation of these defects from the pn-junction takes place. Such isolation is not possible in the case of two epitaxial layers.

By fixing the thickness of the n-AlGaAsSb layer and changing position of pn-junction in it, different types of diodes were fabricated. If pn-junction is in AlGaAsSb and far from the AlGaAsSb-InGaAsSb interface, one gets a pn-AlGaAsSb photodiode. The low bandgap of InGaAsSb is not used in this case. Actually, such diodes were not the purpose of this work. If the pn-junction is in AlGaAsSb close to the AlGaAsSb-InGaAsSb interface, a SAM-APD diode is fabricated. And finally, if the whole AlGaAsSb is diffused all the way through, and pn-junction is formed in the InGaAsSb layer, a pn-InGaAsSb photodiode with an AlGaAsSb window is formed. As it was found in this work, some of these pn-InGaAsSb diodes exhibited avalanching characteristics.

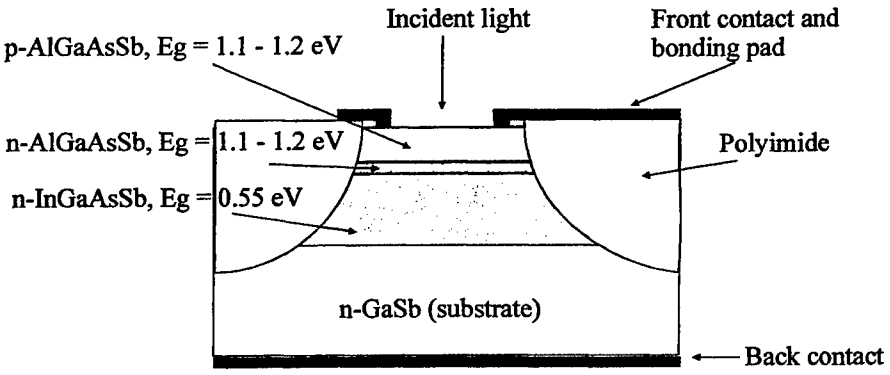


Fig.3 Scheme of the fabricated AlGaAsSb-InGaAsSb SAM-APD. In the case of a pn-InGaAsSb photodiode or APD, the n-AlGaAsSb layer was replaced by a p-InGaAsSb one, and the p-AlGaAsSb layer was used only for the InGaAsSb surface passivation.

Mesa photodiodes with 400-μm diameter total area and 200-μm diameter active area were formed using photolithography and chemical etching (Fig. 4). Metallization for the back n-type contacts was planar Au/Sn while front p-type contacts were annular Ti/Ni/Au A spin-on, photosensitive polyimide

layer was deposited and patterned before contact deposition. This had several functions including planarizing the surface for the front contact deposition, providing insulation of the junction, and passivating the edges of the device area. After photodiodes were formed, the substrate was diced into 1-mm^2 pieces with a single device in the middle of each square. These were mounted to TO-18 headers using silver conducting epoxy and wirebonded from the bonding part of the front contact to the header post. No antireflection coatings were applied.

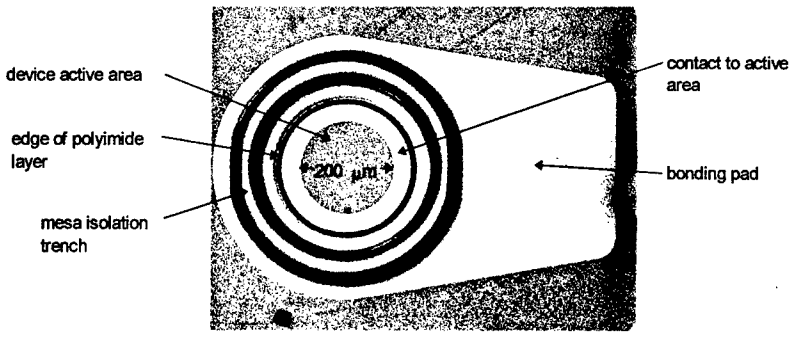


Fig. 4 Top-view of the fabricated photodiodes.

Results and Discussion

Figure 5 shows the comparison of dark I-V curves at room temperature of the best diodes with epitaxial and diffused pn-junctions in the $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ layer. One can see that formation of a diffused pn-junction provides a higher breakdown voltage and essentially lower dark current at the voltages close to the breakdown. This can be explained by the electrical isolation of possible crystal defects in the AlGaAsSb layer due to a higher diffusion rate of Zn in the vicinity of such defects.

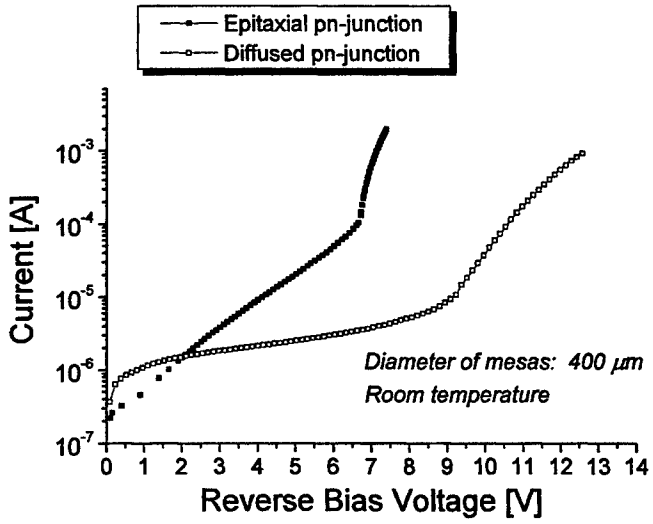


Fig. 5. Dark I-V curves of the best AlGaAsSb/InGaAsSb diodes with epitaxial and diffused pn-junctions in the $Al_{0.28}Ga_{0.72}As_{0.014}Sb_{0.986}$ layer.

Fig. 6 displays dark I-V curves of AlGaAsSb-InGaAsSb diodes with pn-junctions in either AlGaAsSb or InGaAsSb. Samples with pn-junctions in the InGaAsSb layer show quite different behaviors. Two mechanisms of the breakdown are observed: (i) Zener (pn-junction in InGaAsSb of type I), and (ii) avalanching (pn-junction in AlGaAsSb and in InGaAsSb of type II). If avalanching dominates, the breakdown voltage drops with decreasing temperature. Such a behavior was observed in the diode with pn-junction in AlGaAsSb (Fig. 6). The sample with avalanching breakdown of pn-junction in InGaAsSb, in which avalanche multiplication was also determined through responsivity measurements (see Fig.9), have not been measured at low temperature yet. However, one can expect the same positive temperature dependence of the breakdown voltage as it is observed in diodes with pn-junction in AlGaAsSb.

The large difference in IV-curves observed in two types of InGaAsSb samples can be explained by a difference in the n-InGaAsSb doping. As it was mentioned above, the range of doping in InGaAsSb might be wider than 2-4x10^{16} cm^{-3} if no intentional doping is used. Thus a relatively large difference in the width of the space charge region might determine the type of dominating breakdown mechanism: Zener or avalanching.

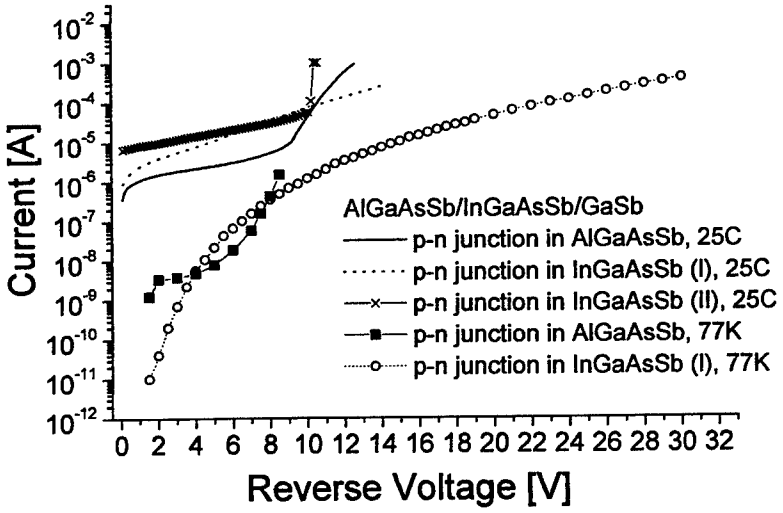


Fig. 6 I-V curves of the AlGaAsSb-InGaAsSb diodes with pn- junctions in different materials at 25°C and 77K. InGaAsSb (I) and InGaAsSb (II) correspond to devices with Zener or avalanching breakdown mechanisms, respectively.

Additional proof of avalanching is provided by spectral response measurements and calculation of quantum efficiency (QE). The only physical reason for the external QE to be higher than 100% is internal amplification caused by the avalanche carrier multiplication.

A computer-controlled spectrometer was used to measure spectral response of the fabricated devices (Fig. 7). The light source is a 1000 W tungsten halogen lamp. A calibrated detector with a calcium fluoride window is used as a reference for relative measurements. This detector has flat response in the wavelength range from 200 nm to over 10 μm. To determine the absolute spectral response, a JPL-calibrated AlGaAsSb-InGaAsSb photodiode with the same design as the tested diodes is used. Additionally, the spectral response of several photodiodes was measured at JPL at 77K.

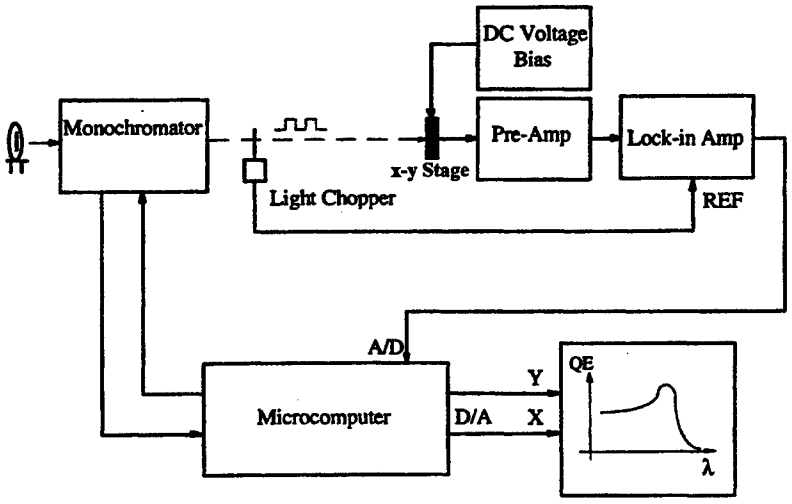


Fig. 7 Spectral response measurement set-up.

Fig.8 shows external QE of an InGaAsSb photodiode with Zener breakdown. Measurements were performed at different reverse biases at 25°C and 77K. A small improvement of the QE is observed after applying the reverse bias up to 3 V. However, there was no further improvement at higher voltages (up to 24V) showing that no avalanche multiplication happened in this diode. The maximum of QE at 77K is shifted to shorter wavelengths due to the increase of the bandgap in InGaAsSb. QE at 77K and at 0 V is lower than at 25°C. However, contrary to the measurements at 25°C, applying reverse voltages at 77K essentially increases QE, and already at 3 V the maximum QE at both temperatures are equal.

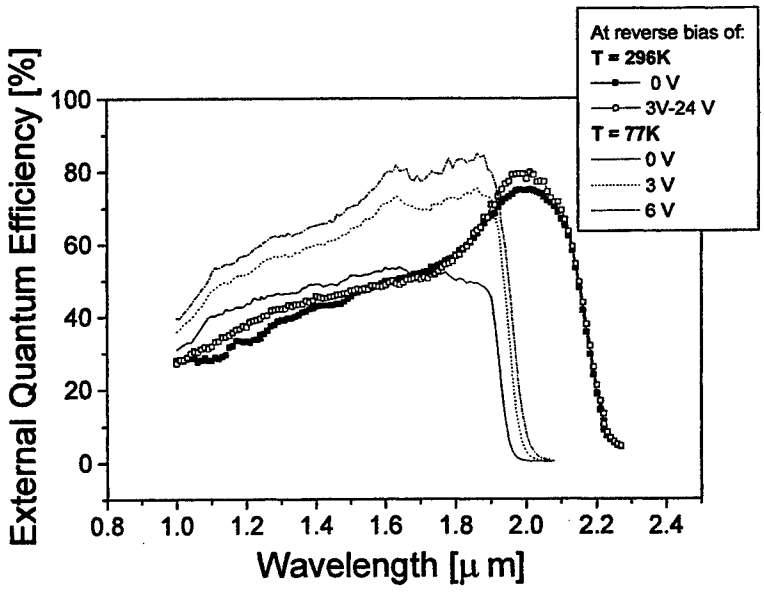


Fig. 8 External quantum efficiency of an InGaAsSb pn-photodiode with the Zener breakdown of pn-junction. Measurements are performed at different reverse biases at 25°C and 77K.

Fig. 9 shows the responsivity of an avalanching InGaAsSb pn-photodiode. Both the IV-curve of this diode with a sharp increase of current at the breakdown voltage (Fig.6), and responsivity vs. reverse voltage (Fig.9) clearly show that this diode is an APD. Improvement of carrier collection and separation due to expanding of the space charge region (SCR) with voltage cannot explain the growth of responsivity up to 3.5 A/W. This value corresponds to an external quantum efficiency of 215 % that is not achievable without the avalanche multiplication. It is noteworthy, that Fig. 9 shows three phases in the dependence of responsivity on reverse bias. The first one is between 0 V and 1 V, when a fast increase of responsivity from 1.2 A/W to 1.6 A/W is observed. The improved collection and separation due to enlarging SCR can explain this increase. The second phase between 1V and 5V is characterized by a saturation of the responsivity increase. Finally, the third phase between 6 V and 8 V shows the avalanche multiplication.

Thus, a low-voltage avalanching regime (starting from 6 V) is achieved in InGaAsSb APDs with an AlGaAsSb window layer. As these diodes demonstrate high responsivity at zero voltage (1.2 A/W), 3.5 A/W responsivity is achieved already at 8 V what we believe is the best result for the wavelength of 2 μm.

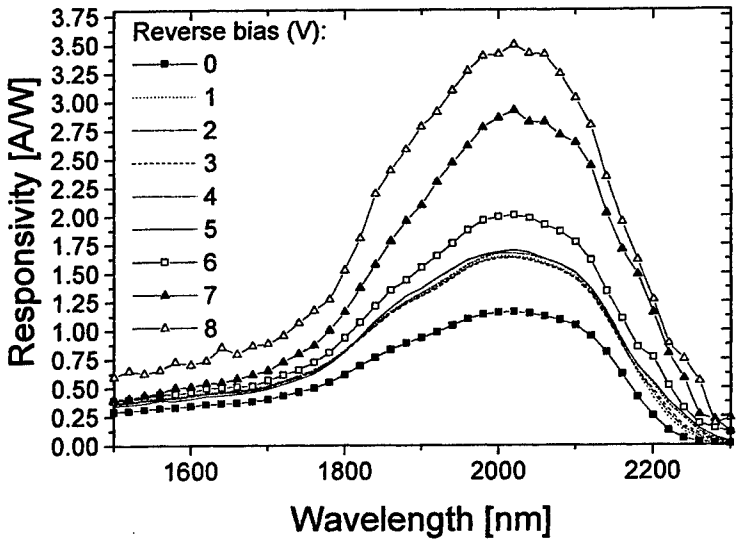


Fig. 9 Spectral response of the low-voltage InGaAsSb APD at different reverse bias voltages. Avalanche multiplication starts at 6 V.

Also, we performed calculations of NEP and D* based on the measured parameters.

The following formula can be derived for *NEP*:

$$NEP = \frac{2qRB + ((2qRB)^2 + 8R^2 qI_d B)^{0.5}}{2R^2},$$

where R is responsivity, I_d is dark current , B is bandwidth, and q is electron charge.

Then

$$D^* = \frac{\sqrt{A} \cdot \sqrt{B}}{NEP},$$

where A is active area of the diode.

Considering the following parameters for the low-voltage InGaAsSb APD at reverse bias of 8V: R = 3.5 A/W (Fig.9), I_d=3x10^{-5}A (Fig.6), A = 3x10^{-4} cm^2 (diameter of photoactive area of 200 μm), and B = 1 Hz, NEP can be calculated as 1x10^{-12} W and D^* value as 2x10^{10} cm·Hz$^{1/2}$/W.

Conclusions

Three different types of heteroface AlGaAsSb/InGaAsSb/GaSb photodiodes are fabricated and studied by using of inexpensive liquid phase epitaxy and diffusion of Zn from the vapor phase.

Both avalanching and Zener breakdown mechanisms are determined in InGaAsSb pn-junctions. This difference can be explained by doping variations of base n-InGaAsSb layers. Controllable rather than unintentional doping must be introduced to provide a more reproducible low doping level of InGaAsSb. Similar to AlGaAsSb doping, it can be done by using GaSb:Te added to the melt as a dopant source.

Low-voltage avalanching regime (starting from 6 V) is achieved in InGaAsSb APDs with an AlGaAsSb window layer. As these diodes demonstrate high responsivity at zero voltage (1.2 A/W), 3.5 A/W responsivity is achieved already at 8 V what we believe is the best result for the wavelength of 2 μm.

An NEP value as low as 1x10^{-12} W or D* value as high as 2x10^{10} cm·Hz$^{1/2}$/W at room temperature is calculated for low-voltage APD diodes with a diameter of photoactive area of 200 μm.

Acknowledgements

The authors wish to thank B. Ber from Ioffe Institute, St. Petersburg, Russia for SIMS measurements and P. Sims from AstroPower for useful discussions.

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Ultrafast Optical Manipulation of Ferromagnetic Order in InMnAs/GaSb

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Abstract. We have performed a two-color time-resolved magneto-optical Kerr effect (MOKE) study of a ferromagnetic InMnAs/GaSb heterostructure. We observed ultrafast photo-induced changes in the MOKE signal induced by a large density of spin-polarized transient carriers created only within the InMnAs layer using intense 140 fs mid-infrared pulses. Our data clearly demonstrates that magnetic properties, e.g., remanence and coercivity, can be strongly modified. The dependence of these changes on the time delay, pump polarization, pump intensity, and sample temperature is discussed.

1. INTRODUCTION

Recently, there has been much interest in ultrafast spin dynamics in ferromagnets, both from scientific and technological viewpoints [1]. Itinerant ferromagnets such as nickel, cobalt, iron, and $CoPt_3$ have been studied extensively using ultrafast optical and magneto-optical spectroscopies, exhibiting an array of new phenomena [2-10]. In particular, the discovery of *ultrafast demagnetization* [2] suggested a novel ultrafast scheme for writing data in magneto-optical recording applications. At the same time, exactly how a laser pulse can effectively change the magnetic spin moment in an ultrafast manner is an open question, motivating intensive experimental and theoretical investigations [8-11]. In extreme cases, intense laser pulses were shown to increase the electron temperature to even above the Curie temperature, driving a ferromagnetic to paramagnetic phase transition in the femtosecond time scale [7].

III-V ferromagnetic semiconductors such as InMnAs [12,13] and GaMnAs [14] can add new dimensions to this problem. The *carrier-induced* nature of ferromagnetism in these semiconductors, whose microscopic origin is a matter of controversy [15], has paved a natural path to electrical [16] and optical [17] control of magnetic order. Since ultrashort laser pulses can create a large density of *transient carriers* in semiconductors, in addition to heating the electron system as in the case of ferromagnetic metals, one can anticipate significant modifications in the exchange interaction between Mn ions. In addition, unlike metals, pumping semiconductors with circularly-polarized light results in spin-coherent carriers, which should not only lead to their own contribution to the net magnetization, but

0-7803-7478/02/$17.00 © 2002 IEEE

also be able to enhance or reduce the magnetization due to the Mn spins via *s–d* and *p–d* exchange interactions, depending on the relative orientations of the carrier spins and localized Mn spins.

Here we report results of an ultrafast optical study of spin/magnetization dynamics in a ferromagnetic InMnAs/GaSb heterostructure. We have developed a novel two-color time-resolved magneto-optical Kerr effect (MOKE) spectroscopy setup, which allows us to create transient carriers *only in the magnetic InMnAs layer* using mid-infrared (MIR) pulses and then probe the induced magnetization changes through the MOKE angle of near-infrared (NIR) probe pulses. Our data indeed shows that magnetic properties, e.g., coercivity and remanent magnetization, can be significantly modified by intense MIR pulses. We performed simultaneous measurements of MOKE angle and reflectivity for examining spin and charge dynamics separately. Furthermore, coherent optical spin injection using different senses of circular polarization led to different signs for the net MOKE changes induced by the pump. Finally, the temperature and pump intensity dependences of these effects will be shown and discussed.

2. EXPERIMENTAL DETAILS

We performed two-color time-resolved MOKE spectroscopy using femtosecond pulses of MIR and NIR radiation. The experimental setup is schematically shown in Figure 1. The source of intense MIR pulses was an optical parametric amplifier (OPA) (Model FS-TOPAS-4/800, Quantronix/Light Conversion) pumped by a Ti:Sapphire-based regenerative amplifier (Model CPA-2010, Clark-MXR, Inc., 7300 West Huron River Drive, Dexter, MI 48130). The OPA was able to produce tunable and intense radiation from 522 nm to 20 μm using different mixing crystals. The CPA produced pulses of NIR radiation with a wavelength of 775 nm, a pulse energy of ~ 1 mJ, and a pulse duration of ~ 140 fs at a tunable repetition rate of 50 Hz – 1 kHz. We used a very small fraction (~ 10^{-5}) of the CPA beam as a probe and the output beam from the OPA tuned to 2 μm as the pump. The CPA probe beam went through a computer-controlled variable delay stage in addition to a fixed ~ 2 m long delay stage that equalized the pump and probe beam path lengths to the sample by taking into account the total path length inside of the multi-pass OPA. The two beams were made collinear by a non-polarizing beam splitter (Lambda Research Optics, Inc.), which was 50% reflective to the NIR probe and 50% transmissive to the MIR pump, and then focused by an off-axis parabolic mirror with a six inch focal length onto the sample mounted inside a 10 Tesla superconducting magnet with ZnS cold windows and CaF_2 room temperature windows. The reflected NIR probe beam entered a Wollaston prism which spatially separated the *s*- and *p*-components of the probe beam, which we then focused on a balanced bridge system consisting of a Si detector pair. The signal from the balanced detectors, which was proportional to the induced MOKE angle change, was fed into a lock-in amplifier or a boxcar integrator and was recorded by a computer. An additional beam splitter was placed before the Wollaston prism for monitoring the reflectivity of the probe. With this setup, we were able to record the MOKE angle and reflectivity as functions of time delay and magnetic field.

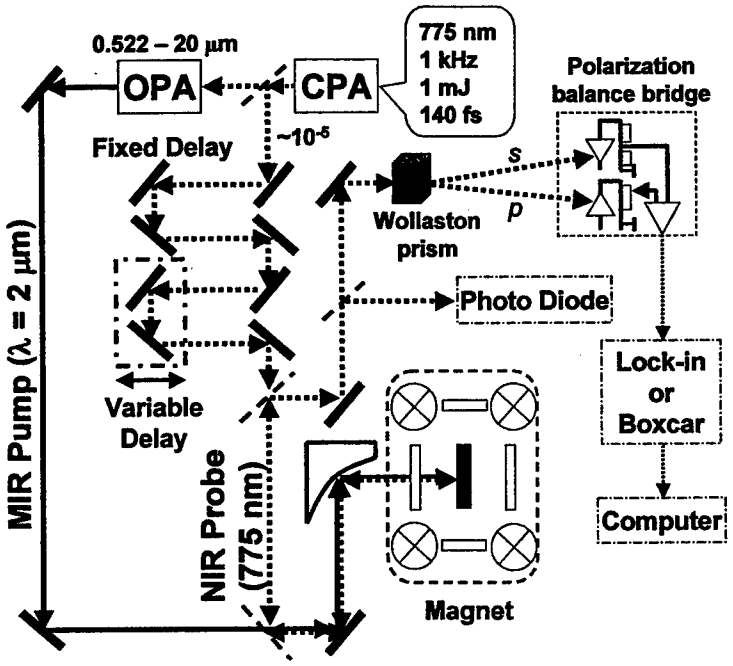


Fig. 1. Schematic diagram for the two-color time-resolved MOKE spectroscopy setup. OPA: optical parametric amplifier. CPA: chirped pulse amplifier. The CPA is a Ti:Sapphire-based regenerative amplifier (Model CPA-2010, Clark-MXR, Inc.). A small fraction (~ 10^{-5}) of the CPA beam is used as a probe and the OPA beam tuned to 2 μm is used as the pump.

At this pump wavelength (2 μm), the photon energy (0.62 eV) was smaller than the band gaps of the GaSb buffer (0.812 eV) and GaAs substrate (1.519 eV) but larger than that of InMnAs (~ 0.42 eV), so the pump created carriers only in the InMnAs layer. The beam diameter of the MIR pump at the sample position was measured by pinholes to be ~ 75 μm. The maximum MIR pulse energy used in this experiment was ~ 6.3 μJ, which corresponds to a fluence of ~ 0.45 J/cm^2. Using the optical constants of InAs and the thickness of the InMnAs layer, we estimated the maximum density of photocreated carriers to be ~ 7.5×10^{22} cm^{-3}, which is an extremely large number, especially if we think of the fact that the density of Mn ions is only ~ 10^{21} cm^{-3}.

The sample studied was an InMnAs/GaSb single heterostructure with a Curie temperature (T_c) of 55 K, consisting of a 25 nm thick $In_{0.91}Mn_{0.09}As$ magnetic layer and an 820 nm thick GaSb buffer layer grown on a semi-insulating GaAs (100) substrate. Its room temperature hole density and mobility were 1.1×10^{19} cm^{-3} and 323 cm^2/Vs, respectively, estimated from Hall measurements. The sample was grown by low temperature molecular beam epitaxy (growth conditions described previously [18]) and then annealed at 250 °C, which increased the T_c by ~ 10 K [19,20]. The magnetization easy axis was perpendicular to the epilayer due to the strain-induced structural anisotropy caused by the lattice mismatch between InMnAs and GaSb (InMnAs was under tensile strain). This allowed us to observe ferromagnetic hysteresis loops in the polar Kerr configuration.

3. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 2(a) shows three magnetic-field-scan data exhibiting ferromagnetic hysteresis loops at a temperature of 16 K, taken under different conditions. The curve labeled 'No Pump' was taken with the OPA pump beam blocked, while the other two curves were taken under high OPA excitation (fluence ~ 0.2 J/cm^2) with a time delay of 0 ps and –7 ps, respectively. It can be seen that at timing zero the loop *horizontally* collapsed, i.e., the coercivity is almost zero. Note that this curve is not intentionally offset; namely, this vertical shift is a real effect induced by the pump, which exists only for a short time (~ 2 ps). As discussed later, we attribute this transient vertical shift of the MOKE signal to the coherent spin polarization of the photo-generated carriers. The negative time delay data also shows similar horizontal shrinkage though it is not as dramatic as the timing zero data. It is important to note that the vertical height (i.e., remanence) of the loops is not much affected by the pump, which excludes simple lattice heating as the cause of the horizontal loop quenching. To support this view more convincingly, we show in Fig. 1(b) CW magnetic circular dichroism data taken for the same sample at 10 K, 35 K, 45 K and 55 K. As can been seen clearly, raising the lattice temperature results in dramatic loop shrinkage *both horizontally and vertically.* Furthermore, we took time-resolved MOKE data with various combinations of average powers and fluences (data not shown) and found that *it is the fluence that determines the degree of collapse, not the average power.* For example, data taken at a low repetition rate with a high fluence displayed significant quenching while data taken at a high repetition rate with a low fluence did not show any quenching.

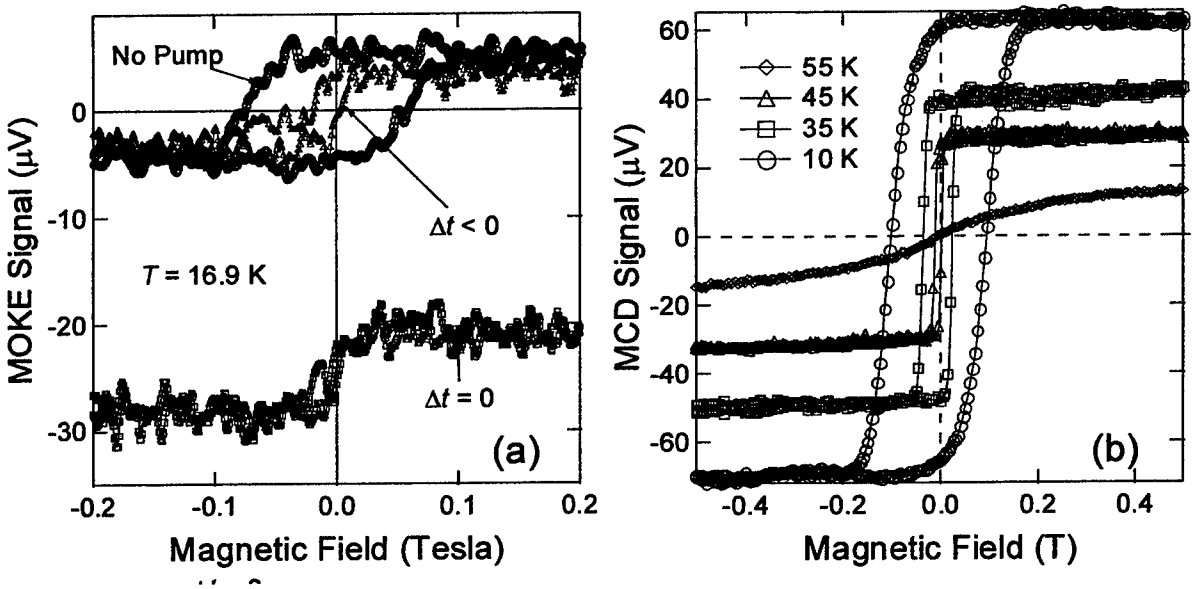


Fig. 2. (a) Black circles: MOKE signal versus magnetic field with no pump. Red squares: MOKE signal versus magnetic fields under MIR pump excitation (~ 0.2 J/cm^2) at timing zero. Blue triangles: MOKE signal versus magnetic field under MIR pump excitation (~ 0.2 J/cm^2) at a time delay of –7 ps. (b) CW magnetic circular dichroism data taken at four different temperatures (10 K, 35 K, 45 K, and 55 K).

Next we discuss some time-scan data. Figure 3(a) shows two traces representing the pump-induced MOKE signal change versus time delay taken under the excitation of the MIR pump with two opposite senses of circular polarization, i.e., σ^+ and σ^-. As clearly demonstrated here, opposite polarizations result in *opposite signs* of the photo-induced MOKE change, suggesting that these fast decaying transient MOKE signals are due to the photo-induced coherent carrier spin polarization. The pump-induced reflectivity change as a function of time is shown in Fig. 3(b). One can see a quick disappearance of the induced reflectivity change. In metals, photo-induced transmission or reflection changes can be attributed to electron temperature changes, which show characteristic cooling behavior as the electron system loses it energy to the lattice. In the present semiconductor system, however, the reflectivity change is most likely due to the transient change of the carrier density. The observed fast (< 2 ps) decay is consistent with the fast decays typically observed in low temperature grown semiconductors such as those used in terahertz emitters and receivers [21]. To further understand the origin of the polarization-dependent ultrafast MOKE change, we did the same measurements at elevated temperatures. As an example, data taken at 122 K is shown in Fig. 4. Here, again, we see opposite signs for σ^+ and σ^- polarization. We attempted to observe photo-induced ferromagnetism by scanning the magnetic field at these high temperatures but did not see any evidence. These facts lead us to believe that these signals are related to the coherent carrier spins. We do not have an explanation for the second peak around 1 ps observed for both polarizations. More detailed temperature dependent measurements are in progress to elucidate this feature.

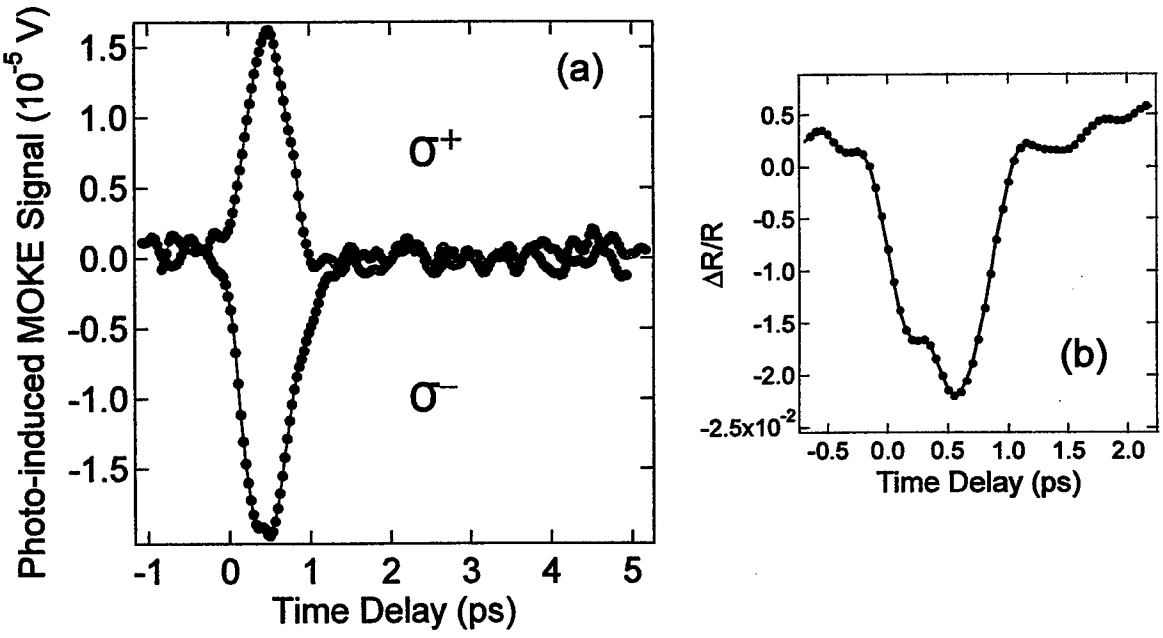


Fig. 3. (a) Photo-induced MOKE signal at a temperature of 16 K versus time delay under pumping with circularly polarized MIR radiation. (b) The reflectivity of the NIR probe is plotted as a function of time delay, showing fast carrier recombination.

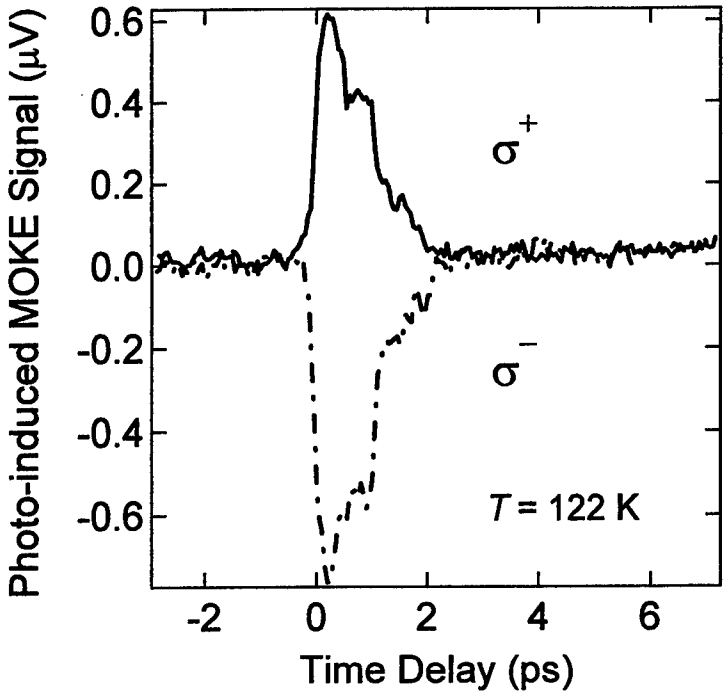


Fig. 4. Photo-induced MOKE signal versus time delay for an InMnAs/GaSb heterostructure with a Curie temperature of 55 K, taken at 122 K under pumping with circularly polarized MIR radiation.

4. SUMMARY

We have presented results of what we believe to be the first ultrafast optical study of spin/magnetization dynamics in ferromagnetic InMnAs/GaSb heterostructures. Using a novel two-color time-resolved magneto-optical Kerr effect spectroscopy technique, we created transient carriers only within the ferromagnetic InMnAs layer using intense mid-infrared pulses and observed the induced magnetization changes through the Kerr angle of near-infrared probe pulses. Our data shows that magnetic properties, particularly coercivity, can be drastically modified by the intense MIR pulses. We were able to study spin and charge dynamics separately by simultaneously measuring MOKE and reflectivity. Finally, coherent optical spin injection using different senses of circular polarization led to different signs for the net MOKE changes induced by the pump.

ACKNOWLEDGMENTS

This work was supported by DARPA through grant No. MDA972-00-1-0034 and the NSF through grant No. DMR-0134058 (CAREER). We are grateful to Bruce Brinson and Ben Schmid for their technical assistance.

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AlGaAsSb/InGaAs/AlGaAsSb Metamorphic HEMTs

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Abstract

Deep quantum well $In_{0.8}Ga_{0.2}As$/AlGaAsSb MHEMTs on GaAs are described. The step-graded AlGaAsSb strain-relief buffer layer provided a high-quality surface for growth of the MHEMT layers. AlGaAsSb barrier layers offer flexibility in choosing the channel composition and the barrier height. Typical Hall mobilities were 11,000 cm^2/V-sec at 300K for carrier concentrations of 2.4×10^{12} cm^{-2}. Extrinsic DC transconductance of 820 mS/mm was obtained for an MHEMT with a 0.15 μm x 64 μm gate. Typical extrinsic unity current gain cutoff, f_t, was 173 GHz with maximum frequency of oscillation, f_{max}, of 474 GHz. Aside from layer growth, the MHEMTs were fabricated using only small changes from conventional GaAs PHEMT processing. This technology promises affordable production costs for high performance millimeter-wave low noise amplifiers.

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I. Introduction

InGaAs has been established as the preferred channel material for high performance microwave and millimeterwave High Electron Mobility Transistors (HEMTs). Pseudomorphic InGaAs/AlGaAs HEMTs on GaAs substrates with up to 30% indium are widely used in the microwave and low millimeterwave range and 6" wafer fabrication technology is well established. Increasing the indium content in the ternary alloy produces higher low- field mobility and higher saturation velocity, leading to higher gain and lower noise figures in the HEMT [1]. On InP substrates, lattice matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs achieve excellent performance beyond 200 GHz. However, InP technology is not as mature as GaAs technology, and the cost of producing InP based HEMTs is higher. Metamorphic growth technology loosens the constraints of lattice-matched and pseudomorphic materials. With a strain-relief metamorphic layer, device quality $In_xGa_{(1-x)}As$ can be grown for the full range of $0 \leq x \leq 1$ on GaAs substrates, enabling high performance Metamorphic HEMTs (MHEMTs).

Quaternary AlGaAsSb buffers provide considerable flexibility in growing high performance MHEMT structures on GaAs. Gill, et al. [1], reported f_t of 150GHz for 0.1 μm gate, $In_{0.53}Ga_{0.47}As/In_{0.52}As_{0.48}As$ MHEMTs made atop graded AlGaAsSb buffers on GaAs, performance comparable to InP based lattice matched HEMTs. W-band MMIC MHEMT low noise amplifiers [2] and V-Band MHEMT monolithic power amplifiers [3] demonstrate the promise of this graded AlGaAsSb buffer technology. A similar MHEMT, reported by Behet, et al. [4], was made on a 2 μm thick $Al_{0.5}Ga_{0.5}As_{0.55}Sb_{0.45}$ layer on GaAs. This strain-relaxed buffer was lattice-matched to an $In_{0.53}Ga_{0.47}As/ In_{0.52}As_{0.48}As$ structure and the 0.25μm gate MHEMT had an f_t of 87GHz. Even more flexibility in choosing In concentration and band offsets can be obtained by using AlGaAsSb as the barrier material, forming an AlGaAsSb/InGaAs/AlGaAsSb MHEMT [5]. Miya, et al. [6,7] reported deep-quantum-well, InAs channel MHEMTs using quaternary barriers of several different

$In_{0.7}Ga_{0.3}As$	n = 1E18 cm^{-3}	125 A
AlGaAs Barrier	undoped	10 A
AlGaAsSb	undoped	120 A
Te-doping Spike	n_s = 5E12cm^{-2}	
AlGaAsSb	undoped	35 A
$In_{0.8}Ga_{0.2}As$	undoped	125 A
InAlAs Barrier	undoped	30 A
AlGaAsSb Buffer	undoped	1.5 um
	SI GaAs Substrate	

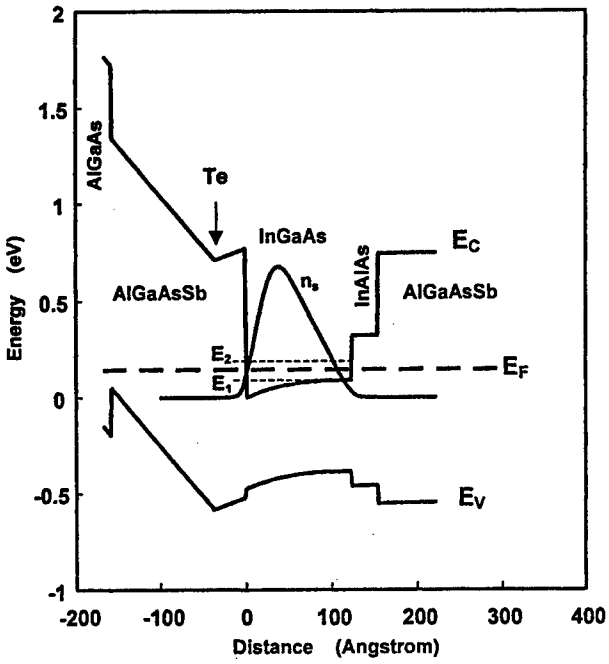


Figure 1. Layer structure and band diagram of AlGaAsSb/InGaAs MHEMT .

compositions all lattice matched to InAs. The 1.0 μm MHEMTs had f_t's of around 30 GHz, but the authors noted a strong kink effect, suggesting breakdown of the narrow band gap channel.

In this paper, we report an $In_{0.8}Ga_{0.2}As$/AlGaAsSb channel HEMT with a graded AlGaAsSb buffer on GaAs. The indium concentration of 80% provides excellent transport properties with a bandgap of 0.47 eV, providing channel breakdown voltage compared to InAs channels. In the following sections, we will present results of our initial effort to develop this material structure and the associated fabrication processes.

II. Metamorphic Growth and Characterization

The layer structure, grown by MBE on a semi-insulating GaAs substrate, is shown schematically in Fig. 1 along with a band diagram. The antimony concentration of the 1.5 μm AlGaAsSb quaternary buffer layer was step-graded to shift the lattice constant from that of the GaAs substrate to a value equivalent to $In_{0.7}Ga_{0.3}As$. This strain relief buffer layer confines dislocations to the AlGaAsSb and provides a suitable surface for growth of high quality channel material [1]. A 30 Å InAlAs spacer was grown on the buffer to reduce buffer leakage current. The high mobility channel layer is 125 Å pseudomorphic $In_{0.8}Ga_{0.2}As$. A 35Å AlGaAsSb spacer layer is followed by a 5×10^{12} cm^{-2} Te doping spike, and an additional 120 Å of undoped AlGaAsSb. A 10 Å undoped AlGaAs barrier was added to reduce gate leakage current. The final layer is a 125 Å InGaAs contact layer doped at 1×10^{18} cm^{-3}. The two dimensional electron gas (2DEG) is formed in the $In_{0.8}Ga_{0.2}As$ layer at the AlGaAsSb/InGaAs heterointerface. The wide band gap of the quaternary provides a large conduction band offset, close to 0.8 eV in this structure, leading to good confinement of the channel electrons. Typical measured Hall mobilities were 11,000 $cm^2/V\text{-}s$ at 300K for a 2DEG concentration of 2.4×10^{12} cm^{-2}. Topside processing and metalization was accomplished using the InP HEMT process as a starting point. Nonselective and

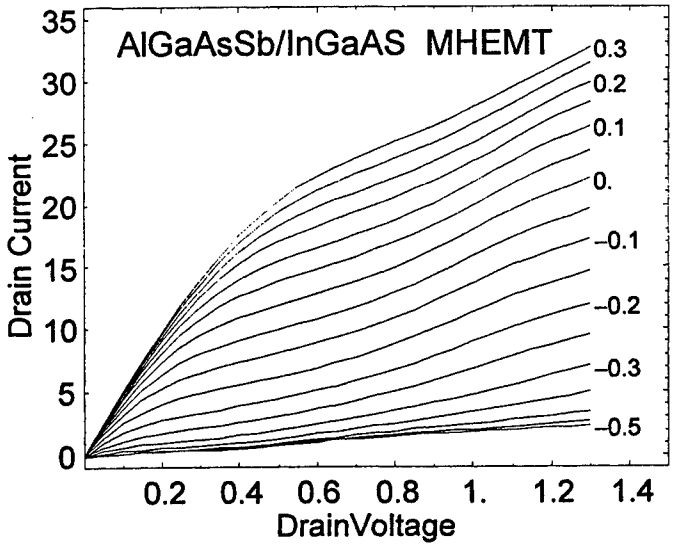


Figure 2: Typical I-V characteristic of a 0.15μm x 64 μm MHEMT

selective etch chemistries were developed to form mesas and gate recesses in the Sb-based layer structure. Flash annealed ohmic contacts produced contact resistivity in the range of 0.13 to 0.19 ohms-mm. T-gates were formed by direct write E-beam with nominal gate length of 0.15μm. Backside processing followed GaAs rules, including wafer thinning, dry etch vias, and backside metalization.

III. Device Measurements

Fig. 2 shows the typical measured current-voltage characteristics for a 0.15 μm x 64 μm AlGaAsSb/$In_{0.8}Ga_{0.2}As$ HEMT. The source-to-drain spacing of this HEMT is 2.0 μm, with source-to-gate spacing of 0.5 μm. The device pinches off at V_G=-0.5 V. The output conductance remains below 150 mS/mm for drain-to-gate voltages in the range of 0.65 V to 1.05 V. The maximum saturation current at V_D=1.3 V and V_G=0.0 V is 345.0 mA/mm. In Fig.3, the DC transconductance and drain current are plotted as a function of gate voltage for V_D=1.3 V. The transconductance peaks broadly around V_G=-0.2 with a value of 820 mS/mm. The gate current plot shown in Fig. 4 reveals the characteristic hump associated with impact ionization similar to the one observed in InP-based HEMTs [8]. The hump

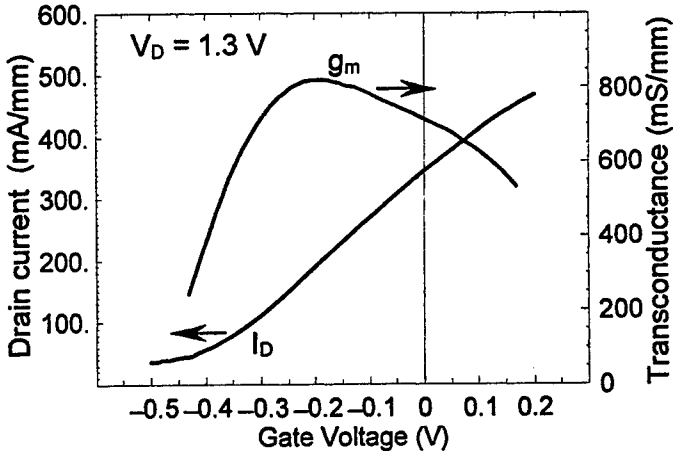


Figure 3: Typical transconductance and drain current of a 0.15μm x 64 μm MHEMT

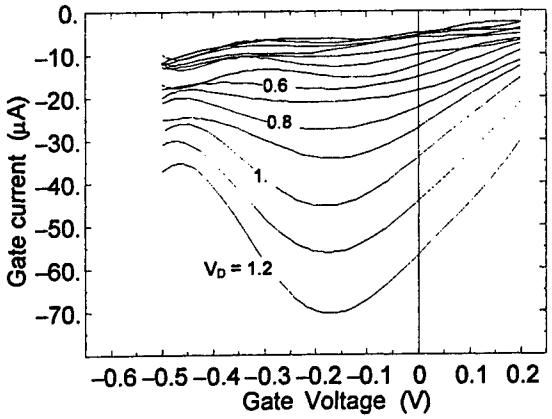


Figure 4: Typical gate current of a 0.15μm x 64 μm MHEMT

becomes particularly prominent at higher drain-to-source voltages. For low noise applications, the MHEMT would be biased at lower voltages, avoiding this region of higher impact ionization. The leakage current is relatively high for this size device. Leakage tends to be higher for buffers with higher Sb concentrations. This dependence needs further investigation. Higher aluminum concentration in the barriers would produce a higher hole barrier between the channel and the gate, but may risk instability of the layer due to oxidation.

RF performance of the fabricated devices was characterized by S-parameter measurements up to 60 GHz. The layout, shown in Fig. 5, embedded the transistor in

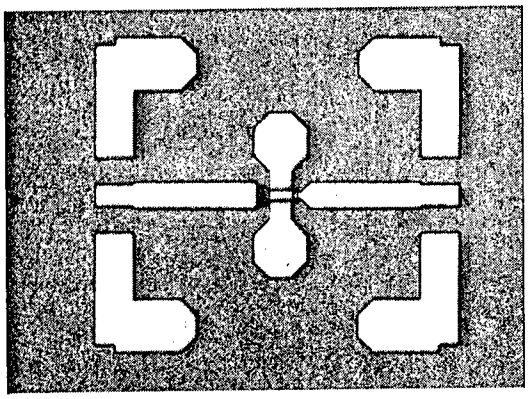


Figure 5: Layout of a 0.15μm x 64 μm MHEMT

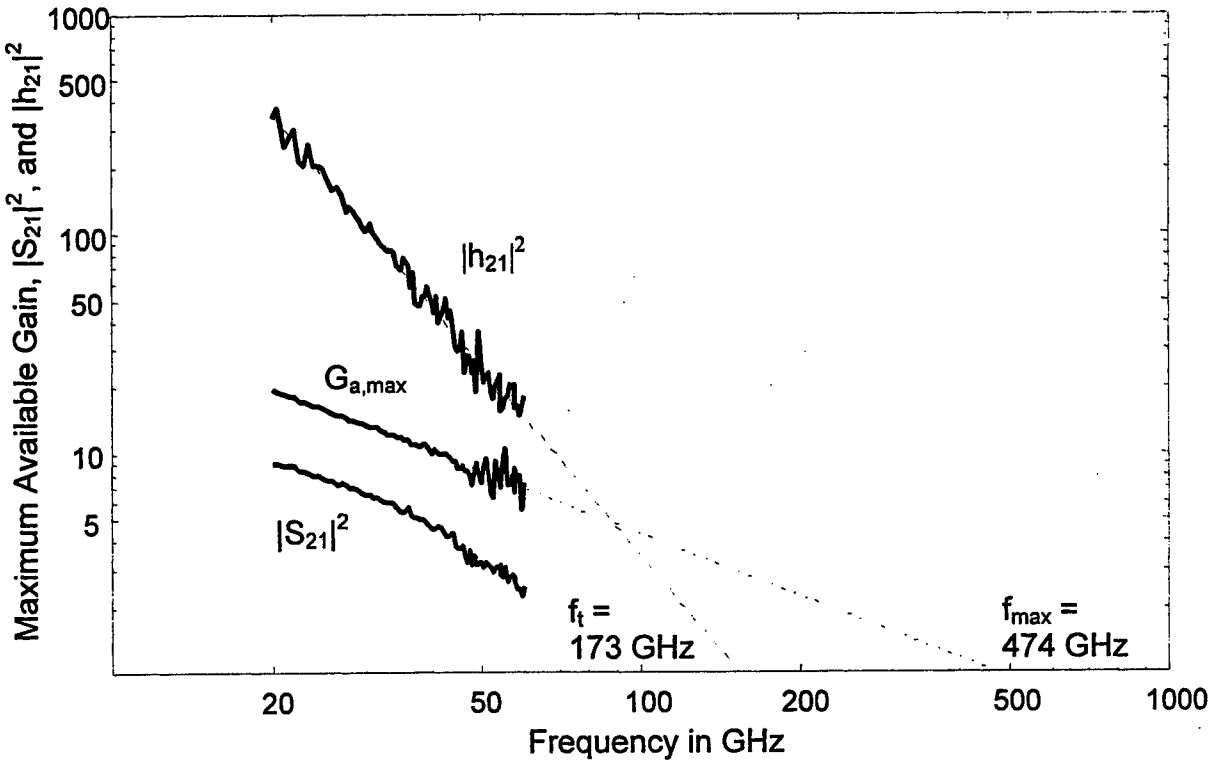


Figure 6. Maximum available gain, $|S_{21}|^2$, and $|h_{21}|^2$ of an AlGaAsSb/InGaAs HEMT as a function of frequency. V_D=0.5V, I_D=10.0mA, and V_G=-0.2V.

microstrip lines and included two source vias and microstrip-to-coplanar transitions for wafer probing. On-wafer calibration standards were used to de-embed the measurements to the transistor gate and drain terminals. The maximum stable gain, $|S_{21}|^2$, and $|h_{21}|^2$ are plotted in Fig. 6 as a function of frequency with V_D=0.5V, I_D=10mA and V_G=-0.2V. Extrapolating to unity gain intercepts indicate that the maximum frequency of oscillation, f_{max} = 474 GHz and the unity gain current cut-off frequency, f_t = 173 GHz.

IV. Conclusion

The AlGaAsSb/InGaAs/AlGaAsSb MHEMT on GaAs is a strong candidate for millimeter-wave low noise applications. The step-graded AlGaAsSb buffer layer on GaAs takes advantage of established wafer fabrication technology. Using AlGaAsSb as the MHEMT barrier allows flexibility in engineering the channel transport properties and the quantum well profile. The DC and RF results obtained from these devices indicate the high performance that can be obtained from this system with further optimization.

Acknowledgement

This work was supported in part by the Air Force Office of Scientific Research and by AFRL Contract F19628-95-C-0077.

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INTERSUBBAND TRANSITIONS IN NARROW InAs/AlSb QUANTUM WELLS

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Abstract

We have investigated intersubband transitions (ISBTs) in InAs/AlSb multiple quantum wells. In wells from 7 to 10 nm wide, the ISBT energy increases with decreasing well width and temperature. We do not observe photoluminescence (PL) from these wells. In wells from 2.4 to 6 nm wide, we observe PL but not ISBTs. We have calculated the band structure of these samples using an 8 band ***k.p*** theory including strain and many-body effects. We have modelled the dependence of the ISBT energy on well width and temperature. In addition, we have observed the effects on ISBTs of QW interface type and Si doping in the well.

1. Introduction

Intraband devices for infrared generation such as difference frequency convertors [1], quantum cascade lasers [2], and optically pumped lasers [3] have reached great levels of sophistication in AlGaAs systems. But the family of III-V semiconductors with lattice constants around 6.1 Å (InAs, GaSb, and AlSb) offers superior flexibility for intraband wavefunction engineering due to the large conduction band offset between InAs and AlSb (2.1 eV). In particular, the 6.1 Å heterostructures are more promising for building all-optical

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intraband devices with a short-wavelength pump [4].

We have investigated intersubband transitions in undoped InAs/AlSb multiple quantum wells (MQWs) of 20 periods with well widths from 2.4 to 10 nm. The wells' room temperature electron densities and mobilities were ~10^{12} cm^{-2} and 10^3-10^4 cm^2/Vs, respectively, and the lowest conduction subband was populated. The absorption was measured in a multipass geometry using a Fourier transform infrared spectrometer (FTIR). The absorption energy increased with decreasing well width and decreasing temperature, and the absorption linewidth showed a weak dependence on temperature. We computed the band structure of the quantum wells using an 8 band ***k.p*** theory. We took into account the temperature dependence of the strain effects due to the different thermal expansions of the well and barrier materials and of the bulk bandgaps, as well as many-body effects. We also investigated the dependence of the ISBT on the heterointerface type and Si doping in the well. We find that ISBTs and photoluminescence (PL) are mutually exclusive.

2. Experimental Procedures

The samples were grown by solid-source molecular beam epitaxy (MBE). The GaAs substrates were thermally cleaned before growth at 630 °C for 30 min in an As_4 atmosphere. Buffer layers consisting of 10 nm AlAs, 1000 nm AlSb and 15 periods of GaSb (6 nm)/AlSb (6 nm) SLs were grown at 550 °C. These buffer layers are used to change from the lattice constant of GaAs (0.56 nm) to that of GaSb (0.60 nm). After the growth of buffer layers, InAs (2.1 to 10 nm)/AlSb (10 nm) MQWs were grown at 420°C. Finally, GaSb was grown as a cap layer.

The InAs/AlSb MQW interface types can be controlled by the growth sequence and are expected to affect the band structure [5]. Both the group III (In, Al) and group V (As, Sb) atoms change across the InAs/AlSb interface. Two types of interface are possible: InSb-like and AlAs-like. Yano et al. have reported that the low temperature PL intensities of InAs/AlSb QWs with InSb-type interfaces were much stronger than those with AlAs-type [6]. From these results, two types of interfaces were grown for this study: (1) InSb-like on both sides of the QW, and (2) AlAs-like from InAs to AlSb and InSb-like from AlSb to InAs.

The shutter sequence for the growth of an InSb-like interface is as follows. First Al and Sb are grown, then the Al is turned off while the Sb is left on for five seconds. The Sb is turned off and after a wait of 1.4 seconds, the In is turned on. After growing one monolayer of InSb, the As is turned on.

The MQW growth was monitored by reflection high energy electron diffraction

(RHEED). The RHEED patterns along [1$\bar{1}$0] obtained during the formation of the InSb bonds were (1×3) druing the growth of AlSb and InSb, and (2×4) during the growth of InAs. These results indicate that the interface of InAs/AlSb can be controlled by the shutter sequence described above.

The sample structures we have studied are as follows: with both interfaces InSb-like, not intentionally doped, on GaAs substrates: well widths of 2.4, 2.7, 3.0, 3.3, 3.6, 4, 6, 7, 8, 9, and 10 nm; with one interface InSb-like and one AlAs-like, both undoped and Si well-doped, on GaAs substrates: well widths of 3.3 and 10.5 nm; and with both interfaces InSb-like, not doped, on GaSb substrates well widths of 3.3 and 10.5 nm.

The ISBTs were measured in a parallelogram multibounce geometry (see inset to Fig. 1) using an FTIR. The edges of the sample were polished at 45 degrees. This geometry couples the incident beam to the ISBTs, which can be excited only by an electric field perpendicular to the layers [9]. The QW surface of each sample was coated with 100 nm of gold to enhance the electric field perpendicular to the layers at the QWs [7, 8]. The samples were 2.3 mm long, corresponding to 2.3 bounces. We performed polarization modulation spectroscopy using a holographic grating polarizer to select the ISBT active or inactive polarization, *p* or *s*.

3. Results

3.1 Interband absorption

Figure 1 shows the *s* polarized interband absorption spectra of samples with well widths from 8 to 10 nm. These samples have both interfaces InSb-like, are undoped, and are grown on GaAs substrates. The interband spectra are the ratio of the sample transmission at one polarization to the transmission of a reference sample, grown without quantum wells, at that polarization. The figure shows -log($Transmission_{sample}/Transmission_{reference}$), i.e. absorbance, versus energy in eV.

The interband absorption edge shifts to higher energy as the well width decreases, mainly due to the increase in energy of the lowest quantized state in the well. Prevot et al. [10] have observed similar spectra in 6.5 to 8.5 nm InAs/AlSb wells. They also observe a difference between the shapes of the *s* and *p* polarized interband absorptions below the interband peak which is not present in our data.

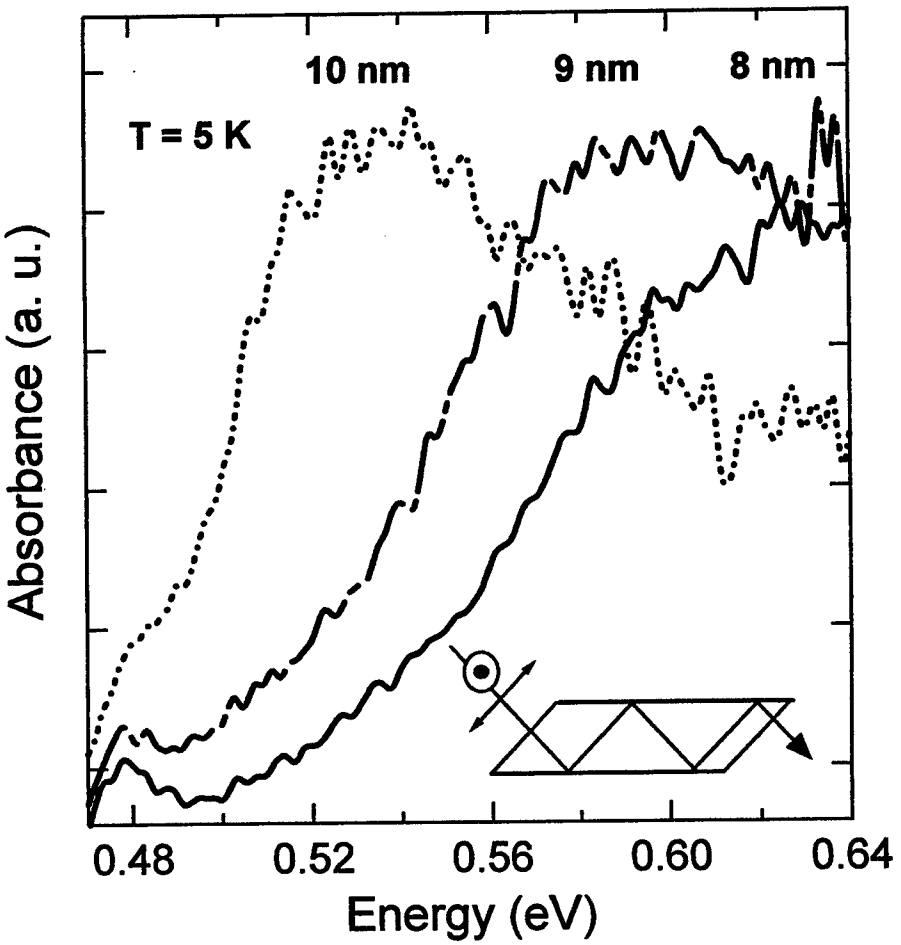


Figure 1. The *s* polarized interband spectra at 5 K are shown, normalized to a sample without quantum wells. The well widths in nm are indicated in the figure. The interband absorption edge shifts to higher energy with decreasing well width. The *p* polarized interband spectraare similar. The inset shows the sample measurement geometry and the two possible polarizations of the incident light.

3.2 Intraband absorption

We observed ISBTs in 10, 9, 8, and 7 nm wells. Figure 2 shows the temperature dependence of the ISBTs for different well widths. These samples have both interfaces InSb-like, are undoped, and are grown on GaAs substrates. The ratios of the *p*-polarized to the *s*-polarized spectra for each sample are plotted in absorbance versus energy. The traces are vertically offset for clarity. The traces are normalized to the same sample width so that different samples are directly comparable. For example, the ISBT for the 7 nm well is significantly weaker than the others.

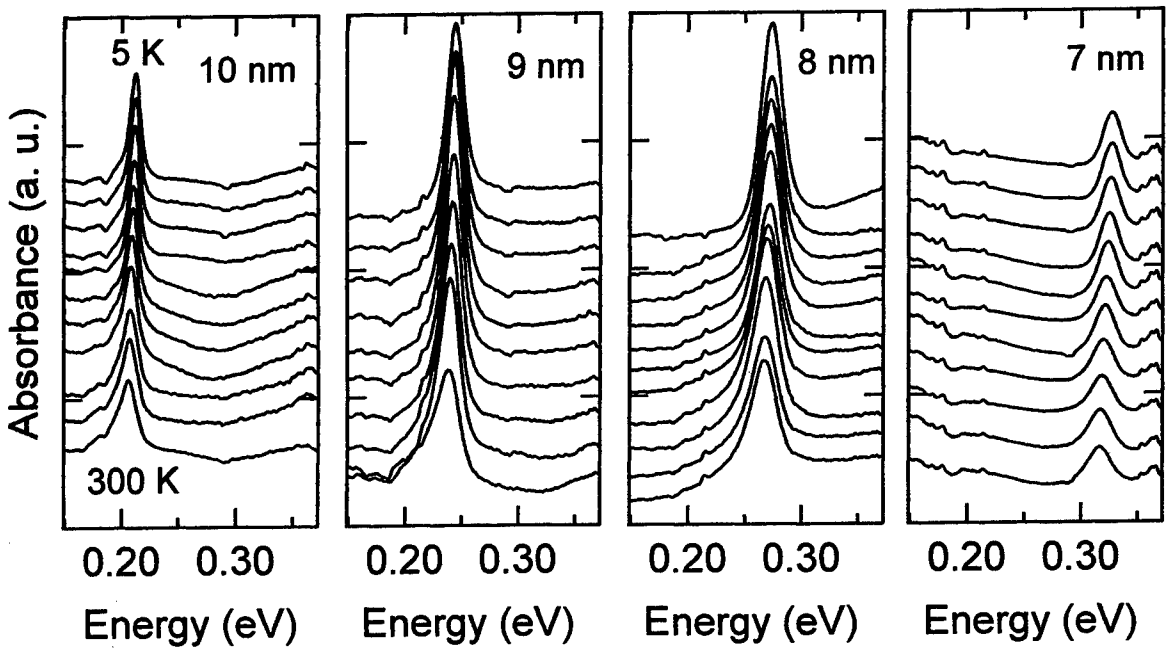


Figure 2. The intersubband absorptions of 10 through 7 nm wells as a function of temperature are shown. The *p* polarized spectrum is divided by the *s* polarized, and the traces are vertically offset for clarity. All traces are normalized to the same sample width so different samples are directly comparable. The resonance positions increase with decreasing well width and temperature, the linwidths narrow slightly with decreasing temperature, and the resonance intensity for the 7 nm sample is significantly smaller than the others.

The energy of each ISBT increases with decreasing well width and increases with decreasing temperature by about 8 meV from room temperature to 5 K. The full width at half maximum (FWHM) decreases by a factor of about 0.7 from 300 K to 5 K. Specifically, the room temperature FWHM for the 10, 9, 8, and 7 nm samples is 167, 221, 224, and 188 cm^{-1} (21, 27, 28, and 23 meV), and the FWHM at 5 K is 92, 144, 178, and 150 cm^{-1} (11, 18, 22, and 19 meV). The temperature-insensitive linewidth and relatively high mobility (10^3-10^4 cm^2/Vs) indicate that interface roughness scattering is the major broadening mechanism for intraband absorption [8, 11]. The FWHM increases with decreasing well width because interface fluctuations make up a larger fraction of the well width for narrorwer wells, and so interface roughness scattering is stronger.

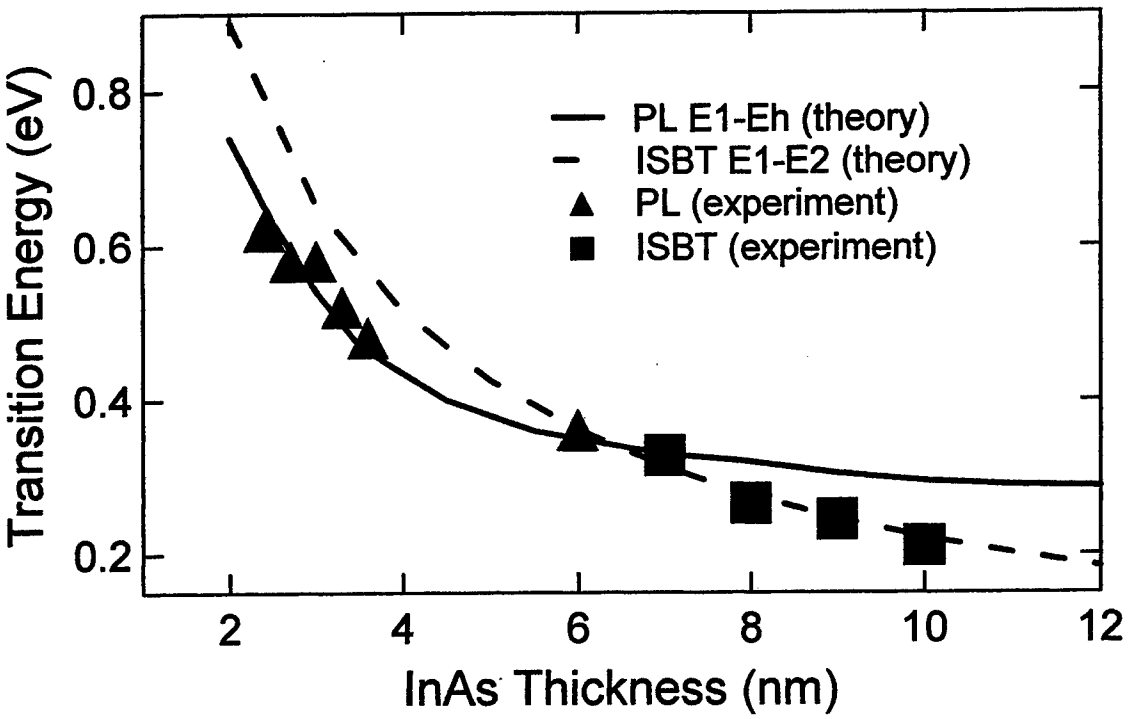


Figure 3. Transition energies as a function of quantum well thickness are shown. The ISBT energy E_1-E_2 is predicted from a flat-band calculation, and the PL is fitted with E_1-E_h from the Kronig-Penny model.

3.3 Photoluminescence

We observed PL in 2 to 6 nm wells, as shown in Figure 3. We could not observe PL in any of the samples which showed ISBTs; neither could we observe ISBTs in the samples which showed PL. It appears that whichever of these two transitions is lower in energy completely supresses the other. We are currently investigating this situation theoretically. The InAs/AlSb system offers the possibility of growing a sample in which the ISBT and PL are expected to occur *at the same energy*, accessing an unusual and intriguing crossover.

3.4 Interface and doping

We have made preliminary investigations of the dependence of the ISBT on interface type and Si doping. The samples shown in Figure 4 are (solid black) 10 nm wells, both interfaces InSb-like, no doping, (dotted black) 10.5 nm wells, one interface InSb-like, one interface AlAs-like, no doping, and (grey) 10.5 nm wells, one interface InSb-like, one

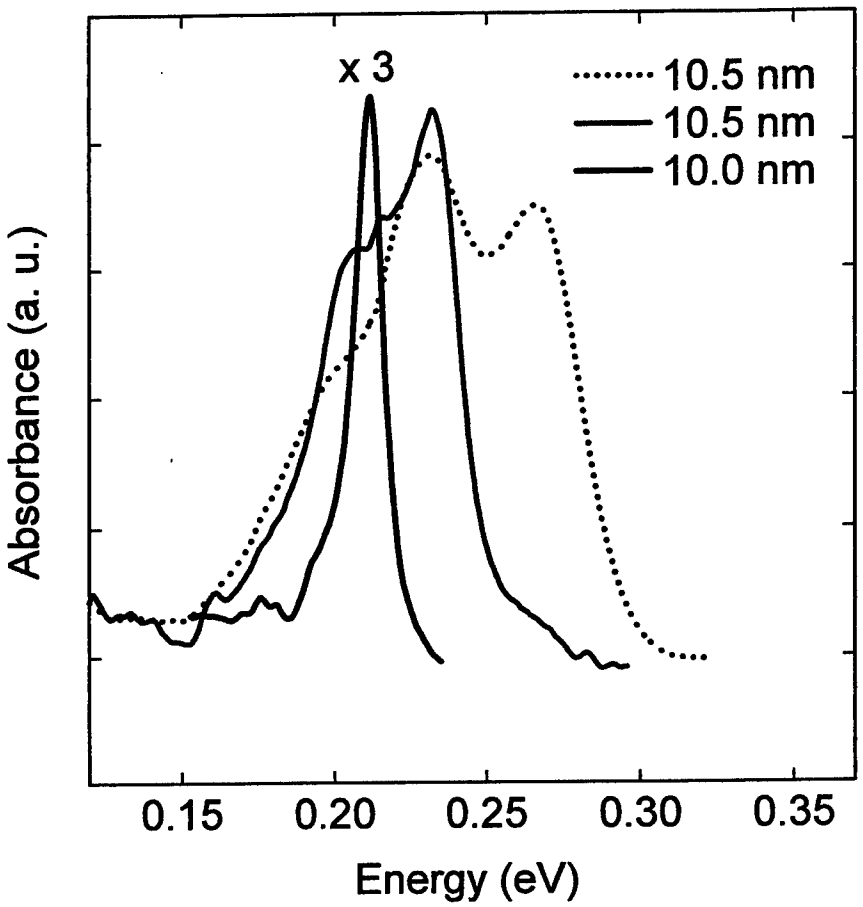


Figure 4. The intersubband absorptions of wells with different interfaces and dopoing are shown at 5 K. The *p* polarized spectrum is divided by the *s* polarized, and the black trace is scaled by a factor of 3 to compare ISBT widths between samples. All traces are normalized to the same sample width. The solid black sample has both interfaces InSb-like and no doping, the dotted black sample has one interface InSb-like and one AlAs-like and no doping, and the grey sample has one interface InSb-like and one AlAs-like and Si doping in the well. The sharp feature at 0.215 eV in the grey trace is an artifact of atmospheric absorption.

interface AlAs-like, Si well doping. The spectra shown are the *p* polarization divided by the the *s* polarization at 5 K. The black trace is scaled by a factor of 3 in order to compare the widths of the resonances more easily. The effect of changing one of the two InSb-like interfaces to AlAs-like is to change the shape to double-peaked and to increase the width and strength of the resonance. The low-energy shoulder in the undoped trace (dotted black) is more pronounced at lower temperatures. The effect of doping is to sharpen the resonance.

Theoretical work is in progress to elucidate our results in these situations.

3.5 Other parameters

We have investigated the dependence of the ISBT on substrate type (GaAs or GaSb). GaSb is attractivebecause it is lattice matched to InAs and AlSb and therefore does not require the growth of a buffer layer. We are also studying couple double quantum wells. All of these results will be published in a separate paper.

4. Calculations

The bandstructure of the QW structure is computed using an 8 band ***k.p*** theory in the envelope function approximation. Strain effects are included according to the Bir-Pikus description [12]. The Poisson and Schrödinger equations are solved self-consistently. The temperature dependence of the lattice constant is taken into account empirically according to a linear expansion expression. The temperature depencence of the band gap is included via the Varshni formaula [13]:

$$E_g(T) = E_g(0) - \alpha T^2/(T + \beta)$$

The model successfully describes the well width dependence of the ISBT energy. Due to the high density of free carriers in the quantum well, however, many-body effects on the absorption need to be included. Preliminary theoretical results corroborate standard understanding of the ISBT. For example, in Fig. 4 the solid curve shows the transition energy versus the quantum well thickness from a flat-band calculation. In addition, the depolarization shift causes blue shift, the exchange correlation induces red shift, and the vertex correction leads to lineshape narrowing.

The temperature dependence of the ISBT energy is affected by competing effects. As the temperature increases, the band gap decreases, which causes a blue shift, but this shift is compensated to certain degree by the increasing density and linewidth. Full modeling capability of type II QW structures and their optical properties with many-body interactions within the density matrix formalism is under development.

5. Conclusions

We have investigated intersubband transitions in narrow InAs/AlSb QWs. The transition energies increase with decreasing well width and decreasing temperature, and the linewidths decrease slightly with decreasing temperature. We have developed an 8-band ***k.p*** model

including strain and many-body effects which successfully describes these well width and temperature dependences. We have observed interband absorption, and its energy increases with decreasing well width. We have observed that photoluminescence and intersubband transitions are mutually exclusive in these QWs.

6. Acknowledgements

This work was supported by the Defense Advanced Research Projects Agency through grant No. F49620-01-1-0543, the NASA-NCI BSRP, and the Robert A. Welch Foundation.

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Performance and Modeling of Antimonide-Based Heterostructure Backward Diodes for Millimeter-Wave Detection

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Abstract

Heterostructure backward diodes have been fabricated and characterized for use as zero-bias millimeter-wave detectors. Sensitive detector performance in W-band was achieved by scaling the active area to 1.5x1.5 μm^2 through the use of high-resolution I-line stepper lithography. Responsivities of 2450 V/W and 2341 V/W were measured on-wafer at 95 GHz and 110 GHz, respectively. The detectors exhibit good detection linearity, with 0.8 dB compression measured at an RF power of 4 μW at 95 GHz. A nonlinear device model based on bias-dependent millimeter-wave s-parameter measurements has been developed. The model is consistent with the measured frequency response, responsivity, and detector compression characteristics. Extrapolation using the model to reduced device dimensions suggests that this device technology should provide appreciable responsivities (> 1000 V/W) at frequencies through G-band and beyond.

I. Introduction

Sensitive detectors at W-band and beyond have many potential uses, including applications in passive imaging arrays and radiometry. Of particular interest for arrays are zero-bias detectors since they obviate the need for bias control circuitry, simplifying the implementation of large arrays. Ge backward diodes [1] and planar-doped barrier diodes [2] can be used as zero-bias detectors at millimeter-wave frequencies, but have proven difficult to fabricate reproducibly in quantities sufficient for imaging array applications.

We report the millimeter-wave detection performance of InAs/AlSb/GaSb heterostructure backward diodes fabricated using high-resolution I-line stepper lithography for accurate definition of the small active areas needed for high sensitivity at W-band. The devices exhibit a strongly

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nonlinear current-voltage characteristic at zero applied bias, and have small associated capacitances as a consequence of the small device area facilitated by fine-line lithography. Measured device performance from dc-110 GHz and the development of a nonlinear device model that matches closely the experimental results are reported.

II. Device Design and Operation

The heterostructure used consists of an n-type InAs cathode (doped $7x10^{17}$ cm^{-3}), a 40 Å-thick AlSb barrier layer, and 200 Å of undoped $Al_{0.1}Ga_{0.9}Sb$, followed by a 500 Å p^+ GaSb anode (doped $4x10^{18}$ cm^{-3}) and an n^+ InAs anode contact layer. The staggered band alignment of GaSb to InAs facilitates this approach to low-resistance contacts to the anode side of the diode without the need for ohmic contact directly to the p-type GaSb.

The energy band diagram for this structure as calculated from a self-consistent Poisson/ Schrodinger solver [3] is shown in Figure 1. The doping level in the cathode contact layer was chosen in conjunction with the Al mole fraction in the AlGaSb barrier layer to place the Fermi level above the conduction band edge in the cathode and below the valence band edge in the AlGaSb simultaneously, as shown in Figure 1. As suggested by the band diagram in Figure 1, the staggered band alignment between AlGaSb and InAs facilitates a large reverse current due to interband tunneling. The forward current, on the other hand, is blocked by the bandgap of the AlGaSb layer. The resulting current-voltage characteristic exhibits strongly nonlinear behavior near zero bias, as desired for unbiased direct detection.

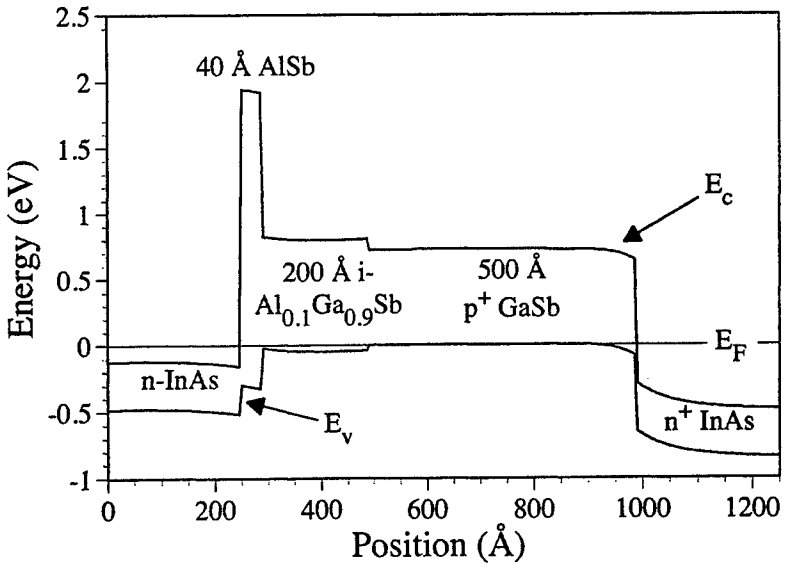


Figure 1. Calculated band diagram for Sb-based heterostructure backward diode detector.

Figure 2 shows the measured current-voltage characteristic of a typical 1.5x1.5 μm^2 area device. As can be seen, the IV curve is strongly nonlinear around zero applied voltage.

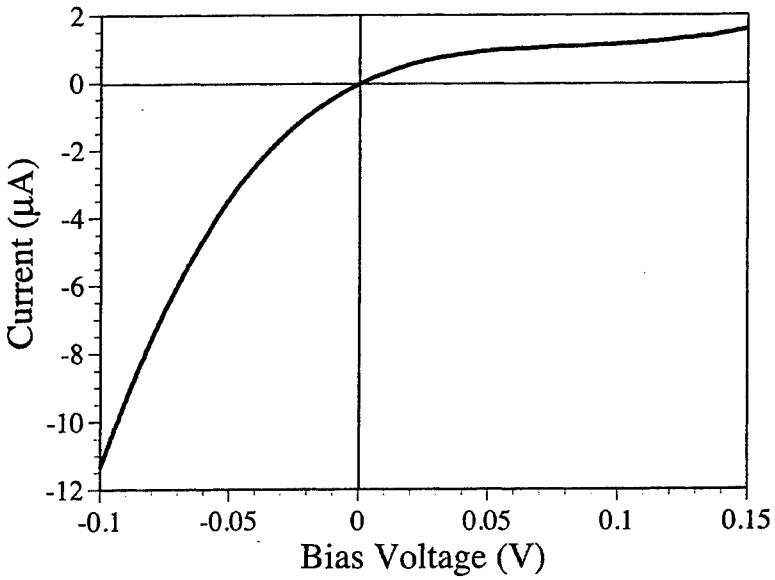


Figure 2. Measured current-voltage characteristic for a typical 1.5x1.5 μm² area device. Curvature at V=0 is 25.9 V⁻¹.

The curvature, $\gamma = \left(d^2I/dV^2\right)/\left(dI/dV\right)$, was measured to be 25.9 V-1 at V=0. The responsivity of the detector can be estimated from the curvature through the expression $\Re = 2Z_s\gamma$, where $\Re$ is the responsivity and Z_s is the RF source impedance [4]. This expression follows directly from the assumption of ideal square-law device behavior. For Z_s=50 Ω, this simple analysis suggests that the responsivity of these detectors should be approximately 2590 V/W. Higher-order nonlinearities and other effects not considered in this simple model are expected to cause the actual responsivity to deviate from this simple model.

III. Nonlinear Device Model

For the development of a nonlinear equivalent circuit model, on-wafer s-parameters were measured from 1-110 GHz as a function of externally applied bias. A network analyzer port power of -33 dBm was used to minimize distortion of the small-signal s-parameters due to device nonlinearity. The parameters for the equivalent circuit shown in Figure 3(a) were extracted as a function of applied bias. The bias dependence of junction capacitance, c_d, and conductance, g_d, are shown in Figure 3(b) for a typical 1.5x1.5 μm² area device. As can be seen in Figure 3(b), the conductance as extracted from the s-parameter measurements is nearly identical to the conductance determined from the derivative of the dc current-voltage characteristics. The absence of any detectable conductance dispersion suggests that no significant carrier trapping or surface effects are present in the device. The series resistance, r_s, was found to be approximately 14 Ω independent of applied bias.

A nonlinear device model based on these extracted parameters was implemented in a commercial harmonic balance simulator [5] using the equivalent circuit model in Figure 3. The

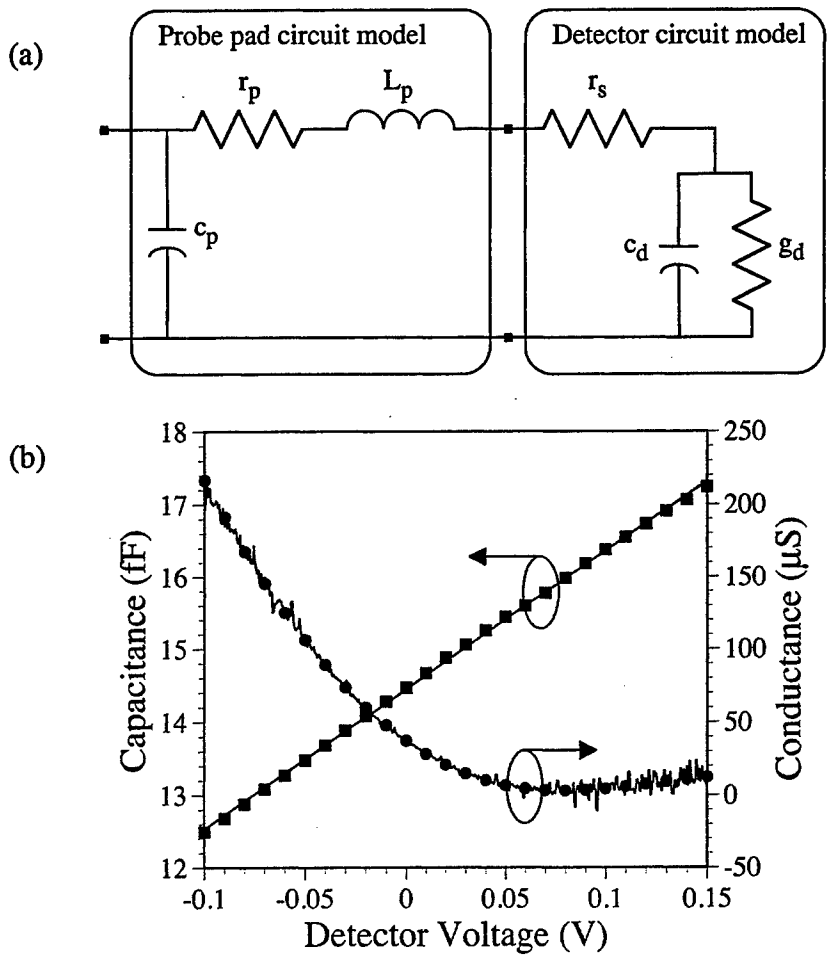


Figure 3. (a) Equivalent circuit for nonlinear circuit model. (b) Extracted junction capacitance (■) and conductance (●) from on-wafer s-parameter measurements from 1-110 GHz for a typical small-area device. Best-fit line through capacitance is shown, and conductance obtained from s-parameter measurements is superimposed over dc conductance for reference (solid line).

model is implemented as a nonlinear voltage-dependent current source for the junction conductance, and a voltage-dependent capacitor for the junction capacitance. The functional form of the current source was obtained by fitting a fourth-order polynomial to the extracted junction conductance vs. bias curve, and then integrating once with respect to voltage to obtain a current-voltage relation. The constant of integration was chosen to ensure that the dc current was zero at V=0. A least-squares linear fit to the extracted junction capacitance vs. applied voltage characteristic in Figure 3(b) was used to model the junction capacitance. Harmonic balance simulations using this model resulted in a predicted low-frequency detector responsivity of 2581 V/W. This is in good agreement with the value of 2590 V/W predicted from the ideal square-law model described previously. Examination of the relative contributions of various terms in the equivalent circuit model indicated that device series resistance is primarily responsible for the small observed deviation from the simple square-law model.

IV. High Frequency Detector Performance

The performance of the diodes as zero-bias detectors from 1 to 110 GHz was assessed through on-wafer measurements. The RF drive was supplied through a 1 mm coaxial cable and bias tee to a 100 μm pitch W-band Cascade wafer probe, and the detector voltage was measured using a microvoltmeter connected to the dc arm of the bias tee. Figure 4 shows the measured responsivity for a 1.5x1.5 μm^2 area detector as well as the result from simulations based on the nonlinear circuit model described above. For the measured data points shown, a source-impedance correction technique was used to remove the effects of the variation in wafer probe and millimeter-wave source impedance over the frequency range measured. The average measured responsivity over the frequency range from 1-50 GHz was 2597 V/W, consistent with the responsivity anticipated from the device model (2581 V/W). The frequency dependence of the responsivity predicted by the circuit model is also similar to that obtained by direct measurement, with both the measured and modeled responses starting to fall off for frequencies just above 100 GHz. At 110 GHz, the model predicts the responsivity should decline by 0.7 dB to 2390 V/W, while the measured responsivity at 110 GHz is 2341 V/W, 0.9 dB below the average responsivity from 1-50 GHz. The model predicts a -3 dB frequency for the responsivity of 187 GHz, which is beyond the maximum frequency attainable with the equipment currently available in the laboratory.

The maximum responsivity was also evaluated, as shown in Figure 4. For the modeled maximum responsivity curve shown in Figure 4, the source impedance was chosen to be conjugately matched to the detector equivalent circuit at the fundamental frequency. The low-frequency impedance-matched responsivity predicted by the model is $3.44x10^5$ V/W, and the responsivity at 95 GHz is $11.5x10^3$ V/W. For higher frequencies the responsivity falls to the

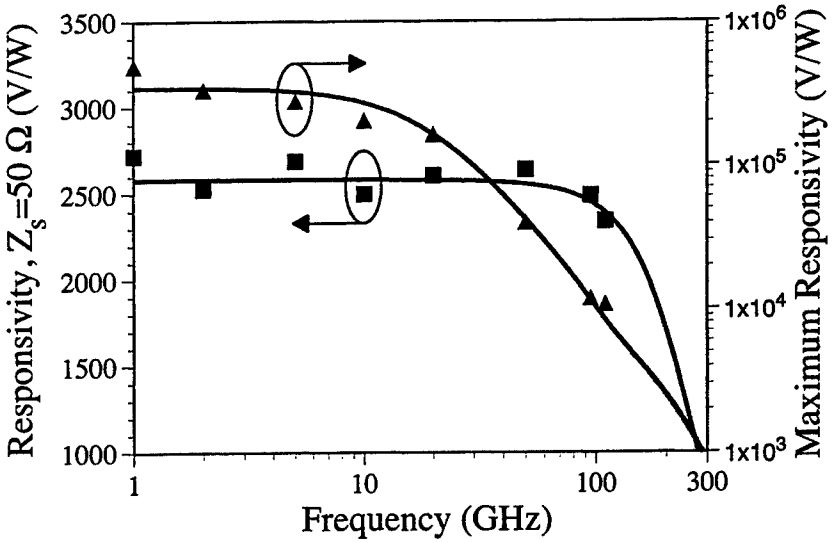


Figure 4. Measured and modeled responsivity vs. frequency for 1.5x1.5μm^2 area device. Data points (■) and curve referenced to left axis is for 50 Ω RF source; right axis data (▲) and curve is responsivity for conjugately-matched source impedance.

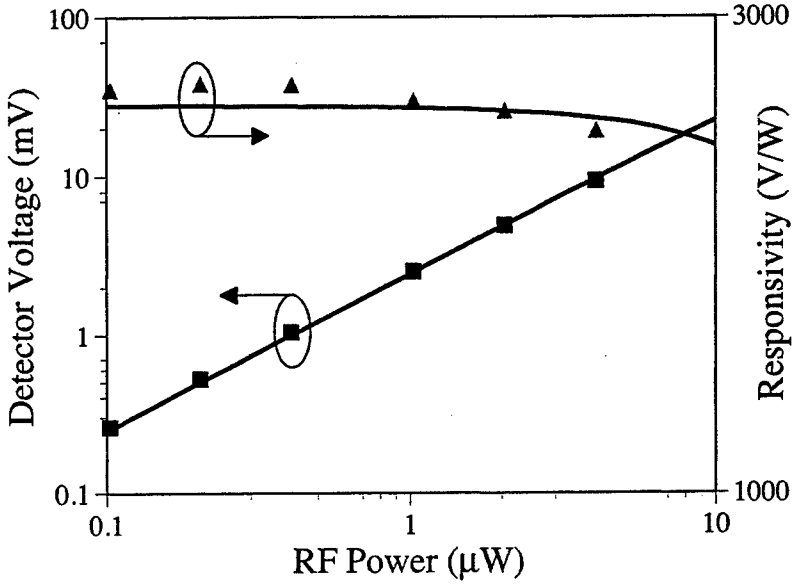


Figure 5. Measured and simulated detector voltage and responsivity vs. incident RF power at 95 GHz.

same magnitude as the low-frequency unmatched responsivity at 197 GHz, and to 1000 V/W at 286 GHz. As millimeter-wave tuners were not available to experimentally measure the impedance-matched responsivity directly, the unmatched measured responsivity data points, in conjunction with the measured s-parameters of the detectors, were used to project the responsivity that could be achieved with the inclusion of a lossless matching network between the source and detector. The measured Z_s=50 Ω responsivity, $\Re$, and measured S_{11} were used in the expression

$$\Re_{max} = \frac{\Re}{1-|S_{11}|^2}$$

to project the maximum responsivity experimentally; the results are plotted in Figure 4. Although this projection is approximate, neglecting in particular the effects of harmonic termination, it does give reasonably good agreement with the harmonic balance simulation.

The dependence of responsivity on incident RF power was also measured on-wafer as well as assessed through simulations using the device model. Figure 5 shows the measured and modeled responsivity vs. incident RF power at 95 GHz for a typical 1.5x1.5 μm^2 area detector. The measured and modeled detector dc voltage and responsivity track each other closely over almost the entire range of experimentally-accessible power levels. The maximum power in the experiments was limited to approximately 4 μW by the millimeter-wave source and cable losses. Compression of the responsivity by approximately 0.8 dB is observed experimentally for an incident power of 4 μW. The equivalent circuit model is somewhat optimistic in this regard, predicting a smaller drop in responsivity (0.3 dB) at 4 μW. At a drive level of 4 μW, the peak-to-peak voltage impressed across the diode due to the RF drive is approximately 80 mV due to the high diode impedance. This voltage swing is approaching the limits of validity of the

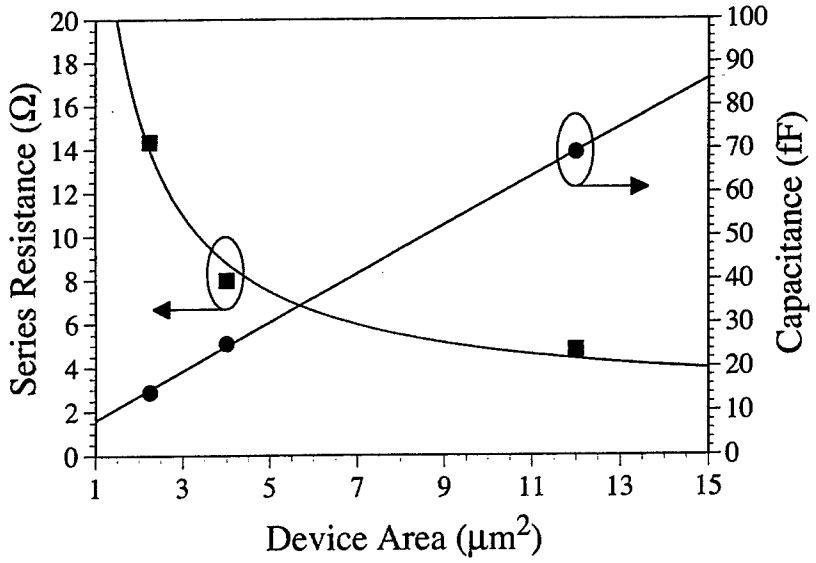


Figure 6. Scaling trends for series resistance(■) and device capacitance (●) obtained from fitting parameters of equivalent circuit to measured s-parameters of devices with varying areas.

current circuit model. Characterization of the devices over a larger bias range and use of higher-order fitting functions may be required to achieve better agreement at high drive levels.

V. Device Scaling and Optimization

The dependence of detector performance on diode area was investigated by characterizing devices with active areas ranging from 3x4 μm^2 to 1.5x1.5 μm^2. On-wafer s-parameter measurements of devices of different areas were made, and the circuit model shown in Figure 3 was extracted for devices of each size. The scaling trends for series resistance and junction capacitance are shown in Figure 6. Least-squares fitting to the extracted series resistance and junction capacitance resulted in the scaling relations

$$r_s = 26.65\ \Omega\mu m^2 / A + 2.15\ \Omega$$

$$c_d = 5.58\ fF / \mu m^2 A + 2.49\ fF$$

where A is the device area. The series resistance very nearly follows the expected inverse-area scaling, with the addition of a small offset resistance. Similarly, the diode capacitance was found to be nearly proportional to area except for a small additional parasitic component.

The scaling trends in series resistance and diode capacitance give rise to an optimal device area that maximizes detector bandwidth. For devices based on this heterostructure and fabrication process driven from a millimeter-wave source with Z_s=50 Ω, this optimum device area is approximately 0.19 μm^2. The I-line stepper used to fabricate the devices reported here has previously demonstrated the ability to print 0.4x0.4 μm^2 features, suggesting the feasibility of such a scaled device in this fabrication technology. Figure 7 shows the projected responsivity for a 50 Ω source and a conjugately-matched source vs. frequency for such an optimally-sized

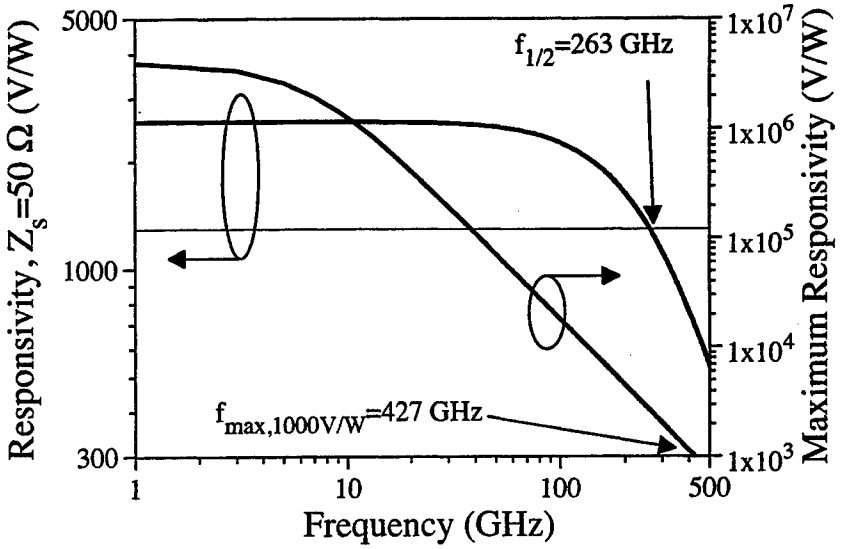


Figure 7. Projected responsivity vs. frequency for an optimally scaled 0.19 μm² area device. Responsivity with Z_s=50 Ω is 1/2 its low-frequency value at 263 GHz, while the conjugately-matched responsivity is > 1000 V/W for frequencies up to 427 GHz.

detector, as determined from the harmonic balance model using the scaling relations shown above. The Z_s=50 Ω responsivity drops to 1/2 of its low-frequency value at 263 GHz, while an impedance-matched detector exhibits a responsivity greater than 1000 V/W up to 427 GHz. Within the limitations of the circuit model, these Sb-based heterostructure backward diodes appear to be promising candidates for applications through G-band and beyond.

VI. Conclusions

The performance of antimonide-based heterostructure backward diodes as sensitive zero-bias detectors at millimeter-wave frequencies has been investigated. An average responsivity of 2597 V/W has been obtained experimentally from 1-50 GHz, and millimeter-wave responsivities of 2450 V/W and 2341 V/W at 95 GHz and 110 GHz, respectively, have been obtained. A nonlinear equivalent circuit model based on bias-dependent small-signal s-parameter measurements that is suitable for use with commercial harmonic balance simulators has been developed. The model has been verified using on-wafer responsivity and responsivity compression measurements of devices, and found to closely mirror the experimental data. The model has been used to predict the performance of a scaled detector, and suggests that this device technology should be suitable for detection at G-band and above.

VII. Acknowledgements

The authors wish to thank A. Seabaugh for the use of his 8510XF network analyzer for s-parameter measurements, M. Morgan and S. Weinreb for sharing their preliminary analyses of similar heterojunction detectors, and L. Warren and H. Dunlap for technical assistance.

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— INVITED PAPER—

InP/GaAsSb/InP Double Heterojunction Bipolar Transistors

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Abstract — InP/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) are some of the fastest bipolar transistors ever fabricated, with current gain cutoff and maximum oscillation frequencies simultaneously exceeding 300 GHz while maintaining breakdown voltages $BV_{CEO} > 6$ V [1]. InP/GaAsSb/InP DHBTs are particularly appealing because excellent device figures of merit are achievable with relatively simple structures involving abrupt junctions and uniform doping levels and compositions. This is a tremendous manufacturability advantage and the reason why some organizations have moved aggressively toward GaAsSb DHBT production despite a relative scarcity of information on the physical properties of the GaAsSb alloy in comparison to GaInAs. The present paper reviews some of the key concepts associated with the use of GaAsSb base layers, and discusses the physical operation InP/GaAsSb/InP DHBTs. In particular, we will describe the implications of the staggered band lineup at the E/B and B/C heterojunctions for charge storage in the devices, and show that InP/GaAsSb/InP DHBTs offer inherent advantages from that point of view. We will also show that GaAsSb-based DHBTs can be expected to display better scalability than GaInAs-based devices because of their inherently superior base Ohmic contacts.

I. Introduction

InP/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) are among the fastest bipolar transistors ever fabricated, with current gain cutoff and maximum oscillation frequencies simultaneously exceeding 300 GHz while maintaining breakdown voltages $BV_{CEO} > 6$ V when implemented with a 2000 Å InP collector [1]. We anticipate that $f_T = 400$ GHz should be achievable with a breakdown voltage of > 4 V in a 1000-1500 Å collector. The staggered band lineup and the absence of collector blocking effect in abrupt junction InP/GaAsSb/InP DHBTs enable a very high current drivability (even with relatively lightly doped emitter layers) that makes these devices attractive for ultrahigh speed digital circuits of the type needed for fiber network and instrumentation applications at 40 Gb/s and beyond. InP/GaAsSb/InP DHBTs feature a very low turn-on voltage $V_{BE,ON} \sim 0.4$ V at $J_C = 1$ A/cm^2 which also makes them attractive for long talk-time wireless applications operating with low battery voltage requirements [2]. InP/GaAsSb/InP DHBTs are particularly appealing because excellent device figures-of-merit are achievable with relatively simple structures involving abrupt junctions and uniform doping levels and compositions: the applicability of these devices outside a

[†] Now at *Agilent Technologies MWTD*, Santa Rosa CA.

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research laboratory setting has been validated at *Agilent* with the realization of circuit blocks based on conservative device structures: performances are already competitive with published state-of-the-art results for both GaInAs SHBTs and DHBTs [3]. The benefits of simple epitaxial structures allowing superior device performance simply cannot be overstated: InP/GaAsSb/InP DHBTs can be fabricated using selective wet etching techniques, and this is a critical manufacturability advantage when one is faced with the realization of HBTs with sub- 300 Å base layers in a production setting. In addition, C-doped GaAsSb can be grown by MBE and MOCVD, but the MOCVD growth proves extremely advantageous because it can be carried out using H_2 as the carrier gas and organo-metallic sources without running into H-passivation problems like GaInAs does. In this fashion, C- doped GaAsSb layers with hole concentrations as high as 3×10^{20} /cm^3 have been produced at SFU [4]. In general, SIMS analysis indicates that MOCVD-grown C-doped GaAsSb epilayers feature a much lower [H]/[C] concentration ratio than found in GaInAs, a finding of obvious potential interest from a burn-in / reliability point of view.

The situation with InP/GaAsSb/InP DHBTs is in marked contrast to the GaInAs –based DHBT case: the latter require sophisticated grading schemes at both the emitter and the collector (unless an InP emitter is used): by now it is widely understood that even a single extraneous/missing layer in a superlattice grading can have dire consequences on both the device static and dynamic characteristics (such as negative differential conductance, depressed current carrying capabilities, low current gains, large offset and knee voltages, and low cutoff frequencies). *With InP/GaAsSb/InP DHBTs the E/B and B/C junction characteristics are determined by the doping levels, heterojunction band offsets, and the bandgaps, not the effectiveness —or lack thereof— of various grading schemes intended to mask the natural blocking band offset between GaInAs and InP.* In a way, a GaAsSb base affords advantages that are of a similar nature to those provided by HBTs over HEMTs as far as turn-on voltage uniformity goes. Stated differently, InP/GaAsSb/InP DHBTs are practically unaffected if the emitter/collectors layers are off from their nominal design value by ± 50-100 Å.

The increasingly widespread acceptance and independent verification of the aforementioned manufacturing and device performance advantages by various entities of the III-V electronics community is at the root of the fast paced evolution of InP/GaAsSb/InP DHBTs from the status of an apparent technological dead end [5] to a technology worthy of serious consideration today. Industrial initiatives toward the development of GaAsSb –based DHBTs have now been launched in Canada, Europe, Japan and in the United States. A potential outcome of these R&D initiatives is that some organizations may, as we ourselves did at Simon Fraser University, simply abandon the development of GaInAs DHBTs in favor of the better-suited band alignment afforded by the GaAsSb alloy for DHBT applications.

II. Physical Operation of InP/GaAsSb/InP DHBTs

The Emitter/Base Junction

The equilibrium band alignment for an InP/GaAsSb/InP DHBT is shown in Fig. 1: the advantages from a collector blocking point of view are immediately apparent in comparison to the GaInAs-based DHBT case — because the p^+ base conduction band edge sits above the InP collector CB edge, electrons are injected into the collector *even under zero electric field conditions* at the B/C heterojunction. Some, perhaps taken aback by the unusual band diagram for a type-II DHBT, have expressed the concern that this approach may displace the "design problem" from the collector to the emitter. Firstly, the emitter is probably a better place to have a

problem in an HBT, if indeed one is going to have to solve one; secondly, there is no "design problem" with an InP emitter on a GaAsSb base as long as the ΔE_C is not too sizable. In fact, for a lattice-matched $GaAs_{0.51}Sb_{0.49}$ base with $\Delta E_C \sim 0.15$ eV at room temperature [6], a little bit of reflection should suffice to convince one that electrons experience thermal injection from the InP emitter into the GaAsSb base when the junction is forward biased. Back injection of holes is simply a non-issue because of the very large valence band discontinuity of $\Delta E_C \sim 0.78$ eV. This band lineup enables a very simple emitter structure consisting of a GaInAs contact layer followed by an abrupt junction to the InP emitter *per se*. On the other hand, one can also opt for a type-I $Al_{0.48}In_{0.52}As$ emitter that would launch electrons into the GaAsSb base with roughly some 0.1 eV of kinetic energy, based on our measurement of the band alignment between InP and $GaAs_{0.51}Sb_{0.49}$ [6], and on transitivity arguments with AlInAs. Care probably needs to be used in launching 'hot' electrons in GaAsSb because the ternary alloy may well have a low intervalley separation since both its binary constituents feature low Γ-L valley separations (GaAs: 0.29 eV and GaSb: 0.08 eV). Thus, even if feasible, hot electron injection beyond ~0.1 eV with an Al-rich $Al_{0.48+x}In_{0.52-x}As$ emitter is probably not a very good idea as far as speeding up transport across base is concerned.

Once across the E/B junction and into the quasi-neutral GaAsSb base, minority carrier electrons diffuse toward the collector with an apparent mobility of 900-1000 cm^2/Vs according to our most recent estimates. Others [7] believe the electron mobility in the base could be closer to values reported for GaInAs, and a definitive measurement remains to be carried out. This notwithstanding, the possibility of grading the base exists if it ever becomes necessary, although in our opinion it takes away from the simplicity of implementation inherent with InP/GaAsSb transistors. With an AlInAs emitter, nearly $4kT$ become available for grading across the base: apparently the most favorable grading approach would involve the formation of a Ga-rich (Al,Ga)AsSb base layer because the GaAsSb alloy features a stronger bandgap bowing than GaInAs, and that would diminish the potential impact of a group-V grading across the base.

The Base/Collector Junction

The staggered band lineup at GaAsSb/InP heterojunctions reduces the collector design problem to a consideration of doping and thickness of the InP collector for a given peak f_T current density J_C because electrons can be injected across the heterojunction *even under flat band conditions (i.e at high current density) at the B/C junction.* B/C grading design is not necessary, as the alloy potential effect[1] first described by Tiwari is non-existent in this system [8]. A simple uniformly doped InP collector of thickness W_C can thus be used with an abrupt heterojunction to the GaAsSb base. The resulting InP/GaAsSb/InP DHBT structure is thus nearly symmetric and about as simple as any transistor structure is going to get. Besides its simplicity, the GaAsSb base is directly sandwiched by (relatively) high thermal conductivity InP on both sides.

It has long been known that type-I GaInAs-based DHBTs with attractive device performances *can* be achieved [9], but it is interesting to consider the issues involved in such an undertaking: *a*) the blocking

[1] The alloy potential effect occurs when the increasing energy gap at a graded B/C junction is revealed as a result of the traveling electron space charge. Careful junction design and implementation is required to manage the effect by tailoring the electric field profile at the junction. Eventually, for a high enough current density, a retarding quasi-electric field appears at the junction that reduces the electron exit velocity from the base and cuts down the transistor cutoff frequency.

potential of 0.25 eV between GaInAs and InP results in a retarding quasi-electric field of $125/t$ kV/cm if a $200t$ Å grading length is used, and this sizable quasi-electric field intensity must be compensated by a combination of doping profile and applied junction reverse bias V_{CB}; *b*) the extent to which grading layers affect the electron velocity profile through the collector region; and *c*) the extent to which potential base dopant (Be/Zn, but not C) out-diffusion will interfere with the intended B/C band profile. Obviously, all these design issues can be addressed by a combination of less than mature numerical modeling tools and brute force trial-and-error.

In principle, based on the reported band alignment, electron injection from a GaAsSb base into an InP collector occurs by "ballistically" launching electrons with roughly $\Delta E_C = 0.15$ eV initial kinetic energy [5]. In practice things may occur somewhat differently: band gap narrowing due to the high doping concentrations of $4\text{-}8 \times 10^{19}$ /cm^3 used in GaAsSb bases may reduce ΔE_C below 0.15 eV, just as will the use of an As rich alloy in the base layer. A non-zero launching energy is expected to be beneficial from a collector signal delay time point of view because high velocities can be achieved over significant distances and over a range of electric fields in InP. Brennan and Hess considered the effects of launching energy in InP and reported that $E_i = 0.1$ eV would result in a velocity of $5.5\text{-}6.0 \times 10^7$ cm/s maintained over nearly 1500 Å in a field of 10 kV/cm. By contrast, $E_i = 0.42$ eV would lead to $\sim 8.5 \times 10^7$ cm/s maintained over nearly 1000 Å [10].

The staggered band lineup in InP/GaAsSb/InP DHBTs has interesting consequences inasmuch as charge storage is concerned during transistor operation. We previously contrasted the behavior of GaInAs SHBTs and DHBTs to that of GaAsSb based devices and found that the GaInAs DHBT features a dramatic increase of charge storage at high current densities because of the alloy potential effect at the B/C junction results in a sharp increase of the minority electron stored in the base layer. The InP/GaAsSb/InP DHBT features an altogether different behavior which was first discovered by Tom MacElwee of *Nortel Networks* while measuring devices fabricated at the SFU-CSDL (see Fig. 2): C_{BE} first dips with increasing current density and reaches a minimum value corresponding to the peak f_T bias occurring for the condition of zero electric field at the B/C junction. Further increases in current density reverse the electric field at the B/C junction resulting in the formation of a small field-induced thermionic electron barrier at the B/C junction. Despite the smallness of the induced barrier E_B, it is seen to have a tremendous effect on the base charge storage because it can be expected to reduce the effective base exit velocity by a factor $\sim\exp(-E_B/kT)$, resulting in a sharp rise in C_{BE} and a drop in $f_T(J_C)$. An indication of the smallness of E_B is confirmed by measurements of $f_T(J_C)$ characteristics as a function of temperature: as Fig. 3 clearly shows, the f_T roll-off with increasing current at higher temperatures becomes less abrupt as the chuck temperature increases because more base electrons can thermally overcome the small field-induced barrier at the B/C junction. Fig. 3 also shows that the current for peak f_T decreases with increasing chuck temperature as a result of the decreasing electron velocity in the InP collector at higher temperatures.

It is interesting to reflect on the implications of the above findings: we have found that InP/GaAsSb/InP DHBTs reach peak performance for zero B/C electric fields. In contrast, GaInAs –based DHBTs rely on a high B/C electric field to overcome the alloy potential due to the increasing energy gap moving from the base toward the collector, and this is true whether a bandgap grade or a launcher structure is used. This observation suggests that InP/GaAsSb/InP DHBTs would perform well even under low B/C biases V_{CB} such as those encountered in some bipolar logic families such as current mode logic (CML) circuits. Indeed, Fig. 4 shows that devices

maintain excellent cutoff frequencies even in saturation mode. This is because the large $\Delta E_V = 0.78$ eV at the GaAsSb/InP B/C heterojunction completely suppresses hole injection from the base into the collector.[2]

III. Scalability Issues

Antimonides generally feature a low hole Schottky barrier height which enables the formation of very low resistance p-type Ohmic contacts, an advantage that is in principle compounded by the affinity of GaAsSb layers for C-doping to very high levels. We have measured TLM base contact specific resistances for non-alloyed contacts as low as 10^{-7} Ohms-cm^2, a value for which the contact transfer length becomes comparable in magnitude to the error on the TLM gap spacing measurement in a scanning electron microscope (~ 0.1 μm). Roughly speaking, we have found that Ohmic contacts on GaAsSb bases typically yield 5-10× better Ohmics than on GaInAs, and this finding has been confirmed by others as well. This bodes very well for ultra-scaled DHBTs with deep submicron emitters since for such devices the base resistance no longer is dominated by the base spreading resistance (as it is with 1-2 μm wide emitters) but rather by the base metal/semiconductor contact itself.

We estimate that the hole Schottky barrier on GaAsSb should be of the order of 0.27 eV (compared to roughly 0.45 eV for metals on GaInAs). Based on these values, Fig. 5 shows the calculated specific contact resistance as a function of the base doping level: the plot shows that GaAsSb is expected to maintain an advantage up to ~ 10^{20} /cm^3. The different slopes in Fig. 5 is due to the difference in the valence band density of states for GaInAs and GaAsSb. Fig. 6 shows the evolution of f_{MAX} as a function of emitter width for a 250 GHz InP/GaAsSb/InP DHBT and shows that even conservatively scaled triple mesa devices maximum oscillation frequencies that are very close to what a GaAsSb transferred substrate device would show. Fig. 6 also shows the impact of a 10× degradation in base contact resistance (which is a typical contact resistance for GaInAs devices). Obviously, the excellent base Ohmic contact allows the device to scale very well.

Acknowledgements

This work was funded by the Canadian NSERC Strategic Partnership Programs, and by grants from *Agilent Technologies* (Palo Alto, CA) and *Nortel Networks* (Ottawa, ON). The authors are particularly indebted to Nick Moll (*Agilent*) and Tom MacElwee (*Nortel*) for their numerous contributions to this work.

[2] A side benefit of the large ΔE_V is that the hole injection into the collector through base pushout that occurs in SHBTs (and in some launcher-type DHBTs with a narrow gap collector section) at high current levels does not occur in GaAsSb DHBTs. The GaAsSb DHBTs are therefore not subject to the resonant enhancement of Mason's unilateral power gain U that can result in grossly overestimated values of f_{MAX} when U is extrapolated at –20 dB/dec from a frequency domain where U is resonantly enhanced by the injection of holes into the collector region. Bosse Willén and Heinz Jäckel from KTH/Stockholm and ETH/Zurich have pointed out this mechanism and investigated its impact on the perceived device performance [11]. They have shown that following a resonance U can roll off as fast as –40 dB/dec. Clearly, if the last measurement frequencies overlap with the frequency band of resonant enhancement, the f_{MAX} value obtained through –20 dB/dec extrapolation is of little relevance.

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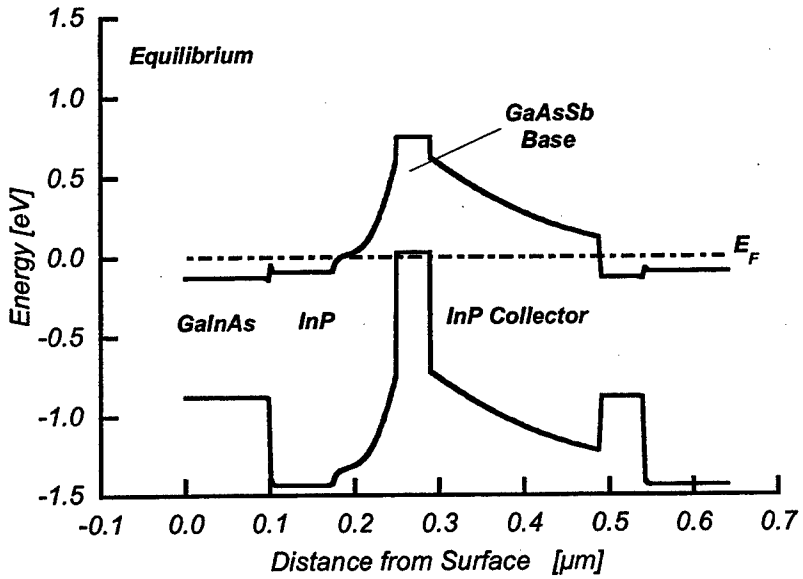


Figure 1: Equilibrium band diagram for an InP/GaAsSb/InP DHBT.

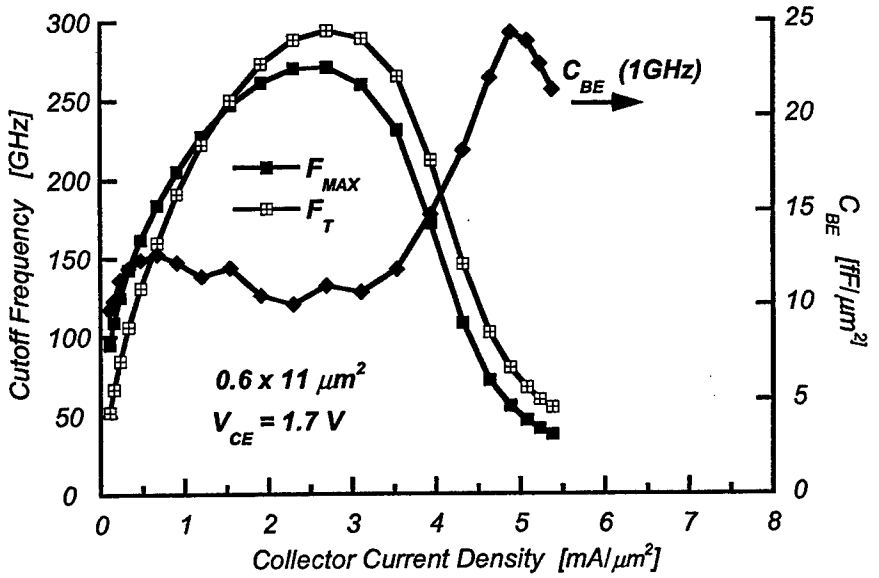


Figure 2: f_T and f_{MAX} plotted as a function of collector current density for an InP/GaAsSb/InP DHBT with a 200 Å base and a 2000 Å InP collector. C_{BE} displays an interesting behavior that is markedly different from the increases seen in type-I GaInAs or GaAs based SHBTs and DHBTs. For InP/GaAsSb devices, f_T peaks when the electric field drops to zero at the B/C junction, and further increases in J_C induce a small electrostatic barrier at the B/C that dramatically increases charge storage above 4 mA/μm² in this case. Measurement by T. MacElwee, *Nortel*.

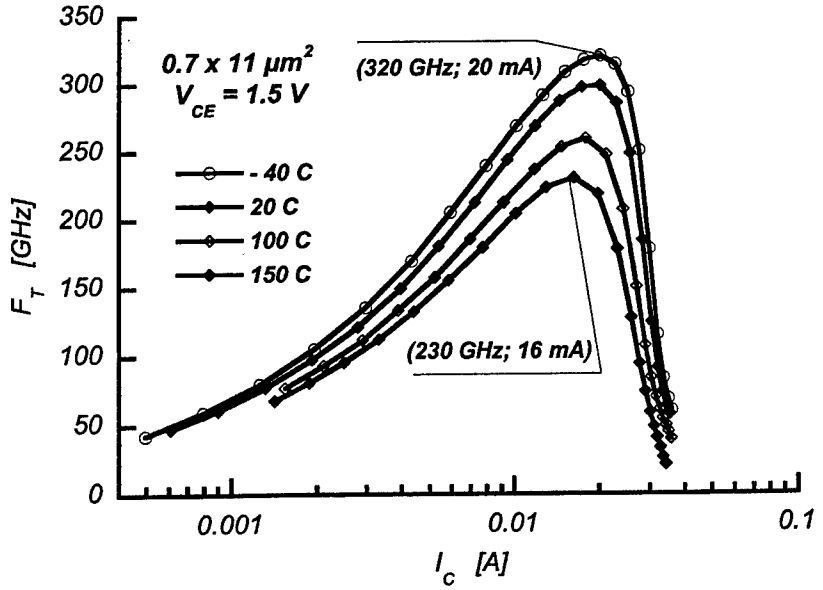


Figure 3: f_T dependence on temperature between –40 C and +150 C chuck temperature. Note that the high current roll off is less abrupt at higher temperatures, indicating that the electrostatic barrier at the B/C junction is small. The peak f_T current decreases with increasing temperature as a result of the lower electron velocity in the InP collector. Data by T. MacElwee, *Nortel*.

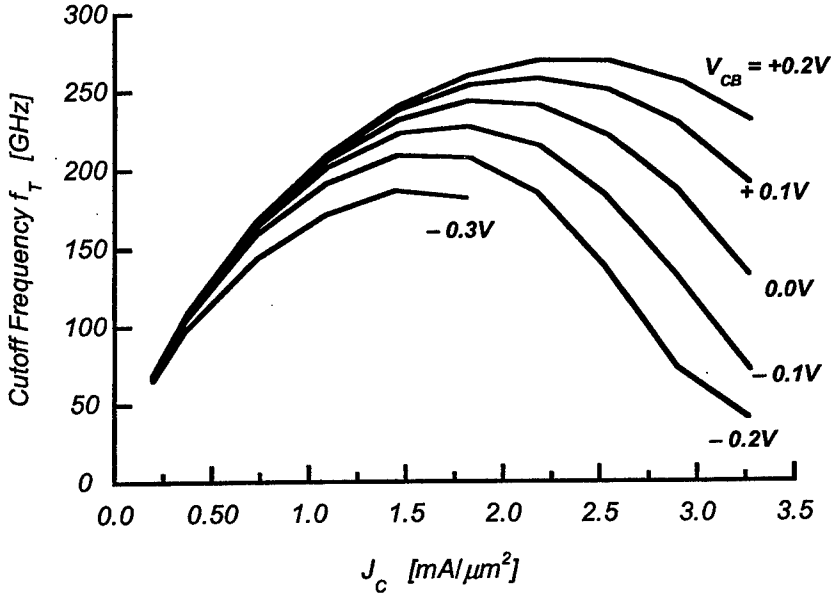


Figure 4: f_T dependence of a 200 Å base InP/GaAsSb/InP DHBT with a 2000 Å InP collector. The device clearly maintains excellent dynamic properties even in saturation mode. The data suggest that GaAsSb-based DHBTs should perform very well in ultrahigh speed CML circuits.

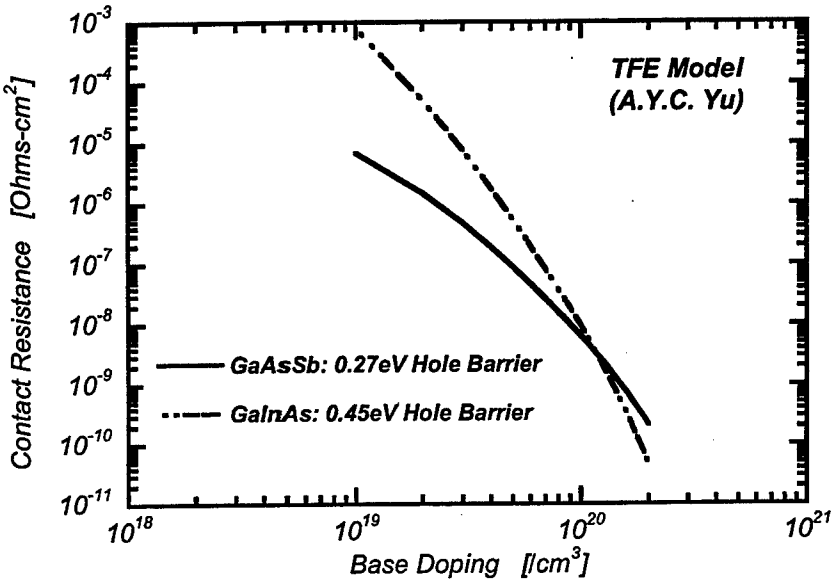


Figure 5: Calculated dependence of base specific contact resistance on base doping for GaAsSb and GaInAs base layers. The cross-over at very high doping levels occurs because the calculation assumes a lower valence band density of states for GaInAs —this assumption may no longer be valid for extremely high doping densities.

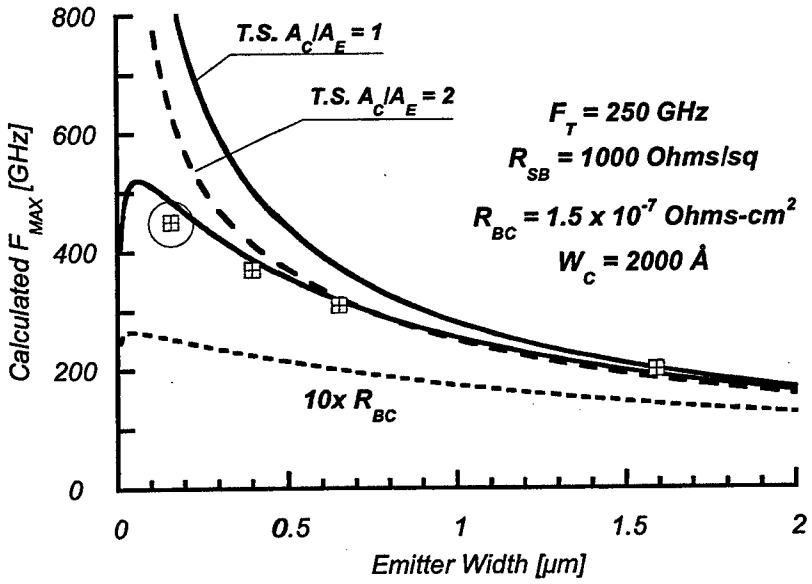


Figure 6: Calculated f_{MAX} for triple mesa InP/GaAsSb/InP DHBTs assuming a 0.5 μm base contacts. The two upper curves represent GaAsSb transferred substrate devices with the indicated area ratios, and the lower dashed curve shows the effect of a tenfold increase in contact resistance on the performance of mesa devices.

40 GHz MMIC Power Amplifier in InP DHBT Technology

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Abstract

We report a 40 GHz MMIC power amplifier in InP DHBT technology that exhibits 14 dBm output power at 1 dB gain compression and 17 dBm saturated output power with 4 dB associated gain. The small-signal power gain is 6.8 dB, the input return loss is less than –20 dB and the output return loss is less than -6 dB. The peak power added efficiency is 12.5%.

I. Introduction

Ka band power amplifiers have been broadly applied in satellite communication systems, wireless LANs, local multipoint distribution system, personal communications network links, and digital radio.

Although single heterojunction bipolar transistors (SHBT) have demonstrated high linearity and current density, the low breakdown voltage limits output power [1]. We have recently reported 0.5 um InP double heterojunction transistors (DHBT) in transferred-substrate technology having 7-volt collector breakdown voltage (BV_{CEO}) and 425 GHz maximum oscillation frequency (f_{max}) [2]. In the same process, multi-finger [3] DHBTs with emitter area of 16 um^2 per finger have been developed. These DHBTs exhibit 330 GHz small signal f_{max} at 100 mA bias current and 8 V breakdown at low current [4].

Here we report 40 GHz power amplifier employing this multi-finger DHBT. The amplifier achieves 6.8 dB power gain and 14 dBm output power at 1dB gain compression. The saturation output power is 17 dBm with a corresponding power gain of 4 dB and the peak power added efficiency is 12.5%. The die area of the power amplifier is only 0.6mm x 0.7 mm.

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II. Circuit design and fabrication

The amplifier is designed in the Cascode topology, taking advantage of the DHBT's high breakdown voltage. Thermal stability is a major design concern. As shown in Fig.1, in the multi-finger Cascode each emitter finger of the common base device is connected to only a single collector finger of the common emitter device. In this thermally-stable Cascode configuration [5,6], stability against current-hogging by a single emitter finger is ensured with less emitter ballasting than is required for a common-emitter HBT operating at the same collector bias voltage. Emitter ballast resistance nevertheless significantly reduces gain. Gain degradation due to parasitic layout impedance of the base bypass capacitor is a major difficulty in Cascode amplifier design. Even a very small parasitic inductance in the bypass capacitor results in significantly reduced gain. The emitter finger spacing is 7 um, with results in negligible thermal coupling between fingers [7].

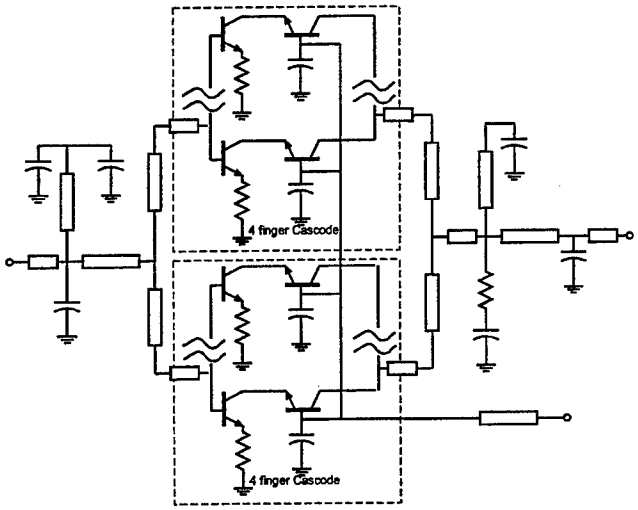


Fig.1: Cascode power amplifier circuit schematic

The 40 GHz power amplifier employs two parallel multi-finger Cascodes. Each multi-finger Cascode consists of 4 emitter/collector fingers. Each emitter finger has a contact size of 1um x 16um and the corresponding collector area is 2um x 20um. The two parallel 4-finger Cascode topology is chosen for two reasons: First, the low input and output impedances of each Cascode are pre-matched through their interconnecting microstrip lines. This eases design of the amplifier's matching networks. Second, by reducing the size of the multi-finger transistor from 4 to 8 fingers, reduced lengths are obtained for the wires interconnecting emitter and

collector fingers within the multi-finger cell. This is a key advantage in computer-aided design, as layout parasitics within the multi-finger cell are electrically significant yet difficult to model with finite-element CAD tools. The longer wires connecting the two 4-finger cells into an 8 finger transistor are microstrip lines with negligible line coupling, and are readily and accurately modeled.

The input network matches the transistor to 50 Ohms using an inductive microstrip line and MIM radial stub capacitors. A large shunt AC-grounded resistor connected to the Cascode output provides unconditional stability. In the output matching network, a shunt AC–grounded inductive microstrip line compensates the HBT output parasitic susceptance arising from the base-collector capacitance, and a low-impedance quarter-wave transformer transforms the 50 Ohm load to the HBT maximum-saturated load impedance:

$$R_L = (V_{CE,\max} - V_{CE,sat}) / I_{C,\max}$$

The maximum DHBT current is $I_{C,max}$ =128 mA with $V_{CE,sat}$=1.2 V, while a maximum collector emitter voltage $V_{CE,max}$=6.5 V< $V_{CE,breakdown}$ is selected as the dynamic operating range to avoid risk of device destruction.
The expected class-A saturated output power is approximately:

$$P_{\max} = I_{\max}(V_{CE,\max} - V_{CE,sat})/8 = 80\,\mathrm{mW}$$

The IC employs two types of MIM capacitors, with higher-capacitance devices using 0.4 μm Si_3N_4 dielectric and lower-capacitance capacitors to ground using the 5 μm BCB microstrip wiring dielectric. The SiN capacitors have much larger capacitance per unit die area, but have substantially larger processing variability due to variations in the thickness of the deposited dielectric film. Parallel combinations of the two, with capacitances appropriately partitioned between the SiN and BCB elements, result in a compact IC layout with reduced processing variability.

III. Measurement and results

Small signal measurements were performed on-wafer on an HP8150 network analyzer with on-wafer TRL calibration. Saturated power measurements were also performed on-wafer using micro-coaxial wafer probes. Reported power measurements include corrections for the known attenuation of bias tees, probes, and cables.

The amplifier die (Fig.2) is 0.7 mm ×0.6 mm. The circuit is biased at I_C=80 mA with 3.5 Volts V_{CE} applied to the common-base device and 1.5 Volts V_{CE} to the common emitter. The power supply is thus 5 V. Fig. 3 shows the small-signal S-parameter measurements. The small-signal power gain is 6.8 dB, the input return loss is better than –20 dB and the output return loss is better than -6 dB. Low S_{22} is not expected in power amplifiers, unless the balanced configuration is employed. The 3 dB bandwidth of S_{21} is 16 GHz. Fig. 4 shows 40 GHz saturated power measurements. The output power at 1 dB gain compression is 14 dBm, while the saturated output power is 17 dBm with a corresponding 4 dB gain. The peak power added efficiency is 12.5% when the amplifier is operating close to full power saturation.

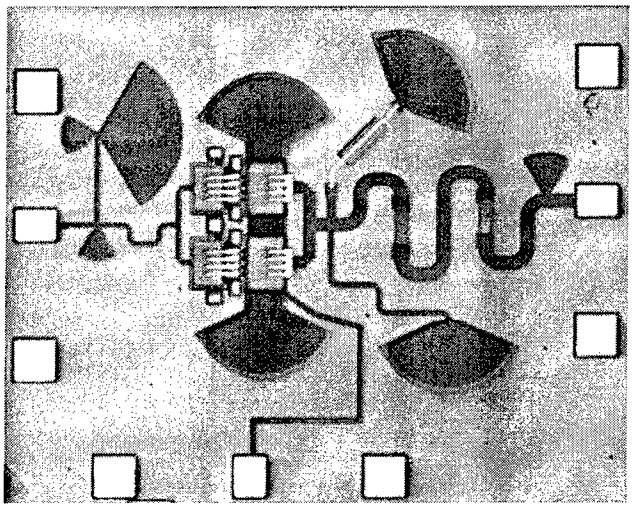


Fig.2: Amplifier die photograph

IV. Conclusion

We report a 40 GHz MMIC power amplifier in InP DHBT technology that exhibits 6.8 dB power gain and 14 dBm output power at 1 dB compression. The saturation output power is 17 dBm (50 mW) while the peak power added efficiency is 12.5%. Future work will seek to extend these results to higher power levels at higher frequencies.

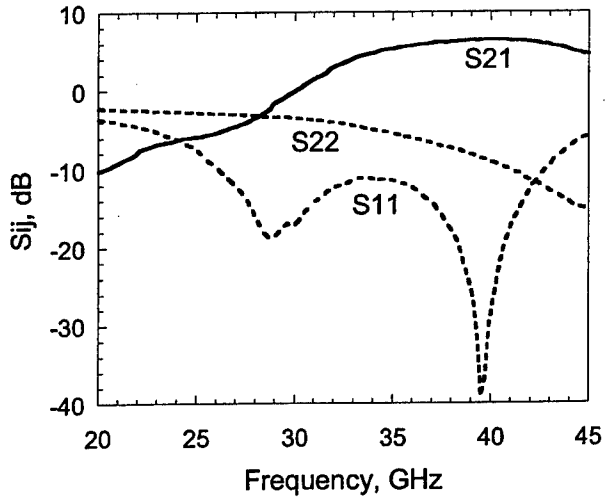


Fig.3: Amplifier small-signal gain-frequency characteristics

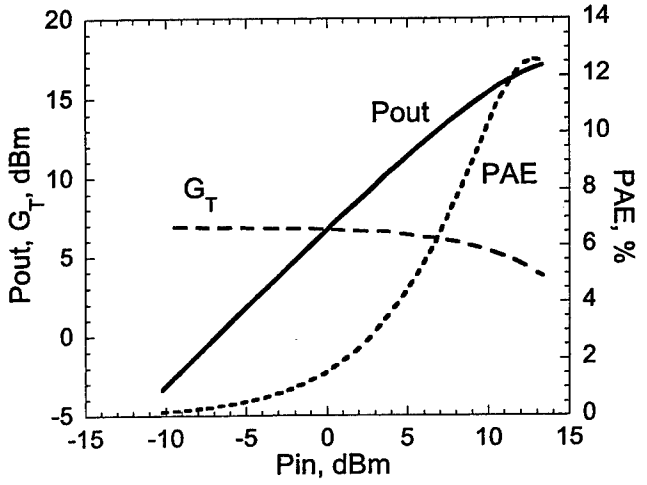


Fig.4: Amplifier saturated power characteristics

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Acknowledgement

This work was supported by the ARO Quasi-optical MURI under grant number PC249806.

GaInP/GaAs Tunnel Collector HBTs: Base-Collector Barrier Height Analysis

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Abstract

Tunnel collector HBTs employ a thin layer of GaInP between the GaAs base and collector regions, in order to suppress hole injection when the base-collector junction is forward biased. Devices with a low offset voltage of 30 mV, and low knee voltage of ~0.3 V, while still maintaining high current gain (170), and good RF performance with f_T=54 GHz and f_{MAX}=68 GHz have been demonstrated. The devices exhibit increased output conductance as compared to conventional GaInP/GaAs SHBTs, due to a residual barrier at the base-collector junction. This paper presents an experimental method for the determination of such barriers, by analyzing the collector current as a function of applied base-collector voltage, V_{CB}.

Introduction

GaInP/GaAs tunnel collector HBTs are under development in order to improve efficiency of battery-operated power amplifiers, by providing lower offset voltage, lower knee voltage and lower saturation charge storage than conventional HBTs [1]. The tunnel collector structure, shown in Figure 1, employs a thin wide-bandgap layer inserted between base and collector, with a thickness chosen such that electrons can tunnel through the layer while holes are blocked. Many of the positive attributes of both a SHBT and DHBT are thereby combined into one device. For example, because of the increased symmetry of the base-emitter and base-collector junction, the offset voltage is substantially reduced. Also, the majority of the collector is composed of GaAs, which avoids the reduction of mobility, saturation velocity, and thermal conductivity associated with GaInP collectors.

Layer	Material	Thickness(Å)	Doping (cm^{-3})
Emitter Cap	n^+-$In_{0.5}Ga_{0.5}As$	500	n > 1e19
	n^+-$In_xGa_{1-x}As$ (x=0-0.5)	500	n > 1e19
Emitter 1	n^+-GaAs	1000	n = 5e18
Emitter 2	n-InGaP	300	n = 3e17
Base	p^+-GaAs	500	p = 4e19
Tunnel	i-InGaP	100 / 200	-
Collector	n^--GaAs	4000	n = 3e16
Sub Collector	n^+-GaAs	4000	n = 5e18
Substrate	Semi Insulating GaAs		

Figure 1. Epitaxial layer structure for the Tunnel Collector HBT.

A representative TC-HBT structure is illustrated in the band diagram of Figure 2. Fabricated devices have demonstrated a low offset voltage, down to 30 mV, and low knee voltage of ~0.3 V, while still maintaining high current gain (170), and good RF performance with f_T=54 GHz and f_{MAX}=68 GHz [2]. Representative common emitter I-V curves are shown in Figure 3.

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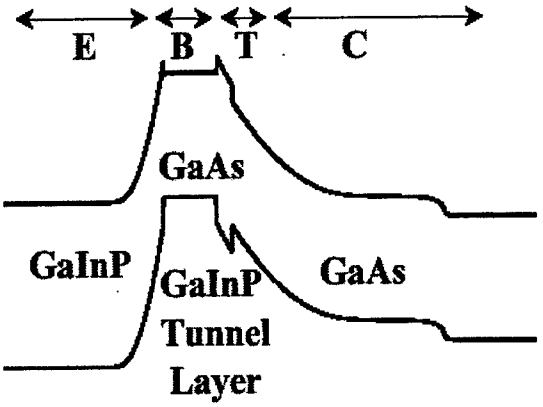


Figure 2: TC-HBT energy band diagram.

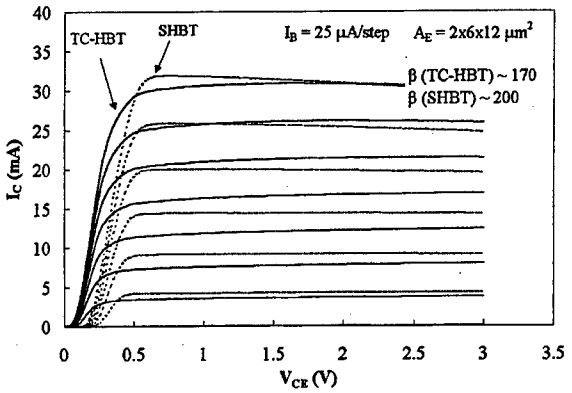


Figure 3: Common Emitter curves.

Typically, GaInP/GaAs tunnel collector HBTs show increased output conductance as compared with SHBTs of similar structure, as a result of a residual barrier at the base-collector junction that must be surmounted by electrons before reaching the collector. This barrier leads to a buildup of the electron density at the collector edge of the base. As a result, it tends to diminish the electron current reaching the collector because of a reduction in concentration gradient across the base. As the reverse bias on the base-collector junction increases, this barrier is pulled down, and transport through the GaInP is enhanced, resulting in an increase in the collector current, I_C. Figure 4 illustrates the I_C vs. V_{CE} curves for various devices, measured at a fixed V_{BE}, on a scale where the V_{CE} dependence is evident. At sufficiently large V_{CB}, the barrier drops below the conduction band in the base, becoming invisible to electrons, and the collector current saturates. By analyzing the collector current as a function of voltage applied to the base-collector junction, in conjunction with a theoretical model for its behavior, given below, it is possible to extract the effective height of this barrier.

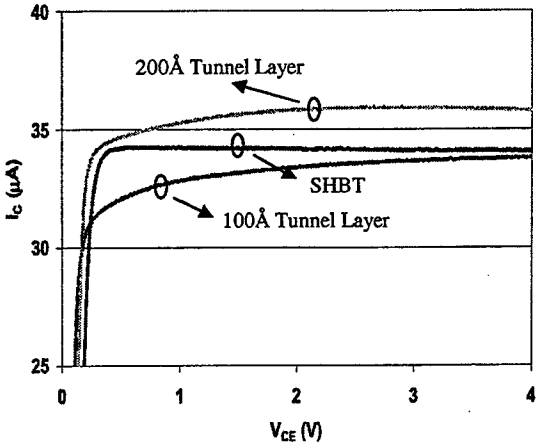


Figure 4. I_C versus V_{CE} for V_{BE}=1.08 V.

Theory

The collector current for a HBT, based on diffusive transport across the base, in the absence of any barriers at the base-collector junction, can be expressed as

$$I_{C0} = \frac{qD_n}{w_b}\frac{n_i^2}{p_b}\frac{\exp\frac{qV_{BE}}{kT}}{1+\frac{qD_n}{w_b v_{th}}} \qquad (1)$$

However, with an energy barrier present, electrons tends to accumulate at the collector edge of the base, and the expression becomes

$$I_C = \frac{qD_n}{w_b}\frac{n_i^2}{p_b}\frac{\exp\frac{qV_{BE}}{kT}}{1+\frac{qD_n}{w_b v_{th}}\exp\frac{E_b}{kT}} \qquad (2)$$

where E_b is the effective height of the barrier present at the base-collector junction and v_{th} is the effusion velocity for carriers [3]. Equation (2) assumes that electrons are thermally activated across the barrier at the base-collector junction. For the analysis of the tunnel collector HBT, it is assumed electron transport occurs by a combination of tunneling and thermionic emission over an effective barrier, the height of which is related to the tunneling probability. Tunneling effectively serves to reduce the given height of the barrier to a smaller value, which is the effective barrier height. In addition, the effective height of the barrier is dependent on the base-collector voltage, as shown schematically in Figure 5.

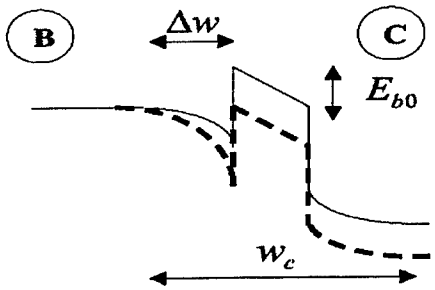


Figure 5. Base-Collector junction schematic.

Accordingly,

$$E_b = E_{b0} - \frac{\Delta w}{w_c} V_{CB} \qquad (3)$$

where E_{b0} is the effective barrier height in the absence of any externally applied V_{CB}, Δw is the width of the depletion region in the base, and w_c is the total depletion width at the base-collector junction. Equation (3) states that E_{b0} is reduced by the proportion of V_{CB} dropped in the base region. Combining equations (1), (2) and (3) yields an expression for the collector current that is dependent on V_{CB}, and serves as the theoretical model for the subsequent extraction of the effective base-collector barrier height:

$$I_C = I_{C0} \frac{1 + \frac{D_n}{w_b v_{th}}}{1 + \frac{D_n}{w_b v_{th}} \exp \frac{E_{b0} - \frac{\Delta w}{w_c} V_{CB}}{kT}} \qquad (4)$$

Experimental Results

For this work, two tunnel collector HBT structures, having 100Å and 200Å GaInP tunnel layers between base and collector, were employed. In order to extract the magnitude of the effective barrier height, the measured data was compared to predictions from the model above. A theoretical plot of the collector current as a function of base-collector voltage, V_{CB}, is overlaid onto a plot of the measured data, and fit accordingly as shown in Figure 6. Here, normalized data, $\Delta I_C/I_{C0}$, is used to allow direct comparison of the 100Å and 200Å structures on a single plot, where ΔI_C is the difference between the saturated value of the collector current and the collector current for a given V_{CB}, and I_{C0} the saturated value of the collector current. Straightforward manipulation of equation (4) allows the theoretical data to be cast into this normalized form, and is given by:

$$\frac{\Delta I_C}{I_{C0}} = 1 - \frac{1 + \frac{D_n}{w_b v_{th}}}{1 + \frac{D_n}{w_b v_{th}} \exp \frac{E_{b0} - \frac{\Delta w}{w_c} V_{CB}}{kT}} \qquad (5)$$

In order to fit the theoretical data to the measured data, it is necessary to input values for μ_n (for D_n through the Einstein relation), w_b, and v_{th}, which are displayed in Table 1.

Table 1. Material parameters for barrier height extraction.

μ_n (cm^2 / V s)	v_{th} (cm / s)	w_b (Å)
1000	2.0×10^7	500

Fitting of the 100Å and 200Å tunnel layer structures yielded effective barrier heights of 7 and 10 meV, respectively. These values are in the range expected, since the tunnel layers are quite thin, and designed such that electrons easily traverse the base into the collector.

An observation not anticipated by the above theory is the current dependence of the effective barrier height, as shown in Figure 7 for the 100Å tunnel layer device. As the current level increases in the device, shown in the plot as increasing V_{BE}, it can be seen that the magnitude of the effective barrier also increases, from 7 meV for V_{BE} = 0.99 V to approximately 13 meV for V_{BE} = 1.17 V. This

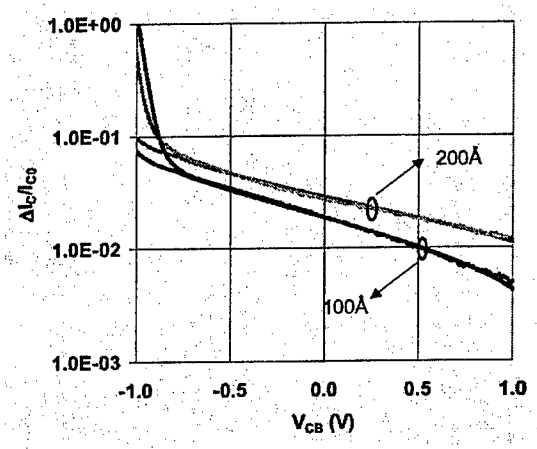


Figure 6. Comparison of theoretical and experimental values of $\Delta I_C/I_{C0}$ for barrier height extraction.

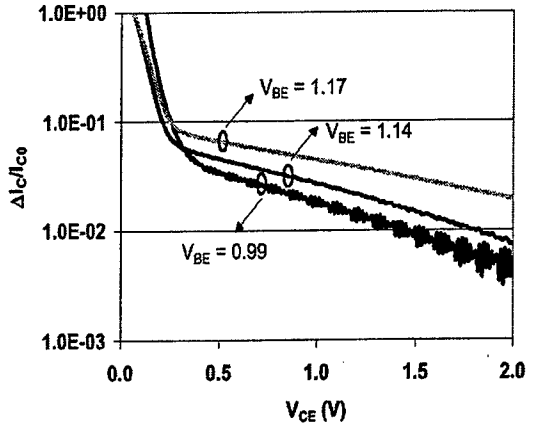


Figure 7. Measured values of $\Delta I_C/I_{C0}$ with varying V_{BE}, showing barrier height increasing with V_{BE}.

result is attributed to the current blocking effect of the barrier at the base-collector junction. As a result of the barrier, some electrons get trapped in the conduction band notch near the interface of the base region and the GaInP tunnel layer. Higher current levels tend to trap more electrons, which modifies the band profile in the vicinity of the base-collector junction, effectively pushing up the barrier, which in turns enhances the blocking effect. Similar effects have been observed for InAlAs/InGaAs DHBTs [4], as well as for SiGe HBTs operating at very high current densities [5]. This has important implications for tunnel collector HBT design, in that relatively small barriers of order 10 meV, can become increasingly troublesome as the device is operated at higher current densities.

Conclusion

A model capable of estimating the magnitude of the effective barrier height present at the base-collector junction, based on the fitting of theoretical expectations to measured experimental data, is proposed. The model predicts small barriers of approximately 7 and 10 meV for 100Å and 200Å GaInP tunnel layers between base and collector, at low current levels. In addition, measurements at various current levels indicate an increase in the barrier height for higher current levels, likely the result of the current blocking effect of the barrier, which traps electrons and modifies the band profile in close proximity to the barrier.

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Acknowledgements

The authors would like to acknowledge partial funding from the Army Research Office.

On-chip Out-of-Plane High-Q Inductors

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Abstract – Integrating high-Q inductors on semiconductor circuits has been an elusive goal for years due primarily to the eddy current losses and skin effect resistance associated with in-plane spiral inductors. Three-dimensional out-of-plane coils reduce eddy current and skin effect losses by virtue of their geometry and magnetic field orientation. However, out-of-plane coils were not deemed producible by standard semiconductor fabrication methods.

This paper reports on a novel use of conventional semiconductor processing techniques to batch-fabricate three-dimensional high-Q inductors on a wide range of insulating or active semiconductor substrates. Thin molybdenum-chromium films are sputter deposited with an engineered built-in stress gradient so that, when patterned and released from their substrate, they curl into circular springs. These springs self-assemble into three-dimensional scaffolds that form highly conductive windings after being copper plated. Quality factors up to 85 are observed at 1GHz on standard CMOS silicon.

The in-circuit microcoil performance is also compared in BiCMOS silicon L-C oscillators to that of state-of-the-art planar spirals with slotted grounds. A 12.3dB phase-noise improvement is observed with an earlier coil design that produced a maximum Q of 40, and 14.6dB taking the frequency and power differences into account. A 5μm copper layer underneath the coil boosts the quality factor to 85 and should therefore further improve the phase noise by up to 6dB.

I. Introduction

Transistors, capacitors and resistors are routinely integrated in massive quantities on various semiconductor circuits. The high-quality inductor hasn't been added this list. This hasn't slowed down the development of high-performance digital and baseband analog circuits. But it is increasingly troublesome for the RF front ends in cell phone handsets and mobile data devices. These are rapidly becoming commodity items and economic, thus preferably fully integrated standard CMOS front ends are needed to make next generation wireless devices possible. The quality factor of the current integrated inductors rarely exceeds 8, especially on standard low-resistance CMOS silicon, but values above 50 are often required.

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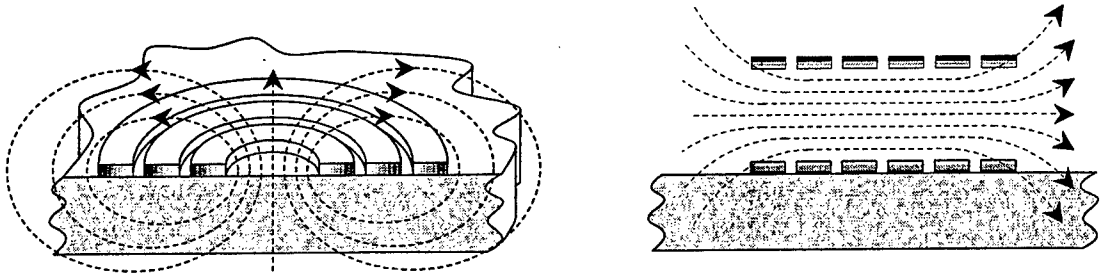


Figure 1. The magnetic flux and current density in conventional planar inductors (left) and out-of-plane solenoids (right). The shading indicates the current density.

Conventional integrated inductors are planar spirals implemented in one or several IC metal layers. These spirals suffer from two fundamental problems (Figure 1, left). First, the magnetic fields are projected straight into the substrate where they induce eddy currents that cause resistive losses. Second, skin and proximity effects push the coil current to the outer winding edge, which reduces the effective winding cross section. As the skin depth for copper at 1GHz is only 2μm, widening the traces does not improve their resistance.

Various configurations have been suggested to deal with these issues. Removing the substrate underneath the coil avoids the eddy currents [1], but leaves the skin effect problem. It is also expensive in terms of wafer real estate, as one cannot put circuits underneath the inductor anymore. Inductors tend to be large compared to the other components because a quality factor fundamentally scales with the inductor size. Lifting spiral inductors out of the wafer plane after processing improves their performance and leaves the substrate available for circuits. Magnetic forces [2] and the surface tension of a molten dot of solder [3] or polymer [4] have been proposed to lift planar structures. However, none of these techniques solve the skin effect problem. This issue has been addressed in the past with very tall windings fabricated by plating copper in a high-aspect ratio mold created in UV-sensitive SU-8 photoresist [5] or by LIGA[2] processing [6], [7]. Unfortunately, producing tall structures is difficult and often expensive, and the substrate eddy current losses remain unaddressed.

Out-of-plane inductors with a coil axis parallel to the substrate plane offer an answer to both issues (Figure 1, right). The bulk of the magnetic flux runs above the circuit substrate. Skin and proximity effects push the coil current to the outer winding surface rather than its edge. Widening the traces, a straightforward lithographical step, now does reduce the winding resistance. Out-of-plane solenoids were initially made by plating a connection between traces above and below a thick dielectric [8] but they were not tall enough for optimal Q. The bond wire microcoils in [9] have the appropriate large cross section, but the bond wire is too thin for optimal Q. Yoon *et al* present an out-of-plane solenoid with large cross section and ribbon windings [10], [11] using three-dimensional laser lithography on coil cores individually picked and placed on the wafer surface. The geometry approaches the ideal cylindrical solenoid of Figure 1, but the process seems difficult to scale to large volume production.

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[2] LIGA is a German acronym for Lithographie, Galvanoformung, Abformung (lithography, galvanoforming, molding).

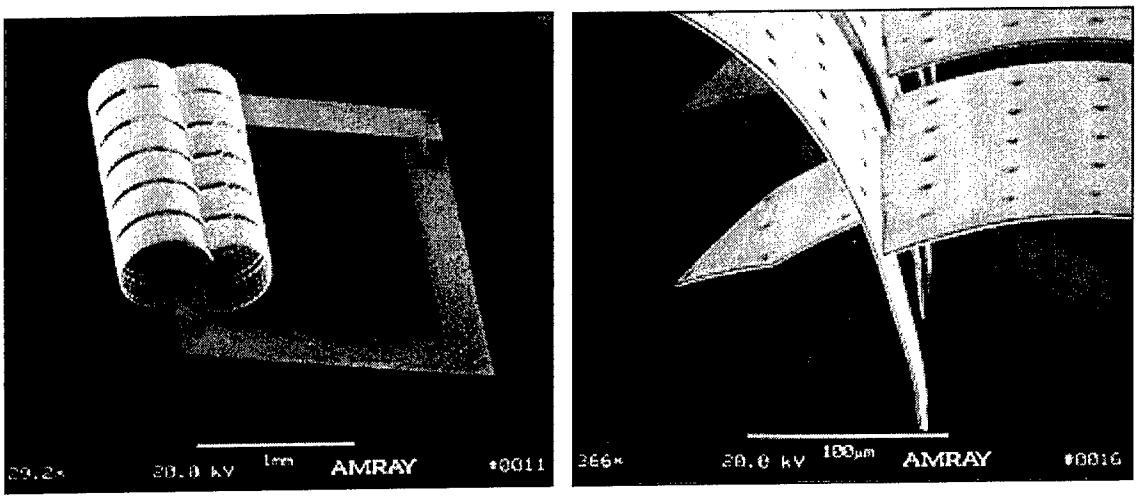


Figure 2. Self-assembled scaffold of a 6-turn out-of-plane coil (left) and close up of the interlocking springs (right).

This paper proposes a low-temperature batch process to micromachine cantilevers with engineered internal stresses that release from the wafer surface and interlock to a scaffold that is then electroplated with low-resistance metal for the coil windings (Figure 2). The solenoid shape is very close to the ideal cylinder and therefore promises excellent RF performance.

II. StressedMetal™ Out-of-plane Microcoils

The cantilevers in Figure 2 are made from a sputtered stress-engineered molybdenum-chromium (MoCr) alloy. MoCr is chosen because it is a refractory metal and can support large internal stresses. It can also be readily wet etched selectively from a host of commonly used release materials.

Stress engineering is accomplished by controlling the ambient pressure during film deposition. Many refractory metals have a common property of acquiring tensile stress when sputtered at high pressures and compressive stress when sputtered at low pressures. At low ambient pressures, sputtered atoms encounter few collisions before reaching the substrate. These energetic atoms tend to pack tighter than their natural arrangement. The tighter atomic arrangement forms compressively stressed films that prefer to expand when "released". Conversely, at high pressures, sputtered atoms loose most of their energy through collisions with ambient atoms before reaching the substrate surface. The sputtered atoms do not have sufficient energy to orient fully to their preferred natural arrangement. Consequently, they tend to form arrangements that are more loosely packed than normal. The film becomes tensile and would contract when released. Figure 3 plots the measured intrinsic stress versus the sputter ambient pressure of MoCr. There is a pressure, about 2.35mTorr in this case, where a stress-free film can be obtained. The exact stress-versus-pressure behavior depends on the sputter conditions, the substrate, and other process parameters and must be characterized for each particular configuration.

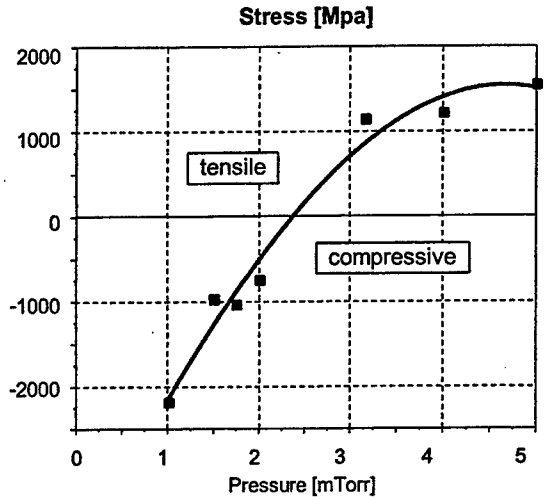


Figure 3. Stress versus sputter ambient pressure of MoCr alloy.

A film that is compressive at the bottom and tensile on the surface will, when patterned and released, curl up with a radius of curvature given by

$$r = h\frac{Y}{\Delta\sigma} \tag{1}$$

where h is the film thickness, Y the biaxial Young's modulus, and $\Delta\sigma$ the stress difference between the surface and bottom of the film [12].

The out-of-plane inductors are assembled from springs in opposite directions so that when released and self-assembled, they curl and interlock in pairs to form the coil windings (a movie of this process is available at http://www.parc.com/solutions/oopcoil/). The self-assembly of this symmetric double-spring structure is more tolerant to radius variations than a simple spring that curls all the way back to the substrate. The 3μm perforations shown on the right of Figure 2 provide extra access points for the etchant to speed up the release.

Unfortunately, good spring materials like MoCr are poor electrical conductors. The assembled spring structure is therefore electroplated with a 5 to 10μm thick copper skin. This also electroforms the interlocked spring tips to a permanent, continuous and solid structure that safely survives a drop from 1m on a hard tile floor.

With mobile communication applications in mind, a demonstrator coil was designed to operate around 1 GHz with a few nH inductance, a minimal Q of 60 and a parasitic resonance well above 1GHz. The quality factor requirements set the coil size: 200μm springs at a 230μm pitch, and a 267μm spring radius. Ten to 15μm of benzocyclobutene (BCB), a low-loss photo-definable dielectric, separates the microcoil from the substrate and controls the parasitic resonances. Vias through the BCB connect the coil terminals to the underlying circuitry.

Note that the microcoil size can be readily reduced to boost the operation frequency. The minimal coil dimensions are actually limited by the lithography and plating. Three-micron spring structures on a 6um pitch were demonstrated before for high-density interconnects [13]. Preliminary calculations suggest that a 10GHz operation frequency is quite feasible.



Figure 4. Alternative probe configuration: vias connect the probe ground to a metal layer underneath the coil.

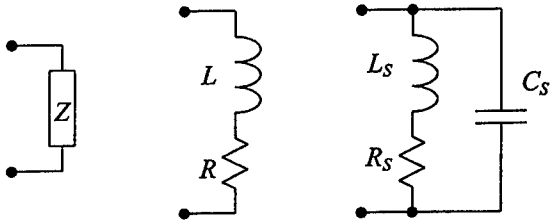


Figure 5. Equivalent L-R and L_S-R_S-C_S coil models.

III. Microcoil Measurements

In order to characterize the microcoil performance, their impedance is measured with an HP4396B combination analyzer and a HP43961A impedance RF test adapter. Each microcoil sample includes a set of ground-signal-ground landing pads for a Cascade Microtech ACP40 GSG-100 probe. The nearest coil terminal connects to the signal pad. The farthest terminal goes to the ground pads either via a loop around the coil (Figure 2) or via a metal layer underneath the coil (Figure 4). The latter configuration minimizes the in-plane inductance and associated losses.

Capacitive parasitics turn the coil impedance real at a resonance frequency ω_0. An analyzer measures the real and imaginary impedance terms R and $X = \omega L$ and thus lumps the resonance effects in the parameters L and R (Figure 5). A series L_S-C_S-R_S model separates the resonance from the inductance and loss resistance, and therefore allows a better understanding of the loss physics. Also, in a circuit where the coil is connected to a loss free capacitor, Q_S ($= \omega.L_S/R_S$) and not Q ($= \omega.L/R$) expresses the tank quality factor. The following expressions allow converting L-R data to L_S-C_S-R_S data [9]. Expression (2) for Q_S is exact. The L_S and R_S expressions are approximations for $|(\omega_0/\omega)^2 - 1| >> 1/Q_S$ but are numerically more stable near coil resonance than their exact versions.

$$Q_S = \left[Q \pm \sqrt{Q^2 + 4\left(\frac{\omega}{\omega_0}\right)^2\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)} \right]\left[2\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)\right]^{-1} \quad \begin{cases} + \text{ for } \omega < \omega_0 \\ - \text{ for } \omega > \omega_0 \end{cases} \tag{2}$$

$$R_S \approx R\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)^2, \quad L_S \approx L\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right) \text{ and } C_S = \frac{1}{\omega_0^2 L_S} \tag{3}$$

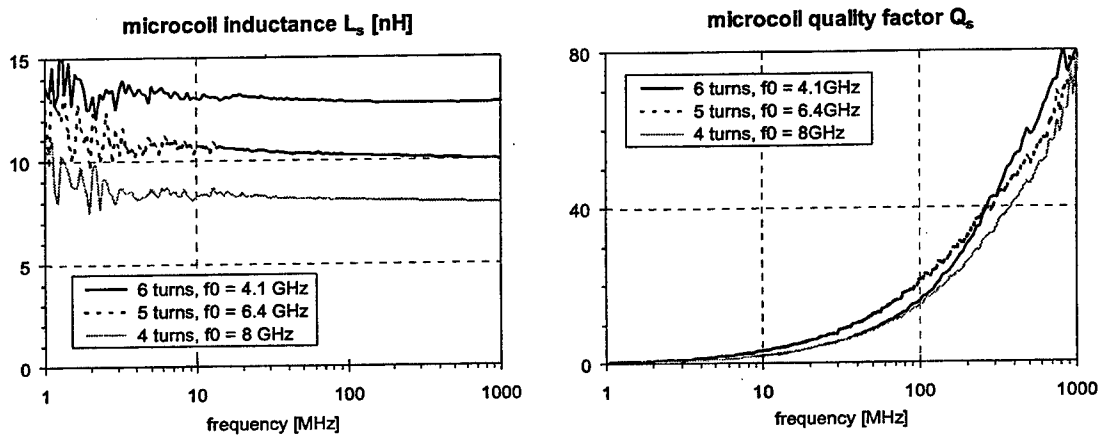


Figure 6. Inductances L_s (left) and Q_s factors (right) of out-of-plane coils on glass and quartz substrates. (f_0 is the parasitic resonance frequency). The probe pads are configured as shown on Figure 2.

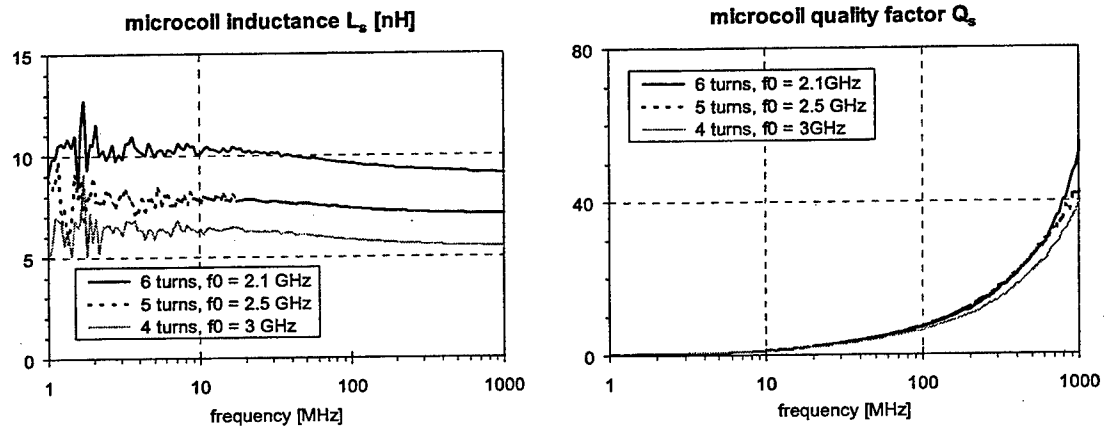


Figure 7. Inductances L_s (left) and Q_s factors (right) of out-of-plane coils on 15 to 20Ω·cm silicon (f_0 is the parasitic resonance frequency). Note the somewhat lower inductance compared to Figure 5 because of the alternative probe configuration.

Figure 6 plots L_S and Q_S data for a number of microcoils on glass and quartz. These data are an excellent a benchmark to compare the values on silicon against. The initial samples on silicon (Figure 7) had a probe configuration as shown in Figure 4 with the return current flowing in a 1μm aluminum on 50nm titanium-tungsten layer, comparable to the top metal on a conventional silicon circuit wafer. Although their quality factors rival the best values found in literature, they do show some substrate loss. Field simulations indicated eddy currents in the substrate and the aluminum near the solenoid ends. Lab experiments also confirmed that the 53mΩ/square aluminum was too resistive. A 5μm thick 5mΩ/square copper layer was therefore adopted to allow the eddy currents to run freely so they shield the silicon from the magnetic fields, but without causing significant resistive loss (Figure 8). The resulting quality factors of 60 to 85 at 1GHz represent an 8 to 10x improvement in comparison to the best spiral inductors on unaltered CMOS silicon that we are aware of.

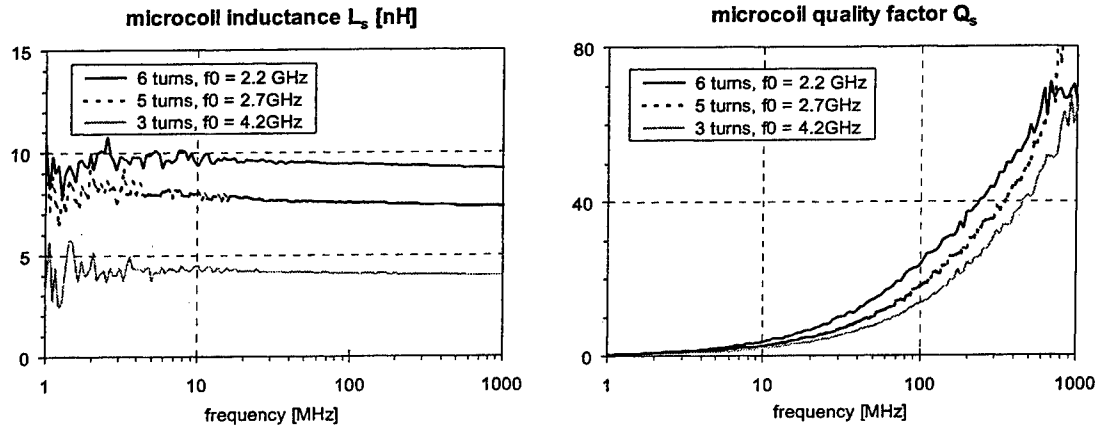


Figure 8. Inductances L_s (left) and Q_s factors (right) of out-of-plane coils on 15 to 20Ω.cm silicon with a 5μm copper layer for the return current (f_0 is the parasitic resonance frequency).

IV. OSCILLATOR

Leeson describes how the close-in phase noise of an oscillator relates to the quality factor of its loaded resonator [15]-[17]. The higher the quality factor, the lower the close-in phase noise. Oscillators are therefore often used to characterize in-circuit inductor performance.

The StressedMetal coils were compared in single ended and balanced L-C oscillators against state-of-the-art integrated spiral inductors with slotted ground planes [18]. The four oscillators were implemented on a chip (Figure 9) in a commercial 0.6μm BiCMOS silicon process (X-FAB XB06, 2 metals, 15GHz f_{Tmax} for the RF NPN BJT). The out-of-plane coils were configured as in our first design with the return currents flowing in the IC top metals. The oscillators shared a common architecture but the component values were optimized to each specific inductor. They were designed to operate around 1GHz but no attempt was made to match the frequencies.

The oscillator phase noise was measured with an HP8561E spectrum analyzer equipped with an HP85671A phase noise utility. As expected, the balanced oscillators outperformed the single ended designs because of the lower supply noise. In the balanced oscillators, a 12.3dB phase-noise improvement was observed with the StressedMetal inductors (TABLE 1), and 14.6dB taking the frequency and power differences into account [19]. This is in line with a Q improvement of a factor of approximately 4. The planar spirals are believed to have a Q of 8 to 10. The first out-of-plane coil design yielded a Q between 35 and 40 (Figure 7). The new design with a 5μm copper layer between the coil and the circuit substrate double that number (Figure 8) and should therefore further improve the phase noise up to 6dB. Current RF-IC processes frequently provide thick copper as the top metal.

Encapsulating the out-of-plane inductor in Dexter HISOL FP4511 epoxy did not influence the oscillator phase-noise. The microcoils were also found much sturdier than conventional 25μm bond wires. The StressedMetal coil technology is therefore believed to be compatible with standard injection molding IC packaging.

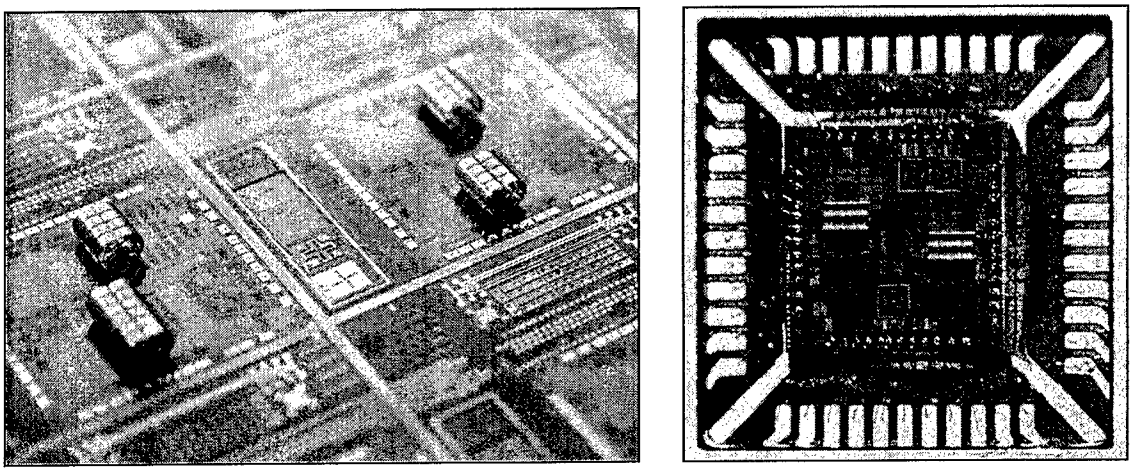


Figure 9. Out-of-plane inductors integrated on a BiCMOS silicon circuit wafer, before (left) and after (right) dicing and packaging. This prototype sports four oscillator cores: a single ended and a balanced circuit with either a conventional planar spiral on a patterned ground or an out-of-plane inductor.

TABLE 1. CIRCUIT RESULTS FOR THE BALANCED OSCILLATORS.

	Planar inductor	Out-of-plane inductor	
f_{osc}	966.6	1215	MHz
V_{CC}	3.3	3.3	V
I_{CC}	20	21	mA (incl. output buffers)
	3..4	3..4	mA (oscillator core only)
P_{out}	-1.2	-1.5	dBm in a 50Ω load
PN	-98.6	-110.9	dBc/Hz @ 100kHz offset

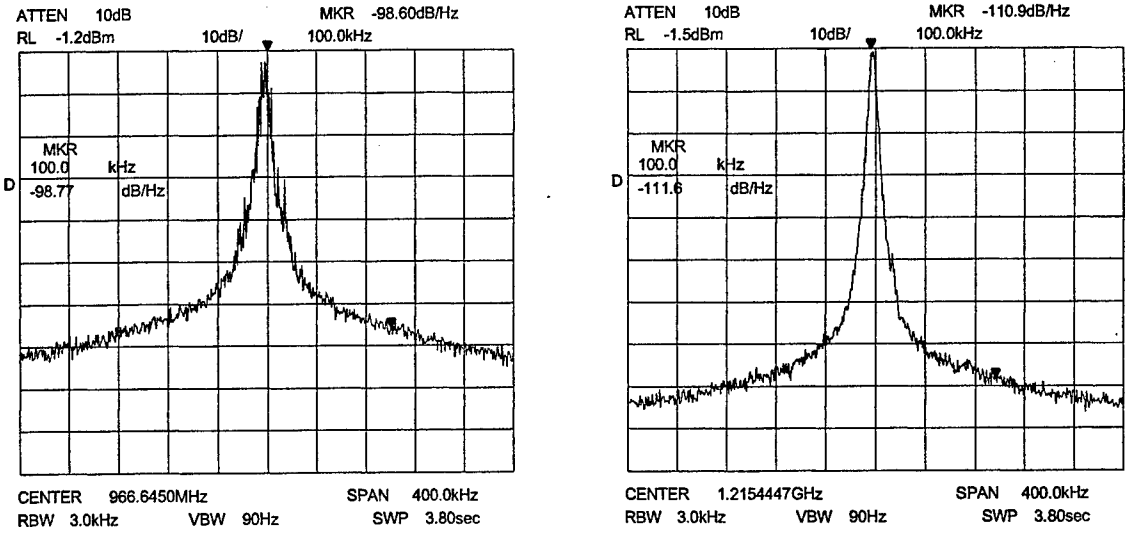


Figure 10. Phase noise plots of the balanced oscillators with planar spiral inductor (left) and with out-of-plane StressedMetal inductor (right).

V. Conclusions

The StressedMetal technology offers a new way to batch-process high-Q out-of-plane inductors by standard semiconductor fabrication methods on wide range of substrates, including active circuit wafers. Three-dimensional out-of-plane coils reduce eddy current and skin effect losses by virtue of their geometry and magnetic field orientation.

The demonstrator coils on 15 to 20Ω.cm silicon showed quality factors up to 85 at 1 GHz. The performance and manufacturability suggest substantial improvement over out-of-plane inductors previously reported.

To explore the circuit performance improvements obtainable with these inductors, coils of both the spiral (with slotted ground plane) and out-of-plane type were fabricated side by side on a chip manufactured in a commercial 2-metal 0.6μm BiCMOS silicon process. Each oscillator was optimized to its specific inductor. A 12.3dB phase-noise improvement was observed with an initial coil design that produced maximum Q's of 40, and 14.6dB taking the frequency and power differences into account. A 5μm copper layer between the coil and the circuit substrate, a feature that is often available with current RF-IC processes, should further improve the noise by up to 6dB.

Because this MEMS structure does not move after self-assembly, inexpensive molded packages with integrated coils should be feasible. Encapsulating the coils with Dexter HISOL FP4511 material did not affect the oscillator phase noise or measured quality factor.

VI. Acknowledgements

The authors are most grateful to Ms. Lai-Lui Wong and Ms. Yan-Yan Yang for the many weeks of processing microcoil samples, and Dr. Armin Völkel for the finite element simulations.

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Packaging of Microwave Integrated Circuits Operating Beyond 100 GHz

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Abstract

Several methods of packaging high speed (75-330 GHz) InP HEMT MMIC devices are discussed. Coplanar wirebonding is presented with measured insertion loss of less than 0.5 dB and return loss better than -17 dB from DC to 110 GHz. A motherboard / daughterboard packaging scheme is presented which supports minimum loss chains of MMICs using this coplanar wirebonding method. Split-block waveguide packaging approaches are presented in G-band (140-220 GHz) with two types of MMIC-waveguide transitions: E-plane probe and antipodal finline.

I. Introduction

In recent years, improvements in integrated circuit technologies have made robust, reproducible active monolithic microwave integrated circuits (MMICs) operating above 100 GHz a reality. Such circuits enable applications in high bandwidth communications, passive remote sensing, gas analysis, and millimeter wave astronomy. Although techniques for characterization and packaging of these mm-wave MMICs can often be scaled from lower frequency approaches, for frequencies above 100 GHz their implementation can become the primary factor limiting performance and subsequent system insertion. A significant amount of work has been performed in the area of packaging and testing of passive electrical devices operating up to extremely high frequencies (in the few THz) [1-2]. However, active devices provide additional challenges. This paper presents some examples of packaging of MMICs fabricated in an 0.1 μm InP HEMT process at HRL Laboratories with operating frequencies in the 75-330 GHz range. First, we discuss wirebond performance in this frequency range, as this is relevant to all packaging schemes presented here (as well as many others). Then, two packaging approaches are described. The first, a motherboard/daughterboard approach, is aimed at chaining many die with minimum loss while maintaining good DC delivery. The specific implementation demonstrated is for rapid prototyping in a laboratory setting. The second packaging approach is more conventional, interfacing the MMICs with standard mm-wave waveguide in split-block fixtures.

II. Wirebond Performance

The packaging schemes described below rely on wirebonding of the MMIC die to other components. Although this is common practice in the mm-wave circuit field, and published literature describing

0-7803-7478/02/$17.00 © 2002 IEEE

wirebond interfaces operating up to 40 GHz is available [3-4], we are aware of little published work characterizing such bonds up to or above 100 GHz. Here we present results of a study of coplanar wirebond interfaces between two 50 Ω coplanar waveguide with ground (CPWG) transmission lines fabricated in the same InP HEMT process as the MMICs described in this paper.

Each CPWG line is 1.83 mm long and contains closely spaced vias to the metallized back side of the 2 mil thick InP substrate as well as air bridge connections between the two coplanar grounds to suppress higher order modes. Measurements were performed using an HP8510XF vector network analyzer (VNA) with GGB Industries microwave probes, allowing single-sweep measurement from 45 MHz to 110 GHz. An LRRM calibration was performed to the probe tips using a GGB CS-5 calibration substrate and Cascade Microtech's WinCal™ software. Each line was individually measured before bonding was performed, in addition to the measurements performed after bonding.

The bonding procedure used for preparing these samples (and for high frequency MMIC bonding in general) is quite different from standard production wedge or ball bonding. The goal is to provide minimum length gold bonds very close to the substrate surface in such geometry as to minimize inductive or capacitive discontinuities at the interface. In order to minimize the bond length, if sufficiently narrow dicing channels cannot be provided, it is necessary to remove the excess bare InP substrate left between the edge of the pads and the die edge after scribing. This, in fact, was required with the die available for the work presented here. While additional dicing or scribing steps can be performed, it is exceedingly difficult to do this without chipping or otherwise damaging the extremely fragile 2 mil thin InP die. Our typical procedure is to grind down the die edge on a polishing turntable. After this step, the die are attached to a gold-plated handling substrate using silver-filled epoxy, with the polished die edges butted together. Then, 0.5 mil diameter gold wires are manually cut to length and bonded in place using a manual thermocompression bonder. Note that care is taken to ensure minimal spread of the bond feet on the center conductors into the signal-ground gap to minimize capacitive discontinuity. Also, multiple bond wires are provided on each ground, with one very close to the edge near the signal trace in order to minimize inductive discontinuity.

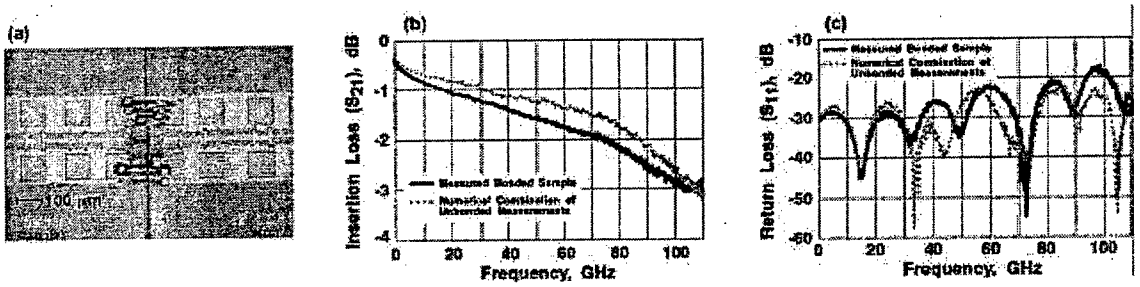


Figure 1. (a) Photograph and (b), (c) measured S-parameters of bonded CPWG transmission lines with minimum length bonds.

Photographs and measured data for a sample prepared in this manner are shown in Figure 1. Figures 1(b)-(c) show measured S-parameters for the bonded sample as well as the numerical chain combination of the measured S-parameters of the individual lines – an approximation of a "perfect" bond. The incremental insertion loss contributed by the bond is less than 0.5 dB across the entire measurement range, and the return loss is less than -20 dB across nearly the entire range, edging up to

-17 dB at 100 GHz. In short, excellent electrical performance is provided up to at least 110 GHz and likely much higher.

As the processing required to remove the excess bare InP between the pad edges and the die edge can be considerable, it is natural to ask to what extent this improves the electrical performance. Photographs and measured data taken on a sample prepared without the removal of the excess InP (roughly 300 microns total between the pads) are shown in Figure 2. The measured S-parameters (Figures 2(b)-(c)) show significantly degraded insertion and return loss above 40 GHz. Observation of the time domain step response representation of S11 (analogous to a time domain reflectometry measurement, not shown here) indicates somewhat more distortion and a significant inductive reflection at the bond interface. It is somewhat surprising that the degradation is so severe, given that the set of bond wires replicates the top-side coplanar environment fairly well. We speculate that the tendency of the bond wires to pull up slightly from the surface and the lack of vias or air bridge ties in the bond region are responsible for the parasitic inductance and resonances evident.

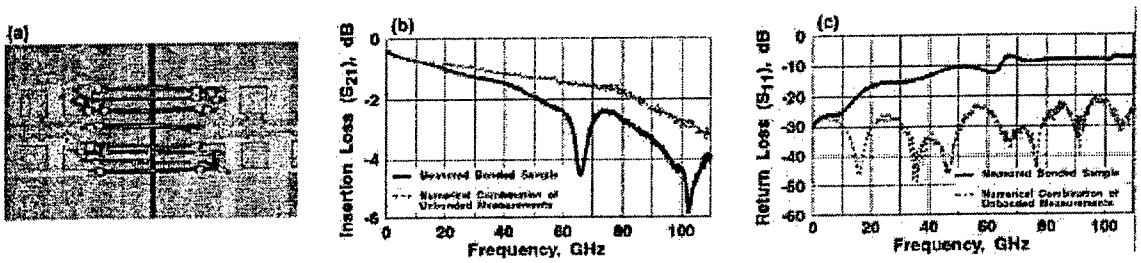


Figure 2. (a) Photograph and (b), (c) measured S-parameters of bonded CPWG transmission lines without excess substrate removed be tween pads.

III. Motherboard / Daughterboard Packaging

The most commonly used methods of packaging small circuits with inputs and outputs operating at more than 100 GHz utilize waveguide interfaces. As will be discussed in the next section, the key issue with waveguide packaging schemes is the design of a transition from the waveguide modes to the CPWG or microstrip environments typically used on the integrated circuit chips. Here we present an alternative packaging scheme that can be used for systems in which many MMIC die are to be chained end-to-end, in which these waveguide transitions are avoided, thereby minimizing the loss and volume associated with the packaging. This situation is not uncommon, as low yield of extremely high frequency, high performance devices is common, making monolithic integration of such a chain of MMICs difficult or impossible. In addition, in a development phase, it may be desirable to evaluate each component individually before chaining all devices together, not only due to yield issues, but also as accurate simulation and modeling of such high frequency circuits is extremely challenging.

The specific motherboard/daughterboard packaging approach described here (shown in Figure 3(a)) was designed for the development and test of high frequency sources comprised of a chain of InP HEMT MMICs. For example, a packaged 330 GHz source is shown in Figures 3(b)-(c), consisting of an 82.5 GHz voltage controlled oscillator (VCO) followed by an active frequency doubler, a 165 GHz amplifier, a second active doubler, and finally, a 330 GHz quasi-Yagi antenna [5-9]. Several design considerations led to the implementation shown. Many different candidate chains of MMIC die were

to be considered, so the design could not be optimized for a single MMIC chain – versatility was required. Independent control of each DC bias was desired for optimization. Minimization of the signal loss along the chain was deemed critical. It was assumed that there would be no external input (with the VCO providing the initial input to the subsequent stage) and that the output would either be to a high frequency microwave probe for laboratory testing, or antenna coupling to free space (as shown in Figure 3(c)).

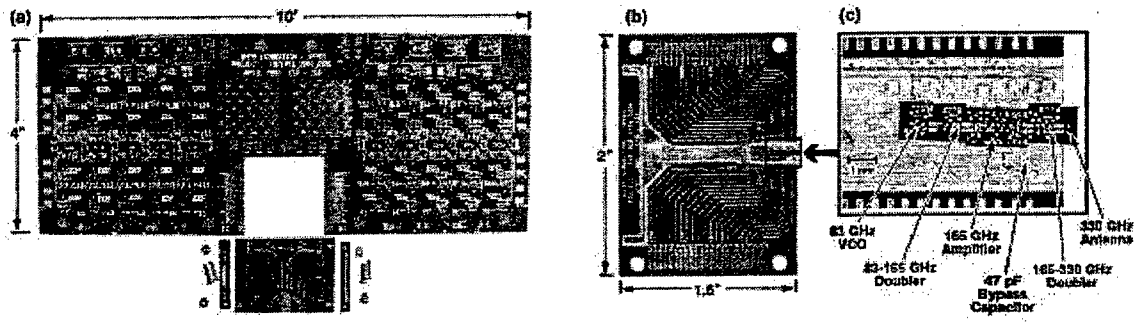


Figure 3. Photographs of (a) Motherboard with elastomer interconnects and daughterboard, (b) close-up of daughterboard with 330 GHz source MMICs, and (c) close-up of MMIC die in daughterboard cavity.

The daughterboard is simply a carrier for the MMIC die and some associated passives (e.g. bypass capacitors). It consists of a thick (1/8") copper plate covered with a layer of dielectric prepreg (2.5 mil polyimide) and core laminate (4 mil thick polyimide). A channel is milled through the dielectric layers, slightly into the copper base, the side walls of which are plated to provide a continuous wrap-around ground from the copper base to a ring around the cavity on the top surface of the dielectric. A 5 mil thick gold-plated copper shim is epoxied into the channel, on which the MMIC die as well as wirebondable bypass capacitors are placed. The shim provides a very flat surface on which the die can sit, and it also juts out slightly from the end of the copper base, providing additional support to the antenna die. A single gold-plated copper layer on top of the dielectric layers provides fan-out of up to 40 traces designed for delivering DC or low-speed (1 GHz) signals to the die from pads along the two shorter edges of the daughterboard. It was not anticipated that this many DC or low speed signal lines would be needed for any single MMIC string, but a large density was required in order that a wide range of chip designs and arrangements could be accommodated while still maintaining the flexibility of providing independent control of each DC connection with good power bypass capability (which is critical for stability).

The daughterboard is mounted face-up onto the underside of the motherboard using quick-disconnect vertical elastomer interconnects. The motherboard contains 40 independent simple linear DC supplies which can be used to supply the daughterboard traces with DC bias. Alternatively, these supplies can be disabled and bias can be brought in externally, such that the motherboard merely provides a convenient means for connecting them to the daughterboard. Additional bypass capacitance can also be placed on the motherboard as needed. We note that the MMIC die and associated high frequency interconnects consume a tiny fraction of the motherboard/daughterboard volume, with the rest dedicated to power or low speed signal delivery due to our desire for flexibility. Certainly, one could optimize a similar design specific to a given chipset to consume much less volume. Each high frequency MMIC-MMIC interface in the assembly shown in Figure 3 was

prepared using the method described in the above section for bonding of two transmission lines together. After this bonding was completed, the bypass capacitors were added and DC bond connections made using a commercial gold ball bonder.

Although all die were DC functional immediately following packaging, the 330 GHz source depicted in Figure 3 was found to emit only a few μW of power (compared with the 0.1-1 mW expected), and it was later determined that one or more of the MMIC die had failed during or just before high speed testing. For multiple reasons, we have not attempted to prepare another such 330 GHz source. Nonetheless, this packaging scheme has been used with success: as described elsewhere [8], detailed tests of the 165-330 GHz doubler MMIC used in the 330 GHz source chain were performed using die mounted in a similar package. Certainly, one disadvantage of this packaging method is that it is quite difficult to replace one die in the chain if it is malfunctioning, and it is practically impossible to reconfigure the die once they are committed to a given package. We have therefore moved towards waveguide block packaging methods (described in the following section) for continuation of this work, as it allows rapid reconfiguration and replacement of chain members. However, we maintain that a similar packaging scheme still has significant advantages for compact low-loss packaging of MMIC chains with minimum interconnection loss and reflection when the constituent die are fairly well-characterized and robust. In addition, we point out that the shim mounted in the daughterboard can be removed with die and bypass capacitors intact such that transfer to another (e.g. waveguide) package is possible after testing on the daughterboard.

IV. Waveguide Block Packaging

In the general case of a two-port MMIC (or two-port chain of MMICs), system insertion requires a robust package which is compatible with standard mm-wave interfaces. At frequencies above 100 GHz, rectangular metal waveguide is most often employed. Consequently, the package must include a transition between waveguide and the on-chip transmission line of the active device (usually CPWG or microstrip). To ensure minimum loss through the transitions, careful attention must be paid to their design. Several possibilities for the transition circuit present themselves based on scaling of lower frequency, microwave designs. Presented below are the results for two such approaches scaled to G-band (140 to 220 GHz). The first approach utilizes E-plane probe transitions fabricated on alumina substrates, while the second approach utilizes tapered antipodal finline etched on CuFlon® (copper on Teflon® from Polyflon). Both types of transition circuits are mounted within waveguide channels (albeit with different orientation) milled into solid metal split-block fixtures.

E-plane Probe Transitions

Planar probes have been extensively used at mm-wave frequencies for transitioning from rectangular waveguide to microstrip [10-12]. These planar probe circuits can be printed on any good microwave dielectric such as alumina. The probe itself is basically a metallized patch antenna that penetrates the waveguide at right angles through an opening in the broad wall and sits entirely within the waveguide. One end of the patch is connected to a microstrip line through an impedance matching section to connect to the MMIC outside the waveguide. As such the connecting microstrip line is perpendicular to the longitudinal direction of the waveguide. For minimum loss the connecting microstrip must be as short as possible. This dictates that the waveguides at input and output must provide 90 degree (E-plane) bends. The dimensions of the patch, its penetration into the guide, and its distance from a backshort in the waveguide (for impedance matching to the waveguide) are all part

of the design of the transition. The plane of the patch and its supporting substrate can be either perpendicular to the narrow wall [11], or parallel to it [12]. In the latter case it is called an E-plane probe transition. E-plane probe transitions printed on alumina and Teflon® substrates exhibit insertion loss of less than 0.9 dB and 0.7 dB, respectively, at 100 GHz based on insertion loss measurements of back-to back transitions [12].

We show an example of the use of E-plane probe transitions fabricated on 2-mil alumina for characterizing an InP 165 GHz medium power MMIC amplifier (one of the HRL die mentioned earlier) in a split-block waveguide fixture. The split block, which is machined out of two blocks of metal (gold-plated brass, in this case), is a common approach for packaging mm-wave devices and circuits. Waveguide channels, as well as cavities for active device mounting, and mounting of printed circuit boards (PCB) for bias distribution, can be milled into each half of the block. Figure 4(a) shows the bottom half (base) of such a block with mounted MMIC, E-plane probe transitions, and PCB containing the bias network. All components are mounted with silver-filled epoxy. Also seen in the photo is the bottom half of the G-band waveguide channel. The block is machined so as to split the waveguide down the middle of the broad wall. Half the channel resides in the base with the other half in the mating cover. Both input and output waveguide channels complete 90 degree turns prior to interfacing with the E-plane probe transitions (seen as two 45 degree bends in Figure 4(a)). Note the backshort (the end of the milled channel) that is permanently machined into the block in Figure 4(b). Bias for the MMIC is fed from a printed circuit board (PCB) which provides a common drain voltage and provision for separately adjusting all gate voltages. For stabilizing the high gain transistors at low frequencies, bypass chip capacitors (~ 0.1 μF) and series ferrite beads are used on the PCB. Smaller, 47 pF chip capacitors are mounted directly adjacent to the MMIC.

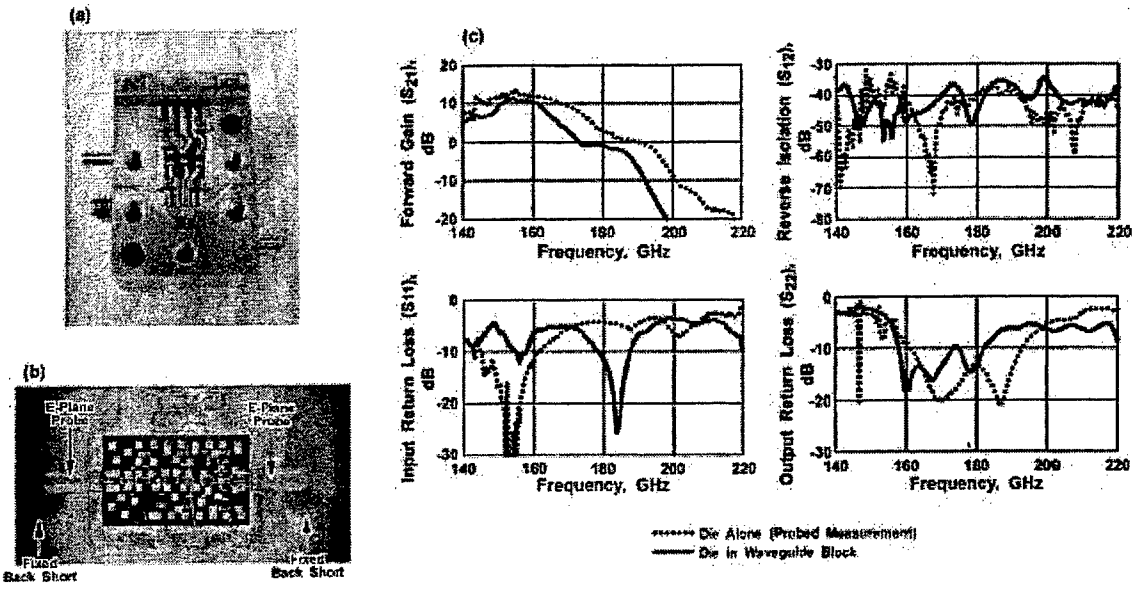


Figure 4. Photographs of (a) full waveguide block (bottom half) and (b) close-up of G-band amplifier with E-plane probe transitions. (c) Measured S-parameter data of amplifier mounted in waveguide block along with measured data on bare MMIC die (using microwave probes).

The S-parameters of the packaged amplifier were measured across the 140-to-220 GHz frequency range (solid lines) using an HP 8510C VNA with extender heads (downconverters) from Oleson Microwave Labs for extending the VNA capability into G-band. Calibration was accomplished using a G-band waveguide calibration kit. Figure 4(c) shows the log magnitude plots for all four S-parameters of the packaged amplifier. A peak gain of 11 dB is obtained at around 155 GHz, and "useful" gain of more than 6 dB is obtained from around 140 to 170 GHz. For comparison, also shown is the corresponding data taken with GGB high frequency probes on bare die with the reference plane established at the probe tips. The forward gain of the packaged amplifier is seen to be degraded by as much as 6 dB in the 160 to 180 GHz band. Similarly, the return loss is generally poorer for the packaged amplifier. The extra loss is due to the unavoidable dissipative loss of the transitions, wire bond interfaces, and limitations of the E-plane probe implementation at G-band (precision placement, backshort optimization, etc.). Although direct measurement of the E-plane probe loss at G-band (e.g., through a measurement of a back-to-back structure) is not available, based on the insertion loss results of Figure 4(c) and published data at lower frequencies [12], we estimate the loss per transition to be at least 1.1 dB at 165 GHz.

Finline Transitions

As an alternative to the E-plane transitions on alumina, another viable approach for interfacing mm-wave MMICs with waveguide is to use a planar transition based on tapered antipodal finline. This type of transition was first described by van Heuven [13] who demonstrated it in the upper microwave range (17.5 to 26 GHz in two waveguide bands) using fused quartz for the substrate. Although quartz is an excellent microwave dielectric material, it is quite fragile, and a more robust solution is to use a soft substrate such as Teflon® [14]. The transition essentially consists of three cascaded transmission lines: a tapered antipodal finline section; a balanced "stripline" section; and finally the unbalanced microstrip (see Figure 5(a)). The plane of the fin-supporting substrate, and the metallized fins, are centered between the narrow walls of the waveguide. The grounded sides of the fins terminate at, and are short-circuited by each broad wall. The dielectric material is kept as thin as possible (limited by mechanical constraints) to minimize unnecessary dielectric loading of the waveguide and to ensure single mode excitation of the microstrip. We have developed a scaled version of such a transition for application in G-band. Its performance in terms of a back-to-back test structure is presented next. To our knowledge, this is the first demonstration of van Heuven's transition above 110 GHz.

Figure 5(a) shows an example of a copper-metallized test structure for G-band operation etched on 2-mil-thick CuFlon®. The structure consists of two back-to-back transitions with an interconnecting microstrip line. In the figure the dark portion of the pattern is actually the backside metallization which, in the center of the structure, serves as the ground plane for the microstrip line. In the tapered section the taper opens up to the full height of the G-band waveguide (0.65 mm). One practical advantage of this transition is that it is aligned longitudinally with respect to the waveguide, and is therefore consistent with an in-line physical configuration for any two-port application.

For mounting and testing of the transitions a split-block approach is used as before. Figure 5(b) shows the assembled split-block with the G-band waveguide aperture, the top cover, and the base with the test structure mounted in the milled channel. Provision is made in the channel to support the CuFlon® card by its edges, so that when the two halves of the block are assembled the edges of the card are clamped between the cover and base. Cavities are also provided in both halves of the block to accommodate PCBs for bias distribution in future active device assemblies. The design of the

transitions was basically scaled from previous lower frequency circuits [14] and optimized for operation in the lower half of the waveguide band. The taper profile is an empirically-derived profile and uses arcs of a circle for the taper shape. Electrically, the length of the taper is about 1.5 wavelengths for a center frequency of 165 GHz.

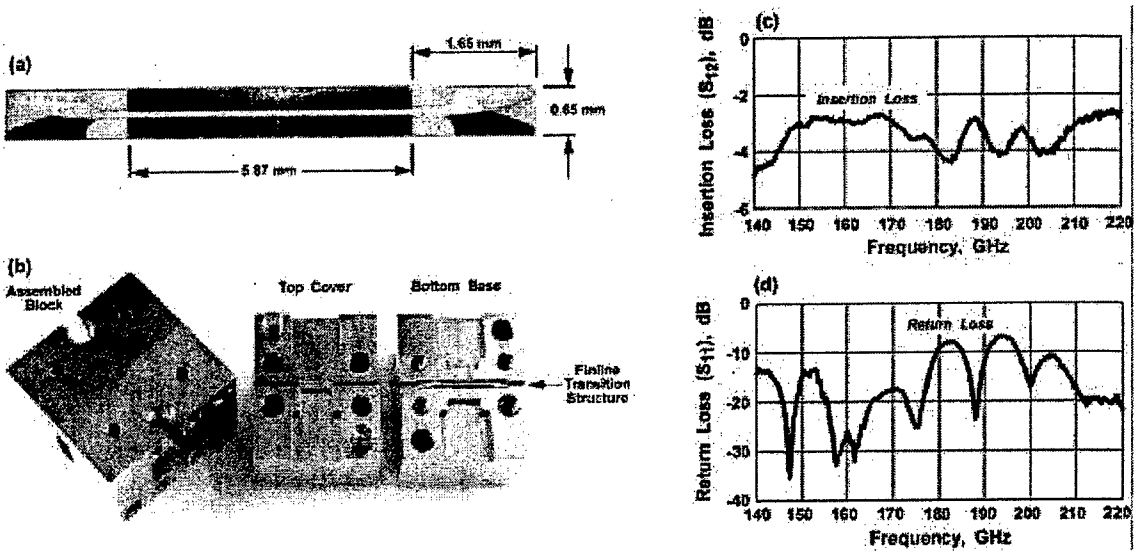


Figure 5. Photographs of (a) back-to-back G-band finline transitions, and (b) same structure mounted in waveguide block, along with measured (c) insertion loss and (d) return loss.

Measurements at G-band were performed using the HP 8510C VNA and the Oleson extender heads mentioned previously. Figures 5(c) and 5(d) show measured results for the insertion loss and return loss, respectively, for the test circuit described above. From about 150 GHz to 170 GHz the insertion loss is less than 3 dB, while the return loss is better than -12 dB across this band. From an independent calculation (Agilent's ADS; multilayer TLines) the loss of the 5.9 mm-long microstrip line alone is about 0.5 dB. Therefore, the loss per transition is estimated to be no worse than 1.3 dB. Note that at 220 GHz the return loss is -20 dB and the insertion loss is likewise less than 3dB. Consequently, there is potential for full band operation with insertion loss per transition of less than 1.3 dB. Work is currently underway to improve the performance of the transition to cover a wider band, and to insert a G-band MMIC amplifier in place of the microstrip line.

Finally, the relative merits of each transition approach are summarized in Table I, with some additional clarification presented in this paragraph. Both transitions have the potential for covering full waveguide bands with good return loss performance (subject to the usual gain-bandwidth tradeoff). For the E-plane probe the backshort and its precise location with respect to the probe is critical for optimized electrical performance. The width of the 50 Ω line on alumina is more compatible for interfacing with typical MMICs than the wider 50 Ω line on CuFlon®. Generally, the finline circuit is more tolerant of small misalignments within the waveguide and is directly compatible with an in-line port-to-port configuration. Although both types of transitions require double-sided processing, the front-to-back alignment is more critical in the finline transition. We note that both types of transitions could be fabricated either in a thin film process (e.g. gold on alumina) or a laminate process (e.g., copper on Teflon®), but there are limitations. Thin film

processes usually require a hard, brittle substrate which is mechanically problematic for the finlines as the fins must be clamped by the waveguide block. On the other hand, laminate processes typically cannot allow such fine features or dimensional tolerances as thin film processes. In addition, for long term reliability and ease of wirebonding, gold plating of the copper traces (which is not trivial) is required.

Table I. Comparison of Waveguide Transition Approaches for >100 GHz Operation

Characteristics	E-Plane Probe	Antipodal Finline
Insertion loss per transition	~1.1 dB @ 165 GHz on alumina	<1.3 dB @ 165 GHz on Teflon®
Bandwidth	Full waveguide band possible	Full waveguide band possible
Orientation w.r.t. waveguide	90°	In-line
Unique circuit requirements	Backshort optimization; 90° bend in waveguide	Fin grounding at waveguide broad walls;
Width of 50 Ω microstrip	1.9-mils on 2-mil alumina	5.9-mils on 2-mil CuFlon®
Sensitivity to alignment within waveguide	High	Less than for E-plane probe

V. Conclusions

Our wirebond test results indicate that excellent electrical performance is possible using CPWG wirebond interfaces above 100 GHz provided that extra care is taken to minimize bond length and faithfully reproduce the CPW trace geometry with the bonds. The motherboard/daughterboard packaging approach exploits this minimum length low loss wirebond interface to facilitate evaluation and characterization of a complex chain of MMICs. The design presented here is perhaps most applicable for development and prototyping, as well as preparation of MMIC sub-assemblies for system insertion. Finally, the performance of E-plane probe and antipodal finline transitions for use in G-band waveguide split block packages have been shown to exhibit reasonable electrical characteristics. It has been shown that the van Heuven transition fabricated on CuFlon® is a viable approach for incorporation in a split-block waveguide package applicable for G-band operation. We anticipate that further scaling of all of these approaches to higher frequencies is possible (at least through the 220-325 GHz Y-band), though many predominantly mechanical difficulties related to thinner substrates, finer trace geometries, and tighter alignment tolerances may ultimately force less conventional approaches to be used, such as the membrane methods used with THz frequency mixers [1].

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Acknowledgements

The Mayo portion of this effort was supported by DARPA/MTO under the auspices of the Terahertz Technology Program under Dr. Edgar Martinez, through Contract N66001-99-CC-8605 from SPAWAR Systems Center San Diego. The portion of the research described in this paper carried out by the Jet Propulsion Laboratory, California Institute of Technology, was supported under a contract with the National Aeronautics and Space Administration. HRL Laboratories contributions to this work were supported by DARPA / AFRL under Contract No. F33615-99-C-1512. The authors would like to thank T. A. Funk, D. K. Jensen, E. M. Doherty, and S. J. Richardson for manuscript and artwork preparation, and W. Fjerstad for mechanical design work.

The Heterogeneous Integration of InAlAs/InGaAs Heterojunction Diodes on GaAs: Impact of Wafer Bonding on Structural and Electrical Characteristics

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Abstract

We have investigated the influence of low temperature wafer bonding on the electrical and structural characteristics of InAlAs/InGaAs n-p heterojunction structures with similar structure to an emitter-base junction of InAlAs/InGaAs HBTs. Those n-p junction heterostructures were grown on an InP (100) substrate by solid source MBE. The effect of the wafer bonding process on the structural properties of the epitaxial layers was studied by comparing triple crystal x-ray diffraction measurements and simulations before and after bonding. In addition, the influence of the bonding process on the electrical properties of the heterojunction structures was assessed through SIMS analysis of both the bonded and non-bonded samples and an analysis of the I-V characteristics of diodes fabricated on both the bonded and non-bonded sample. These analyses show that the structural and electrical properties of the as-grown epitaxial layers were negligibly changed by the low temperature wafer transfer process.

I. Introduction

The need for improved speed and density in high performance multifunctional electronics has motivated extensive research into the transfer and bonding of electronic and optoelectronic devices to host substrates, including silicon [1]-[3]. Wafer bonding is recognized as a key process technology for the integration of Si and III-V compound semiconductor materials and devices onto various insulating integration platforms for advanced RF applications.

Prior to development of a wafer bonding process for InAlAs/InGaAs HBTs with conventional Si CMOS circuitry, it is necessary to investigate any possible degradation deriving from the low temperature bonding process utilizing a simplified test structure, such as the emitter-base junction of the HBT.

During the wafer bonding process, there are various possible negative consequences such as any change of composition and strain of the epitaxial layers, wafer bowing, Be diffusion at

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the p-n junction, oxygen penetration from the bonding interface into the device's active region, and any change in the trap density in critical regions, and so on. In this paper, the composition and strain of each layer after bonding was determined by assessing the mean values and uncertainty from absolute high-resolution x-ray diffraction (HRXD) measurements of the $\theta_{B\ 004}$ and $\theta_{B\ 224}$ peaks. X-ray peak broadening of the bonded sample was determined using triple crystal analysis: (i) distribution in lattice constant ($\theta/2\theta$ scans with the analyzer crystal in place) and (ii) "mosaic spread" corresponding to misorientaion (ω scans with the analyzer crystal in place).

Furthermore, we have studied the effect of the bonding process on material and device properties through comparisons of DC characteristics of diodes fabricated on both bonded and non-bonded structures, including SIMS profiling, and DLTS measurement after wire bonding.

II. Experiments

Lattice matched InAlAs/InGaAs n-p junction heterostructures were grown on 2- inch epi-ready InP (100) semi-insulating substrates in a solid source Riber 2300 molecular beam epitaxy (MBE) system equipped with an arsenic valved-cracker source (EPI RB500V). Figure 1 shows the schematic structures of the samples used for this study. The epitaxial layer structure is similar to the emitter-base junction of the conventional InAlAs/InGaAs heterojunction bipolar transistors in order to investigate the influence of wafer bonding process on the structural and electrical properties of emitter-base junction. Two samples (R84 and R87) were grown at a temperature of 420°C with a V/III BEP ratio of 50 and growth rate of 1 μm/hour.

Cap	InGaAs:Si	2E19	75 nm
Cap	InAlAs:Si	1E19	45 nm
Emitter	InAlAs:Si	5E17	345 nm
Spacer	InGaAs:Si	5E17	5 nm
Base	InGaAs:Be	3E19	100 nm
	InGaAs:Be	1E19	100 nm
	InGaAs:Be	8E18	100 nm
	InGaAs:Be	6E18	100 nm
	InGaAs:Be	4E18	100 nm
	InP (100) Fe substrate		

Figure 1. Schematic structure of InAlAs/InGaAs n-p heterojunction grown by MBE.

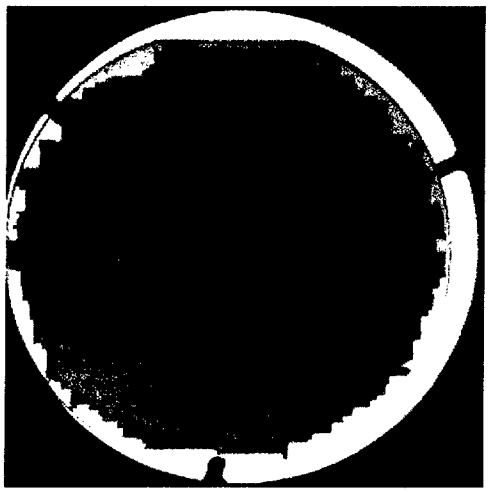


Figure 2. IR image of transferred layer from R87 wafer

The R87 sample was inverted and transferred onto a GaAs (100) substrate using a low temperature wafer bonding process. Surfaces were chemically cleaned by exposure to a O_2 plasma, and then rinsed using megasonically excited DI water and then spun dry. These samples were then joined at room temperature in atmosphere by touching the center of the wafers first to allow the bond front to propagate to the edge of the wafer. Finally the top substrate was selectively removed by submersion in 3:1 HCl:DI water for about 1.5 hours. The infrared transmission image (Figure 2) after bonding showed good uniformity of bonding across the wafer.

The compositional uniformity of the 2-inch as-grown samples was measured with a Bede QC1 x-ray diffractometer. The measured double crystal rocking curve results show that there is a good lattice matched peak in the center area (of diameter 1 cm), and a maximum variance of 1.6% at the edge. This results from the thermal non-uniformity of the substrate heater and cell configuration of the group-III elements in our MBE system. To assess the strain and wafer bowing generated by wafer bonding process, HRXD measurements before and after bonding were performed and compared with x-ray simulation results. We also investigated the extent of Be diffusion during growth and/or bonding, as well as the oxygen penetration from the bonding interface into the sample, through SIMS analysis of the bonded (R87) and non-bonded sample (R84).

Diodes were fabricated on the bonded wafers and non-bonded control wafer in the same batch using a large area mesa HBT design and wet etching. The detailed fabrication process is explained elsewhere [4]. Figure 3 shows the schematic structures of the diodes fabricated on the non-bonded and bonded sample. As shown in this figure, the top InGaAs base layer of 400 nm in the bonded sample was etched before diode fabrication to obtain the same contact resistance with the base of non-bonded sample. The emitter sizes are 200 μm x 200 μm, 100 μm x 100 μm, and 50 μm x 50 μm. To assess any degradation during bonding process, I-V characteristics of both diodes were analyzed and compared with various parameters including breakdown voltage, leakage current at reverse bias of 0.5 V, turn-on voltage, ideality factor, and series resistance. We measured the characteristics of ten diodes at each size to reduce measurement error.

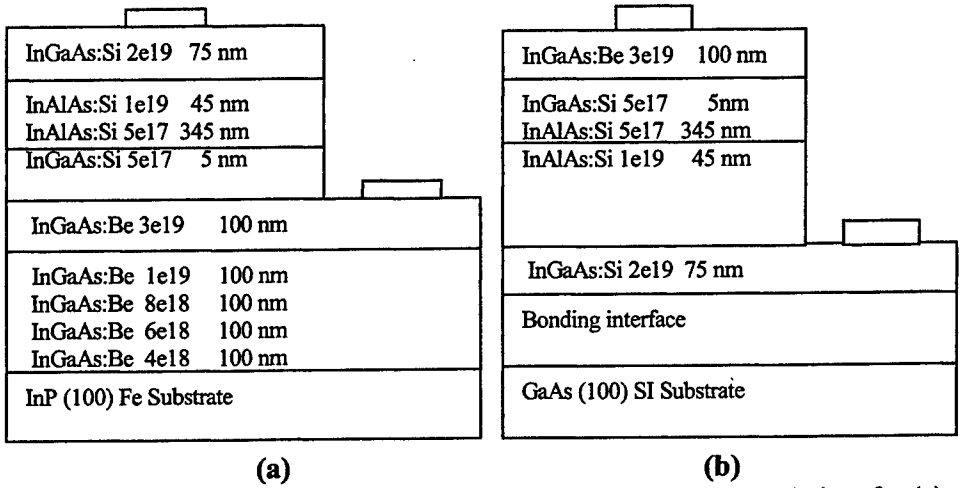


Figure 3. Schematic structure of diodes fabricated on the non-bonded wafer (a) and bonded wafer (b).

III. Results and Discussion

HRXD measurements and analysis were carried out before and after transfer of R87 sample to assess the strain and wafer bowing potentially produced by bonding process. Figure 4 shows the comparison of triple crystal x-ray diffraction (TCD) data measured on as-grown sample before transfer and results simulated with a three-layer model: 505 nm pseudomorphic InGaAs (52.93% In), 390 nm 50% pseudomorphic InAlAs (53% In), and 75 nm pseudomorphic InGaAs (52.93% In). This three-layer model, based on the above parameters, is plotted along with the x-ray analysis of emitter and base layer before wafer transfer, using the compositions based on the absolute measurements of $\theta_{B\ 004}$ and $\theta_{B\ 224}$ ± 10" peak positions for the component layers. Values for In composition and vertical strain ($\varepsilon_\perp$) in the calculation are within experimental uncertainty of those measured after layers were transferred despite the lack of a detailed fit.

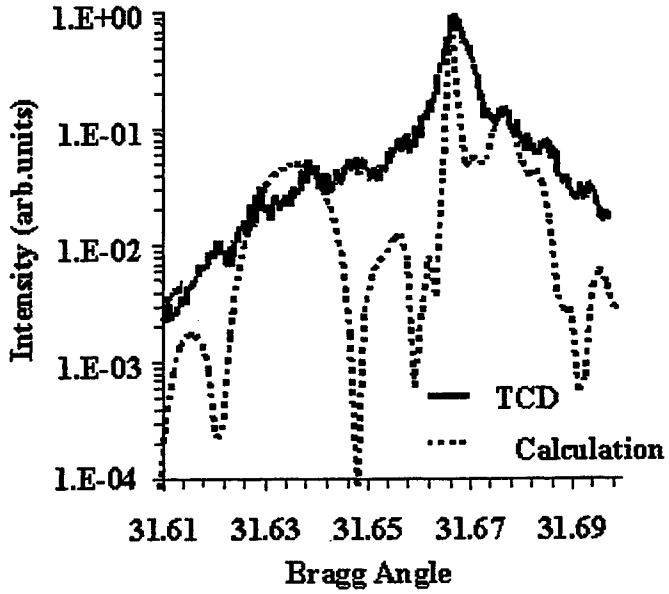


Figure 4. Triple crystal x-ray diffraction data measured on R87 sample before transfer and simulation data with three-layer model.

Peak widths of R87 sample after wafer bonding were investigated by triple crystal x-ray diffraction analysis. θ/2θ peak widths indicate a variation in the lattice parameter such as In composition and/or strain through the measured volume. The ω-peak width indicates a distribution of regions whose lattice–plane normal varies about the average pole position. The θ_{004} scans allow the distribution in the lattice parameter parallel to the surface normal, $a_\parallel$, to be determined from the θ/2θ peak width and the spread of lattice plane orientations about the surface normal from the ω-peak width. The θ_{224} peak is an asymmetric reflection which allows information to be obtained that has contribution from both the lattice constant and orientation in the plane and out of the plane of the substrate, i.e. both $a_\perp$ and $a_\parallel$.

The InGaAs layer of bonded R87 had θ_{004} peak widths of 37" FWHM in $\theta/2\theta$ scan and 50" in ω scan. The InAlAs layer of bonded R87 had θ_{004} peak widths of 74" FWHM in the $\theta/2\theta$ scan and 50" in ω-scan. Figure 5 shows the triple crystal x-ray diffraction data measured on the bonded R87 sample and simulation curve obtained with the same three-layer model used in Figure 4. As seen in Figure 5, the measured TCD θ_{004} data show well defined peaks. However, those peaks are not well described by the three-layer model discussed above. Satellite peaks of base layer are too intense to be thickness of Pendelossung fringes. In addition, the ratio of peak intensities of the emitter to the base regions suggests that base layer, using an average lattice constant, is much thinner than 505 nm. These features of the data suggest that the five different 100 nm layers that form the base layer may have slightly different, but well-defined lattice constants. In Figure 6, the TCD data was compared with the simulation data obtained with assumption that base comprised of three layers with slightly different lattice constants. This comparison shows a better fit between measurement data and simulation data. The Be doping was increased in steps to avoid surface degradation associated with high Be concentrations. It is possible that the changes in the Be cell temperature and/or incorporated concentrations during the growth of the base region could alter the In-composition and/or modify the lattice constant within each Be-doped InGaAs layer. In spite of the possible variations in the individual InGaAs:Be layers, the epitaxial structure transferred onto GaAs wafer has $\theta/2\theta$ widths limited by the thin, finite thickness of the region and not variation in lattice parameter. In addition, the small ω-width indicates very little mosaic spread of lattice planes due to transfer.

SIMS analysis of both the bonded sample (R87) and non-bonded sample (R84) were performed in order to investigate the diffusion of Be as well as oxygen penetration by wafer

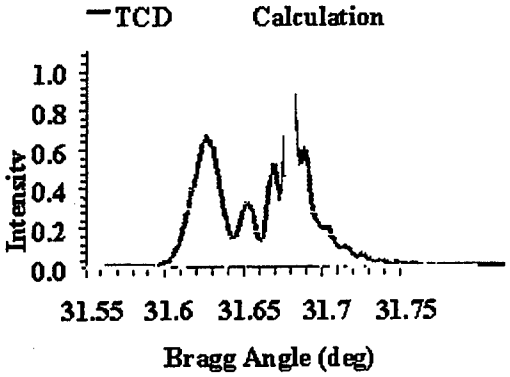


Figure 5. (004) triple crystal x-ray diffraction of bonded R87 compared to three-layer (505 nm base, 390 nm emitter, and 75 nm cap) simulation.

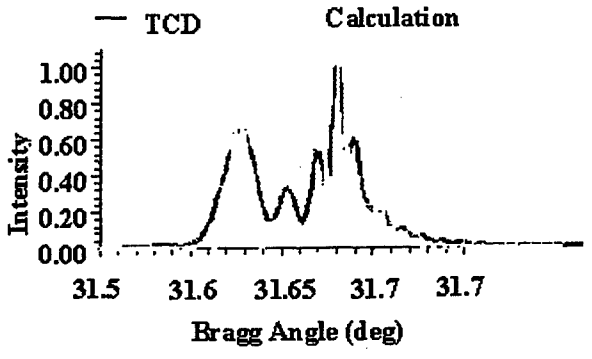


Figure 6. (004) triple crystal x-ray diffraction of bonded R87 compared to five-layer simulation.

bonding process. This analysis was carried out in Charles Evans and Associates. Figure 7 shows SIMS profiles of both bonded and non-bonded sample. As seen in this figure, there is no evidence of Be diffusion at the emitter-base interface in both samples. Be profiles of InGaAs base region clearly show five different Be doping profiles intentionally inserted in both samples. In SIMS profiles of the bonded sample, there is no evidence of oxygen penetration into the emitter-base interface from the bonding interface although there is large peak of oxygen in the bonding interface. The oxygen peak of InAlAs emitter layer was larger than that of InGaAs base. This is due to the larger affinity of Al with oxygen during the growth.

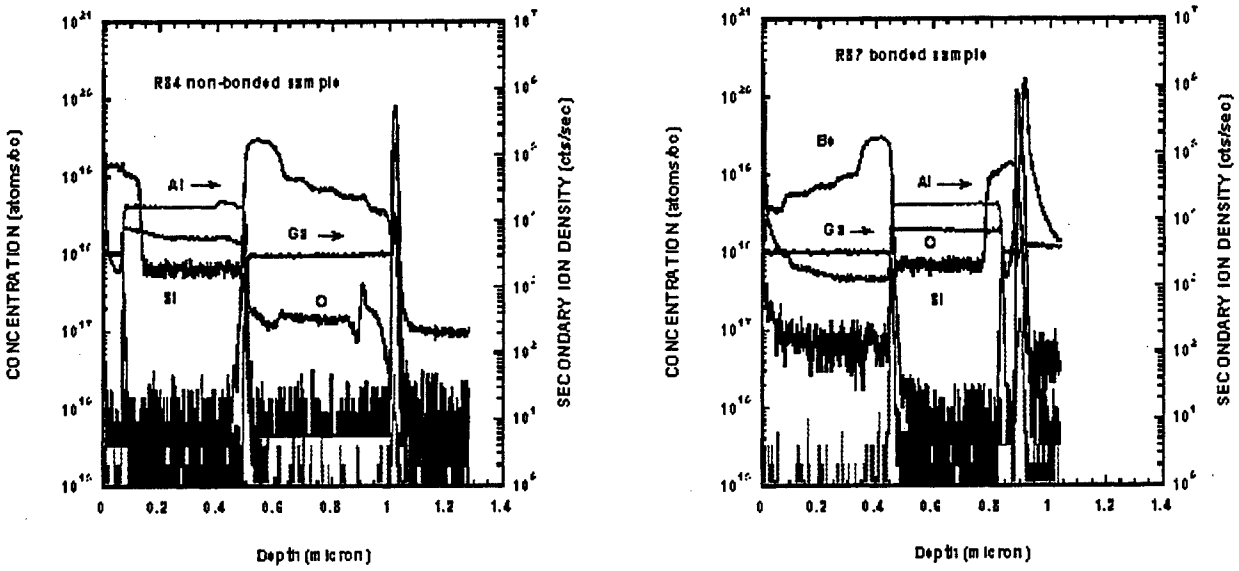
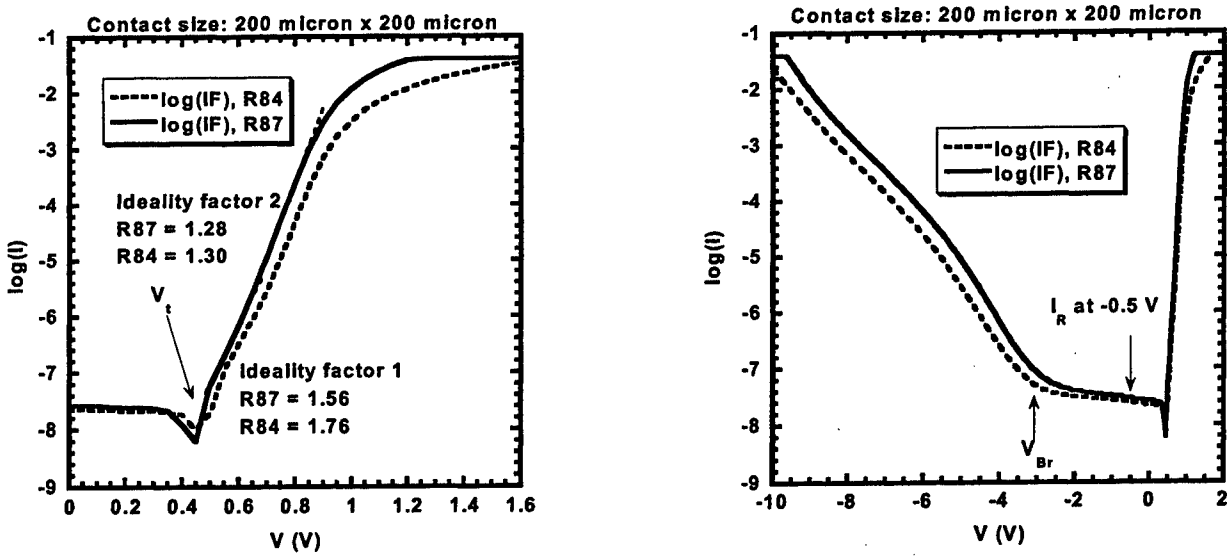


Figure 7. SIMS profiles of non-bonded sample (a) and bonded sample (b).

The influence of the wafer bonding process on the electrical properties was investigated through the comparison of I-V characteristics of diodes fabricated on both bonded and non-bonded sample. Figure 8 shows the semi-log plot of I-V characteristics of diodes fabricated with the contact size of 200 μm x 200 μm on bonded and non-bonded samples. In diodes with the contact size of 200 μm x 200 μm, 100 μm x 100 μm, and 50 μm x 50 μm, five parameters of break down voltage, leakage current, turn-on voltage, ideality factor, and series resistance were investigated. Table 1 shows the summary of I-V characteristics of the diodes. In a highly doped (>5 x 10^{17} cm^{-3}) n-p junction, the tunneling mechanism of breakdown is dominant at the bias value of less than 4 E_g/q of energy band gap in n-p junction and avalanche mechanism is dominant at bias values of larger than 6 E_g/q [5]. By these simple criteria, the breakdown voltage is limited by the tunneling mechanism of InGaAs n-p junction (< about 3 V) without Be diffusion. If Be diffuses into the emitter, the breakdown voltage will increase. As seen in Table 1, breakdown voltages of both samples with the same contact size are similar each other and have values of 3.0 V to 3.38 V.

Table 1. I-V characteristics of diodes fabricated on bonded and non-bonded wafer.

Sample	Contact Size (μm^2)	Ideality Factor η	Turn-on Voltage (V)	Reverse Current at -0.5 V (nA)	Series Resistance (ohm)	Break down Voltage (V)
R84 (Non-bonded)	200x200	1.30	0.50	25	16.5	3.13
	100x100	1.29	0.50	12	30.0	3.25
	50x50	1.25	0.55	6	50.0	3.38
R87 (Bonded)	200x200	1.28	0.48	31	6.5	3.00
	100x100	1.26	0.48	16	9.0	3.25
	50x50	1.28	0.53	10	13.0	3.25



a) b)

Figure 8. log (I) vs. V characteristics diodes fabricated on both bonded (R87) and non-bonded sample (R87): a) forward bias and b) forward and reverse bias region.

The reverse current at biases less than breakdown voltage depends on the recombination current in the depletion region and the surface current. The reverse current measured at a

reverse bias of 0.5 V ranges from 6 nA to 31 nA over the range samples studied. Given that the diodes were not passivated, those values indicate that both diodes are of good quality. However, the reverse current was slightly higher (24% to 66% with different contact sizes) in diodes of the bonded sample than in diodes of non-bonded sample. DLTS was used to investigate the effects of wafer-bonding process on the change of trap concentrations or levels in the junction. No measurable trap concentrations were found in either diodes of bonded or non-bonded samples.

The ideality factor depends on the recombination current in the depletion regions at both the junction and the surface under a forward bias close to the turn-on voltage, and on the diffusion current with the increase of bias. The measured ideality factors of diodes with the same size contact size in both bonded and non-bonded samples were similar, with values of 1.25 tol.30. The turn-on voltage (or threshold voltage of diode) provides important information on the n-p junction interface such as the conduction band discontinuity and Be diffusion. As seen in Table1, the measured turn-on voltages have similar values with the same contact size. From SIMS analysis and investigation of the turn-on voltage, Be diffusion in the junction interface is negligible for both bonded and non-bonded samples.

The diode series resistance results from the voltage drop across the neutral region at high forward bias. As seen in Table 1, there is clear difference between R84 diodes and R87 diodes for all contact sizes. This results from the geometrical difference between the diodes as shown in Figure 3. In particular, the difference in the resistances between the junction and the base contact in R84, and between the junction and the emitter contact in R87 is the main origin of this effect. The R87 diodes have lower series resistance in comparison to the R84 diodes because the R87 diode structure has a smaller neutral region in the base.

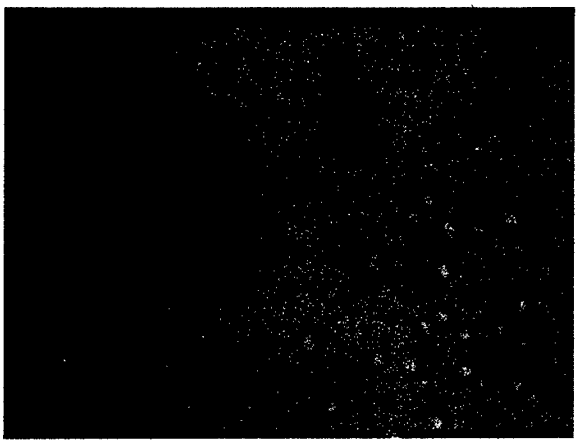


Figure 9. Surface morphology of bonded sample (R87) after 1 min annealing at temperatures greater than 350 °C in an N_2 ambient.

To test the integrity of the samples under thermal cycling, both bonded and non-bonded wafer pieces were annealed in an N_2 ambient while covered with a GaAs wafer during heating. Degradation of the surface morphology, such as the development of blisters (Figure 9), appeared for annealing temperatures greater than 350°C. The development of blisters results from the desorption of residual moisture at the bonded interface.

IV. Summary

We have investigated the viability of a low temperature wafer bonding process for the bonding of InP-based devices onto GaAs or other templates. A low temperature bonded sample exhibited very little broadening of peaks due to structural degradation upon layer transfer. If it is reasonable to expect a difference of 0.4% In over 1 cm of wafer surface, the bonded samples show no evidence of change in strain upon layer transfer. For bonded and non-bonded diodes with the same size, all DC characteristics with the exception of the leakage current are within a difference of ~4%. The low temperature wafer bonding process shows great promise for heterogeneous integration. The low temperature bonding process of InAlAs/InGaAs HBT structure and integration of InP-based HBT on the conventional Si CMOS circuitry is under development.

Acknowledgement

We would like to acknowledge DARPA and the state of Georgia (Yamacraw) for the support of this work.

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Silicon Tunnel Diodes Formed by Proximity Rapid Thermal Diffusion

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Abstract

We demonstrate the first silicon tunnel diodes formed using proximity rapid thermal diffusion and spin-on diffusants. Room temperature peak-to-valley current ratio (PVR) of 2 is obtained at approximately 100 A/cm^2 peak current density. Secondary ion mass spectroscopy is used to compare proximity rapid thermal diffusion with rapid thermal diffusion from spin-coated diffusants in direct contact with a device wafer. The proximity rapid thermal diffusion approach provides a cleaner wafer surface for subsequent processing and yields tunnel diodes with good local uniformity.

I. Introduction

The performance of digital circuitry has grown exponentially for years taking benefit from the continuous decrease of minimum feature size. The further reduction in scale is expected to saturate. Tunnel diodes (TDs), with negative-differential resistance (NDR) and multi-valued current-voltage (I-V) characteristics, can add circuit design options and reduce component count in a CMOS circuit process, often with a reduction in power dissipation and area [1].

Early Si TD technology suffered from being fundamentally discrete [2], but the possibility of integrating TDs with CMOS and HBT technology has rekindled interest. Molecular beam epitaxy (MBE) has demonstrated both Si [3,4] and SiGe [5-8] tunnel diodes, but the incorporation of TDs with CMOS technology awaits the development of a production compatible fabrication process. In this paper, we demonstrate for the first time that Esaki Si TD can be produced using conventional rapid thermal processing tools and spin-on dopants (SODs) sources.

II. Simulations and Fabrication Procedure

The vertical p^+n^+ tunnel diode device structure and energy band diagram are shown in Figure 1. Phosphorus-doped, 1.5 mΩ cm, 100 mm, (100) silicon device wafers were cleaned and hydrogen terminated in buffered HF in preparation for rapid thermal diffusion. Source wafers, in this case n-type, 18 Ω cm Si source wafers, were similarly cleaned and spin coated with Emulsitone phosphorosilicafilm 1×10^{21}, a diffusion source incorporating phosphorus at

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a concentration of 1 x 10^{21} cm^{-3}. To remove the volatile organics in the spin-on film, the source wafers were baked for 20 minutes at 200 °C in air immediately prior to loading into a Modular Process Technology RTP600 rapid thermal processor (RTP). Three cleaned quartz spacers (thickness 0.46-0.48 mm) were placed symmetrically on the source wafer at the wafer edge. The device wafer was placed on top of the quartz spacers, facing the spin-coated source wafer. With this arrangement, on heating, the dopants transport across the short space from the source wafer to the device wafer in a nitrogen (2 slpm flow rate) ambient, a process called proximity rapid thermal diffusion [9]. In the Modular Pro reactor, the tungsten halogen lamps simultaneously illuminate the wafer from both sides. Temperature was measured by a thermocouple in contact with the backside of the source wafer.

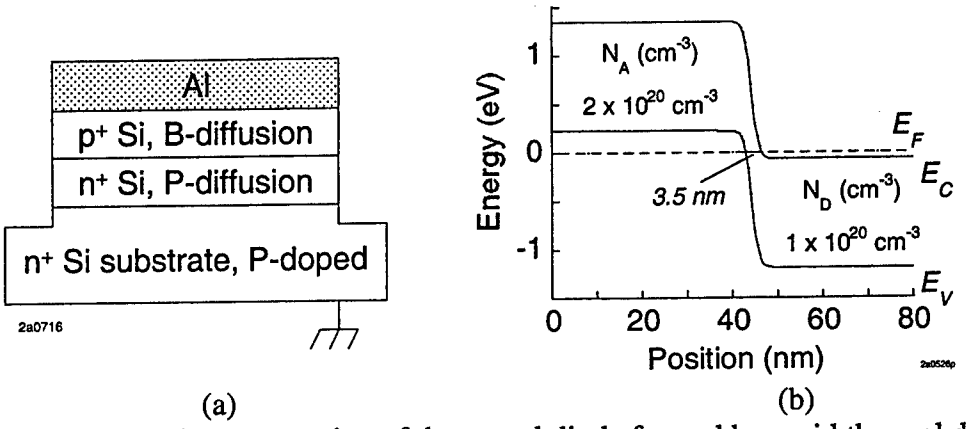


Figure 1. (a) Schematic cross section of the tunnel diode formed by rapid thermal diffusion. (b) Computed energy band diagram for an abrupt p^+n^+ Si tunnel diode (BandProf, W. R. Frensley Poisson solver).

For diffusion of phosphorus a heating rate of 30 °C/s was used with an anneal of 900 °C for 1 s. The source wafer was then removed and the device wafer was annealed again at 900 °C for 90 s to lower the phosphorus surface concentration. The wafer was next cleaned in buffered HF prior to loading for the boron rapid thermal diffusion. Emulsitone Borofilm100 was used as the spin-on source in the same way as the phosphorus source. A single anneal of 900 °C for 1 s using 30 °C /s heating rate was used. The cooling rate in the Modular Pro RTP is approximately 30 °C/s for the first 400 °C, after which the cooling takes less than approximately 90 s to return to 200 °C. Buffered HF was used again to remove the residual spin-on diffusant. Aluminum was applied by blanket electron beam evaporation, then lithography and wet chemical etching in Cyantec Al-12 (HNO_3, HPO_3) were used to define the device contacts. Reactive ion etching in SF_6, 26 sccm, 30 mTorr, 200 W was used to form the device mesa, approximately 700 nm in depth, using aluminum as the etch mask.

A process simulation of the phosphorus and boron diffusion profiles using Silvaco's Suprem3 is shown in Figure 2. We utilized the transient-enhanced diffusion model with the model parameters shown. These model parameters were obtained from curve-fitting to secondary ion mass spectroscopy (SIMS) measurements of boron diffusions from

Emulsitone's 5257 diffusion source utilizing ramp rates between 60 and 75 °C/s. By lowering the ramp rate to 30 °C/s, the transient-enhanced diffusion is significantly suppressed. From Figure 2, a boron profile with an abruptness of 4 nm/decade at a junction depth of approximately 5 nm is expected. For carrier densities exceeding 10^{20} cm^{-3}, a zero bias depletion width of approximately 3.5 nm is expected as shown in Figure 1(b).

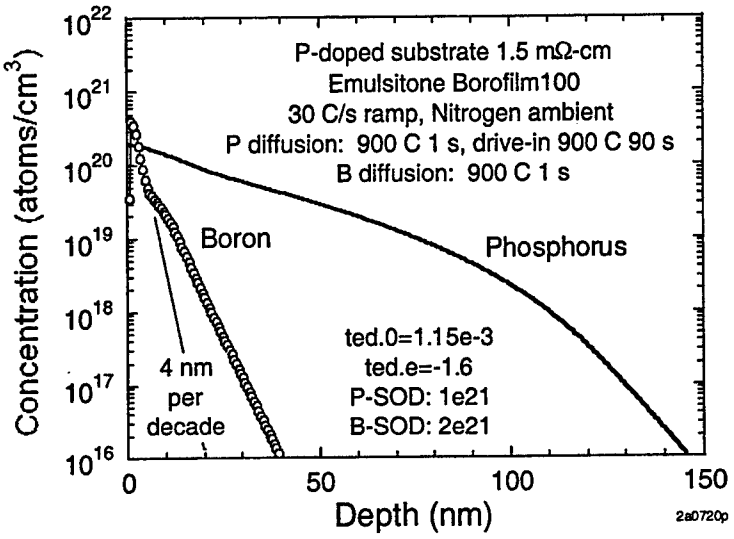


Figure 2. Simulated (Silvaco Suprem3) diffusion profiles for boron and phosphorus to form a p^+n^+ tunnel junction.

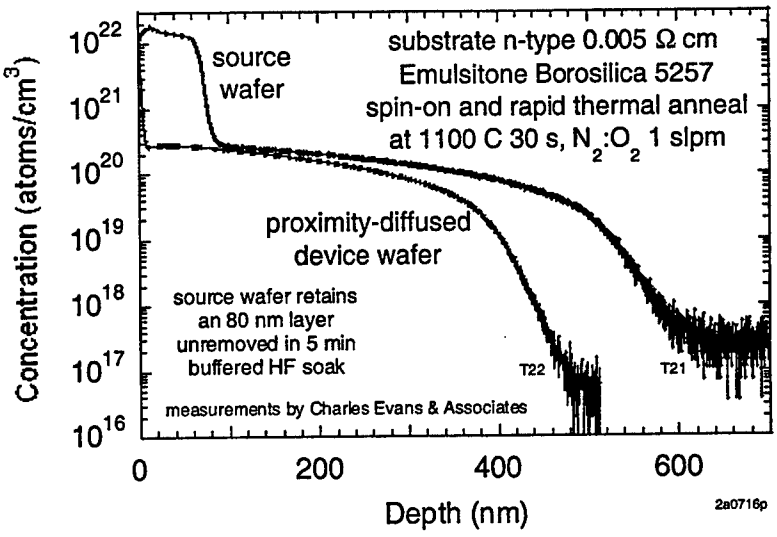


Figure 3. Secondary ion mass spectroscopy measurements of boron diffusion into silicon comparing the profile obtained from a source wafer in direct contact with the spin-on diffusant with the profile resulting from proximity diffusion from the source wafer.

In contrast with rapid thermal diffusion of the spin-on diffusant in direct contact with the wafer, the clean-up process is significantly improved using proximity rapid thermal processing and the doping efficiency is not significantly impeded. Shown in Figure 3 are SIMS measurements of the concentration profiles obtained in the case of boron diffusion where both source and proximity-diffused wafers from the same anneal were analyzed. Both wafers were cleaned in buffered HF to remove the spin-on diffusant prior to the SIMS analysis. A significant insulating residue with high boron content, approximately 80 nm thick remains on the source wafer while in the proximity-diffused wafer the residue thickness is less than approximately 5 nm.

III. Device Results and Discussion

We observe that without an initial diffusion of *P* into the 1.5 mΩ-cm, n^+ substrates, backward tunnel diodes are formed as shown in Figure 4. A measure of the rectification property of the backward diode is to consider the ratio of the reverse current at –0.1 V to the forward current at 0.1 V which we term the RFR. A positive RFR is an indication of a backward tunnel diode characteristic while a number less than 1 is an indication of a normal diode characteristic. In Figure 4, 10 diodes are measured across a 100 mm wafer, with an RFR of 9.9 +/– 1.3.

Figure 5 shows measured current voltage characteristics for the proximity rapid-thermal-diffused tunnel diodes. The highest peak current density 112 A/cm^2 as shown in Figure 5(a) and the highest peak-to-valley current ratio (PVR) device is shown in 5(b).

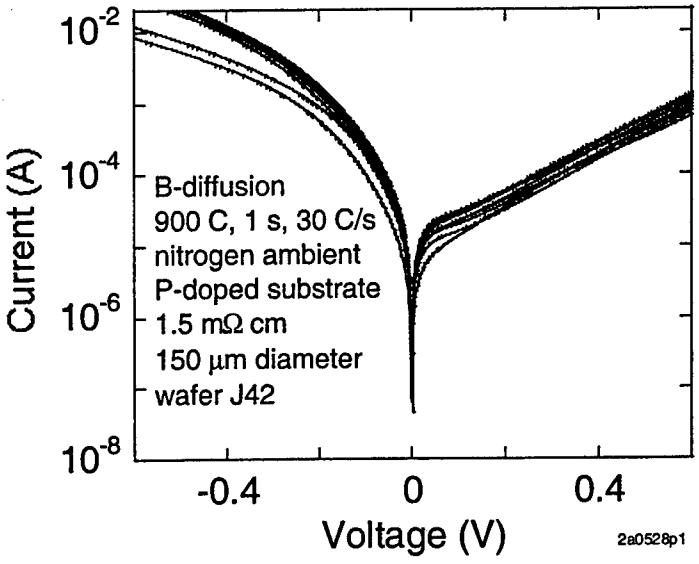


Figure 4. Measured backward tunnel diodes obtained without pre-diffusion of phosphorus.

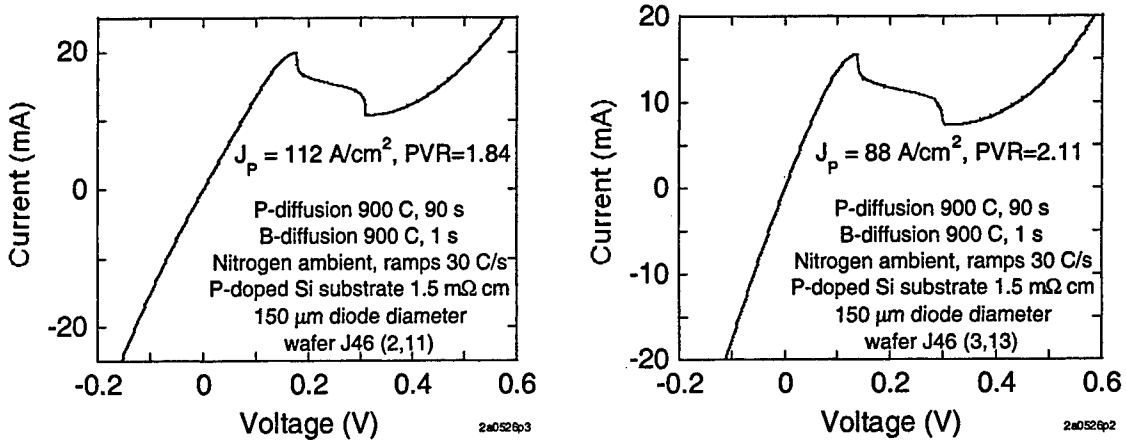


Figure 5. Measured room temperature I-V characteristic showing (a) highest peak current density device and (b) highest peak-to-valley current ratio (PVR) device.

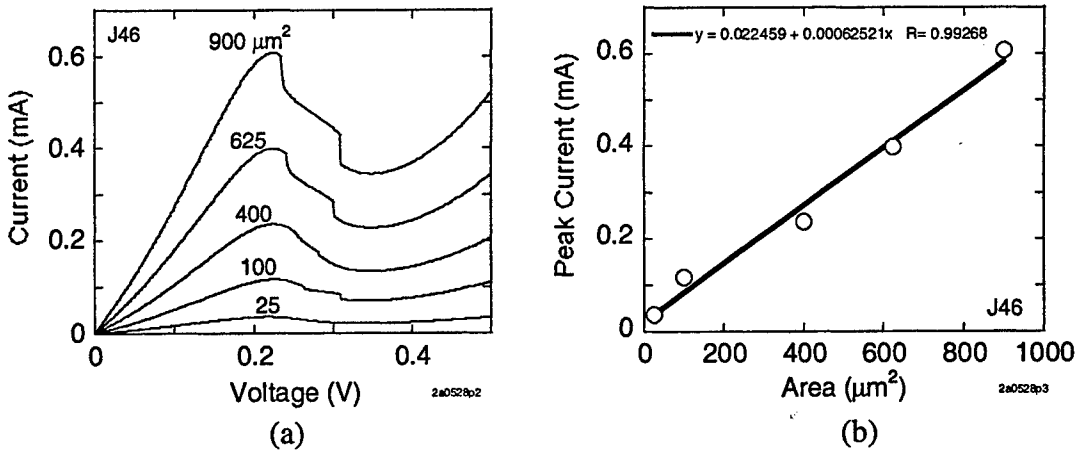


Figure 6. (a) Dependence of current-voltage characteristics of tunnel diodes on (a) device area and (b) dependence of peak current on device area.

Area dependence of the tunnel diode peak current is shown in Figure 6(a). Peak current scales linearly with area indicating no edge leakage effects are present for the device sizes tested.

Temperature dependence of the TD's I-V characteristics was measured on a Cascade 11861 wafer prober with a Temptronic TP03000A thermal chuck system. In Figure 7(a), the different I-V curves of the same device from –60 °C to 160 °C show a monotonic increase in current with temperature. Negative differential resistance is apparent at all measured temperatures through 140 °C. Figure 7(b) plots the temperature dependence for three different bias points: pre-peak (V = 0.15 V), valley (V = 0.4 V), and post-valley (V = 0.6 V).

We find a weak, approximately linear dependence of the current on temperature in the tunneling pre-peak portion of the characteristic, Figure 7(b). In both the valley and post-valley regions, we find that the temperature dependence cannot be fit by any function of the form, $I = \alpha T^{\beta} \exp(-\gamma / kT)$, where α, β, and γ are constants, as might be expected for a diode in forward bias. This is consistent with the findings of Chynoweth, et al. [10] who found in alloy tunnel diodes that this temperature dependence can be explained by a transport model invoking tunneling via energy states in the energy band gap.

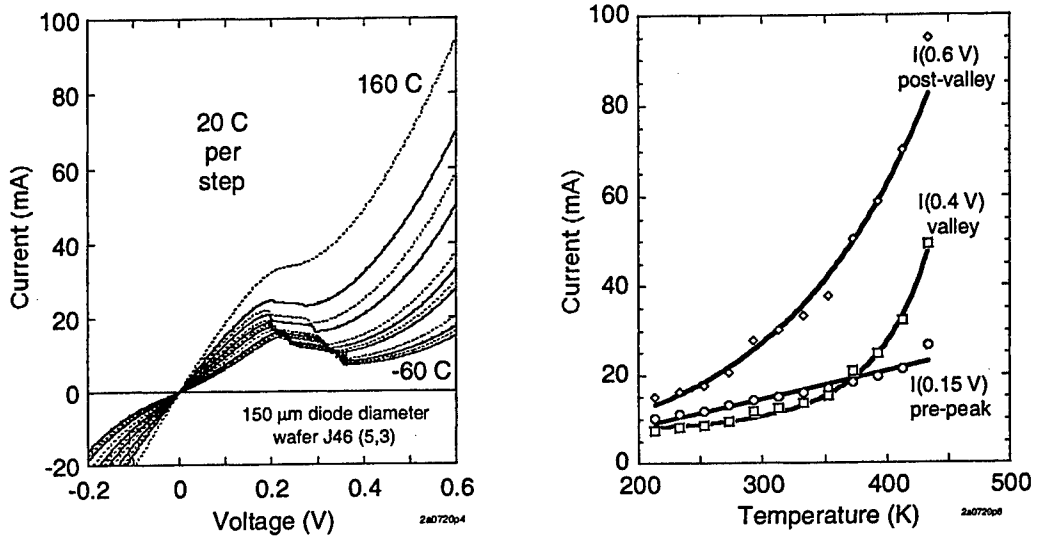


Figure 7. (a) Temperature dependence of the current-voltage characteristics between −60 and 160 °C with a 20 °C step. (b) Dependence of pre-peak tunnel current (V = 0.15 V), valley current (V = 0.4 V), and post-valley current on temperature.

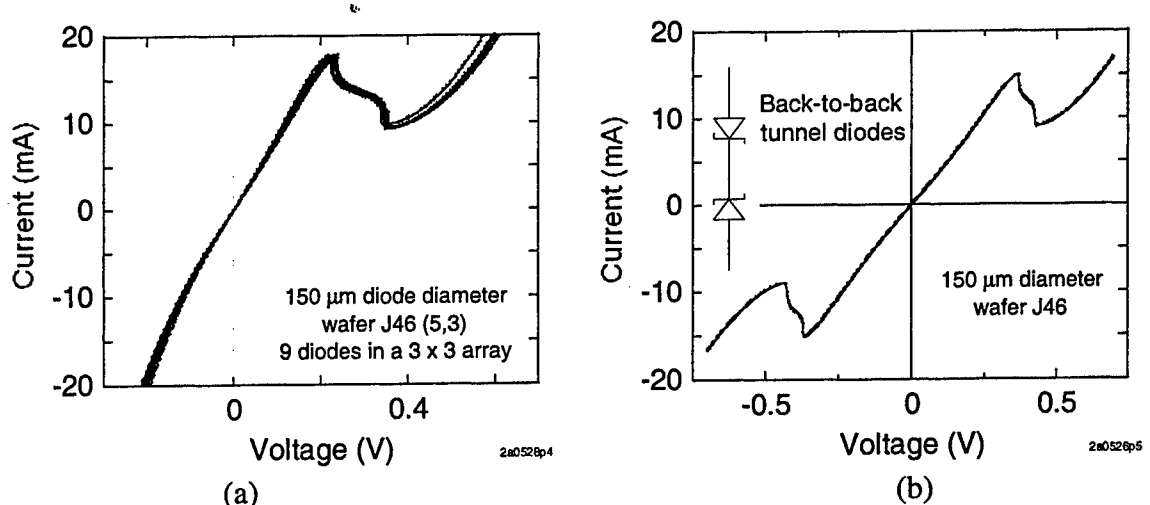


Figure 8. (a) Local uniformity of adjacent tunnel diodes, 9 diodes in 900 × 900 µm^2.
(b) Series connection of two adjacent tunnel diodes to form a symmetric I-V characteristic.

We observe good local uniformity of adjacent tunnel diodes as shown in Figure 8(a). In a 900 × 900 μm^2 area, 3 × 3 device array is investigated with +/-2% deviation in peak current and +/-3% deviation in peak voltage. Two adjacent identical TDs are connected in series and a symmetric current-voltage characteristic is achieved as shown in Figure 8(b).

From the DC I-V characteristics of Figures 5 through 8, we observe a sharp decrease in the peak current after the peak voltage to a plateau region followed by a similar sharp decrease in the current to the valley current minimum. This well-known plateau is an indication of oscillation in the NDR region of the characteristic. By biasing the tunnel diode at 0.275 V while still on the wafer chuck, we observe that this 150 μm diameter TD oscillates at a frequency of 370 kHz. This low frequency is consistent with the 20 mA peak current and large capacitance (120 pF) of the coaxial cabling in this measurement configuration. The intrinsic oscillation frequency of this device is approximately 100 MHz.

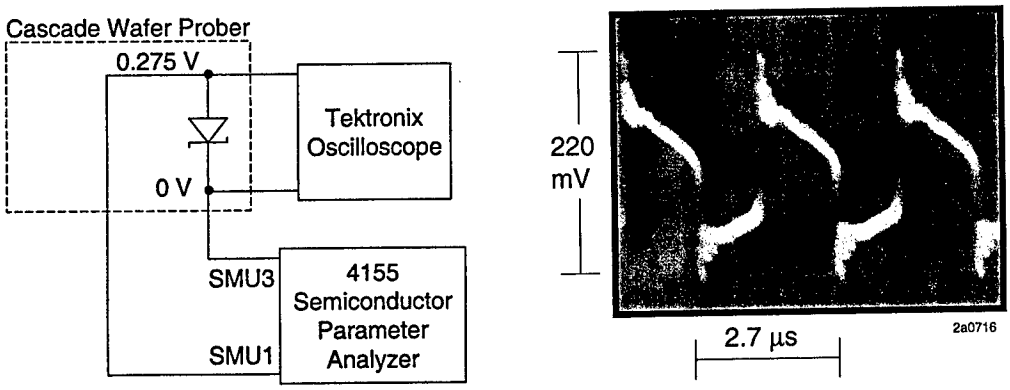


Figure 9. Silicon tunnel diode oscillator on-wafer biased at 0.275 V and exhibiting a characteristic frequency of 370 kHz.

TABLE 1. Technology comparison of tunnel diode peak current density (J_P) and speed index (J_P/C).

Author	Year	Approach	Type	J_P (kA/cm^2)	Speed Index (mV/ps)
Franks, et al. [11]	1965	Alloy	Si	1	1.2
Duschl, et al. [7]	2000	MBE	Si/SiGe	0.52	0.45
Rommel, et al. [5]	2000	MBE	Si/SiGe	22	11.0*
Dashiell, et al. [3]	2000	MBE	Si	47	23.5*
Dashiell, et al. [4]	2002	MBE	Si	16	7.1
This work	2002	RTP	Si	0.1	0.05*

* Computed using a tunnel diode capacitance (C) of 20 fF/μm^2 obtained from simulation of an abrupt tunnel diode with symmetric *n* and *p* doping densities of 10^{20} cm^{-3} using the Poisson solver, BandProf, written by W. R. Frensley.

Since the speed index is the primary factor governing switching speed, we survey prior best results across fabrication approaches in Table 1. The initial results for the proximity-diffused tunnel diodes are not meant to indicate a performance limitation.

V. Conclusions

In this paper we demonstrate the first silicon tunnel diodes formed by proximity rapid thermal diffusion from spin-on dopants. We have characterized the devices by current-voltage-temperature measurements and examined area dependence, uniformity, and ac oscillations in the negative differential resistance region to show unambiguous tunnel diode behavior. The ability to form tunnel diodes in a simple process is a first step toward an integrated tunnel diode/CMOS process.

Acknowledgements

This work is sponsored by the Navy/SPAWAR, DARPA, and the SRC. We would like to thank Brian Doyle from the Intel Corporation for providing SIMS measurements and Lars-Erik Wernersson for useful discussions.

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The Design and Fabrication of Microdisk Resonators for Terahertz Frequency Operation

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Abstract

The design and fabrication of resonators and waveguides operating at THz frequencies are reported. Resonance frequencies, mode confinement, quality factors, and stop-bands were calculated for resonators with and without photonic elements. The estimations show that very narrow modes can exist within the propagation bandgap of a photonic lattice. Microdisk devices were designed and fabricated for high-quality whispering-gallery modes centered around 10 THz. Combined with silicon-germanium quantum wells grown by molecular beam epitaxy, these resonators are promising candidates for silicon-based miniature far-infrared lasers.

Introduction

Strong molecular absorption of terahertz radiation (1-30 THz) due to vibrational and rotational transitions[1] makes THz optical components and devices an attractive choice for chemical and biological sensing and imaging applications[2]. The predicted low absorption coefficient of electromagnetic radiation at 30 THz in air suggests a wide range of free-space communication[3] and military applications, such as ranging[4] and imaging[5]. Outside this atmospheric window, the extremely high absorption coefficient (>10^3 dB/km), makes it suitable for short-range applications. Compared to microwave systems, THz-based devices are expected to be smaller and more compact due to the shorter wavelength. To support new applications in this frequency regime, components such as sources, detectors, and couplers must be designed and optimized. Our sources and detectors are based on intersubband transitions in SiGe quantum wells[6]. The resonators and waveguides are based on structures that incorporate photonic crystal elements for frequency selection and mode control. Microdisk resonators support high azimuthal whispering gallery modes with quality factors near 10^5, and are therefore superb candidates for ultra-low-threshold lasers. To fabricate THz microdisks that can be integrated with quantum wells and photonic crystal elements, we have developed an anisotropic deep reactive ion etching technique that combines sacrificial micromasking layers with cyclical replenishing and removal. This technique has led to the fabrication of unique resonator and waveguide structures that will be described here.

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Theory

Dielectric resonators[7] and waveguides with photonic crystal elements were simulated using the Finite-Difference Time-Domain (FDTD) method. Our mathematical model and numerical method are published elsewhere[8]. Briefly, the structures were meshed in two dimensions, using a perfectly matched layer as the absorbing boundary and a $\lambda/40$ sampling grid, where λ is the center wavelength (30μm or 10 THz). After launching a Gaussian pulse having a 1/e bandwidth spanning the frequency range of interest (here ± 5 THz), the electric and magnetic field components were calculated and stored at a time interval of $\Delta t=\Delta/2c_0$, where c_0 is the velocity of light in free-space and Δ is the sampling grid step size. After N time steps, the computation was ended and field components were Fourier transformed with a frequency resolution of $\Delta f=1/N\Delta t$.

Simulations were performed for a microring structure suspended in air with an inner radius of 70 μm, annulus width of 8 μm, with and without photonic crystals (PC) of varying period and size. As shown in Figure 1(a), the microring permits the propagation of a multitude of frequencies without any PC. The most effective stop-band was achieved using etched holes with a radius of 2.5 μm and period of 7.97 μm. In this configuration, which is displayed in Figure 1(b), the propagation of light with frequencies between 8 and 11.5 THz was forbidden. When every fourth element in the photonic crystal was omitted, a very narrow mode around 9.55 THz within the forbidden gap was allowed, depicted in Figure 1(c). The best transmission properties of this frequency were achieved by adjusting the ring radius and PC period to 70.2 and 8 μm, respectively.

Microdisk resonators supported by a pedestal have been predicted to exhibit quality factors in excess of 5,000[7]. We propose to combine the high-quality factor and mode confinement of microdisks with the propagation selectivity of PCs to select the highest quality modes in microdisk resonators.

Experimental

Optical components, such as waveguides and resonators, often require extremely low surface roughness and high aspect ratios (HAR) to sustain the predicted propagation properties. We have developed and optimized a novel two-part etching process that produces freestanding HAR features in silicon grown by chemical vapor deposition (CVD) on highly doped silicon substrates. The process is schematically shown in Figure 2. Lightly doped layers (approximately 140 Ωcm) were grown by atmospheric-pressure chemical-vapor deposition (APCVD) on p-type $5\cdot10^{18}cm^{-3}$ doped three-inch silicon substrates using dichlorosilane as the precursor and hydrogen as carrier gas. After a short cleaning etch in hydrochloric acid vapor, the layers were deposited at a substrate temperature of 1100 °C. No dislocations were observed using Nomarski-contrast microscopy. The doping concentration was constant throughout the layer and the interface was sufficiently abrupt, as confirmed by spreading resistance measurements on a 1-degree beveled edge.

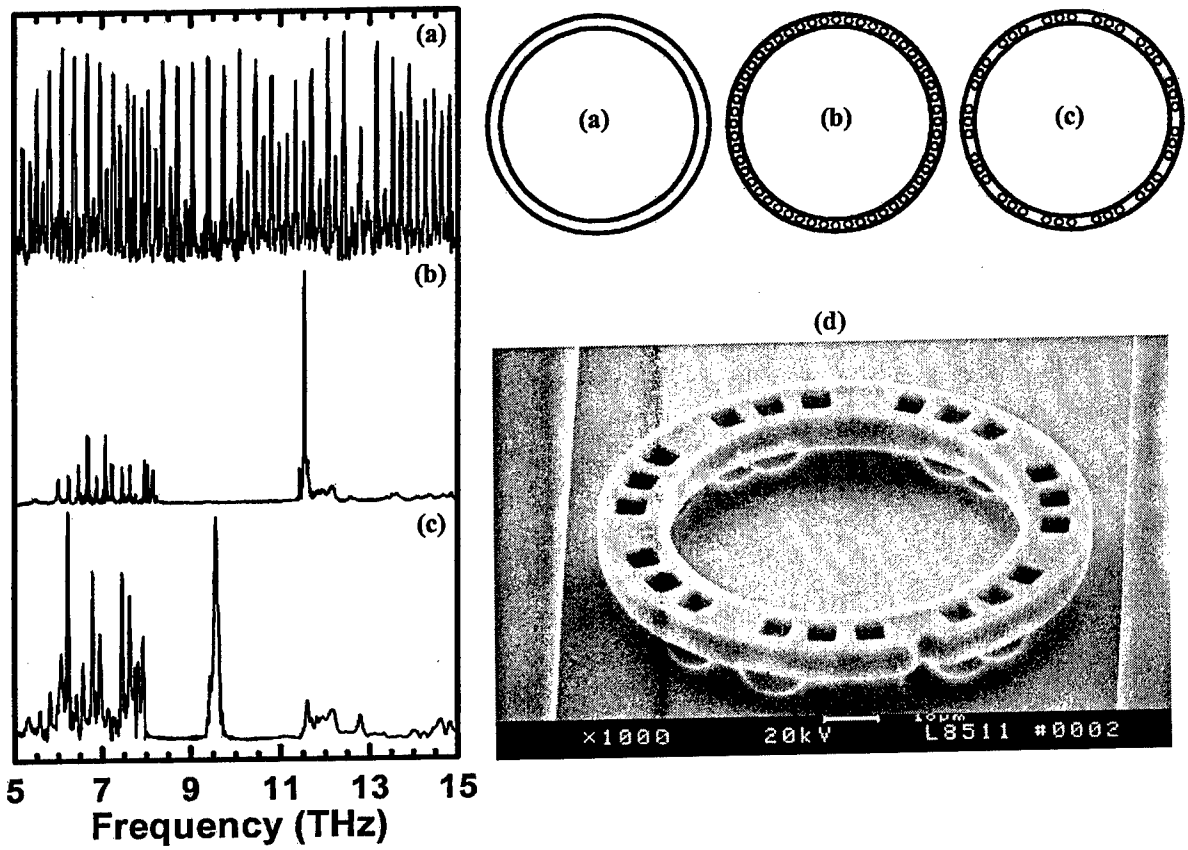


Figure 1: Finite-Difference Time-Domain simulations of microring resonator. The ring has an inner radius of 70 μm, annulus width of 8 μm, PC period of 7.97 μm, and PC radius of 2.5 μm. (a): Ring resonator without photonic crystal structure showing broadband character. (b): Periodic PC etched into the ring, resulting in a stop-band between 8 and 11.5 THz. (c): Periodic placement of defects in PC permitting the propagation of a narrow part at 9.55 THz inside the stop-band. (d): Scanning electron micrograph of fabricated microring structure with PC and periodic defect. Linear waveguides are nearby in order to capture the evanescent tail of the propagating mode.

Vertical Etch

Presently, high-aspect ratio features in silicon are commonly obtained in dry etchers. The silicon etching process with the highest dissolution rates and anisotropies is patented by the Robert-Bosch GmbH[9]. However, this process relies on fast gas and pressure management, helium-flow-cooled substrates, requires inductive plasma enhancement, and in its original configuration does not allow irregularly shaped samples to be processed. We have developed a similar process that operates on conventional parallel plate reactive ion etchers. This process is inherently much slower due to the lack of plasma enhancement by an inductive coil.

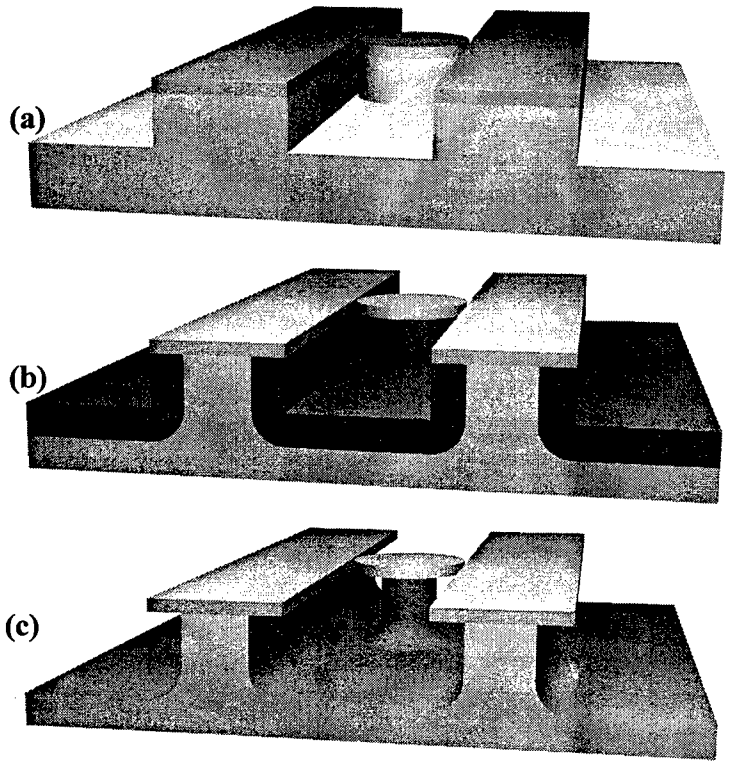


Figure 2: Schematic Birdseye view of the process flow for freestanding all-silicon devices. The microdisks are placed near linear waveguides to capture the evanescent tail of the well-confined optical mode through optical tunneling. (a): Multi-step reactive ion etch producing nearly straight side walls, approximately 10 μm deep. (b): Formation of porous silicon in highly doped areas only. (c): Anodic oxidation and removal of porous silicon.

Consequently, no further substrate cooling is required other than the water-cooled platen. Our system was a Plasmatherm 790 parallel plate etcher having an 8-inch substrate holder. Process gases were introduced through a bank of eight massflow controllers using a shower head distributor. A feedback-controlled flapper-type throttle valve stabilized the pressure. The 13.56 MHz rf-power was coupled to the 8-inch parallel plates with a 7-cm separation. The (typically two-step) Bosch process is incompatible with this configuration, because it does not selectively deposit the protective polymer on the vertical sidewalls of the etched structures, even at the highest rf-powers and lowest gas pressures. In addition, the horizontal coverage could not be removed during the etch part of the cycles without sufficient selectivity to photoresist. We have therefore added a third step to the cyclic process and optimized each one individually.

A schematic overview of this process is depicted in Figure 3. Positive photoresist (AZ5214E[10]) was spun coated and patterned using a contact exposure mask aligner. During the etching step, silicon was isotropically etched in a mixture of SF_6 and He optimized in power, pressure, and gas composition for maximal etch rates and mask selectivities. The lack of inductive coils required a plasma pressure of 200 mT to achieve satisfying etch rates, but

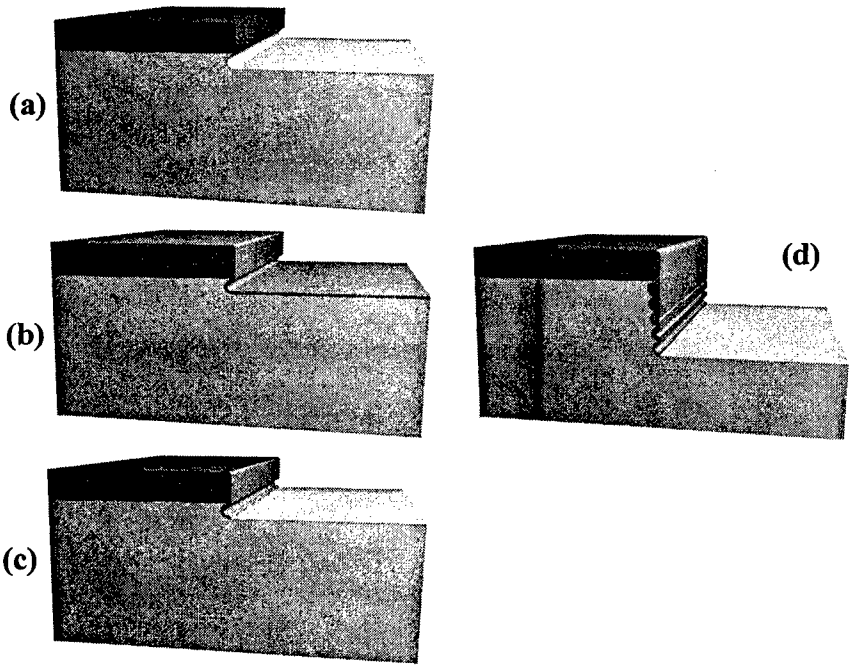


Figure 3: Schematic Birdseye view of a feature evolving during multi-step reactive ion etch process. Substrate is silicon and masking material is photoresist. (a): Isotropic silicon etch to a typical depth of 300 nm. High pressures, low powers, and gas mixtures of SF_6 and He ensure mask selectivity and high etching rates. (b): Isotropic deposition of etch-prohibiting polymer in a mixture of CF_4 and H_2. (c): Anisotropic removal of polymer in short high-ion energy plasma. Horizontal surfaces are cleared of the polymer by ion-bombardment assisted etching. (d): Feature edge after a few cycles. Due to the accumulation of polymer towards the top of the feature the underlying silicon sidewall can never be perfectly vertical.

decreased the lateral uniformity drastically. Polymer deposition was performed in a second step using a mixture of CF_4 and H_2 optimized for highest deposition rates. This etch-prohibiting polymer was anisotropically removed employing a short low-pressure high-energy plasma step in a mixture of SF_6 and He. The system was evacuated to <1 mT between all plasma steps, and the timing was adjusted to yield the target depth/cycle, minimal required sidewall polymer thickness, best mask selectivity, and highest aspect ratio. A depth of 10 μm was typically achieved after 8 to 10 hours of cyclic etching. Unlike a version of the Bosch process, this process did not promote forward scattering of the sidewall material, to maintain high mask selectivity. Consequently, the etch-prohibiting polymer accumulated towards the top of the features. Typically, 15 nm of polymer were required during each cycle, resulting in a total thickness of 0.5 μm after 33 cycles. The sidewall protection layer caused the features to broaden at the bottom, producing an aspect ratio of ≈20.

Porous Silicon Formation and Removal

Preliminary investigations revealed that traditional doping-selective etchants, such as $HF:HNO_3:CH_3COOH$ (1:3:8) do not provide sufficient selectivities to allow micron and submicron features to be fabricated. Even after extensive optimization, a doping contrast of $\approx 5 \cdot 10^{18} cm^{-3} / 10^{14} cm^{-3} = 50{,}000$ only produced a selectivity of less than 20. While electrochemical etching or polishing is theoretically capable of stopping at low-doped or undoped layers, the selectivity degenerates when the stopping layer and its features are exposed during the bulk removal. In a typical electrochemical setup, the epitaxial layer is covered with wax while the bulk is removed from the backside. However, we observed excellent selectivities for porous silicon formation at lower current densities. Unprotected features were subjected current densities of less than 10 mA/cm^2 in 49 % HF. The underlying p^{++} layer was converted to porous silicon, subsequently oxidized anodically in KNO_3, and removed in ethanoic HF. A final short dip in 1% KOH removed remaining porous silicon debris, as still visible on the left-hand side of Figure 4. Freestanding waveguide samples were stored in isopropanol and dried in a CO_2 critical-point dryer, while microdisk samples were rinsed in isopropanol and allowed to dry in air.

This process was used to fabricate linear waveguides, microrings, and microdisks as displayed in Figure 1(d) and Figure 4, to serve as THz resonators. The resonators and photonic crystal elements were patterned and etched using one photoresist masking layer. The structures were anisotropically etched with 300 nm per cycle to a depth of 10 μm. Microrings were subsequently undercut 3 μm while microdisk were underetched ≈20 μm.

Discussion of Results

We have fabricated freestanding all-silicon waveguides, couplers, and resonators with excellent surface and sidewall roughness and incorporated scale-model photonic elements, as depicted in Figure 4. The propagation of light at THz frequencies is currently under investigation using state-of-the-art Fourier Transform Infrared Spectroscopy. Transmission spectra can be recorded with resolutions as high as 0.125 cm^{-1} using a helium-cooled silicon bolometer detector and a broadband glowbar infrared source. However, coupling to and from our structures was difficult to obtain. Although optical fibers may be positioned accurately in a laboratory environment using micrometer xyz-stages, no far-infrared fibers were available to date. Most commonly, silicon or germanium lenses or prisms are employed, but the freestanding character of our structures prohibits a direct contact. Effectively, only end firing to freestanding waveguides was possible, which is expected to increase coupling losses to several tens of decibels. Until now, we were not able to couple to our structures efficiently enough to measure the transmission characteristics.

We have shown with Finite-Difference Time-Domain simulations that resonators based on whispering gallery modes are promising candidates for ultra-low threshold lasers and that holes etched periodically into our structures form photonic crystals with desirable photonic bandgap characteristics. Frequency selection using periodic defects was effective allowing narrow band propagation.

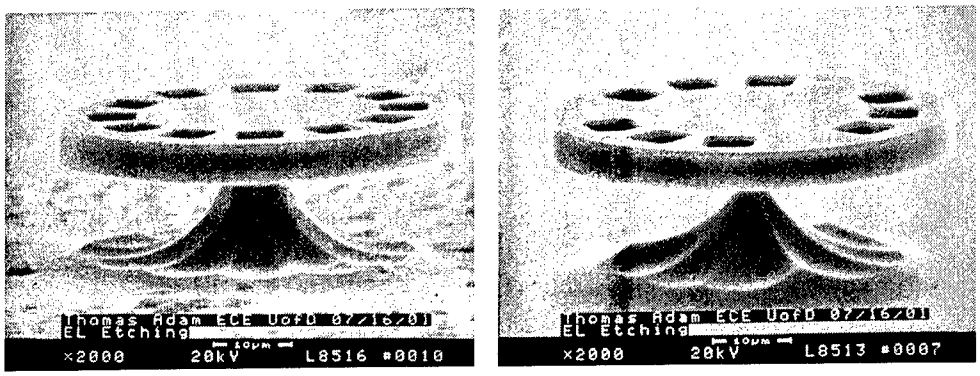


Figure 4: Birdseye view scanning electron micrograph of fabricated 50-μm diameter microdisk with photonic crystal elements. Left: Stop-band arrangement. Right: Frequency selection mode.

Acknowledgements

The authors gratefully acknowledge support by the DARPA-funded Air Force contract number F19628-00-C-0005, and by the AFOSR grant award number F49620-01-1-0042. Special thanks to Ayre Rosen and Gary Looney for useful discussions and CVD growth.

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RF and DC characteristics of low-leakage InAs/AlSb HFETs

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Abstract

InAs/AlSb HFETs with excellent RF and DC properties are reported. The drain currents are 750mA/mm with peak transconductance g_m of 1.1 S/mm. The gate leakage in is below 1nA/μm^2 for low gate bias. The threshold voltages of 0.25 μm and 0.5 μm gate-length devices are –2.5 and –1.5 V respectively, indicating short channel effects are present. Small-signal measurements on a 0.25 μm gate-length device show f_τ of 120 GHz and f_{max} of 100 GHz at drain voltages below 0.4V.

I. Introduction

Electrons in InAs/AlSb HFETs have high low-field mobility, high concentrations, and high peak and saturated velocities. A drawback of the technology is the low "breakdown" voltage associated with the relatively narrow bandgap InAs channel. As a result, InAs/AlSb HFETs are candidates for low-power high-frequency low-noise amplifiers and low-power high-speed digital ICs.[1] For such applications, we must design devices that exhibit high RF and DC performance at low drain and gate voltages. In the present work we report on the high quality characteristics of InAs/AlSb HFETs at drain biases below 0.4V.

II. Growth and Process Details

The InAs/AlSb HFET materials were grown by solid-state MBE on a semi-insulating (001) GaAs substrate. Valved cracker cells were used for both the Sb and the As beams. For Te doping, a PbTe source was used. The growth temperatures were calibrated with a pyrometer before starting the growth. Growth was initiated with a 0.1μm thick smoothing layer of GaAs and a 10nm thick transition layer of AlAs just before the nucleation of the 7% mismatched AlSb buffer layer. The AlSb buffer, grown at 570 °C, is 2μm thick and serves primarily to reduce the high density of threading dislocations to below 10^8 cm^{-2}. A 0.2 μm thick $Al_{0.8}Ga_{0.2}Sb$ layer was inserted prior to the growth of the InAs/AlSb HFET layers. The $Al_{0.8}Ga_{0.2}Sb$ layer provides a stable surface exposed during the mesa isolation fabrication step in the HFET process. The HFET active layers were grown at 500 °C and consisted of an 8nm thick AlSb bottom barrier, a 15nm thick InAs channel, and a 20nm thick AlSb top barrier. The InAs/AlSb interfaces are forced to be "In-Sb like" to provide the best transport properties

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for the InAs channel.[2,3] Tellurium modulation-doping of the top AlSb barrier is employed to supply the charge to the channel. The modulation doping layer is 3nm thick and separated from the InAs channel by a 5nm thick spacer. Finally, the layers are capped with a 5nm thick layer of $In_{0.5}Al_{0.5}As$. The energy band diagram for the device is shown in Figure 1. The $In_{0.5}Al_{0.5}As$ cap layer serves a dual purpose of protecting the underlying layers from oxidation and reducing gate leakage by increasing the valence band barrier between the channel and the surface.[1,4] Hall measurement on the as-grown wafer revealed a 300 K mobility of μ_e=16,000 $cm^2/V.s$ and an electron sheet concentration of N_s=5x12 cm^{-2}.

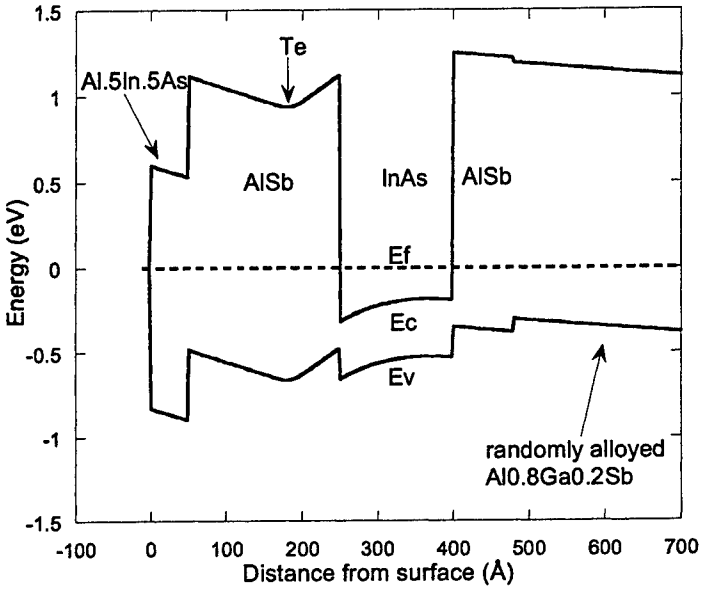


Figure 1. Energy band diagram of the InAs/AlSb HFET. The channel is modulation doped with Te donors in the top barrier and an $In_{0.50}Al_{0.50}As$ cap protects the AlSb barrier from oxidation and reduces gate leakage.

InAs/AlSb HFETs were fabricated using a conventional mesa-isolation process with alloyed Pd/Au contacts for the source and drain, and Cr/Au T-gates written with electron beam lithography. No gate-recess was required for these devices. Transmission-line measurements showed a contact resistance of 0.09 Ω-mm to the channel with a channel sheet resistance of 86 Ohms/square. The sheet resistance is consistent with the value obtained from the hall measurement. Devices with various gate-lengths and widths were written to understand the impact of these parameters on device operation.

III. Measurement and Results

The devices show typical output characteristics for InAs/AlSb HFETs with an enhanced drain conductance caused by impact ionization generated holes forward biasing the source-to-channel barrier.[5] We concentrate here on the input characteristics and the sub-threshold

characteristics of the device. Figure 2a shows the drain current and the transconductance g_m as a function of the gate voltage for an HFET with a gate length of 0.5μm. The drain current is a respectable value of 750 mA/mm at a drain voltage of 0.4V. The threshold voltage is -1.5V. The drain current changes only slightly at gate voltages close to zero volts thereby leading to lower g_m as may be expected for a device operating in the linear region. The g_m increases as the gate voltage is decreased and the device begins to operate in the saturated regime. We also note that the peak g_m increases dramatically as the *drain* voltage is increased peaking at a value over 1.1S/mm at a drain bias of 0.4V.

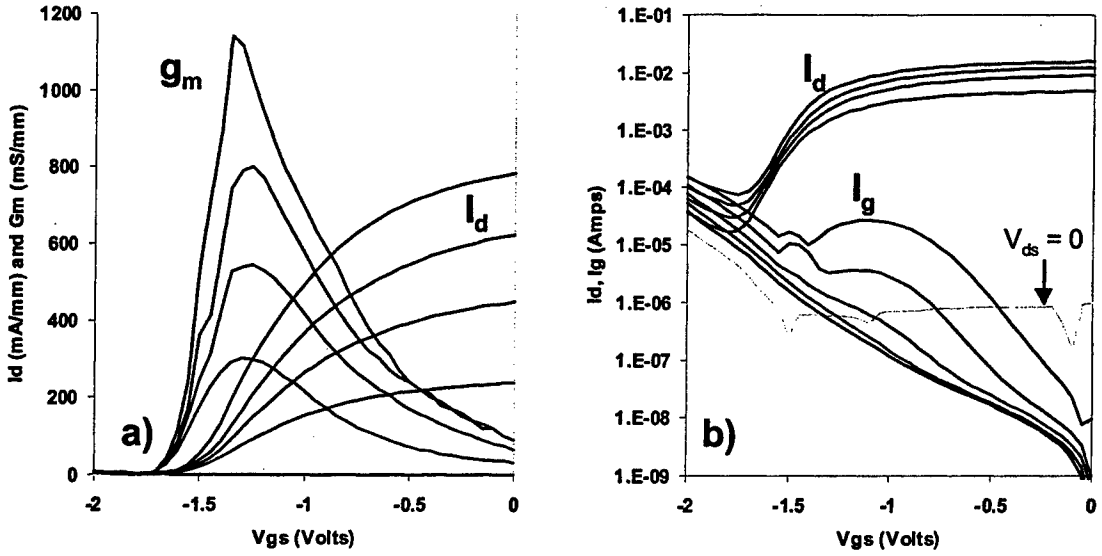


Figure 2 a) Drain current and DC transconductance g_m as a function of gate voltage for an HFET with a gate length of 0.5μm. The drain voltage is stepped at 0.1V with a maximum value of 0.4V. An I_{dss} of 750 mA/mm and $g_{m,max}$ of above 1.1 S/mm is excellent at these drain voltages. b) Sub-threshold characteristics of the same device showing very low gate leakage current below 10nA at low gate bias. The excess gate current at higher drain bias is a result of impact ionization in the channel. The dashed line is the drain current at 0V on the drain.

To further understand this increase in the g_m it is instructive to consider the sub-threshold characteristics of the device as shown in Figure 2b. The gate characteristics in Figure 2b show the previously observed excess gate current bumps associated with the collection of impact-generated holes by the negatively biased gate. The increase in g_m is commensurate with the excess gate currents. It appears that the dc g_m is artificially high due to the additional positive charge provided by the holes generated through impact ionization of hot electrons in the channel. The impact-generated holes are known to cause the increased output conductance in these devices, which simply translates into an inflated value for the transconductance.

A significant feature of our devices is their low-bias gate leakage of 1nA/μm^2, which is lower than the best published values for the InAs/AlSb HFETs. The low gate leakage is presumably a result of the $In_{0.5}Al_{0.5}As$ cap layer that presents a valence band barrier and reduces the leakage caused by hole conduction.[4] Devices with gate lengths of 0.25 μm were also characterized. The basic DC characteristics were largely similar with the exception of the threshold voltage, which was -2.5V compared to -1.5V for the 0.5 μm devices. This is the first indication that short channel effects (drain-induced barrier lowering) affect our present device design.

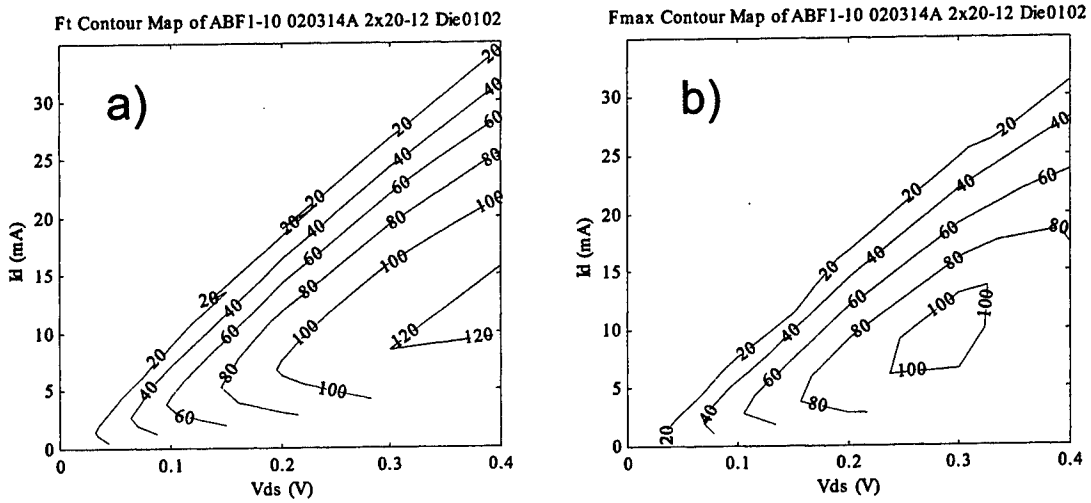


Figure 2 a) A contour plot of the small-signal current gain cutoff frequency f_τ for a 40μm wide InAs/AlSb HFET with a 0.25um gate length for a variety of gate and drain biases. b) A similar plot of the power gain cutoff frequency f_{max} for the same device. The pad parasitics have not been de-embedded from the small-signal data.

The RF characteristics of the devices were measured over a range of biases and contour maps of the RF parameters were generated as a function of dc bias. Figure 3 shows the contour maps for f_τ and f_{max} as a function of bias. For the 0.25 μm gate length HFET we obtain a peak f_τ of 120 GHz and f_{max} of 100 GHz for drain biases between 0.3V and 0.4V. The pad parasitics have not been de-embedded from the RF data. The devices exhibit poor RF performance at low gate biases, almost independent of the (relatively small range in) drain voltage. Given the high threshold voltages of these transistors, the lower f_τ and f_{max} at the low gate biases is a direct consequence of operating the device in its linear region. We also observe that the range in f_τ for these devices is considerably lower than the relative range of the dc g_m. The poor correlation between f_τ and dc g_m is consistent with our qualitative explanation that the anomalously high dc g_m reflects charge modulation from sources other than the input signal on the gate.

IV. Conclusions

The InAs/AlSb devices presented exhibit high drive current, low gate-leakage, excellent sub-threshold characteristics, and good RF properties. Sub-threshold measurements show gate currents below 1nA/μm^2 at low gate bias. Small-signal measurements on a 0.25 μm gate-length device demonstrate f_τ of 120 GHz and f_{max} of 100 GHz at drain voltages below 0.4V. The absolute threshold voltage for the present device design is high and must be increased above –1V for use in low-power high performance circuits.

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High Linearity, Robust, AlGaN-GaN HEMTs for LNA & Receiver ICs

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1. Introduction

AlGaN-GaN HEMTs have not only been identified as the technology of choice for next generation high-power, high frequency applications but recently have also garnered interest for low noise receiver applications[i,ii]. These devices have shown one-order higher power density over conventional GaAs-based HEMTs at X band and exhibit comparable cut-off frequencies for similar gate-lengths[iii]. The high power capability directly translates into the ability to handle a high input power or energy spike without failure in a receiver front-end.

For low-noise applications at microwave frequencies, the most important factors include: 1) channel sheet resistance and, 2) saturation velocity. Traditionally, InGaAs-channel HEMTs excel in both aspects and have been the champion of low-noise devices, with a representative device noise figure of 0.45 dB and circuit noise figure of 1.2 dB at X band.[iv] However these devices are typically limited by the small breakdown voltages and are susceptible to failure due to energy spikes at the input of the receiver, requiring an input protection diode that increases the system complexity as well as noise figure. Inspection of the properties of GaN-channel HEMTs shows that the very high 2-DEG density well compensates the lower mobility leading to a low channel resistance approaching InGaAs HEMTs, thereby enabling low noise figure operation.

In this paper, we will discuss the noise figure and linearity of robust GaN HEMTs for LNA integrated circuits. GaN HEMTs with a low noise figure of 0.75 dB at X-band are presented. We believe this is the first comprehensive report combining all major requirements of a Robust LNA-receiver technology: low noise figure, high linearity and high survivability.

2. Epistructure Growth and Device Fabrication

AlGaN-GaN HEMTs on SiC substrate were grown by MOCVD. An AlN nucleation layer was grown on the SiC substrate followed by an insulating GaN buffer and an AlGaN barrier layer with Al composition greater than 30%. The

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schematic of the AlGaN-GaN HEMT is shown in Figure 1. Subsequently, AlGaN-GaN HEMTs were fabricated using our standard process described elsewhere[v] and a T-Gate E-beam lithography technology. The gate-length of the fabricated HEMTs was ~ 0.18 μm for the low NF devices. The SEM photograph of a typical AlGaN-GaN HEMT device is shown in Figure 1.

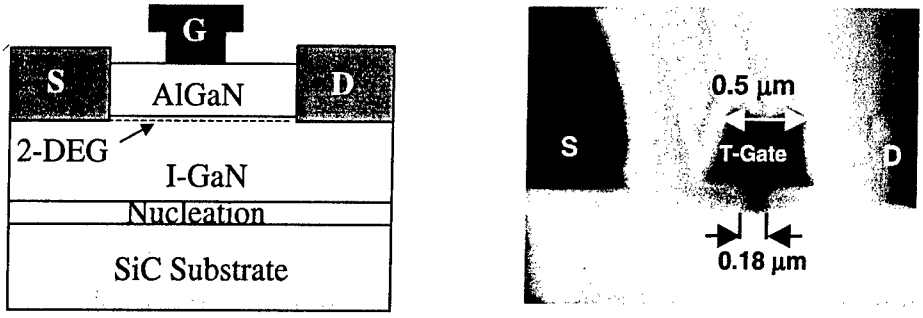


Figure 1. Schematic of the AlGaN-GaN HEMT on SiC & SEM of the 0.18 μm T-Gate

3. Noise Characterization

Noise characterization was done on an ATN Noise measurement system from 2-18 GHz. Noise figure performance was comprehensively studied as a function of gate-length/cut-off frequency, AlGaN barrier thickness, bias current and bias voltage. This resulted in complete mapping of the I-V plane for NF as well as indicated the trends that result from different device designs.

The 0.18-μm gate length devices exhibited a high small-signal gain of 17 dB at X band with an f_τ of 70 GHz and f_{max} of 105 GHz, on par with pHEMTs of the same gate length. The best NF obtained at 10 GHz was 0.75 dB, with a gain of 12 dB. By observing the trends in NF vs. gate-length (f_t), it is expected that a NF could be reduced to the 0.5-0.6 dB range for a device with >100 GHz f_τ. The small-signal frequency and the noise characterization data are shown in Figure 2. The V_{ds} was 15 V and V_{gs} was –4.5 V (~ 10% I_{dss}).

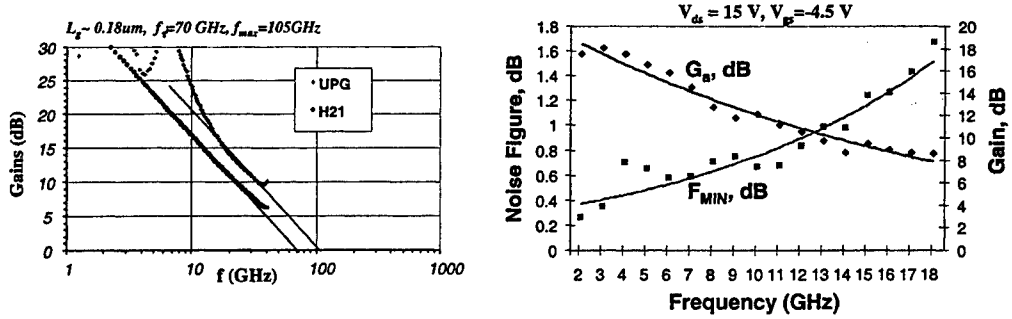


Figure 2. Small-signal characterization and Noise Figure measurement

The four-parameter noise model was also determined for this device giving F_{min} of 0.75 dB, R_n of 40 ohms, the real and imaginary parts of the optimum generator impedance being 0.76 (magnitude) and 14.4 (angle) respectively (W_g=150 μm).

The results of NF versus bias are shown in Figure 3. As a function of gate bias (drain current), the NF is high near pinch-off due to lower gain. As the device comes out of pinch-off, the gain increases and the NF drops. As the drain current further increases, the noise contribution from the drain current increases the NF. The best NF is obtained at about 10-15 % I_{dss}. This also happens to match the range of bias for obtaining high efficiency. With respect to the drain bias, NF is relatively insensitive, as long as the bias is above the knee voltage, in the high gain regime. Thus for the AlGaN-GaN HEMT, drain bias can be chosen to optimize other parameters of interest, such as linearity.

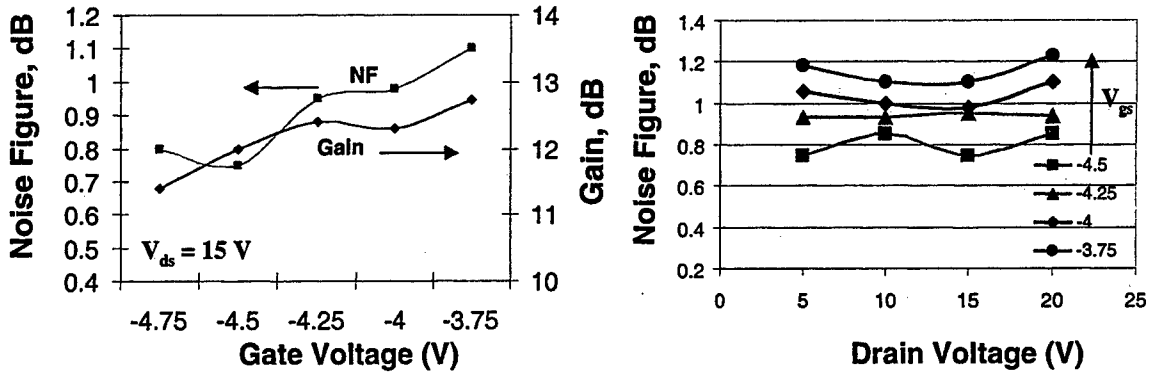


Figure 3. Characterization of NF as a function of bias at 10 GHz. The gate voltage range represents drain current from 5% to 30% I_{dss}.

For another set of devices (with longer gates), we also studied the NF behavior with respect to device parameters such as AlGaN barrier thickness and cut-off frequency. Figure 4 shows the effect of AlGaN barrier thickness (higher AlGaN barrier thickness implies lower transconductance and a higher pinchoff voltage for a fixed charge density). It is observed that for a given current level, it is desirable to have a lower AlGaN barrier thickness. This leads to higher gain and lower noise figure. However if the AlGaN barrier thickness is increased and the charge is also increased then the impact on NF could be different (for example the device resistances would be decreased, positively impacting the NF). It is clearly seen that a high f_τ is essential for lower NF.

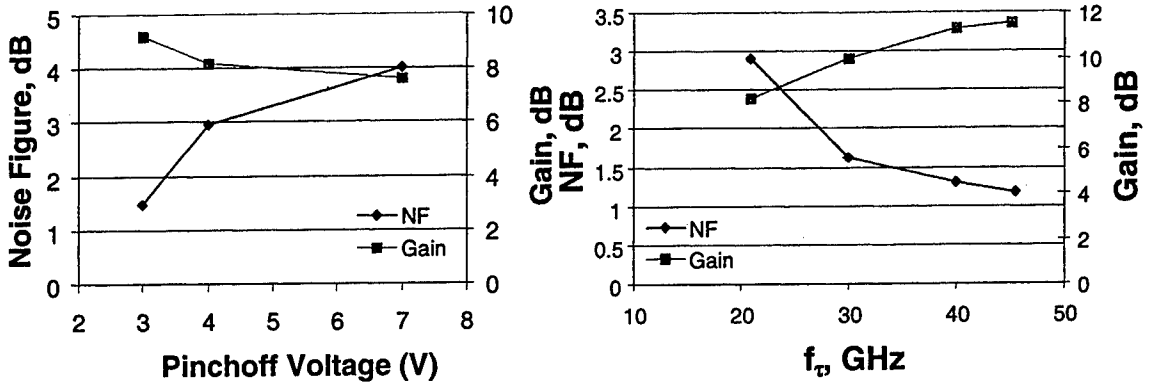


Figure 4. Noise figure as a function of AlGaN thickness/pinchoff voltage and f_t/gatelength

4. Linearity Characterization

Linearity characterization was performed with a two-tone intermodulation test at 10 GHz with an offset frequency of 100 kHz. The performance benchmark for a typical receiver application is the third order output intercept, referred to as the OIP_3. C is the carrier power and I3 is the power in the third order intermodulation product. G_p is the power gain. IP_3 is the power at which the level of I3 is equal to the carrier power. For a theoretical power sweep with class A bias, the I3 has a well-defined slope of 3 and the IP_3, which is the intersection of the two curves, is a fixed value. In most cases, especially for Class AB, and Class B, the IP_3 changes with input power since the I3 may not exhibit a fixed slope of 3. In such cases, extrapolations for IP_3 are more meaningful if taken from the region in which the C and the I3 conform to their expected slopes. The IP_3 is quite relevant for receiver devices like LNAs, which typically operate in the linear regime. A rule of thumb is that for high linearity devices, the separation between OIP_3 (Output Power corresponding to the IP_3 point) and P_{1dB} (1 dB Saturation power) is about 9-10 dB or higher. The results are shown in Figure 5 illustrating an OIP3 of 41 dBm and a LFOM (Linearity Figure of Merit = OIP3/DC Power) of 8.4. The P_{1dB} (single tone) was 29 dBm with a PAE of 30%.

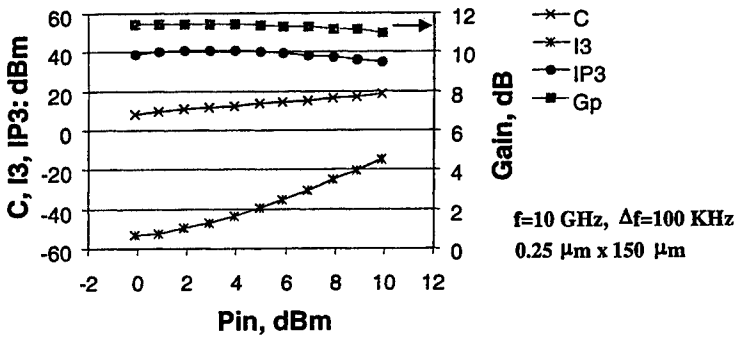


Figure 5. Linearity characterization at 10 GHz

Classic behavior is observed as a function of gate bias where Class AB-Class A operation results in high linearity. As a function of drain bias, linearity degraded at higher drain biases (> 20V). This could be the result of degradation or trapping effects at higher drain voltages and will be investigated in future. The results are shown in Figure 6.

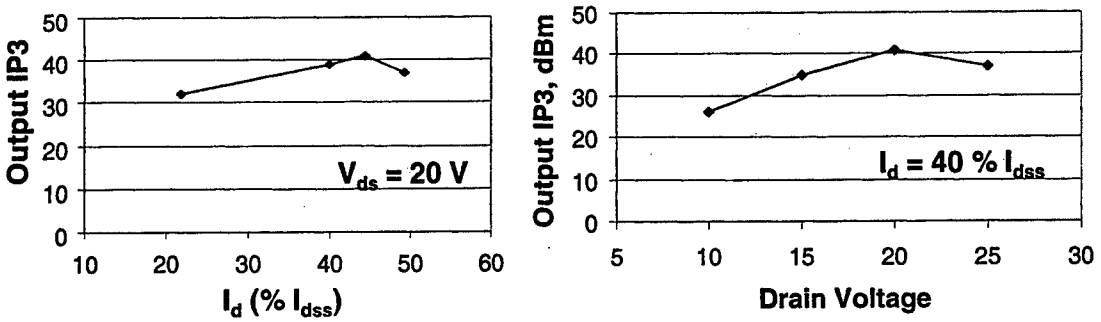


Figure 6. OIP3 (measure of receiver linearity) as a function of bias

5. Survivability Characterization

As stated earlier, the high survivability of GaN based HEMTs is an important feature making these devices attractive for robust LNA applications. We characterized low noise AlGaN-GaN HEMTs for sustaining high input power without failure. For the test device of 0.25 μm x 100 μm, the input survivability (we used maximum CW power with input of 50 ohms, that leads to failure as shown in Figure 7) ranged from 32-37 dBm depending on the bias conditions.

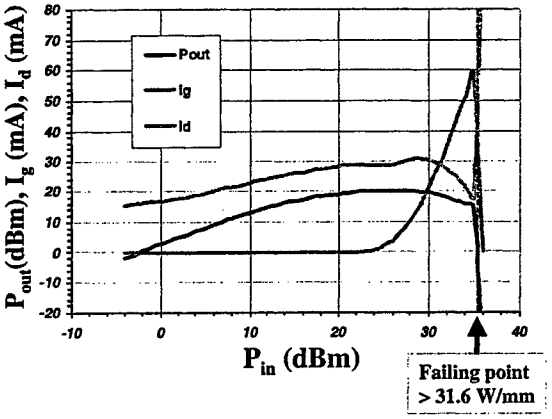


Figure 7. Typical Survivability test

The detailed results as a function of bias are shown in Figure 8. An interesting observation is that the survivability peaks around drain voltages of 25-30 V. At lower

voltage, the failure seems to be dominated by the gate current while at higher drain voltages, it is dominated by conventional channel breakdown. These effects have to be investigated in detail and could lead to ways of further improving the survivability.

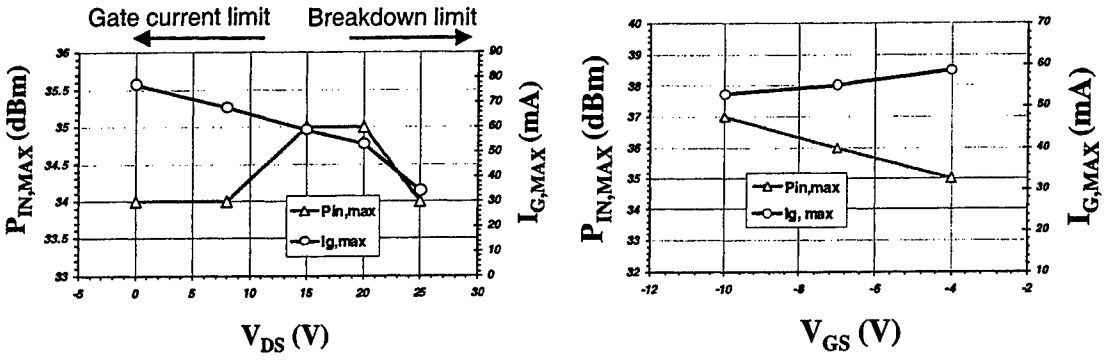


Figure 8 Input survivability as a function of drain and gate bias

While AlGaN-GaN HEMTs promise robust operation for LNA receiver applications, more detailed measures of survivability such as degradation of gain following an input pulse have to be developed and device structures optimizing the same need to be demonstrated.

6. Summary

We have demonstrated 0.18-μm AlGaN-GaN HEMTs with X-band noise figure of 0.75dB and gain of 12 dB. The key to achieving the low noise figure is realizing high f_t with minimized gate leakage. 0.25-μm AlGaN-GaN HEMT devices exhibited OIP3 (2-Tone linearity) of 37-40 dBm, which was about 8-10 dBm higher than P_{1dB}, with the best OIP3 being 41 dBm (12 dBm higher than P_{1dB}) indicating very linear operation. An input survivability capability of 32-50 W/mm (~ 10-15x higher than GaAs/InP) was demonstrated. The high survivability can help eliminate the input protection diode in LNA receivers improving the overall system noise.

With the careful optimization of linearity, noise figure and survivability, AlGaN-GaN HEMTs are very attractive for robust, high dynamic range LNA ICs for receiver applications. Future work will focus on further optimization of the device performance and the development of GaN HEMT LNA ICs. Already the leading candidate for next generation transmit power amplifiers, GaN-based HEMTs have the potential of delivering a complete transmit-receive solution.

Acknowledgments

This work was supported by ONR Research contract N00014-00-C-0175 monitored by Dr. H. Dietrich and Dr. J. Zolper. Bill Mitchell at University of California Santa Barbara assisted in the E-beam lithography.

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AlGaN/GaN HEMT high-power and low-noise performance at $f \geq 20$ GHz

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Abstract

In this paper, we report on the power and noise performance of AlGaN/GaN HEMTs in the K (18 – 27 GHz) band. At 20 GHz, a record CW output power of 2 W with an associated gain of 8 dB and PAE of 33 % has been achieved on a 8-finger 0.2 μm x 500 μm device. Minimum noise figure of 1.4 dB has been achieved on a 0.15 μm x 200 μm device at 26 GHz. The data demonstrate the viability of AlGaN/GaN HEMTs for high-frequency power and LNA applications.

I. Introduction

The high breakdown fields, high electron saturation velocity, and high electron densities in AlGaN/GaN HEMT structures have led to microwave power performance significantly exceeding the performance of state-of-the-art GaAs and InP-based devices [1-3]. Demonstrated low minimum noise figures make AlGaN/GaN HEMTs very attractive for use in robust low-noise amplifiers (LNAs). Low-noise, high breakdown GaN HEMTs [4] in amplifier front-ends eliminate the need for diode limiters as protection against RF overstress. This can reduce the overall LNA noise figure by 1dB. While the performance of GaN HEMTs in the L-Ku bands has been thoroughly investigated in recent years, very few reports are available on the operation of these devices at frequencies above 18 GHz [2,5]. These frequencies are important for satellite communication and high-performance radar applications. In this paper, we report on the power and noise performance of AlGaN/GaN HEMTs in the K (18 – 27 GHz) band.

II. Device Fabrication

The AlGaN/GaN structures were grown by metalorganic chemical vapor deposition (MOCVD) on top of semi-insulating 4H-SiC substrates and showed an average sheet resistance in the range of 350-450 Ω/sq. The device mesa etch was performed using Cl_2/BCl_3 ICP etching technique. Ti/Al/Ni/Au ohmic contacts with an

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average contact resistance of 0.6-0.8 Ω mm were formed by alloying at 880 °C in a nitrogen atmosphere. Electron beam lithography was utilized to fabricate 0.12-0.2 μm Pt/Au T-gates in a 2 μm source-drain region. The source to gate distance was 0.8 μm. The devices were passivated with PECVD SiN and two levels of interconnect metal including airbridges were used for external connections. The AlGaN/GaN HEMTs had a peak transconductance of ~ 300 mS/mm and a maximum drain current density in excess of 1 A/mm (measured at V_G = + 1V). The typical on-state breakdown voltage was 35-40 V. A negative output conductance was observed under high bias conditions for large gate periphery devices due to self-heating effects. Small-signal RF measurements yielded a unity gain cut-off frequency (f_t) of 34 GHz for HEMTs with 0.2 μm gates, 44 GHz for 0.15 μm devices, and 50 GHz for 0.12 μm HEMTs. The maximum frequency of oscillations (f_{max}) was around 77 GHz for 0.15 and 0.2 μm-gate devices and 103 GHz for 0.12 μm HEMTs.

III. Microwave Power Performance

Continuous wave power measurements at 20 GHz were performed on 8-finger devices with the total gate periphery of 500 μm and the gate pitch of 40 μm using a Q-band Focus load-pull system. The results of the on-wafer load-pull measurements are shown in Fig. 1.

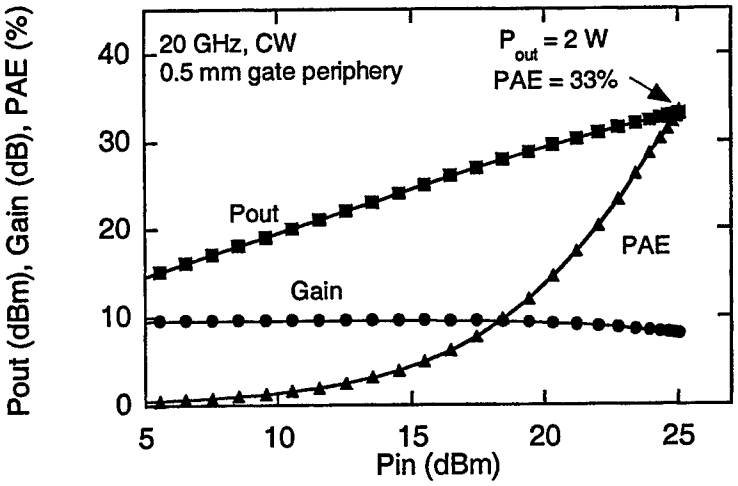


Figure 1. Power performance of a 500 μm AlGaN/GaN HEMT showing a total CW output power of 2 W at 20 GHz. The device was biased at V_{DS} = 25 V and I_{DS} = 250 mA.

When biased and tuned for the maximum output power, the device under investigation showed the total output power of 2 W with an associated power added efficiency (PAE) of 33 % and gain of 8 dB. To the best of our knowledge, this is the highest total output power reported for AlGaN/GaN transistors at 20 GHz. Note, that the device was not driven far into gain compression in this case and the measured maximum output power was limited by the available input drive power.

IV. Microwave Noise Performance

High frequency noise performance of the devices was measured using an ATN noise parameter test set. Noise figure measurements have been performed from 2 to 26 GHz. A plot of the noise characteristics as a function of frequency for a 0.12 μm gate device (wafer A) and a 0.15 μm device (wafer B) with the total gate peripheries of 200 μm is shown in Figure 2. The minimum noise figure of 1.4 dB was achieved for the AlGaN/GaN HEMTs at 26 GHz. This is comparable to the NF_{min} of 1.4-1.6 dB typically demonstrated by GaAs HEMTs at this frequency.

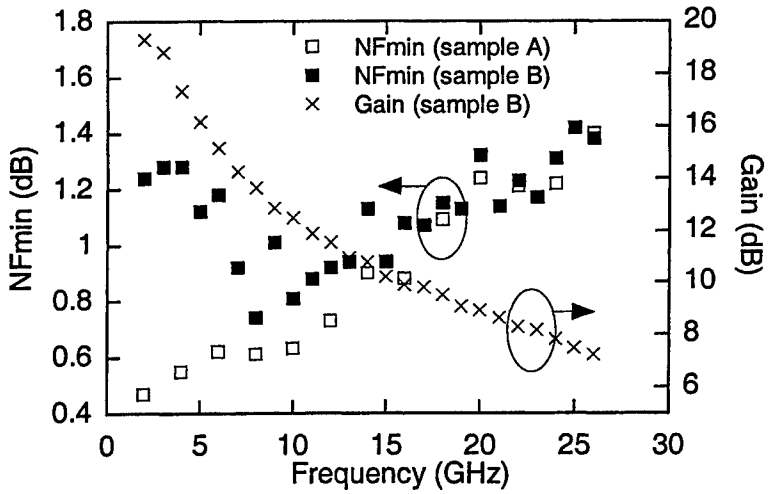


Figure 2. Minimum noise figure versus frequency for a 0.12 μm AlGaN/GaN HEMT (wafer A, open squares) and a 0.15 μm gate device (wafer B, dark squares) with the gate peripheries of 200 μm. The associated gain is shown for a 0.15 μm HEMT (crosses). The devices were biased at V_{DS} = 15 V and I_{DS} = 12 mA.

An unusual behavior of F_{min} is observed for wafer B below 10 GHz where the device noise increases with decreasing frequency. Similar $1/f$ dependence of NF_{min}

below ~ 8 GHZ is often observed in InP/InAlAs/InGaAs HEMTs [6]. In InP-based devices, the upturn in the minimum noise figure at high drain-source biases is typically attributed to the increase in the gate current dominated by impact ionization process in the InGaAs channel [6,7].

However, for a typical wide-band gap AlGaN/GaN HEMT one would not expect significant impact ionization to occur at moderate V_{DS} voltages. This is exemplified in our results from wafer A's devices which do not exhibit $1/f$ dependence of NF_{min} (Fig.2) or impact ionization gate current (Fig.3(a)). On the other hand, devices from wafer B do exhibit the bell-shaped feature in I_G-V_G plots (Fig.3(b)), which is the signature of impact ionization generated gate current [8].

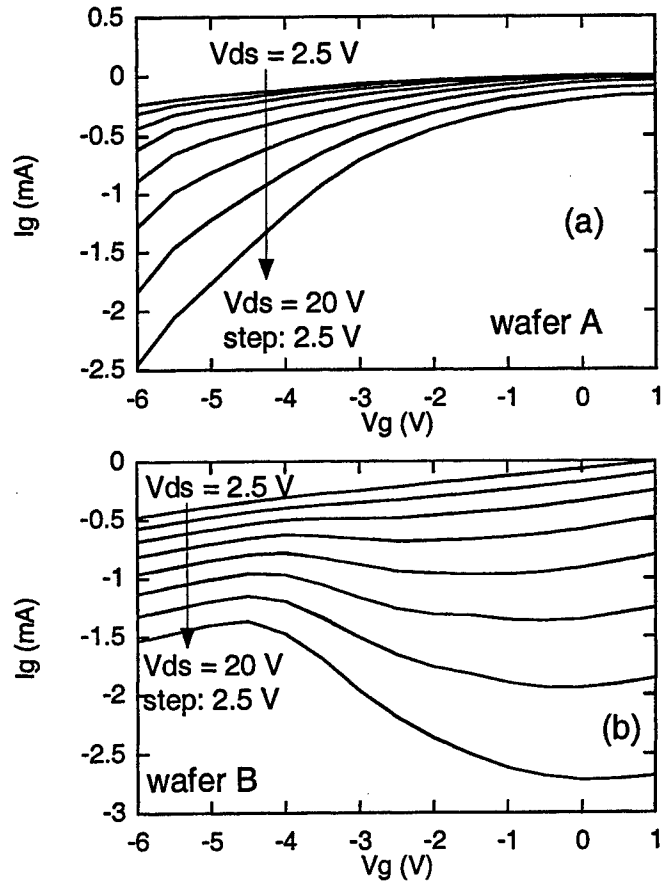


Figure 3. Gate current I_G versus gate-source voltage V_G for (a) a 0.12 μm x 200 μm AlGaN/GaN HEMT on wafer A, and (b) a 0.15 um x 200 um device on wafer B for different drain-source voltages.

The impact ionization gate current for the devices on wafer B correlates to significant increase in the low-frequency noise. Figure 4 shows that the magnitude of $1/f$ dependent NF_{min} increases almost proportionally with impact ionization generated gate current. On the other hand, devices on wafer A do not show any evidence of the impact ionization and, as a result, the low-frequency noise is significantly smaller in this case. More studies are currently under way to determine the reasons for such a significant difference in the device behavior between different AlGaN/GaN wafers.

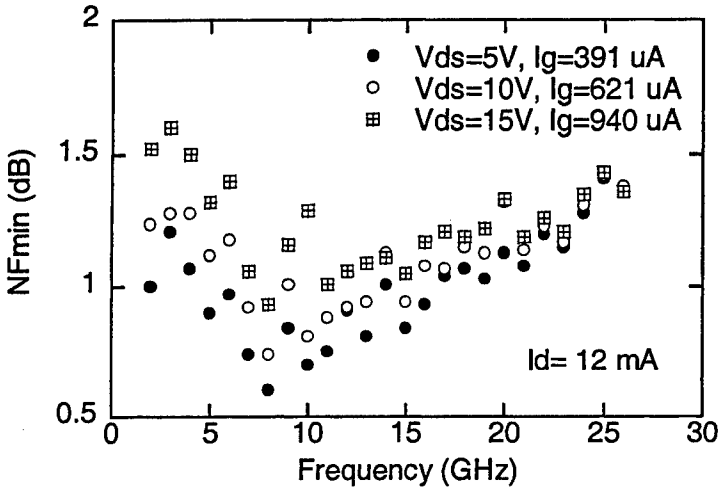


Figure 4. Minimum noise figure versus frequency for a 0.15 μm x 200 μm AlGaN/GaN HEMT (wafer B) at different values of V_{DS}: 5 V (dark circles), 10 V (open circles) and 15 V (squares with crosses). The drain current was kept constant at 12 mA.

V. Summary

In summary, we demonstrated an excellent power and microwave performance of AlGaN/GaN HEMTs at $f \geq 20$ GHz. The maximum total CW output of 2 W with an associated power added efficiency of 33 % and gain of 8 dB was measured on a 8-finger 500 μm device. Minimum noise figure of 1.4 dB has been achieved on a 0.15 μm x 200 μm device at 26 GHz. The presented data demonstrate the viability of AlGaN/GaN HEMTs for high-frequency power and LNA applications.

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Effect of recess length on DC and RF performance of gate-recessed AlGaN/GaN HEMTs

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Abstract

We present the effect of gate-recess length on DC and RF performance of AlGaN/GaN gate-recessed HEMTs. 0.15 μm gate-length AlGaN/GaN HEMTs with varying gate-recess lengths were fabricated. DC and microwave performance did not exhibit significant dependence on the gate-recess length. We attribute these results to essentially identical series source resistances, so that all the gate-recessed HEMTs exhibited similar DC and RF performance. This conclusion is derived from the fact that the values of ohmic contact resistances dominated over the values of channel resistances. The nature of the breakdown in the HEMTs was also studied. The results of temperature-dependent breakdown voltage measurements suggest that the breakdown mechanism was mainly due to tunneling gate leakage currents via shallow traps.

1. Introduction

GaN-based high-electron mobility transistors (HEMTs) are promising candidates for high power and high temperature applications due to excellent properties of the material such as high critical breakdown field, high saturation and overshoot electron velocities, and good thermal conductivity. Recently, AlGaN/GaN HEMTs with record unity current gain cut-off frequency of 110 GHz and maximum frequency of oscillation over 140 GHz have been demonstrated by reducing the gate-length down to 50 nm [1]. However, short gate-length HEMTs typically produce poor channel modulation and low breakdown voltages. Two-dimensional full-band Monte Carlo simulations including polarization effects showed that, as the gate length for $Al_{0.2}Ga_{0.8}N$/GaN HEMTs decreases from 0.9 to 0.1 μm, threshold voltage shifts from -8 V to -12 V, and breakdown voltage drops from 300 to 60 V [2]. Further improvements for the short-gate length devices are expected through the use of gate-recessing, since the gate-recessing leads to better channel modulation, while the gate-length shrinks. Another advantage of gate-recessing is that breakdown voltage can be improved by mitigating the highest electric field strength at the drain-side of the gate, where breakdown typically occurs.

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The breakdown mechanism in FETs is a complicated phenomenon, where one needs to consider combined effects of impact ionization, tunneling current, and surface states. It is important to identify the dominant breakdown mechanism in order to optimize device design or fabrication process to enhance the device performance. Study [3] on the gate leakage mechanisms in AlGaN/GaN HEMTs showed that vertical tunneling was the main mechanism for gate leakage current in standard-barrier HEMTs, whereas lateral tunneling becomes substantial in enhanced-barrier HEMTs with GaN cap. The same study considered the possibility of defect-assisted tunneling. Another group [4] proposed hopping conduction along the surface to be the dominant leakage mechanism in their AlGaN/GaN HEMTs. The average activation energies were determined to be 70 ± 20 meV and 200 ± 20 meV for SiN passivated and unpassivated devices, respectively. More recent study [5] on the gate leakage effects in GaN-based HEMTs reported the surface hopping conduction with an activation energy of 210 meV.

AlGaN/GaN HEMTs in this work were recessed in an inductively-coupled-plasma reactive ion etching (ICP-RIE) system. Etching in the ICP-RIE reactor allows separate control of the plasma density and ion energy, which enables operation at low substrate biases, while achieving high etch rates [6]. Successful gate-recessed AlGaN/GaN HEMTs using ICP-RIE were reported recently with the breakdown voltage of 90 V for 0.25 μm devices [7].

2. Experimental

The device structure under study was grown on a sapphire substrate by molecular beam epitaxy (MBE). The epilayer consisted of 2 μm undoped GaN, 30 nm undoped $Al_{0.24}Ga_{0.76}N$ and a 5 nm undoped GaN cap layer. Hall measurements showed a sheet carrier concentration of 1.5 x 10^{13} cm^{-2} and an electron mobility of 1170 cm^2/V-s. Device fabrication started with the mesa isolation using Cl_2/Ar plasma in the ICP-RIE system. The source and drain ohmic contacts were formed by rapid thermal annealing of evaporated Ti/Al/Mo/Au at 875 °C for 30 s. Using on-wafer transfer length measurement (TLM) patterns, the ohmic contact resistance (R_c) and sheet resistance (R_{sh}) were typically measured to be 0.7 Ω-mm and 330 Ω/sq.

For gate-recessing, PMMA resist was used as an etch mask. Three different lengths (L_{gr}) for the gate-recess area were designed: 0.5, 0.75 and 1.0 μm. The recess windows, centered between the source and drain, were patterned by e-beam lithography. The recess etch was performed in Cl_2/Ar plasma with a gas flow rate of 15/5 sccm, a pressure of 3 mT, a self-induced bias of -50 V, and an ICP coil power of 150 W. Initially, gate-recess etching was characterized with test devices by measuring the decrease in the drain current as a function of etch time as shown in Figure 1. The drain current density for the unetched test devices was approximately 1.30 A/mm at V_{DS} = 10 V; after 30 s of etching, it decreased by ~10 % to 1.15 A/mm and did not change substantially upon further etching by 30 s steps until the drain current significantly degraded after total etch time of 120 s. Therefore, we performed the recess etch for the devices under study for 80 s. Figure 2 shows an atomic force microscope

(AFM) image of the etched area for a 1.0 μm opening. The gate-recess area dimensions were close to the designed values, and the average etched depth was 5 ± 1 nm. The main uncertainty in the depth measurements was due to the surface roughness of the original sample, which was approximately 1 nm as estimated from AFM scans. The surface roughness did not change upon gate-recess etching. To reduce any etch-induced damage and restore Schottky barrier height of the etched surface to that of unetched surface, the sample was rapid-thermally annealed at 700 °C for 1 min in N_2 ambient [8]. Finally, T-gates (Ni/Au) with the gate-length (L_g) of 0.15 μm were patterned using e-beam lithography within the recess windows. The devices had a gate width (W) of 100 μm and source-drain spacing (L_{sd}) of 2.6 μm.

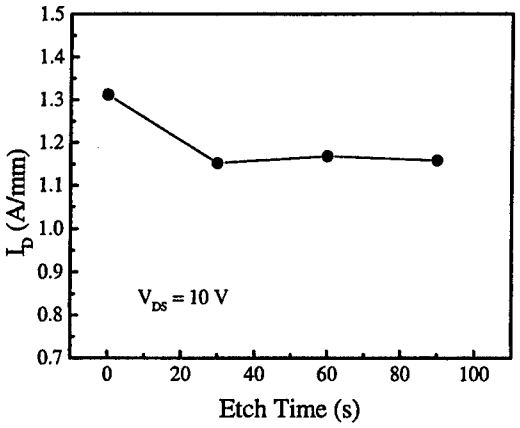


Fig. 1. Drain current as a function of gate-recess etch time at V_{DS} = 10 V for the HEMT with L_{gr} = 0.5 μm.

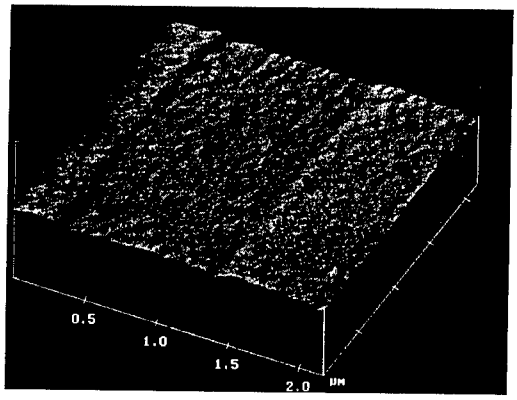


Fig. 2. AFM image of the gate-recessed area with L_{gr} = 1.0 μm.

DC measurements were carried out using HP 4142B semiconductor parameter analyzer, while the small signal RF performance was measured using an HP 8510B network analyzer. A Cascade Microtech probe station with a temperature-controlled stage was employed for temperature-dependent breakdown voltage (BV) measurements. The stage had a temperature range of -55 to 200 °C and was situated within an enclosure that was purged with nitrogen.

3. Results and discussions

3.1. DC and microwave performance

Figure 3 shows DC performance of 0.15 μm gate-length device with L_{gr} = 0.5 μm. Maximum drain current density (I_{Dmax}) was 1.1 A/mm at a gate bias of 2 V. The device was completely pinched off at a gate bias of -8 V. The DC transfer characteristics at a drain bias of 7 V produced an extrinsic transconductance ($g_{m,ext}$) peak value of 213 mS/mm at V_{GS} = -6.25 V. The threshold voltage (V_T) is defined as the gate voltage intercept of the linear

extrapolation of $I_D - V_{GS}$ characteristic at the maximum transconductance point. According to this definition, the threshold voltage was -7.5 V. The gate-to-drain Schottky characteristics with a floating source were used to estimate the gate-to-drain breakdown voltage (BV_{GD}). Figure 4 shows a typical characteristic with a BV_{GD} of 22.5 V measured at a reverse gate leakage current (I_G) of -1mA/mm.

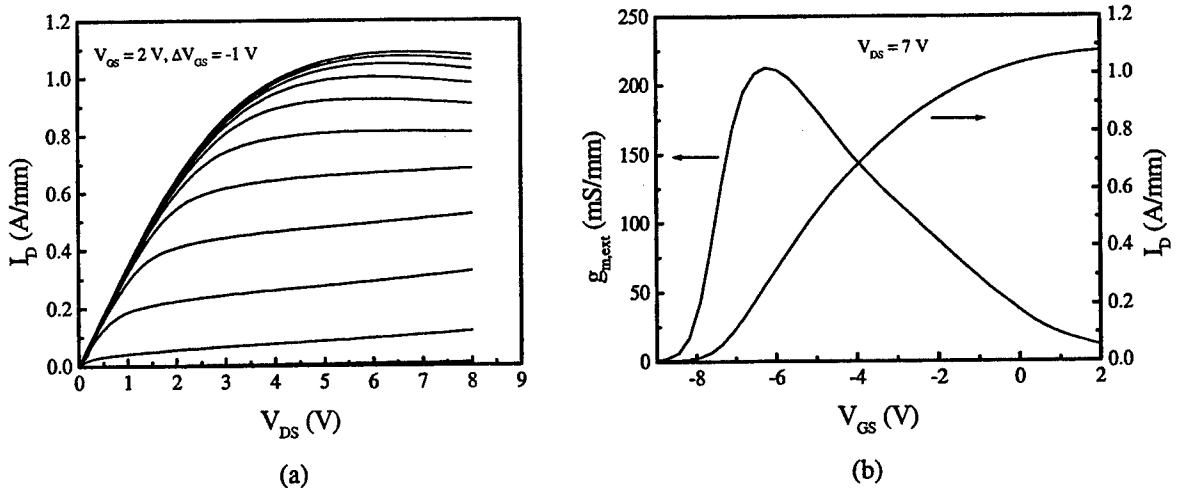


Fig. 3. DC performance of a typical recessed 0.15 μm x 100 μm AlGaN/GaN HEMT with L_{gr} = 0.5 μm: a) I_D-V_{DS} characteristics, the V_{GS} is swept from 2 to – 8 V; b) transfer characteristics at a drain bias of 7 V.

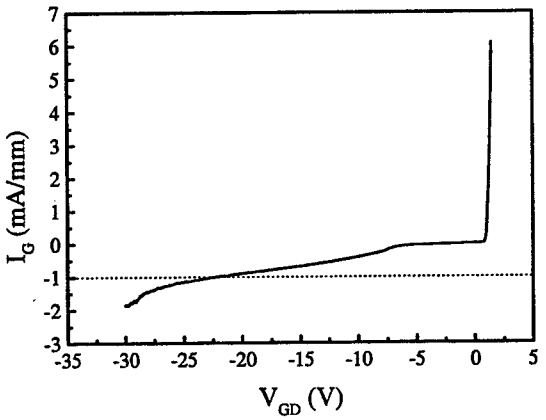


Fig. 4. Gate-to-drain Schottky diode characteristic of a typical recessed 0.15 μm x 100 μm AlGaN/GaN HEMT with L_{gr} = 0.5 μm.

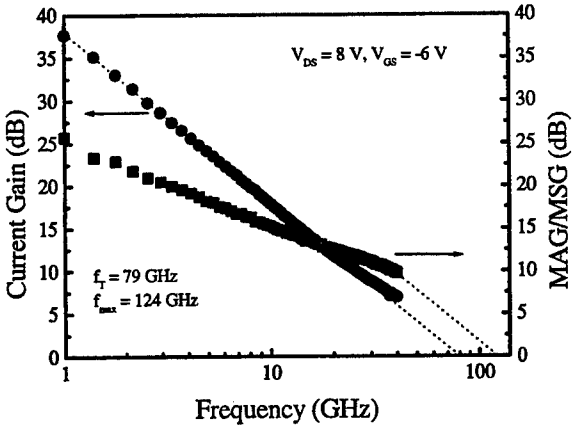


Fig. 5. Measured current gain and maximum available power gain of a typical recessed 0.15 μm x 100 μm AlGaN/GaN HEMT with L_{gr} = 0.5 μm. The device was biased at V_{DS} = 8 V and V_{GS} = -6 V.

Figure 5 shows the short-circuit current gain ($|h_{21}|$) and maximum available power gain (G_{Amax}) derived from on-wafer S-parameter measurements for a 0.15 μm gate-length gate-recessed HEMT with L_{gr} = 0.5 μm. The measurements were carried out at V_{DS} = 8 V and V_{GS} = -6 V. The values of unity gain cutoff frequency (f_T) and maximum frequency of oscillation

(f_{max}) were determined by extrapolation of the $|h_{21}|$ and G_{Amax} data at -20 dB/decade. The f_T and f_{max} were measured to be 79 and 124 GHz, respectively.

HEMTs with different L_{gr} produced similar DC and RF data. The comparison of typical device performances for different L_{gr} is presented in Table 1. It can be seen that the data are essentially identical for various gate-recess window lengths. Therefore, varying L_{gr} in the range of 0.5 – 1.0 μm did not affect the HEMT performance substantially, and the slight variation in the data was, mainly, due to non-uniformity of the sample and measurement errors.

Table 1. Comparison of typical DC and microwave performances for 0.15 μm gate-recessed AlGaN/GaN HEMTs with different L_{gr}.

L_{gr} (μm)	$g_{m,ext}$ (mS/mm)	I_{Dmax} (A/mm)	f_T (GHz)	f_{max} (GHz)	BV_{GD} (V)
0.5	210	1.1	77	125	22.5
0.75	185	1.07	75	125	25
1.0	190	1.1	75	125	24

In order to analyze the results obtained, we addressed the series source resistance (R_S) of the devices under study, since its value specifies the extrinsic transconductance and also affects f_{max} of HEMTs. The expression for the source resistance of gate-recessed HEMTs is given by

$$R_S = \frac{R_c}{W} + R_{sh1}\frac{L_{gs1}}{W} + R_{sh2}\frac{L_{gs2}}{W}, \qquad (1)$$

where L_{gs1} and L_{gs2} are the parts of the total gate-to-source distance (L_{gs}) in the unrecessed and recessed areas, respectively; R_{sh1} and R_{sh2} are the corresponding sheet channel resistances. From TLM measurements, we obtained R_c = 0.7 Ω-mm and R_{sh1} = 330 Ω/sq. The R_{sh2} can be estimated from the data taken during gate-recess etching of "ungated" HEMTs, where we can extract total resistance between the source and drain contacts (R_{DS}) from the slope $I_D - V_{DS}$ at low V_{DS} (below knee voltage). R_{DS} can be written as follows

$$R_{DS} = 2\frac{R_c}{W} + \frac{R_{sh1}(L_{sd} - L_{gr})}{W} + \frac{R_{sh2}L_{gr}}{W}. \qquad (2)$$

It was found that for HEMTs with L_{gr} = 0.5 μm, R_{DS} increased by ~10% after gate-recess etch. After the substitution of TLM data and device parameters into Equation 2 for etched and unetched HEMTs, we estimated R_{sh2} to be ~ 780 Ω/sq. With all parameters known, we

applied Equation 1 to the gate-recessed HEMTs and calculated that R_S increased by only ~9% for L_{gr} varying from 0.5 to 1.0 μm.

Thus, the gate-recessing with a length range of 0.5 – 1.0 μm did not lead to a significant variation of R_S, and we attribute this fact to the relatively high contact resistance (typical for AlGaN/GaN HEMTs) compared to the low sheet resistance. The source resistance was dominated by the contact resistance, and, therefore, increased sheet resistance in the gate-recessed region, R_{sh2}, had no substantial effect on R_S, which lead to identical DC and RF performance for devices with different gate-recess length.

3.2. Temperature-dependent BV measurements

Temperature-dependent I_G – V_{GD} characteristics are shown in Figure 6. The stage temperature was swept from -50 °C to 100 °C. BV_{GD} was defined at a reverse gate leakage current of -1 mA/mm. The BV_{GD} as a function of temperature is plotted in the inset in Figure 6. It is clearly seen that the dependence of BV_{GD} on temperature is negative, which suggests that the main breakdown mechanism is the tunneling gate leakage current. It was observed that the gate leakage current decreased exponentially versus reciprocal temperature within the temperature range of -25 – 75 °C. This type of temperature-dependence is typical for shallow trap-assisted (hopping) conduction mechanism [9]. In Figure 7, the Arrhenius plot for the gate leakage current at V_{GD} = -10 V is presented. The activation energy for recessed devices was 80 ± 10 meV. The definite origin of these traps is under investigation.

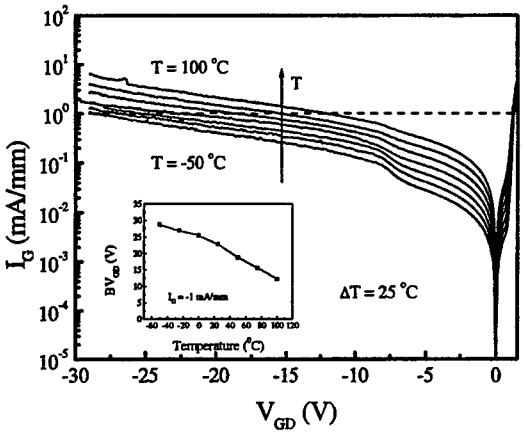


Fig. 6. Temperature-dependent I_G -V_{GD} characteristics of a typical recessed 0.15 μm x 100 μm AlGaN/GaN HEMT with L_{gr} = 0.5 μm. The temperature was swept from – 50 to 100 °C, with the step of 25 °C. The inset shows BV_{GD} as a function of temperature. The BV_{GD} is measured at the I_G = - 1 mA/mm.

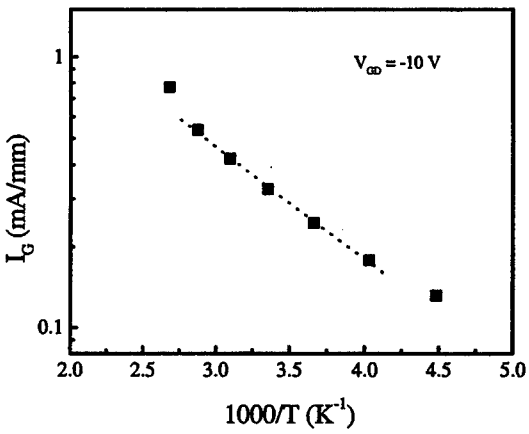


Fig. 7. The Arrhenius plot for the gate leakage current at V_{GD} = -10 V.

4. Conclusion

Gate-recessed AlGaN/GaN HEMTs with varying gate-recess lengths have been studied. These 0.15 μm gate-length devices exhibited I_{Dmax} =1.1 A/mm, f_T = 79 GHz, and f_{max} = 125 GHz. Typical BV_{GD} was 24 V for reverse gate leakage current of -1 mA/mm. Our findings indicated that DC and microwave performance did not change substantially for various recess lengths in the range of 0.5 – 1.0 μm. The estimated values of series source resistances suggest that the value of ohmic contact resistance dominated the change in the channel resistance after gate-recessing, so that the etch step did not lead to noticeable variation in R_S due to the size of recessed window. Breakdown voltages also did not show any correlation with gate-recess lengths, and the main breakdown mechanism was attributed to tunneling through shallow traps with an activation energy of 80 ± 10 meV.

Acknowledgements

This work was supported at UIUC by ONR under contracts N00014-01-1-1000 and N00014-01-11072 supervised by Dr. J. Zolper.

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Reliability Evaluation of AlGaN/GaN HEMTs grown on SiC Substrate

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Abstract

AlGaN/GaN HEMTs have achieved record output power densities at microwave frequencies; however, reliability of these devices is still a major concern. In this paper, the results of DC and RF stress tests at several drain voltages of passivated 75 μm devices are discussed. After DC stress for 48 hours, negligible differences in I-V and small signal performance were observed in some devices, while significant reduction in drain current, decrease in transconductance, and increase in on-resistance were measured in some other devices. RF stress for 40 hours has resulted in lower transconductance and drain current and degradation in power performance at 10 GHz. A comprehensive comparison of equivalent circuit models before and after stress is presented.

Introduction

The wide interests to develop high-power, high-efficiency microwave transistors for defense applications have fueled the recent advances in AlGaN/GaN high electron mobility transistors (HEMTs). This material system's intrinsic properties lead to high breakdown voltage and high saturation current, which are required to produce large RF current and voltage swing. Record output power densities of 10.7 W/mm at 10 GHz [1] have been demonstrated, however reliability is still a main concern to realize the potential of manufacturing AlGaN/GaN HEMTs. There have been few reports on the reliability evaluation of these devices. One study showed that no changes in the DC characteristics of doped channel AlGaN/GaN HEMTs were observed after heating the device up to 600 °C [2]. Another recent study showed that under RF stress conditions for over 10 hours, Si_3N_4 provided better reliability than SiO_2 [3] on undoped AlGaN/GaN HEMTs.

The aim of this paper is to present the results and observations of the degradation characteristics due to DC and RF stress tests on AlGaN/GaN HEMTs grown on silicon carbide (SiC) substrate. For the stress tests, several devices were randomly selected across a 2" wafer, and the DC and microwave performance were measured and compared before and after stress. Small-signal equivalent circuit parameters (ECPs) were extracted and compared using the measured s-parameters before and after DC and RF stress.

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Device Fabrication and Characteristics

The AlGaN/GaN HEMTs were grown at the University of South Carolina on a 2" insulating SiC substrate by metal organic chemical vapor deposition (MOCVD). The epilayer structure consisted of a 0.2-μm thick AlN layer, a 2-μm undoped GaN buffer, and a 200-Å AlGaN barrier layer. All the layers contained trace amounts of Indium to improve morphology and interface roughness. Sheet resistance mapping across the 2" wafer yielded an average sheet resistance of 297 ohms/sq., where the maximum was 357 ohm/sq. The fabrication was completed entirely at TriQuint Semiconductor Texas's facility. Each level was patterned using a stepper process, except for gates, which were exposed by e-beam. PECVD silicon nitride (Si_3N_4) was deposited to passivate the devices.

An average peak extrinsic transconductance G_m of 220 mS/mm and an average maximum drain current of 1 A/mm at a gate bias of 2 V were measured. Following Si_3N_4 deposition, a 5 to 10 % increase in peak G_m and a 15 % increase in drain current were observed. More importantly, the Si_3N_4 passivation layer was effective in reducing the surface effects that limit the RF current and voltage swing as the reduction in gate lag effect was observed. An output power density of 6.95 W/mm and a power-added-efficiency (PAE) of 42 % with an associated gain of 8.6 dB at a drain bias of 30 V were achieved at 10 GHz on a 200 μm device on this wafer.

Result and Discussion

DC Stress

DC stress tests were performed on-wafer at room temperature at 3 drain biases: 10, 15, and 18 V. The gate voltage was adjusted for each stressed device to achieve I_{DS} = 23 mA (~300 mA/mm). All devices were under constant V_{DS} and V_{GS} bias for a minimum of 40 hours, and both the drain and gate current were recorded every 5 minutes during stress. The gate length and width of all the devices in this study were 0.25 μm and 75 μm, respectively, and the source-drain spacing was 4 μm.

The change in I_{DS} as a function of stress time of 6 devices across the wafer was collected and shown in Fig. 1. Figure 1 (a) shows that some of the devices had an initial fast drop (or rise as in the V_{DS} = 18 V case) in drain current in the first 2 hours, then degraded very slowly after the initial hours. The drain current decreased by 1.9 % for V_{DS} = 10 V, while more significant changes of 6.8 % and 7.2 % were recorded for V_{DS} = 15 and 18 V after 24 hours of stress for the 3 devices shown in Fig. 1 (a). The devices that were stressed at higher voltages degraded faster due to the higher gate-to-drain field. In contrast to Fig. 1 (a), severe degradation of I_{DS} was observed of 3 other devices stressed at V_{DS} = 10, 15, and 18 V in Fig. 1 (b). For all 3 drain biases, the output current increased a few percent within the first half hour, then degraded rapidly during the entire stress duration of 48 hours. The % change in drain current of devices shown in Fig. 1 (b) was about 10 % after 24 hours. Based on the sampled data, some devices on the wafer appear to have "better" reliability than others even though the processing was identical.

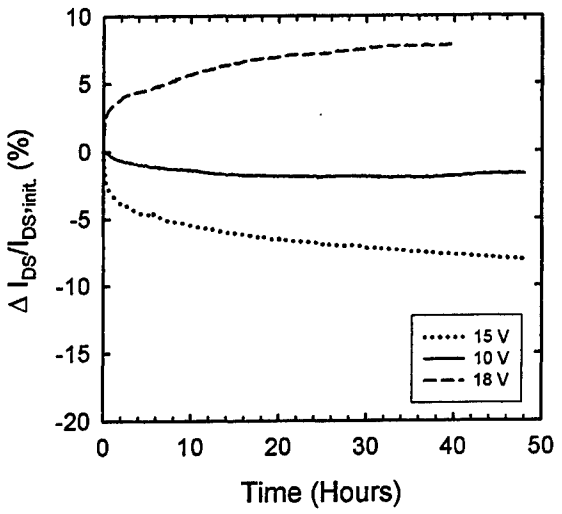


Figure 1 (a) Degradation of drain current as a function of stress time of 3 DC stressed devices with better reliability out of the total 6 stressed devices. Initial I_{DS} for all devices was 23 mA.

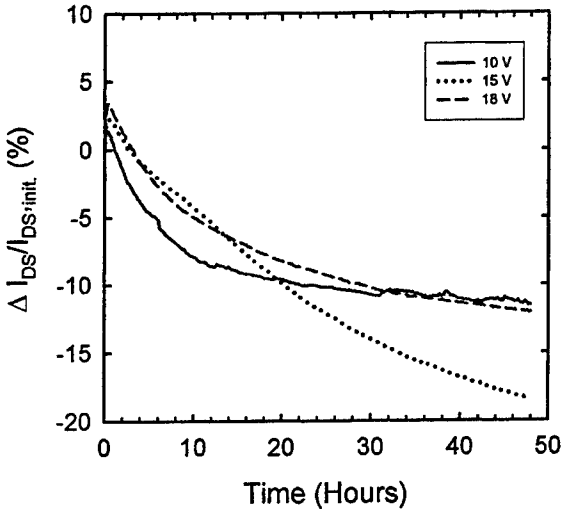


Figure 1 (b) Degradation of drain current as a function of stress time of 3 DC stressed devices that showed severe degradation of the total 6 stressed devices. Initial I_{DS} for all devices was 23 mA.

The I-V characteristics of all 6 devices were measured before and after stress. Drastic differences were noticed between the pre- and post-stress characteristics of the 3 devices shown in Fig. 1 (b), while surprisingly, negligible changes were observed between the "before" and "after" characteristics of the 3 devices shown in Fig. 1 (a). The I-V data of the device with "better" reliability that was stressed V_{DS} = 15 V is shown in Figure 2 (a). There was a slight decrease in I_{max} and peak G_m and a small positive shift of a few mV in threshold voltage. On the other hand, the effects of the DC stress were clearly evident in the devices that exhibited rapid degradation, and the comparison of the I-V characteristics of the device stressed at 18 V is shown in Fig. 2 (b) as an example. A small reduction in drain current at each corresponding gate voltage and reduction in transconductance in the saturation region is observed, and this change is also reflected in the positive shift in threshold voltage of 90 mV measured at V_{DS} = 20 V. At lower drain voltages, a significant increase in knee voltage and negative dip in G_m were evident. A transfer curve of I_{DS} vs. V_{GS} measured at lower drain voltages would show a "double hump" phenomenon in the transconductance. The higher on-resistance after stress suggests an increase in the drain resistance (R_D) and the channel resistance. This degradation in R_D has been attributed to the hot electron and impact ionization in AlGaAs/GaAs and InAlAs/InGaAs HFETs [4-6]. These effects may lead to an increase in surface charges at the high-field gate to drain region, which results in an increase in the depletion which generate a larger barrier for electrons to travel to the drain. The significant shift in knee voltage limits the lower end of the RF voltage swing and hence power performance of the transistor. The larger degradation in drain current, G_m, and an observed "kink" effect post stress are similar to the effects also seen in AlGaAs/GaAs HFETs [4]. Under high-field stress conditions, traps that are created capture electrons at the surface which may account for the large reduction in current and increase in resistance at the linear

region. At high drain bias of 20 V, electrons are released from the traps, therefore a small difference in current is measured before and after stress.

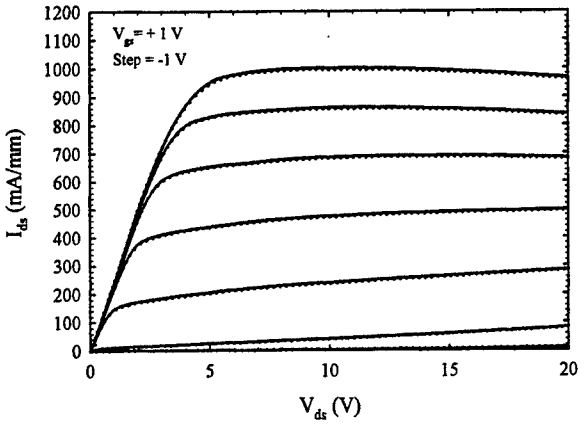


Figure 2 (a) I-V characteristics before (solid) and after (dotted) DC stress of one of the devices from Fig. 1 (a). This device was stressed at V_{DS} = 15 V.

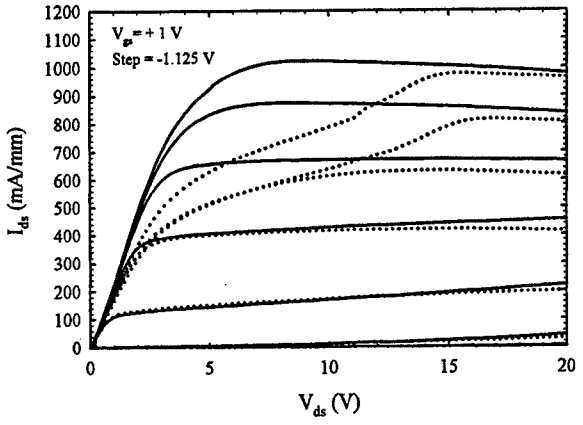


Figure 2 (b) I-V characteristics before (solid) and after (dotted) DC stress of one of the devices from Fig 1 (b). This device was stressed at V_{DS} = 18 V.

RF Stress

RF stress tests were also performed on 0.25 μm × 75 μm devices, which were biased under class AB condition at V_{DS} = 15 and 25 V. The load and source impedances were tuned for maximum output power (P_{out}) at peak PAE at 10 GHz. For each drain bias, the device was stressed at the input drive where the gain compression was > 5 dB and peak PAE is obtained. The degradation of P_{out} in dB and the change in drain current as a function of RF stress time for V_{DS} = 15 and 25 V are shown in Fig. 3. The initial measured output power was 23.9 dBm (3.2 W/mm) and 25.9 dBm (5.2 W/mm) at 15 and 25 V of drain bias, respectively. Under RF stress for 24 hours, P_{out} was reduced by 0.9 dB at V_{DS} = 15 V and by 1.3 dB at V_{DS} = 25 V, and the corresponding drain current degraded by 8 % and 13.2 %.

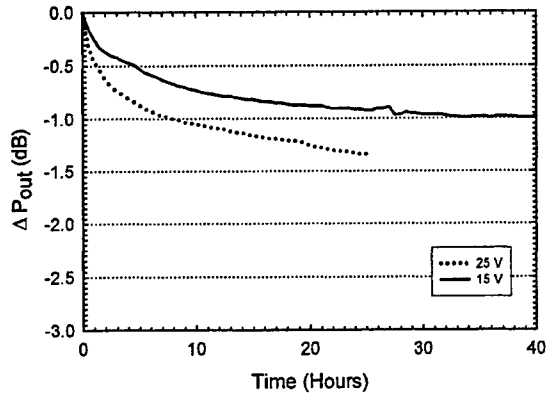


Figure 3 (a) Degradation of P_{out} as a function of stress time of 2 devices stressed at V_{DS} = 15 V (solid) and 25 V (dotted).

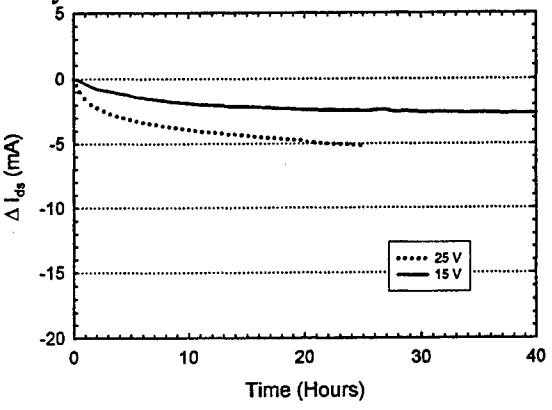


Figure 3 (b) Degradation of I_{DS} as a function of stress time of 2 devices stressed at V_{DS} = 15 V (solid) and 25 V (dotted).

Figure 4 compares the load-pull results at 10 GHz before and after RF stress at V_{DS} = 15 V and at the quiescent current of 23 mA. The power sweep results show that power, gain, and PAE are degraded compared to the before stress results. The peak PAE dropped from 48.7 % to 41.1 %, and the power degraded by 0.8 dB at that corresponding input power after 40 hours of RF stress at 5 dB gain compression. The degradation in power performance can be explained by the reduction in drain current and increase in on-resistance as shown in Fig. 5. The increase in gate leakage current was also observed. The threshold voltage shifted by 180 mV measured at a V_{DS} = 20 V; a larger change compared with the results of DC stress, due to a more significant reduction in I_{DS}.

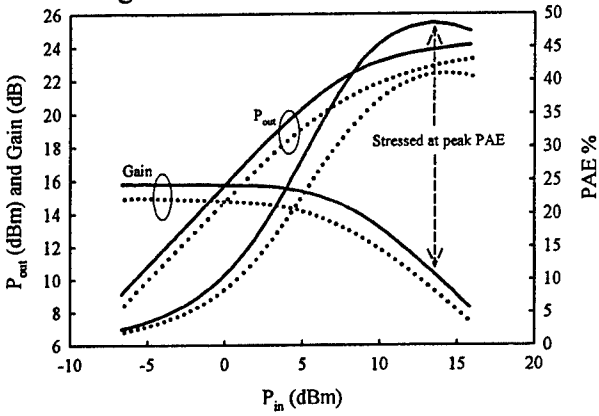


Figure 4 Load-Pull results before (solid) and after (dotted) RF stress at V_{DS} = 15 V

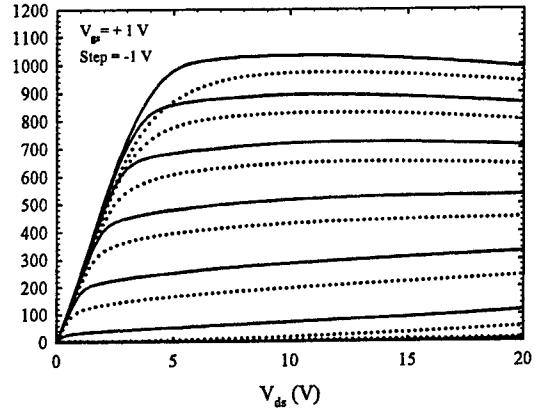


Figure 5 I-V characteristics before (solid) and after (dotted) RF stress at V_{DS} = 15 V

Discussion

On-wafer small signal S-parameter measurements were performed using an HP network analyzer from 0.1 to 40.1 GHz before and after DC and RF stress, and the change in equivalent circuit parameters and f_T and fmax are summarized in Table 1.

Stress Type	Stress V_{ds} V	Δ (R_g + R_i) Ω	Δ C_{gs} pF	Δ C_{gs}/C_{dg} pF	Δ g_m mS	Δ Tau pS	Δ R_s Ω	Δ R_{ds} Ω	Δ R_d Ω	Δ R_{sh} Ω	Δ F_t GHz	Δ F_{max} GHz
RF	15	1.25	0.004	1.19	-1.25	0.11	0.00	130.26	-1.46	4590	-3.10	0.89
RF	25	1.48	0.007	1.21	-0.33	0.16	0.00	120.62	-0.89	4366	-2.90	0.47
DC	10	-0.40	0.000	0.07	-0.29	-0.11	0.01	76.00	-0.12	-	0.00	0.06
DC	15	-0.13	-0.001	0.29	-0.51	-0.10	0.00	172.16	-0.28	-	-0.10	3.21
DC	18	0.58	0.002	0.42	-0.82	0.04	0.00	110.15	-0.72	-	-1.80	-2.72
DC	10	6.81	0.007	3.19	-5.46	1.10	0.08	732.64	-0.06	-	-10.00	-23.36
DC	15	5.90	0.031	5.88	-3.30	0.98	0.00	430.23	-0.93	-	-11.80	-21.58
DC	18	4.08	0.006	4.82	-3.50	1.03	0.14	565.00	-0.05	-	-6.80	-19.32

Table 1 Summary of the change in small signal equivalent circuit parameter before and after DC and RF stress.

The devices that were subjected to RF stress and the group of devices that had "better" reliability under DC stress (shaded rows in Table 1) showed a slight decrease in f_T due to the

small decrease in intrinsic g_m and slight increase in C_{gs}. As shown in the table, a rise of more than 100 Ω in the drain-to-source resistance (R_{ds}) was observed in these devices. The gate leakage current was modeled by the small shunt resistance (R_{sh}) at the gate terminal after RF stress. Notice that the last 3 entries in Table 1, which were extracted from the group of DC stressed devices shown in Figure 1 (b), exhibit severe degradation in each of the key parameters. Significant reduction in f_T and f_{max} are shown, which can be accounted for by the large decrease in g_m, increase in C_{gs}/C_{dg} ratio and in R_{ds}. The increase in R_D, which is modeled in series with R_{ds}, could not be deduced from S-parameter measurements; however, the impact of a larger R_D is evident in the increase in on-resistance and the reduced transconductance in the linear region in the I-V characteristics after stress. These effects revealed by the models correlate with the phenomenon induced by increased surface charge at the gate-drain region, which causes an increase in depletion and series resistance.

Conclusion

In this paper, the degradation characteristics of AlGaN/GaN HEMTs grown on SiC substrates under DC and RF stress was presented. The DC stress resulted in higher on-resistance, higher knee voltage, lower current and g_m. Small signal modeling showed an increase in R_{ds} and decrease in f_T and f_{max}. R_D and R_S, which are not sensitive enough to be extracted, need to be measured using the "end resistance" method. The degradation in power, gain, and PAE post RF stress can be attributed to the decrease in drain current, g_m, lower f_T, and a more leaky gate. These effects are similar to the phenomenon induced by high-fields at the gate-drain region in AlGaAs/GaAs HFETs.

Acknowledgement

This work is supported by Lockheed Martin Corporation.

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DYNAMIC LOADLINE ANALYSIS OF AlGaN/GaN HEMTS

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Abstract

Surface trapping has been identified as a mechanism for lower than expected output power for experimental AlGaN/GaN HEMT's devices. This paper presents dynamic loadline analysis as a means of understanding device behavior that limits large signal performance. From observations of measured data, a model for bias-dependent drain resistance caused by trap-induced space-charge in the un-gated region on the drain side of the gate is proposed. This bias-dependent drain resistance model is implemented in conjunction with a Curtice-cubic analytical transistor model to simulate the observed behavior.

I. Introduction

Aluminum Gallium Nitride/Gallium Nitride high electron mobility transistor (AlGaN/GaN HEMT) technology has established itself as a leading competitor for future high frequency, high power microwave applications. Results at several laboratories have shown especially promising results with both pulsed and CW power densities in the neighborhood of 10 W/mm [1], [2]. Innovations in growth and processing of the III-V nitrides are responsible for this remarkable progress. Reducing the influence of surface trapping effects in the devices has been found to be key to obtaining these record results. Previously it was found that Si_3N_4 passivation is key to realizing significant output power from the devices [3], [4].

This paper presents dynamic loadline analysis of state-of-the art AlGaN/GaN HEMT's under pulsed bias conditions and then develops a simple circuit model that gives insight into the effect that the device surface has on the RF on-resistance and hence power density of the devices. Using this model, the implications of device passivation on device on-resistance are explored. Finally, the results of the study are summarized in the context of the model predictions.

II. Device Technology and Pulsed RF Measurement System

The AlGaN/GaN HEMT's used for this study, schematically illustrated in Fig. 1, are grown by organo-metallic vapor phase epitaxy on 330 μm SiC substrates and processed as described elsewhere [5]. For these devices, the AlGaN barrier thickness is 200-250 Å and the aluminum mole fraction is 0.33. The charge in the channel is due to spontaneous and piezoelectric polarization– no intentional doping is employed in the structure. The processing of the device includes passivation by a 1000 Å Si_3N_4 as described in [3].

A dual CW and pulsed bias RF measurement system, was realized as shown in Fig. 2. Continuous wave bias or pulsed bias with widths down to 100 nS are supplied through the drain bias tee. A CW/pulsed RF input signal is supplied by controlling the signal source with the Microwave Transition Analyzer (MTA). The MTA also sends a trigger signal to the HP 214 B pulse generator to synchronize it with the RF input pulse. The pulsed experimental data presented here uses 500 nS pulse widths with a 1% duty cycle. These short pulse lengths and duty cycles prevent heating of the device when in operation. An algorithm based on Fourier analysis of the signals read by the MTA is used to extract the dynamic loadline of the device [6].

III. Dynamic Loadline Analysis of State-of-the-Art Large Periphery Devices Under Pulsed Bias Conditions

Figure 3 (a) shows saturation characteristics as a function of drive for a $10\times150\times0.25\mu m^2$ AlGaN/GaN HEMT at $V_D = 40$ V, $V_G = -3.75$ V under pulsed RF measurement conditions at 8 GHz. Here a total

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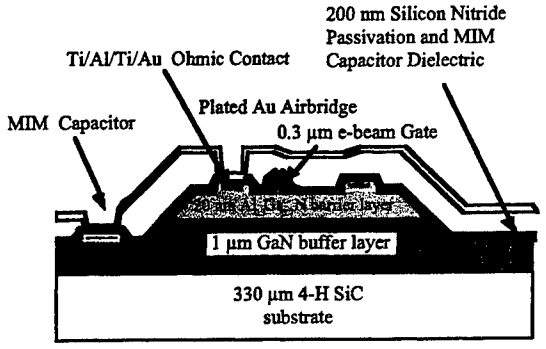


Fig. 1. Cross-section schematic of AlGaN/GaN HEMT device process used in this work.

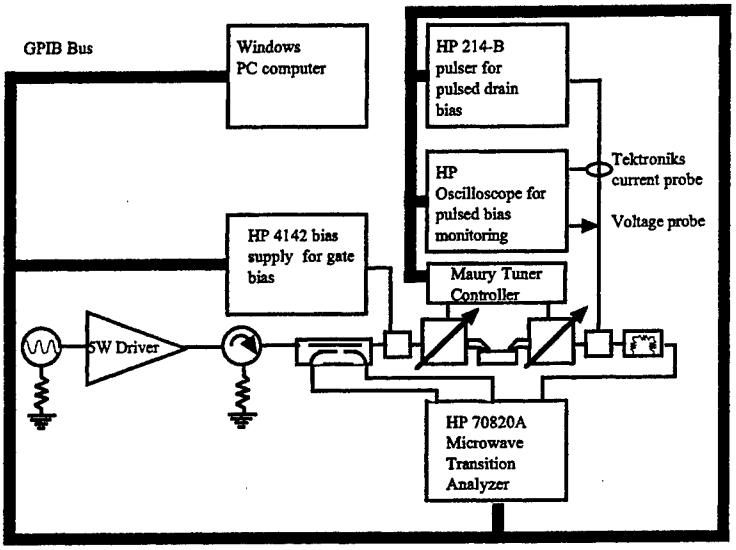


Fig. 2. Block diagram of CW/pulsed RF loadpull system used to collect data presented in this chapter.

output power of 14.1 W with an associated PAE of 43% is achieved. While this electrical result is on par with some of the best results reported in the literature, an examination of Fig. 3 (b) showing measured dynamic loadlines corresponding to this power sweep superimposed on DC I-V curves shows that at 40 V the RF knee voltage of the device does not reach the DC knee voltage causing some degree of pre-mature gain compression. Figure 4 shows dynamic loadlines for this device taken as a function of bias at a constant load impedance of $Z_L = 19 + j16$. These loadlines plotted as a function of V_{DS} indicate that the RF on-resistance of the device increases with increased drain bias. Since self-heating is negligible due to the pulsed bias conditions, surface traps are the main contributor to this undesirable behavior. The next section develops a model for this bias-dependent on-resistance that describes the effect.

IV. Large Signal Description of Trapping Effects

The dynamic loadline data presented in the previous section point to the push-out of the RF knee voltage with increasing bias as the main factor limiting the large signal operation of the devices. Surface-related trapping pushes the microwave knee voltage approximately 10 V beyond that of the DC knee voltage. Because of this, the power, linearity, and PAE of the device suffer immensely. Intuitively, one

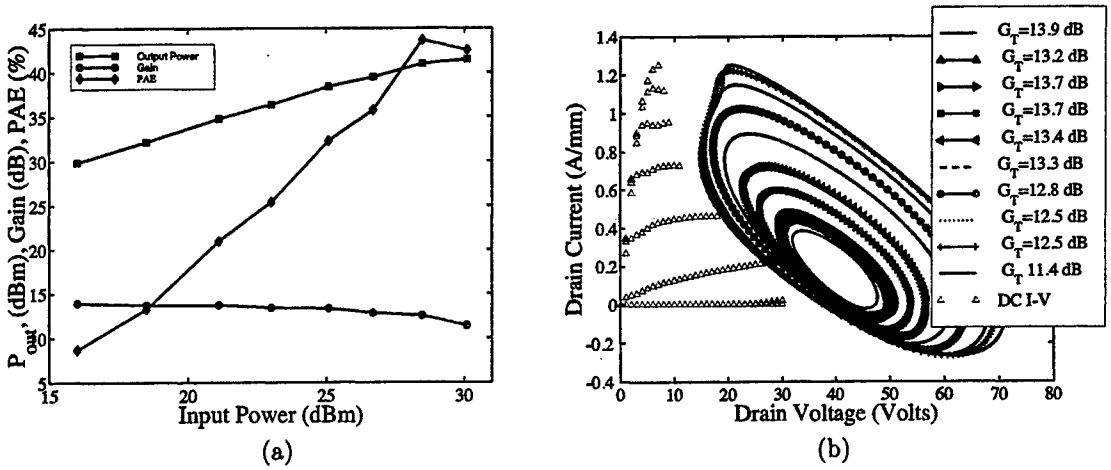


Fig. 3. (a) Output Power as a function of drive power and (b) corresponding dynamic loadlines at 8 GHz for 0.25 x 1500 μm^2 HEMT device biased at $V_D = 40$ V, $V_G = -3.75$ V. DC $I-V$ curves measured on a 0.25 x 250 μm^2 HEMT with $V_{G,top} = +2$ V and $V_{G,step} = +1$ V.

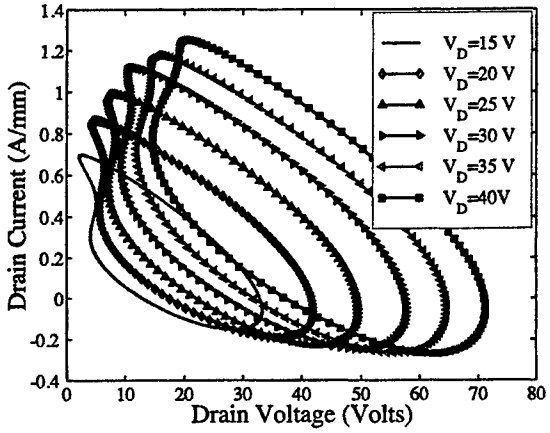


Fig. 4. Dynamic loadlines at 8 GHz as a function of bias for 0.25 x 1500 μm^2 HEMT device. Each dynamic loadline is measured at 2-3 dB gain compression.

may reason that the drain resistance of the device at microwave frequencies is much higher than that of the static case. This section builds on this idea and extends the analytical large signal model of [7] to include the effect of a bias-dependent parasitic drain resistance due to traps.

Previously, a model suggesting such an increase in drain resistance for MESFET's was proposed [8]. However, this early model was not used for calculations of the RF voltage and currents. The model presented here employs a space-charge limited current flow approximation to model the bias dependence of the drain resistance due to electron trapping. The model is validated using measured 8 GHz CW dynamic loadlines from passivated and unpassivated devices. The model gives further insight into the role that passivation has in reducing the length of the space charge region in the gate drain region thereby lowering the microwave drain resistance. The model is first developed in the context of an unpassivated device where trap effects are quite severe. The model is then applied to the case of a passivated device.

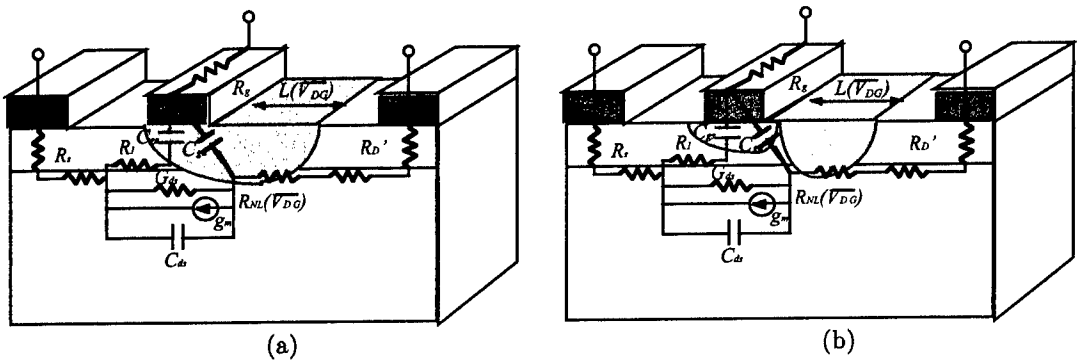


Fig. 5. Small signal equivalent circuit superimposed on device structure showing the effect of surface state depletion on R_D for cases of an applied gate bias pulse (a) off-state and (b) on-state.

A. Effect of Traps on Large Signal On-Resistance

Figure 5 qualitatively illustrates the geometry of a HEMT and the gate-drain region of the device responsible for the increase in microwave drain resistance. As shown in Fig. 5 (a), under static bias conditions at or close to pinch off in the off-state, the device is depleted not only in very close proximity to the gate, but is also depleted a distance L along the ungated region of the device. As shown in conductance DLTS analyses of both GaN [9] and GaAs devices, [10], hole-like traps are responsible for DLTS signals corresponding to the ungated regions of the device. This means that in very close proximity to the gate on the drain side, the device operates as it should with the depletion region under the gate changing nearly instantaneously when the applied gate bias instantaneously changes from pinched off conditions to the on-state as shown in Fig. 5 (b). In this case, the depletion region in the un-gated region does not respond as would be the case for large signal microwave operation. In general, there are several trap time constants present in the structure ranging from nanoseconds to seconds [11], [12]. Here we restrict ourselves to the effect that these traps have on the microwave performance of the device; a full discussion of the physics and characterization of deep levels [13] goes far beyond the scope of this work. It suffices to say that once the DC bias conditions set up a particular trapped electron distribution on the surface, it remains constant during steady state operation.

B. Development of Model

The two-dimensional nature of the HEMT device makes exact analytical solutions describing the effect of traps on the large signal current-voltage characteristics impossible. For the development of the model,the following assumptions are used:

(1) The extension of the high-field region next to the gate, due to electron trapping, sets up an extnded space charge region that impinges on the area of the device one normally associates with the drain resistance of the device as shown in Fig. 5. However, a large change in the *microwave* value of R_D goes un-noticed in both the DC or small signal responses since the traps causing the space charge region can respond to the DC bias. Furthermore, a change in R_D does not affect the small signal gain as shown by the relationship for G_{max} given by

$$G_{max} \approx \frac{(f_T/f)^2}{4[\pi f_T c_{gd}(\Sigma r + 2\pi L_S) + g_{ds}(\Sigma r + \pi f_T L_s)]} \tag{1}$$

where $\Sigma r = R_s + R_g + R_{gs}$.

Since the transport of electrons through the region of the device denoted R_{NL} in Fig. 5 is dominated by space-charge limited current flow [14], [15], a current law appropriate for the planar geometry of the problem must be used. To this end, a thin slab geometry as shown in Fig. 6 is used to model R_{NL}. The space charge limited current flow model that will be used here considers transport in a thin film $n^+ - i - n^+$ diode having the same geometry as Fig. 6. The vertical dimension, D, of this region is considered to be vanishingly thin compared to the lateral dimension, L. The linear current density in the thin film limit having units of amperes/cm takes the form [16], [17]

$$J = \frac{4\epsilon_s v_{sat} V}{\pi L(V)}. \tag{2}$$

From this relationship, the resulting expression for the bias-dependent component of the drain resistance, R_{NL}, takes the form

$$R_{NL} = \frac{V_{dg}}{JW} = \frac{\pi L(\overline{V}_{dg})}{4\epsilon_s v_{sat} W} \tag{3}$$

where W corresponds to the gate width and $\overline{V}_{dg}$ refers to the static drain-gate bias.

(2) Based on the arguments on the frequency response of the traps, it is assumed that the extended space charge region has a fixed extent for a given bias in steady state operation. From one-dimensional junction theory, the bias dependence of $L(\overline{V}_{dg})$ is approximated as [18], [19]

$$L(\overline{V}_{dg}) = \gamma_L \sqrt{1 + \frac{\overline{V}_{dg}}{\phi_b}} \tag{4}$$

where γ_L refers to the zero-bias depletion length due to traps while, ϕ_b represents the built-in potential of the heterojunction.

(3) In active-bias operation, carriers entering the space-charge region near the gate edge are accelerated by an electric field greater than the critical field of 300 kV/cm and are therefore assumed to be at a saturated velocity of 1×10^7 cm/s.

Using the assumptions implicit in (1)-(3), the nonlinear dependence of R_D with drain bias is treated by partitioning R_D into two sections corresponding to the extended space charge region near the gate denoted by R_{NL} and R'_D which combines the resistance remaining undepleted portion of the device with the ohmic contact resistance, R_c. Figure 5 exhibits this partitioning in terms of the physical device structure with the associated equivalent circuit elements. Therefore R_D takes the form

$$R_D \approx R_{NL} + R'_D \tag{5}$$

where R'_D is the value of the drain resistance taken from cold FET measurements. This relationship is approximate due to the fact that changes in the extent of the space charge region decrease R'_D. However, as will be shown, R_{NL} has a much larger value at typical operating points making the approximation a good one.

C. Incorporation into Large Signal Model and Comparisons to Continuous Wave Measurements

The model for the nonlinear drain resistance was combined with a large signal model [7] to show the effects of the variable-length space charge region on output power and efficiency. The results of the extraction are shown in Table I. To make use of the bias-dependent model for R_{NL} described above, the following procedure is used to obtain the correct value of γ_L for the devices studied. This procedure consists of (1) measuring dynamic loadlines at several bias points and (2) selecting a value of γ_L that yields the best overall prediction of the measured results. Figure 7 compares the dynamic loadline obtained from an unpassivated $2 \times 125 \times 0.25$ μm^2 at $V_D = 30$ V with results calculated from the large signal model

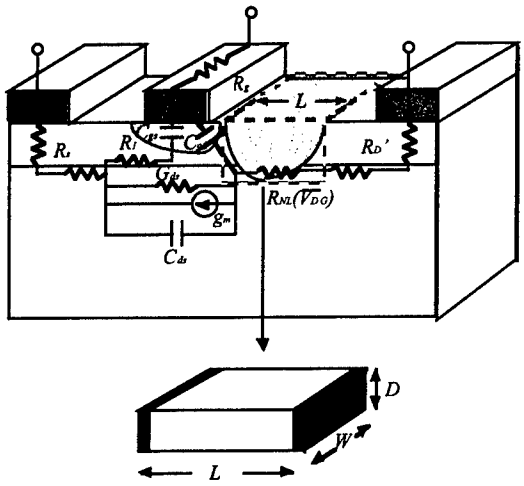


Fig. 6. Thin film geometry valid for the space charge limited current law of Eq. (2).

under the same bias and loading conditions. Under these conditions, an output power density of 3 W/mm was measured. For this case, the result of Fig. 7 where $\gamma_L = 0$ (no trapping) shows a gross overestimate of the output power at 8.6 W/mm. Setting $\gamma_L = 300$ Å, the model predicts a more reasonable value of 2.8 W/mm. Here, the length of the space charge region, L, was estimated to be 0.15 μm. Reported values for the length of this depletion region from actual measurements on unpassivated devices vary between 0.2 μm and 0.5 μm for comparable biases [20], [21] . The fact that the calculated value of L is comparable to physical measurements of depletion regions in un-passivated AlGaN/GaN HEMT's lends additional validity to the model assumptions. In addition, intuition gained from using $L(\overline{V}_{dg})$ as a measure of the space charge region at the gate edge is beneficial for understanding the impact of traps on microwave performance and optimizing the devices accordingly.

Figure 8 shows the dependence of R_D on V_{DS} in Ω-mm for the case of $\gamma_L = 300$ Å. As the plot shows, at $V_D = 30$ V, R_{NL} takes a value of approximately 16 Ω-mm (64 Ω for 0.25 mm device). Table I shows that this value is an order of magnitude larger than the R_D extracted using cold FET methods, clearly explaining the clamping of the microwave current and voltage swing. Leaving γ_L fixed at a value of $\gamma_L = 300$ Å, results for $V_D = 20$ V, and 25 V were also run and compared to the case of $\gamma_L = 0$ (no trapping) as summarized in Fig. 9.

The comparison of the measured and modeled data in Fig. 9 shows that the large signal model is grossly inaccurate unless modification is made to include the bias-dependent space charge length effect on R_{NL} by giving a non-zero value to γ_L. The figure shows relatively good agreement between the measurement and simulation results when the traps are accounted for.

D. Effect of Passivation

As was shown previously, Si_3N_4 passivation has a profound influence on the power density achieved by the devices [3]. Figure 10 shows again the comparison of dynamic loadlines for passivated and unpassivated devices this time with predictions from the model laid on top of the measured dynamic loadlines. In the case of the unpassivated result, γ_L again takes the value of 300 Å. However, to obtain agreement with the case of the passivated device, γ_L takes a value of 140 Å. This decrease in the zero-bias depletion length, γ_L, corresponds directly to a decrease in L under static bias conditions and therefore a reduction of the microwave drain resistance, R_D from 14 Ω-mm to 7 Ω-mm as shown in Fig. 11.

TABLE I

CURTICE-CUBIC MODEL PARAMETERS AND EQUATIONS FOR PASSIVATED $2 \times 125 \times 0.25$ μM^2 ALGAN/GAN HEMT (EQUATIONS AFTER [7], [22], [23]).

Current Control Equation $I_{DS} = (A_0 + A_1V_1 + A_2V_1^2 + A_3V_1^3)\tanh(\gamma V_{out})(1 + \lambda V_{out})$						
A_0	A_1	A_2	A_3	γ	λ	β
0.267	0.0284	-0.00244	0.00024	0.986	1×10^{-6}	0.001

Device Resistances						**Diode Param.**	
R_G	R_{GS}	R_{DSO}	R_C	R_S	R_D	ϕ_{bi}	I_S
3.75 Ω	0.92 Ω	310 Ω	1 kΩ	3.3 Ω	5.3 Ω	1.5 V	1×10^{-6} A

Device Capacitances at V_{DS0}, V_{GS0}				Device Delay	g_m Dispersion
C_{GS0}	C_{GD0}	C_{DS}	C_{RF}	τ	$g_{m,RF}/g_{m,DC}$
$0.27pF$	0.032 pF	0.053 pF	1 μF	1.25 pS	1.24

Nonlinear Capacitance Equations $C_{GS} = C_{GSO}\frac{1+c_vV_{out}}{1+c_vV_{DSO}}\frac{1+f_{c1}\tanh[f_{c2}(V_i+v_{fcg})]}{1+f_{c1}\tanh[f_{c2}(V_{GSO}+v_{fcg})]}$ $C_{GD} = C_{GDO}\frac{1-fc3\tanh(f_{c4}V_{out})}{1-fc3\tanh(f_{c4}V_{DSO})}$							
f_{c1}	f_{c2}	f_{c3}	f_{c4}	c_v	v_{fcg}	V_{DSO}	V_{GS0}
0.42	2.68	0.79	0.15	.0083	5.72	10 V	-3.5 V

Nonlinear Drain Resistance		
v_{sat}	ϕ_b	ϵ_s
1×10^7 cm/s	1.5 eV	8.9

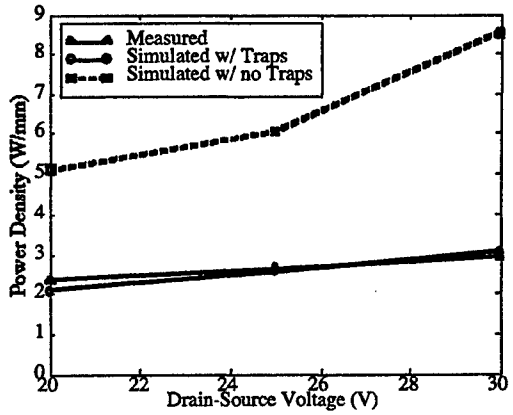


Fig. 9. Measured and simulated 8 GHz power densities for a 0.25×250 μm^2 un-passivated HEMT as a function of bias comparing the cases of calculations with and with out the inclusion of R_{NL}.

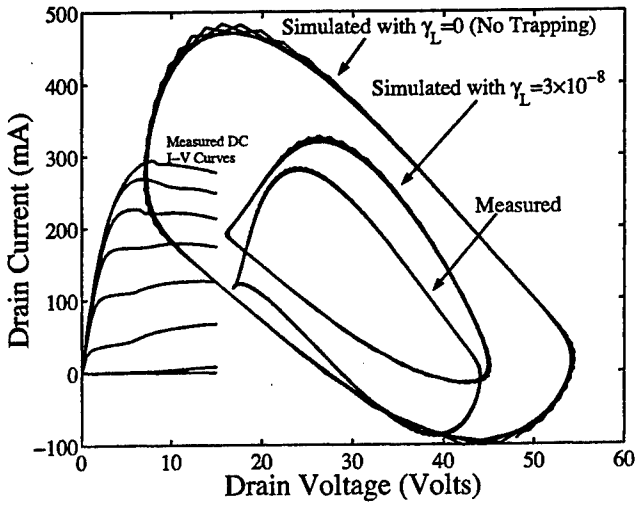


Fig. 7. Measured and simulated 8 GHz loadlines for a 0.25 x 250 μm^2 un-passivated HEMT at V_D= 30 V comparing the cases of calculations with and with out the inclusion of R_{NL}.

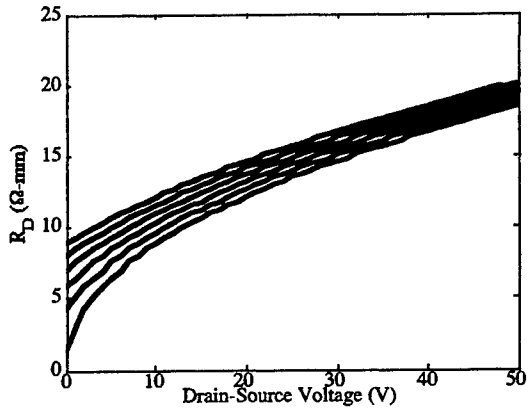


Fig. 8. Value of R_D vs. V_{DS} for $V_{GS} = -8 - +2$ V for un-passivated device results in steps of +2 V simulated using large signal model.

However, as the figure indicates, the passivation still does not allow the microwave voltage and current to swing to the DC knee. Therefore the increase in power from 2.65 W/mm to 4.5 W/mm still falls somewhat short of the output power that should be realized at this drain bias. In fact, the simulations of Fig. 9 suggest that with no trapping, a power density greater than 6 W/mm should be able to be realized at $V_D = 25$ V. Other work using this device process has shown such power densities at a 25 V drain bias [1]. For this to be done consistently, however, additional maturity is still needed in the process technology to control the surface. One improvement may include a gate recess in conjunction with an undoped GaN layer in the un-gated region to move the surface/interface states further from the channel and prevent the walk-out of the knee voltage. Another would be to have the passivation act as a protective dielectric cap layer over the surface during ohmic contact annealing.

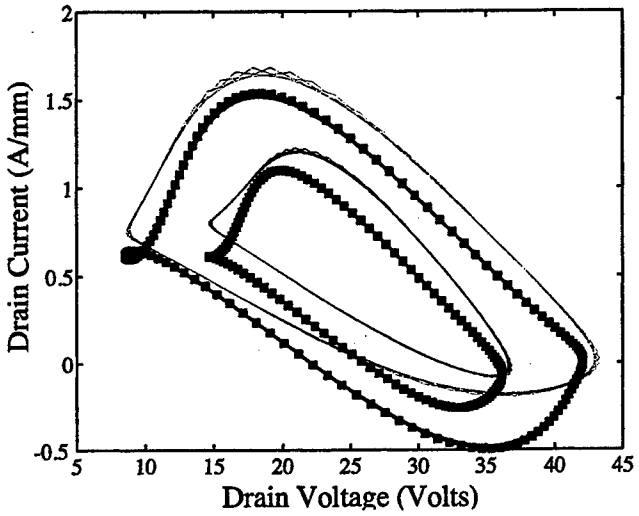


Fig. 10. Comparison of calculated (lines) and measured (squares) 8 GHz loadlines on 0.25 x 250 μm^2 HEMT at V_D=25 V, V_G=-2.5 V showing the improvement in voltage and current swing with passivation.

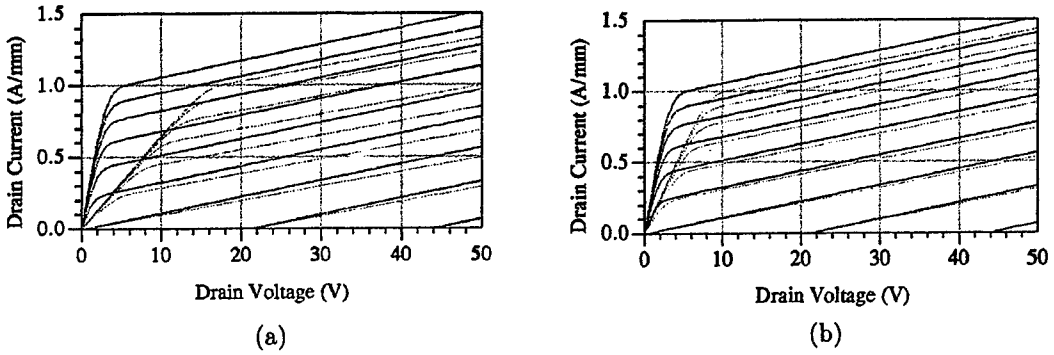


Fig. 11. Comparison of simulated DC I-V curves (solid) to transient I-V curves (dashed) corresponding to (a) un-passivated (b) passivated AlGaN/GaN HEMT of Fig. 10 taken at a static bias point of V_D = 25 V, V_G = −2.5V showing the change in microwave on-resistance with passivation.

V. Conclusion

This paper has discussed dynamic loadline analysis of AlGaN/GaN HEMT's. It is seen through the model for the bias-dependent drain resistance that the growth of the gate extension degrades the RF knee voltage as the bias is increased. Passivation was seen to have a tremendous effect on the large signal performance of the devices. In the future, structures grown on lattice-matched materials with fewer defects, gate recesses will help reduce the negative effects assoicated with surface, interface, and bulk traps.

Acknowledgements

The authors would like to acknowledge W.R. Curtice, W. R. Curtice Consulting for donation of a CFET model package and C. Weitzel, Motorola for helpful discussions. This work was supported under ONR MURI Contract N00014-96-1-1223 at Cornell Univ., monitored by Dr. John Zolper.

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Characterization and Analysis of Gate and Drain Low-frequency Noise in AlGaN/GaN HEMTs

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Abstract

The gate and drain low-frequency noise (LFN) characteristics of 0.15×200 μm^2 AlGaN/GaN HEMTs are reported. The measured gate noise current spectral density is low and insensitive to the applied high reverse bias voltage between the gate and the drain. Typical gate noise level values vary from ~ 1.9×10^{-19} to ~ 3.4×10^{-19} (A^2/Hz) as the drain voltage increases from 1 V to 12 V (V_G= -5V) at 10 Hz. The calculated Hooge parameter is ~ 5.9×10^{-4}, which is comparable to traditional III-V FETs. Lorentz noise components were observed when V_{DS} is higher than 8 V. The peak of Lorentz component moves toward higher frequency when V_{DS} increases and V_{GS} decreases. The exponent γ of the $1/f^{\gamma}$ was found to reduce from 1.17 to 1.01 when V_{DS} increases from 8 V to 16 V. The observed trends are discussed in terms of electric field, carrier velocity and trapping-detrapping considerations.

I. Introduction

GaN-based HEMTs have demonstrated excellent microwave power and noise characteristics [1]. The low-frequency noise (LFN) characteristics of these devices have also attracted significant attention since LFN can be upconverted to microwave frequencies in nonlinear circuits and may lead to circuit performance degradation. In addition, LFN often originates from defects and traps and can be a useful tool to diagnose problems of materials and technologies. LFN and deep-level traps have been reported for GaN-based HEMTs [2], [3]. There is, however, still a need for better understanding and analysis of LFN mechanisms in AlGaN/GaN HEMTs. This paper presents a systematic study of LFN in such devices. Submicrometer gate AlGaN/GaN HEMTs were characterized for both gate and drain noise characteristics under different bias conditions. Section II describes the layer structure and the device DC and microwave characteristics. Section III presents the experimental results of both the gate and drain noise current characteristics. The bias dependence and the origin of LFN were also investigated. Section IV discusses the observed trends of LFN in AlGaN/GaN HEMTs and compares different models.

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II. DC and Microwave Characteristics

The AlGaN/GaN HEMTs tested were grown by RF-assisted MBE on 4H-SiC substrates. An undoped GaN buffer layer was grown on top of the substrate, followed by an undoped AlGaN spacer, an AlGaN barrier layer, and an undoped AlGaN cap layer. The measured device had a gate length of 0.15 μm and a total gate periphery of 200 μm. The peak transconductance was ~ 280 mS/mm and the maximum current capability was ~ 1 A/mm. Typical DC *I-V* characteristics of the device are shown in Fig. 1. The pinch-off voltage of the device is ~ -5.5 V. The positive slope of the *I-V* characteristics in the saturation region results from short-channel effects, which lead in a reduced output resistance. The presence of finite output resistance needs to be considered, and a correction factor was used when calculating the drain noise current from the measured drain noise voltage. Fig.2 shows the maximum oscillation frequency (f_{max}) and cut-off frequency (f_T) under various bias conditions. As can be seen, the maximum oscillation frequency (f_{max}) and cut-off frequency (f_T) were ~ 75 GHz and ~ 50 GHz, respectively.

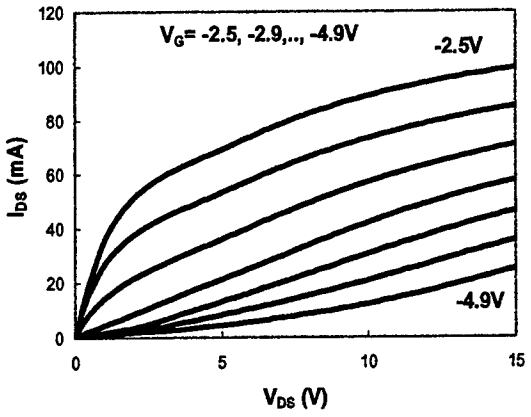


Fig. 1: DC *I-V* characteristics of the investigated 0.15× 200 μm^2 AlGaN/GaN HEMTs.

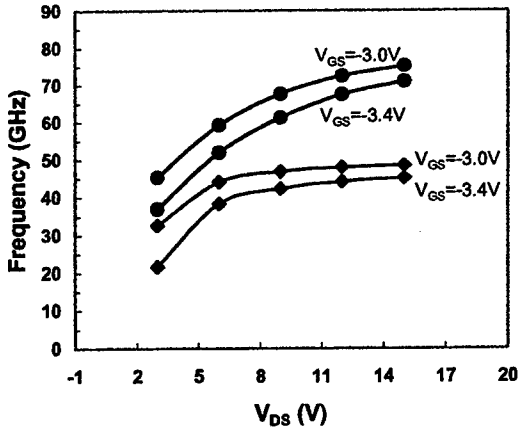


Fig. 2: Maximum oscillation frequency (f_{max}) and cut-off frequency (f_T) under different bias conditions.

III. Low-frequency Noise Characteristics

On-wafer LFN characterization was performed using an in-house developed measurement system. Microwave probes and bias-Tees were used to provide consistent contact and reduce the possibility of oscillation at low frequencies. Batteries were used for biasing to reduce undesired noise sources from the power supply. A low-noise amplifier (LNA) with a gain of ~ 60 dB was used to increase the signal level and an HP3561A analyzer with a high dynamic range was used to collect data. The gate noise was measured when the drain terminal is AC grounded, while the drain noise was measured when the gate terminal is AC grounded. Measurements were performed from 10 Hz to 100 kHz with automatic computer control. The system was calibrated using resistors from their thermal noise values and was placed in a Faraday cage to minimize interference from the environment.

The gate noise current spectral density was first examined under a wide range of bias conditions. Fig. 1 shows the results obtained when the device is biased in the saturation region (V_{DS}= 12 V) under different gate voltages. The gate noise level increases as the gate-drain reverse bias increases due to the increased gate leakage current. The gate noise level changed from 1.93×10^{-19} A^2/Hz to 3.42×10^{-19} A^2/Hz when the drain voltage increased from 1 to 12 V under V_{GS}= -5 V.

The small dependence of the gate noise current on the drain bias voltage can be explained using the Schottky diode noise model. Under reverse bias conditions, the major low-frequency noise source in a Schottky diode is generation-recombination (G-R) noise current originating from the space-charge-region (SCR) and can be associated with the gate leakage current. As a result of the wide bandgap AlGaN layer used as barrier, the gate leakage current increases only slightly even under strong gate-drain reverse-bias conditions. This results in small gate noise current levels and characteristics insensitive to gate-drain reverse bias even under pronounced bias conditions. Measurements of the gate leakage current showed that I_g only increased from ~ 0.2 to ~ 0.5 μA when V_{DS} increases from 1 to 12 V under V_{GS}= -5V, which is consistent with the LFN results. In addition, the small gate noise variation even under a large change of V_{DS} suggests that the devices can be used for large-signal applications with low gate noise level.

Fig. 4 shows the normalized drain noise current spectral density for the devices biased in the linear region (V_{DS}= 0.5 V) as a function of effective gate voltage. The result shows that S_{Id}/I_D^2 reduces monotonically when the effective gate voltage increases. Similar characteristics have been observed in AlGaN/GaN HEMTs from other researchers, and were explained by the screening effect from the high electron density in the channel [4]. When the devices operate close to open-channel conditions, the sheet carrier density increases and Coulomb interaction between scattering centers and channel carriers reduces due to high carrier concentration screening effects. As a result, the electron mobility increases resulting in a reduced noise level. On the contrary, when the devices operate close to pinch-off conditions, the scattering mechanism is enhanced, and a higher noise level was observed.

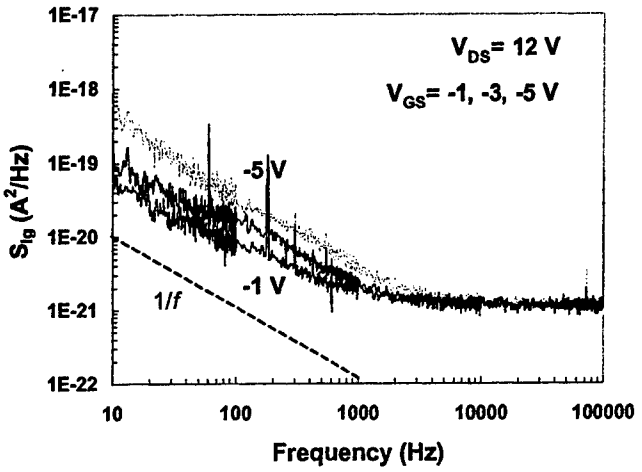


Fig. 3: Gate noise current spectral density of AlGaN/GaN HEMTs biased in the saturation region.

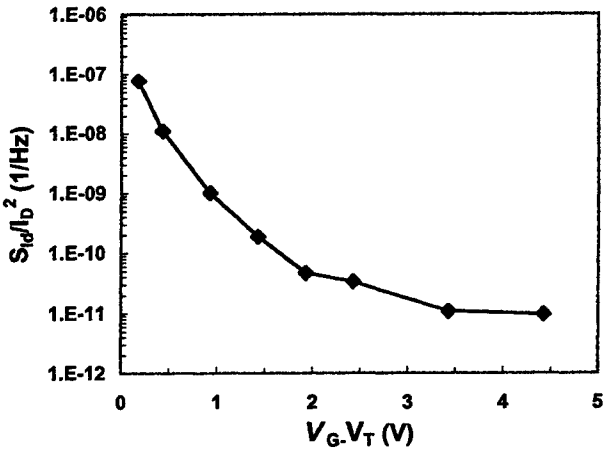


Fig. 4: Normalized drain noise current spectral density for 0.15×200 μm^2 AlGaN/GaN MODFETs at 10 Hz. The drain voltage is 0.5 V.

The Hooge parameter can be calculated using the following equation:

$$\alpha_H = \frac{S_{Id}}{I_{DS}^2} f N \tag{1}$$

where f is the frequency, N is the total number of carriers. I_{DS} is the drain-source bias current and f is the frequency. The calculated α_H values were 5.9×10^{-4} under V_G= 0 V and V_{DS}= 0.5 V. The obtained values are comparable to those reported in [2] for AlGaN/GaN MODFETs, where $\alpha_H \sim 10^{-4}$ were found under different gate bias voltages.

The obtained values are also close to traditional III-V based FETs, which are normally in the range of ~ 10^{-4} to 10^{-5} [5].

Fig. 5 shows the drain noise current spectral density under various drain voltages. The device presents clear $1/f^{\gamma}$ characteristics with $\gamma \sim 1.05$ under low drain bias conditions. However, one can see "bulges" appearing in the $1/f$ characteristics as V_{DS} increases. The bulges shown in the $1/f$ noise characteristics originate from trapping-detrapping and/or generation-recombination (G-R) processes and are often referred to "Lorentz components". As can be seen, the Lorentz components are only present at high drain voltages. It is therefore reasonable to associate the appearance of bulges to the strength of the applied electric field. Under high V_{DS}, the electric field along the submicrometer-gate channel can become extremely high. For example, the electric field can reach ~ 6.67×10^{7} V/m at V_{DS}= 10 V for a device with L_g= 0.15 μm. Under such conditions, the carriers may become very energetic, and the trapping-detrapping and G-R processes may be enhanced. Since these processes are very noisy, the Lorentz components become more pronounced. In addition, the observed noise spectral densities show a small curvature, which indicates that the noise occurs from traps with a broad distribution in time constants.

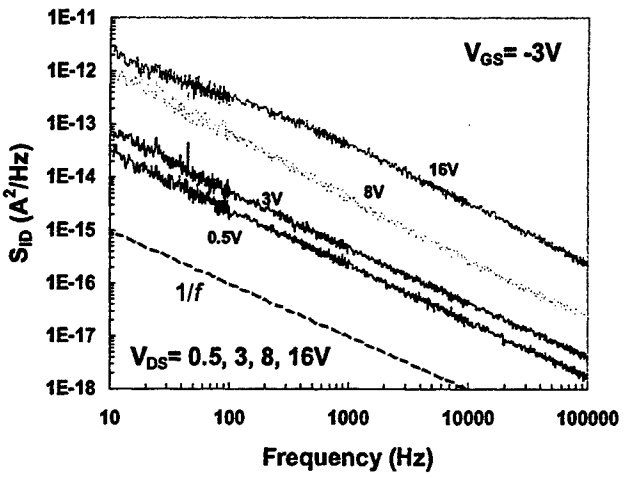


Fig. 5: Drain noise current spectral densities of AlGaN/GaN HEMTs under different drain voltages.

Fig. 6 shows $S_{Id}(f)\times f$ as a function of frequency at V_{GS}= -3V and under different drain voltages. This representation makes a better distinction between the Lorentz components and the $1/f^{\gamma}$ characteristics. The results show noticeable bulges and their peaks move toward higher frequencies as V_{DS} increases. In addition, measurements also show that the peak of Lorentz components move toward higher frequencies when V_{GS} becomes more negative. This can be explained using the modified carrier density fluctuation model, which has been applied to explain LFN characteristics in MOSFETs [6]. The SiO_2/Si structure in MOSFETs can be assumed to be analogous to the AlGaN/GaN structure of the devices under study and therefore a similar theory may be applied. As the drain voltage increases, the band-bending near the drain end between gate and drain reduces. As a result, carriers encounter an increased number of effective

traps and reduced carrier-tunneling distance. The latter is due to relatively smaller band-bending which in case of tunneling into the AlGaN spacer leads in less time required for the trapping-detrapping process. Based on this consideration, the bulge peaks are expected to move toward higher frequencies. A similar explanation can be applied to the dependence of the bulges on V_{GS}.

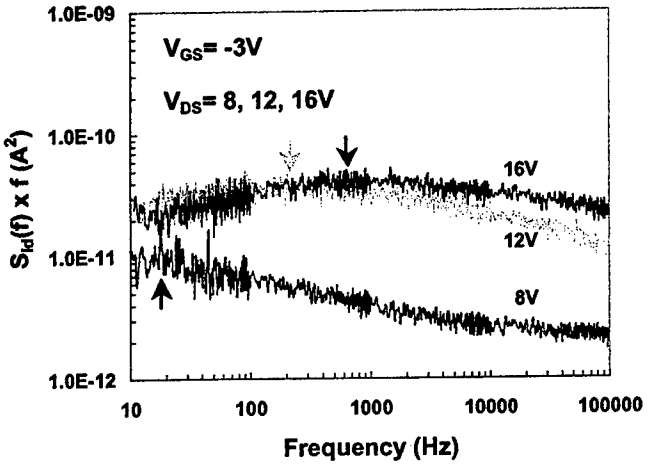


Fig. 6: Product of drain noise current spectral densities and frequencies under different drain voltages.

Fig. 7 shows the bias dependence of γ in saturation region. The γ values were extracted using the $S(f)= A/f^{\gamma}$ equation to fit the measured data, where A is a constant. The device presents a clear trend of reduced γ as the drain voltage increased. γ was found to reduce from 1.17 to 1.01 when V_{DS} increases from 8 V to 16 V. As noted already, the increased drain bias results in relatively smaller band-bending. The time constant needed for the trapping-detrapping process is consequently shortened and a higher noise power appears in the high frequency region, leading in reduction of the γ exponent. Results on the dependence of γ on the bias have already been reported. Balandin *et al.* [2] found for example, that γ decreases from ~ 1.3 to ~ 1.0 when V_{GS} decreases from 0 V to - 6 V. The observed results can also be interpreted using the modified carrier density fluctuation model with band-bending variation as discussed in the next section.

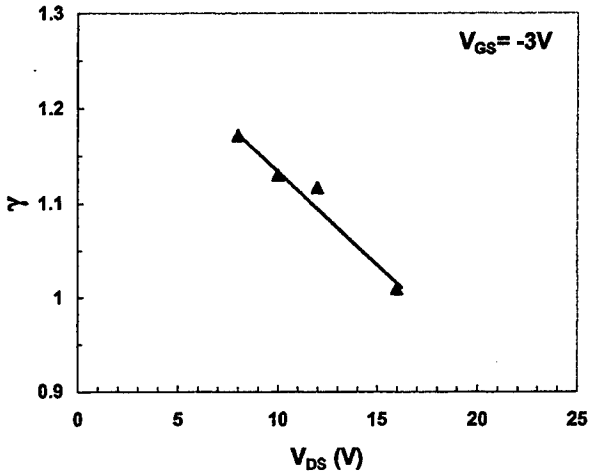


Fig. 7: Dependence of the exponent γ of the $S_{Id}(f)$ $1/f^{\gamma}$ characteristics on V_{DS}. γ reduces when V_{DS} increases.

IV. Discussion

Although the number fluctuation theory provides a more intuitive approach to explain the observed experimental results, the mobility fluctuation model with the activation energy and temperature related time constant can also be used to interpret the experimental results of this work. Ho *et al.* [7] suggested that the dependence of γ on V_{GS} observed in AlGaN/GaN MODFETs is due to the change of trap energy level with respect to the Fermi level in the device, which leads to variation of activated traps in the devices. As a result, the trapping time constants and γ change. γ could increase or decrease depending on the actual distribution of the traps in both real space and energy levels. The number fluctuation model with trapping time constant depending on band-bending appears to be applicable in explaining the experimental results in this study. However, since the trapping time constant is only a function of tunneling distance, this theory is insufficient to describe the $1/f^{\gamma}$ characteristics under different temperatures. On the other hand, the mobility fluctuation model used in [7] where the trap time constants are a function of thermal activation energy does not clearly relate the bias dependence to the $1/f^{\gamma}$ characteristics. Moreover, the LFN characteristics of our study seem to closely relate to the electric field applied along the channel, which will change the carrier velocity and therefore may also impact the trapping-detrapping time constant. This is an aspect that has not been explained extensively since most of reported device characteristics are usually under low drain voltage. A better $1/f^{\gamma}$ noise model including the impact of carrier tunneling distance and activation energy on trapping-detrapping time constants, and the impact of hot carrier effects may therefore be necessary for the analysis of low-frequency noise in AlGaN/GaN MODFETs under high bias conditions.

V. Conclusion

Overall, LFN of AlGaN/GaN HEMTs was investigated for both gate and drain under different bias conditions. The results indicate that the gate noise current was low and insensitive to the gate-drain reverse bias. The normalized drain noise current in the linear region increases as the device is biased close to pinch-off, which can be explained by screening effects. The drain noise current spectral density in the saturation region presented bias-dependent Lorentz components. The observed LFN characteristics are discussed in terms of electric field, carrier velocity and trapping-detrapping considerations. Overall, this study provides further physical understanding of LFN characteristics in AlGaN/GaN HEMTs.

Acknowledgement: Work supported by ONR (contract nos. N00014-00-1-0879, N00014-02-1-0128) and HRL Laboratories. The authors are grateful to Drs. J. Zolper and H. Dietrich for technical discussions and support of this work.

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Digital Etching for Highly Reproducible Low Damage Gate Recessing on AlGaN/GaN HEMTs

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Abstract

A room temperature digital etching technique for aluminum gallium nitride has been developed. An oxidizing agent and an acid have been used in a two step etching cycle to remove aluminum gallium nitride in approximately 5–6 Å increments. The process has been characterized to be reasonably linear and highly repeatable, offering an alternative to currently not available gate recess etch stopper technologies. Recessed gate $Al_{0.35}Ga_{0.65}N$/GaN HEMTs on sapphire were compared to un-recessed devices realized on the same sample. A fivefold gate leakage decrease and negligible variations on breakdown voltage support digital recessing as a viable solution for highly reproducible low surface-damage gate recessed structures.

I. Introduction

Recessed gate geometries, in which the gate metal is placed slightly below the original epilayer surface, are conventionally achieved on III-V semiconductors using either wet or dry etching. The improvements in terms of breakdown, transconductance, and linearity due to the recessed geometry are balanced by an increase in gate leakage (due to etch damage) and by a decrease in threshold voltage uniformity (due non-reproducible etch depth). The last two drawbacks have to be properly considered when comparing different etch techniques. Conventional wet recess etching is a low damage technique characterized by poor wafer uniformity and poor run to run reproducibility. Dry recess etching has been shown to be more reproducible, particularly when used with an etch stop layer, but at the same time more prone to damage. Both dry [1], [2], [3], [4], [5], [6], [7] and wet [8] etch techniques have been demonstrated to be feasible for gate recess etching on AlGaN/GaN HEMTs, but no etch stop for high aluminum content AlGaN has so far been reported, possibly leading to poor run to run threshold voltage uniformities [6]. Surface damage, poor reproducibility, and high variability in AlGaN:GaN selectivity are at present the three main shortcomings of dry etching on GaN. In the present study the accuracy and repeatability of a different, potentially low-damage, digital etching technique for gate recessing on AlGaN/GaN HEMTs has been analyzed. The resolution and reproducibility of the technique have been characterized to be in the 6 Å range, challenging the accuracy achievable by an etch stopper technology.

Digital recess etching was first suggested on GaAs by Bozada *et al.* [9]. The idea was to achieve a specified etch depth by consecutive repetitions of a two step process. On the first step the semiconductor epitaxial layer is oxidized by a diffusion limited process (rinse in H_2O_2) in which the oxidation depth is considerably process independent. On the second step the so formed oxide is selectively removed, with negligible effect on the underlying un-oxidized material. In the present study the technique has been successfully transferred to AlGaN/GaN HEMTs, the oxidation step being achieved by exposure to a low power oxygen plasma descum. The following results have been achieved: (a) reasonably linear,

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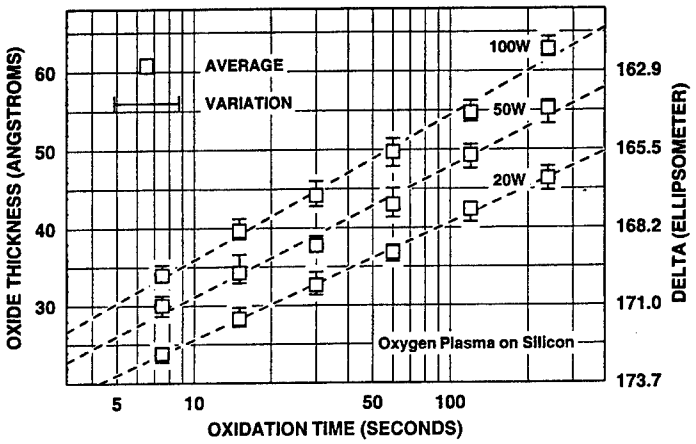


Fig. 1. Measured oxide thickness as function of oxygen plasma exposure time. The substrate was n-type, phosphorus doped, silicon single-crystal with an (111) oriented cleaved surface. The oxygen plasma was generated by a Technics Planar Etch PEIIA Plasma System. RF excitation was applied at the electrode at a frequency of 30 kHz. Oxide thicknesses were measured by a Rudolph Research AutoEL III ellipsometer. Oxide thicknesses were deduced assuming an index of refraction for silicon dioxide of 1.45. An error of ±0.05 on index of refraction will induce an error of ∓6% on oxide thickness in the present oxide thickness range.

accurate, and extremely reproducible gate recess depths were determined by atomic force microscopy (AFM) as function of number of digital recess cycles, even for very shallow etches (less than 50 Å); (b) decreased gate leakage and unaffected three-terminal off state destructive breakdown were experienced for recessed devices compared to un-recessed ones, attesting the low surface-damage profile of the

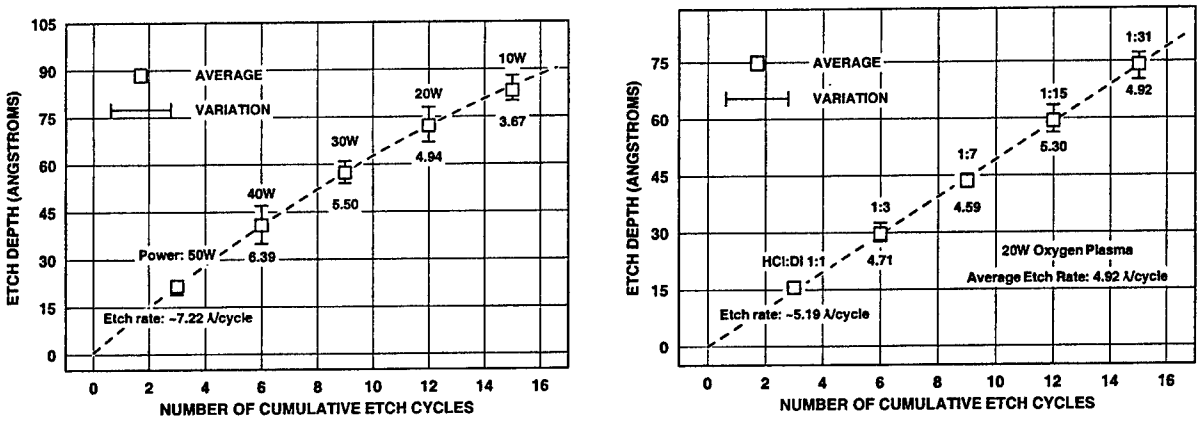


Fig. 2. Left. Measured etch depths as function of digital etch cycles for different oxygen plasma powers. Plasma power was progressively decreased from 50W to 10W at 10W increments. Three digital etch cycles were cumulatively performed for each plasma power. Etch depths were measured by atomic force microscopy (AFM) and averaged on 6 measurements. Averaged etch depths after 3, 6, 9, 12, and 15 etch cycles were 21.7, 40.8, 57.3, 72.2, and 83.2Å. Corresponding standard deviations were 1.5, 4.3, 2.8, 4.0, and 3.1 Å. — Right. Measured etch depths as function of digital etch cycles for different hydrochloric acid concentrations. HCl:DI oxide removal solution was progressively diluted from 1:1 to 1:31. Three digital etch cycles were cumulatively performed for each solution. Plasma power was 20W. Etch depths were measured by atomic force microscopy (AFM) and averaged on 6 measurements. Averaged etch depths after 3, 6, 9, 12, and 15 etch cycles were 15.6, 29.7, 43.5, 59.4, and 74.1Å, respectively. Corresponding standard deviations were 1.0, 2.0, 1.1, 2.7, and 2.7 Å.

technique; (c) no etch selectivity between GaN and AlGaN was detected for oxygen plasma powers in the 20–50 W range.

II. Process Characterization

The diffusion limited nature of the oxygen plasma oxidation was verified by ellipsometric techniques on silicon samples. We used n-type, phosphorus doped, Si single-crystals with an (111) oriented cleaved surface. The natural oxide was removed by a dip in HF (49%) for 1 min. Initial oxide thicknesses were in the 13.1–19.4 Å range. Different samples were cumulative oxidized at 20, 50, and 100 W oxygen plasma powers, corresponding to 0.027, 0.069, and 0.137 $W cm^{-2}$ power densities (12 inch diameter plate electrode). The samples were cumulatively exposed to the plasma for 7.5, 15, 30, 60, 120, and 240 s (Fig. 1). System pressure was 300 mTorr. The oxygen plasma was generated by a Technics Planar Etch PEIIA Plasma System. RF excitation was applied at the electrode at a frequency of 30 kHz. After each oxidation step oxide thicknesses were measured by a Rudolph Research AutoEL III ellipsometer. The angle of incidence was $\varphi = 70°$ and the wavelength used was $\lambda = 632.8$ nm (He-Ne laser). Oxide thicknesses were deduced assuming an index of refraction for silicon dioxide of 1.45. Average natural oxide thickness after HF treatment was 16.9 Å with a standard deviation of 1.5 Å, as measured on 4 different samples averaging 6 times each measurement. Oxide thickness after the whole experiment on an untreated sample kept at room atmosphere was 19.5 Å, with a standard deviation on 6 measurements of 1.6 Å. The dependence of film thickness on time was strictly logarithmic in the tested time frame. The pre-exponential period of oxidation [10] was shorter than 7.5 s . Growth rates at 20, 50, and 100 W were 15.1, 16.7, and 18.5 Å/decade. The logarithmic dependence of oxide thickness on oxidation time is representative of a self-limiting process. A self-limiting thickness is significant for digital etching because it results in an effective etch depth that is not proportional to time, but is essentially constant over a reasonably large time frame. The dependence of oxide thickness on oxidation plasma power was instead roughly linear, with a possible negative impact on digital etch repeatibility.

The effect of different plasma powers on $Al_{0.35}Ga_{0.65}N$ digital etch rate is shown in Fig. 2 (left). Tests were performed on a sample grown by metal organic chemical vapor deposition (MOCVD) on a c-plane

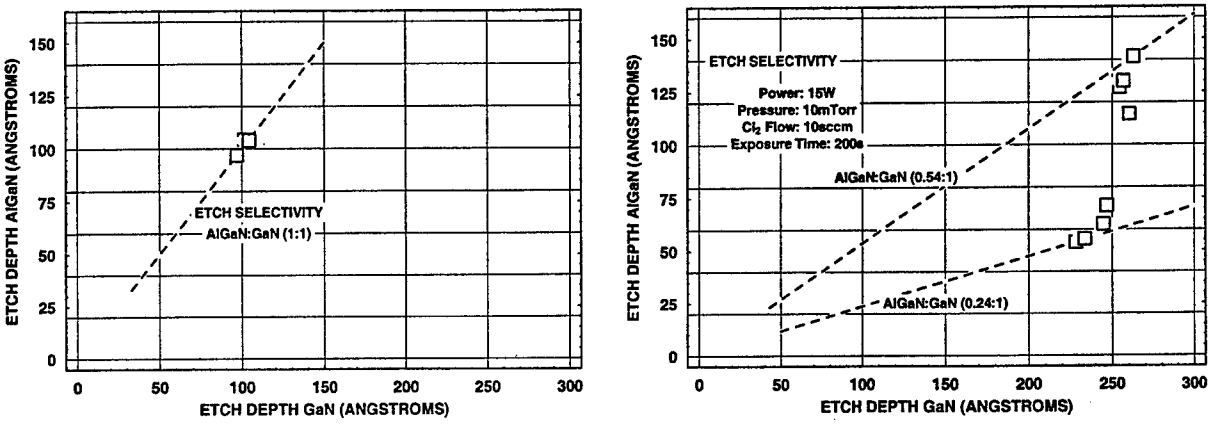


Fig. 3. Left. Etch selectivity between GaN and $Al_{0.35}Ga_{0.65}N$ for digital recesses performed at oxygen plasma powers between 20 and 50W. — Right. Etch selectivity between GaN and $Al_{0.35}Ga_{0.65}N$ for low power chlorine RIE etches. Etch depths were measured by atomic force microscopy (AFM) on top and bottom of lithographically defined mesas (corresponding to $Al_{0.35}Ga_{0.65}N$ and GaN material, respectively). GaN etch depth (rate) was found to be relatively repeatable, with an average of 249 Å (1.24 Å/s) and standard deviation of 13 Å (0.06 Å/s). AlGaN etch rate was more variable, with an average of 94.6 Å (0.47 Å/s) and standard deviation of 37.1 Å (0.18 Å/s). AlGaN:GaN etch ratio varied between 0.54:1 and 0.24:1.

sapphire substrate. The epilayer consisted of a semi-insulating GaN buffer, a 5 Å AlN dipole barrier [11], and a 290 Å silicon doped $Al_{0.35}Ga_{0.65}N$ layer. Estimated etch rates were roughly linear in power, varying from 3.67 Å/cycle for the 10 W plasma oxidation to 7.22 Å/cycle for the 50 W plasma oxidation. No etch selectivity between AlGaN and GaN was ever detected on multiple tests at plasma powers in the 20-50W range (Fig. 3 left). A selective character was instead found for low power chlorine (Cl_2) dry etching [6] (15 W input power, ~1V DC voltage, 10 sccm Cl_2 flow, 10 mTorr pressure, 200 s exposure time), with highly variable selectivity from run to run (Fig. 3 right).

The so formed oxide was removed by a solution of HCl:DI. The samples were rinsed in the solution for 1 min at 25°C. The solution was constantly mixed by a magnetic stirrer rotating at 160 rpm, and it was left covered for most time during the experiment. The independence of etch rate on acid concentration is illustrated on Fig. 2 (right), were the etch rate is constant for HCl:DI ratios between 1:1 and 1:31.

The degradation in 2DEG sheet charge density and mobility due to cumulative exposures to oxygen plasma was evaluated by Hall measurements (Fig. 4). Measurements were averaged on 3 different dies, and each measurement was repeated 3 times. No oxide removal was intentionally performed between

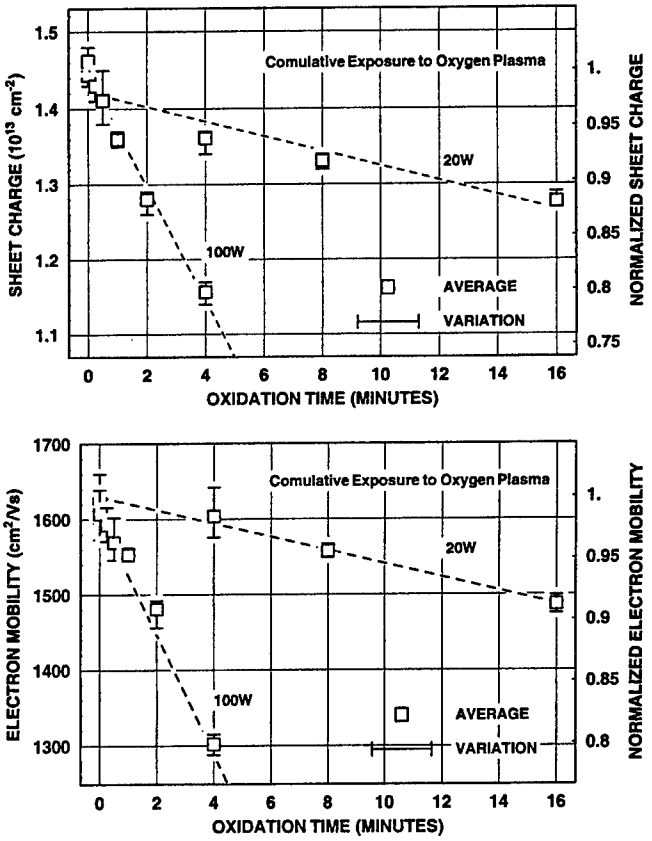


Fig. 4. Top. Degradation in 2DEG sheet charge density due to cumulative exposures to oxygen plasmas at two different power levels (20 and 100 W). Channel degradation increased at the increase in plasma power and oxidation time. No oxide removal was intentionally performed between subsequent oxidations. — Bottom. Degradation in 2DEG electron mobility due to cumulative exposures to oxygen plasmas at different power levels. Channel degradation increased at the increase in plasma power. No oxide removal was intentionally performed between subsequent oxidations.

subsequent oxidations, leaving the AlGaN barrier thickness unchanged during the experiment. Channel degradation increased at the increase in plasma power and oxidation time. After 4 minutes exposure to 100W oxygen plasma a degradation of 21% (19%) was detected in channel charge (mobility), compared to 6% (1%) in the case of 20W exposure. At 20W plasma power, 16 minutes exposure, a reduction of 12% (9%) was detected in channel charge (mobility).

III. Device Fabrication

Devices were fabricated on a sample grown by metal organic chemical vapor deposition (MOCVD) on a c-plane sapphire substrate. The epilayer consisted of a semi-insulating GaN buffer, a 5 Å AlN dipole barrier [11], and a 290 Å silicon doped $Al_{0.35}Ga_{0.65}N$ layer. On the wafer, HEMTs were fabricated through Ti/Al/Ni/Au ohmic metal evaporation, mesa isolation, and Ni/Au/Ni gate definition. All layers were defined by i-line stepper lithography. Ti/Al/Ni/Au (200 Å/1500 Å/375 Å/500 Å) ohmic contacts were deposited by e-beam, and annealed at 870°C for 30 s in forming gas. Mesa isolation was obtained by reactive ion etching (RIE). Plasma conditions were 100 W power, 5 mTorr pressure, and 10 sccm Cl_2 flow rate, corresponding to an etch rate of about 10 Å/s. The mesa etch depth was about 1200 Å. After gate lithography, and before gate metal evaporation, a self aligned gate recess was achieved by a digital etching technique. As already explained, an oxidizing agent and an acid were used in a two step etching cycle to remove the aluminum gallium nitride in approximately 6 Å limited increments. In the first step of the cycle the AlGaN surface layer was oxidized by a low power oxygen plasma descum (20 – 50 W power, 300 mTorr oxygen pressure, 30 s exposure). In the second step of the cycle the oxide was removed by a rinse in HCl:DI (1:1−1:15) for 1 min at 25 °C. These steps were repeated to reach the desired etch depth. After completion of the gate recess etch step the gate metal (Ni/Au/Ni) was deposited by e-beam evaporation (300Å/2000Å/500Å) . Devices adopted a 2 finger T-layout configuration with a nominal gate length of 0.7μm and a gate width of 150μm. The spacing between gate and drain was 2.0μm and gate-source spacing was 0.7μm. Recessed and un-recessed devices were obtained on the same sample.

IV. Measurements and Results

Etch depths were measured by atomic force microscopy (AFM) after 0, 2, 4, 8, 12, and 16 etch cycles (Fig. 5) at a plasma power of 50 W. The oxide removal solution was HCl:DI (1:1). Increasing the number of digital etch cycles produced larger etch depths, but the etch rate as calculated by:

$$\text{Digital etch rate(Å/cycle)} = \frac{\text{Measured etch depth}}{\text{Number of digital etch cycles}} \quad (1)$$

remained relatively constant. Depth data were collected on 3 different dies for each number of digital etch cycles. For each measurement both the downward and upward trench edges were measured and averaged. Average etch depths after 2, 4, 8, 12, and 16 etch cycles were 14.0, 23.0, 51.9, 75.9, and 97.0 Å, corresponding to digital etch rates of 7.0, 5.7, 6.5, 6.3, and 6.0 Å/cycle. Standard etch depth deviations were 1.2, 2.7, 3.3, 0.7, and 4.5 Å, respectively. Average etch depth after lithography, but before any digital etching was 1.7 Å, with a standard deviation of 1.4 Å. While the 2, 4, 8, and 12 etch cycles were cumulatively reached by progressively covering portions of the sample, the 16 etch cycle was achieved in a separate run. The high linearity of etch depth vs number of etch cycles supports the repeatability and accuracy of the method. A possible slight decrease in etch rate at the increase in the number of etch cycles is apparent from Fig. 5. The decrease could be due to the incomplete effectiveness

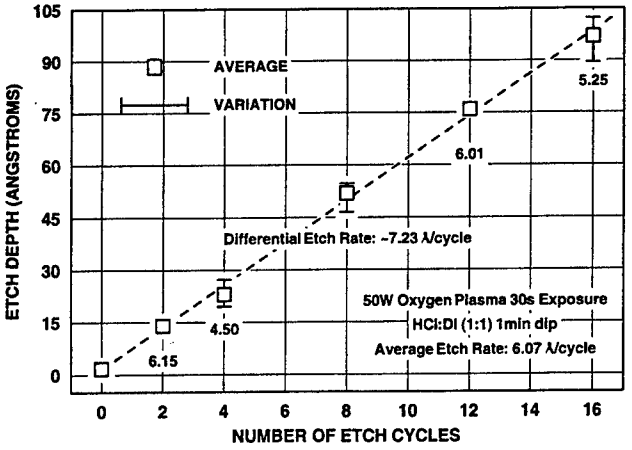


Fig. 5. Measured etch depths as function of digital etch cycles. Oxygen plasma conditions were: 50 W power, 300 mTorr pressure, 30 s exposure. Acid rinse was performed in HCl:DI (1:1) for 1 min at 25°C. Etch depths were measured by atomic force microscopy (AFM) and averaged on 6 measurements. Averaged etch depths after 2, 4, 8, 12, and 16 etch cycles were 14.0, 23.0, 51.9, 75.9, and 97.0 Å. Corresponding standard deviations were 1.2, 2.7, 3.3, 0.7, 4.5 Å. Average etch depth after lithography, and before any digital etching was 1.7 Å, with a standard deviation equal to 1.4 Å.

of hydrochloric acid in removing oxidation byproducts like aluminum oxide. Gate lengths as measured by AFM after 2, 4, 8, 12, and 16 digital recess cycles were 0.71, 0.70, 0.83, 0.87, and 0.85 μm. The slight enlargement in gate length at the increase in number of digital etch cycles was related to the action of oxygen plasma and hydrochloric acid on Shipley MEGAPOSIT^{TM}SPR^{TM}950 photoresist. No dependence of recess depth on feature dimensions was detected in the $0.65 - 5.0\mu$m gate length range.

The digital nature of the process was verified by comparing the etch depth obtained after 16 cycles of (a) 30 s oxygen plasma descum (50W); (b) 1 min rinse in HCl:DI (1:1) to the one obtained by a single cumulative cycle characterized by an 8 min oxygen plasma exposure (30 s $\times$ 16) followed by a 16 min HCl:DI rinse (1 min $\times$ 16). Averaged etch depths as measured on 3 dies were 97 Å for multiple cycles and 12 Å for the single cumulative cycle. Corresponding standard deviation were 4.5 and 0.89 Å. The approximate oxide growth rate deduced by these data was 4.9 Å/decade.

Devices were realized for the 16 digital etch cycle recesses and the results were compared to nearby un-recessed devices ($\simeq 400\,\mu$m apart). An increase in extrinsic transconductance and a positive threshold shift were observed as a consequence of the recess etch (Fig. 6). Threshold voltage shifted from -6V for un-recessed devices to -2.5V for the recessed ones, and extrinsic transconductance, measured at a drain bias of 4V, increased from about 220 to 250 mS/mm. Despite the source-drain saturation current (I_{dss}) was reduced from 1.0 to 0.45 A/mm due to the recess etch (Fig. 6 left), the maximum source-drain current, (I_{dmax}), measured at a forward gate bias current of 1 mA/mm, remained almost unchanged, decreasing only slightly from 1.2 to 1.1A/mm [7]. The two terminal gate-drain leakage, measured at a gate-drain voltage of 10V with the source floating, averagely decreased from about 4 μA/mm to 0.8 μA/mm. Standard deviations, collected from measurements on 10 devices, were 0.62 μA/mm and 0.091 μA/mm, respectively. The destructive three-terminal breakdown voltage was between 40V and 60V for both etched and un-etched devices. Hall measurement data performed before and after 10 digital etch cycles revealed a drop in charge from 1.48×10^{13}cm^{-2} to 1.13×10^{13}cm^{-2} due to thinning of the AlGaN barrier, and a slight drop in mobility from 1620 cm^2/Vs to 1320 cm^2/Vs.

In an attempt to minimize 2DEG degradation multiple oxidations were performed at a lower power level of 20 W. After each oxidation the sample was rinsed in HCl:DI (1:15) for 1 min at 25°C. 26 cycles were performed (Fig. 7 right). The expected etch depth as extrapolated from Fig. 2 (right) was 128 Å. The experimental one was 103.8 Å, with a standard deviation of 5.5 Å. The error in etch depth could be due to a reduction in etch rate at the increase in the number of digital etch cycles, as mentioned above. Hall measurements performed before and after the digital etch process revealed a drop in charge from $1.43 \times 10^{13}\,cm^{-2}$ to $0.79 \times 10^{13}\,cm^{-2}$, and a drop in mobility from $1590\,cm^2/Vs$ to $708\,cm^2/Vs$. Standard deviations in charge and mobility were $0.93 \times 10^{11}\,cm^{-2}$, $6.17 \times 10^{11}\,cm^{-2}$ and $10.2\,cm^2/Vs$, $92.6\,cm^2/Vs$, respectively. The causes of the unexpected channel degradation are currently under study. No recovery in channel performance was obtained by rapid thermal anneal in nitrogen atmosphere for temperatures in the $400-800$°C range (1 min anneals). A recovery in channel performance after anneal has been previously reported in the case of high frequency (13.56MHz), medium power, RIE oxygen plasma exposures [12].

AFM scans of the etched AlGaN surface revealed no appreciable degradation in surface morphology. The associated RMS roughness measured on multiple $0.5\,\mu m \times 0.5\,\mu m$ windows was 1.9 Å, compared to a typical as grown surface roughness of 1.8 Å. The apparent surface roughness measured on a $2.0\,\mu m \times 2.0\,\mu m$ window increased from 2.5 Å to 6.9 Å, due to enlargement of surface dislocations consequent to isotropic etching. Gate leakage, measured in a two terminal configuration, at a gate-drain voltage of 10V with the source floating, averagely decreased from 0.01 mA/mm to 0.003 mA/mm. Standard deviations were 0.002 and 0.001 mA/mm, respectively.

A comparison with standard low power chlorine etches was performed. Etch conditions for the Cl_2 reactive ion etches were: 15 W input power, ~1V DC voltage, 10 sccm Cl_2 flow, 10 mTorr pressure, 200 s exposure time (corresponding to an etch depth of ~ 130 Å). A clear degradation in surface quality was detected in this case. RMS surface roughness increased from 1.9 to 9.0 Å, independent of windows size in the $0.5-2.0\,\mu m$ range. Surface morphology showed an Al/Ga droplet-like structure, which could

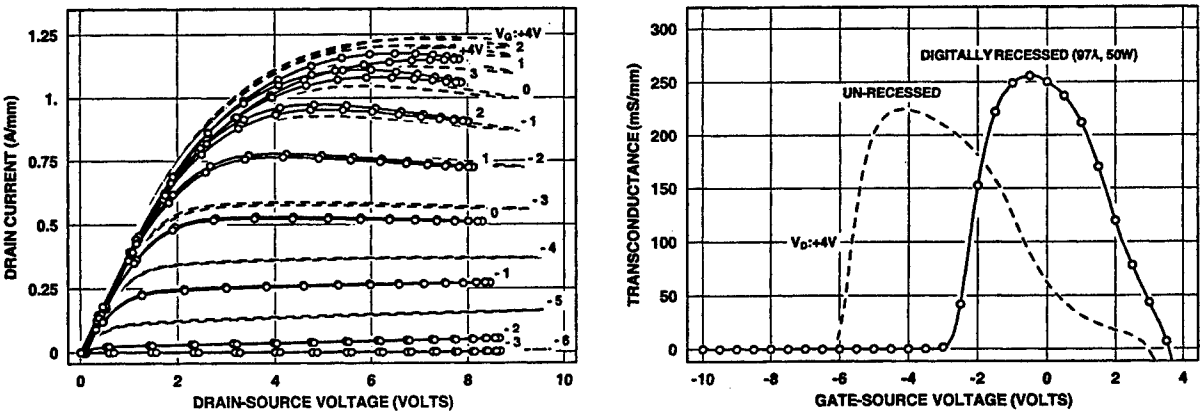


Fig. 6. Left. $I_d - V_d$ characteristics for digitally recessed and un-recessed devices as measured on $75\mu m$ gate width transistors. Gate-source voltage was varied between +4V and −6V. Dashed lines correspond to un-recessed conditions and open-circles refer to 97 Å recesses (50W oxygen plasma power). Threshold voltage shifted from −6V for un-recessed devices to −2.5V for the recessed ones. — Right. Transconductance characteristics for digitally recessed and un-recessed devices as measured on $75\mu m$ gate width transistors. Gate-source voltage was varied between −10V and 5V. Drain voltage was 4V. Dashed lines correspond to un-recessed conditions and open-circles refer to 97 Å recesses. Original $Al_{0.35}Ga_{0.65}N$ barrier thickness was 290Å. Threshold voltage shifted from −6V for un-recessed devices to −2.5V for the recessed ones. Extrinsic transconductance increased from about 220 to 250 mS/mm.

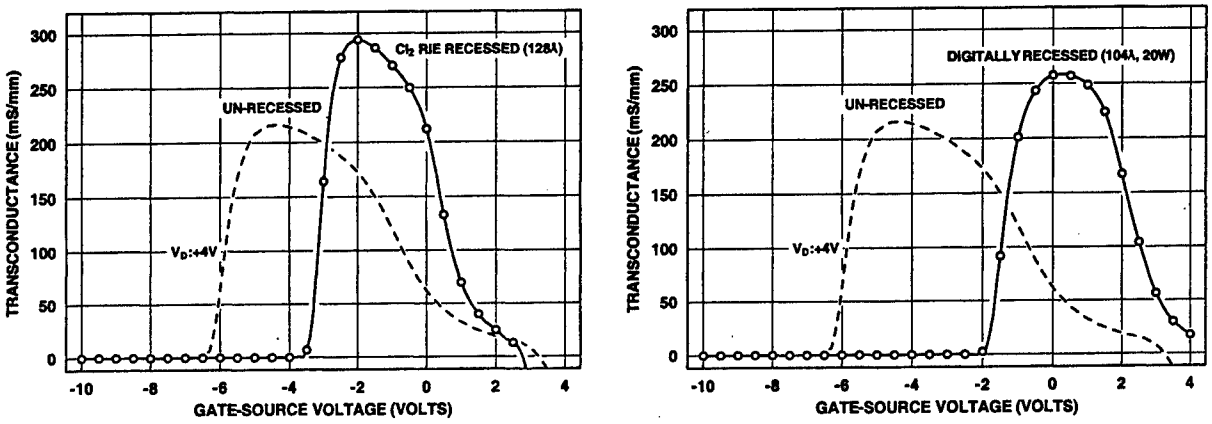


Fig. 7. Left. Transconductance characteristics for chlorine recessed and un-recessed devices as measured on 75μm gate width transistors. Gate-source voltage was varied between -10V and 4V. Drain voltage was 4V. Dashed lines correspond to un-recessed conditions and open-circles refer to 128 Å recesses (20W oxygen plasma power). Original $Al_{0.35}Ga_{0.65}N$ barrier thickness was 290Å. Threshold voltage shifted from -6V for un-recessed devices to -3.5V for the recessed ones. Extrinsic transconductance increased from about 220 to 300 mS/mm. — Right. Transconductance characteristics for digitally recessed and un-recessed devices as measured on 75μm gate width transistors. Gate-source voltage was varied between -10V and 4V. Drain voltage was 4V. Dashed lines correspond to un-recessed conditions and open-circles refer to 104 Å recesses (20W oxygen plasma power). Original $Al_{0.35}Ga_{0.65}N$ barrier thickness was 290Å. Threshold voltage shifted from -6V for un-recessed devices to -2.5V for the recessed ones. Extrinsic transconductance increased from about 220 to 250 mS/mm.

be attributed to preferential removal of nitrogen [13]. The degraded surface morphology could justify the average increase in gate leakage from 0.01 mA/mm to 0.95 mA/mm for unrecessed and Cl_2 recessed structures. Standard deviations were 0.002 and 0.13 mA/mm. Surface degradation had negligible consequences on active channel performances. Hall data revealed an increase in mobility from 1607 cm^2/Vs (standard deviation: 23.3 cm^2/Vs) to 1668 cm^2/Vs (standard deviation: 31.7 cm^2/Vs). Channel charge density decreased from $1.44 \times 10^{13}\,cm^{-2}$ (standard deviation: $8.8 \times 10^{10} cm^{-2}$) to $1.28 \times 10^{13}\,cm^{-2}$ (standard deviation: $6.7 \times 10^{11}\,cm^{-2}$). The decrease in channel charge was qualitatively compatible to thinning of the AlGaN barrier (from $\sim$290 Å to $\sim$160 Å), and the increase in electron mobility testifies the low damage profile of low power Cl_2 plasma etch techniques on active channel (Fig. 7 left).

V. Discussion and Conclusions

Previous reports of digital recess etching on GaAs-based FETs suggested the feasibility of the technique for highly reproducible low damage gate recesses on III-V semiconductors [9]. The present study confirms the potential of the technique even in the case of AlGaN/GaN HEMTs. Extremely controllable etch depths were achieved by successive surface oxidations and oxide removal etches. The reduction in gate leakage, the invariability in breakdown voltage, and the promising reproducibility and control in gate recess depth support digital etching as a viable tool for reproducible processing of gate recessed structures. Nevertheless a reduction in channel degradation and a simplification of the oxidation process have to be achieved in order to render the technique attractive. Since the process does not intrinsically require the action of a plasma but only the availability of an oxidizing agent of any kind, it is expected that the process could be slightly modified to be completely damage free. Such a modification should not affect the results on accuracy and reproducibility presented in this work.

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ACKNOWLEDGMENT

The authors would like to thank ONR IMPACT MURI, ONR CANE MURI, and AFOSR programs for support. This work made use of MRL Facilities supported by National Science Foundation under award No. DMR96-32716.

Surface trapping effects observed in AlGaN/GaN HFETs and heterostructures

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Abstract

We have observed very slow surface potential transients in AlGaN/GaN HFETs induced by high drain and gate bias stresses. The surface potential has been observed to change as much as 2.5 V near the gate. It is proposed that the change in surface potential is caused by electrons that tunnel from the gate and get trapped at the surface states. The increase in the net negative charge at the surface raises the surface barrier, which in turn reduces the 2DEG concentration. Simultaneous measurements of surface electrostatic potential and drain current indicate that the transients have similar transient responses and are therefore related. A spatial map of the surface potential change after stress with respect to time shows that maximum changes occur close to the gate. Exposure to UV laser light completely eliminates the transients, while large reduction in transient magnitude has been observed for devices passivated with SiN_x. Contrary to the gate and drain stress, UV laser exposure of AlGaN/GaN heterostructure samples has been observed to reduce the surface barrier, which slowly increases following a stretched exponential type transient after the laser is switched off. Such an observation is explained by the creation of electron-hole pairs, which decrease the net charge dipole across the AlGaN barrier and lower the barrier. The transient response is modeled by thermionic emission of electrons from the interface, which recombine with the holes trapped at the surface.

I. Introduction

AlGaN/GaN heterostructure field effect transistors (HFETs) have been the focus of intense research in recent years due to very high microwave output power density associated with them [1], [2]. Due to the polarization properties of III-nitrides a huge density of two-dimensional electron gas (2DEG) is formed at the AlGaN/GaN interface even in absence of any intentional doping [3], [4]. Presence of such a high 2DEG density in addition to the high breakdown field associated with these materials enable the AlGaN/GaN HFETs to deliver as much as 10.7 W/mm of microwave output power at 10 GHz [5]. In spite of the exceptional promise held by the AlGaN/GaN HFETs, there are certain technological issues associated with them that need to be resolved in order to realize their full potential. One such problem is the reduction of output power at high frequencies commonly called "current slump" or "current collapse". The reason behind current slump is not clear at present though several mechanisms have been proposed to explain the observation [6] – [8]. It has however been found out that passivation of the surface with SiN_x is quite effective in reducing the current slump [6], [9]. Since SiN_x passivation is expected to affect only the surface, it can be argued that the 2DEG at the AlGaN/GaN interface is largely influenced by the surface. In fact, the

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surface barrier is related to the net charge dipole across the AlGaN barrier, which in turn is related to the 2DEG at the interface [4]. In this paper we will discuss the large variation of surface barrier height caused by bias stress or UV illumination. As expected these changes in surface barrier strongly affects the 2DEG at the AlGaN/GaN interface. These observations clearly demonstrate the unstable nature of the 2DEG present in unpassivated AlGaN/GaN heterostructure samples that can possibly cause the current slump in HFETs.

II. Experiments

The experiments were performed on samples with layer structure AlGaN (200 – 250 Å)/GaN (1–2 μm)/nucleation layer/Sapphire grown by metalorganic chemical vapor deposition technique. Details of the growth conditions are reported elsewhere [10]. Transistors were fabricated following the standard procedures of mesa etching, ohmic contact formation, gate contact formation and pad deposition. Usually transistors are passivated with SiN_x, after measurements are made on unpassivated devices. Details of the fabrication procedure are described elsewhere [1]. The surface potential measurements were performed using a commercial unit from TM Microscopes attached with a scanning Kelvin probe microscopy (SKPM) module. The Kelvin probe works on the basis of electrostatic force between the tip and the sample. Principles of SKPM technique has been described in detail elsewhere [11]. The measurement set up for HFETs is shown in Figure 1. A negative dc bias is applied to the gate while a positive dc bias is applied to the drain during stress. After the device is stressed for a while, the stresses are withdrawn and the drain current is measured at a very low applied drain bias. The probe tip is positioned close to the gate towards the drain side. The drain current is estimated from the potential difference measured across a 20 Ω resistor connected in series with the source. This helps in simultaneous measurement of the drain current and surface potential with respect to time, as both of them can be measured together via two computer input channels.

The devices were usually stressed stressing continuously for few seconds to few minutes under gate bias of –12 V and drain bias of 20 V. Stressing for about two minutes was found to be adequate for the study while smaller time of stress would give lesser changes that would vary in magnitude and sometimes difficult to measure. Also the above bias levels were found to be suitable for giving rise to large changes that could be measured easily by our system. For UV effects studies, the heterostructure samples were exposed to UV illumination from a He-Cd UV laser (325 nm) to observe the variation of surface potential.

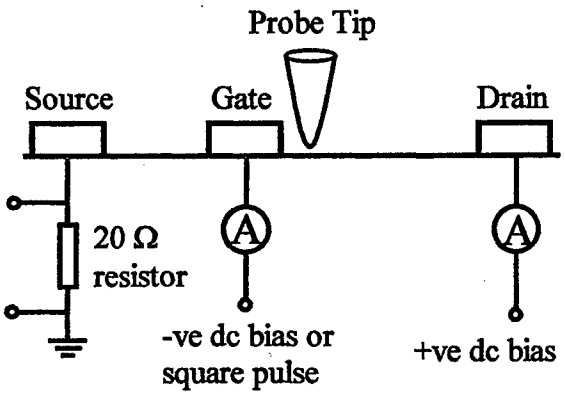


Figure 1: Schematic diagram showing the measurement set up. The probe tip is usually positioned close to the gate during measurements.

Results and discussion

Figure 2 shows simultaneously measured surface potential and drain current transients after an AlGaN/GaN HFET device was stressed for 2 minutes at drain bias of 20 V and gate bias of –12V. After the stress, during the actual measurement, the drain bias was kept at 1 V and gate bias at 0 V to measure the variation of drain current also along with the surface potential. This measurement was made at a distance of few tenths of a micron from the gate towards the drain side. As can be seen from Figure 2, the surface potential decreases significantly after stress and slowly reaches the equilibrium value after the stress is withdrawn. The drain current also has a very similar transient as the surface potential, which indicates that they are related. The actual value of the surface potential is lower than what is shown in Figure 2(a) by few tenths of a volt. This is because the surface potential measured by the probe tip has two components, the actual surface potential component, and a component due to the electrostatic bias applied to the drain during measurement (1V). However, the shape of the transient has been found to be unaffected by the applied drain bias. Since the surface potential decreases after the stress, the surface barrier (same sign as electron energy) is expected to increase which will also increase the charge dipole across the AlGaN barrier. This would reduce the 2DEG after stress that is reflected in the observation of reduced drain current after stressing. Since the bias on the gate was 0 V during the measurements, it follows that the gate did not control the drain current rather the changed surface potential which controlled the drain current. To determine the spatial variation of surface potential and its evolution with time after stress, potential scans were made up to a distance of 1 μm from the edge of the gate. Figure 3(a) shows the surface potential variation with distance, after the device was stressed for 2 minutes at a drain bias of 20 V and gate bias of –12 V. As we can see from the surface potential profile, most of the changes occur near

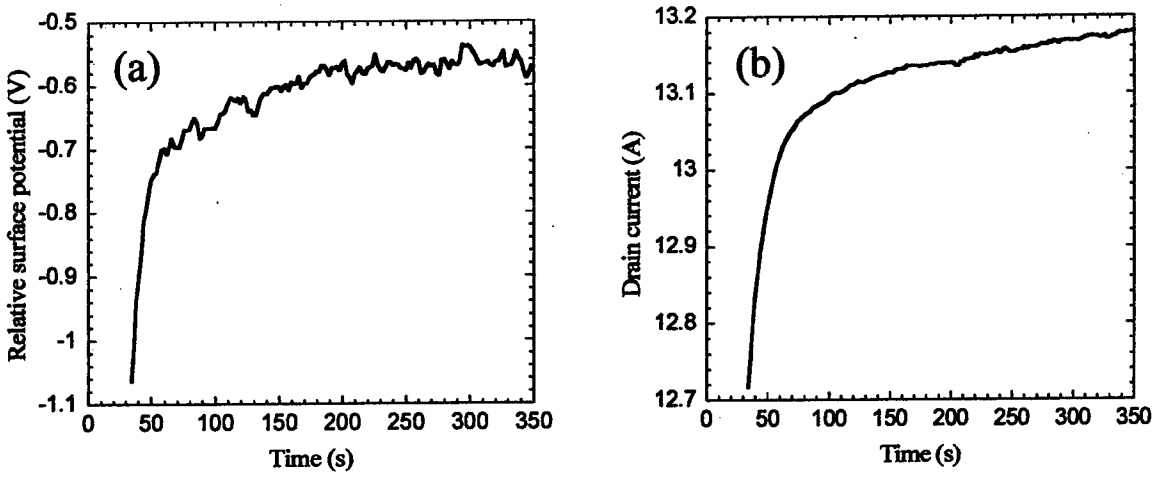


Figure 2: Simultaneous measurement of (a) surface electrostatic potential and (b) drain current for a 250 μm device after stressing for 2 minutes at –12 V gate bias and 20 V drain bias. The measurements after stress were made under 1 V drain bias and 0 V gate bias.

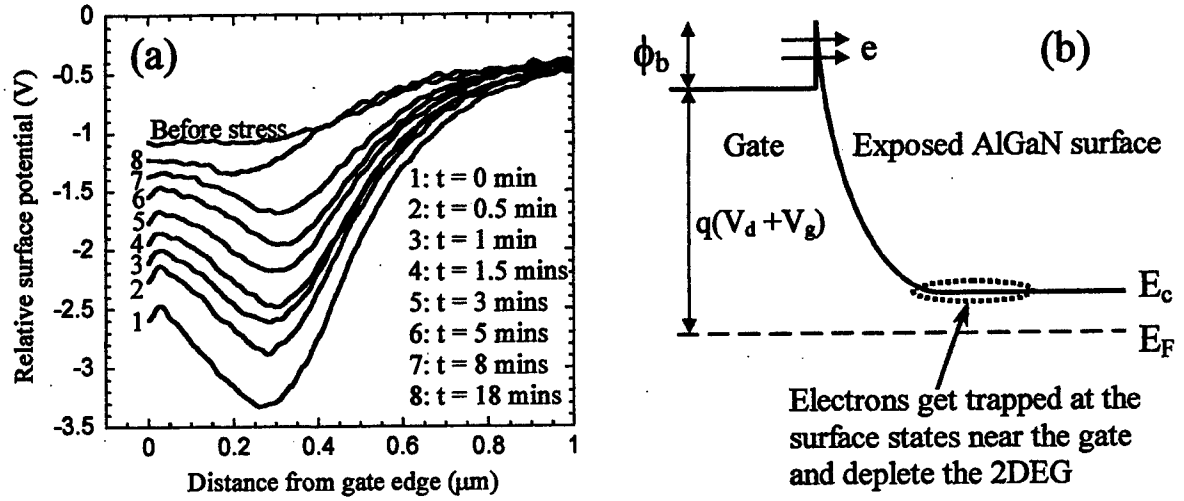


Figure 3: (a) The surface potential variation with distance from the gate edge for an HFET after it was stressed for 2 minutes at 20 V drain bias and –12 V gate bias. The surface potential profile before stress is also shown for comparison. (b) Schematic band diagram explaining the tunneling of electrons under high gate and drain bias stresses. The tunneled electrons get trapped at the surface near the gate and deplete the 2DEG at the interface.

the gate, and the surface potential reaches a minimum value at ~0.3 μm from the edge of the gate. The surface potential changes very slowly with time and reaches the unstressed condition only after a long time. To explain the observed changes in surface potential a model based on the tunneling of electrons for the gate under applied bias stress is proposed as shown in Figure 3(b). Under high bias stresses, electrons tunnel from the gate and get trapped at the surface states. This causes the surface potential to decrease or the surface barrier to increase. Thus the 2DEG is decreased and a reduction in drain current is observed after the stress. Since the surface potential is lowered after stress, even if the gate potential increases the drain current will not increase, and will be controlled by the magnitude and extent of the surface potential lowering. Thus a "virtual gate" is formed at the free surface near the gate, which controls the drain current. At higher frequencies the surface potential will not be able to change as quickly (due to large detrapping time constant associated with the traps) as the gate bias, and the drain current will remain lowered. This can also be a possible mechanism for the current slump observed at high frequencies in nitride HFET devices. To further support this mechanism as responsible for current slump, measurements were performed on unpassivated and passivated (with SiN_x) devices. It was found out that the magnitude of drain current and surface potential transients become much lower after passivation for similar conditions of stress. This indicates that charge stabilization can be achieved after passivation, which helps in current slump reduction. Further, under UV illumination the reduction in drain current and surface potential was not observed. This can be explained by noting that under UV illumination the electron-hole pairs are generated in the bulk of which the holes move towards the surface and neutralize electrons tunneled from the gate, thus preventing the surface potential from getting lowered. These results will be published elsewhere in detail.

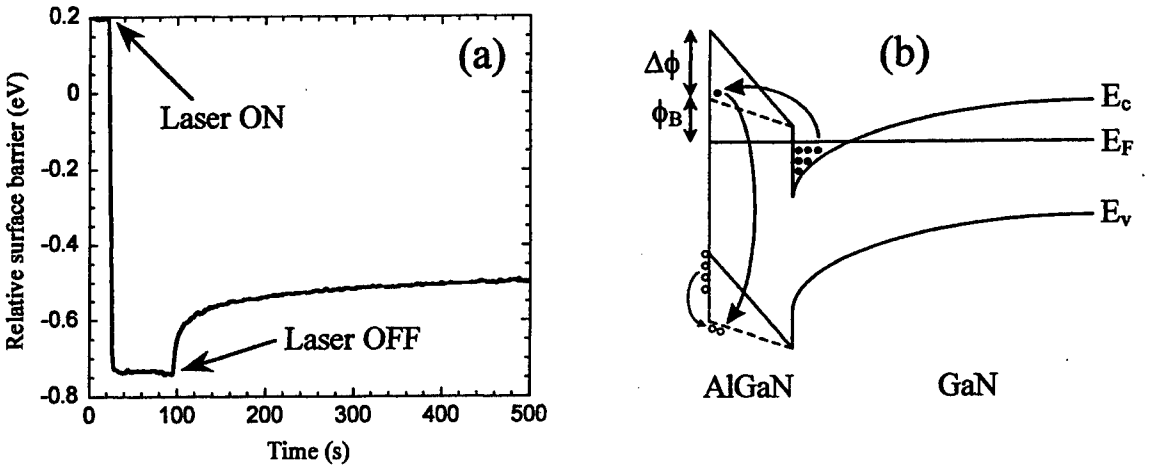


Figure 4: (a) Surface potential transient measured on an AlGaN/GaN heterostructure induced by switching the UV laser on and off. (b) Schematic band diagram explaining the observed UV laser induced transients. The surface potential reduces by $\Delta\phi$ under illumination (from top) due to change in charge dipole magnitude across the AlGaN barrier layer. After the laser is turned off, the electrons (solid dots) emit thermionically from the quantum well and recombine (shown by big arrows) with the excess holes (hollow dots) trapped at the surface thus causing a very slow rise in surface potential.

Significant changes in surface barrier due to UV illumination were observed in AlGaN/GaN heterostructures. Figure 4(a) shows the surface barrier transient observed by switching the UV laser on and off. As can be observed the surface barrier changes by ~0.95 V due to UV laser exposure. After the laser is switched off the surface barrier slowly returns to the equilibrium value (value attained by storage in dark at room temperature for several weeks to several months). The observations can be explained as follows. As the UV laser is switched on electron-hole pairs are photo-generated in the bulk (mostly in GaN layer as AlGaN bandgap for 35% Al composition is larger than the laser energy), which screen the high electric field in the AlGaN layer and reduce the surface barrier. As a result of decrease in surface barrier, 2DEG at the interface is increased. After the laser is switched off, the excess electrons thermionically emit from the quantum well and recombine with the excess holes trapped the surface giving rise to the slow recovery transient observed. The recovery transient is non-exponential since the emission of electrons from the quantum well and the subsequent recombination with holes increases the barrier height and decreases the rate of electron emission. The theoretically calculated transient has been compared to the experimentally measured one and excellent fit has been observed [12], which validates the model. The only fitting parameter required for theoretical calculations is the initial value of surface barrier (just after the laser is switched off), ϕ. Interestingly, from ϕ, and the change in surface potential under illumination, $\Delta\phi$, and the initial equilibrium value of the surface potential can be estimated. This was found to be ~1.65 eV for 35% Al composition in the barrier layer. The transients become faster at higher temperature, which also supports the thermionic emission model. For larger composition of Al in the AlGaN barrier layer, the

transient becomes slower due to increased barrier height seen by the electrons. Samples that just have the GaN epilayer do not show the long recovery transient, however GaN capped AlGaN/GaN heterostructures show the long transient, which indicates that it is the presence of a barrier (with a built-in electric field which causes the charge separation) rather than the nature of the surface that is responsible for the observed transients.

Conclusions

In conclusion, we have observed large changes in the surface barrier of AlGaN/GaN HFETs and heterostructures. The increase in surface barrier in AlGaN/GaN HFETs after stress is caused by the trapping of electrons at the surface, which have tunneled from the gate under high bias stresses. These trapped electrons increase the surface barrier and reduce the 2DEG concentration at the interface acting like a virtual gate. The surface barrier mostly changes close to the gate towards the drain side. The formation of a virtual gate causes the actual gate to lose control over the drain current and this can possibly be a reason for the observed current slump at high frequencies. UV illumination eliminates the surface potential transients while passivation with SiN_x significantly reduces them. In contrary to the stress induced effects, UV illumination of an AlGaN/GaN heterostructure reduces the surface barrier by screening the built-in electric field in the AlGaN layer by photo-generated electron-hole pairs. The excess 2DEG formed due to UV illumination, emit thermionically from the quantum well after the laser is switched off to give a transient response with a stretched exponential behavior.

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Acknowledgements

The authors would like to acknowledge Joe Smart, Tom Prunty and Professor J. R. Shealy for AlGaN/GaN heterostructure samples. This work is supported by the Office of Naval Research MURI on semiconductor interface electronics under Contract no. N00014-96-1-1179 under the direction of Dr. Colin E. C. Wood.

Comparison of Surface Passivation on Films for Reduction of Current Collapse in AlGaN/GaN High Electron Mobility Transistors

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Abstract

Three different passivation layers (SiN_X, MgO and Sc_2O_3) were examined for their effectiveness in mitigating surface-state-induced current collapse in AlGaN/GaN high electron mobility transistors (HEMTs). The plasma-enhanced chemical vapor deposited SiN_X produced ~80-85% recovery of the drain-source current, independent of whether SIH_4/NH_3 or SiD_4/ND_3 plasma chemistries were employed. Both the Sc_2O_3 and MgO produced essentially complete recovery of the current in GaN-cap HEMT structures and ~80-95% recovery in AlGaN-cap structures. The Sc_2O_3 had superior long-term stability, with no change in HEMT behavior over 5 months aging.

Introduction

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AlGaN/GaN high electron mobility transistors (HEMTs) show great promise for applications, such as high frequency wireless base stations and broad-band links, commercial and military radar and satellite communications [1-7]. One problem commonly observed in these devices is the so-called "current collapse" in which the application of a high drain-source voltage leads to a decrease of the drain current and increase in the knee voltage [7-9]. This phenomenon can also be observed by a current dispersion between dc and pulsed test conditions or a degraded rf output power.

Gd_2O_3, Sc_2O_3 and MgO have been used as gate oxide for the metal oxide semiconductor (MOS) technology and oxide/GaN interface state densities were ~$2 \times 10^{11} - 1 \times 10^{12}$ cm^{-2}[10-13]. Sc_2O_3 and MgO have smaller lattice mismatch to GaN and larger bandgap than Gd_2O_3. Recently, we demonstrated promising results for passivating AaGaN/GaN with Sc_2O_3 and MgO [14, 15]. In addition, these oxides do not contain hydrogen and may have advantages over SiN_X in that respect because atomic hydrogen diffuses rapidly and could enter the GaN or gate metal over extended periods of device operation.

In this talk, we report on a comparison of SiN_X, MgO and Sc_2O_3 passivation layers on AlGaN/GaN HEMTs with different layer structures (GaN vs AlGaN cap layer) and show the long-term (5 month) stability of the MgO and Sc_2O_3 passivation.

Experimental

Two different HEMT structures were used in our studies as shown in Figure 1. The first employed an undoped GaN-cap layer on top of an undoped $Al_{0.2}Ga_{0.8}N$ layer. Both Al_2O_3 and SiC substrates were used. The second type of HEMT employed an undoped $Al_{0.3}Ga_{0.7}N$-cap layer on top of a doped $Al_{0.3}Ga_{0.7}N$ donor layer. Around 100Å thick dielectric layers, MgO, Sc_2O_3, or SiN_X, were deposited on completed devices using either Molecular Beam Epitaxy (MBE) for the oxides or PECVD for the SiN_X, with deposition temperatures of 100°C in the oxide case and 250°C for the SiN_X case. The SiN_X films were deposited with either SiH_4 + NH_3 or SiD_4 + ND_3 to examine the effect of deuterated precursors. The HEMT dc parameters were measured in dc and pulsed mode at 25°C, using a parameter analyzer for the dc measurements and pulse generator, dc power supply and oscilloscope for the pulsed measurements. For the gate lag measurements, the gate voltage V_G was pulsed from –5V to 0V at different frequencies with a 10% duty cycle.

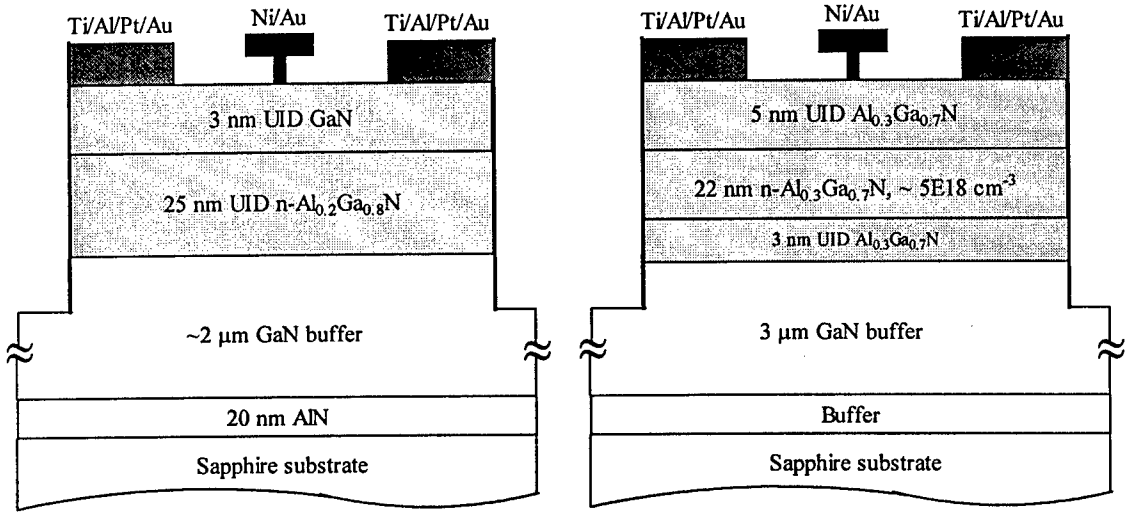


Figure 1. Schematic cross-sections of GaN-cap (right) and AlGaN-cap (left) HEMT structures.

Results and Discussion

Figure 2(left) shows typical gate lag data for 0.5 × 100μm^2 GaN-cap HEMT grown on sapphire substrates. The decrease in drain-source current becomes more pronounced at high frequencies. The degradation in current was less significant when these same structures were grown on SiC substrates. The defect density will be lower in the latter case due to the closer

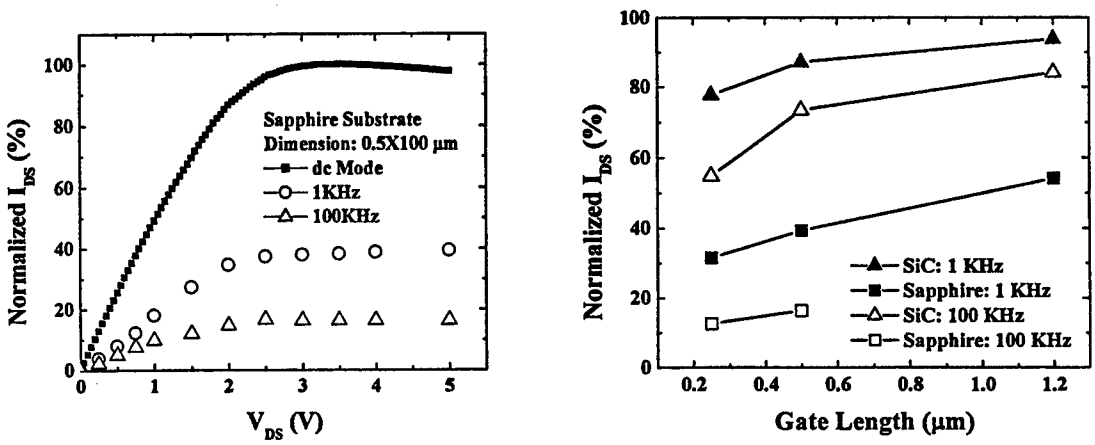


Figure 2. Gate lag measurements on unpassivated 0.5μm gate length, GaN-cap HEMTs grown on either sapphire (left) and normalized I_{DS} as a function of both gate length and substrate type for GaN-cap HEMTs at pulse frequency of 1 KHz and 100 KHz (right).

lattice match between GaN and SiC. This suggests that at least some of the surface traps are related to dislocations threading to the surface. The effects of both substrate type and HEMT gate length on the change in drain-source current are shown in Figure 2(right). The shorter the gate length, the more pronounced degradation observed in current due to larger surface area and higher electric field in the channel between gate and drain.(the source-to-drain distance was fixed in all devices).

The I_{DS}-V_{DS} characteristics before and after SiN_X passivation using either hydrogenated or deuterated precursors are illustrated in Figure 3. The inset shows the complete set of I-V curves for the as-fabricated HEMT and the main figure shows only the uppermost curves for clarity. The I_{DS} increases after passivation with either type of SiN_X, which indicates that the passivation of the semiconductor is improved. Similarly, the transconductance (g_m) increases after SiN_X deposition, which also suggests a decrease in surface trap density (Figure 3, right).

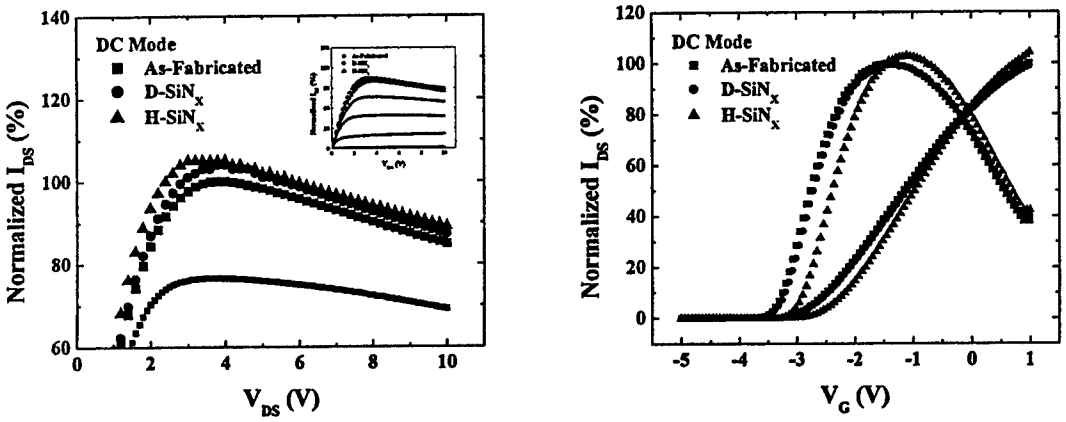


Figure 3. Normalized I_{DS} versus V_{DS} (left) or V_G (right) for 1.2×100μm^2, GaN-cap HEMTs before and after SiN_X passivation using either hydrogenated or deuterated precursors.

The gate-lag data for the HEMTs before and after SiN_X passivation are shown in Figure 4(left). Note that both the hydrogenated and deuterated precursor dielectrics produce a recovery of 80-85% in the drain-source current. The unity current gain frequency (f_T) and maximum frequency of oscillation (f_{MAX}) data before and after passivation are shown at the right of Figure 4. There is a slight increase in both parameters, in contrast to previous

reports[15]. There were no systematic differences between the results of hydrogenated and deuterated precursor SiN_X, even though the latter typically produce slightly denser films when deposited under the same PECVD conditions.

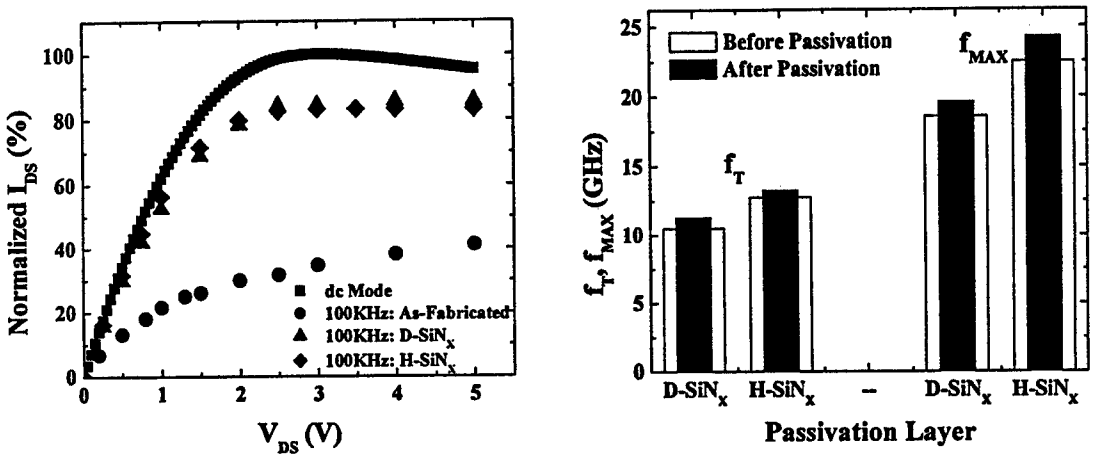


Figure 4. Gate lag measurements before and after SiN_X passivation of $1.2\times100\mu m^2$, GaN-cap HEMTs (left) and f_T and f_{MAX} before and after SiN_X passivation (right).

The gate lag measurement for MgO-passivated HEMTs immediately after MgO deposition and after 5 months aging without bias on the devices under room conditions are

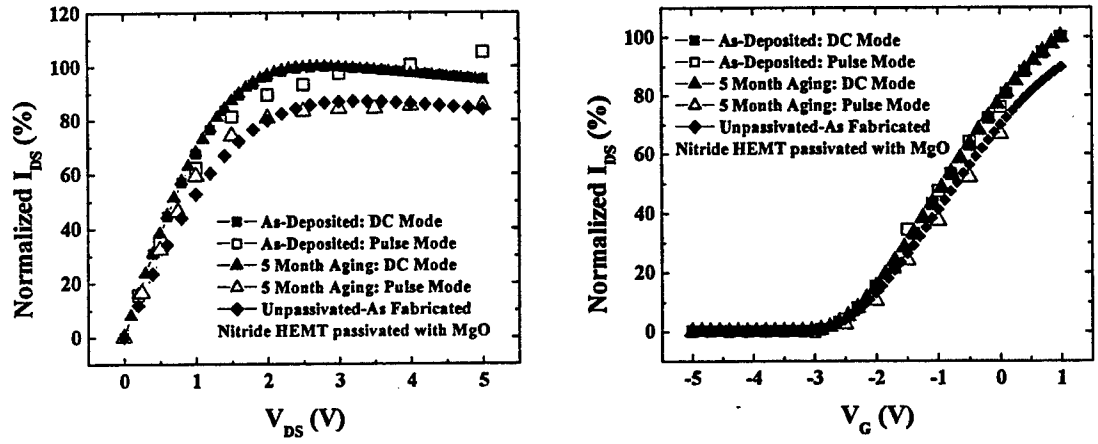


Figure 5. Gate lag measurements before and after MgO passivation and following 5 months aging of $1.2 \times 100\mu m^2$, GaN-cap HEMTs. At left V_G was switched from –5 to 0V, while at right it was switched from –5V to the value shown on the X-axis

shown in Figure 5. The I_{DS} increases ~20% upon passivation and there is almost complete mitigation of the degradation in I_{DS} immediately after MgO deposition. However, after 5 months aging, there is a clear difference between the dc and pulsed data, indicating that the MgO passivation has lost some of its effectiveness. We are currently investigating possible mechanisms of degradations, such as hydration of MgO.

Similar data is shown in Figure 6 for Sc_2O_3-passivated HEMTs. In this case, the I_{DS} also increases upon deposition of the oxide and there is also essentially complete mitigation of the degradation in drain-source current. In the contrary to MgO passivation, after 5 months aging, there is no significant change in the device characteristics. This indicates that Sc_2O_3 provides more stable passivation than that of MgO. We have noticed in separate experiments that the MgO/GaN interface deteriorates over time. A higher interface state trap densities of GaN MOS diodes were observed, if MgO surface left uncapped for a while before diode metal is deposited. However, if the MgO is immediately covered with the diode gate metal, the lower interface state densities were observed. The MgO degradation may be easily resolved by depositing another dielectric such as SiN_X, since thicker dielectric film will be needed for capacitors or insulated layer between metal layers during the fabrication of power amplifiers or

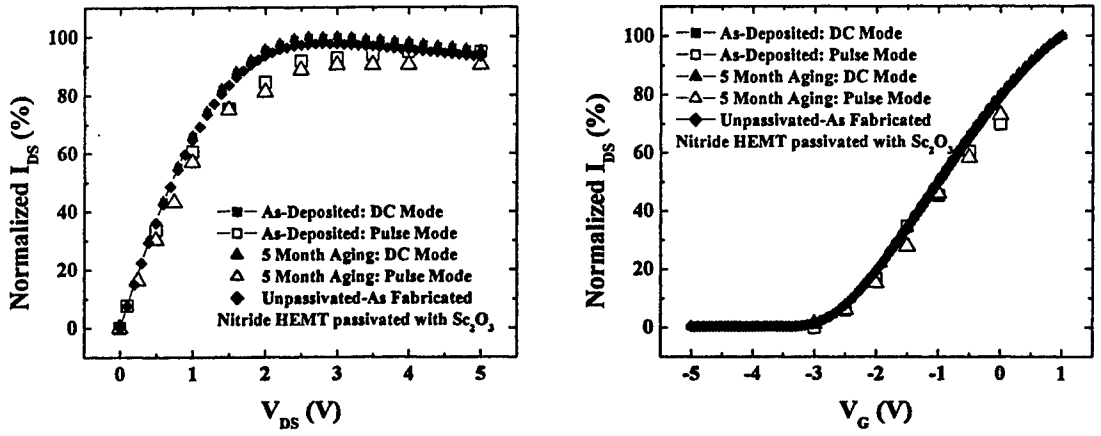


Figure 6. Gate lag measurements before and after Sc_2O_3 passivation and following 5 months aging of $1.2\times100\mu m^2$, GaN-cap HEMTs. At left V_G was switched from –5 to 0V, while at right it was switched from –5V to the value shown on the X-axis.

integrated circuits. However, further work is needed to establish the long term reliability of Sc_2O_3 and MgO passivation, but the preliminary data with Sc_2O_3 looks very promising.

The cap layer of AlGaN/GaN HEMT also plays an important role for the passivation. The gate lag data for the HEMT structures with $Al_{0.3}Ga_{0.7}N$ as the top layer as illustrated in Figure 1(right), shows less recovery of drain current as compared to that of GaN capped HMET. Figure 7 shows typical gate-lag data from a Sc_2O_3 passivated AlGaN-cap HEMT. The Sc_2O_3 passivated HEMTs were typically able to restore 80-90% of the drain current loss relative to dc measurement conditions.

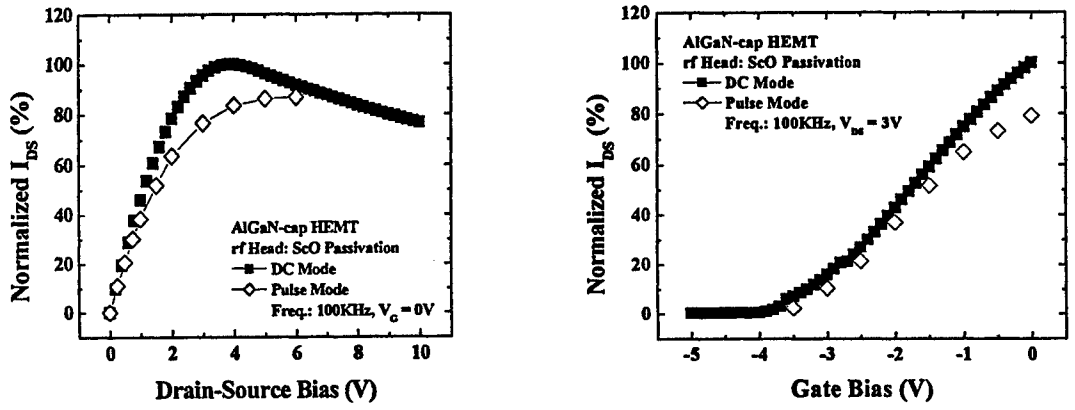


Figure 7. Gate lag measurements before and after Sc_2O_3 passivation of $0.5\times100\mu m^2$, AlGaN-cap HEMTs. At left V_G was switched from –5 to 0V, while at right it was switched from –5V to the value shown on the X-axis.

Similar results were obtained for MgO passivation, as shown in Figure 8. This may attributed to the in-situ cleaning procedure prior to deposition of oxides in the MBE chamber is not able to completely remove the native oxide from the AlGaN surface. The native oxides limit the effectiveness of the resulting passivation and account for the more variable results we observe for the AlGaN-cap devices.

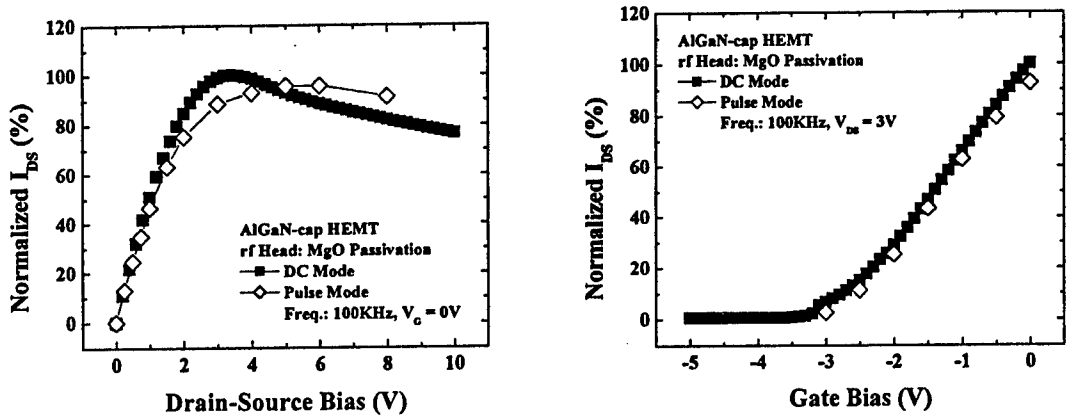


Figure 8. Gate lag measurements before and after MgO passivation of $0.5\times100\mu m^2$, AlGaN-cap HEMTs. At left V_G was switched from –5 to 0V, while at right it was switched from –5V to the value shown on the X-axis.

Conclusion

MgO and Sc_2O_3 thin films deposited by MBE showed very promising as the surface passivation layers on GaN based HEMTs. HEMTs with GaN-cap layer provide more effective mitigation of drain current collapse than AlGaN-capped HEMT. The Sc_2O_3 provides stable passivation characteristics over a period of at least 5 months, while the MgO was found less effectiveness under the same conditions. With respect to SiN_X passivation, we found no obvious advantage to the use of deuterated precursors for the deposition.

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Acknowledgments

The work at UF was partially supported by ONR (H. B. Dietrich, N00014-1-02-04) and NSF (DMR010438 and CTS 9901173).

Impact Ionization in High Performance AlGaN/GaN HEMTs

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Abstract

We report compelling evidence of impact ionization in high-performance AlGaN/GaN HEMTs. Relevant to the present paper, these devices also show excellent low-leakage DC properties that contain signatures of impact ionization in the output and sub-threshold characteristics. Temperature and bias dependent data are presented to support the identification of impact ionization in the devices.

I. Introduction

Gallium Nitride HEMTs are the focus of intense research and development for the realization of power amplifiers with high gain and record levels of power delivery. Very high power densities > 10W/mm have been published.[1] Assisted by significant momentum in Nitride-based optical devices, the materials growth and process techniques for electronic devices have been steadily improving. Such improvements would allow the observation of fundamental phenomenon reported in more-mature semiconductor materials. In the present paper, we report on a relatively well-known field-effect transistor phenomenon commonly referred to as the "kink effect," observed for the first time in GaN/AlGaN HEMTs. The "kink effect" simply describes an increase in the drain conductance of the device under open-channel operation at drain biases nominally greater than the bandgap of the channel. The effect is initiated by impact ionization of hot electrons in the drain-to-gate region of the device and proceeds with the accumulation of the impact-generated holes at the source-end of the channel. The impact-generated holes forward-bias the source-to-channel energy barrier thereby causing an increase in the drain conductance. The feedback process is well studied and documented in other materials, but the detailed mechanisms remain a subject of investigation.[2,3,4]

II. Growth and Process Details

The epitaxial materials were an $Al_{0.3}GaN_{0.7}$/GaN π-HEMT structure obtained from RF Nitro and grown at Cornell University. The device layers consisted of a conventional GaN/AlGaN HEMT single heterostructure on a 2" semi-insulating SiC substrate. The top AlGaN barrier was nominally

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30% Al with a thickness of 25nm. The charge was supplied to the channel from the surface through so-called piezoelectric-doping.[5] The transistors were fabricated at RSC in the baseline High Power Amplifier process using implant isolation, Ti/Al/Ti/Au Ohmic contacts, and a 0.25 μm electron-beam Pt/Au T-gate. The Ohmic contact resistance was in the range 0.5-0.8 Ω-mm. Measured DC device parameters show an I_{dss} of 1.2 A/mm, and a G_m of 230 mS/mm. The threshold voltage varied systematically across the wafer from -4 to –9 V. Small-signal RF measurements show extrapolated f_τ of 70GHz and f_{max} of 90 GHz. On-wafer large-signal measurements at X-band gave power densities as high as 6 Watts/mm on 100 μm devices, at modest drain voltages of 20-25 V. Measurements on 800 μm wide devices showed that power density was maintained above the 3 W/mm level for the same drain bias. The devices had a power density of 3.3 W/mm and a maximum output power of 2.63 Watts. This output power was achieved while maintaining a high gain of 9.2 dB, and a PAE of 44.3%.

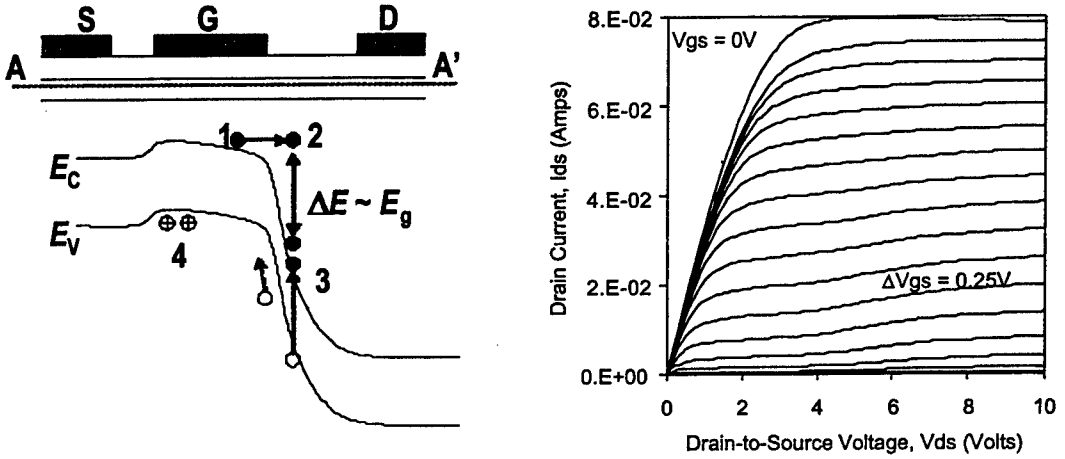


Figure 1 a) Schematic of the energy band diagram along the channel (A-A') showing electrons in the channel at 1 picking up energy from the drain voltage between 1 and 2. Impact ionization at 3 generates an electron hole pair. The impact-generated hole moves back towards the source along the channel to 4. At 4 the hole represents a positive charge that lowers the potential barrier, which increases the drain current. The holes at 4 are also collected by the negatively charged gate and contribute to the gate current. b) Output characteristics of a GaN/AlGaN HEMT with an 80 μm gate width The "kink" in the output characteristics is a direct result of the feedback mechanism described in Fig. 1a. Note the "kink" in the drain current occurs for drain biases greater than the bandgap of the GaN channel.

III. Experimental and results

Impact ionization in the channel affects device operation in many ways. The basic mechanism relevant to the present paper is described in Fig. 1a. In Fig. 1a electrons in the channel at 1 enter the high-field drift region between the gate and drain and pick up energy equal to the bandgap of the GaN channel at 2. These hot electrons undergo impact ionization, producing two conduction band

electrons and a hole in the valence band. The electrons are simply collected by the drain and by themselves do not account for the large increase in the drain conductance.[3] The holes at 3 are attracted to the source and the gate, and in some cases may be trapped in the barriers. The positive charge contributed by the holes that accumulate at 4 lower the barrier between the source and the channel and increases the drain conductance.

The room-temperature output characteristics of the GaN/AlGaN HEMT are shown in Fig. 1b. The increased output conductance or "kink" is evident at drain biases above 4V. The effect is more readily observed in a plot of the same output characteristics on a semi-log plot as shown in Fig. 2a. Measurement of the device at lower temperatures enhances the "kink" as shown in Fig. 2b for –50C. The enhancement of the output conductance at lower temperatures is consistent with the "kink" being associated with impact ionization: As the device temperature is reduced the electron mean-free-path increases and the impact ionization rate increases.

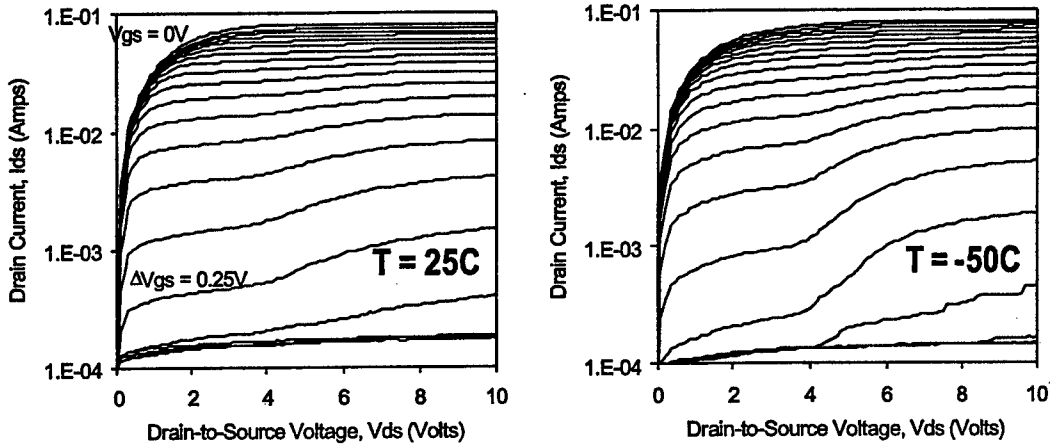
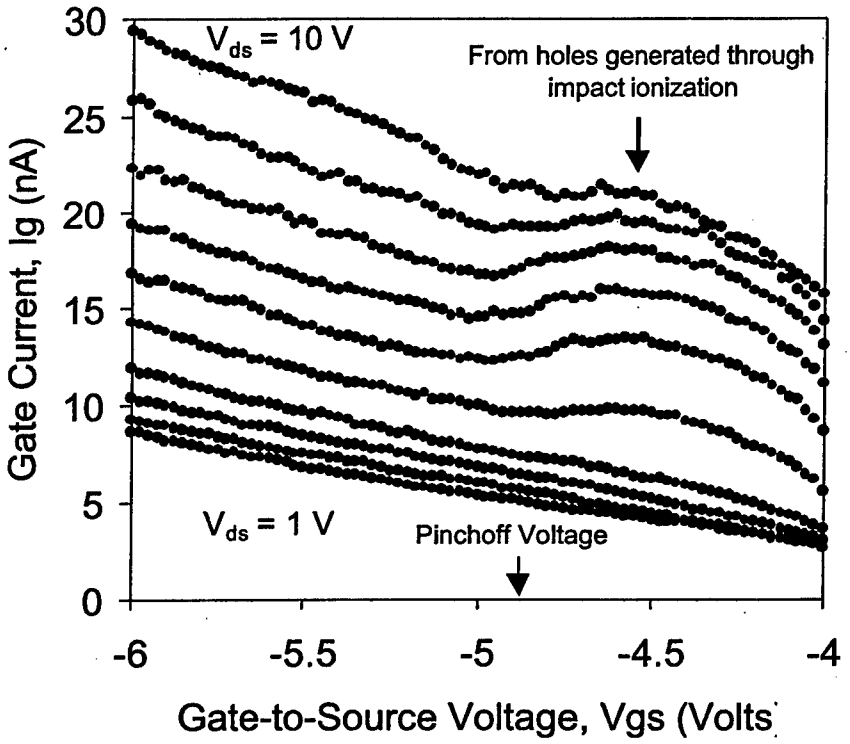


Figure 2 a) Output characteristics of an 80 μm wide AlGaN/GaN HEMT at room temperature. The logarithmic scale is chosen to highlight the increase in the output conductance at lower drain currents. V_{gs} is stepped from 0 to –5V. b) Output characteristics of the device from Fig. 1 at –50C. The impact ionization rates increase at lower temperatures and the enhancement in the output conductance is more pronounced.

The most important aspect of the devices described in the present paper is their low gate-leakage characteristics. Devices with low gate leakage allow us to probe the generation of holes with impact ionization directly, through an excess gate leakage. As described in Fig. 1a the holes that are generated are also attracted to the negatively charged gate. These holes, if collected by the gate, will provide an excess gate leakage current over and above the nominal gate leakage observed in the device. The excess gate leakage has the following unique dependencies on the applied bias: 1. The drain voltage has to be above the threshold for impact ionization (~ 4V from Fig. 2); 2. The excess

gate current will increase as the gate-to-drain voltage is increased; and 3. The excess gate current will decrease as the device nears pinch-off and the drain current in the channel is turned off. Such an unambiguous signature of impact ionization is found in the gate current for these devices.

The gate currents at –25C in these AlGaN/GaN HEMTs are plotted in Fig. 3 and clearly show an excess leakage that has the requisite functional dependence on drain current and drain voltage. We add that while the increase in the output conductance was seen on all our devices, the enhanced gate leakage in Fig. 3 was not as easily observed in all our devices and in all parts of the wafer. The device had to have a combination of high quality material allowing electrons to gain energy for impact ionization *and* low gate leakage to observe the signature of the impact-generated holes. In fact, the temperature of the device had to be lowered to –25 C to be able to observe the excess



current.

Additional measurements of gate leakage as a function of temperature, not shown here, seem to indicate that impact ionization continues to play a role in the sub-threshold region of device operation. Such measurements will be useful to monitor the quality of the GaN materials and may ultimately provide important information about breakdown and physics of failure of GaN/AlGaN

Figure 3. Gate current vs. gate voltage for various drain biases (from 1 to 10 V in 1V steps) at –25C. The "bump" in the gate current is a clear signature of impact ionization generated holes that are collected by the gate electrode and is only observed for drain voltages commensurate with the increase in the output conductance in figures 1 and 2. For a given drain voltage, the gate current increases above the ordinary leakage as the gate-to-drain voltage increases. As the device pinches-off at -5V, the drain current decreases and the number of holes generated by the impact ionization also decrease causing the excess gate leakage to decrease.

HEMTs.

IV. Conclusions

The DC characteristics of our low-leakage high-performance GaN/AlGaN HEMTs show compelling evidence of impact ionization of hot electrons in the GaN channel. The impact ionization process generates holes that increase both the output conductance and the gate leakage in these devices with a nominal bias threshold associated with the bandgap of the GaN channel. Lowering the temperature enhances these signatures due to an increase in the impact ionization rate of the hot electrons. The voltage and current dependence of the gate leakage arising from the impact-generated holes is shown to be consistent with our claim.

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Ohmic Contact Technology in III-V Nitrides Using Polarization Effects in Cap Layers

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Abstract

A novel technology for low-resistance ohmic contacts to III-V nitrides is presented. The contacts employ polarization-induced electric fields in strained cap layers grown on lattice-mismatched III-V nitride buffer layers. With appropriate choice of the cap layer, the electric field in the cap layer reduces the thickness of the tunnel barrier at the metal contact / semiconductor interface. Design rules for polarization-enhanced contacts are presented giving guidance for composition and thickness of the cap layer for different III-V nitride buffer layers. Experimental results for ohmic contacts with p-type InGaN and GaN cap layers are markedly different from samples without a polarized cap layer thus confirming the effectiveness of polarization-enhanced ohmic contacts.

Introduction

Ohmic contacts with specific contact resistances in the 10^{-4} $\Omega\,cm^2$ range or smaller are imperative to minimize parasitic voltage drops and to increase the reliability and lifetime of optoelectronic devices such as heterobipolar transistors, light-emitting diodes, and lasers [1]. Ohmic contacts in most III-V semiconductors are achieved by heavily doping the contact region thereby reducing the tunnel-barrier thickness at the metal / semiconductor interface.

The wide bandgap and large electron affinity of III-V nitrides compared to other III-V semiconductors generally result in high Schottky barriers for metal contacts to p- and n-type material. In addition, the large thermal activation energy of p-type dopants in III-V nitrides [2] makes it difficult to create heavily doped layers with high free-hole concentrations. It is therefore particularly challenging to form low-resistance ohmic contacts to p-type III-V nitrides.

Several approaches have been used to fabricate low-resistance ohmic contacts to p-type III-V nitride compounds such as deposition of high-work function metals with subsequent alloying at elevated temperatures [3-6], deposition of conductive oxides [7,8], and various types of surface treatments [9]. Extensive stability studies for alloyed metal contacts have been performed [10].

A completely different approach to reduce the tunneling barrier width is based on the use of strained cap layers or superlattices pseudomorphically grown on top of the III-V nitride semiconductor of interest [11, 12, 13]. Strain-induced as well as spontaneous polarization result in electric fields that tilt the conduction and valence bands in the cap layers in such a way that tunneling of charge carriers through the barrier can be drastically enhanced. A significant advantage of this approach is its limited reliance on doping, the metallization type, and annealing conditions.

In this work, the theory of polarization-enhanced ohmic contacts using strained cap layers is discussed. Practical guidance is given for the selection of suitable cap / buffer layer combinations

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including the composition and thickness of the cap layers. Experimental results are presented that show the viability of polarization-enhanced ohmic contacts. InGaN caps on GaN, and GaN caps on AlGaN, significantly reduce the contact resistances as compared to contacts not utilizing cap layers.

Theory

The magnitude of polarization fields in III-V nitrides is well known [14 - 18]. The piezoelectric polarization of a generalized wurtzite III-V nitride cap layer $X_xY_{1-x}N$ (X and Y represent a group-III element such as Al, Ga, or In) pseudomorphically grown on a relaxed buffer layer depends on the strain in the basal plane of the wurtzite crystal

$$\varepsilon_\perp(x) = [a_{buff} - a(x)] / a(x) = \Delta a / a \tag{1}$$

with the equilibrium lattice constants of the buffer, a_{buff}, and the cap layer, $a(x)$. Values of the equilibrium lattice constant and strain for different III-V nitrides are given in ***Tab.*** 1 and ***Fig.*** 1. By taking into account second order effects, the piezoelectric polarizations along the c-direction of strained binary layers can be written as [17,18]

$$P^{pz}_{AlN} = [-1.808\varepsilon_\perp + 5.624\varepsilon_\perp^2]\ \mathrm{C\,m^{-2}} \quad \text{for } \varepsilon_\perp < 0 \tag{2a}$$

$$P^{pz}_{AlN} = [-1.808\varepsilon_\perp - 7.888\varepsilon_\perp^2]\ \mathrm{C\,m^{-2}} \quad \text{for } \varepsilon_\perp > 0 \tag{2b}$$

$$P^{pz}_{GaN} = [-0.918\varepsilon_\perp + 9.541\varepsilon_\perp^2]\ \mathrm{C\,m^{-2}} \tag{2c}$$

$$P^{pz}_{InN} = [-1.373\varepsilon_\perp + 7.559\varepsilon_\perp^2]\ \mathrm{C\,m^{-2}} \tag{2d}$$

with the piezoelectric polarization in a strained *ternary* layer (in $\mathrm{C\,m^{-2}}$) given by a Vegard-like law.

$$P^{pz}_{X_xY_{1-x}N}(x) = xP^{pz}_{XN}[\varepsilon_\perp(x)] + (1-x)P^{pz}_{YN}[\varepsilon_\perp(x)]\ . \tag{3}$$

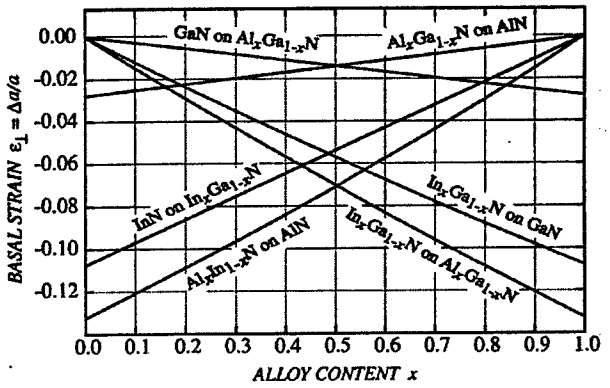


Fig. 1. Elastic strain $\varepsilon_\perp$ in the basal plain of Ga-faced $X_{1-x}Y_xN$ compounds pseudomorphically grown as cap layers on top of relaxed III-V nitride buffer layers. Negative values of $\varepsilon_\perp$ indicate compressive strain.

		Cap layer					
		AlN	$Al_xGa_{1-x}N$	$Al_xIn_{1-x}N$	GaN	$In_xGa_{1-x}N$	InN
Buffer layer (Ga-face)	AlN	3.1095 Å					
	$Al_xGa_{1-x}N$		(3.1986 -0.0891 x) Å				
	$Al_xIn_{1-x}N$			(3.5848 - 0.4753 x) Å			
	GaN				3.1986 Å		
	$In_xGa_{1-x}N$					(3.1986 +0.3862 x) Å	
	InN						3.5848 Å

Tab. 1. Cap / buffer layer combinations for polarization-enhanced ohmic contacts to Ga-faced wurtzite III-V nitride semiconductors. Shaded regions show combinations resulting in a compressively strained cap layer suitable for p-type contacts to $X_xY_{1-x}N$ compounds. The diagonal elements of the table contain the respective in-plane lattice constants taken from ref. [17].

The spontaneous polarization can be expressed by [17]

$$P^{sp}_{Al_xGa_{1-x}N}(x) = [-0.09x - 0.034(1-x) + 0.019x(1-x)]\ \mathrm{Cm}^{-2} \tag{4a}$$

$$P^{sp}_{In_xGa_{1-x}N}(x) = [-0.042x - 0.034(1-x) + 0.038x(1-x)]\ \mathrm{Cm}^{-2} \tag{4b}$$

$$P^{sp}_{Al_xIn_{1-x}N}(x) = [-0.09x - 0.042(1-x) + 0.071x(1-x)]\ \mathrm{Cm}^{-2}\ . \tag{4c}$$

To obtain the electric field $\mathcal{E}^{pol}$ in the cap layer caused by the spontaneous and piezoelectric polarization fields P^{sp}_{cap}, P^{sp}_{buff}, and P^{pz}_{cap}, it is assumed that the free charge density inside the sample is negligible; therefore $\nabla \boldsymbol{D} = 0$ with $\boldsymbol{D}$ being the dielectric displacement field. The displacement fields $\boldsymbol{D}_{(i)}$ in the cap and buffer layers may be written as [19]

$$\boldsymbol{D}_i = \varepsilon_0 \varepsilon_i \mathcal{E}_i + \boldsymbol{P}^{sp}_i + \boldsymbol{P}^{pz}_i \qquad (i = \mathrm{cap, buff}) \tag{5}$$

where ε_0 is the dielectric permittivity of vacuum; ε_{cap} and ε_{buff} are the relative dielectric constants in the cap and buffer layer, respectively, and may be obtained from the relationship $\varepsilon_{X_xY_{1-x}N}(x) = x\varepsilon_{XN} + (1-x)\varepsilon_{YN}$. Using the boundary condition $D_{n,cap} = D_{n,buff}$ at the cap /

buffer interface with D_n denoting the component of $\boldsymbol{D}$ normal to the interface, $\mathcal{E}^{pol} \equiv \mathcal{E}_{cap}$ is given by

$$\mathcal{E}^{pol} = \frac{1}{\varepsilon_0 \varepsilon_{cap}} \left(- P^{pz}_{cap} - P^{sp}_{cap} + P^{sp}_{buff} \right) + \frac{\varepsilon_{buff}}{\varepsilon_{cap}} \mathcal{E}_{buff} \ . \tag{6}$$

The field $\mathcal{E}_{buff}$ will be screened by free charge carriers as soon as the tilted conduction or valence bands in the buffer layer come close to the Fermi level; this condition allows to obtain an upper limit for $\mathcal{E}_{buff}$ according to

$$\mathcal{E}_{buff} d_{buff} \leq \frac{E_{G,buff}}{e} \tag{7}$$

where e is the elementary electric charge and $E_{G,buff}$ and d_{buff} denote the bandgap energy and the thickness of the buffer layer, respectively. For GaN and thicknesses $d_{buff} > 300$ nm the value of the field $\mathcal{E}_{buff}$ is about 10^7 V/m or smaller; this may be neglected compared to typical values $P^{pz}_{X_xY_{1-x}N} / (\varepsilon_0 \varepsilon_{X_xY_{1-x}N}) \geq 10^8$ V/m in strained III-V nitrides [16,17,18]. Eq. (6) may therefore be approximated

$$\mathcal{E}^{pol} \approx \frac{1}{\varepsilon_0 \varepsilon_{cap}} \left(- P^{pz}_{cap} - P^{sp}_{cap} + P^{sp}_{buff} \right) . \tag{8}$$

It turns out that for *compressive strain* ($\varepsilon < 0$, see ***Fig.*** 1), $\mathcal{E}^{pol}$ as obtained from Eq. (8) points along the *negative* c-direction of the Ga-faced wurtzite crystal, that is, towards the substrate. In the case of p-type III-V nitride materials this results in a *decrease* of the tunnel barrier thickness and will therefore be beneficial to attain smaller specific contact resistances. ***Tab.*** 1 summarizes possible cap/buffer layer combinations resulting in compressive strain in the cap layer.

For strong enough electric fields or sufficiently thick cap layers, the formation of a two-dimensional hole gas at the interface between the cap and the buffer layers will occur. The density p_{2DHG} of the two-dimensional hole gas can be calculated by numerically solving the condition for the constancy of the Fermi level (see ***Fig.*** 2 (a)).

$$e\Phi_B + e d_{cap} \mathcal{E}_{tot} + (E_0 - E_V) + (E_F - E_0) = 0 \tag{9}$$

In Eq. (9), d_{cap} denotes the thickness of the cap layer, $\mathcal{E}_{tot}$ the total electric field in the cap layer, Φ_B the Schottky barrier height, E_V the valence band energy at the cap / buffer layer interface; E_F and E_0 are the Fermi energy and the energy of the 2DHG groundstate, respectively. The terms on the left-hand side in Eq. (9) are given by

$$e\Phi_B = E_{G,cap} - e(\Phi_M - \chi_{cap}) \tag{10a}$$

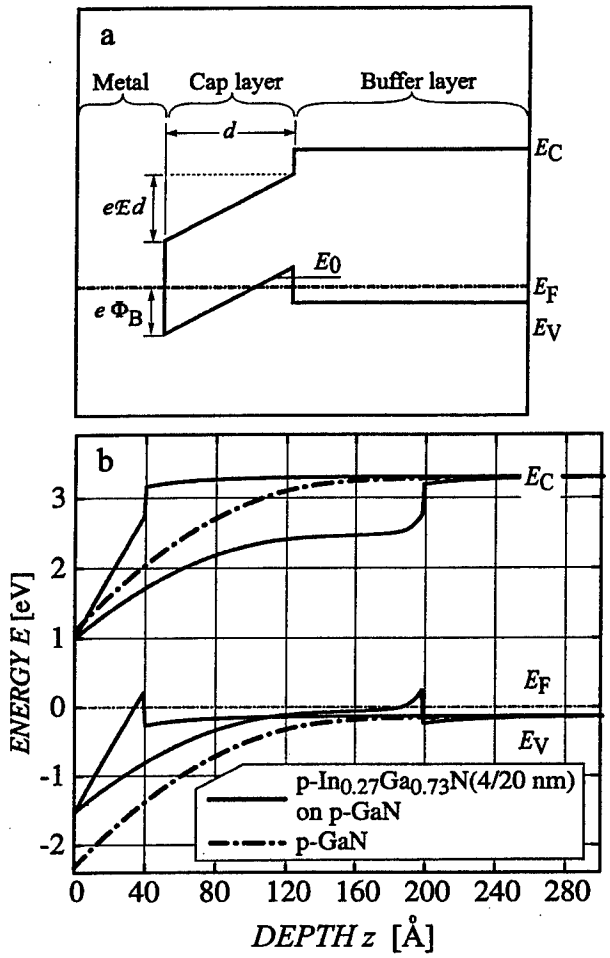


Fig. 2 (a) Schematic band diagram for a polarization-enhanced contact employing a strained p-type III-V nitride cap layer pseudomorphically grown on top of a relaxed III-V nitride buffer layer. E_0 denotes the groundstate energy of a 2DHG formed in the triangular barrier at the interface between cap and buffer layer, d the cap layer thickness, $\mathcal{E}$ the electric field in the strained cap layer, Φ_B the Schottky barrier height. (b) Self-consistently calculated band diagram [22] for Ni-contacts to bulk p-type GaN and to polarization-enhanced structures consisting of strained p-$In_{0.27}Ga_{0.73}N$ cap layers (d = 4 nm and d = 20 nm) on top of relaxed p-GaN. The dopant concentration was assumed to be 10^{19} cm^{-3}.

$$\mathcal{E}_{tot} = \mathcal{E}^{pol} + \frac{e\, p_{2DHG}}{\varepsilon_{cap}\, \varepsilon_0} \tag{10b}$$

$$E_0 - E_V = \frac{3}{2}\left[\frac{3}{2}\frac{e^2\hbar}{\varepsilon_{cap}\varepsilon_0\sqrt{m^*}}\, p_{2DHG}\right]^{2/3} \tag{10c}$$

$$E_F - E_0 = \frac{\pi\hbar^2}{m^*} p_{2DHG} \tag{10d}$$

In Eq. (10a), $E_{G,cap}$, χ_{cap} are the bandgap energy and the electron affinity of the cap layer, Φ_M is the work function of the contact metal; here we use the work function of Ni of Φ_M = 5.2 eV. The ternary bandgap energy can be obtained from

$$E_{G,X_xY_{1-x}N} = x\,E_{G,XN} + (1-x)\,E_{G,YN} - b\,x\,(1-x) \tag{11}$$

where a bowing parameter b=2.5 eV [15] is used; the ternary electron affinity may be obtained from linear interpolation of the respective binary values according to

$$\chi_{X_xY_{1-x}N} = x\,\chi_{XN} + (1-x)\,\chi_{YN}\ . \tag{12}$$

In Eq. (10c), $E_0 - E_V$ is calculated using the Fang-Howard approximation [20] for energy states in a triangular well. The effective hole mass m^* in the cap layer is $1.0 \times m_0$, and $\hbar$ is Planck's constant divided by 2π. $E_F - E_0$ in Eq. (10d) is calculated using the high-density approximation of the Fermi-Dirac distribution and the two-dimensional density of hole states $\rho_{2D} = m^* / (\pi\hbar^2)$.

Tunneling from the contact metal into the cap layer requires the existence of unoccupied valence band states in the cap layer. This condition allows one to calculate the minimum thickness of the cap layer

$$d_{min} = -\frac{\Phi_B - E_0/e}{\mathcal{E}_{tot}} \approx -\frac{\Phi_B}{\mathcal{E}_{tot}} \tag{13}$$

corresponding to the minimum thickness required for the formation of a 2DHG. The approximation in Eq. (13) is valid if quantum-size effects in the triangular potential well at the cap / buffer layer interface are neglected, in analogy to the approach in [21]. Thus Eq. (13) is the solution of Eq. (9) for $p_{2DHG} = 0$, the onset of the 2DHG.

Fig. 2 (b) shows self-consistently calculated band diagrams [22] for $In_{0.27}Ga_{0.73}N$ cap layers on GaN with two different cap layer thicknesses, d = 4 nm and d = 20 nm, as well as the band diagram of bulk p-type GaN. We assumed a uniform Mg dopant concentration of $N_{Mg}=10^{19}$ cm^{-3} with an acceptor activation energy of E_a = 50 meV in the capping layer obtained by extrapolating the values of E_a given in ref [23] towards larger In-contents. Nickel was used in the calculation as the contact metal.

It can be seen that for the thicker cap layer, the Schottky barrier width approaches that of bulk p-type GaN; therefore no reduction of the specific contact resistance compared to p-type GaN can be expected.

Figure 3 shows the dependence of the electric field $\mathcal{E}^{pol}$ for various cap / buffer layer configurations. Also included is the dependence of d_{min} on the electric field in the cap layer calculated from Eq. (13) assuming $\mathcal{E}_{tot} = \mathcal{E}^{pol}$ and using the barrier heights Φ_B of Ni on GaN (Φ_B = 2.3 V), InN (Φ_B = 1.3 V), and AlN (Φ_B = 1.8 V). As an example, the minimum thickness of an $In_{0.27}Ga_{0.73}N$ cap layer on a GaN buffer layer can be determined to be between 2 and 4 nm.

According to the WKB approximation the tunneling probability T^* through a triangular barrier for holes with energy $E = 0$ is given by

$$T^* = \exp\left[-\frac{4\Phi_B^{3/2}\sqrt{2m^* e}}{3\hbar|\mathcal{E}_{tot}|}\right]. \tag{14}$$

By using the slope of the valence band at $z = 0$ in ***Fig.*** 2 (b) to estimate the electric field $\mathcal{E}_{tot}$ a tunneling probability $T^* \approx 10^{-8}$ can be obtained for the cap layer with thickness $d = 4$ nm, which is much larger than the value $T^* \approx 10^{-24}$ for the 20 nm thick cap layer. It is therefore prudent to not exceed the minimum cap layer thickness d_{min} by more than a factor of two.

The cap layer will change the barrier height as compared to a no-cap layer situation. Note, however, that the barrier thickness is much more important than the barrier height. This is because the thickness can vary by a larger factor than the barrier height and also because the tunneling probability has a stronger dependence on the thickness as compared to the barrier height [see Eq. (13) and Eq. (14)]. Therefore it is reasonable to assume that the change in barrier height will be of minor importance.

The electric fields $\mathcal{E}^{pol}$ shown in ***Fig.*** 3 are similar or even larger than the critical fields $\mathcal{E}_c$ in InN ($\mathcal{E}_c \approx 1 \times 10^8$ V/m), GaN ($\mathcal{E}_c \approx 3 \times 10^8$ V/m), and AlN ($\mathcal{E}_c \approx 9 \times 10^8$ V/m) obtained from a power law relationship [24]. For doped samples, however, $\mathcal{E}^{pol}$ will be reduced by free charge carriers and ionized impurities. In addition, if d_{min} approaches the critical thickness of the cap layer for pseudomorphic growth, the onset of elastic strain relaxation will result in further reduced fields $\mathcal{E}^{pol}$. Therefore minimum cap layer thicknesses obtained from ***Fig.*** 3 have to be regarded as a lower limit.

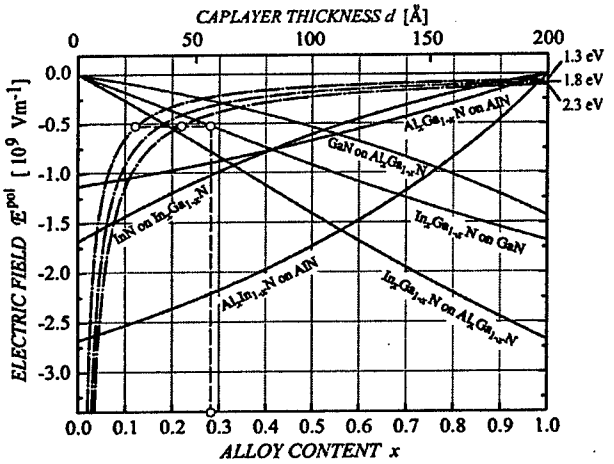


Fig. 3. Polarization-induced electric field $\mathcal{E}^{pol}$ in Ga-faced $X_{1-x}Y_xN$ cap layers pseudomorphically grown on different buffer layers (strain relaxation due to critical thickness effects is not taken into account). Negative values indicate that the $\mathcal{E}^{pol}$ vector points towards the buffer layer. The dashed-dotted curves correspond to the cap layer thickness d_{min} given by Eq. (9) using Schottky barrier heights $e\Phi_B$ for Ni on GaN ($e\Phi_B$ = 2.3 eV), on InN ($e\Phi_B$ = 1.3 eV), and on AlN ($e\Phi_B$ = 1.8 eV) . As an example, the dashed lines indicate how to determine the thickness d_{min} of an $In_{0.27}Ga_{0.73}N$ cap layer on GaN.

Experimental results

Several experiments were conducted to confirm the validity of polarization-enhanced contacts. Here we report on the marked difference in the I-V characteristic obtained for samples with and without a cap layer. Detailed experimental studies on contact resistances have been reported elsewhere [11, 12].

Metallic contacts (Ni / Au and Pd / Au) were deposited by electron beam evaporation using lift-off photolithographic techniques. The contacts were square-shaped pads (200 μm × 200 μm) separated by 2, 4, 6, 8, 10, and 15 μm wide gaps. To remove surface oxide layers, the samples were treated with a buffered-oxide etch (BOE) or in a solution containing 20 % HF and 80 % H_2O. Subsequently, the contacts were annealed in a rapid thermal annealing furnace at 500° C in either nitrogen (Pd / Au contacts) or oxygen (Ni / Au contacts) ambient. The contact resistances were determined from current-voltage (I-V) measurements using the transfer length method (TLM).

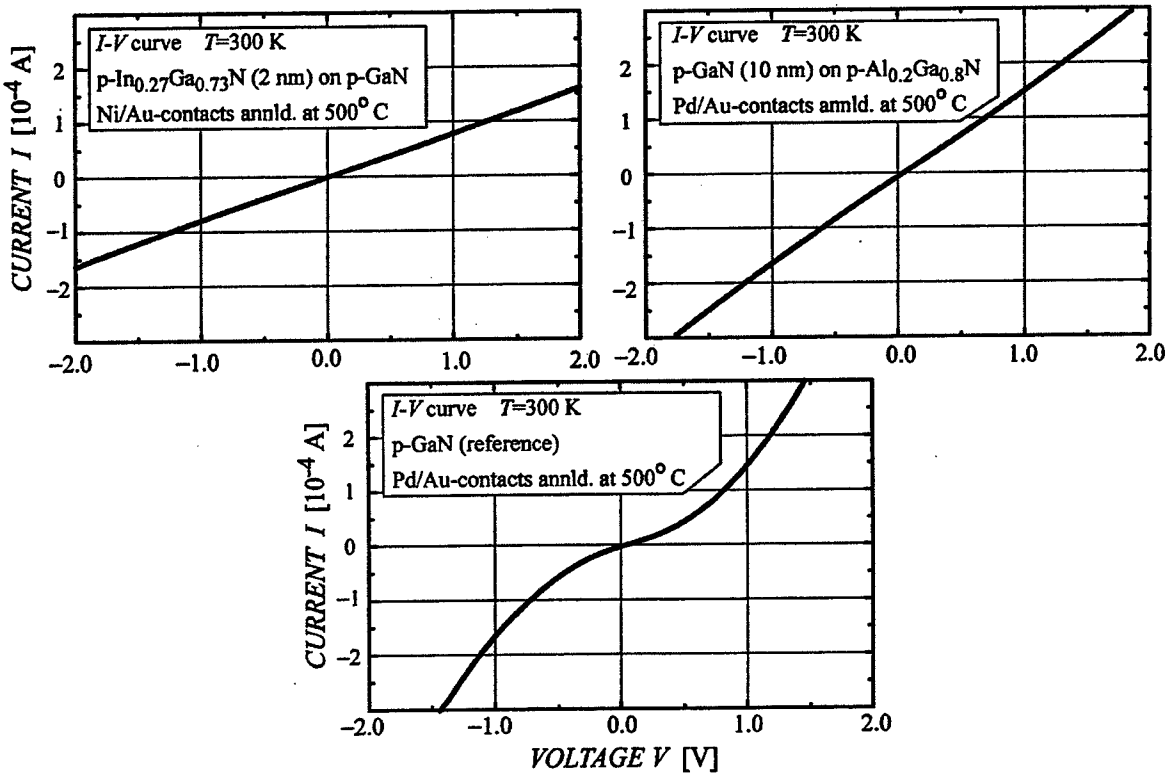


Fig. 4. I-V curves for ohmic contacts to p-type GaN and for polarization-enhanced contacts utilizing InGaN-on-GaN or GaN-on-AlGaN cap layer structures. The data are obtained for TLM pads with a separation of 10 μm.

Fig. 4 shows the I-V curves of samples with an $In_{0.27}Ga_{0.73}N$ cap layer on a GaN buffer, a GaN-on-$Al_{0.2}Ga_{0.8}N$ superlattice structure and a p-type GaN reference sample. The thicknesses $d = 2$ nm of the InGaN cap layer and d = 10 nm of the GaN cap layer agree well with the respective minimum thicknesses d_{min} that can be obtained from ***Fig.*** 3.

Inspection of ***Fig.*** 4 shows that excellent ohmic I-V characteristics were found for both samples containing cap layers. However the I-V characteristic for the p-type GaN reference sample is markedly nonlinear. This clearly indicates the advantageous effect of polarization fields in the cap layers. Specific contact resistances of $\rho_c = 6 \times 10^{-3}\ \Omega\ cm^2$ for the InGaN cap layer and $7 \times 10^{-4}\ \Omega\ cm^2$ for the GaN cap layer were determined. Additional experimental results have been reported elsewhere [11, 12].

The two experimental examples reported here, namely the InGaN cap on GaN layers and the GaN cap on AlGaN layers have great practical importance. It is expected that the InGaN cap layer can be applied to LEDs emitting in the visible spectrum. Such LED's usually have GaN upper cladding layers. Furthermore, the GaN cap layer on AlGaN buffers will be useful for UV LEDs and lasers. Such devices usually have AlGaN upper cladding layers.

Conclusion

A novel technology for low-resistance ohmic contacts to III-V nitrides is presented. Strong polarization fields exist in III-V nitrides pseudomorphically grown as thin non-lattice-matched cap layers on top of relaxed III-V nitride buffer layers. The corresponding electric fields in Ga-faced cap layers are calculated for different cap / buffer layer combinations and are on the order of $10^9\ V\ m^{-1}$. It is shown that a GaN cap on AlGaN, an InGaN cap on GaN, and other material combinations are suited for low-resistance p-type ohmic contacts to III-V nitrides.

For a proper choice of cap and buffer layer, the tunneling barrier thickness at the contact metal / semiconductor interface is drastically reduced as a result of band tilting in the cap layer region. For p-type contacts, enhanced by polarization effects, the hole tunneling probability through the surface barrier is increased by more than ten orders of magnitude compared to bulk p-type GaN without cap layer.

The beneficial effect of cap layers is demonstrated experimentally for an $In_{0.27}Ga_{0.73}N$-on-GaN structure and a GaN-on-$Al_{0.2}Ga_{0.8}N$ structure. As opposed to a p-type GaN reference sample, excellent linearity of the I-V characteristics independent of the choice of contact metalization was achieved for the polarization-enhanced contacts. The specific contact resistances obtained from the TLM-method were $\rho_c = 6 \times 10^{-3}\ \Omega\ cm^2$ for the InGaN cap layer and $7 \times 10^{-4}\ \Omega\ cm^2$ for the GaN cap layer.

Acknowledgment

This work was supported by Office of Naval Research (Dr. Colin E. C. Wood), the University of New Mexico (Dr. Stephen Hersee), and the National Science Foundation.

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AlGaN/GaN-HEMTs for Power Applications up to 40 GHz

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Abstract

A 0.15 µm T-gate AlGaN/GaN-HEMT 2-inch technology has been developed. Transistors with 120 µm gatewidth show a peak transconductance of 300 mS/mm and cut-off frequencies f_t and f_{max} of 65 GHz and 149 GHz, respectively. Large periphery 720 µm gatewidth devices are capable of CW operation up to 40 GHz yielding an output power of 0.91 W and a linear gain of 6 dB at 35 GHz. To the authors' knowledge these results represent the highest absolute power level so far achieved with a GaN-HEMT in the K_a-band.

Introduction

There is a steadily growing interest in AlGaN/GaN based high electron mobility transistors (HEMTs) on SiC substrates for microwave power applications driven by the much higher power densities achievable compared to competitive technologies. The main advantages of GaN over Si and GaAs are its high electric breakdown field, the high electron saturation velocity as well as the high sheet charge of the two dimensional electron gas (2DEG). Based on these advantages, the GaN technology offers large potential to surpass existing device limitations in operation voltage, RF output power and low impedance level.
So far, absolute power performance of GaN devices has mainly been demonstrated up to 20 GHz [1,2]. For higher frequencies power measurements have been made only with small periphery devices [3]. This paper, for the first time presents absolute power levels for realistic power cells in the K_a-band.

Device Technology

The HEMT structures were grown on semi-insulating SiC substrates by metal organic vapor phase epitaxy (MOVPE) in an AIXTRON 2000 6x2"multi-wafer reactor. The epitaxial structure consists of the following layers: a 0.35 µm undoped AlGaN layer, a 2.7 µm undoped GaN buffer, a 5 nm undoped $Al_{0.25}GaN$ spacer, a 10 nm Si-doped $Al_{0.25}GaN$ supply layer, a 10 nm undoped $Al_{0.25}GaN$ barrier and a 2 nm thick GaN cap layer. From Hall measurements typical sheet carrier concentrations and electron mobilities of $8x10^{12}$ cm^{-2} and 1400 cm^2/Vs respectively, were obtained. Sheet resistance mappings proved an excellent uniform sheet resistance of 450 Ω/sq and a standard deviation of 1.5 %.
Device fabrication was done on full 2" wafers by contact lithography. Device isolation was accomplished by a 180 nm deep mesa dry etch into the GaN buffer by chemically assisted ion beam etching using chlorine. Ti/Al/Au alloyed ohmic contacts were annealed at 825 °C for 30 s yielding an average ohmic contact resistance of 0.6 Ωmm. The T-shaped Ni/Au -gates with gatelengths of 0.15, 0.3 or 0.5 µm were defined by electron-beam lithography using a 3-layer resist. All devices were passivated by a 100 nm thick SiN layer and multi-finger transistors were fabricated using first level metal interconnects and galvanic Au air bridges.

Device Data

A typical DC transfer characteristics of the 0.15 µm AlGaN/GaN HEMTs with gatewidth of 2x60 µm is depicted in figure 1. The transistors show a peak transconductance g_m of 300 mS/mm and a maximum drain current I_D of 1.12 A/mm. Figure 2 exhibits the extracted f_t and f_{max} values for a 2x60 µm gatewidth device. Values of f_t = 65 GHz and f_{max} = 149 GHz are achieved. The gatewidth scaling of f_t and f_{max} is presented in figure 3 for devices with 60 µm, 90 µm and 120 µm gatefingers and different number of fingers. Apparently f_{max} scales with the total gatewidth but even the HEMT with the largest 10x120 µm gatewidth still shows an f_{max} of 60 GHz. As expected, f_t remains fairly constant. As seen in figure 4,

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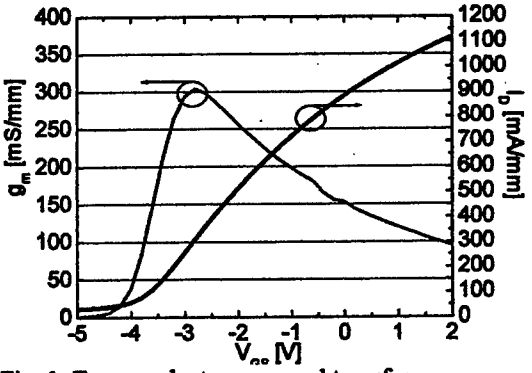


Fig. 1: Transconductance g_m and transfer characteristics for V_{DS} = 7 V of a 0.15x 120 µm AlGaN/GaN-HEMT.

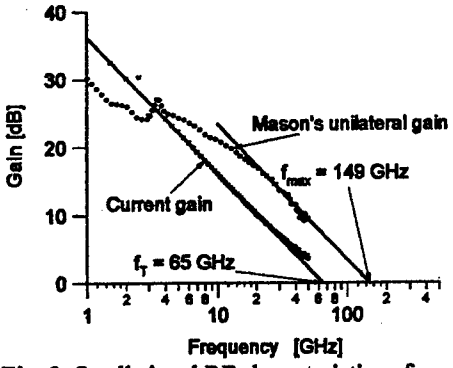


Fig. 2: Small signal RF characteristics of 0.15x120 µm AlGaN/GaN-HEMT.

S-parameters can be modeled with good accuracy between 0.25 and 120 GHz using a standard eight element small-signal equivalent circuit. At V_{DS} = 7 V, an intrinsic RF-g_m = 416 mS/mm, a C_{GS} = 0.78 pF/mm, a g_{DS} = 32 mS/mm and a C_{GD} = 0.105 pF/mm are obtained.
Load-pull measurements were carried out in the 2-40 GHz frequency range showing excellent performance of our GaN devices but emphasis was put on the K_a-band. Figure 5 presents the power performance at 30 GHz and at V_{DS} = 26 V for a HEMT with 8x90 µm = 720 µm gatewidth. A record CW output power of 1.1 W with a power density of 1.52 W/mm and a linear gain of > 6 dB was achieved. Figure 6 shows the results for the same large periphery device operating at 35 GHz. A CW output power of 910 mW was obtained with a slightly lower power density value of 1.26 W/mm and still a linear gain of 6 dB. These results show the potential of our 0.15 µm T-gate AlGaN/GaN HEMT technology for the realisation of power amplifier stages with AlGaN/GaN-HEMTs for the K_a-band. Reducing the gatewidth from 720 µm to 480 µm improves the transistor performance only marginally. As shown in figure 7 the maximum CW output power density amounts to 1.31 W/mm with a gain of > 6 dB. But more important the influence of operation temperature on the transistor performance can be seen additionally in figure 7. Operating the device at 100°C distinctly reduces the available output power from 0.63 W to 0.48 W corresponding to a 30% decrease. This clearly reveals the trade-off between high temperature operation and available output power. Therefore thermal management is considered an important aspect in power amplifier design.
In summary, our results are promising for the application of this technology in the K and K_a-band for satellite communication and high performance radar.

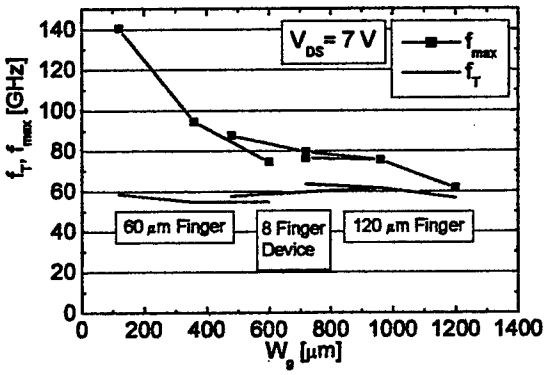


Fig. 3: Gatewidth scaling of f_T and f_{max} versus gatewidth W_g at V_{DS} = 7 V for different gatefinger lengths (60, 90, 120 µm) and different number of fingers.

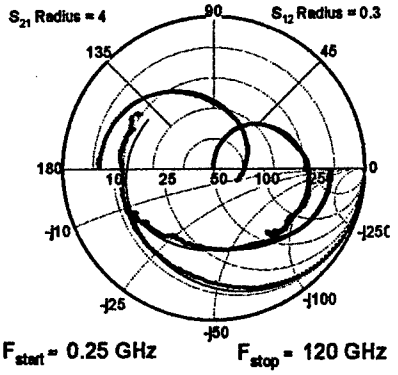


Fig. 4: Measured (x) and modeled (-) S-parameters between 0.25 GHz and 120 GHz.

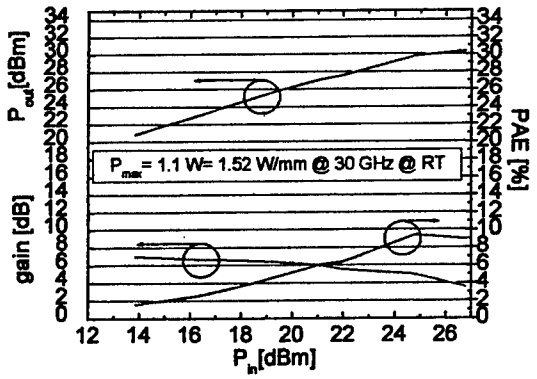


Fig. 5: Power characteristics of a 0.15 µm AlGaN /GaN-HEMT with a gatewidth W_g = 8x90 µm = 720 µm measured at 30 GHz and V_{DS} = 26 V

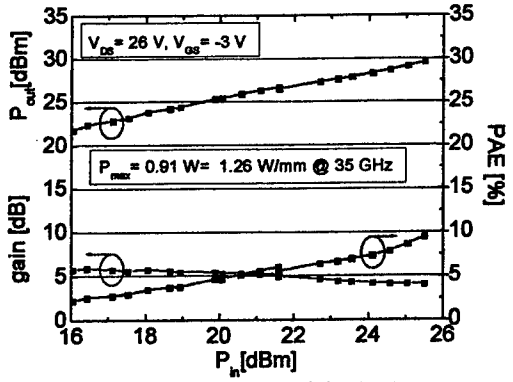


Fig. 6: Power characteristics of the 0.15 µm AlGaN/GaN HEMT as given in figure 5 but measured at 35 GHz and V_{DS} = 26 V.

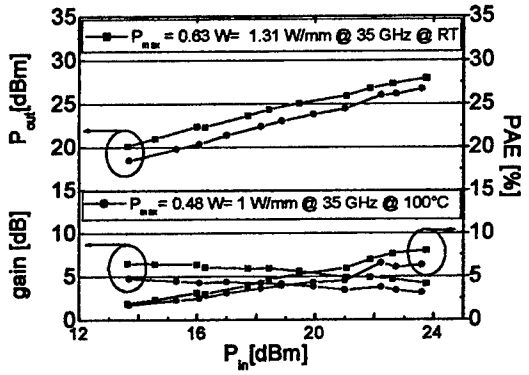


Fig. 7: Power characteristics of a 0.15 µm GaN HEMT with a gatewidth W_g = 8x60 µm = 480 µm measured at 35 GHz and V_{DS} = 26 V and two different substrate temperatures(RT=20°C, 100°C).

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Acknowledgements

This work was supported by the German Ministry for Education and Research (BMBF).

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