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During this grant period we have taken our established single junction process to the next step in realizing a very large scale Josephson integrated circuit technology. We have made many process level improvements to address nonuniformity issues. We have fabricated identical junction pairs to study the mutual interactions between junctions. We have also fabricated arrays of 10, 50, and 100 junctions and have demonstrated a giant Shapiro step in the 10 junction case. Lastly we have updated and improved our measurement system and capabilities.

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Applications of High T_c Planar Josephson Technology
Final Report AFOSR Grant F49620-01-1-0174 (2001-2004)
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I. Introduction

In an earlier funding period we demonstrated a process for manufacturing single S-S'-S Josephson junctions from high temperature superconducting material (YBCO). This process holds many advantages over competing junction technologies. Our junctions are planar with all *a-b* plane conduction with no interfaces between different materials. Our technique has fewer processing steps which simplify fabrication while minimizing adverse reactions between the superconductor and process reagents. It employs the same equipment used in semiconductor microelectronics processing which makes this technology suitable for integration with VLSI semiconductor electronics. For many relevant DOD applications a junction technology is desired to fabricate large numbers of junctions in a series array with a 5-10% tolerance in operating parameters and to keep the junctions closely spaced (sub-micron) so that the junction array may be treated as a lumped element, which considerably simplifies circuit design. During this funding period 2001-2004 we have made substantial progress in obtaining these goals and have begun to transfer this technology to Northrop Grumman and ultimately the Air Force.

II. Approach

It has been well documented that ion implantation introduces disorder into HTS films by creating point defects with high anneal energies.¹ This disorder increases the resistivity and lowers the T_c of the material. Fluences in the example in figure 1 of Ne⁺ at 1MeV and doses of the order of 2×10^{13} ions/cm² result in metallic material with a lower T_c than the original film.² Selectively disordering by masking all but narrow S' regions can result in SS'S junctions where S' denotes a reduced T_c superconductor (figure 3).

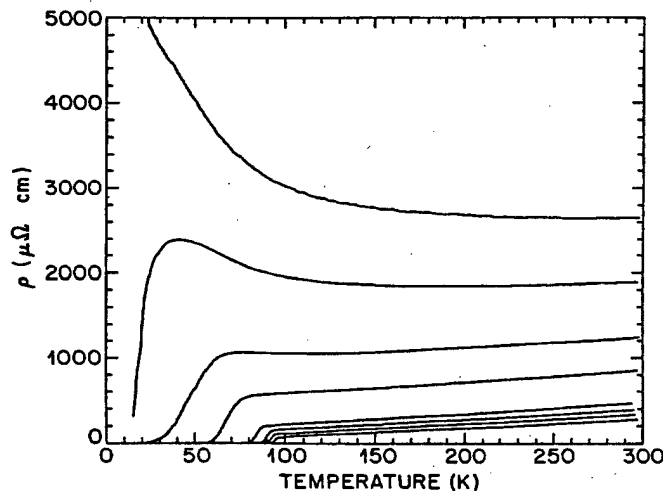


Figure 1. The superconductor insulator transition on a 1 MeV Ne⁺ ion irradiated YBCO film, fluences of 0.0, 0.1, 2.5, 4.0, 10.0, 15.0, 20.0, 22.0 x 10¹³ ions/cm².



Figure 2. Planar junction array depicting *a-b* transport.

Previously our junctions were fabricated from material grown in our laboratory by laser ablation. This resulted in relatively uniform junctions but it was felt that improvements could be made by employing better starting material. Films grown by laser ablation have rough surfaces and many large scale defects compared with films grown by co-evaporation techniques. A rough surface will lead to variation in the amount of material in the non-superconducting region resulting in non uniform critical currents and resistances. We have converted our process to fabricating junctions from high quality commercial electronics grade HTS material deposited on sapphire substrates by thermal co-evaporation.³ The films are capped with an *in-situ* gold contact layer which reduces contact resistance by over 4 orders of magnitude. The gold layer also serves as a protective cap that protects the underlying HTS material from chemical and thermal damage from developers and ion milling respectively. Our current fabrication process is depicted in figure 3.

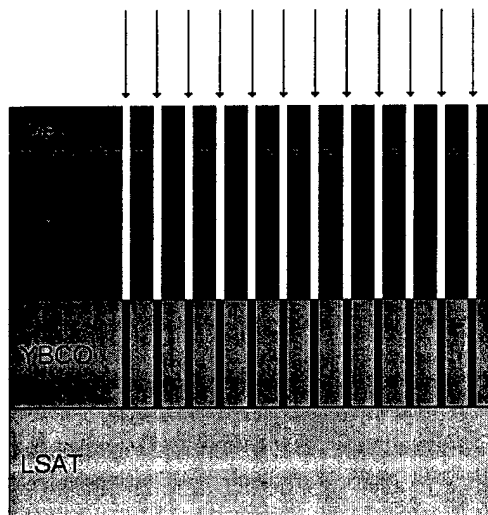


Figure 3. Diagram of germanium /photoresist bilayer hard mask .

Optical lithography is used to pattern 5 x 5 mm chips with 4 micron wide bridges along with the chip's electrodes. After removing the gold contact region over the active device region, the chip is coated with an 800nm layer of polymer photoresist, 50 nm layer of germanium and 5 nm of electron beam resist (PMMA). Electron beam lithography is used to write lines in the PMMA that will define the junction normal (*S'*) regions and this pattern is transferred into the Germanium layer with an anisotropic fluorocarbon reactive ion etch. The germanium layer serves as an etch mask of the underlying photoresist with subsequent RIE oxygen etch. The function of the 800nm of resist is to act

as a mask to shield the superconductor from ion damage in regions where we do not desire a reduction in T_c . The Ge is used as an intermediary layer to transfer the pattern from the PMMA because we do not know of an etch available that will etch photoresist and not PMMA. The sample is then irradiated in a commercial ion implanter⁴ where material not protected by the hard mask has its T_c lowered by disorder hence forming the S' region of the planar inline SS'S junctions. Previous chip layouts placed the device active regions (junction arrays) throughout the chip's area. This design resulted in non-uniformities in the electron beam writing due to the fact that the field of view of the microscope in the high resolution mode is $90 \times 90 \mu\text{m}$. To go beyond that field of view requires refocussing the beam. Therefore a 5 array chip required the instrument to be focused 5 times resulting in differences in line widths. Recently we have developed a 16 bridge chip where every bridge is contained within a $90 \times 90 \mu\text{m}$ area allowing us to create 16 different array devices all with a single focus and writing procedure (figure 4). This results in a considerable decrease in manufacturing time and over a 3X increase in device yield for a single chip. This is of utmost importance for a reliable technology. Using this technique we have demonstrated single junctions and arrays of up to 100 junctions with junction period less than 200nm (figure 5).

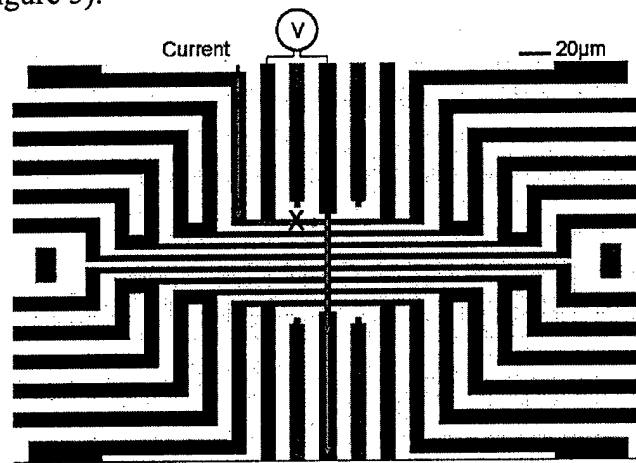


Figure 4. Active device region depicting a four point measurement on one of the sixteen 4 micron bridges. Blue is HTS material and green is alignment marks for electron beam lithography. The Josephson array is depicted with a black X, the path of the current is highlighted in red, and the voltage is measured on the remaining two electrodes.

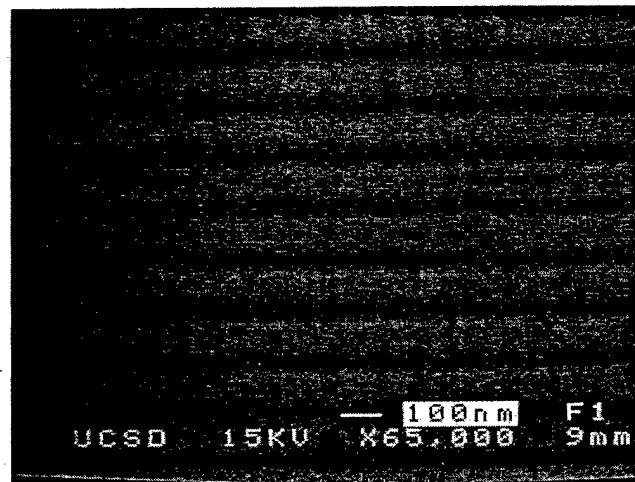


Figure 5. Etched hard mask depicting junction period less than 200nm for a 100 junction array.

II. Double Junction Studies

In addition to optimization of the device fabrication process we have also worked towards gaining a better understanding of the physics governing the functionality of our devices, in particular the nature of phase locking between adjacent junctions in an array. Our ultimate goal is to achieve collective phase locking of large arrays. Three mechanisms are usually proposed for phase locking between junctions. They are 1) order parameter locking that has a length scale of the superconducting coherence length, 2) quasi-particle locking with a length scale of microns and 3) electromagnetic field “push and pull” with a length scale that depends on the design. To explore this, a test structure of two junctions with an electrical contact in between them was fabricated. This posed a significant challenge because our goal was to have inter junction spacing of approximately 100nm. The main fabrication difficulty is that even with state-of-the-art electron beam lithography systems the precision of the alignment is limited to $\approx 20\text{nm}$. We have developed a technology to use our hard mask to define both the area of implantation along with the electrodes. This configuration allowed us to probe whether the junctions are phase locked by observing the IV characteristic under microwave radiation of the pair while current biasing one of the junctions. For example, if they are tightly locked, a step on the IV curve of one of the junctions is expected to be observed if the other junction is biased. The height of the step is a measure of lock stability. The locked region can be studied as a function of the bias of the pair of junctions by changing the bias of one of the junctions until phase unlock occurs. We expect that this locking should be related to the distance between the two junctions, the characteristic difference between the junctions and the working temperature. Our experiments have not yet detected any significant order parameter interactions. However, we have succeeded in fabricating junction pairs with almost identical parameters.

Figure 6. (a) and (b) show the top view of a three-layer stencil on top of a patterned YBCO film. Figures (c) and (d) are the results of I - V measurements carried on a Josephson junction pair at 63 K. Curves A, B and C are the I - V curves of the two single junctions and the junction pair. They are shifted horizontally for clarity. There was no applied microwaves in (c), while 12 GHz microwave radiation was applied to the junction in (d). The two junctions are remarkably similar. In fact, on the scales shown they are identical. Curve A can be shifted to overlap curve B quite accurately in both cases, which shows that the two junctions have nearly identical I - V properties. In fact, within the precision of our measurement system, we could find no difference in I_c or R_n of these two junctions. All the curves can be fit well by the RSJ model. In (d), on curve C Shapiro steps occur at $V = N \times nhf / 2e$, where $N = 2$ is the number of junctions, f is the microwave frequency, order number $n = 0, \pm 1, \pm 2$ and ± 3 . All the steps are flat and have the same widths with the corresponding steps on single junction I - V curves. We did not see any apparent mutual phase locking between the two junctions of the junction pairs we have fabricated to date. One of the possible reasons can be that the coherence length of $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ is much shorter than those of conventional superconductors (e.g. Sn). To have the order parameters of two junctions affect each other, we may have to put junctions even closer together than 150 nm, which is the closest junction center-to-center distance we have achieved to date. At this distance, current through the middle electrode will have impact on the two junctions either by induced magnetic field or current injection⁵. This introduces a difficulty of characterizing one

junction while current biasing the other junction independently as in conventional superconducting Josephson junction pairs⁶.

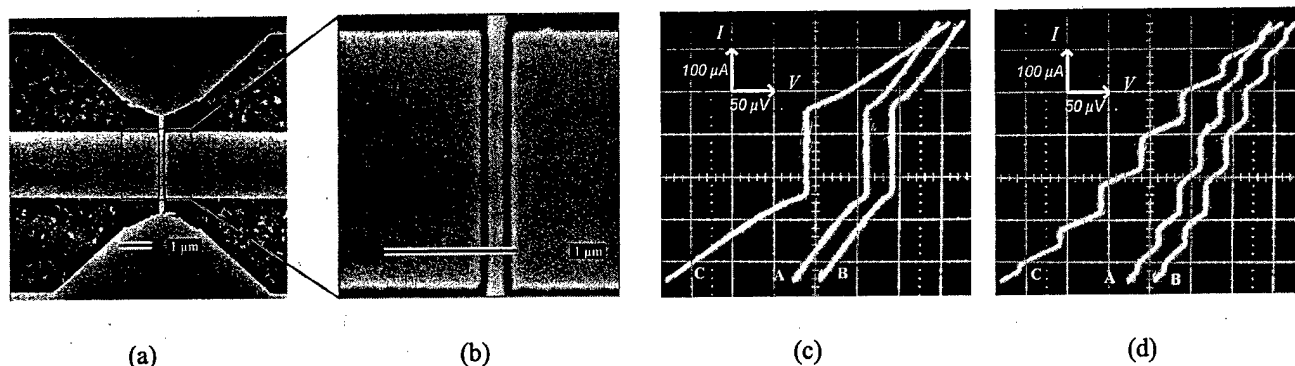


Figure 6 (a) Top view of three-layer stencil on top of a patterned YBCO film. It forms a 150nm spaced two Josephson junction array. The zoom-in picture (b) shows two 50nm wide trenches, beneath which two Josephson junction will be created by ion implanting. The center electrode between the two junctions gives us a chance to measure the properties of each individual junctions. Scope pictures of the current voltage characteristics of junction 1 (curve A), junction 2 (curve B) and the junction pair (curve C) at 63 K without (c) and with (d) 12 GHz microwave radiation.

III. 10-Junction Array

After achieving identical junction pairs, we have concentrated on fabrication of 10-junction arrays. Since the previous attempts to enhance phase-locking by placing junctions as close as possible have not met with success, we focussed on fabricating arrays which consisted of highly uniform Josephson junctions. The spaces between adjacent junctions are 2 μm typically. The ebeam lithography suffers much less proximity effect at such comparatively larger spaces, and this gives us better control to hopefully fabricate more uniform junctions.

Fig 7. shows $I-V$ curves of a 10-junction array with and without microwave radiation at 84 K. Giant Shapiro steps are observed at 10x the single Shapiro step voltage signifying that all the ten junctions are phase locked to the microwave field. However, from the roundness of the corner at I_c for the no microwave $I-V$ curve and the imperfect flatness of the first Shapiro step we conclude that the junction parameters of the array were not absolutely identical and there was a distribution of junction I_c 's and possibly resistances.

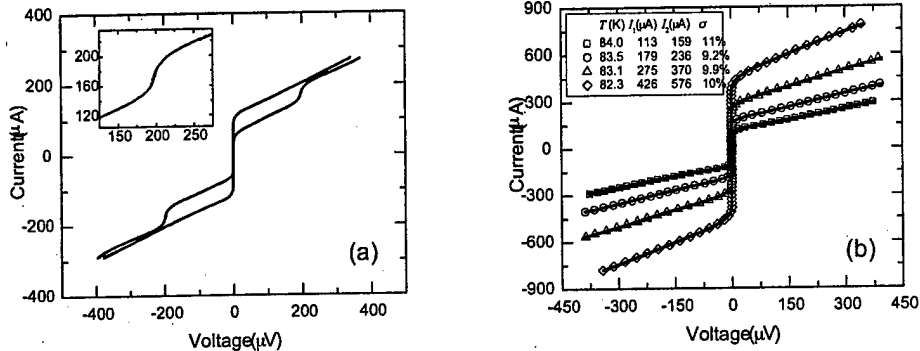


Figure 7 (a) The current-voltage characteristics of a 10-junction array with and without 10 GHz microwave radiation at 84 K. The first-order giant Shapiro step in detail is shown in the inset. (b) Fitting results for 82.3 K, 83.1 K, 83.5 K and 84 K.

Unlike the case of the junction pairs, it is not practical to characterize individual junctions by probing every center electrode between adjacent junctions for a large- N array. We propose a simple model to determine the spread of the critical currents of individual junctions within an array by fitting its I - V curves. We assume that each individual junction follows the RSJ model, has the same $I_c R_n$ product. For simplicity we assume that their I_c 's distribute evenly from the lowest I_c to the highest I_c (I_1 to I_2). We take the thermal noise contribution into consideration⁷ and include the current dependent resistance $R(I) = R_0 + \alpha I$ due to the moving S/N interface as bias current changes⁸. By fitting the single junction I - V curve A in Fig. 7 (c), we obtain noise temperature $T = 72$ K, which is only a little larger than the measurement temperature 63 K. We attribute the extra noise to our measurement system. A very good fit results for the 10-junction array at 82.3 K, 83.1 K, 83.5 K and 84 K and those fits are illustrated in Fig. 7 (b). The standard deviation σ at all temperatures is approximately 10%. We believe that the model reflects the junction I_c spread in the array.

IV. 50-100 Junction Arrays

Arrays of 50 and 100 junctions were fabricated and measured. Resistance as a function of temperature measurements for a 50 junction array damaged by 1×10^{13} ions/cm² Ne+ at 200 keV shows the T_c of the starting material to be 94K and the T_c of the disordered S' regions to be 64K (see Figure 8). Electrical transport data in figure 9 show an excellent improvement in critical current and resistance uniformity amongst different arrays on a chip. However rounded I - V characteristics at or near the critical current is an indication that non-uniformity still exists between junctions inside of the array.

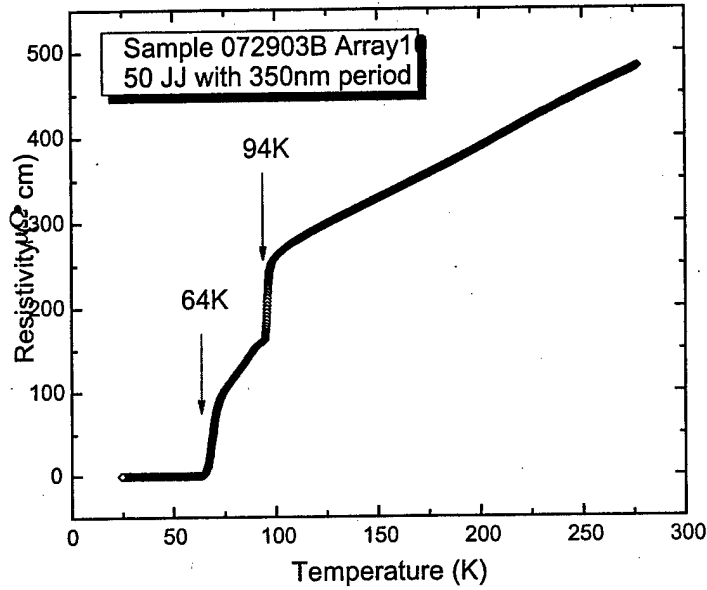


Figure 8. Resistance as a function of temperature for a 50 junction array showing the transition of bulk material (94K) and that of the array (64K).

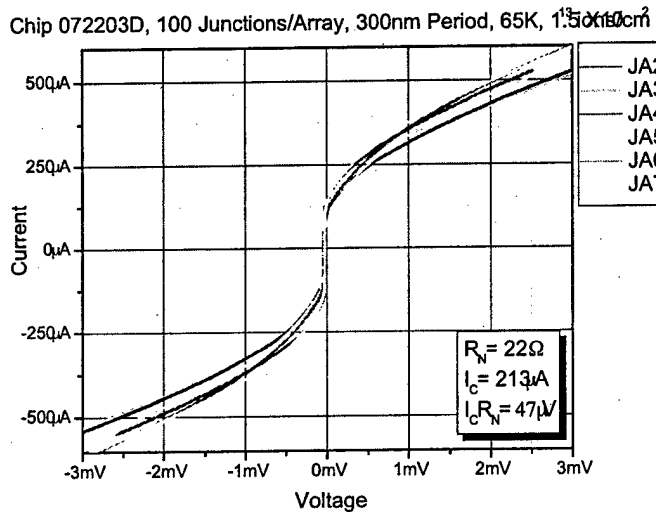


Figure 9. Current voltage characteristics demonstrating excellent chip uniformity for 6 one hundred junction arrays.

To further probe this non-uniformity, arrays were exposed to microwave radiation for study of the ac Josephson effect. Rather than exhibit vertical Shapiro steps at $V = N\hbar f / 2e$ in the I-V characteristic, as expected for a phase locked array of N junctions, our arrays exhibit a rounded step attributed to non-uniformity (figure 10).

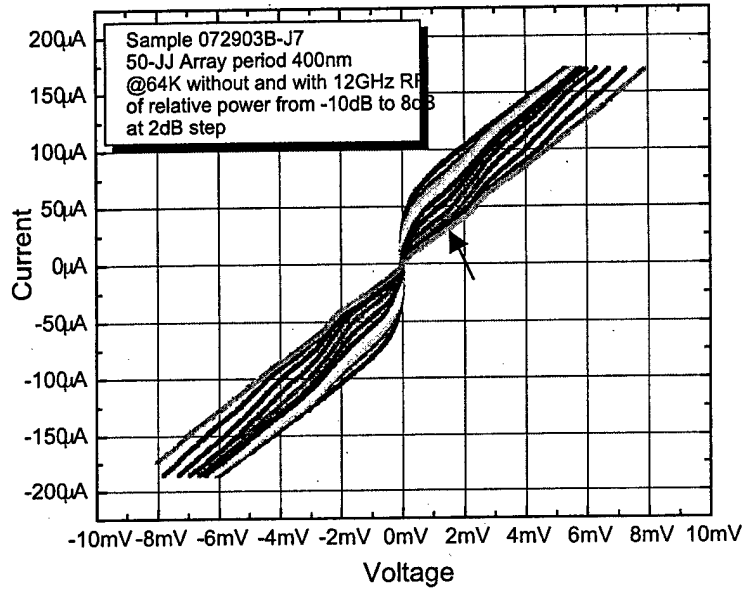


Figure 10. Current voltage characteristics with varying powers measured at 12GHz. A Shapiro step occurs at 2.4mV

This is more easily seen in figure 11 where the non-uniform steps appear as minima in the differential resistance (dV/dI). It is encouraging that we have observed the Shapiro steps at the expected voltage (50x that expected for a single junction). The steps are rounded and that must be improved.

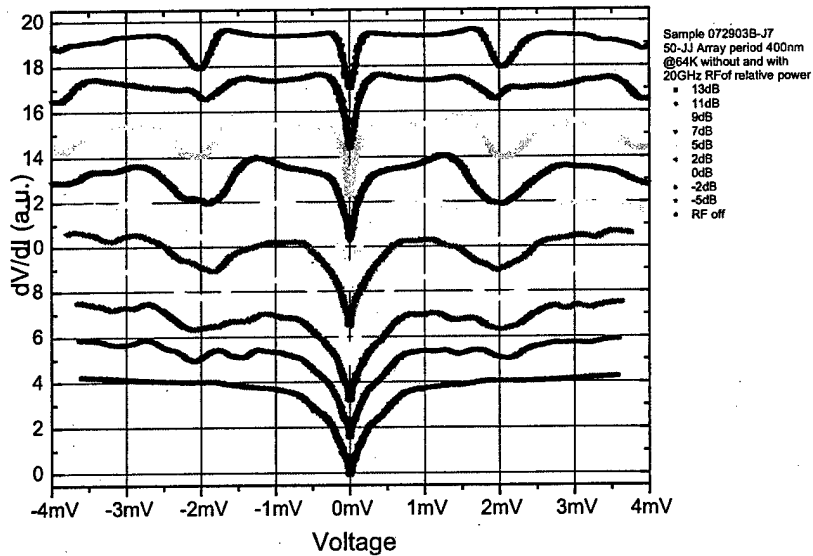


Figure 11. 20 GHz dV/dI measurements at different powers for a 100-junction array, showing the (broadened) Shapiro steps

VII. Metal masked junctions

The hard mask used to define the ion damage region of the bridge is another area of interest affecting junction uniformity because it must be constructed from materials that can be vertically etched, and of sufficient density to protect the underlying material from ion damage. Furthermore materials and etchants must be carefully selected and controlled to avoid adverse reactions with the HTS materials. Our reactive ion etch system is designed for etching with either an oxygen or fluorocarbon plasma. Oxygen readily etches polymer resists but does not significantly etch metals or HTS materials. The uniformity of these etches is essential for making uniform damage regions. We have observed that the thickness of the underlying photoresist is limited to thicknesses less than 800 nm because undercutting and sidewall collapsing occurs in thicker layers. This places a limit on the density of the mask that can be created using this material system and hence limits the ion implant energy that may be used. With this knowledge in hand we have explored different materials and etches for the hard mask. Niobium and Tungsten masked junctions have been fabricated and found to have inferior uniformity compared to our current process. We attribute this to three possible effects: Increased electron scattering during the electron beam lithography, non uniform etching due to the poly crystalline nature of the two metals and scattering of ions at mask edges during the ion damage process.

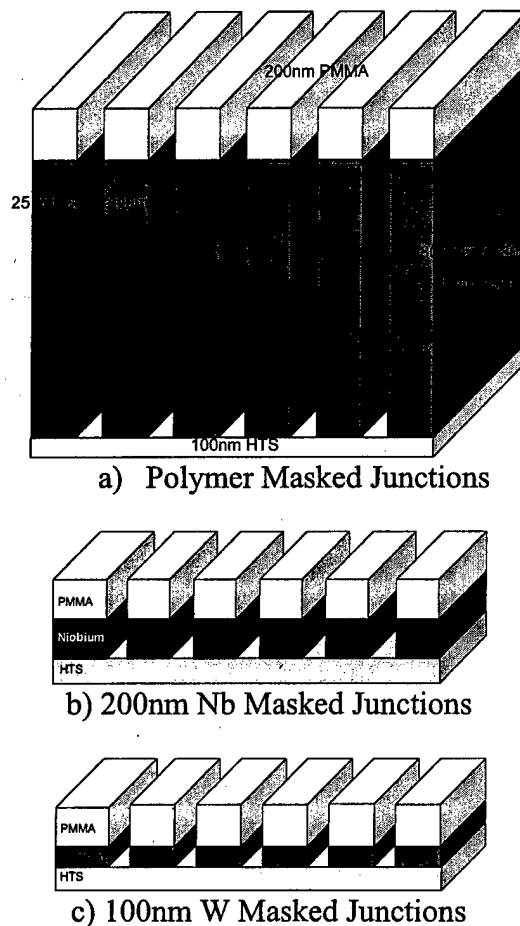


Figure 12. Comparison of Polymer masked and metal masked junctions.

V. Test Equipment

We have also redesigned and updated our custom low noise, low temperature measurement system housed in a RF shielded room. The heart of the system is a vacuum cryostat which accepts a 44 pin J-lead chip carrier where samples are attached via ultrasonic wire bonding. The chip carriers produced from Kyocera are a non-standard product made without any magnetic material in the "pocket" of the carrier. They are provided to us from Northrop Grumman and compatible with their measurement system. The cryostat is cooled in one of many dewars depending on the desired temperature and measurement. Most measurements are performed using a vacuum glass dewar filled with liquid nitrogen whose temperature can be controlled between 77-62K depending on the pressure in the dewar. Lower temperatures can be obtained by simply inserting the cryostat into a liquid helium storage dewar. For precise control of sample temperature the sample mount contains two thermometers and a heater connected to a temperature controller. Electrical signals from the cryostat are first amplified using low noise preamps and then output to a digital oscilloscope for observation and data acquisition. The cryostat has also been fitted with a coaxial cable to bring microwave radiation to the sample from a 0.6-20GHz microwave sweeper for AC Josephson measurements.

VI. Conclusion

During this grant period we have taken our established single junction process to the next step in realizing a very large scale Josephson integrated circuit technology. We have made many process level improvements to address nonuniformity issues. We have fabricated identical junction pairs to study the mutual interactions between junctions. We have also fabricated arrays of 10, 50, and 100 junctions and have demonstrated a giant Shapiro step in the 10 junction case. Lastly we have updated and improved our measurement system and capabilities.

VII. References

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- ⁴ Ion implanted by Core Systems Inc., 1050 Kifer Road, Sunnyvale, CA 94086.
- ⁵ W. E. Booij, A. J. Pauza, D. F. Moore, E. J. Tarte, M. G. Blamire, **Electrodynamics of Closely Coupled $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ Junctions**, IEEE Trans. Appl. Supercond. **7**, 3025 (1997).
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VIII. Papers during Grant Period

Planar thin film $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$ Josephson junction pairs and arrays via nanolithography and ion damage (submitted April 2004 APL).

Teizer, W.; Hellman, F.; Dynes, R.C. Spin Polarized Tunneling at the Metal-Insulator Transition Int. J. Mod. Phys. B, Vol. **17**, Nos. 18-20 (2003) 3723-3725

Teizer, W.; Hellman, F.; Dynes, R.C. Hall effect at a tunable metal-insulator transition Physical Review B, vol.67, (no.12), APS, 15 March 2003. p.121102-1-4.

Woods SI, Katz AS, Applebaum SI, de Andrade MC, Maple MB, Dynes RC. Nature of conduction in disordered Nd/sub 2-x/Ce/sub x/CuO/sub 4- delta / films. Physical Review B, vol.66,(no.1), 1 July 2002, pp.014538/1-4.

Price, E.P.; Smith, D.J.; Dynes, R.C.; Berkowitz, A.E. Do ballistic channels contribute to the magnetoresistance in magnetic tunnel junctions? Applied Physics Letters, vol.80, (no.2), AIP, 14 Jan. 2002. p.285-7.

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