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13. ABSTRACT (Maximum 200 words)

This report presents the final results of an investigation into direct radio frequency (RF) sampling receiver front ends and compares their performance to the traditional digital receiver front end designs. The distinction between the two implementations is that a direct RF sampling front end uses no analog frequency down conversion, rather the information bandwidth is aliased through the sampling process. This type of design significantly simplifies multiple frequency receiver design, important for receivers used in the Global Positioning System. However, the consequences of such an architecture are not fully understood as the technology required for their implementation has only recent become available. Past work has shown the feasible of the approach. This effort and report document the impact on the resulting phase noise, an important element in receiver design, as a result of the direct RF sampling.

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A Comparison of "Direct RF Sampling" and "Down-Convert & Sampling" Global Positioning System (GPS) Front End Receiver Architectures

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Introduction

A direct RF sampling radio receiver front end uses an analog-to-digital converter (ADC) to sample the RF signal without first mixing the signal down to a lower intermediate frequency. Figure 1 compares a traditional superheterodyne RF front end with a direct RF sampling front end. The main difference between the two receivers is that the traditional RF front end uses local oscillators and mixers to down-convert the signal to an intermediate frequency (IF), typically in the MHz range, before it samples the signal using an ADC. The direct RF sampling front end eliminates the mixing stages.

The ADC of the superheterodyne receiver typically samples at a frequency of about 4 times the final IF, which is typically in the MHz range. Surprisingly, the ADC in the direct RF sampling front also can sample at a rate in the MHz range even if the carrier wave is in the GHz range. The bandpass sampling theorem enables this type of approach, but only if the bandpass filter (BPF) upstream of the ADC has been designed to filter out unwanted signals and noise that are not near the nominal carrier frequency. The resulting ADC output has an IF of

$$f_{IF} = f_c - f_s round(f_c/f_s) \tag{1}$$

where f_c is the original carrier frequency, f_s is the sampling frequency, and the *round*() function rounds to the nearest integer. Note that eq. (1) guarantees that f_{IF} falls within the Nyquist bandwidth: $-f_s/2 \le f_{IF} \le f_s/2$. A negative f_{IF} occurs when *round*() rounds upwards, and it is the direct RF sampling equivalent of high-side mixing. If B is the information bandwidth of the signal, then a good design procedure chooses f_s so that $B/2 \le |f_{IF}| \le (f_s/2 - B/2)$ [1]. These constraints imply that $f_s \ge 2B$, which is the requirement of the bandpass sampling theorem.

Direct RF sampling offers several advantages for GNSS RF front end design. First, it reduces the parts count, as is obvious from Fig. 1, and it eliminates the need to design and fabricate a mixing chip with a specially tailored frequency plan. Second, it simplifies the design of new receivers for the new signals that will become available as GPS gets modernized and as Galileo comes on line. All that is needed to work with a new carrier frequency is to select an appropriate sampling frequency and to incorporate an appropriate BPF. Third, it is possible to make a single RF front-end for multiple frequency bands. This approach to multi-frequency GNSS receiver front end design eliminates the need for multiple front ends, which reduces the parts count and eliminates some potential sources of inter-channel line bias.

Interest in direct RF sampling front-ends has been spurred by recent advances in ADC technology. The most important advance is the introduction of commercial ADCs that can operate continuously on input signals with bandwidths in excess of 2 GHz. This technology allows practical direct RF sampling receivers to be designed for a host of applications that include GNSS.

The one significant drawback of the direct RF sampling front end is the possible need for a high Q in its BPF. The bandwidth of the filter that is upstream of the ADC must equal B, the information bandwidth, if one wants to keep the sampling rate to a minimum without degrading the carrier-to-noise ratio, C/N_0. The required BPF Q for a GPS L1 C/A code receiver would be 1575.42MHz/2MHz $\cong$ 800, which is very high. It is very difficult to obtain a Q larger than 500 in this frequency range. Thus, a direct RF sampling design might have to settle for a non-minimal sampling frequency, a slightly degraded C/N_0, or both in order to use a practical filter. For P(Y) code the situation is better. A BPF Q on the order 80 is acceptable.

Brown and Wolt and Akos and Tsui were the first to report on the use of direct RF sampling for the design of GPS receiver front ends. Brown and Wolt concentrated on a system that uses a very fast sampling rate, 800 MHz. This system captures the entire spectrum from L2 at 1227.6 MHz up to L1 at 1575.42 MHz in a single information bandwidth centered at 1400 MHz. Their design uses 1-bit digitization and post-processes the signal using digital filters in order to select either L1 or L2. They analyze the effects of ADC sample clock jitter. Their paper presents no experimental results for actual GPS signals.

Akos and Tsui explored issues of gain, sensitivity, and dynamic range. They settled on a design that placed the BPF between the last stage of amplification and the ADC in order to minimize the folding of out-of-band noise from the amplifiers into the Nyquist spectrum and in order to minimize sensitivity losses due to filter insertion loss. Their design accepts a lowered third-order intermodulation point in order to use this filter placement. They tested their designs by performing acquisitions and FFT analysis for short batches of actual GPS RF front-end data that were acquired using a high-speed digital oscilloscope. The oscilloscope limited them to a sub-optimal sampling frequency that did not obey all of the design criteria given above.

Other efforts in direct RF sampling include the work of Ledvina et al., Akos et al., Psiaki et al., and Lindfors et al. Although the main point of Ledvina et al. is the development of a real-time software GPS receiver, the work also involved the demonstration of a continuously operating real-time GPS receiver whose front end used direct RF sampling. To the authors' knowledge, this is a first in the GNSS literature. Akos et al. developed a method for designing direct RF sampling front-ends for multiple frequency bands, and they tested their method by acquiring GPS L1 C/A signals and GLONASS signals using a signal prototype direct RF-sampling front end. Their method of designing for multiple frequency bands allows the use of a much lower sampling frequency than does the method of Brown and Wolt because they do not attempt to digitize the entire information bandwidth between the multiple frequency bands of interest. Psiaki et al. use a technique similar to that of Akos et al. to design a single RF front end for receiving GPS C/A and P(Y) code on both the L1 and L2 frequencies. Lindfors et al. discuss the importance of the proper design of the anti-aliasing filter, they discuss the effects of sample aperture width and jitter, and they develop a CMOS sampling system and test it using pure

carrier wave signals.

The present work makes several contributions to the area of direct RF sampling front-ends for GNSS receivers. First, it presents an improved analysis of the effects of sample clock jitter. Second, it gives detailed signal tracking results for actual GPS L1 C/A signals that have been received using direct RF sampling front ends. Third, it compares direct RF-sampled signals with signals from a superheterodyne front end in terms of carrier-to-noise ratio and carrier phase jitter as deduced from experimentally tracked signals and as deduced from analysis. Fourth, it shows that the ADC jitter's impact on carrier phase is a common-mode receiver clock error effect which can be removed by the standard navigation solution techniques. Last, it develops guidelines for designing direct RF sampling front ends so that ADC sampling jitter does not seriously degrade performance. Although this paper's title gives "equal time" to the standard approach of superheterodyne frequency down conversion, the bulk of the paper concentrates on the new technology of direct RF sampling.

These issues are addressed in the remaining five main sections of this paper. Section II develops signal models that include the effects of ADC sampling jitter, analyzes the impact of jitter, and develops guidelines for limiting its adverse affects. Section III describes the experimental set-ups that have been used to collect GPS output data from direct RF sampling front ends and from a superheterodyne front end. Section IV describes the off-line acquisition and tracking algorithms that have been used to process the experimental data. Section V presents the experimental results that have been obtained using these set-ups and algorithms, and it discusses these results in light of the analyses of Section II. Section VI discusses an off-line simulation study that has been conducted in order to further verify the analysis conclusions. Section VII summarizes the paper's results and conclusions.

II. Modeling and Analysis of Direct RF Sampling and Superheterodyne Mixing Front Ends

A. Signal Models

The signal that comes out of the front end of a direct RF sampling GNSS receiver can be modeled as

$$y_j = A\, C[t_j+\Delta t_j-t_{c0}]\, cos[2\pi f_c(t_j+\Delta t_j) + \phi(t_j+\Delta t_j)] + n_j \qquad (2)$$

where A is the signal amplitude at the output of the front end, $C[]$ is the ± 1 pseudo-random number (PRN) code of the CDMA spread-spectrum signal, $t_j = j/f_s$ is the time of the j^{th} sample as measured by the receiver oscillator, Δt_j is the receiver clock error on the j^{th} sample, t_{c0} is the start time of the PRN code, $\phi(t_j+\Delta t_j)$ is the integrated Doppler shift carrier phase (also known as the accumulated delta range in the GPS literature), and n_j is the receiver noise plus the interference from other signals.

The output of a direct RF sampling front-end can be modeled by eq. (2), but one usually uses the following alternate formula to model this output:

$$y_j = A\, C[t_j+\Delta t_j-t_{c0}]\, cos\{2\pi f_{IF} t_j + [2\pi f_c \Delta t_j + \phi(t_j+\Delta t_j)]\} + n_j \qquad (3)$$

The substitution of f_{IF} for f_c in the first term of the cosine argument has been made so that the modeled intermediate carrier frequency falls within the Nyquist range $[-f_s/2, f_s/2]$. This substitution is possible because of the relationship between f_{IF} and f_c given in eq. (1) and because of the formula for t_j given after eq. (2). Note that the receiver clock error in eqs. (2) and (3), Δt_j, includes both the effects of oscillator drift and the effects of ADC sampling jitter.

A superheterodyne GNSS receiver front end's output can be modeled as

$$y_j = A\, C[t_j+\Delta t_j-t_{c0}]\, cos\{2\pi f_{IF} t_j + [2\pi f_c \Delta t_j + \phi(t_j+\Delta t_j) + \Delta\phi_j]\} + n_j \qquad (4)$$

This formula is similar to that of the direct RF sampling front end except for two features. First, eq. (1) does not characterize the relationship of the intermediate carrier frequency f_{IF} to the original carrier frequency f_c. Instead, this relationship is a function of the frequency mixing plan chosen for the design. Second, there is an extra carrier phase perturbation $\Delta\phi_j$. This perturbation represents the possibility of relative phase jitter in the synthesizer chain that links the local oscillators in the mixer with the ADC sample clock. This additional phase perturbation introduces a differential code/carrier Doppler shift jitter. This additional jitter is not present in direct RF sampling receivers, which gives them an advantage in this respect.

In Ref. **Error! Bookmark not defined.** Akos and Tsui concentrated on the signal power effects of direct RF sampling, on the noise power spectral density of n_j, and on nonlinear distortion and intermodulation interference. The goal was to achieve a usable carrier-to-noise ratio without introducing too much distortion or interference. The key idea was to use the proper BPF in the proper location to limit the post-sampling power spectral density of n_j. The main focus of the present work is to explore the effects on power level and carrier phase tracking of ADC sample timing jitter in Δt_j.

Two important concepts in direct RF sampling are aperture width and aperture jitter. These are depicted in Fig. 2. The aperture width is the time duration of the dotted window that constitutes the effective time duration over which the carrier signal gets averaged to produce a given ADC output. The width of this window is inversely proportional to the maximum input bandwidth that the ADC can accommodate. If a higher frequency carrier is input, then the ADC's averaging process will significantly degrade the strength of the sampled signal. The remainder of this paper assumes that the system's ADC has been design to have a sufficiently small aperture width.

The aperture jitter is the amount by which the sample aperture spacing varies from its nominal value of $T_s = 1/f_s$. Aperture jitter causes the ADC to sample at a different phase of the carrier wave than assumed by the aliasing calculations of eq. (1). Jitter can lead to signal power loss and to carrier phase and code phase measurement errors.

B. Analysis of ADC Aperture Jitter Effects

The effects of ADC aperture jitter will be analyzed using two assumptions. The first assumption is that the aperture jitter is a discrete-time random noise process that arises from several possible sources: oscillator frequency drift, synthesizer phase noise, and ADC trigger delay jitter. The net

result of these random processes is the discrete-time ADC sampling time error sequence Δt_0, Δt_1, Δt_2, ..., Δt_j, ... The statistics of this discrete-time sequence are completely specified by its power spectral density $P_{\Delta t}(f)$, which is defined over the Nyquist frequency range $-f_s/2 \le f \le f_s/2$.

The second analysis assumption is that the signal gets processed downstream of the front end by in-phase and quadrature baseband mixing, correlation with a PRN code replica, and accumulation of correlations. The resulting accumulations are

$$I = \sum_{j=1}^{N} y_j C[t_j - \hat{t}_{c0}] cos[2\pi f_{IF} t_j + \hat{\phi}(t_j)] \tag{5a}$$

$$Q = -\sum_{j=1}^{N} y_j C[t_j - \hat{t}_{c0}] sin[2\pi f_{IF} t_j + \hat{\phi}(t_j)] \tag{5b}$$

where I is the in-phase accumulation, Q is the quadrature accumulation, N is the number of samples in each accumulation, $\hat{t}_{c0}$ is the receiver's estimate of the code phase start time, and $\hat{\phi}(t_j)$ is the receiver's estimate of the carrier phase at time t_j. Suppose that the estimated code phase offset $t_j - \hat{t}_{c0}$ is very close to the true code phase offset $t_j + \Delta t_j - t_{c0}$ and that the estimated carrier phase $\hat{\phi}(t_j)$ is very close to the true carrier phase $\phi(t_j + \Delta t_j) - \pi/2 + \Delta\phi_{\Delta t}$, where $\Delta\phi_{\Delta t} = 2\pi f_c \Delta t_{avg}$ with $\Delta t_{avg} = (\Delta t_1 + \Delta t_2 + ... + \Delta t_N)/N$ is the average carrier phase error due to clock jitter. These assumptions are reasonable for a properly working receiver with a strong enough signal. The accumulations can then be modeled as:

$$I = -\frac{A}{2}\sum_{j=1}^{N} sin(2\pi f_c \delta t_j) + n_I \cong -A\pi f_c \sum_{j=1}^{N} \delta t_j + n_I \tag{6a}$$

$$Q = \frac{A}{2}\sum_{j=1}^{N} cos(2\pi f_c \delta t_j) + n_Q \cong \frac{NA}{2}\{1 - [\frac{(2\pi f_c)^2}{2}]\frac{1}{N}\sum_{j=1}^{N} \delta t_j^2\} + n_Q \tag{6b}$$

where $\delta t_j = \Delta t_j - \Delta t_{avg}$ and where n_I and n_Q represent the effects of the thermal noise n_j on the accumulations. The approximations on the far right-hand sides of these equations assume that $2\pi f_c \delta t_j << 1$.

The principal effect of ADC sampling jitter on signal power can be analyzed by considering eq. (6b). The average signal power in eqs. (6a) and (6b) all resides in the Q accumulation (because of the $-\pi/2$ term in $\hat{\phi}$). The extreme right-hand side of eq. (6b) shows that there is a power loss which is proportional to the average of δt_j^2 over the sample interval. Thus, a power loss occurs if the ADC sampling jitter is not constant over an accumulation interval. The loss occurs because the random phase errors get accumulated coherently, which causes the signal power at different samples to add in a partially destructive manner.

Equation (6b) can be used to calculate the signal power loss factor based on the power spectral density of Δt_j:

$$Loss\ Factor = \left\{1-\left[\frac{(2\pi f_c)^2}{2}\right]\left[\int_{-f_s/2}^{f_s/2}\left(1-\left\{\frac{\sin[N\pi f/f_s]}{N\pi f/f_s}\right\}^2\right)P_{\Delta t}(f)df\right]\right\}^2 \quad (7)$$

Equation (7) implies that the power loss is due principally to the spectral content of the jitter above the frequency $f_s/(2N)$ because the (1 - sync) function that weights $P_{\Delta t}(f)$ in the integral of eq. (7) is close to 1 above that frequency and close to 0 below that frequency. This frequency cut-off equals half the accumulation frequency of the receiver.

Equation (7) differs from the loss equations of Refs. **Error! Bookmark not defined.** and **Error! Bookmark not defined.**. Both references analyze the jitter as causing an increase in noise rather than a decrease in accumulation power. They also both ignore the effect of the spectral distribution of the Δt_j noise power and express the loss solely as a function of the total jitter noise power, $\sigma^2_{\Delta t}$. The loss formula in eq. (5) of Ref. **Error! Bookmark not defined.** agrees with this paper's eq. (7) in the limit of small $\sigma^2_{\Delta t}$, a flat jitter power spectrum, and large N.

The carrier phase measurement error due to ADC sample timing jitter is $\Delta\phi_{\Delta t} = 2\pi f_c \Delta t_{avg}$. The mean square value of this error can be determined from the power spectrum of Δt_j:

$$\sigma^2_{\Delta\phi} = (2\pi f_c)^2\left\{\int_{-f_s/2}^{f_s/2}\left[\frac{\sin(N\pi f/f_s)}{N\pi f/f_s}\right]^2 P_{\Delta t}(f)df\right\} \quad (8)$$

This equation dictates that the carrier phase error arises mostly from the spectral content of the jitter below the frequency $f_s/(2N)$ because the sync function that weights $P_{\Delta t}(f)$ in the integral of eq. (8) is close to 1 below that frequency and close to 0 above it.

In summary, the high-frequency components of the jitter act mostly to degrade the signal power, and the low-frequency components act to degrade the carrier phase accuracy. The low-frequency/high-frequency boundary occurs at half the accumulation frequency, $f_s/(2N)$. If the high-frequency jitter power is too large, then the signal power will be seriously degraded, and it may not be possible to acquire or track the signal. If the low-frequency jitter power is too large, then it will be hard to measure carrier phase accurately, and it may become difficult to track the carrier signal using a phase-locked loop (PLL) or a frequency-locked loop (FLL).

The carrier phase error shows up as a common-mode error on all receiver channels. It amounts to receiver clock error. All receivers have clock error, and all standard navigation algorithms compensate for this effect. Therefore, if the ADC sample timing jitter is small enough to allow carrier tracking, then any residual jitter will have a minimal impact on receiver performance because the navigation solution procedure will compensate for it. A similar statement applies to the effects of ADC jitter on a receiver's code phase measurements.

C. Guidelines for Allowable Jitter Levels In Direct RF Sampling Front Ends

The guidelines for acceptable ADC sample timing jitter in a direct RF sampling receiver front-end place upper bounds on the low-frequency and high-frequency power of the jitter. Given an upper bound on the power loss of $+L$ dB and given the accumulation interval $T_a = N/f_s$, the jitter power spectrum must obey the bound:

$$\int_{1/(2T_a)}^{f_s/2} P_{\Delta t}(f)df \cong \int_{0}^{f_s/2} \left(1-\left\{\frac{sin[\pi f T_a]}{\pi f T_a}\right\}^2\right) P_{\Delta t}(f)df \leq \frac{1}{(2\pi f_c)^2}[1-10^{(-L/20)}] \tag{9}$$

The far left-hand side of eq. (9) is an approximate formula for the bound on the integrated power spectral density. Equation (9) is a direct consequence of eq. (7). Similarly, given an upper bound on the accumulations' carrier phase error variance, $(\sigma^2_{\Delta\phi})_{max}$, the jitter power spectrum must also obey the bound:

$$\int_{0}^{1/(2T_a)} P_{\Delta t}(f)df \cong \int_{0}^{f_s/2} \left(\frac{sin[\pi f T_a]}{\pi f T_a}\right)^2 P_{\Delta t}(f)df \leq \frac{1}{2(2\pi f_c)^2}(\sigma^2_{\Delta\phi})_{max} \tag{10}$$

which is a direct consequence of eq. (8).

D. Comparison with a Superheterodyne Front End

The need to meet these bounds does not represent a drawback of the direct RF sampling front end design approach. A superheterodyne mixing receiver front end design must obey similar guidelines. Jitter in its mixing local oscillators causes $\Delta\phi_j$ jitter as defined in eq. (4). This jitter, if too large, will have similar negative impacts on carrier phase measurement error and on accumulation power. What is more, there is the possibility of additional Δt_j phase jitter showing up in the ADC sample clock.

Therefore, the only possible detrimental effect of a direct RF sampling front end occurs if the power of the timing jitter gets increased by the use of high-frequency ADC sampling. Such jitter must exist in the ADC itself for it to be a new jitter source. As it turns out, there exists ADC technology that adds negligible jitter when working with carrier signals in the L band and below.

III. Experimental Set-Up

This section documents the experimental set-ups that have been used to evaluate direct RF sampling. The generic experimental set up is depicted in Fig. 3. It consists of a roof-mounted antenna connected through a low-noise amplifier (LNA) and cable system to the front end under test. The front end's digital ADC output gets sent to a Personal Computer (PC) through a generic data acquisition system (DAQ) where it gets stored on disk for off-line processing. Afterwards, the data gets processed using signal acquisition and tracking software that runs in MATLAB on the PC.

Several different GPS receiver front ends have been used to experimentally evaluate the concept of direct RF sampling and to compare it with a front end based on down conversion through superheterodyne mixing. These include a number of direct RF front ends and one superheterodyne front end. The important aspects of each experimental set-up are its cumulative gain and noise figure, the bandwidth of the front end's BPA, the ADC used, the sampling frequency, and the nominal intermediate frequency. This frequency can be computed from eq. (1) for all of the direct RF sampling front ends, but it must be specified for the superheterodyne front end. Distortion parameters such as the third-order intermodulation intercept point and the 1 dB compression point are essentially irrelevant for the present discussion because of the low levels of the GPS signals that have been used.

Table 1 summarizes many of the important characteristics of the front ends and systems that have been tested. The gains and noise figures quoted in the table include the effects of the LNA, the BPF, and any cable that is upstream of the ADC.

Each system used a Dallas Semiconductor MAXIM MAX104 ADC **Error! Bookmark not defined.**. It has an input bandwidth of 2.2 GHz, a maximum sampling rate of 1 GHz, 8 bits of output, a full input range of -2 dBm at 50 Ω, and an aperture jitter of less than 0.5 psec. This aperture jitter spec implies that the ADC's contribution to carrier phase jitter will be no more than $1575.42\times10^{6}\times0.5\times10^{-12}$ cycles = 0.28 deg and that the signal power loss due to the ADC's jitter contribution will be no more than 0.0001 dB.

The front ends in set-ups A, B, and C use direct RF sampling, and the front end in set-up D uses superheterodyne mixing down conversion. Systems A and B have been implemented at Cornell. Their difference lies in the filter that has been used. The filter in system A is a ceramic filter that passes only L1 with a 100 MHz bandwidth. The filter in system B is an active system that passes 20 MHz bands around both L1 and L2. It consists of two passive dual-frequency cavity filters, one on either side of an LNA. This latter system is described in detail in Ref. **Error! Bookmark not defined.**. The use of two filters separated by an amplified makes system B different from direct RF sampling systems A & C, both of which use only one BPF just before the ADC. Systems C and D have been implemented at Stanford. They have been designed to be as similar as possible, except that system C uses direct RF sampling and system D uses superheterodyne mixing for pre-sampling down conversion.

Systems A and B retain only 2 bits of the MAX104's 8-bit output. This approach has been used in order to allow the systems to economize on data storage with minimal quantization losses. Systems A and B store the ADC sign bit and a magnitude bit which is synthesized from the two most significant magnitude bits that vary due to the input signal. Simple Boolean logic is used in this synthesis. The magnitude is low when the signal is no more distant from zero than the bit level of the least significant of the 2 magnitude bits. An attenuator is placed upstream of the last LNA, the filter, and the ADC. It is tuned by hand to give a low magnitude bit reading 70% of the time, which yields nearly optimal gain control for the 2-bit conversion. A similar manual gain control approach is used with system C, and only the 4 most significant bits of the 8-bit MAX104 output are saved.

A number of different sampling frequencies have been considered. Direct RF sampling systems

A and B have been used with the following sampling-frequency/intermediate-L1-frequency pairs: f_s = 5.71429 MHz/f_{IF} = -1.72404 MHz, f_s = 55.5053 MHz/f_{IF} = 21.2716 MHz, f_s = 77.33 MHz/f_{IF} = 28.82 MHz, and f_s = 99.23 MHz/f_{IF} = -12.26 MHz. The first sampling frequency, 5.71429 MHz, has been used to consider only C/A code operation, and the latter 3 sampling frequencies, 55.5053 MHz, 77.33 MHz, and 99.23 MHz, have been designed for use in the dual-frequency front end of Ref. **Error! Bookmark not defined.**, which aliases the L1 and L2 bands to minimally overlapping portions of the Nyquist spectrum. System C has been run at two of the same direct RF sampling frequencies as systems A and B, f_s = 77.33 MHz and f_s = 99.23 MHz. It has also been run at the slower direct RF sampling frequency f_s = 16.3676 MHz, which yields an intermediate L1 frequency of f_{IF} = 4.1304 MHz. Mixed down-conversion system D uses this latter sampling frequency, and its mixing plan has been designed to yield the same intermediate L1 frequency that system C (or any direct RF sampling system) yields at this f_s value, f_{IF} = 4.1304 MHz.

Another important aspect of the experimental systems is the stability of their ADC clocks. ADC jitter can originate in the ADC itself or in the oscillator/synthesizer system that provides the ADC sample clock. All 5 systems have used ovenized crystal oscillators with excellent frequency stability characteristics. Sampling and mixing frequencies have been generated based on an ovenized crystal oscillator and a frequency synthesizer that uses frequency dividers and PLL's to develop clock signals at other frequencies. Two different frequency synthesizers have been used with systems A and B. One is a Fluke 6060B. Its FM noise specification implies that its clock jitter standard deviation obeys the bound $\sigma_{\Delta t} \leq$ (0.0018 cycles)/f_s. The other synthesizer is an HP 3325A. Its RMS clock jitter obeys the bound $\sigma_{\Delta t} \leq$ (0.00016 cycles)/f_s. Systems C and D used an Agilent 8648B oscillator/frequency synthesizer. Its nominal phase noise PSD translates into the RMS clock jitter bound $\sigma_{\Delta t} \leq$ (0.00029 cycles)/f_s. These numbers indicate that the Fluke synthesizer has the poorest clock jitter performance and that the HP and Agilent synthesizers have similar performance.

IV. Software Receiver-Based Signal Acquisition, Tracking, and Analysis

Experimental data have been evaluated by using an off-line software receiver. It acquires and tracks GPS signals that are present in the output data of the experimental RF front ends. The outputs of this software receiver can be used to determine signal power and carrier phase jitter, which can be used to evaluate the performance of each receiver front end. This section gives an overview of how the software receiver acquires and tracks the signals and of how the tracking results have been used to evaluate the carrier-to-noise ratio and phase jitter of each signal.

The software receiver's acquisition and tracking algorithms are described in detail in Refs. [2] and [3]. The acquisition algorithm uses 10 periods of the C/A PRN code and performs two different coherent integrations separated by 0.010 sec in order to ensure that one of the integration intervals does not occur during a navigation data bit transition. FFT-based techniques are used to rapidly calculate correlations at multiple code offsets for a given guess of the carrier Doppler shift. The acquisition algorithm yields initial estimates of the PRN code start time and the carrier Doppler shift, which are used to initialize the tracking algorithm.

Precise code and carrier phase tracking is accomplished in two steps. The first step implements a

Kalman filter-based PLL to track carrier phase based on *atan2(Q,I)* carrier phase measurements from 1000 Hz I and Q accumulations. A Kalman filter-based DLL with carrier aiding tracks the code phase using the function $(\sqrt{I_{early}^2+Q_{early}^2}-\sqrt{I_{late}^2+Q_{late}^2})/(\sqrt{I_{early}^2+Q_{early}^2}+\sqrt{I_{late}^2+Q_{late}^2})$ as a code phase measurement. The second step of the tracking algorithm performs a backwards smoothing pass to refine the carrier and code phase estimates. The smoother is non-causal, which means that its phase estimates at a given time of interest depend on accumulations that fall both before and after that time. Although smoothing is not useful for real-time operation, this non-causal approach is perfect for off-line studies because it improves the accuracy of the phase estimates. As with the Kalman filters, the carrier phase smoother's outputs are used to aid the code phase smoother.

The carrier-to-noise ratio C/N_0 and the carrier phase jitter can be calculated using the smoothed code and carrier phase estimates. These phase estimates can be used to calculate smoothed 1000 Hz in-phase and quadrature prompt accumulations for a given batch of data from a receiver front end. These are I_0, Q_0, I_1, Q_1, I_2, Q_2, ..., I_N, Q_N for a data batch of duration 0.001N seconds. Let $\overline{Z}$ and σ_z^2 be the mean and variance of the time series $Z_k = (I_k^2+Q_k^2)$. The quantities $\overline{Z}$ and σ_z^2 are not affected by the carrier phase jitter that results from ADC sample timing jitter. Referring to eqs. (6a) and (6b), one can use these statistics to estimate the accumulation power $(NA/2)^2$ and the variance of the accumulation noise terms n_I and n_Q, σ_{IQ}^2:

$$\left(\frac{NA}{2}\right)^2 = \sqrt{\overline{Z}^2-\sigma_z^2} \tag{11a}$$

$$\sigma_{IQ}^2 = \tfrac{1}{2}(\overline{Z}-\sqrt{\overline{Z}^2-\sigma_z^2}) \tag{11b}$$

These quantities, in turn, can be used to estimate the carrier-to-noise ratio:

$$\frac{C}{N_0} = 10log_{10}\left[\frac{1000(NA/2)^2}{2\sigma_{IQ}^2}\right] \text{ dB Hz} \tag{12}$$

Carrier phase jitter can be examined by comparing the variance of the I_k accumulations to that of the Q_k accumulations. As in eqs. (6a) and (6b), the smoother-based PLL tracks the carrier phase so that the signal power nominally appears on the Q_k accumulations. For small phase jitter, the variance of the Q_k accumulations will equal σ_{IQ}^2, but the variance of the I_k accumulations will take on the increased value $\sigma_{IQ}^2 + (NA/2)^2\sigma_{\Delta\phi}^2$, where the additional term is the carrier phase jitter term. This jitter term can be estimated by computing variance(I_k) - variance(Q_k).

This analysis of carrier phase jitter is based on two assumptions about the smoother's estimated

carrier phase time history $\hat{\phi}(t)$. First, it assumes that all of the actual signal's carrier phase dynamics are exactly captured by $\hat{\phi}(t)$. Second, it assumes that none of the sample timing jitter effects are folded into $\hat{\phi}(t)$. Although not perfectly satisfied, these assumptions are reasonable because the smoother-based PLL's I_k accumulation time history is effectively a high-pass filtered version of the carrier phase dynamics. If most of the true signal's carrier phase dynamics occur below the break frequency of the PLL and if most of the jitter occurs at frequencies above the break frequency, then $\hat{\phi}(t)$ is primarily the phase of the true signal, and the phase error $atan(I_k/Q_k)$ is primarily clock jitter plus receiver thermal noise. The smoother bandwidth has been tuned to be very low. The smoother is also 3rd-order, which means that a constant phase acceleration (a constant rate of change of Doppler shift) will produce zero phase error for an arbitrary bandwidth. The GPS satellite motions with respect to a roof-mounted antenna are very well approximated by a constant phase acceleration. Therefore, very little actual signal phase is present in atan(I_k/Q_k) due to the benign signal dynamics, and very little sample timing jitter is present in $\hat{\phi}(t)$ due to the low smoother bandwidth.

V. Experimental Results

A. Comparison Between Direct RF Sampling and Superheterodyne Mixing Front Ends

Signals have been acquired and tracked using the superheterodyne mixing front end, system D of Table 1, and the equivalent direct RF sampling front end, system C operating at the identical sampling frequency f_s = 16.3676 MHz. Figure 4 shows 1000 Hz Q_k vs. I_k plots for satellite PRN No. 14. These plots are normalized by $NA/2$ in order to give them common scales. The top plot is for the superheterodyne receiver, and the bottom plot is for the direct RF sampling front end. The two clouds of points on each plot correspond to +1 and -1 50 Hz navigation data bits. The clouds are separated along the vertical Q_k axis because the PLL tracks the phase estimate so as to put all of the signal power on the quadrature accumulations.

The carrier-to-noise ratio C/N_0 of each plot is proportional to the square of the separation between the two clouds divided by the vertical variance of each individual cloud. It is apparent from the bottom plot that the direct RF sampling front end has a higher C/N_0 because its clouds have the smallest vertical extent. The calculated carrier-to-noise ratios are C/N_0 = 46.6 dB Hz for the superheterodyne front end and C/N_0 = 48.5 dB Hz for the direct RF sampling front end.

The direct RF sampling front seems to have almost 2dB more sensitivity than the superheterodyne front end, but this C/N_0 difference is negligible due to limitations of the experimental setup. The superheterodyne data was collected almost 40 minutes later than the direct RF sampling data. Thus, the actual satellite signal strength could easily have changed by 2 dB during this time period. PRN 11, which was also present in these two data sets, showed just the opposite trend between these two data sets. The direct RF sampling front end found it to have a C/N_0 equal to 44.3 dB Hz, and the superheterodyne front end found its C/N_0 to be 47.1 dB Hz. Thus, the two receiver frond ends have similar sensitivities.

The carrier phase jitter also can be deduced from the Q_k vs. I_k plots of Fig. 4. Carrier phase jitter affects the aspect ratio of each cloud. Zero jitter variance will produce equal variances in the I_k

and Q_k directions, which results in a circular cloud. A non-zero jitter will elongate the cloud in the horizontal I_k direction. Both pairs of clouds in Fig. 4 appear to be very slightly elongated, which indicates a very modest amount of carrier phase jitter. The calculated carrier phase jitter standard deviations corresponding to Fig. 4 are $\sigma_{\Delta\phi}$ = 3.2 deg for the superheterodyne front end and $\sigma_{\Delta\phi}$ = 3.5 deg for the direct RF sampling front end. This latter value is significantly lower than the predicted maximum based on the sample clock synthesizer's phase jitter spec: $\sigma_{\Delta\phi\,max}$ = (0.00029 cycles)×(1575.42 MHz)/(16.3676 MHz) = 0.028 cycles = 10.0 deg. This low value of the RMS carrier phase jitter indicates that the synthesizer is performing better than its worst-case specifications or that most of its jitter power occurs at a frequency higher than half the accumulation frequency, i.e., higher than 500 Hz. This result also indicates that there are no surprise jitter effects such as out-of-spec. variability of the ADC trigger delay. These numbers represent a low level of carrier phase noise. The 1000 Hz carrier measurement noise standard deviation due to receiver thermal noise is $\sigma_{\Delta\phi therm} = [1000/(2C/N_0)]^{0.5}$ rad, which equals 4.8 deg for the direct RF sampling front end and 6.0 deg for the superheterodyne front end. Thus, sample clock jitter is not the dominant source of carrier phase measurement error.

B. The Effects of Significant ADC Sample Clock Jitter

A number of direct RF sampling cases for systems A and B show significant carrier phase jitter effects when using the lower quality Fluke synthesizer. This is to be expected based on the looser phase noise performance specification of that synthesizer. Figure 5 shows what happens in this situation for two different sampling frequencies when using system B. The top plot, which uses f_s = 99.23 MHz, yields the phase jitter $\sigma_{\Delta\phi}$ = 9.8 deg and the carrier-to-noise ratio C/N_0 = 54.7 dB Hz. The bottom plot yields $\sigma_{\Delta\phi}$ = 12.1 deg and C/N_0 = 54.0 dB Hz at f_s = 77.33 MHz. The sensitivities of these two cases, as evidenced by their C/N_0 values, are superior to the sensitivities of the Fig. 4 cases, but the sample-jitter-induced carrier phase errors are much larger. This carrier phase degradation is evidenced by the horizontal lengthening of the point clouds on both plots of Fig. 5. Sample jitter is the dominant source of carrier phase error for these cases; the RMS carrier phase error due to C/N_0 is 2.6 deg or less.

Two facts demonstrate the culpability of the lower quality synthesizer as the cause of this increased carrier phase jitter. First, the phase jitter standard deviations computed for Fig. 5 are consistent with the synthesizer specification: $\sigma_{\Delta\phi} \leq$ (0.0018 cycles)f_{LI}/f_s, which yields $\sigma_{\Delta\phi} \leq$ 10.3 deg when f_s = 99.23 MHz and $\sigma_{\Delta\phi} \leq$ 13.2 deg when f_s = 77.33 MHz. Note how Fig. 5 illustrates this inverse relationship between the carrier phase jitter and the direct RF sampling frequency: The slower sampling rate of the lower figure yields more elongation in the I_k direction. Second, a test has been run in which the Fluke synthesizer and the HP synthesizer have been compared. This test uses f_s = 55.5053 MHz because the HP synthesizer cannot operate above 60 MHz. This comparison has been performed for both system A and system B. The Fluke synthesizer yields Q_k vs. I_k plots whose point clouds are noticeably elongated in the I_k direction, as in Fig. 5, but the HP synthesizer yields nearly circular point clouds. The superior performance of the HP synthesizer is consistent with the following fact: its maximum RMS timing jitter is more than 10 times smaller than that of the Fluke synthesizer.

It is interesting to look at the power spectral density of the carrier phase jitter. Figure 6 plots the power spectral density of $atan(I_k/Q_k)$ for the data from the top plot of Fig. 5. This plot shows that the phase noise consists primarily of 2 components. One occurs at 60 Hz and its harmonics, with the strongest harmonic peak occurring at the 120 Hz. This appears to be a power supply effect of the Fluke synthesizer. The other phase noise component is broad-band noise that is distributed fairly equally from 100 Hz to 500 Hz. It is not clear why there is a noise peak near 0 Hz. Perhaps this represents residual true carrier phase variations of the tracked GPS signal.

Another test has examined the effects of sample clock jitter on signal power. System A has been run at a sampling frequency of f_s = 5.71429 MHz. GPS signals can be acquired and tracked when the HP synthesizer is used. The value of C/N_0 gets degraded because the bandwidth of system A's BPF is many times wider than the Nyquist frequency. Nevertheless, the system is able to acquire and track a signal with C/N_0 = 45.3 dB Hz. When the Fluke synthesizer is used, however, the system is unable to even acquire a signal. This inability to acquire is the result of extreme power loss. The sample clock phase jitter standard deviation may be as large as half a carrier cycle. In this extreme case, eq. (7) breaks down for predicting the power loss because the approximation in eq. (6b) is not valid. The effective received power is zero if most of the spectral density of the clock jitter occurs above half the accumulation frequency.

C. Common-Mode Nature of Jitter-Induced Carrier Phase Errors

The analysis of Section II indicates that sample clock jitter induces common carrier phase errors on all channels. This has been confirmed experimentally using tracking data from PRN Nos. 10 and 24 for the same data set as has been used to produce the bottom plot of Fig. 5. Figure 7 shows the normalized cross correlation between the $atan(I_k/Q_k)$ carrier phase errors of the two tracked GPS signals. The correlation peak at the time delay $\tau = 0$ reaches 0.95. This level of correlation is closely consistent with the predicted value $\sigma^2_{\Delta\phi}/(\sigma^2_{\Delta\phi}+\sigma^2_{\Delta\phi therm}) = 0.96$ -- recall that $\sigma_{\Delta\phi}$ = 12.1 deg and $\sigma_{\Delta\phi therm}$ = 2.6 deg (for PRN 10) in this case.

This result confirms the analytical prediction that the $\sigma_{\Delta\phi}$ component of the carrier phase error is the same for all tracked satellites. If it is a significant error source, then it can be removed from the navigation solution via the usual clock error correction techniques. This implies that one need not be overly fussy about minimizing sample clock jitter as long as the resulting carrier phase jitter is not large enough to cause tracking problems for the PLL. Note, however, that this ability to correct for the clock phase error may be sensitive to differential tuning of the PLLs for different channels. In the present analysis, the smoother-based PLL is tuned the same for each channel. If one uses a Costas loop, then the PLL bandwidth becomes a function of C/N_0, and this differential tuning may negatively impact the carrier phase error correlation shown in Fig. 7.

VI. Simulation Study

The effects of ADC sample clock jitter have been further investigated using an off-line simulation. The simulation study had two goals. The first was to confirm that the I_k spreading on the Q_k vs. I_k plots could be produced by the addition of ADC timing jitter. The second was to

verify that direct RF sampling also would work with a temperature-compensate crystal oscillator, which has poorer frequency stability than the ovenized crystal oscillators that have been used in this paper's experimental studies.

The simulation mimics a GPS signal and the actions of a direct RF sampling front end. It includes the effects of multiple GPS signals, receiver thermal noise, distortion and delay of the C/A code in the bandpass filter, oscillator frequency drift, synthesizer phase jitter, gain-controlled optimal 2-bit digitization, and actual signal dynamics from line-of-sight motion that is typical of a roof-mounted antenna. Practical implementation issues have limited the simulation's ADC sample clock phase jitter to occur in the frequency band below 500 Hz. Therefore, the simulation can be used to investigate the effects of sample timing jitter on carrier phase measurements and on carrier tracking, but it cannot be used to investigate the effects on signal power -- review eqs. (7) & (8).

The simulation results further confirm that the I_k spreading is caused by ADC clock jitter, and they demonstrate that direct RF sampling works well even when the receiver oscillator is a temperature-compensated crystal oscillator. Consider a typical case whose direct RF sampling frequency is f_s = 11.04612 MHz. This sampling frequency would be good for a dual-frequency direct RF front end that was designed to receive both the C/A code on L1 and the new civilian codes that are slated to begin appearing on L2 in the near future. The L1 carrier gets aliased down to f_{IF} = -4.17516 MHz. The simulation includes an L1 BPF model that has a 3 dB bandwidth of 3.15 MHz (Q = 500) and a model of a temperature compensated crystal oscillator that has a minimum root Allan variance of 1.4×10^{-10} at an averaging time of τ = 0.5 sec. The sample clock jitter is $\sigma_{\Delta t}$ = (0.00028 cycles)/f_s = 2.5×10^{-11} sec, which translates into $\sigma_{\Delta\phi}$ = 14 deg at the L1 carrier frequency. The sample clock jitter power is split evenly between broad-band noise from 0 to 500 Hz and narrow band noise at the discrete frequencies 120 Hz, 180 Hz, 240 Hz, and 300 Hz, as evidenced in the Fluke synthesizer results of Fig. 6. The software receiver is able to successfully acquire and track a signal whose simulated C/N_0 = 49.9 dB Hz. The smoother results show a received C/N_0 of 48.8 dB Hz and an I_k spreading that corresponds to $\sigma_{\Delta\phi}$ = 14 deg. Thus, the simulation verifies that the analytical predictions of Section II indeed explain the experimental results of Section V. It also demonstrates that direct RF sampling can work when the sample clock is a temperature-compensated crystal oscillator.

VII. Summary and Conclusions

Direct RF sampling front ends for GNSS receivers have been studied analytically, experimentally, and via simulation. This type of front end samples at more than twice the information bandwidth of the signal, but at much less than twice the carrier frequency. Such a front end uses intentional aliasing to map the signal band around the GNSS carrier frequency into the Nyquist bandwidth of the sampling system. Bandpass filters ahead of the analog-to-digital converter are used to avoid the loss of carrier-to-noise ratio that otherwise would result from aliased folding into the Nyquist bandwidth of out-of-band noise and interference.

The principal goal of this study has been to investigate the effects of ADC sample timing jitter on the performance of a receiver that uses direct RF sampling. One part of the experimental

study compares the performance of such a system with that of a traditional superheterodyne front end that uses mixing to down-convert the signal before sampling.

The analytical, experimental, and simulation results all demonstrate that direct RF sampling front ends can have performance equal to that superheterodyne mixing front ends. If care is taken not to allow too much timing jitter in the ADC sample clock, then signal power losses and increases in the carrier phase measurement errors can be kept within reasonable bounds. Furthermore, jitter-induced carrier phase measurement errors are common-mode errors that can be removed by the usual technique whereby receiver clock errors are estimated as part of the navigation solution. Limits on jitter-induced carrier phase measurement errors translate directly into bounds on the clock jitter power in the frequency range from DC to half the accumulation frequency. Limits on power losses translate into limits on the jitter power in the frequency range from half the accumulation frequency to half the direct RF sampling frequency.

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Table 1. Characteristics of Experimental Set Ups

Front End Label	A	B	C	D
Gain (dB)	86.1	90.6	88.0	86.0
Noise Figure (dB)	1.0	1.0	2.0	2.0
-3dB Bandwidth at L1 (MHz)	100	20	3.2	3.1
Ant. Gain at Zenith (dB)	4.5	4.5	4.5	4.5

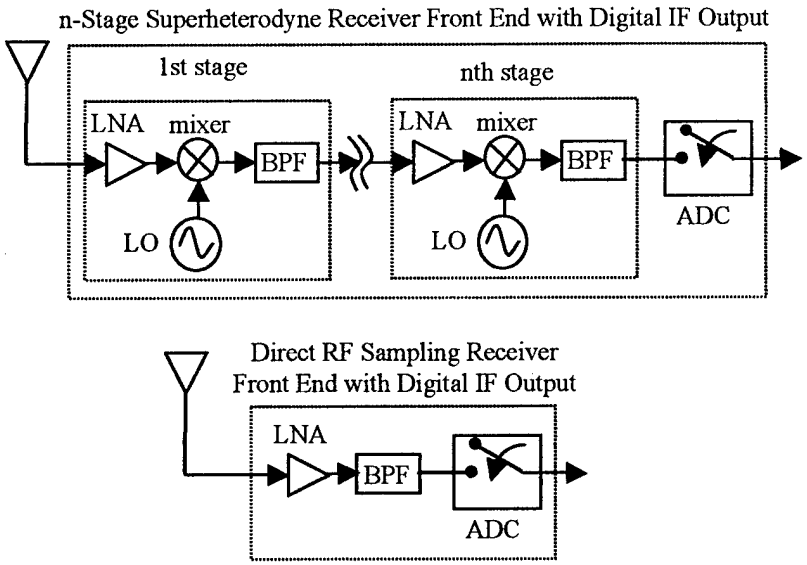

Fig. 1. Superheterodyne receiver front end (top) and direct RF sampling receiver front end (bottom).

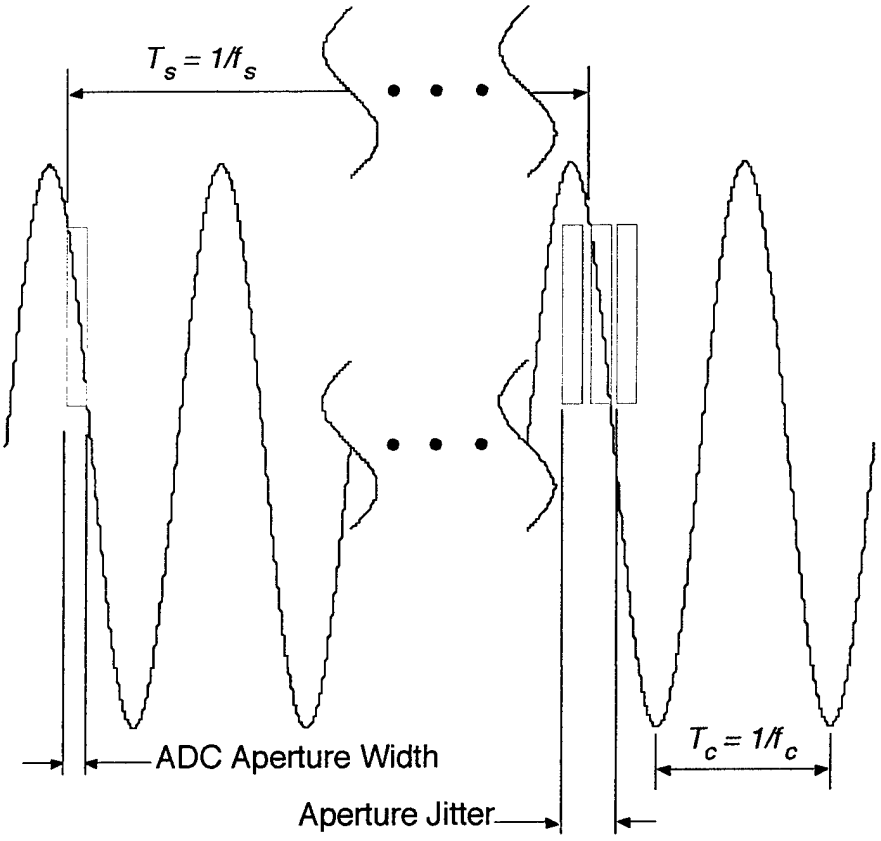

Fig. 2. Direct RF sampling ADC aperture windows superimposed on a nominal carrier wave.

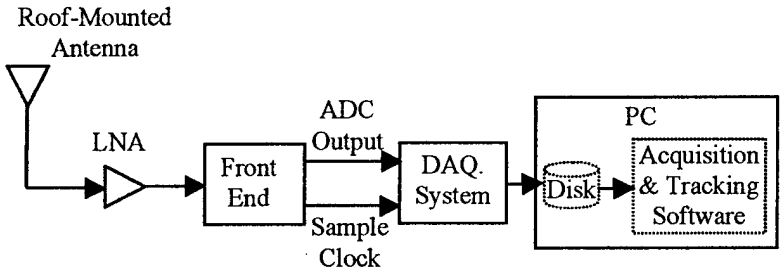

Fig. 3. Generic experimental set-up for evaluation of front ends.

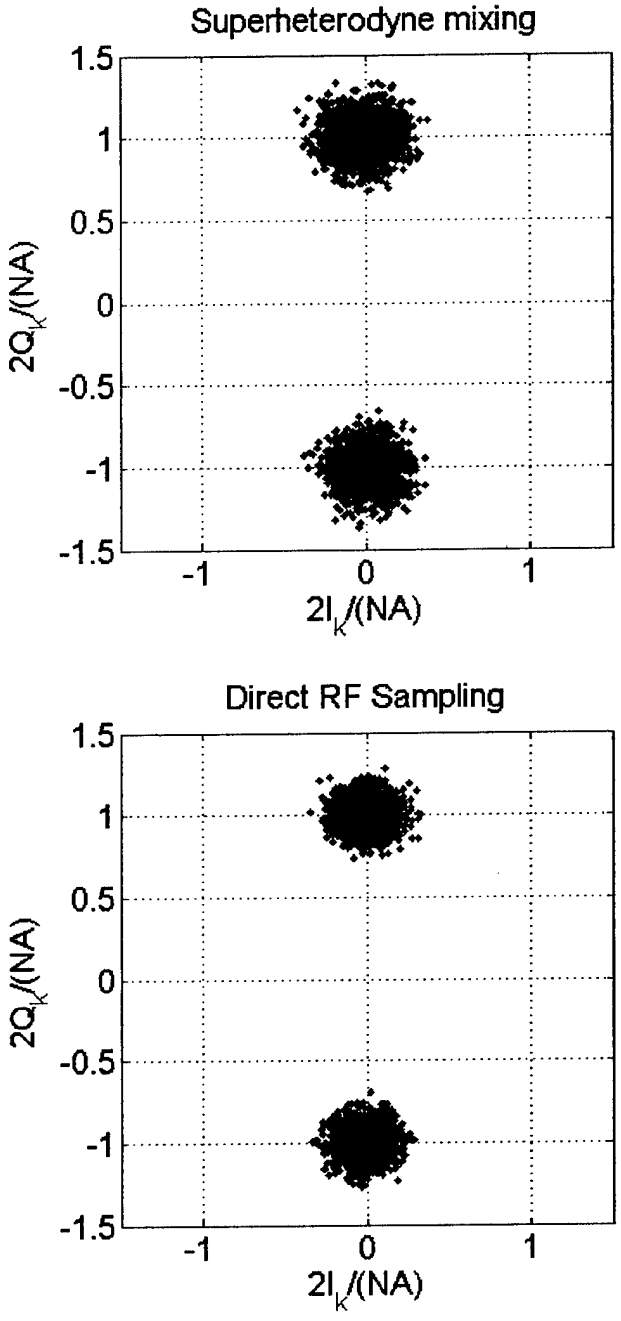

Fig. 4. Normalized Q_k vs. I_k plots for a superheterodyne mixing front end (top plot) and for a direct RF sampling front end (bottom plot) when tracking GPS PRN No. 14.

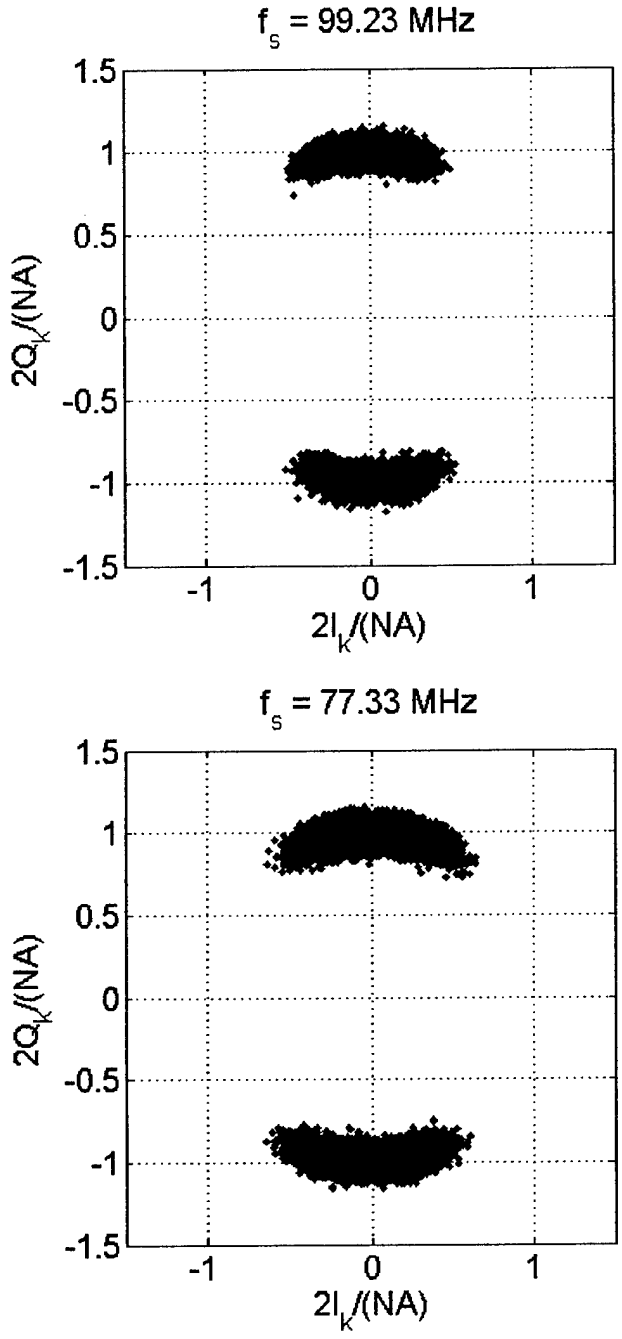

Fig. 5. Normalized Q_k vs. I_k plots for direct RF sampling cases that include significant sample timing jitter when tracking GPS PRN No. 10 (top plot: f_s = 99.23 MHz; bottom plot: f_s = 77.33 MHz).

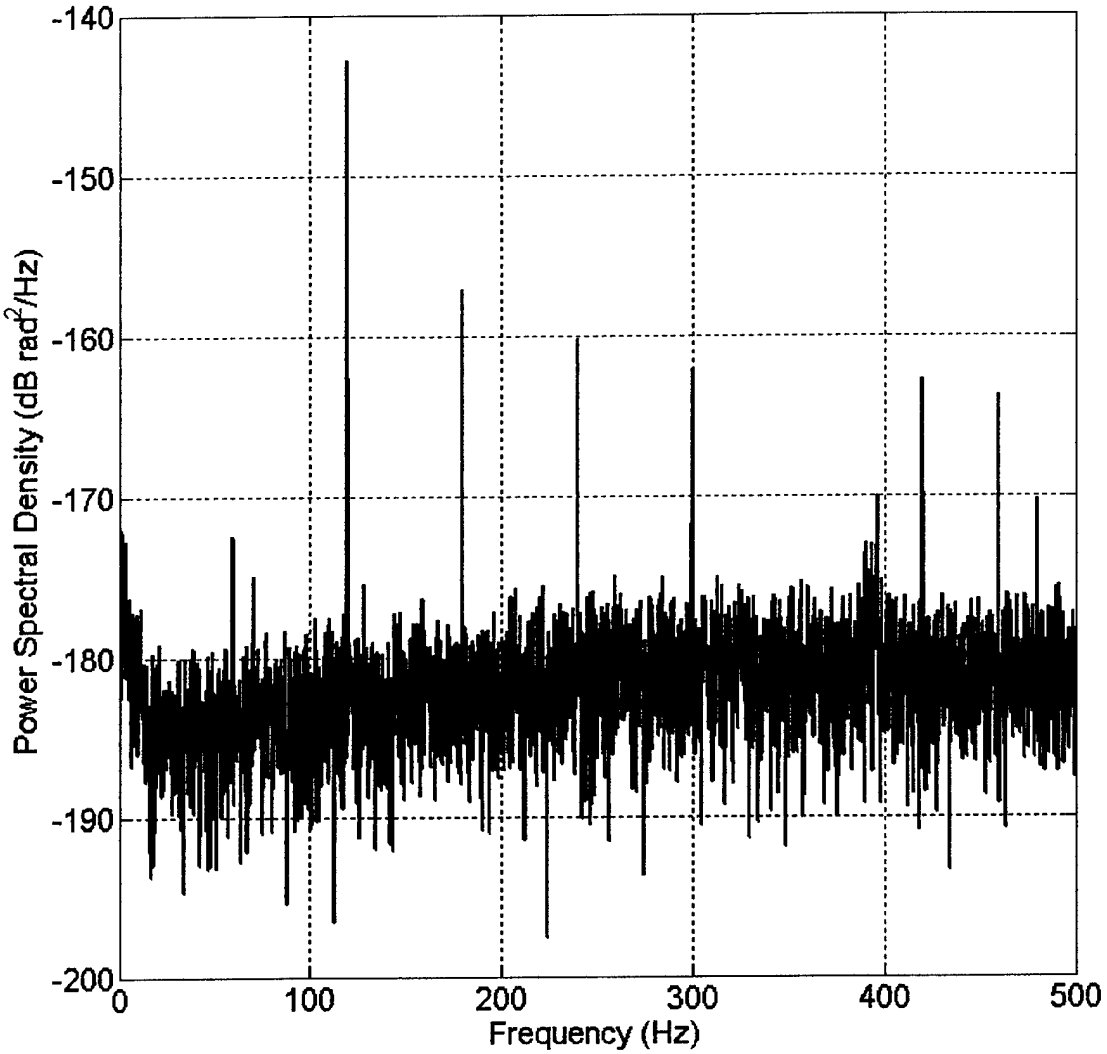

Fig. 6. Power spectral density of the atan(I_k/Q_k) carrier phase jitter, GPS PRN No. 10 with system A using f_s = 99.23 MHz and the Fluke synthesizer.

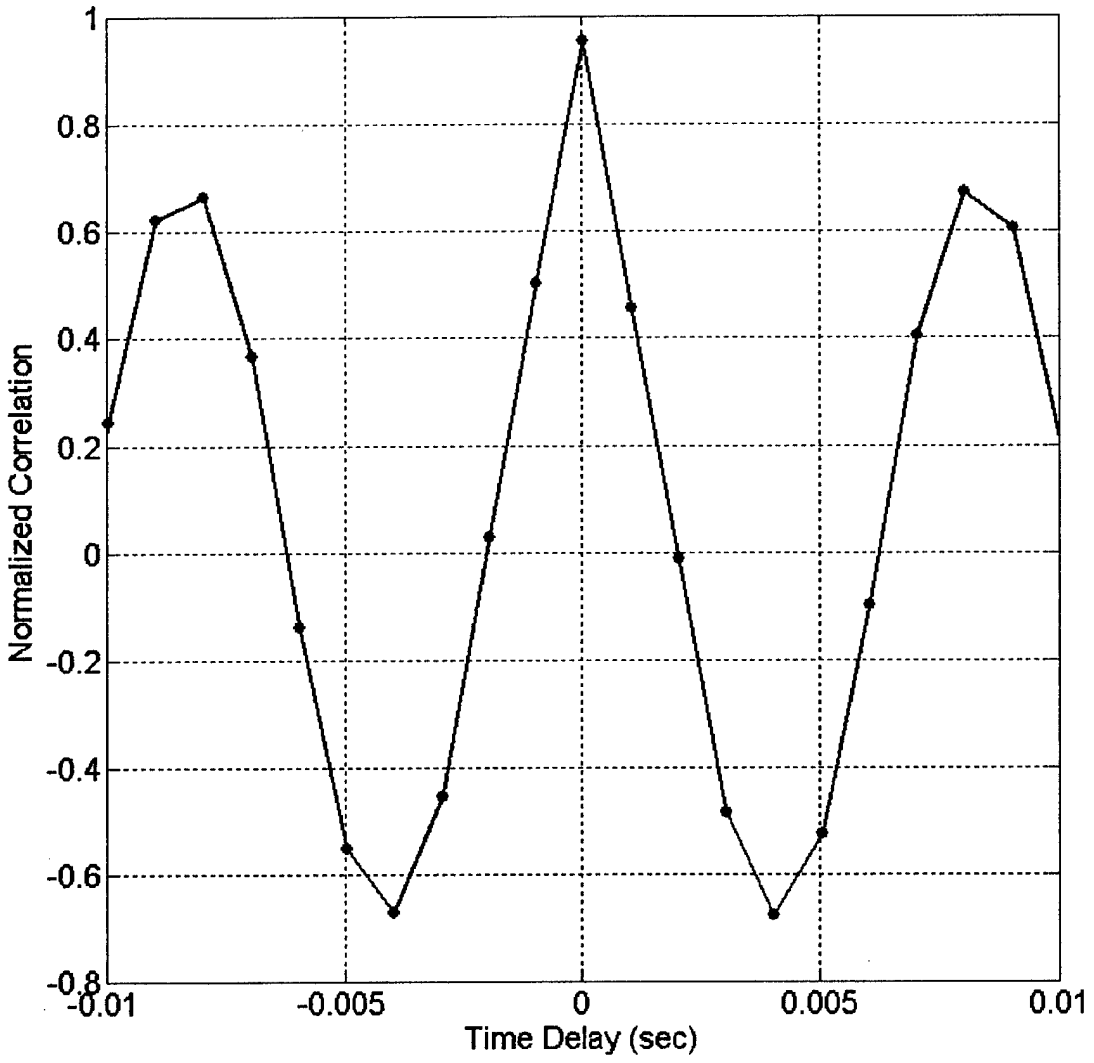

Fig. 7. Correlation between atan(I_k/Q_k) carrier phase jitter time histories of PRN Nos. 10 and 24 when using f_s = 77.33 MHz and the Fluke synthesizer.