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FINAL REPORT

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I. Project Summary/Abstract:

As a step towards developing FET's with a device length of single molecule, modeling shows that FET action in FET's of very short channel length are most likely to occur for long (>5 nm) channel lengths. Therefore self-assembled monolayers of a stacked 11-mercaptoundecanoic acid (MUA) were grown to define an arbitrarily long device length (in excess of 10 nm). The electrical properties of these films were investigated with a self-aligned mesa structure which maximizes device yield by minimizing the device area while still retaining compatibility for the first time with integrated metal wiring. Devices with between 3-7 MUA layers (device length up to 11 nm) were insulating, with currents that decreased exponentially with the number of MUA layers. At higher voltages, the devices exhibiting negative differential resistance and could be used as a non-volatile memory, with enormous (up to 10^6 A/cm^2) current densities, which are necessary for fast access times.

II. Technical Report:

II.A. Introduction and Summary of Major Results

The prospect of employing single organic molecules or organic self-assembled monolayers as the active elements in electronic devices has generated much recent interest. To make a FET structure, we first investigate the fields required in gate oxides in very short channel devices which are required to change the surface potential by a significant amount. We find the that higher fields are required for $L < 5$ nm, higher than that of the breakdown of good insulators. We then focus on growing molecular structures with a thickness longer than 5 nm, and growing them in structure amenable to integrated wiring but still with minimum junction areas.

The major results were:

(i) As channel length decreases, the gate insulator field required to modulate a surface potential increases.

(ii) For a gate insulator with a breakdown of silicon dioxide, FET's will probably require $L > 5$ nm

(iii). A structure for creating organic devices with L defined by molecular length, with very small junction area AND capable of integrated wiring (for circuits, HF probes, etc) was developed.

(iv.) The structure was realized with self-assembled Self Assembled Multilayers of 11-mercaptoundecanoic acid (MUA) ($HS(CH_2)_{11}COOH$)) with device L up to 11 nm defined by the monolayers. The high yield of this structure was confirmed, and an insulating behavior of the MUA, depending on the number of monolayers as expected, was observed.

(vi). At higher voltages, negative differential resistance was observed with exceedingly high current densities, up to 10^6 A/cm2

(vi) The NDR was due to a dynamic programming/erasing mechanism, which varied the device conductivity between high and low conductivity states.

(vii) Functioning as a nonvolatile memory, the device could be written and erased over 10^4 X with little if any degradation.

II. B. VLSI FET Scaling Considerations Applied to Self-Assembled Monolayer Organic FETs

Organic self-assembled monolayer and single-molecule devices have received much attention as potential alternatives to silicon for the scaling of device dimensions to a few nanometers. In this work, we use VLSI scaling considerations and 2-D electrostatic modeling to determine guidelines for designing monolayer-FET structures that can hope to sufficiently modulate the semiconductor (monolayer) surface potential via the gate terminal for transistor action. Such guidelines are necessary since it is widely recognized that the ultra short (~1-2 nm) monolayer channel makes gate-channel coupling difficult. The key results of this section of work are:

(i) Contrary to expectations, the gate insulator thickness should not be scaled to very short dimensions to obtain a maximum modulation of the surface potential for a fixed maximum gate field.

(ii) Regardless of the choice of gate insulator, it will be very difficult to obtain transistor action for channels less than 5 nm in length.

The modeling focuses on the subthreshold region where the channel surface potential (φ_s) must be modulated by a substantial fraction of the bandgap to turn the device on (Figure 1). For example, experimental measurements of the model Au-benzenedithiol-Au system suggest that it will be necessary to modulate the channel potential by ~1 V to align molecular levels with source-drain Fermi levels [1].

The maximum ability of the gate potential V_g to control the surface potential is determined by both the gate-surface coupling efficiency $\xi \equiv \Delta\varphi_s / \Delta V_g$ and the maximum electric field that the gate insulator can sustain before breakdown. A large ξ depends on a low t_{ins}/L ratio, as expected for VLSI short-channel scaling, and is little affected by the gate dielectric (Figure 2). For VLSI technology, typical ratios of t_{ins}/L are ~ 0.03, which corresponds to $\xi \sim 1$ [2]. In contrast, a typical monolayer FET structure has a channel length of only 1-2 nm and insulator thickness of at least 2-3 nm [3,4], which we find leads to a ratio of $t_{ins}/L \geq 2$ and poor gate-surface coupling of $\xi \leq 0.1$. Physically, this results from the classic short-channel effect of a large surface-source/drain capacitance.

The above analysis suggests (falsely) that structures with thin gate insulators and high ξ should be used for a maximum surface modulation. However, the possibility of dielectric breakdown of the gate insulator must also be considered. Figure 3 shows the electric fields

inside an SiO_2 gate insulator as a function of t_{ins} under the condition that a sufficient voltage is applied to the gate to obtain $\Delta\varphi_s = 1$ V. Both the vertical gate field in the middle of the channel (A) and gate-drain field (B) are similar at thick t_{ins} for given L. Although the required gate-channel field drops with thin t_{ins} as expected for increasing ξ, the gate-drain field grows rapidly. Breakdown in the gate-drain region is thus the limit for modulating the surface potential. We note that this limit is not observed in VLSI because of longer channels and lower required $\Delta\varphi_s$. Because the gate-drain field is minimized in thicker insulators, increasing t_{ins} is the optimal approach to measure a gate effect, although the resulting transistor may have a poor transconductance. Furthermore, devices with $L <$ 4 nm cannot be modulated by 1 V, regardless of insulator material or thickness (Figure 4). For example, with $L = 2$ nm, $\Delta\varphi_s$ of ~ 1 V would require an SiO_2 field of 18-22 MV/cm, well beyond breakdown (~10 MV/cm in SiO_2). If L is increased to 5 nm, a field of 15 MV/cm is required if $t_{ins} = 1$ nm, but with a thicker $t_{ins} = 10$ nm the field decreases to 8 MV/cm, below breakdown.

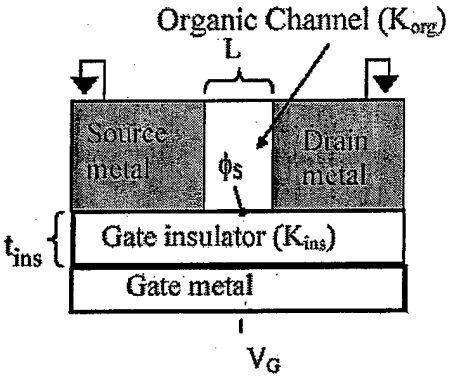

Figure 1. FET geometry used in simulations. Variable parameters are channel length L, insulator thickness t_{ins}, and insulator and channel dielectric constants κ_{ins} and κ_{org}. Of particular interest is the channel potential φ_s for a voltage V_g applied to the gate with source and drain grounded. The inverted structure with gate on bottom is typical in monolayer FETs but is not critical to the results.

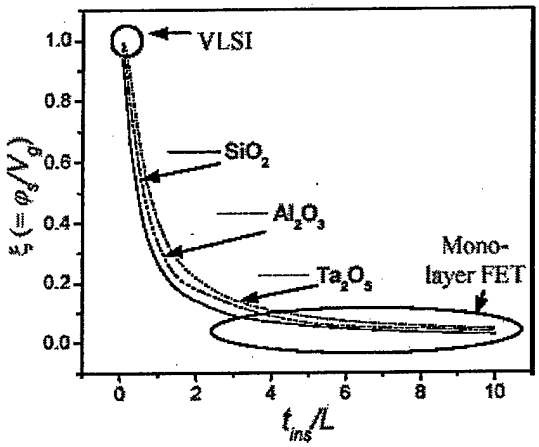

Figure 2. Coupling efficiency ξ vs. t_{ins}/L for an organic channel with $\kappa_{org} = 2.5$ and gate insulators SiO_2 ($\kappa_{ins} = 3.9$), Al_2O_3 ($\kappa_{ins} = 9$), and Ta_2O_5 ($\kappa_{ins} = 25$). Also shown is coupling for typical VLSI transistor ($t_{ins}/L \sim 0.03$) and typical monolayer FET ($t_{ins}/L \sim 2$ - 50).

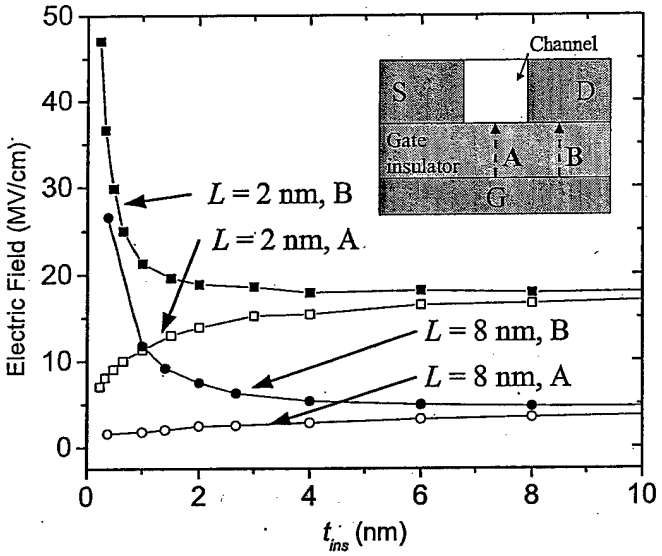

Figure 3. Average electric fields along axes A and B (inset) in an SiO_2 gate insulator necessary to obtain $\Delta\varphi_s$ = 1 V as a function of t_{ins} for L = 2 nm and L = 8 nm. The highest field, which is along axis B, limits the gate modulation.

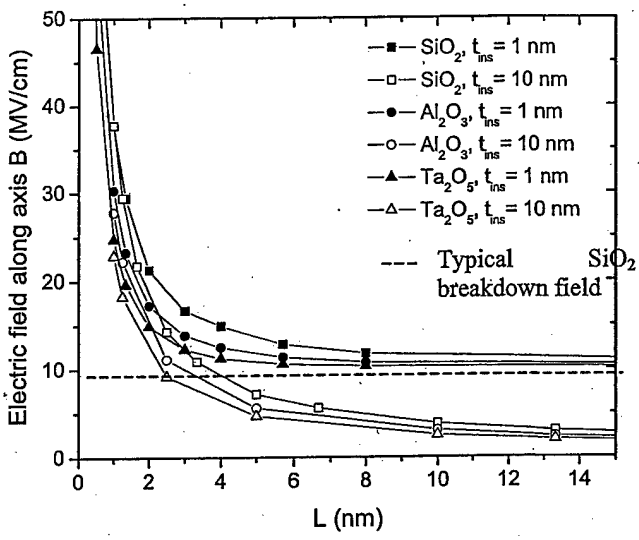

Figure 4. Average electric fields along axis B (inset, Figure 3) necessary to obtain $\Delta\varphi_s$ = 1 vs L for different gate dielectrics of thickness 1 and 10 nm. A typical breakdown field (10^7 V/cm) for SiO_2 is also shown. SiO_2 structures with t_{ins} = 10 nm and L > 4 nm will be able to modulate φ_s by 1 V without insulator breakdown. Although the required electric fields in Al_2O_3 and Ta_2O_5 are lower than in SiO_2, this advantage is offset by lower breakdown fields (~ 3 MV/cm for Ta_2O_5) [5].

In summary, 2-D modeling indicates that relatively thick gate insulators are desirable for successfully realizing monolayer FETs. Most significantly, it will be very difficult to obtain transistor action under any circumstances for L ~ 1-3 nm, and the best chance for success is for L> 5 nm. This is because to turn on a FET it will be necessary to modulate the surface potential on the order of 1 V. The required electric fields in gate oxides to achieve this condition for very short channel lengths (e.g. < 5 nm) will be greater than the breakdown fields of very good dielectrics (e.g. SiO2). Thus the best chances of FET action will occur for longer channel lengths where such large fields are not required.

The next section of the work is therefore geared towards creating monolayer structures which are thicker than 5 nm.

II. C. Growth of Self Assembled Multilayers of 11-mercaptoundecanoic acid (MUA) ($HS(CH_2)_{11}COOH$)) in a Self-Aligned Mesa Structure

A variety of two-terminal monolayer devices and even integrated memory circuits (based on bi-stable devices) have been demonstrated. [6-10] One of the critical issues in the design of monolayer devices is the minimization of the overlap area between the metal electrodes that contact the monolayer. The minimization of device area is necessary to reduce the power consumption and to reduce the likelihood of metal penetration through the thin organic layer, which can lead to electrical defects and shorting. A further constraint in the development of monolayer devices for circuit application is that the fabrication procedure must allow integrated metal wiring. This requirement is particularly challenging because of the limited compatibility between most self-assembled monolayers and conventional metal-patterning techniques. Many common approaches for fabricating self-assembled monolayer and single molecule devices, such as scanning tunneling microscopy/conducting-probe atomic-force microscopy, mercury-drop junctions, and crossed-wire junctions, are not compatible with such integration. [7] A structure that minimizes device areas but still allows the use of (relatively) large patterned metal for connection to other devices or measurement probes is therefore desirable.

In this work, we demonstrate such an approach to fabricating molecular-scale devices that allows very small dimensions and integrated metal wiring. We also present the use of self-assembled multilayers of 11-mercaptoundecanoic acid (MUA) ($HS(CH_2)_{11}COOH$)) to define an arbitrarily long distance between electrodes and report the first current-voltage characteristics of these multilayers. The ability to define arbitrarily long distances between the electrodes is of interest not only for further study of transport in thin organic layers but also because it provides the potential for three-terminal measurements. In a three-terminal, field-effect transistor (FET) geometry, a large distance between source and drain contacts helps to allow penetration of the gate field into the organic layer for current modulation.

A self-aligned procedure was used to fabricate electrical test devices with minimal overlap areas while still allowing integrated metal wiring. This approach utilizes the thickness of a deposited metal (which can be controlled to a resolution of ~1 nm) to define the width of the device area. The device dimension defined by the deposited metal is therefore much smaller than can be achieved by standard lithography techniques. Our work differs from other work that utilizes the thickness of a deposited layer as a critical dimension in that we do not cleave the sample or polish a cross-section. [11-14]

In our work, silicon wafers were patterned by standard photolithography followed by plasma-etching to define mesas that were 2-3 μm high (Fig. 6(a)). A ~30-nm thermal oxide was then grown on the silicon wafer, including the step edges. Next, an electron-beam evaporator was used to deposit a layer of Au (25 nm) followed by an insulating layer of layer of silicon oxide (SiO_x) (30-50 nm) (Fig. 6(b)). Thin adhesion layers of Ti (~5 nm) were evaporated prior to both Au and SiO_x deposition. The evaporation direction was

normal to the surface. The evaporation geometry was kept constant for every layer by rotating the source materials between evaporations while maintaining the same focal point for the electron beam so that each film was evaporated from the same location. The sequential deposition of the Au layer followed by the insulating SiO_x in identical evaporation geometries ensures that, although the top of the Au is covered by SiO_x, a small fraction of the Au layer along the side of the mesa remains exposed. Multilayers of MUA were then grown on this exposed Au (as described later in further detail) (Fig. 6(c)). Finally, a second Au layer (50 nm) was deposited onto the sample at an angle (~60° from the normal) to form a top contact to the organic (Fig. 6(d)). The azimuthal angle was chosen to be incident towards the site of the etched step. This layer was patterned by shadow mask to limit the area of the second gold layer on top of the mesa, so that the first gold layer could be electrically contacted later with a probe (Fig. 6(e)). During the second Au evaporation, the sample stage was cooled to temperatures of 100 K, and the Au evaporation rate was kept below 0.05 nm/s to minimize damage to the MUA. [15] For comparison, some devices were fabricated without any SiO_x deposition so that the Au electrodes were separated by only the MUA layer over the entire electrode overlap area. (In these devices, the first Au/Ti layer was defined by a shadow mask instead of silicon etching.)

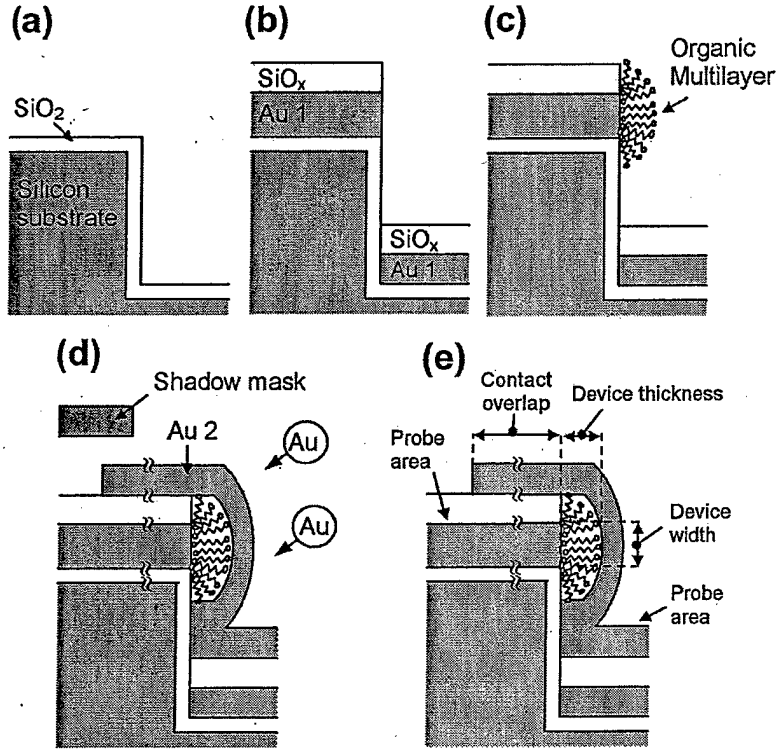

Figure 6. Schematic of device fabrication. (a) A silicon wafer is patterned by photolithography, plasma-etched to define 2-3 μm tall mesas, and thermally oxidized (30 nm). (b). A thin gold layer (25 nm) and SiO_x layer (30 nm) are deposited sequentially by e-beam evaporation, with 5-nm Ti layers used for adhesion purposes (not shown). (c). Organic multilayer is grown on exposed gold edge. (d) Second gold layer (50 nm) is

deposited at angle to define top contact. (e) Probe areas are much larger than effective device width, which is defined by the thickness of the first gold layer.

The critical feature of this process is the use of an insulating layer to limit the device area to the gold edge. As indicated in Fig. 6(e), this self-aligned layer allows the use of large electrode contact pads (typically 25 x 50 μm) and large electrode overlap areas (25 x 50 μm) while still retaining minimal device areas. The accuracy of the shadow-mask alignment to the mesa edge was not critical, typically being 5 – 50 μm. In the area where the two metals overlap the deposited oxide insulator prevents any conduction between electrodes, and the device area is limited to the sidewall of the mesa. This device area is defined as the product of the thickness of the gold layer and the width of the second shadow-masked Au layers to obtain 25 nm x ~25 microns $\cong 6 \times 10^{-9}$ cm^2. (Note that in the active device, the distance between the metal electrodes is defined by the thickness of the self-assembled organic layer and is typically 3 to 10 nm). For comparison, when the devices were fabricated without the insulating layer, the device area includes the much larger top overlap area, typically ~25 x 50 μm, corresponding to an increase in area of $\sim 10^6$. We also note that these minimal device areas are attainable without the need for careful alignment and could be readily decreased by over an order of magnitude or more by using photolithography to define the width of the device instead of a shadow mask.

The organic layer examined in this study consisted of self-assembled multilayers of 11-mercaptoundecanoic acid (MUA). Using MUA, ordered layers of arbitrary thickness were possible, whereas conventional rigid monolayers do not assemble well for molecules with lengths > 5 nm. [16] MUA has been shown to form well-ordered multilayers via a simple deposition process. [17] Briefly, a gold-coated substrate is immersed in a 1 mM solution of MUA in ethanol for 2-12 hours to form a monolayer of MUA. The exposed COOH functional groups of the MUA monolayer are then bonded to Cu ions by immersing the sample in a solution containing $Cu(ClO_4)_2$ for 5 minutes. A second layer of MUA (with the same orientation as the first) is grown by returning the sample to the MUA solution. Multiple layers can be grown by alternating MUA and Cu depositions. A conceptual diagram of the structure of an assembled mercaptoalkanoic acid multilayer is shown in Fig. 2(a). Previous work suggests that the oxidation state of the Cu is +2; however, the exact stoichiometry of the binding between the copper ions and molecules is less clear and may not correspond to the simple 1:1 ratio depicted in Fig. 7(a) [18] A linear increase in thickness of 1.6 nm/layer for MUA was measured in our work by ellipsometry (with n = 1.45) on samples grown on a thin layer of Au (80 nm, with 5 nm Ti adhesion layer) thermally evaporated onto silicon substrates (Fig. 7(b)).

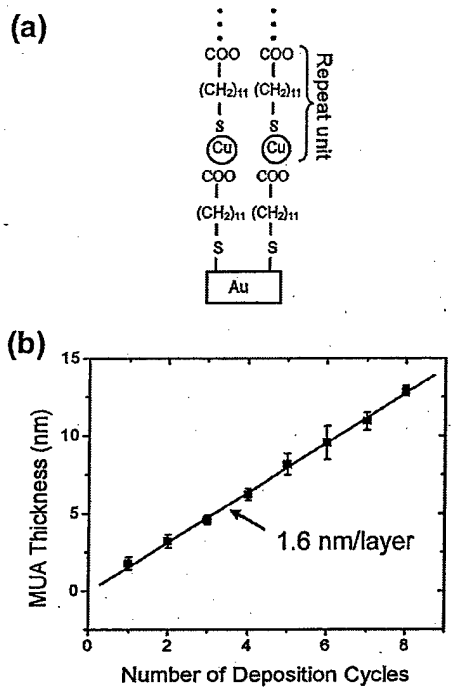

Figure 7. (a) Conceptual structure of MUA multiplayer on Au substrate. The actual stoichiometry of the binding between the copper and molecules may not correspond to the depicted 1:1 ratio. (b) MUA film thickness (determined by ellipsometry) vs number of deposition cycles.

II.D. Electrical Properties of Self-Assembled MUA layers on self-Aligned Edge Structure

The device fabrication approach was evaluated by recording the electrical characteristics of devices with differing numbers of MUA layers at room temperature. Devices were either insulating, with low current densities (up to a factor of 10^7 smaller than control samples prepared without an organic layer between the gold electrodes) (Fig. 8(a)) and nonlinear current-voltage characteristics (Fig. 8(b)), or shorted, with high current densities and ohmic current-voltage traces. The resistances of the shorted devices were comparable to those of devices fabricated without an organic layer, indicating the presence of conducting pathways between the gold electrodes. As the number of MUA layers was increased from 3 to 7 layers, the yield of insulating devices increased to as high as ~90% for 7 layers of MUA (devices made with 1-2 MUA layers were typically shorted) (Fig. 4). Yields of unshorted devices were also much higher than in comparison devices fabricated without deposition of the SiO_x layer. For example, in devices with 7 MUA layers, only 16% of devices without the SiO_x layer (with top overlap area averaging from 10- 600 μm^2) are not shorted, whereas with the self-aligned SiO_x layer ~90% of the devices are not shorted.

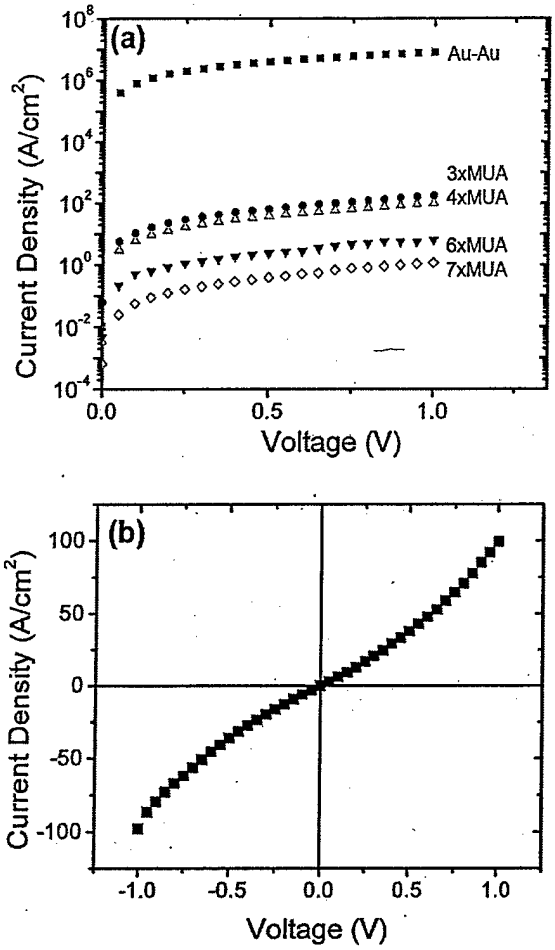

Figure 8. (a) Average current densities vs voltage (top contact with respect to lower contact) of devices with three to seven MUA layers. Also shown for reference is the current density of devices without any MUA layers (Au-Au contact). Each curve represents the geometric average of 6 to 22 devices. (b) Average current density vs. voltage for devices with four MUA layers.

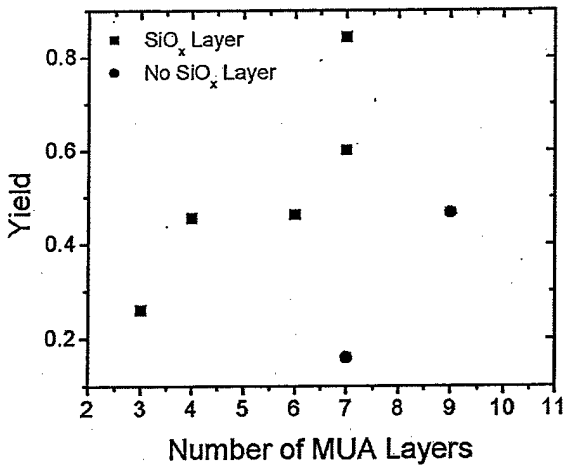

Figure 9. Yield (defined as fraction of unshorted devices) for samples made with SiO_x layer over first gold layer (squares) and without SiO_x layer (circles). Each point corresponds to at least 15 measured devices. Typical overlap areas in devices without SiO_x were $10 - 600\ \mu m^2$.

Current densities in insulating devices at a given voltage were similar for devices with the insulating SiO_x layer and without the insulating layer (Fig. 10). Device currents decreased exponentially with the number of MUA layers. The best fit to the geometric average of current density (measured at 0.5 V) yields a slope of one decade per 1.8 layers. Previous work on similar, alkanethiol monolayers indicates that the transport mechanism for such layers at low bias is coherent tunneling, implying that the current (generally measured near a bias of 0 V) decreases exponentially with the length of the monolayer (or multilayer). [19-25] Reported values of the decay constant β, which varies only slightly with voltage, range from 5/nm to ~10/nm. [25] Our slope corresponds to a much lower $\beta = 0.7$/nm at 0.5 V, which indicates that transport in these multilayers (with interspersed copper layers) differs substantially from transport in pure alkanethiol monolayers. Further, although device currents remained stable over multiple sweeps in each device, the current density varied significantly (by up to a factor of 100) between similar devices. The source of this variation is not clear. A more detailed study of the active layer was inhibited by the geometry of the structure, which prevented us from studying the MUA multilayer formation on the sidewall of the mesa with conventional means such as scanning probe microscopy. However, the similarity between current densities for devices with and without the SiO_x layer suggests that the structure of the layers grown on the gold sidewalls was similar to that on conventional flat surfaces. Furthermore, the possibility that a thin oxide incidentally forms over portions of the gold sidewall in the insulating-layer devices so that the observed electrical characteristics are dominated by leakage through the thin oxide film is unlikely. In this case, the current density would not decrease with the number of MUA layers and would also not be similar to that measured in control devices, in contrast to what is observed in our experiments.

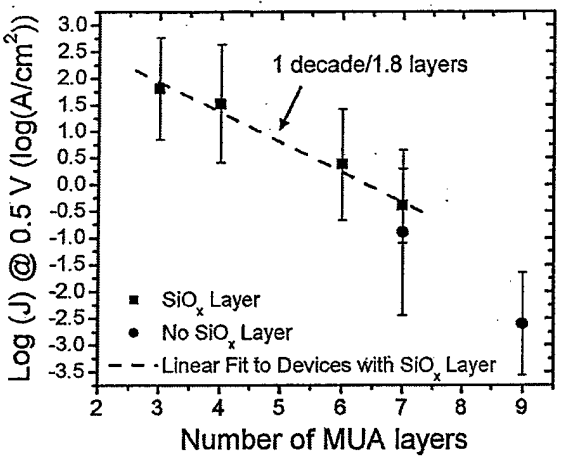

Figure 10. Log_{10} of current density (measured at a voltage of 0.5 V applied to top electrode) vs number of MUA layers. Each point was calculated by averaging the logarithms of 6 to 22 device currents; error bars represent the standard deviation of these logarithms. Data from devices with an SiO_x layer (squares) and without an SiO_x layer (circles) are shown, as well as a linear fit to the data of devices with an SiO_x layer.

In conclusion, we have demonstrated a promising approach for fabricating molecular-scale electronic devices. This approach employs a self-aligned insulating layer to minimize device area combined with multiple self-assembled organic layers to further minimize electrical defects and obtain arbitrary device lengths. The device structure was used to measure the electrical characteristics of self-assembled multilayers of MUA. These layers were electrically insulating, and yields of unshorted devices as high as 90% were obtained. This approach may provide a robust platform for measuring and integrating small-area molecular-scale organic devices into circuits.

II.E. Non-volatile Memory and NDR with Record High Current Densities in Organic Thin Films and Frequency Behavior

Thin (12 nm) organic films consisting of self-assembled multilayers of 11-mercaptoundecanoic acid (MUA) were contacted by gold electrodes. Room-temperature current-voltage measurements of the resulting devices revealed negative differential resistance with very high current densities (10^6 A/cm^2). The devices could be operated as non-volatile memory by applying high-voltage pulses to decrease the device conductivity or low-voltage pulses to increase the conductivity; the conductivity of the stored state ranged over 10^3 and could be read non-destructively by applying a still-lower voltage pulse. The programmed state remained stable for longer than a month [check] and devices were functional for more than 10^4 write/erase cycles. These films are promising candidates for use in dense, high-speed memory arrays, where resistance-capacitance (RC) delays can be minimized by large current densities.

There is growing interest in using organic devices as electronic memory elements [26]. A variety of promising approaches, including reconfigurable and redox-active molecules [27,28-30], charge-trapping [31], write-once mechanisms [32], and others [33], have recently been demonstrated. Much of this research has been driven by the desire for non-volatile, high-speed, and high-density memory with inexpensive fabrication costs. A fundamental challenge in satisfying the demands for high speed and density is that speed-limiting resistance-capacitance delays tend to increase rapidly as the capacitance between metal interconnect lines is increased in high-density arrays. High-current densities are desirable to overcome these delays. In this work we report devices consisting of self-assembled multilayers of the insulating molecule 11-mercaptoundecanoic acid (MUA) display negative differential resistance (NDR) and non-volatile, programmable conductance switching with high current densities (up to 10^7 A/cm^2). These current densities are higher than those reported in the previous studies by ..... and the devices are therefore promising candidates for high-density, non-volatile memory with high density and speed.

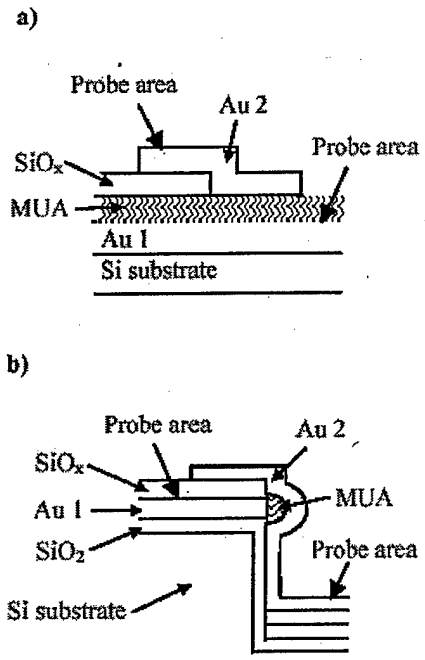

Figure 11. a) Schematic of planar structure. The active device area (where the Au electrodes overlap with no SiO_x present) is typically 200 μm^2. The device can be contacted through probe areas (typically >1000 μm^2) on top of and adjacent to the SiO_x layer. b) Schematic of insulating-layer structure. The active device area is defined by the thickness of the 1st Au layer on which the MUA self-assembles and the width of the 2nd, shadow-masked Au layer (25 nm x 25 μm). The electrical characteristics can be probed through large-area contact pads (25 x 50 μm).

Devices were fabricated using both planar and self-aligned structures (Fig. 11 (a,b)). In the planar structure, a layer of Au (80 nm, with 5-nm Ti layer for adhesion) was deposited onto a Si substrate. Multiple layers of MUA (typically 7-8, to a total thickness of ~12 nm) were then grown on the exposed Au along the edge of the mesa by alternating immersions of the sample in dilute solutions of MUA and $Cu(ClO_4)_2$ in ethanol [17]. Next, a patterned layer of SiO_x (70 nm) was deposited through a shadow mask. Finally, another Au layer was deposited through a second shadow mask with the sample held at low temperatures (100 K) to avoid thermal damage to the organic layer. The SiO_x layer provides a rigid platform so that the 2nd Au layer can be contacted by a needle probe for electrical measurements without damaging the organic film and helps minimize the device active area (to avoid pinholes leading to shorted devices). Still, these planar-type devices typically had relatively large device areas of 10^{-6} cm^2.

To further decrease the device area, the second structure used a self-aligned, insulating layer of silicon oxide (SiO_x) deposited on a gold electrode (Fig. 11b). Details of the structure fabrication are described in an earlier section of this report. Briefly, trenches were etched into a Si wafer to define mesas, onto which self-aligned layers of Au (25 nm) and SiO_x (40 nm) were deposited (with 5-nm Ti layers for adhesion). After MUA growth, a second Au layer was then deposited on top of the organic film to define the second electrode. In this structure, the active device area is limited to the edge of the first Au film by the SiO_x layer and so is typically 10^{-9} cm^2.

Most devices were initially insulating, with current densities that ranged from 10^{-3} to 10^{-1} A/cm^2 at 1 V. After sweeping the voltage to ±6.5 V, the current increased sharply and in subsequent direct-current (DC) scans symmetric, N-shaped negative differential resistance (NDR) with a peak at ±3.5 V was observed (Fig. 12a). Scan-to-scan variations in peak current of up to 50% and in the peak voltage (±0.5 V) were observed, but devices could be scanned multiple times without failing. Devices had very large peak-to-valley ratios (PVRs) of up to 140:1, although ratios of ~10:1 were more common.

The current-voltage characteristics of both structures were qualitatively similar; however, much higher current densities of up to 10^6 A/cm^2 were observed in the smaller-area, insulating-layer structure (Fig. 12b). That the MUA layer is responsible for the observed electrical characteristics was confirmed by studying control devices fabricated without the MUA layer or with the 2nd Au electrode overlapping only the SiO_x layer. In both structures, devices without the MUA layer were shorted, and when the electrodes overlapped over only the SiO_x layer, insulating characteristics were measured. Significant hysteresis in the current-voltage trace was observed, with decreasing-voltage scans revealing low-voltage conductivities that were up to 10^3 larger than those observed in increasing-voltage scans. Measurements on devices of varying thickness between 4-20 nm (3-14 MUA layers) indicated an optimal thickness of ~10-14 nm (6-8 layers) for the MUA film. All the studied thickness exhibited the same qualitative effect, but devices thinner than 10-14 nm sometimes failed after several voltage scans and in devices thicker than 10-14 nm the NDR characteristics were observed less reproducibly.

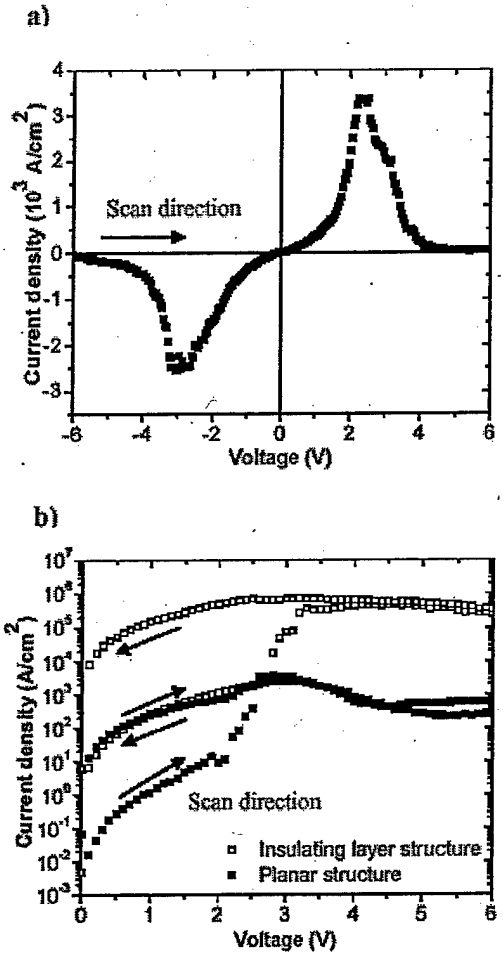

Figure 12. a.) Current density vs voltage of device in planar structure with 12-nm MUA film for scan from –6 to 6 V. b.) Current-density vs voltage (with applied voltage) of 12-nm MUA films in self-aligned (hollow squares) and planar (solid squares) structures.

Devices could be programmed into low- and high-conductivity states by applying high (8 to 10 V) and low (4 to 5 V) voltage pulses. Nondestructive reading of the states could be performed with a yet smaller (1 V) voltage. A typical programming/reading sequence on a self-aligned device is shown in Fig. 13. Initially, the device is in a low-conductivity state so that the 1-V, 7-ms voltage pulse reads a current in the μA range. Next, the device is programmed into a high-conductivity state by applying a 4-V pulse. The subsequent 1-V pulse measures a current of 200 μA. A 10-V pulse then returns the device to a low-conductivity state that is read by the final 1-V pulse. Programmed states remained stable for longer than one month in an inert atmosphere. Preliminary measurements of the transient switching behavior suggest that the device can be switched into the low-conductivity state in less than 100 ns, although the high-conductivity state may take on the order of ms to program. This suggests that the motion of atoms is involved in switching

and that the process is not purely electronic. Most surprisingly, devices could endure multiple programming cycles without degrading (Fig. 14). A ratio of ~10^3 between the high- and low-conductivity states was maintained through 10^4 cycles!

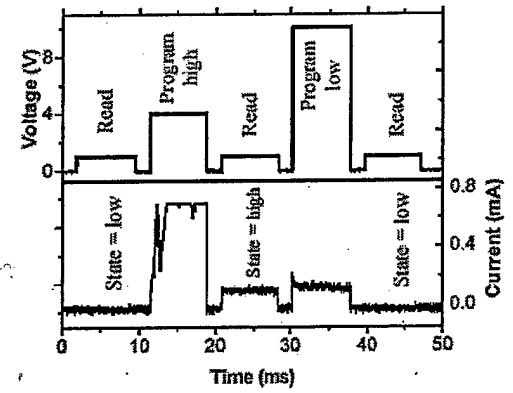

Figure 13. Typical programming sequence for 11-nm MUA film in insulating-layer structure. The current measured in the "Program high" stage exceeds the measurement range of the oscilloscope and is cutoff; however, it is generally ~ 1.5 mA.

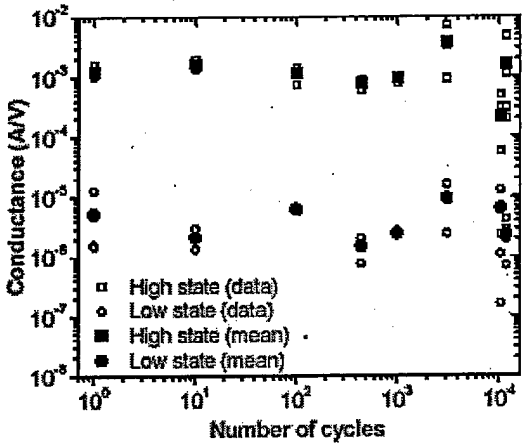

Figure 14. Evolution of the conductance (measured at 1 V) of high and low memory states following multiple program high/low cycles. The device consists of an 11-nm thick MUA film in the self-aligned structure. A pulse generator was used to apply a sequence of several ms 4-V (program high) and 10-V (program low) pulses.

Qualitatively similar electrical characteristics at much lower current densities to those reported here have been observed previously, primarily in electroformed inorganic films, though most recently in thin films of aluminum tris(8-hydroxyquinoline) (Alq_3) containing a thin layer of metallic nanoclusters [34]. Most authors have attributed the behavior of electroformed devices to the formation and destruction of conducting filaments in the insulating layer [35]. Charge trapping (on metal atoms that were fabricated inside or migrate into the insulator) has also been suggested [36], but the stability of our devices and

their extreme thinness (down to 4 nm) indicate that it is unlikely that this is the dominant mechanism in our work. Temperature-dependent measurements will be necessary to determine the relevant conduction mechanism. However, the high current densities of 10^6 A/cm^2 approach the current densities of 10^7 A/cm^2 measured in control devices fabricated without multilayer deposition so there is direct contact between the gold electrodes. This suggests a metallic-type conduction is occurring.

In summary, two alternative structures were used to demonstrate NDR with very high current densities of up to 10^6 A/cm^2 and non-volatile, programmable conductance switching in self-assembled multilayers of the organic molecule MUA. The high-current densities that can be achieved in these devices and the very high current densities show the devices have much promise for potential application as non-volatile memory elements. Further work is necessary to understand the basic mechanism.

II. F. References:

(1) S. Hong et al, Superlatt. and Microstruct. **28**, 289 (2000)
(2) T. Ghani et al, IEDM. (2003).
(3) J.-O. Lee et al, Nano Lett. **3**, 113 (2003).
(4) N. B. Zhitenev, H. Meng, and Z. Bao, Phys. Rev. Lett. **88**, 226801 (2002).
(5) J. W. McPherson et al, IEEE Tran. Electron Dev. **50** 1771 (2003).
(6) Nitzan, A.; Ratner, M. *Science* **2003** *300* 1384.
(7) Mantooth, B. A.; Weiss, P. S. *Proc. of the IEEE* **2003** *91* 1785.
(8) Reed, M. A.; Chen, J.; Rawlett, A. M.; Price, D. W.; Tour, J. M. *App. Phys. Lett.* **2001** *78* 3735.
(9) Chao, L.; Zhang, D.; Xiaolei, L.; Song, H.; Tang, T.; Zhou, C.; Fan, W.; Koehne, J.; Han, J.; Meyyappan, M.; Rawlett, A. M.; Price, D. W.; Tour, J. M. *App. Phys. Lett.* **2003** *82* 645.
(10) Luo, Y.; Collier, C. P.; Jeppesen, J. O.; Nielsen, K. A., Delonno, E.; Ho, G.; Perkins, J.; Hsian-Rong, T.; Yamamoto, T.; Stoddart, J. F.; Heath, J. R. *ChemPhysChem* **2002** *3* 519.
(11) Xu, Q.; Gates, B. D.; Whitesides, G.M. *J. Am. Chem. Soc.* **2004** *126* 1332.
(12) Fasol, G. *Science* **1998** *280* 545.
(13) Stormer, H. L.; Baldwin, K. W.; Pfeiffer, L. N.; West, K. W. *App. Phys. Lett.* **1991** *59* 1111.
(14) Morris, R. B.; Franta, D. J.; White, H. S.; *J. Phys. Chem.* **1987** *91* 3559.
(15) Zhou, C.; Deshpande, M. R.; Reed, M. A.; Jones, L. II; Tour, J. M. *Appl. Phys. Lett.* **1997** *71* 611.
(16) Tour, J. M. *Acc. Chem. Res.* **2000** *33* 791.
(17) Evans, S. D.; Ulman, A.; Goppert-Berarducci, K. E.; Gerenser, L. J. *J. Am. Chem. Soc.* **1991** *113* 5866.
(18) Freeman, T. L.; Evans, S. D.; Ulman, A.; *Langmuir* **1995** *11* 4411.
(19) Wold, D.J.; Frisbie, C. D.; *J. Am. Chem. Soc.* **2001** *123* 5549.
(20) Holmlin, R.; Haag, R.; Chabinyc, M. L.; Ismagilov, R. F.; Cohen, A. E.; Terfort, A.; Rampi, M. A.; Whitesides, G. M. *J. Am. Chem. Soc.* **2001** *123* 5075

(21) Mbindyo, J. K. N.; Mallouk, T. E.; Mattzela, J. B.; Kratochvilova, I.; Razavi, B.; Jackson, T. N.; Mayer, T. S. *J. Am. Chem. Soc.* **2002** *124* 4020.
(22) Rampi, M. A.; Whitesides, G. M. *Chem. Phys.* **2002** *281* 373.
(23) Cui, X. D.; Zarate, X.; Tomfohr, J.; Sankey, O. F.; Primak, A.; Moore, A. L.; Moore, T. A.; Gust, D.; Harris, G.; Lindsay, S. M. *Nanotechnology* **2002** *13* 5.
(24) Wang, W.; Lee, T.; Reed, M. A. *Phys. Rev. B* **2003** *68* 035416.
(25) Salomon, A.; Cahen, D.; Lindsay, S.; Tomfohr, J.; Engelkes, V. B.; Frisbie, C. D. *Adv. Mater.* **2003** *15* 1881.
[26] C.-U. Pinnow and T. Mikoajick, J. Electrochem. Soc. **151**, K13 (2004).
[27] Z. Liu, A. Yasseri, J. S. Lindsey, and D. Bocian, Science **302,** 1543 (2003).
[28] A. Bandyopadhyay and A. J. Pal, App. Phys. Lett. **82,** 1215 (2003).
[29] J. Chen and M. A. Reed, Chem. Phys. **281**, 127 (2002).
[30] Y. Luo, C. P. Collier, J. O. Jeppesen, K. A. Nielsen, E. Delonno, G. Ho, J. Perkins, Hsian-Rong Tseng, T. Yamamoto, J. F. Stoddart, and J. R. Heath, ChemPhysChem **3**, 519 (2002).
[31] L. P. Ma, J. Liu, and Y. Yang, App. Phys. Lett. **80**, 2997 (2002).
(32) S. Möller, S. Forrest, C. Perlov, W. Jackson, and C. Taussig, J. App. Phys. **94**, 7811 (2003).
(33) L. P. Ma, Q. Xu, and Y. Yang, App. Phys. Lett. **84**, 4908 (2004).
(34) L. D. Bolzano, B. W. Kean, V. R. Deline, J. R. Salem, and J. C. Scott, App. Phys. Lett. **84**, 607 (2004).
[35] S. Gravano, E. Amr, R. D. Gould, M. Abu Samra, Thin Solid Films **433**, 321 (2003).
[36] R. E. Thurstans and D. P. Oxley, J. Phys. D **35**, 802 (2002).

III. Publications Resulting from this Project:

T. Graves-Abe, F. Pschentizka, J.C. Sturm. "Anomalous temperature dependence in solvent-enhanced dye diffusion in polymer films," Mat. Res. Soc. Symp. Proc., Vol. **725**, P3.1.1 (2002).

Troy Graves-Abe, Florian Pschenitzka, H. Z. Jin, Brent Bollman, J. C. Sturm and R. A. Register, "Solvent-enhanced dye diffusion in polymer thin films for polymer light-emitting diode application" Journal of Applied Physics **95**, pp. 7154-7163 (2004).

Troy Graves-Abe, Zhenan Bao, and J.C. Sturm, "Self-aligned, insulating-l structure for integrated fabrication of organic self-assembled multilayer electronic devices" Nano Letters **4**, pp. 2489-2492 (2004).

Troy Graves-Abe and J.C. Sturm, "Non-volatile Memory with High Current Densities in Organic Thin Films" manuscript in preparation, 2005

T. Graves-Abe and J.C. Sturm, "Molecular organic films with Negative Differential Resistance with record current densities," to be presented, Mat. Res. Soc, April, 2005.

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V. Inventions and Patent Disclosures/Filings

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2. 04-2138-1, 60/581.132