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Frequency Synthesis using MEMS Piezoelectric Resonators

by

Paul Jacob Calhoun

B.S., Engineering Sciences

United States Air Force Academy, 2002

**Submitted to the Department of Aeronautics and Astronautics
in Partial Fulfillment of the Requirements for the Degree of
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ABSTRACT

This thesis explores the foundational issues in oscillator and frequency synthesizer design using an integrated MEMS piezoelectric resonator. It presents an original low phase-noise oscillator design and two frequency synthesizer designs using the emerging technology of Draper Laboratory's MEMS GHz-range resonator. The designs leverage the extremely small size and high Q of this MEMS resonator to develop integrable, energy efficient, low phase noise oscillators and frequency synthesizers. The circuits presented offer significant size and flexibility advantages over present designs, while promising exceptional performance.

First, a 1 GHz frequency oscillator design is described incorporating the longitudinal mode bar (L-Bar) resonator with a SiGe bipolar junction transistor (BJT) in a one-port reflection topology. This design choice was made to minimize circuit complexity when later employed in a frequency synthesizer with a broadband array of switched resonators. Harmonic frequency matching is considered in a trade study between phase noise, efficiency, and circuit complexity. Performance was further enhanced using a novel approach for selecting the target static negative impedance looking into the transistor. This method modifies the transistor base current and matching networks in a manner that allows simultaneous optimization of phase noise and efficiency. The resulting oscillator has size and predicted performance characteristics that are unachievable using present technology.

Second, the matching networks from the 1 GHz oscillator are altered to allow for oscillation over a frequency range selected by an array of switched resonators. The resulting frequency synthesizer is designed to operate in the range of 200 MHz to 1 GHz. Ultimately, this thesis presents two approaches to frequency synthesizer design. The first uses frequency windows of approximately 200 MHz. The 800 MHz to 1 GHz matching network is presented in detail along with predicted performance capabilities across this frequency range. The second design implements matching networks with variable capacitors and a variable load impedance. CAD performance simulations validate the broadband switched array design concept, and represent a first step towards realizing a new, commercially viable RF MEMS oscillator and switched array frequency synthesizer.

The views expressed in this article are those of the author and do not reflect the official policy or position of the United States Air Force, Department of Defense, or the U.S. Government.

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Title: Principal Member Technical Staff

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1 May 2004

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Publication of this thesis does not constitute approval by Draper or the sponsoring agency of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas

_____

Paul Jacob Calhoun

Assignment

Draper Laboratory Report Number CSDL-T-1485.

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Paul Calhoun **6 May 2004**

Contents

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Chapter 1

Introduction

1.1 Introduction

Clocked synchronous circuits and waveform generation circuits rely on a periodic signal, which is generated by an oscillator or frequency synthesizer. These circuits are needed in transmission and reception for wireless communications, radar, and signal processing. There is currently a demand for small, energy efficient, low phase noise oscillators and frequency synthesizers that provide the same tuning range, tuning speed, and frequency resolution as current larger models. These would be used in wireless communications, local area networks, radio frequency identification tags, and small portable encryption enabled devices for civilian or military use. Due to its small size and high quality factor, the MEMS RF Longitudinal mode Bar (L-Bar) resonator currently under development at Draper Laboratory will enable an oscillator design which meets this demand in the next few years. This thesis presents a low phase-noise oscillator design using this emerging technology. This design leverages the extremely small size and high Q of this MEMS resonator to develop an integrable, energy efficient, low phase noise oscillator. The circuit presented offers significant size advantages, while promising exceptional performance. Based on this oscillator design two frequency synthesizer designs using a switched array of L-Bar resonators are also presented.

1.2 Thesis Objectives

The objective of this thesis is to examine the feasibility of oscillator and frequency synthesizer designs using L-Bar resonators. The L-Bar resonator introduces unique challenges due to its relatively high impedance at resonance, and therefore new design methods are required to develop a feasible oscillator. These challenges are worth addressing, because designs using the L-Bar resonator have the potential for combinations of performance characteristics that present day resonators are unable to achieve. Present day resonators are limited by their frequency range, size, quality factor, and their ability to be integrated on a silicon chip. Design rules of thumb developed using present day resonators need to be reevaluated based on the specific characteristics of the L-Bar resonator. The thesis demonstrates an optimized oscillator design using the L-Bar resonator to show that such a design is possible. Several novel methods of performance optimization were used in this oscillator design. The final design's performanc is compared with present oscillators. Its strong relative performance encourages future work using this resonator in oscillator applications.

The L-Bar resonator also offers the potential to pursue revolutionary frequency synthesizer concepts by using wide range switchable arrays due to its small size and integratability. At each selected frequency, the frequency synthesizer behaves like an oscillator, and thus the frequency synthesizer design is a direct descendent of the oscillator design. The thesis develops logic which leads to novel frequency synthesizer design options and compares their potential performance.

1.3 Chapter Summary

The thesis is organized as follows: In the second chapter, present oscillator designs and historical progress are discussed. In the third chapter, the piezoelectric longitudinal mode bar resonator (L-Bar) is described. The theoretical basis for the circuit model used in this oscillator design is presented. The fourth chapter describes a 1GHz frequency oscillator design incorporating the L-Bar resonator with a SiGe Bipolar Junction Transistor (BJT) in a one-port reflection topology. This topology minimizes circuit complexity when employed in a frequency synthesizer with an array of switched resonators. Higher

harmonic frequency matching is considered in a trade study between phase noise, efficiency, and circuit complexity. Performance was further enhanced using a novel approach for selecting the target static negative impedance looking into the transistor. This method modifies the transistor base current and matching networks in a manner which allows simultaneous optimization of phase noise and efficiency.

After an optimal single frequency design was simulated, the matching networks were altered to allow for oscillation over an array of switched resonators. The frequency synthesizer is designed to operate in the range of 200 MHz to 1 GHz. The fifth chapter presents two approaches to frequency synthesizer design. The first uses frequency windows of approximately 200 MHz. The 800 MHz to 1 GHz matching network is presented in detail along with predicted performance capabilities across this frequency range. A wide range of frequencies can be produced using minimal circuitry, while preserving the highest possible phase noise performance and efficiency. The performance impact of increasing frequency flexibility is demonstrated. The second design implements matching networks with variable capacitors and a variable load impedance. At the cost of added complexity, the variable components allow for better matching at each selected frequency, and thus superior phase noise and efficiency.

This thesis explores the foundational issues in oscillator and frequency synthesizer design using an integrated MEMS piezoelectric resonator. CAD performance simulations validate the broadband switched array design concept and represent a tangible first step towards realizing a new commercially viable RF MEMS switched array frequency synthesizer.

Chapter 2
Background

2.1 Oscillator Purpose

The oscillator is an essential part of any communication system. It is responsible for establishing a channel frequency, or accomplishing timing and synchronization in a digital circuit. Traditional radio systems employ channels for transmission, and the frequencies for the transmitter and the receiver are almost always determined by stable oscillators. Any phase noise on the oscillators, either in the receiver or transmitter, requires that the frequency spacing be increased to limit the susceptibility to adjacent channel interference. In this way, phase noise is directly related to the required bandwidth for a transmission. In a digital system, oscillator phase noise superimposes additional timing jitter that degrades the error rate of the received signal. Because many modern digital signal processing systems use phase modulation to separate bits of information, phase noise also decreases the amount of information that can be sent simultaneously through the same signal. Thus, phase noise limits the achievable efficiency of spectrum use and degrades the error rate in practical applications [1].

An ideal oscillator would produce a pure sinusoidal fundamental frequency that has no phase noise and no frequency drift. If the components in the oscillator are perfectly stable, the oscillator will have no frequency drift, but will still have phase noise. Phase noise is a fundamentally inescapable product of the processes inherent to oscillation, but can be limited through the use of high Q resonators and certain design considerations [1].

2.2 Oscillator Components

Oscillators consist of three fundamental components: a resonant circuit that sets the fundamental frequency, a nonlinear active device to control the output amplitude, and an impedance matching network that provides signal feedback to satisfy the conditions of oscillation. In addition, some form of DC power is required to overcome internal losses and deliver a useful output signal. Typically, the resonant circuit consists of simple LC or transmission line resonators, dielectric resonators, or acoustic resonators such as quartz crystals, or MEMS acoustic devices. Usually the nonlinear device is a diode, op-amp, or transistor. In higher frequency ranges, transistors are used almost exclusively and the oscillator can be further characterized by indicating which port of the transistor is attached to the resonant circuit [2].

2.3 History

Since the development of the Warner quartz resonator in 1952, high performance oscillator designs have historically been dominated by oscillators using quartz crystal resonators [3]. These resonators have been used in a wide range of applications including communications circuits, radio tuners, timing elements, and oscillators. Physically these resonators are carefully cut pieces of quartz crystal that can be excited by attached electrodes. These electrodes are contained within mounting supports that isolate the crystal, and provide an interface for connection to external leads. When excited with a current, the piezoelectric material responds mechanically and electrically. The resulting resonant response exhibits high Q and excellent stability. When used properly, crystal resonators provide electrical and stability characteristics that are unattainable using conventional capacitors, inductors, and resistors.

The Butterworth-Van-Dyke (BVD) model shown in Figure 2.3.1 is a common lumped element circuit model used to characterize the resonator behavior in terms of common electrical components. Within this model, C_p is the static capacitance. This is the capacitance related to the crystal and the electrodes themselves acting as a single large capacitor independent of the vibratory motion of the crystal. The R_o, L_o, C_o portion of the circuit is called the motional arm of the circuit, and arises from the mechanical crystal

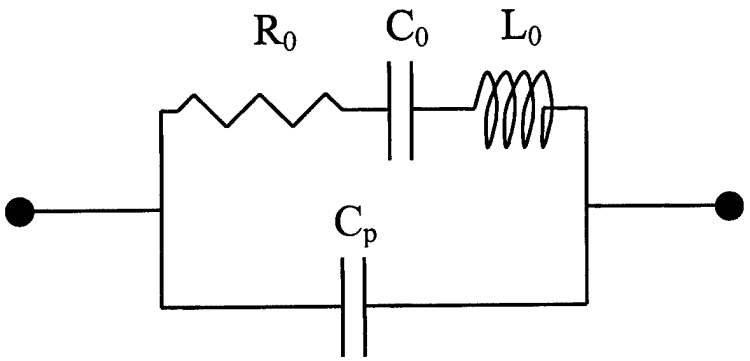


Figure 2.3.1: BVD model of a crystal resonator

vibrations. At frequencies far from the natural mechanical resonance frequency, the resonator has a very high impedance. In most circuits, this impedance value is high enough to simulate an open circuit. In contrast, at values very close to the mechanical resonance frequency, the resonator has a low resistance.

Figure 2.3.2 shows a typical crystal resonator response with a resonant frequency at 200 MHz. The sharp discontinuity seen in Figure 2.3.2 at the resonance frequency is due to the high circuit Q, and illustrates the primary benefit of using crystal resonators. A very small change in frequency in the resonance region has a large effect on the circuit impedance. This means the circuit is very sensitive to small changes in frequency. so it can be used to effectively filter out unwanted frequencies or maintain a desired frequency as in timing circuits or oscillators.

The resonance effect is physically complex, as it deals with coupling between mechanical resonance and an electrical forcing function. However, using the equivalent circuit model shown in Figure 2.1, this interaction can be accurately modeled using a basic electrical circuit analogy. At low frequencies, the capacitors in each parallel circuit branch provide high impedance, effectively blocking almost all current flow. As the frequency increases, the motional branch of the circuit containing the capacitor and inductor in series reaches its natural resonance frequency. The series resonance occurs when the reactance of the inductor and the capacitor cancel. This results in the lowest possible resistance, R_0. The

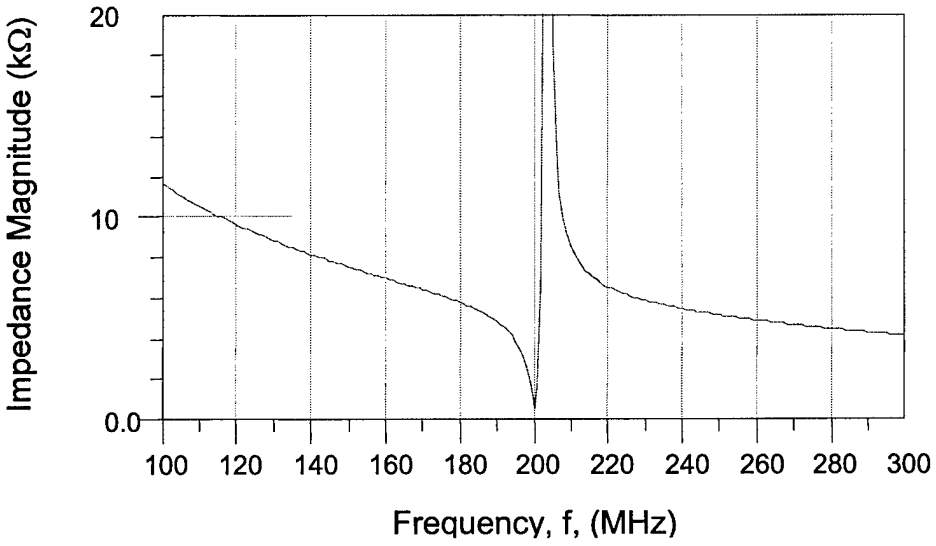


Figure 2.3.2: Resonant crystal frequency response

downward spike seen in Figure 2.2 shows the series resonance frequency. Physically, this is the natural acoustic frequency of the crystal. If the crystal were a simple device such as a metal bar, this is the frequency at which it would vibrate if struck like a bell. However, because the crystal has an electrical response to vibration as well as a physical response, it has an additional resonant response when the reactance of the motional branch of the circuit is equal to the reactance provided by the static capacitance. Typically this parallel resonance occurs at a slightly higher frequency than the series resonance. At this frequency, the resonant circuit has high impedance, as seen by the upward spike in Figure 2.2.

While crystal resonators have been successfully used in many applications, the physical characteristics and configurations of present resonators have limitations that make them unsuitable for very high frequencies. The most important considerations in choosing a circuit resonator are frequency accuracy, quality factor (Q), stability, and range. Crystal resonators have shown steadily improving accuracy and stability, but are physically limited in their applicable frequency range. As technology pushes into higher and higher frequency ranges corresponding to faster data transfer rates, crystal resonators are not suitable. The highest frequency conventional crystal resonators operate at around 200 MHz. This limit is

imposed by the natural resonance frequency of the crystals, and cannot be overcome without a fundamental technological change. There is currently much demand for high Q, accurate, stable resonators in the 200 MHz-5 GHz range that offer the same small size and high fidelity benefits of conventional crystal resonators. Such applications currently use resonant chambers or dielectric resonators, which are relatively large at the lower band of this frequency range. Some non-crystal acoustic resonant components are under development that would meet the high frequency demands of modern circuits with performance characteristics comparable to conventional crystal resonators. These include Thin Film Resonators (TFRs), Surface Acoustic Wave (SAW) resonators, and the Draper L-Bar resonator [4].

Early quartz crystal oscillators were fraught with technical difficulties due to integration challenges. The 1957 Western Electric GS-60157 is a good example of competitive designs before the widespread use of transistors. This device used vacuum tubes and a Warner designed quartz resonator to produce an output frequency of 2.5 MHz. The oscillator unit weighed 23 kg with a volume of 75,180 cm^3. It required 50 W of DC power [3].

As transistors became commercially available they were incorporated into quartz crystal designs. The first all transistor oscillator was the 1958 Sulzer oscillator. This oscillator had a mass of more than 3 kg and a volume of 5162 cm^3 [3]. This is still enormous by present standards, but represents a revolutionary order of magnitude improvement over other contemporary designs by increasing the level of integration. The JHU/APL type 150 crystal oscillator developed in 1996 has a mass of 0.2 kg and a volume of 142 cm^3 [3]. As quartz crystal oscillators become smaller and smaller, they run into the fundamental limit imposed by the size of the quartz crystal and its related off-chip circuitry. Finding a high Q resonator that can be directly integrated should lead to order of magnitude improvements over present designs. The Draper L-Bar resonator can be directly integrated, and thus has the potential to create a new class of oscillators with significant size and power savings.

Table 2.4.1: Comparison of current oscillator specifications

Oscillator	Frequency Range	Phase Noise @10 KHz (dBc/Hz)	Input Power max (W)	Output Power (dBm)	output Power (W)	efficiency
MITEQ	0.8-3.2 GHz	-130	5	13	0.019953	0.40%
General Microwave VCO	2-4 GHz	-95	2.25	10	0.01	0.44%
Huang Integrated Colpitts [5]	925 MHz	-112.7	0.00468	-15.5	2.82E-05	0.60%
Modco LV122	400-800 MHz	-94	0.075	5	0.003162	4.22%
Modco FL1630	500-1000 MHz	-94	0.15	5	0.003162	2.11%
Modco LV155	900-1000 MHZ	-90	0.075	7	0.005012	6.68%
Modco LN139	950-980 MHz	-100	0.06	2	0.001585	2.64%
Sirenza VCO 790-600T	1 GHz- 2 GHz	-100	0.3	7	0.005012	1.67%
Sirenza VCO 793-750T	500 MHz-1GHz	-104	0.3	6	0.003981	1.33%
Sirenza VCO 191-1013U	996-1031 MHZ	-106	0.018	-3	0.000501	2.78%
Draper Oscillator	1 GHz	-158.2	0.0285	11.76	0.0150	52.61%
Draper Window Synthesizer mod 1	200 MHz-1 GHz	-130	0.0220	10.00	0.0100	45.45%
Draper Window Synthesizer mod 2	200-MHz-1GHz	-158.5	0.0385	11.14	0.0130	33.77%
Draper Variable Synthesizer	200 MHz-1 GHz	-161.5	0.0356	11.58	0.0144	40.45%

2.4 Current State of the Art Oscillator Performance

There are many commercially available oscillators in the 200 MHz to 1 GHz frequency range. Table 2.4.1 presents a representative sample of some of these oscillators including their frequency range and performance. The oscillators in this table are Voltage Controlled Oscillators (VCOs), which would be used in a phase locked loop within a frequency synthesizer. The oscillators listed are typically prepackaged and have a size of just under 15 cm^3. The simulated performances of the proposed Draper piezoelectric MEMS oscillator and frequency synthesizer are also presented. The proposed Draper design offers significant potential increases in efficiency and phase noise.

Chapter 3

Draper L-Bar MEMS Resonator

3.1 Resonator Structure

The L-Bar MEMS resonator is a piezoelectric device which can be fabricated directly onto an integrated circuit substrate. The device structure resembles a suspended capacitor shaped like a rectangular bar. The active area consists of a bottom metal electrode, a piezoelectric dielectric, and a top metal electrode. When a field is applied between the bar electrodes (through the thickness of the bar), the device stretches. The bar length, width, and thickness define three fundamental longitudinal stretching modes. These are purposely set far apart in frequency so only one mode appears in the band of interest. In initial designs, the length is the frequency-defining dimension, and both bar width and thickness correspond to much higher frequencies. When a field is applied at the dominant mechanical resonance frequency, the device impedance drops to well below its nominal capacitive impedance.

Devices from the first round of fabrication are shown in Figure 3.1.1. The piezoelectric material used is aluminum nitride (AlN). Typical features for a device with resonant frequencies over the range of 50 MHz to 2 GHz are: thickness of AlN = 0.5 μm, bar length 3-30 μm and width 1-10 μm.

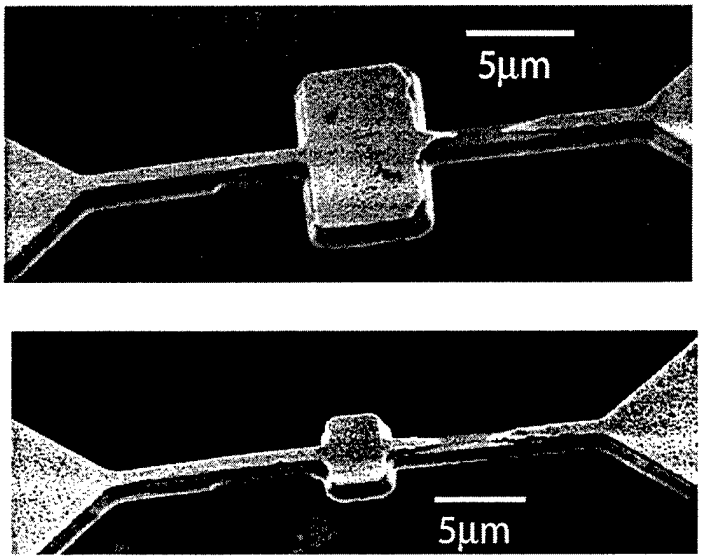


Figure 3.1.1 Scanning-electron micrographs of released resonator structures. TOP: 10 μm long x 6 μm wide resonator. BOTTOM. : 5 μm long x 3 μm wide resonator. Tethers are approximately 1 μm wide for both devices.

3.2 Resonator Model

Figure 3.2.1 shows a sketch of the resonant bar. The intended operating mode is a resonant stretching of the length along the x-axis. The motion will be actuated through an electric field applied parallel to the z-axis, however, and so will rely on a non-zero e_{31} coefficient in the piezoelectric coupling matrix. Analytical models have been developed to determine an equivalent circuit for the idealized device and connect circuit parameters to device dimensions and material properties.[1] The variables used in the analysis are

T_{ij} = stress tensor

S_{ij} = strain tensor

E_k = electric field vector

[1] The following analysis first completed by Dr. Amy Duwel and is summarized here with her permission.

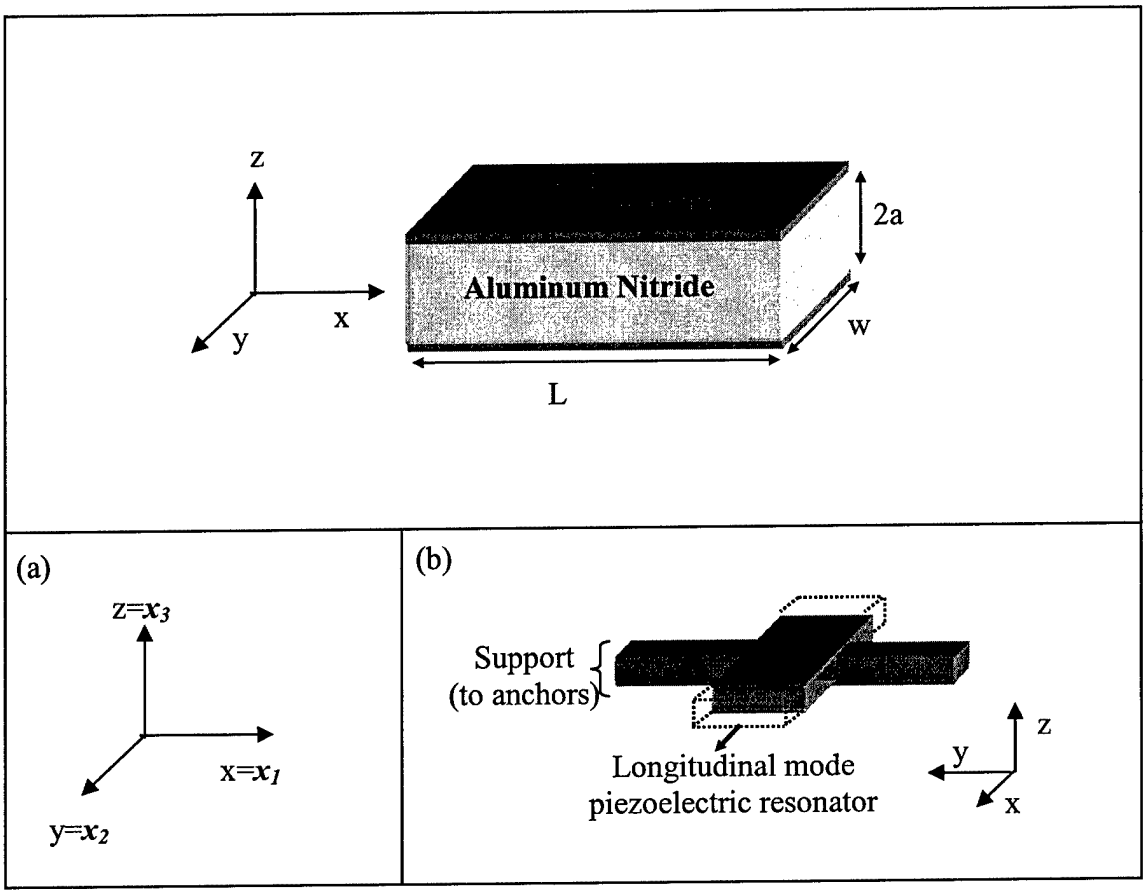


Figure 3.2.1: Resonator bar geometry and dimensions used for analysis. The two insets show (a) additional variables used for identifying directions, and (b) the device with supports, as well as the intended mode of operation.

D_k = polarization charge vector

u_k = displacement vector

ϕ = scalar electric potential

Reduced tensor notation will be applied, so that

$T_{ij} \rightarrow T_k$ = a vector with six elements

$$T_1 = T_{11}; \quad T_2 = T_{22}; \quad T_3 = T_{33};$$
$$T_4 = T_{23} = T_{32}; \quad T_5 = T_{13} = T_{31}; \quad T_6 = T_{12} = T_{21};$$

$S_{ij} \rightarrow S_k$ = a vector with six elements

$$S_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\right)$$

$$S_1 = S_{11}; \quad S_2 = S_{22}; \quad S_3 = S_{33};$$
$$S_4 = 2S_{23} = 2S_{32}; \quad S_5 = 2S_{13} = 2S_{31}; \quad S_6 = 2S_{12} = 2S_{21};$$

Also, electrostatic fields will be assumed, giving

$$E_1 = \frac{-\partial\phi}{\partial x_1}; \quad E_2 = \frac{-\partial\phi}{\partial x_2}; \quad E_3 = \frac{-\partial\phi}{\partial x_3} \tag{3.2.1}$$

Then the natural constitutive lasws are

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} = \underbrace{\begin{bmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ c_{21} & c_{22} & c_{23} & 0 & 0 & 0 \\ c_{31} & c_{32} & c_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{66} \end{bmatrix}}_{\mathbf{c} = \text{ stiffness matrix: } N/m^2} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} - \underbrace{\begin{bmatrix} 0 & 0 & e_{31} \\ 0 & 0 & e_{32} \\ 0 & 0 & e_{33} \\ 0 & e_{24} & 0 \\ e_{15} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{\mathbf{e}^T = \text{piezoelectric coupling: } C/m^2} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{3.2.2}$$

and

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{24} & 0 & 0 \\ e_{31} & e_{32} & e_{33} & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{e} = \text{piezoelectric coupling: } C/m^2} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} + \underbrace{\begin{bmatrix} \varepsilon_{11} & 0 & 0 \\ 0 & \varepsilon_{22} & 0 \\ 0 & 0 & \varepsilon_{33} \end{bmatrix}}_{\boldsymbol{\varepsilon} = \text{dielectric constants: } F/m} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{3.2.3}$$

The values for the nonzero entries in the stiffness, piezoelectric, and dielectric matrices are given in Appendix A.

Mechanical force balance requires that

$$\begin{bmatrix} \rho\ddot{u}_1 \\ \rho\ddot{u}_2 \\ \rho\ddot{u}_3 \end{bmatrix} = \begin{bmatrix} \frac{\partial}{\partial x_1} & 0 & 0 & 0 & \frac{\partial}{\partial x_3} & \frac{\partial}{\partial x_2} \\ 0 & \frac{\partial}{\partial x_2} & 0 & \frac{\partial}{\partial x_3} & 0 & \frac{\partial}{\partial x_1} \\ 0 & 0 & \frac{\partial}{\partial x_3} & \frac{\partial}{\partial x_2} & \frac{\partial}{\partial x_1} & 0 \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} \tag{3.2.4}$$

Equation (3.2.4), with substitutions for displacement and potential, then becomes

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ c_{21} & c_{22} & c_{23} & 0 & 0 & 0 \\ c_{31} & c_{32} & c_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{66} \end{bmatrix} \begin{bmatrix} u_{1,1} \\ u_{2,2} \\ u_{3,3} \\ u_{2,3}+u_{3,2} \\ u_{1,3}+u_{3,1} \\ u_{1,2}+u_{2,1} \end{bmatrix} + \begin{bmatrix} 0 & 0 & e_{31} \\ 0 & 0 & e_{32} \\ 0 & 0 & e_{33} \\ 0 & e_{24} & 0 \\ e_{15} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \phi_{,1} \\ \phi_{,2} \\ \phi_{,3} \end{bmatrix} \tag{3.2.5}$$

The notation uses a comma followed by subscripts to mean derivatives with respect to that spatial coordinate. This can be simplified through a series of approximations. First, assume that for a longitudinal mode vibration in the x-direction, there is no y-dependence, so u_2 and all its derivatives are set equal to zero. Next, the stress in the z direction and the x-z shear stress are zero for all z for the lowest order longitudinal mode. Thus T_3 and T_5 =0. Third, the inertia in the z direction is considered negligible. This gives the acoustic wave equation for longitudinal modes in the x-direction, which is coupled to the electrostatic potential given by

$$\rho\ddot{u}_1 = u_{1,11}\left[c_{11} - \frac{c_{13}^2}{c_{33}}\right] + \phi_{,31}\left[+e_{31} - \frac{c_{13}e_{33}}{c_{33}}\right] \tag{3.2.6}$$

Since AlN is non-conductingm and thus has a free charge density of 0, combining Maxwell's equation and the independence of x_2, we have

$$\nabla \cdot D = 0 = \frac{\partial D_1}{\partial x_1} + \frac{\partial D_3}{\partial x_3} \tag{3.2.7}$$

When combined with (3.2.6) this yields

$$\phi_{,11}\left[\varepsilon_{11}+\frac{e_{15}^2}{c_{55}}\right]+\phi_{,33}\left[\varepsilon_{33}+\frac{e_{33}^2}{c_{33}}\right]=u_{1,31}\left[-\frac{e_{15}}{c_{55}}+-\frac{e_{33}c_{31}}{c_{33}}+e_{15}+e_{31}\right] \tag{3.2.8}$$

The coupled system is described by (3.2.6) and (3.2.8) which are difficult to solve because of the *x*-*z* coupling. Since the equations are linear, break the electrostatic potential into two parts and let

$$\phi=\phi^{BC}+\phi^{u} \tag{3.2.9}$$

where if $\varepsilon_x=\varepsilon_y=\varepsilon_z$, ϕ^{BC} solves

$$\varepsilon_z\nabla^2\phi^{BC}=0 \tag{3.2.10}$$

with voltage biased boundaries, and ϕ^{u} solves

$$\varepsilon_z\nabla^2\phi^{u}=u_{1,31}\left[\frac{e_{15}}{c_{55}}+\frac{e_{33}c_{31}}{c_{33}}-e_{15}-e_{31}\right] \tag{3.2.11}$$

with $\phi^{u}=0$ on the boundaries.

If the coefficients on the left hand side of (3.2.8) are approximately equal, and set to ε_z, then equation (3.2.8) is solved by the sum of ϕ^{u} and ϕ^{BC} as they have been defined. When the beam is much longer than it is thick, the potential can be approximated by

$$\phi(x,z)=f(x)\frac{z}{2a}. \tag{3.2.12}$$

Mechanical Resonance

The mechanical wave equation to solve is

$$\rho\ddot{u}_1-u_{1,11}\left[c_{11}-\frac{c_{13}^2}{c_{33}}\right]=\phi_{,31}\left[-e_{31}+\frac{c_{13}e_{33}}{c_{33}}\right] \tag{3.2.13}$$

We define the intermediate variables

$$c=c_{11}-\frac{c_{13}^2}{c_{33}} \tag{3.2.14}$$

$$e = e_{31} - e_{33}\frac{c_{13}}{c_{33}} \tag{3.2.15}$$

$$\varepsilon_z = \varepsilon_{33} + \frac{e_{33}^2}{c_{33}} \tag{3.2.16}$$

$$\omega_n = \frac{n\pi}{L}\sqrt{\frac{c}{\rho}} \tag{3.2.17}$$

$$\beta_n = \frac{\omega_n}{Q} \tag{3.2.18}$$

The wave solution is

$$u_1(x,s) = \frac{2e}{a\rho L}\cos\left(\frac{\pi x}{L}\right)\frac{V(s)}{s^2 + s\beta_n + \omega_n^2} \tag{3.2.19}$$

and the current is

$$I = -\frac{4we^2}{a\rho L}\frac{sV(s)}{s^2 + s\beta_n + \omega_n^2} + \frac{\varepsilon_z wL}{2a}sV(s) \tag{3.2.20}$$

Equivalent Circuit

The impedance of the bar, as defined by equation (3.2.20), looks similar to an RLC circuit in parallel with a single capacitor. The equivalent parallel capacitance is simply

$$C_p = \frac{\varepsilon_z wL}{2a} \tag{3.2.21}$$

To find the equivalent RLC circuit, consider the transfer function of a series RLC, which is

$$Z = sL_o + R_o + \frac{1}{sC_o} = \frac{s^2 L_o C_o + sR_o C_o + 1}{sC_o} \tag{3.2.22}$$

To match up with (3.2.20), we rearrange

$$Z^{-1} = \frac{s/L_o}{s^2 + s(R_o/L_o) + 1/(L_o C_o)} \tag{3.2.23}$$

Comparing this to the terms in (3.2.20), we identify from the familiar BVD circuit shown in Figure 2.1

$$C_p = \frac{\varepsilon_z wL}{2a} \qquad L_o = \frac{a\rho L}{4we^2} \quad C_o = \frac{4we^2 L}{ac\pi^2} \qquad R_o = \frac{\pi}{Q}\sqrt{c\rho}\frac{a}{4we^2} \qquad (3.2.24)$$

The material parameters for Aluminum Nitride are given in Appendix 1. The modal Q is calculated from known damping mechanisms. However, if the goal of $Q = 10^4$ is reached, and the following dimensions are used

$w = 3.0\ \mu m$

$L = 4.83\ \mu m$

$2a = 0.5\ \mu m$

the equivalent circuit parameters become

$\frac{\omega_1}{2\pi} = 1$ GHz

$C_p = 2.62$ fF

$L_o = 3.01 \cdot 10^{-4}$ H $\qquad R_o = 189\ \Omega \qquad C_o = 0.0842$ fF

Piezoelectric finite elements models in ANSYS[2] were also used to simulate the device impedance as a function of frequency and support the use of a BVD circuit, for even more complicated geometries (including metal electrodes, finite tether widths, etc).

3.3 Advantages of the L-Bar Resonator for Oscillator implementation

Key advantages of the L-Bar design include: (1) the device frequency is set lithographically and is inversely proportional to length; (2) the device footprint is extremely small, ranging from approximately 25 μm x 15 μm to 3 μm x 10 μm over the range of frequencies; (3) arrays of devices with frequencies from 0.05-2 GHz can be fabricated on a single chip; (4) the device impedance can be scaled to the range of several hundred ohms, compatible with RF integrated circuit requirements; (5) the device

[2] ANSYS is a finite element analysis program produced by ANSYS, inc., which is capable of modeling piezoelectric elements.

fabrication is a self-aligned process designed to produce high dimensional precision even at submicron feature sizes, and (6) the device can be integrated directly onto an RFIC.

Data from the first fabricated devices [6] also verify the well-isolated longitudinal modes and the wide scalability of resonant frequencies on a single chip. Quality factors of these first devices were in the range of 100-600, well below the targeted 10^4. This device parameter affects both impedance and frequency selectivity. Thus, ongoing work on the device fabrication and design focuses on this performance parameter.

In designing the MEMS-based oscillator and frequency synthesizer, we use the equivalent circuit BVD circuit in Figure 2.1 to model the L-Bar. We assume the targeted Q of 10^4, and typical dimensions of approximately 5 μm x 3 μm. As additional data becomes available for the MEMS devices, the equivalent circuit parameter values may be refined. For this thesis, we use these ideal values to develop a logic for the oscillator and frequency synthesizer designs, as well as specific designs that can be used to set requirements on the MEMS device itself.

Chapter 4

Low Phase Noise, Low Power Oscillator Design

4.1 Oscillator Theory

In order for oscillation to occur in a circuit, current must build at a desired frequency due to feedback, while currents at other frequency are strongly attenuated. One design method for creating such circuits is using the technique of negative resistance. In this approach, the impedances of the oscillator components are modified to create conditions that lead to steady state oscillation at a desired frequency. This method is well represented in the literature and provides relatively simple intuitive relationships between the component impedances that motivate design choices.

Looking at Figure 4.1.1, the active portion of the circuit which in this case is the transistor and its matching networks has real and imaginary impedances shown by R_A and X_A respectively. Similarly the resonant load has real and imaginary impedances shown by R_L and X_L respectively. Using the method of negative resistance, for oscillation to occur,

$$R_A(I)+R_L = 0 \tag{4.1.1}$$

$$X_A(I)+X_L = 0 \tag{4.1.2}$$

must be satisfied at steady state [7]. Since R_L is a passive resistance and therefore positive, R_A must be a negative value. In order for oscillation to build from an initial static condition with no current flowing, the magnitude $R_{A(I=0)}$ must be greater than R_L. Due to the nonlinearity of the active device, R_A becomes less negative as current builds in the circuit reaching a value equal to R_L at the desired current level for steady state oscillation. In

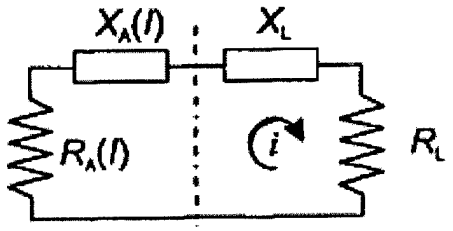


Figure 4.1.1 Oscillation parameters

practice, to ensure oscillation start up, the zero current impedance for $R_A(I=0)$ should be approximately $3R_L$ [7].

Maximum energy transfer at the fundamental frequency occurs across a load impedance seen by the resonator through the matching networks which is equal to the impedance of the resonator itself. Simultaneously, the reflection coefficient *S11* must be greater than one, which constrains the possible values for the load impedance. Another related constraint is introduced by the static negative impedance or R_A required for oscillation start up. Efficiency is a measure of how effectively the device converts DC input power into oscillatory output power at the fundamental frequency. The first step in maximizing efficiency is matching the resonator and load impedances as closely as possible, subject to the constraints introduced by the oscillation conditions.

The circuit load can be presented to the circuit at either the transistor collector or emitter equally effectively. It was decided to present the circuit load to the oscillator at the transistor collector to simplify the circuit layout. The DC input power must be presented at the collector to provide the correct transistor biases. By taking the output at the collector as well, the input and the output of the oscillator can be attached to an external circuit through a single port. Optimizations were performed based on the resonator impedance at 189 Ω, therefore an additional impedance matching network will be necessary to present a load impedance to the rest of the circuit at the standard 50 Ω. At this stage, it is assumed that this network will be built, but that it is outside the scope of the oscillator itself. Instead, this network is an interface issue based on the specific needs of any given application

4.2 Transistor Selection

An important design choice for the oscillator is selecting an appropriate transistor. Important factors in this decision were noise performance, frequency range, commercial

availability, and performance similar to integrated circuit transistors. For demonstration purposes the oscillator will use a discrete transistor. Ultimately, however, an ultra wide range frequency synthesizer built based on the proof of concept shown through the oscillator design would use an integrated circuit transistor to maximize the size advantages of the Draper resonator. With these criteria in mind, the NEC NPN SiGe High Frequency transistor NESG2030M04 was selected. This transistor has a transition frequency of up to 60 GHz, making it practical in applications from 100 MHz to 10 GHz. It is optimized for low voltage/low current performance, has high maximum stable gain, and a low noise figure. The transistor packaging is optimized for RF applications.

To apply the design tools developed using Agilent's Advanced Design System program using a generic transistor, the nonlinear transistor model from the NEC specifications data was implemented in ADS. Table 4.2.1 shows the manufacturer provided Gummel-Poon non-linear transistor model parameters used to model the transistor performance. Figure 4.2.1 shows the circuit used to model the parasitics associated with the transistor and its package. After imputing this circuit model with the listed parameters, the simulated results in ADS are within 1% of the production values reported by NEC.

Table 4.2.1: Gummel-Poon parameters for NES2030M04 bipolar junction transistor

Parameters	Q1	Parameters	Q1
IS	2.42e-13	MJC	0.16
BF	382	XCJC	1
NF	1.025	CJS	0
VAF	87	VJS	0.75
IKF	100	MJS	0
ISE	5.2e-13	FC	0.5
NE	2.806	TF	3e-12
BR	15.7	XTF	2
NR	1.02	VTF	0.1
VAR	1.307	ITF	0.001
IKR	0.037	PTF	0
ISC	9e-14	TR	50e-12
NC	2.194	EG	1.11
RE	2.2	XTB	0
RB	4	XTI	3
RBM	1	KF	120e-15
IRB	0.007	AF	1.37
RC	4.2		
CJE	0.4e-12		
VJE	0.98		
MJE	0.25		
CJC	0.12e-12		
VJC	0.63		

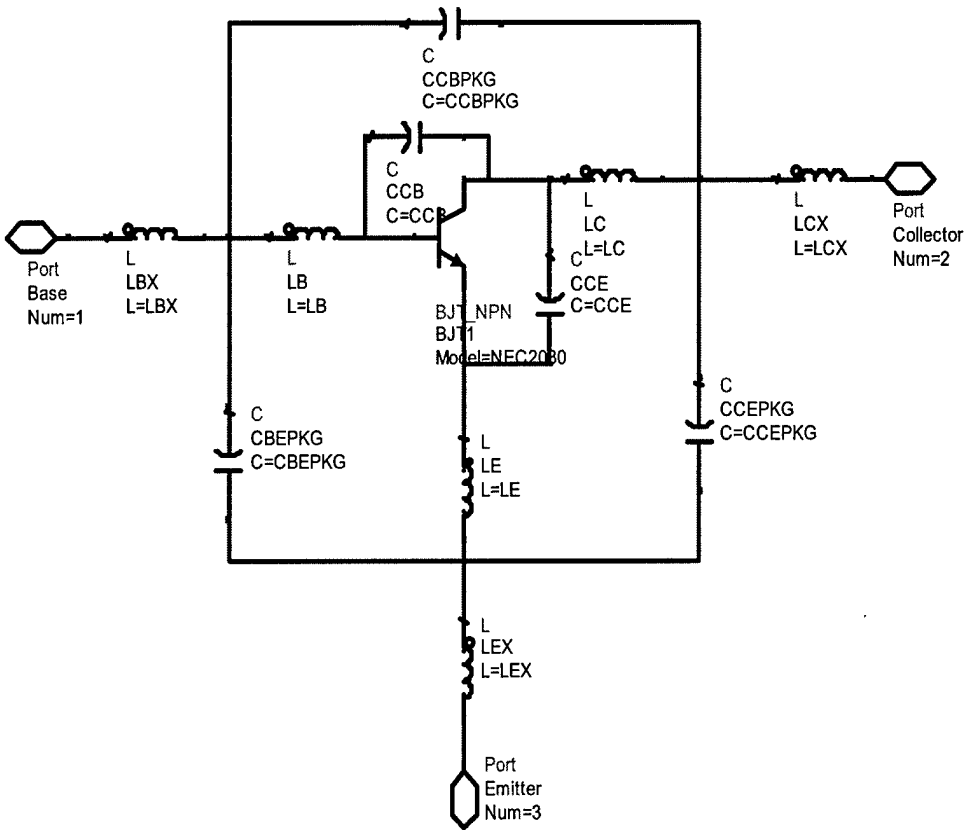


Figure 4.2.1: Transistor package parasitics circuit

Table 4.2.2: NESG2030M04 Transistor Parasitic Circuit Parameters

Parameters	Values
CCB	0.07 pF
CCE	0.05 pf
LB	0.9 nH
LC	0.5 nH
LE	0.14 nH
CCBPKG	0.001 pF
CCEPKG	0.2 pF
CBEPKG	0.1 pF
LBX	0.2 nH
LCX	0.2 nH
LEX	0.1 nH

4.3 Topology Selection

In order for oscillation to build up, the transistor must be forced into an unstable state. This means looking into the transistor from the resonator, *S11* must have a magnitude greater than unity. In the literature, it is recommended to have a *S11* magnitude of 2, which if referenced to the resonator impedance corresponds to a negative impedance looking into the oscillator that is three times the impedance of the resonator. In practice, we are actually only concerned with the real part of this impedance, since at the oscillation frequency the resonator reactance and the matching network reactance cancel.

Different orientations of the transistor are inherently more or less stable depending on the transistor in question. Analysis was done considering the NESG2030M04 transistor in either a common-base or a common-emitter topology. A common-base design places the resonant element on the transistor emitter, and grounds the transistor base through a matching network. This is shown in Figure 4.3.1. In contrast, a common-emitter design shown in Figure 4.3.2 places the resonant element on the transistor base and grounds the emitter through a matching network. In both cases the output signal is directed through the transistor collector. By comparing the DC voltages required to produce a specified real negative impedance seen by the resonator, it soon became apparent that both topologies required almost the same power to produce equivalent instability. The primary difference then between the two topologies is that the common-base setup requires the use of an inductor placed on the transistor base to create transistor instability. In contrast, the common-emitter setup relies on a capacitor and resistor in parallel to maximize instablility. Since inductors should generally be avoided when using IC technology, the common-emitter topology was chosen.

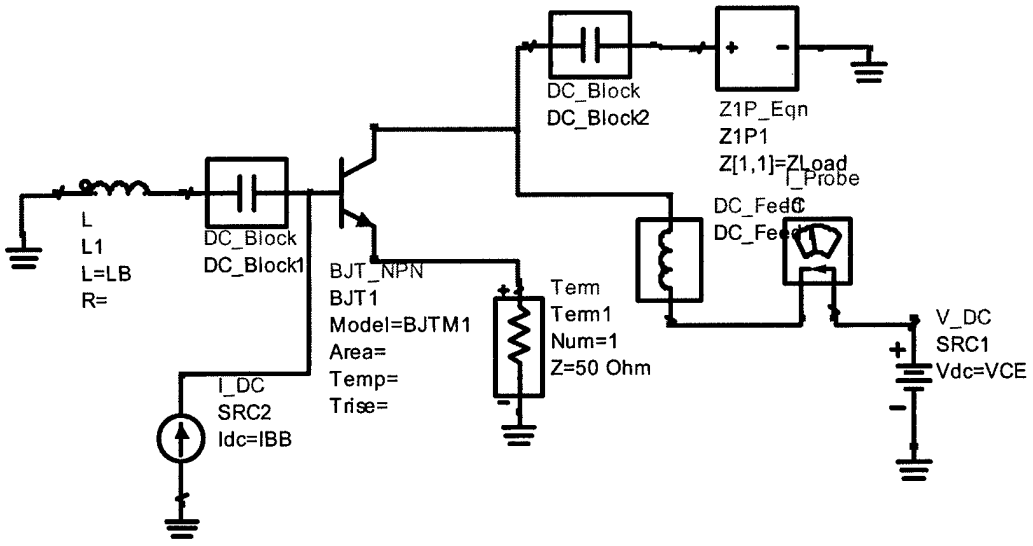


Figure 4.3.1 Typical common-base oscillator topology

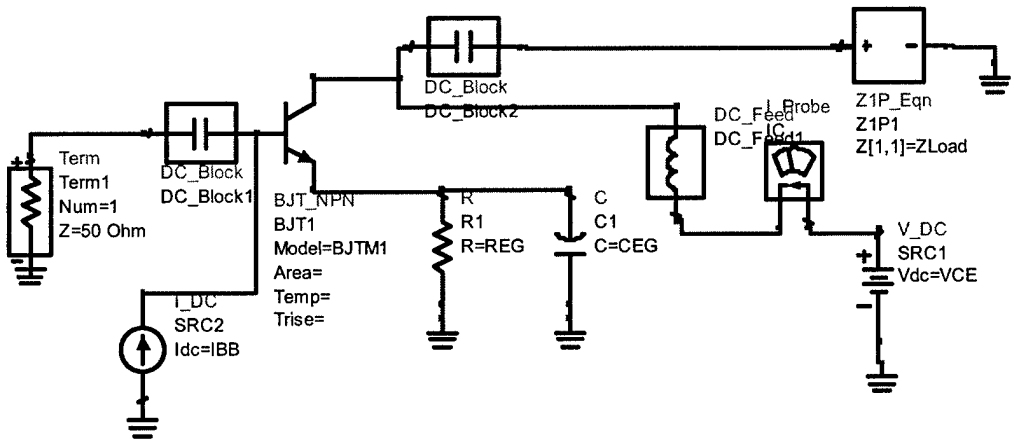


Figure 4.3.2 Typical common-emitter oscillator topology

4.4 Oscillator Efficiency

At its resonant frequency the real and imaginary parts of the 1 GHz L-Bar resonator are

$$R_{RES} = 189.97\ \Omega$$

$$X_{RES} = 138.9\ \Omega$$

Assuming no added real impedance due to the transmission lines, $R_{RES} = R_L$. Ideally we would like an oscillator with the start-up characteristics [7]

$$R_A = Z11 = 3R_L = -567\ \Omega \tag{4.4.1}$$

$$|S11| > 2 \tag{4.4.2}$$

However, a constraint analysis shows that loosening the required value of $Z11$ can significantly improve efficiency. In an ideal system, any static negative impedance with a larger magnitude than the real impedance of the resonator would suffice. Typical oscillator designs use a resonator with very low real impedance. The $3R_L$ rule of thumb stems from experience with such designs. Because the L-Bar resonator has a relatively high real impedance it is worth reconsidering this rule of thumb for this specific design. ADS simulations[3] confirmed $2R_L$ would still lead to oscillation start up as long as equation 4.4.2 is satisfied. Table 4.4.1 shows the overall efficiency benefits from loosening the negative static impedance constraint on a representative design.

The overall efficiency of the device can also be improved by tuning the higher harmonic impedances to minimize higher harmonic power output. Simulations were run in ADS that optimized the matching impedances at higher harmonic frequencies for maximum efficiency. As anticipated, maximum efficiency was achieved when the higher harmonic output power was zero.

The following data are specific to the NESG2030 transistor and a 1 GHz L-Bar resonator, but the trends are based on energy conservation within the system and are therefore universal. The optimization algorithms used set discrete impedances at each harmonic frequency. Simulations were run examining the effects of controlling the impedances at just the fundamental frequency and then also controlling the impedances at increasing numbers of higher harmonic frequencies. When a higher harmonic frequency

[3] All oscillator simulations were done using Agilent's Advanced Design System CAD software (ADS). ADS offers nonlinear noise simulation as well as optimization subroutines to model oscillator performance.

Table 4.4.1: Change in efficiency due to change in Z11

Parameter	Case 1	Case 2	Case 3
S11	1.996	2.056	2.586
Z11 (Ω)	-566.98	-450.01	-300
Efficiency	43.6%	47.3%	57.8%

was not being controlled, it was set to a nominal impedance of 50 Ω. For example, in the case with one higher harmonic, the fundamental frequency impedance at 1 GHz was optimized, the impedance at the second harmonic frequency at 2 GHz was optimized, and at all higher frequencies the networks had an impedance of 50 Ω. The increasing efficiency asymptotically approaches a maximum after matching the first three harmonics as shown in Table 4.4.2.

Efficiency can also be increased by adding a matching network on the resonator side of the transistor. Again, using the 4 higher harmonic system as an example the circuit performance with and without the matching network is listed in Table 4.4.3.
This indicates the matching network in this case can improve efficiency by about 5% without significantly affecting the phase noise.

Perhaps more importantly, adding the matching network on the resonator side of the transistor gave each resonator in a bank of resonators for the frequency synthesizer individually tunable characteristics. It was hoped that the addition of the resonator matching network would reduce or eliminate the need to tune the rest of the matching networks as different resonators are selected and the synthesizer's output frequency shifts. As is shown later in the thesis, using this matching network was not significantly beneficial when using real components, and it was eventually eliminated. Theoretically it does improve performance and allow individual tuning. Further work could be done to see if using resonator side matching networks in other configurations can further enhance overall performance.

Table 4.4.4 shows the improvement to the final design realized by adding the resonator side matching network and simultaneously relaxing the negative impedance constraint.

Table 4.4.2: Increase in efficiency due to addition of higher harmonic matching

Number of Higher Harmonics Matched	0	1	2	3	4	5
Efficiency (%)	1.9	31.6	34.7	53.9	55.0	55.0

Table 4.4.3: Change in efficiency due to resonator matching network

Parameter	Without resonator matching network	With resonator matching network
S11	1.996	2
real(*Z11*) (Ω)	-566.98	-567.02
Efficiency (%)	43.6	48
Noise (PN) (dBc/Hz)	-149.8	-147
Noise (AM) (dBc/Hz)	-146.1	-145.3

Table 4.4.4: Combination of Resonator Matching Network and relaxed Z11 constraint

Parameter	baseline	with resonator matching network	relaxed *Z11* constraint
S11	2	2	2
real(*Z11*) (Ω)	-567	-567	-368
efficiency	53.9%	54.1%	57.3%

4.5 Oscillator Phase Noise

An important performance parameter for a microwave oscillator is the level of noise. Noise can be considered to be equally split between amplitude (AM) and phase (PN) components. In practice amplitude modulation can be neglected or removed by a limiter so the key noise parameter for an oscillator is its phase noise [1]. A common but indirect way of expressing phase nose is expressed by the ratio of the single-sideband noise power (in a 1-Hz bandwidth at an offset frequency from the carrier) to the total carrier power. This is shown in Figure 4.5.1.

Leesom proposed a method of predicting phase noise based on circuit parameters. The phase noise, L is [8]

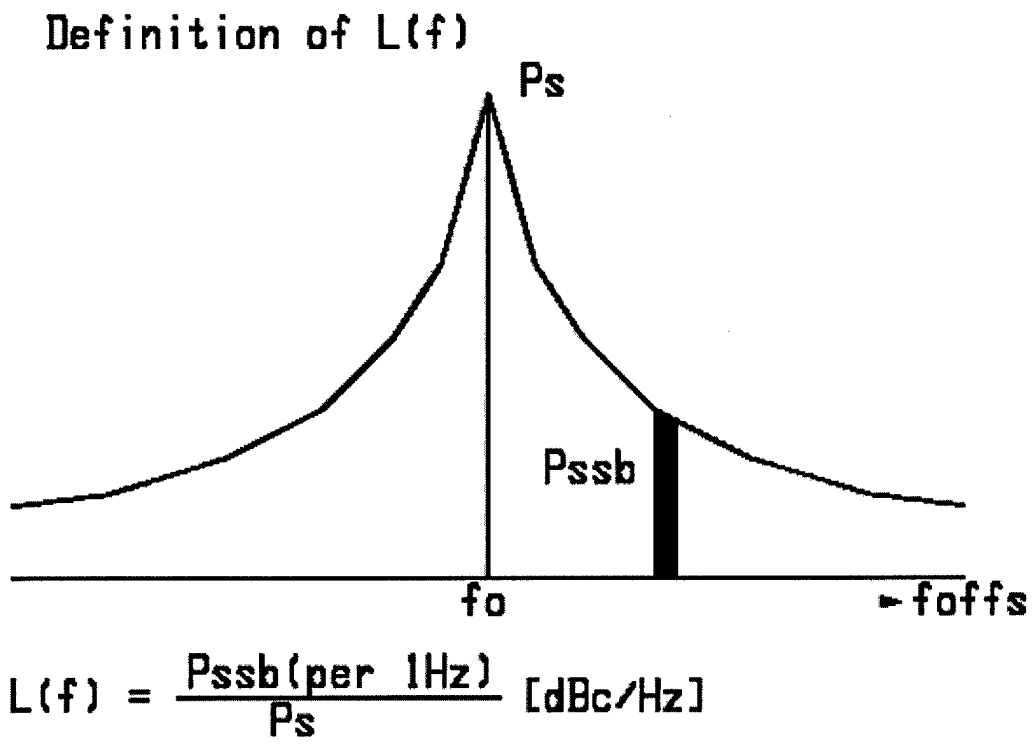


Figure 4.5.1 Definition of Phase Noise

$$L(fm) = \frac{F*k*T}{2P}\left[1+\left(\frac{1}{2Q_L}\right)^2 * \left(\frac{f_0}{f_m}\right)^2\right] \tag{4.5.1}$$

where F is the noise figure of the active device, k is the Boltzman constant, T is the temperature in Kelvins, P is the oscillator power output, Q_L is the resonator loaded Q, f_0 is the oscillation frequency and f_m is the offset frequency from the carrier where the noise power spectral density is measured. Although more accurate noise models have been suggested [5], this form of the noise gives good insight into what factors can be most influenced by design choices. Interestingly, the simple Leesom formulation used to predict phase noise turned out to predict the results found through ADS simulations very well. ADS calculates noise numerically using both small signal mixing and the oscillator's sensitivity to small frequency perturbations. Based on the model proposed by Leesom, the phase noise factors which are most influenced by the design are the output power, and the loaded Q.

The loaded Q, Q_L, is a combination of the circuit effective Q, Q_e and the resonant circuit internal Q, Q_R, such that [9]

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_R} \tag{4.5.2}$$

In a negative resistance oscillator, the resonator appears in parallel with the network seen at the emitter of the transistor. The effective Q for parallel circuits is given by

$$Q_e = \frac{1}{|X_A|} \frac{|R_L \| R_A|}{|R_L| + |R_A|} \tag{4.5.3}$$

In the oscillator case, this can be simplified to

$$Q_e = \frac{1}{|X_A|} \frac{C|R_L|}{C+1} \tag{4.5.4}$$

where R_L is all real resistance on the resonator side of the oscillator, and C is the ratio $|R_L|/|R_A|$. At steady state, with R_L equal to R_A, C is unity and

$$Q_e = 1/2 \frac{R_L}{X_A} \tag{4.5.5}$$

This equation is dominated by X_A which must be equal to X_L and can be close to 0. Low phase noise designs aim to drive this value towards 0 at the oscillation point; however, the transistor topology and packaging lead to non-zero values of X_A. X_A can be minimized by adjusting the transistor base current so the shifts caused by the transistor packaging and the shifts caused by the charge distribution in the transistor counteract each other [10].

4.6 Oscillator Block Matching Networks

Based on the optimization discussed above, the circuit topology used to optimize the impedances is shown in Figure 4.6.1. The circuit consists of three matching networks at each of the transistor ports, the resonator at the transistor base, the emitter grounded through a matching network, and the output at the transistor collector. The output voltage is measured across the transistor collector matching network. The DC power sources provide the transistor base and collector bias.

The optimized frequency based values of each of the matching networks are shown in Table 4.6.1. These values were found using the efficiency based optimization methods discussed in section 4.4. For the selected design the key phase noise parameters as discussed in 4.5 are given in Table 4.6.2.

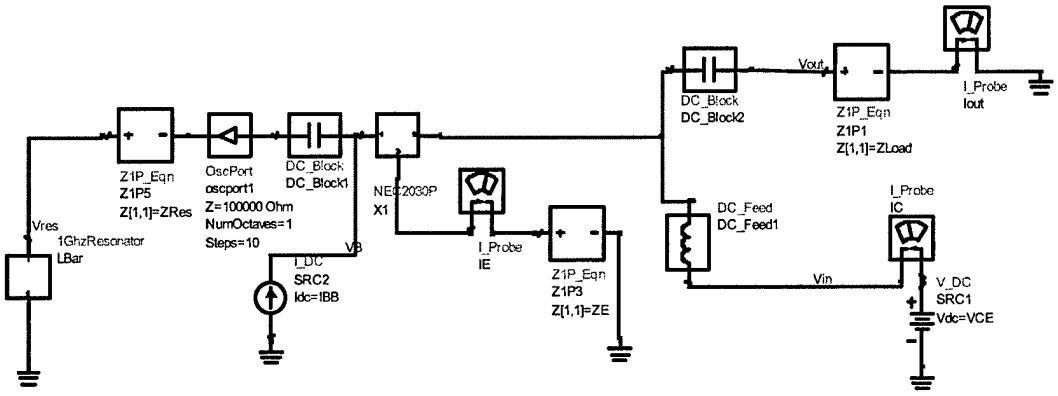


Figure 4.6.1 ADS circuit diagram for block oscillator

This design was optimized to provide maximum efficiency. It is worthwhile to examine the efficiency and phase noise trade space as a function of input power in order to tune the transistor biases. Figure 4.6.2 shows the trade space of the selected design when varying the DC input current into the transistor base. In Figure 4.6.2 we see that although the maximum efficiency occurs at 33.8 μA, the best phase noise is at 34.7 μA. The lowest phase noise point was chosen because the efficiency only decreases slightly with this change while phase noise improves significantly. The large swing in phase noise performance is due to the high sensitivity in loaded Q to slight mismatches in X_{in}.

Running a full noise simulation in ADS gives the predicted values for phase noise, oscillator efficiency, and the output spectrum and waveform shown in Figure 4.6.3. Figure 4.6.3 shows the drop off in phase noise in dBc/Hz at increasing frequency offsets. It corresponds to one half of the signal shown in Figure 4.5.1. The AM noise results and the PM noise results calculated from both small signal mixing and frequency modulation are shown. The most important of these is the PM noise from frequency modulation. This is the noise reported throughout this thesis when describing oscillator performance.

Although the oscillator has significant current and voltage output at higher harmonics as shown in Figure 4.6.4, these are always out of phase with each other so that there is no real power dissipated by these outputs. This was the most efficient design. Optimizations where the higher harmonic voltages or currents were held to zero did not yield designs as efficient, and did not have significantly better phase noise. The presence of these out of phase higher harmonic outputs does not hurt the performance, and in fact helps the design by expanding the solution space. This oscillator performance is summarized in Table 4.6.3.

Table 4.6.1: Block impedance values for the matching networks

Frequency	Base impedance (Ω)	Emitter impedance (Ω)	Load impedance (Ω)
DC	0	0	0
Fundamental	0+j158.11	0.018-j125.49	172.74+j218.27
1st Harmonic	0+j803.70	0-j354.414	0.04+j421.79
2nd Harmonic	0+j1095.9	0.105-j319.30	0.17+j414.19
3rd Harmonic	2.07-j485.53	41.73-j660.53	2.07+j3037.2

Table 4.6.2: Block oscillator key phase noise parameters

Parameter	Value
R_s	189 Ω
X_{in}(approximate)	0.012 Ω
Pout	.011 W
Q_e	94,500
Q_{res}	10,000
Q_L	7875
PQ^2	2.13E6
Phase Noise @10kHz	-156 dBc/Hz

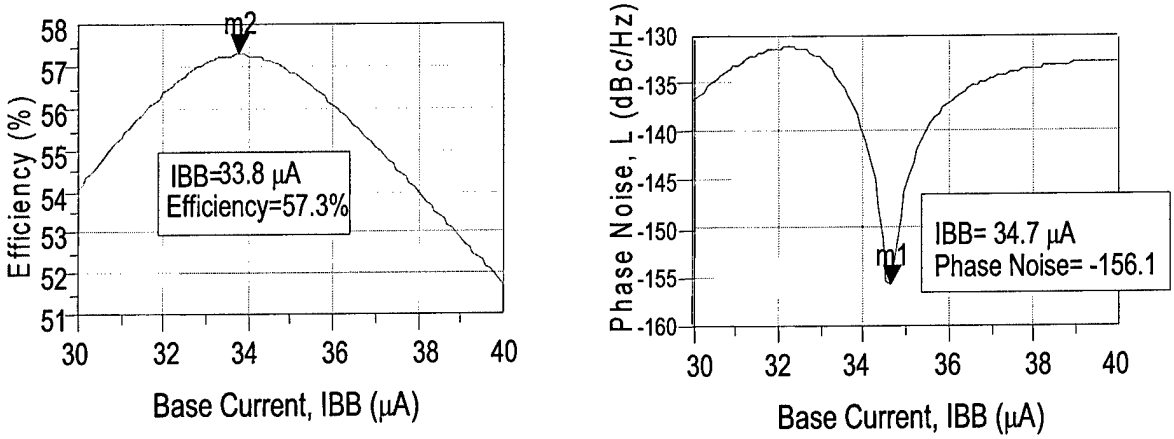


Figure 4.6.2 Efficiency and phase noise vs. base current

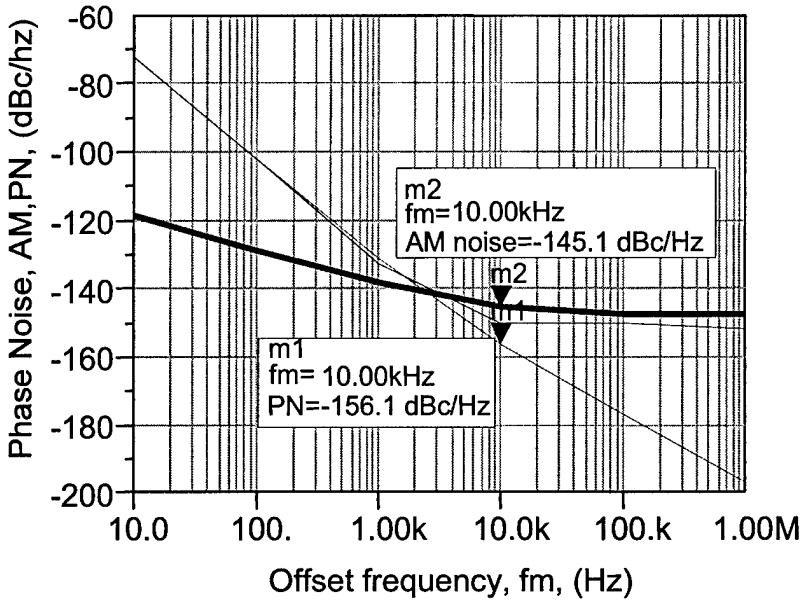


Figure 4.6.3: Block oscillator phase noise

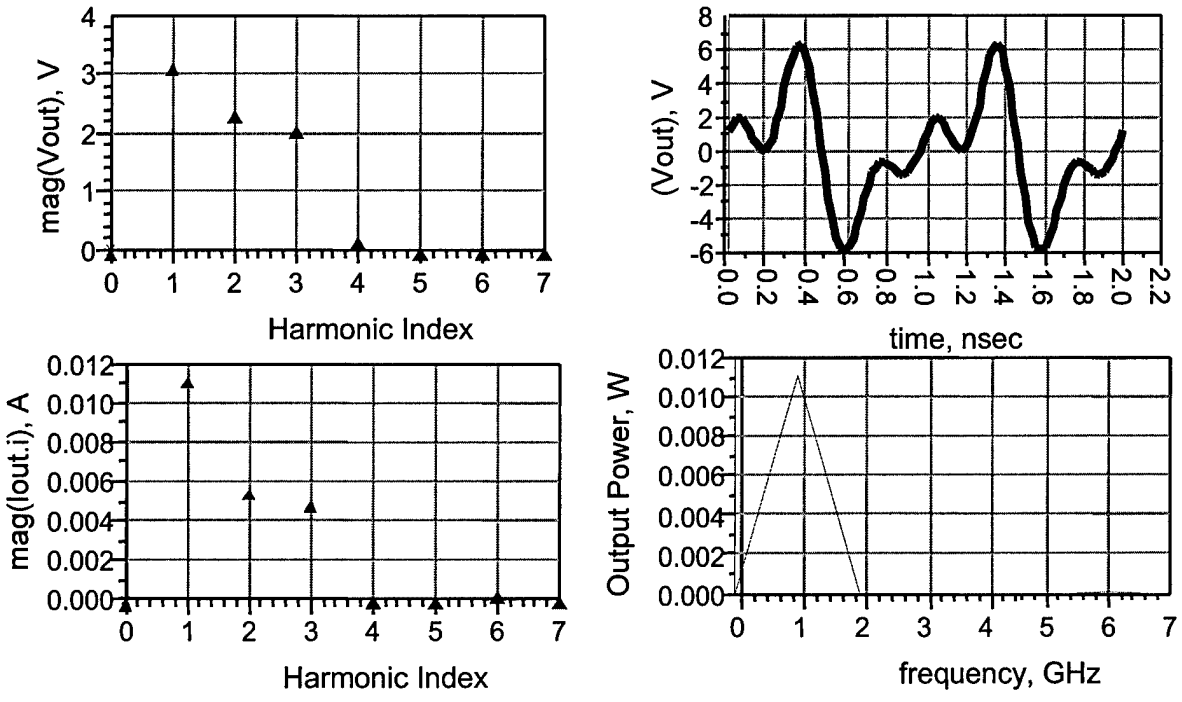


Figure 4.6.4: Block Oscillator Power Spectrum and Output Signal

Table 4.6.3: Block oscillator performance summary

Parameter	Value
Fundamental Frequency	1 GHz
Input Power	19.26 mW
S11	1.997
Z11	-378.8 Ω
Output Power	11 mW
Efficiency	57.1%
Phase noise @ 10kHz	-156.1 dBc/Hz

4.7 Matching Networks: Component Selection

Block impedance models were converted into a design using standard IC compatible electronics components by designing circuit networks that, as closely as feasible, matched the desired frequency dependent impedances at the fundamental and higher harmonic frequencies of the oscillator. A sensitivity analysis was performed to simplify the matching network circuitry while maintaining a high level of oscillator performance.

Sensitivity analysis led to several general rules of thumb that were used in resolving conflicts in the circuit requirements. First, matching impedances at the fundamental frequency and lower harmonics has a greater performance impact than matching at higher harmonics. Second, oscillator efficiency is closely tied to the impedance of the load network, but maintaining the conditions necessary for oscillation is based on the combination of the matching networks at the collector and the emitter. Therefore, it is important to consider these two networks as a single larger network during design. Finally, oscillator phase noise is very sensitive to tuning the base input current. Once an efficient design is found, a base input current sweep should be considered to find a point that optimally trades off phase noise performance and efficiency.

The collector/load network was found to provide optimum performance through theoretical analysis with the block values shown in Table 4.7.1. The values are shown graphically in Figure 4.7.1. It is important to note that the values between the harmonics do not affect the circuit performance. Only the discrete values specifically at 1, 2, 3... GHz affect the performance.

Table 4.7.1 Optimum impedances for collector matching network for 1 GHz oscillator

Frequency (GHz)	DC	1	2	3	4
Real Impedance (Ω)	0	172.74	0.04	0.17	2.07
Imaginary Impedance (Ω)	0	218.27	421.79	414.19	3037.2

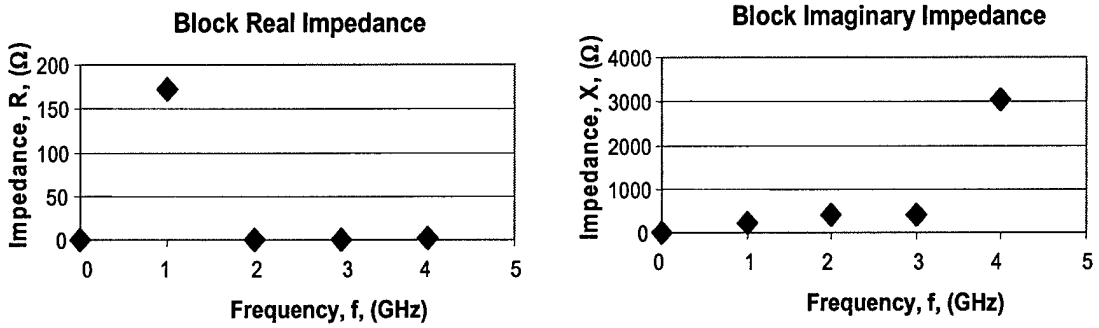


Figure 4.7.1: Optimum impedances for collector matching network for 1 GHz oscillator

Many circuit topologies were considered. The diagram shown in Figure 4.7.2 was selected for its simplicity and close adherence to the desired impedance values. As discussed in Section 4.1, an additional real impedance matching network will be required to interface this network with the desired external circuit impedance. The topology was selected based on the impedance trends found through numerical impedance block analysis. The component values shown were variable throughout the design process. The values shown in Figure 4.7.2 are the final values used after optimization methods that are discussed below. As shown in Figure 4.7.3 the frequency response of this network matches the desired response.

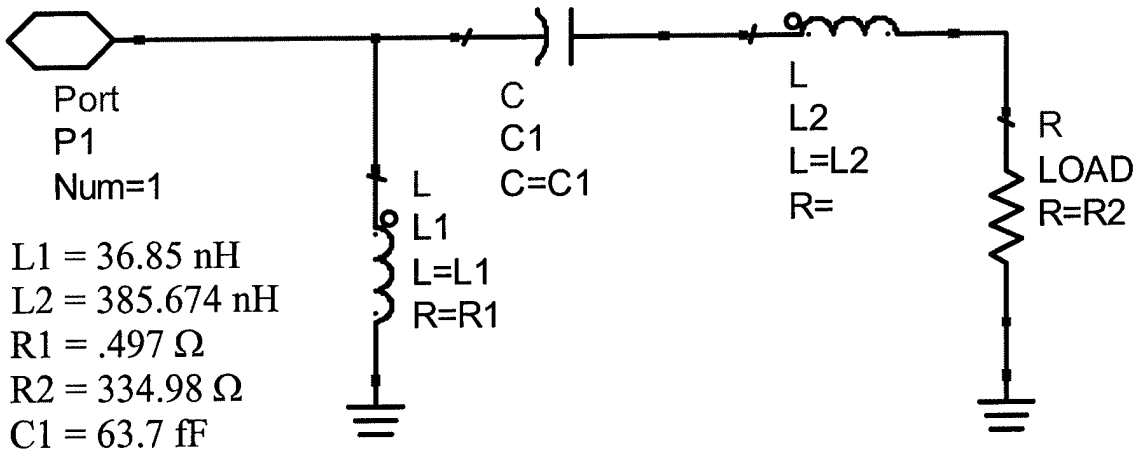


Figure 4.7.2: Collector matching network topology for 1 GHz oscillator design

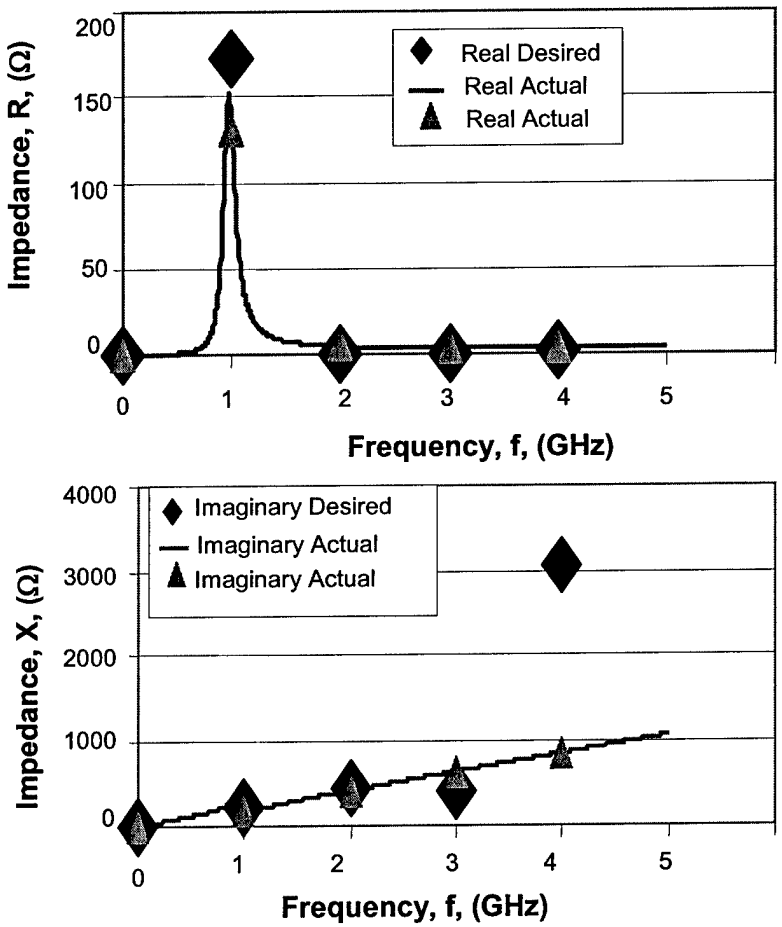


Figure 4.7.3: Actual impedances of collector matching network overlaid with the desired impedances found through block simulations

A similar process was used to design the emitter matching network. First, The desired theoretical block values found through simulation are shown in Table 4.7.2. Graphically these impedances are shown in Figure 4.7.4. Finding a topology that matches these impedances is difficult. No simple network provides monotonically increasingly, negative, purely imaginary impedance with increasing frequency. Therefore, a resonant circuit with several modes was used to match as closely as possible this desired response. The resulting circuit layout is shown in Figure 4.7.5.

The real impedance for the network shown in Figure 4.7.5 is zero at all frequencies. The imaginary impedance frequency response of this network is shown in Figure 4.7.6 overlaid with the desired response. In this figure we see the resonant modes corresponding with the desired impedances at the fundamental and 2^{nd} harmonic.

The base matching network was relatively trivial to design. Theoretical simulations led to the desired block values shown in Table 4.7.3. Sensitivity analysis showed that the 4 GHz harmonic had no noticeable effect on the overall circuit performance. Therefore, the frequency response is the same as a simple low resistance inductor. This base matching network circuit layout is shown in Figure 4.7.7.

Combining these three matching networks in the oscillator design results in the performance shown in Table 4.7.4 and Figure 4.7.8. 51.7% efficiency and -157 dBc/Hz phase noise is comparable to the performance achieved using block impedances. This validates the concept that a highly competitive design can be realized using the L-Bar resonator in conjunction with real components. The next step was attempting to use components that were fully compatible with integrated circuit technology. In practical terms this means limiting inductors to 30 nH and avoiding large (greater than 10 pF) capacitors.

The emitter matching network as shown above already meets these tighter integrated circuit constraints. A redesign of the collector network with the tighter constraints led to unfavorable overall circuit performance. Limiting the inductors in the collector network to a conservative 10 nH resulted in an efficiency degradation of 50%. The performance of this oscillator is shown in Table 4.7.5 and Figure 4.7.9.

Table 4.7.2 Optimum impedances for emitter matching network for 1 GHz oscillator

Frequency (GHz)	DC	1	2	3	4
Real Impedance (Ω)	0	0.18	0	0.105	41.73
Imaginary Impedance (Ω)	0	-125.5	-354.4	-319.3	-660.5

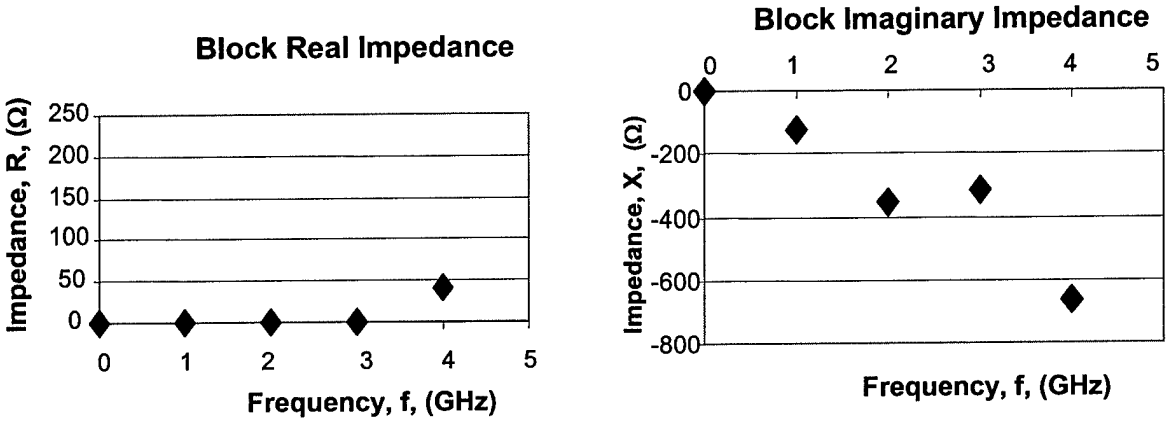


Figure 4.7.4: Desired real and imaginary impedances of 1 GHz emitter network vs. frequency

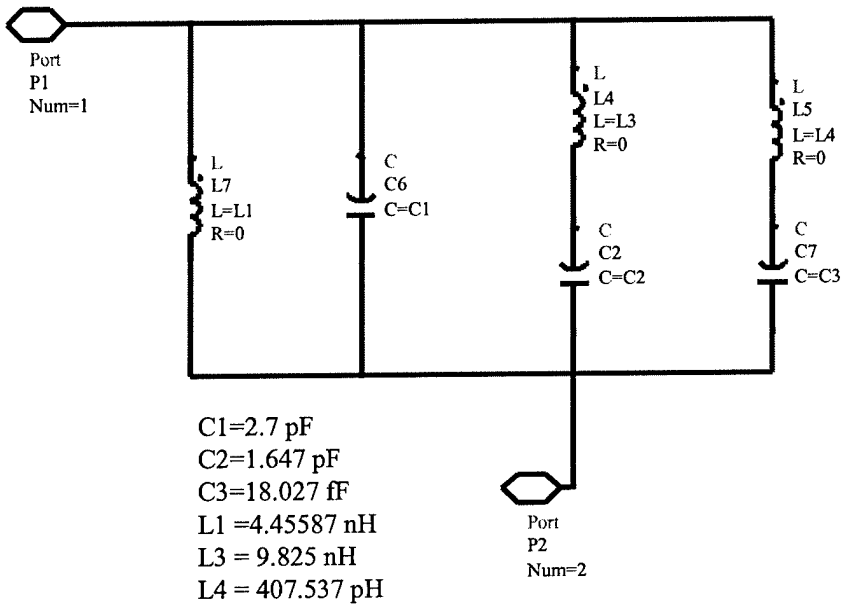


Figure 4.7.5: Circuit topology for emitter matching network for 1 GHz design

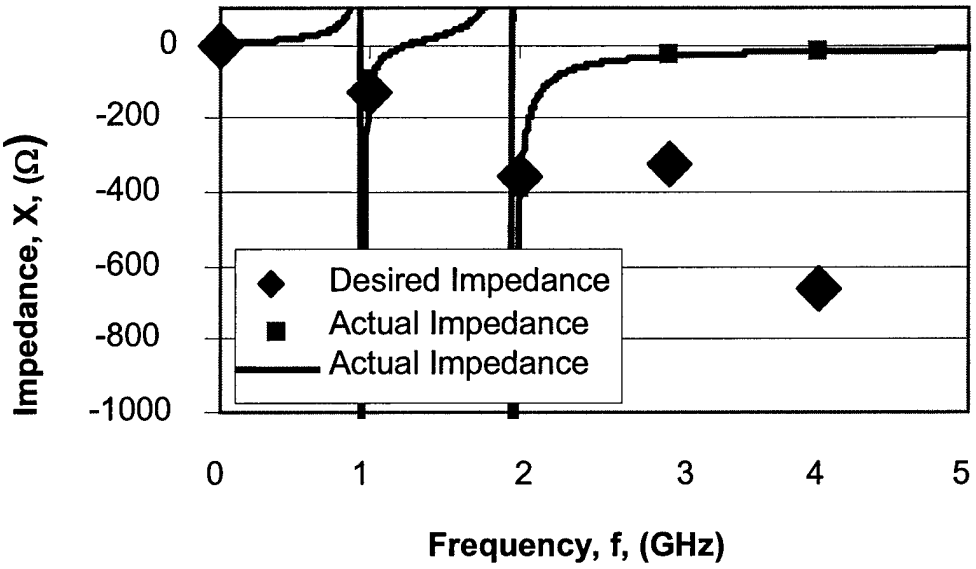


Figure 4.7.6: Actual impedances of emitter matching network overlaid with the desired impedances found through block simulations

Table 4.7.3: Optimum impedances for base matching network for 1 GHz oscillator

Frequency (GHz)	0	1	2	3	4
Real Impedance (Ω)	0	0	0	0	2.07
Imaginary Impedance (Ω)	0	158	803	1095	-485.53

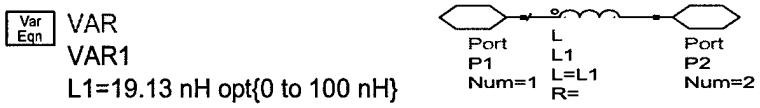


Figure 4.7.7: Circuit topology for base matching network for 1 GHz design

Table 4.7.4 1 GHz oscillator key performance parameters

Parameters	Values
Frequency	1 GHz
Z11	-381.4 Ω
S11	2.059
Efficiency	51.70%

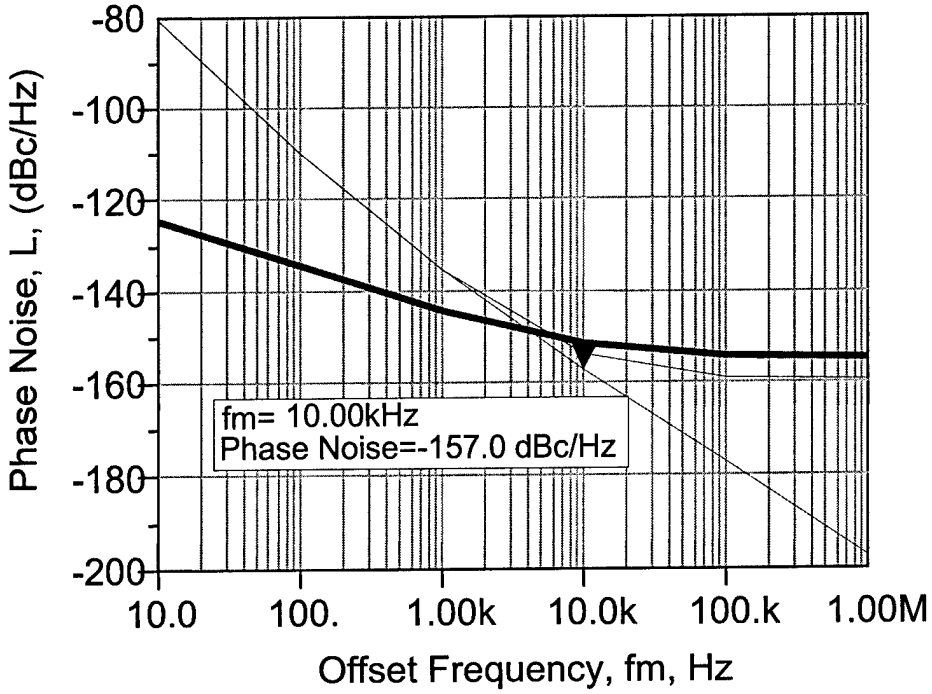


Figure 4.7.8: 1 GHz oscillator phase noise

Table 4.7.5: 1 GHz oscillator with tightened IC constraints key performance parameters

Parameter	Value
Frequency	1 GHz
Z11	-366.1Ω
S11	2.610
Efficiency	25.7%

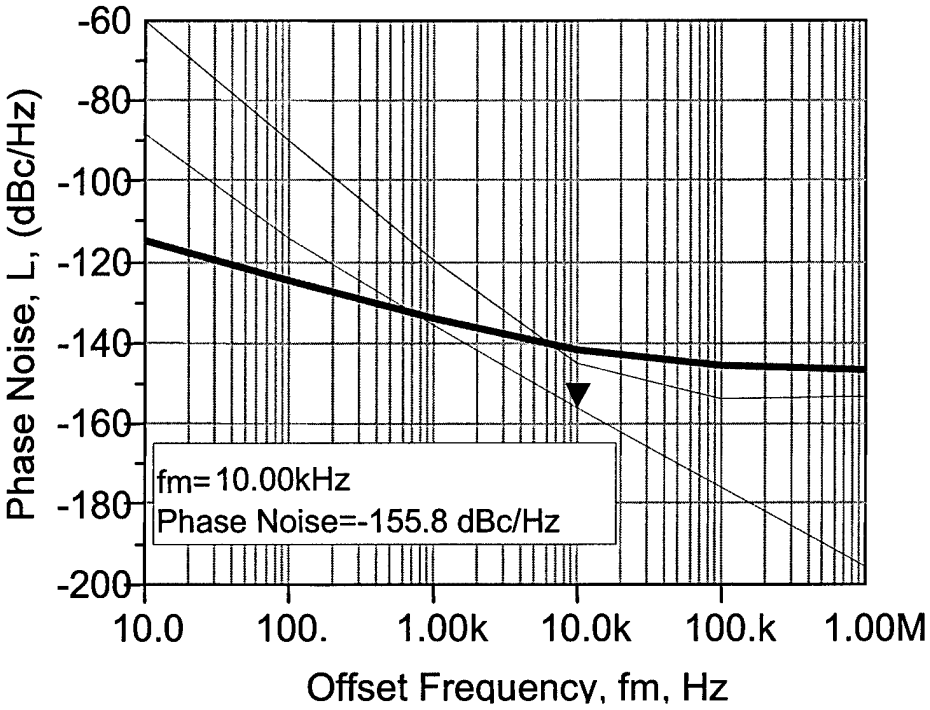


Figure 4.7.9: Phase noise for 1 GHz oscillator with tighter IC constraints

In light of the significant degradation in efficiency, it was decided to relax the constraint on inductor size in the collector matching component. This will require at least one non-integrated inductor on the chip. Future work should consider alternate topologies to eliminate the need for this compromise. Compared to many present designs; however, this fully integrated solution is quite competitive. This was purposely done with very tight constraints as a proof of concept. When selecting actual components competitive performance is predicted even with relatively poor matching network components.

A sensitivity analysis showed that when using real components, the base matching network that consisted of a single large inductor had only a minor effect on the overall circuit performance. Given the difficulty of incorporating a large inductor into an IC design, this feature was eliminated. In final form, eliminating the base matching network resulted in only a 0.1% loss in efficiency. The resulting basic topology is shown in block diagram format in Figure 4.7.10.

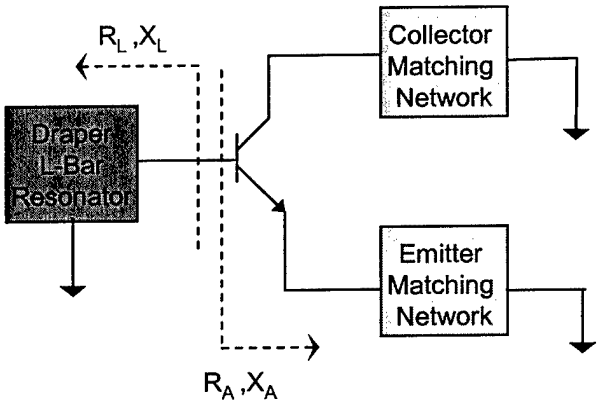


Figure 4.7.10: Block diagram of oscillator topology

The oscillator consists of two matching networks at the transistor collector and emitter, and the resonator at the transistor base. The 3V DC power sources required to provide an adequate transistor bias are not shown in this figure.

Incorporating these matching networks into the oscillator system and performing a base current frequency sweep yielded the efficiency and phase noise response shown in Figure 4.7.11. This figure shows the maximum efficiency and phase noise performance do not occur at the same base current. It was found that increasing the negative impedance looking into the transistor from the resonator shifted the point of maximum efficiency to a higher base current while shifting the point of maximum phase noise performance to a lower base current. The graphs demonstrating this shift are shown in Figure 4.7.12. Table 4.7.6 gives the design goal for static negative input impedance (Z11) used to generate the designs shown in figure 4.7.12. This method of varying the static negative impedance during optimization to create new characteristics curves of the oscillator's efficiency and phase noise offers significant potential improvement in performance. Future oscillator designs should consider this approach to realize low power and low phase noise simultaneously.

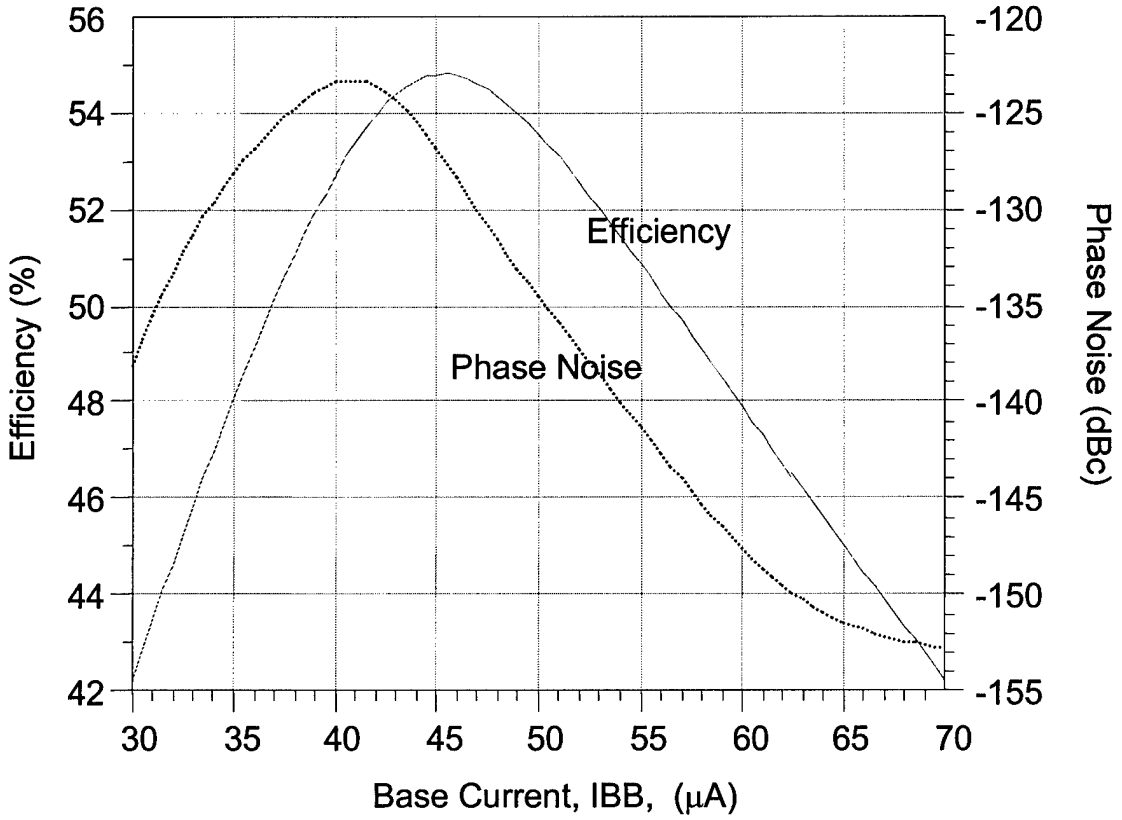
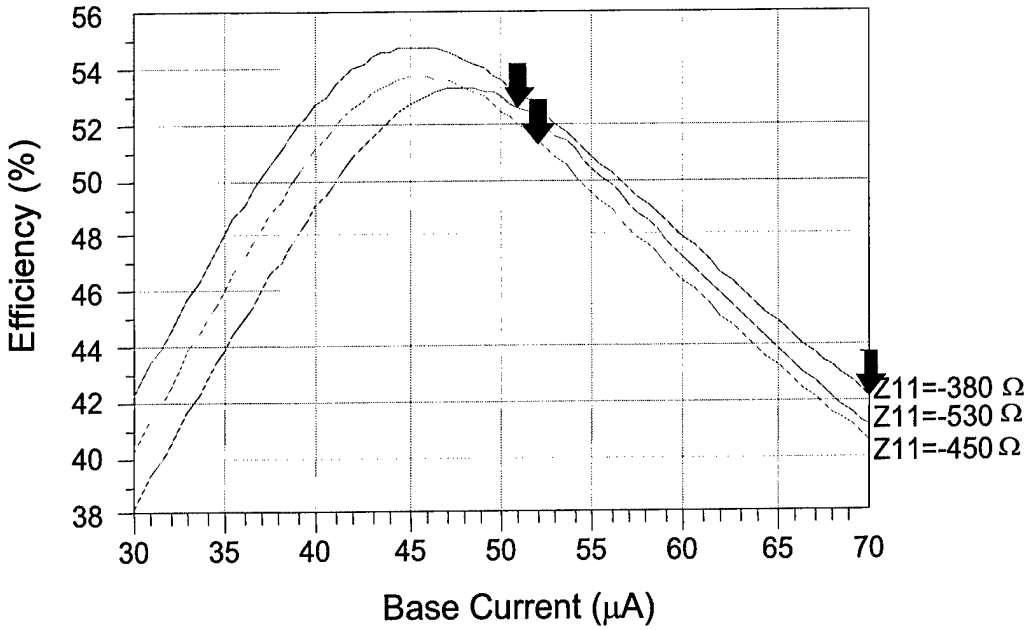


Figure 4.7.11: Efficiency and phase noise vs. transistor base current for baseline design



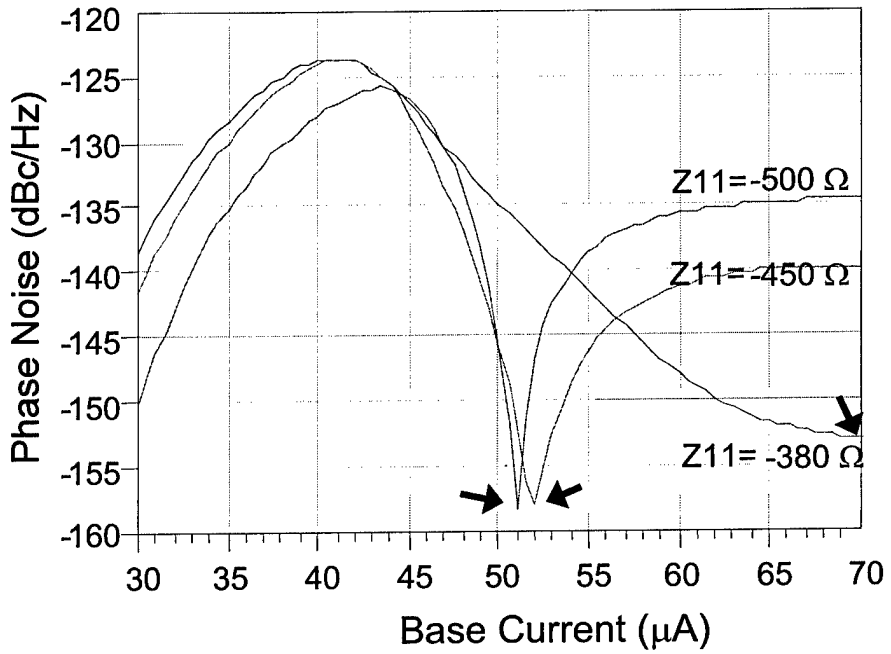


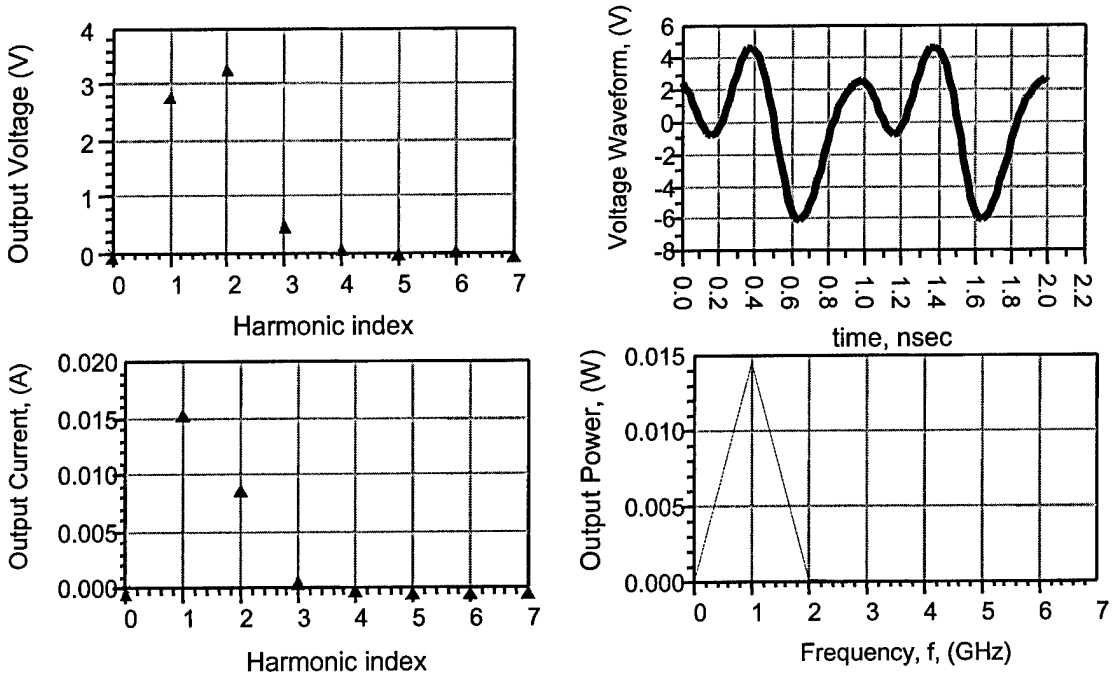
Figure 4.7.14: Phase noise and efficiency with varying static negative impedance goals

Table 4.7.6 Performance with varying static impedances (corresponds to arrows in Figure 4.7.14)

Z11 (Ω)	Base Current (μA)	Efficiency (%)	Phase Noise (dBc/Hz)
-380	70	42.1	-153.1
-450	52	51.4	-158.1
-500	51	52.6	-158.3

4.8 Single Frequency Oscillator Performance

Figure 4.8.1 shows the key oscillation parameters and predicted performance of a design with a static negative impedance goal of at least 500 Ω. ADS predicts exceptional performance for this design. Except for one large inductor used in the collector network, the oscillator can be fully integrated on chip with an extremely small footprint. The fully integrated design without the large inductor showed that even without this inductor this design is competitive. When actually building this device there will be a trade off between the size of this inductor and achievable efficiency.



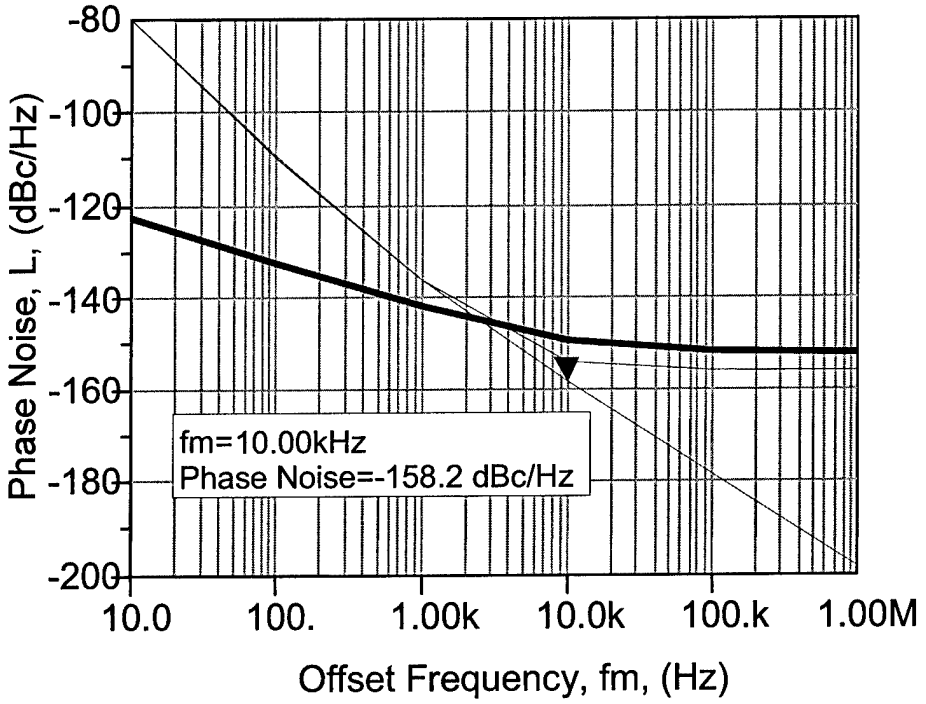


Figure 4.8.1: Power spectrum, output signal, and phase noise for final 1 GHz oscillator design

Table 4.8.1: Performance and key oscillation parameters for final 1 GHz oscillator design

Parameter	Value
Z11	-521 Ω
S11	2.06
DC Input Power	14.55 dBm
Output Power	11.76 bDm
Efficiency	52.6 %
Phase Noise at 10 KHz offset	-158.3 dBc/Hz

Chapter 5
Frequency Synthesizer Design

5.1 Introduction

A frequency synthesizer can be constructed using a switched array of resonators. The array will be connected to the transistor base, and a single resonator will be selected based on the desired frequency of the synthesizer. The extremely small size of the L-Bar resonator makes such arrays practical. Approximately 10,000 resonators could be fit onto a 1 mm^2 chip area. Because each oscillation frequency is derived from a single high Q resonator, excellent phase noise performance over a range of frequencies should be achievable. If continuous tuning or phase locking to a reference is required, it should also be possible to tune the oscillator to create overlap between the resonator frequencies. In both cases an additional load impedance matching network will be needed to match the collector network with the desired external circuit load impedance based on the specific requirements of the application.

Broadband matching networks were developed using two methods. The first approach used networks with fixed components, which had the characteristics necessary for oscillation over a relatively wide frequency window. The second method utilized matching networks with variable components, which would be adjusted based on the selected oscillation frequency.

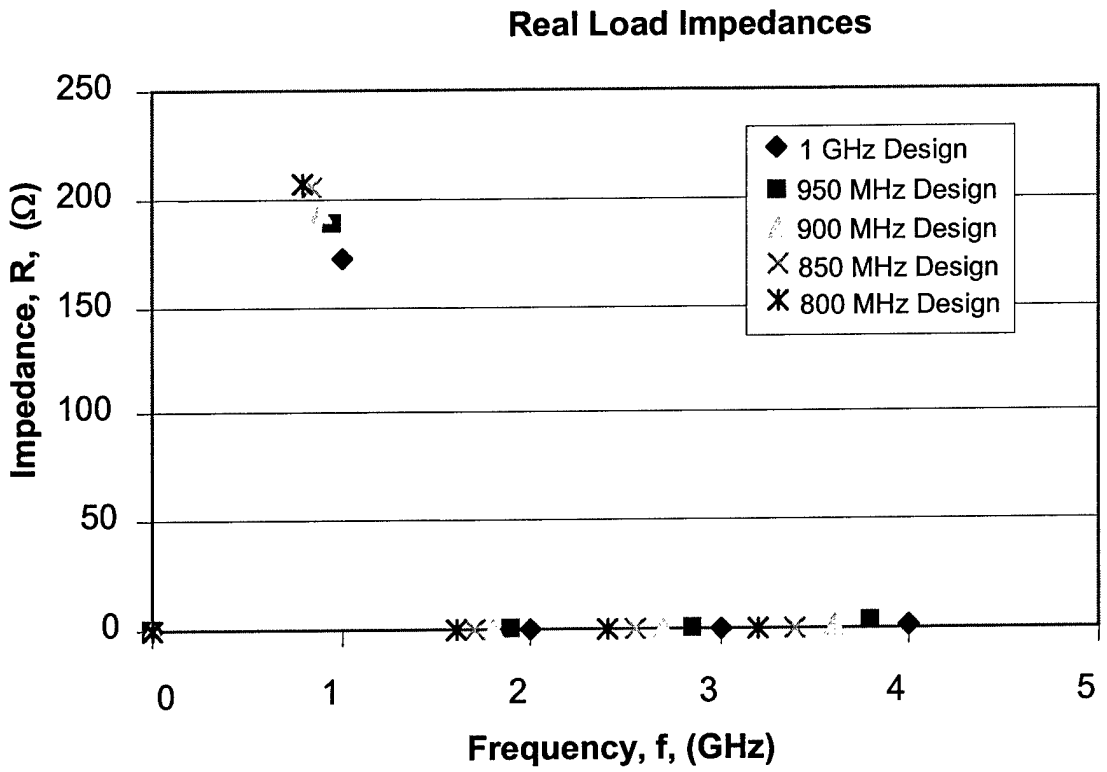
5.2 Frequency Window Design

The first method for designing a frequency synthesizer used low Q matching networks that presented impedances conducive to oscillation over a frequency range. The resonant peaks of these circuits correspond to the desired impedances over a range of fundamental frequencies and the non-resonant portion of the matching networks were designed to match the desired higher harmonic impedance. Four "windows," each covering 200 MHz, would be used to operate from 200 MHz to 1 GHz. The design procedure for each frequency window is the same. The following sections describe a circuit design for the window from 800 MHz to 1 GHz.

5.2.1 Collector Matching Network

First, ADS simulations were used to calculate the block impedances desired at the fundamental and higher harmonic frequencies from 800 MHz to 1 GHz for the collector network. Figure 5.2.1 shows the desired response. The scatter plots in Figure 5.2.1 show a desired response with a real impedance spike over the window of oscillation from 800 MHz to 1 GHz, with no real impedance at higher harmonics. The desired imaginary impedance increases with frequency. An inductor in parallel with a low Q inductor and capacitor pair with some real resistance provides this general response. Figure 5.2.2 shows the circuit diagram. The circuit has the same general topology used in the single frequency oscillator design. The primary difference for application in the frequency synthesizer is that the resonant pair on the right hand side of this parallel circuit has a lower Q. The low Q leads to a wider resonant region, resulting in possible oscillation over the corresponding, wider range of higher real impedance. The general response of this circuit with a low Q resonant pair is shown in Figure 5.2.3.

Figure 5.2.4 shows the actual response overlaid with the desired response. Designing a circuit that exactly matched the desired impedances at both the fundamental and higher harmonics over the full range was not possible. Thus, all designs required some compromise between matching each of the fundamental frequencies and maintaining low real impedance at the higher harmonics. As the range of fundamental frequencies increases, the Q of the resonant branch of the circuit decreases, and the higher harmonic impedance increases. This leads to higher harmonic energy loss, and thus a decrease in efficiency.



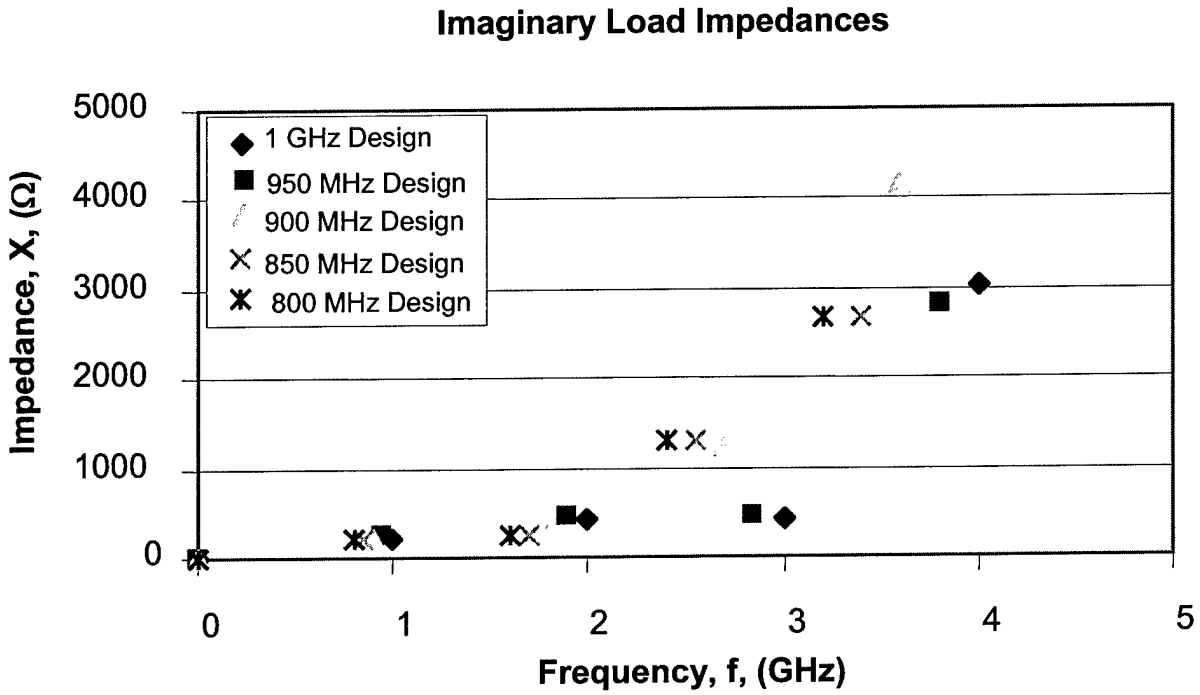


Figure 5.2.1: Theoretical optimum impedances for the collector matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

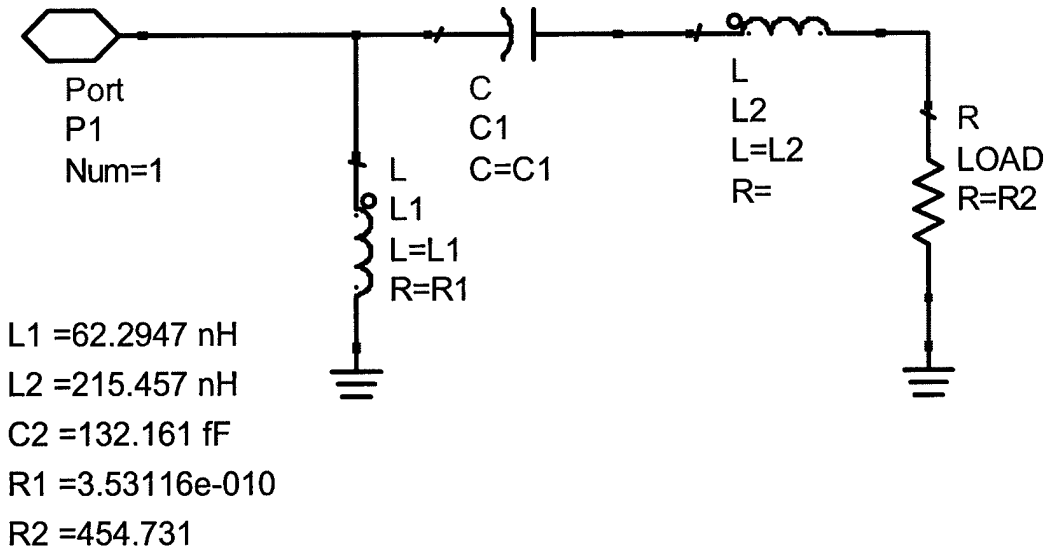


Figure 5.2.2: Circuit topology of the collector matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

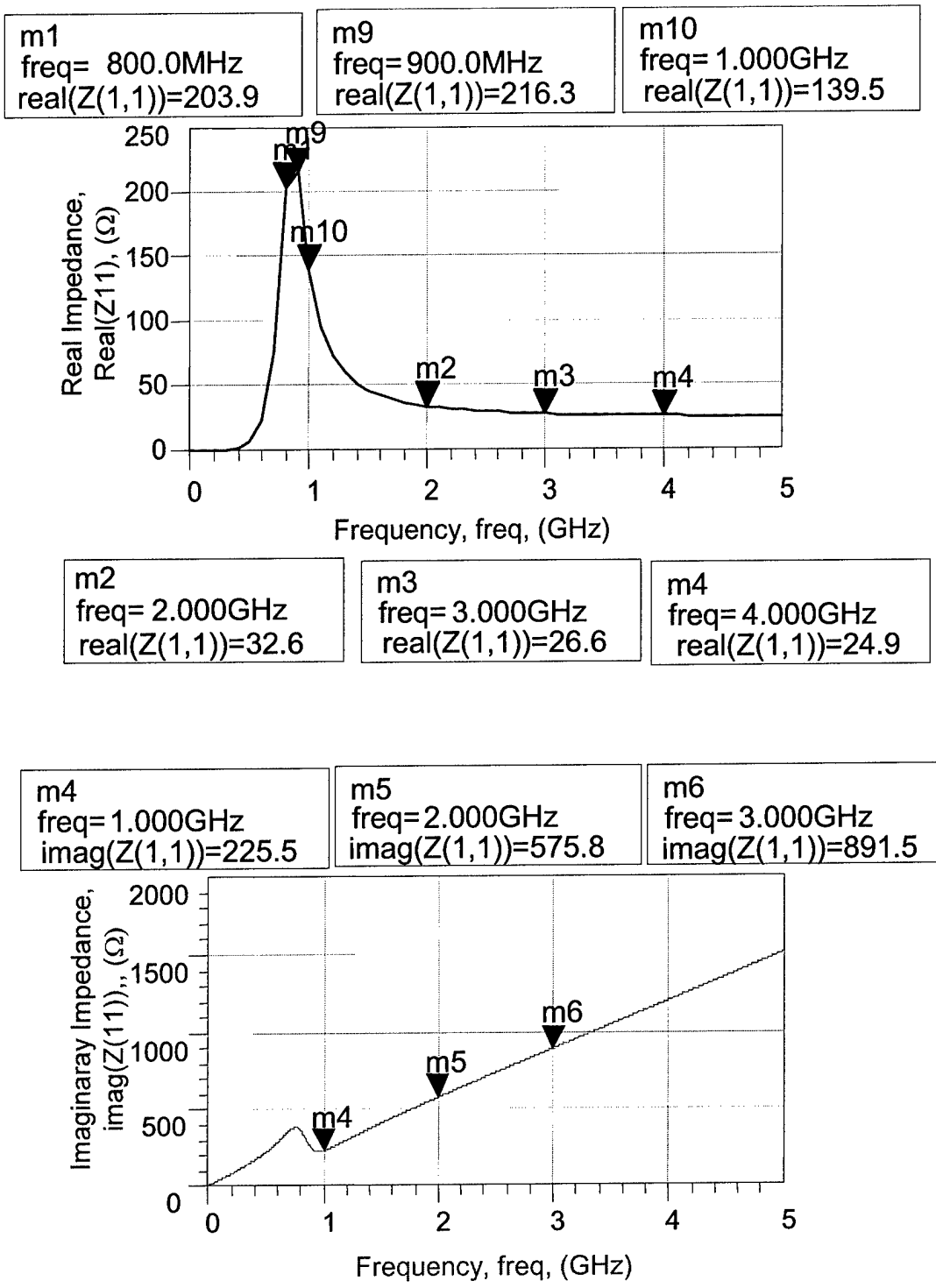


Figure 5.2.3: Real and imaginary response of the collector matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

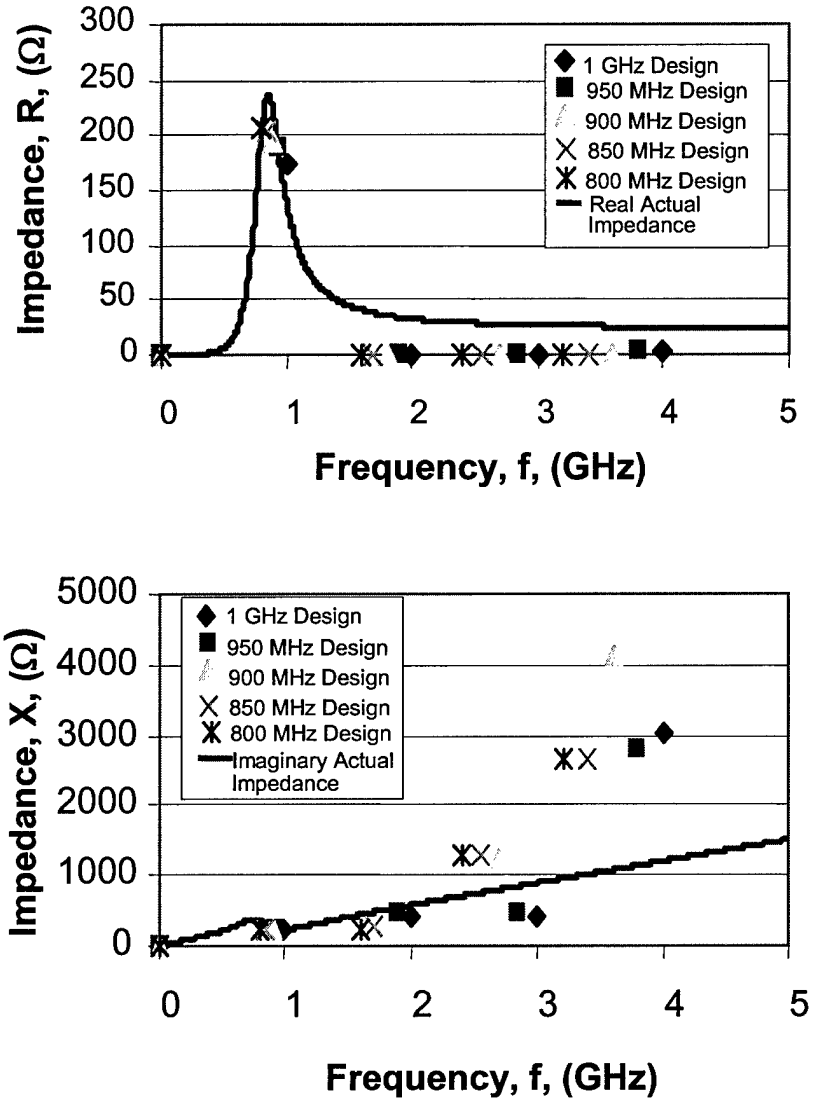


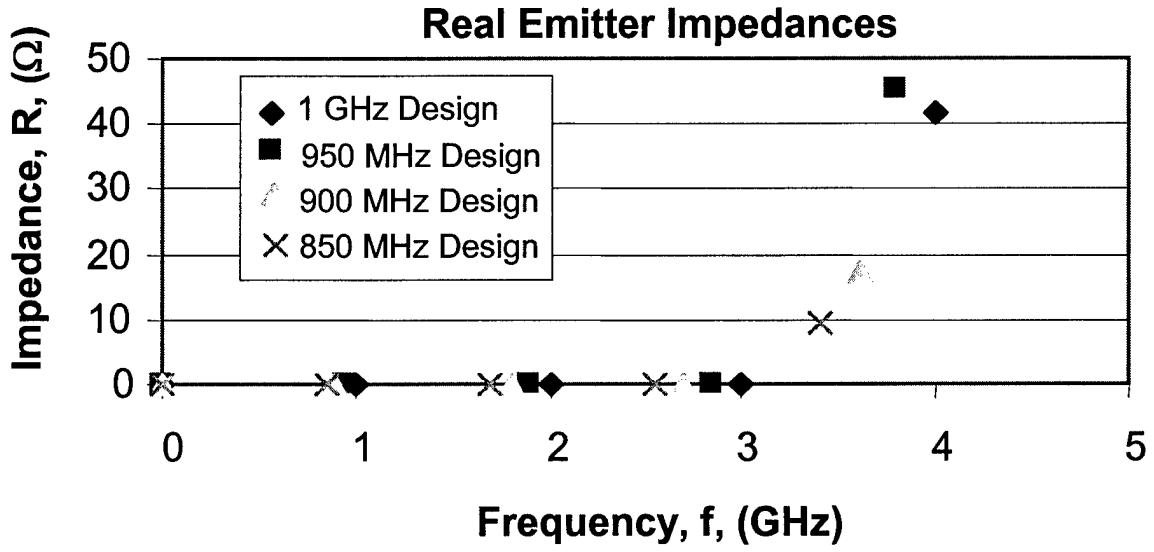
Figure 5.2.4: Theoretical optimum impedances and actual impedances for collector matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

Designing a circuit that exactly matched the desired impedances at both the fundamental and higher harmonics over the full range was not possible. Thus, all designs required some compromise between matching each of the fundamental frequencies and maintaining low real impedance at the higher harmonics. As the range of fundamental frequencies increases, the Q of the resonant branch of the circuit decreases, and the higher harmonic impedance increases. This leads to higher harmonic energy loss, and thus a decrease in efficiency.

5.2.2 Emitter Matching Network

ADS simulations were used to determine optimum block emitter impedances at fundamental and higher harmonic frequencies over a range of oscillator frequencies. Figure 5.3.1 shows the results of these simulations. While the desired circuit response from the simulations shown in Figure 5.3.1 is not quite as clear as in the collector/load network, the basic trend is for zero real impedance and increasingly negative imaginary impedance with increasing frequency. As demonstrated in the single frequency oscillator design, a network with multiple resonant points can create increasingly negative imaginary impedance at discrete points. Therefore a network was designed to match the 2^{nd} harmonic as well as the fundamental. Its response is shown in Figure 5.2.6. This response was achieved using the emitter matching network shown in Figure 5.2.7.

However, this network, when used in the oscillator, did not perform as well as a simpler network that only matched the fundamental frequencies. The method of matching higher harmonics employed by the emitter matching network in the single frequency design did not carry over to this design. When considering a wider frequency range the costs of matching the higher harmonics outweigh the benefits. For a broadband application, the negative effect of decreasing the circuit Q to widen the resonant troughs is more noticeable than the positive effects of matching the higher harmonics. With this being the case, an emitter matching network was designed with just one resonant trough that carefully matched the desired fundamental impedance. This network's frequency response is shown in Figure 5.2.8. This response is overlaid with the desired response in Figure 5.2.9. The topology used to achieve this response is shown in Figure 5.2.10.



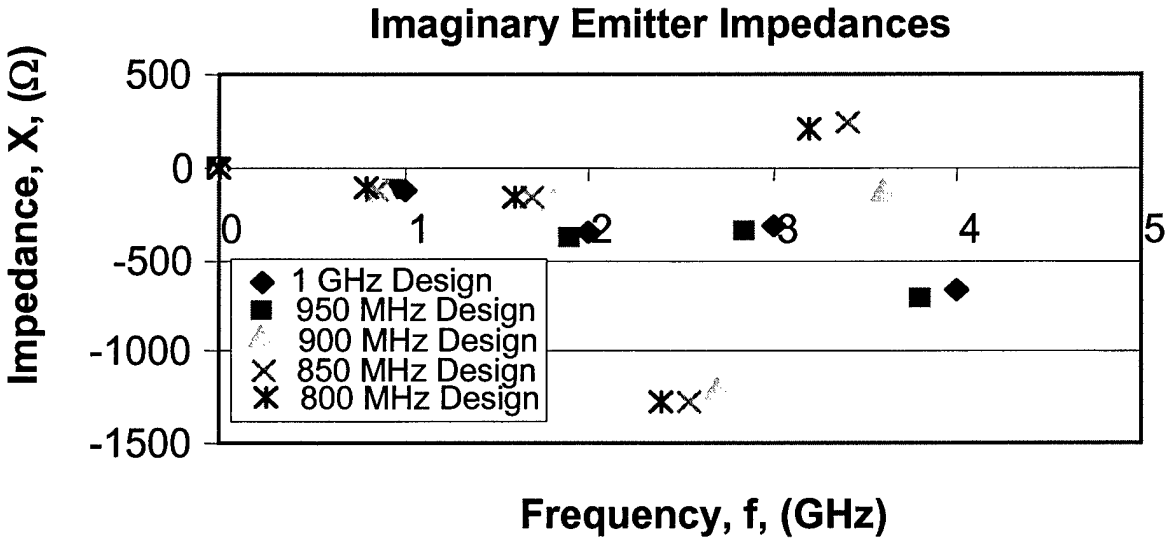


Figure 5.2.5: Theoretical optimum impedances for the emitter matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

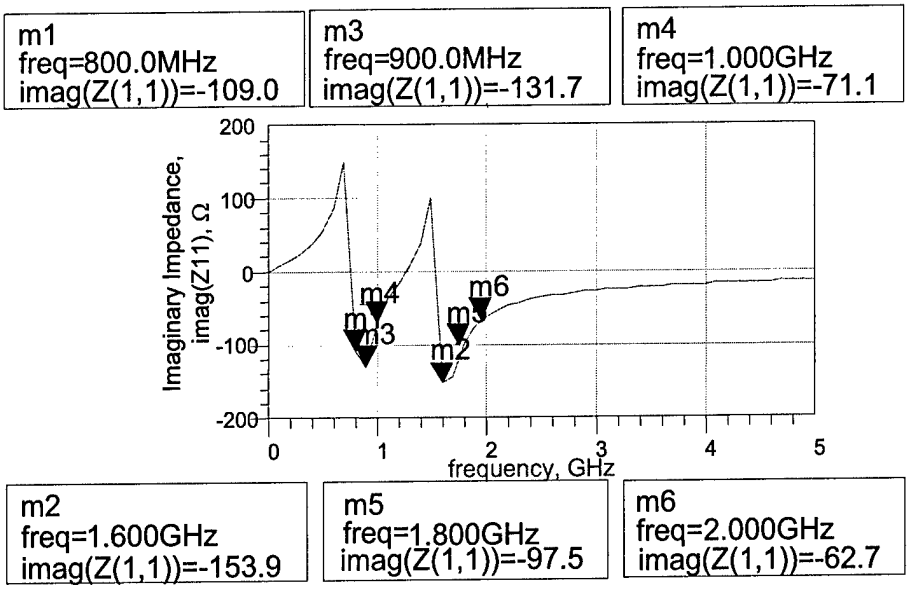


Figure 5.2.6: Imaginary frequency response of a proposed emitter matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

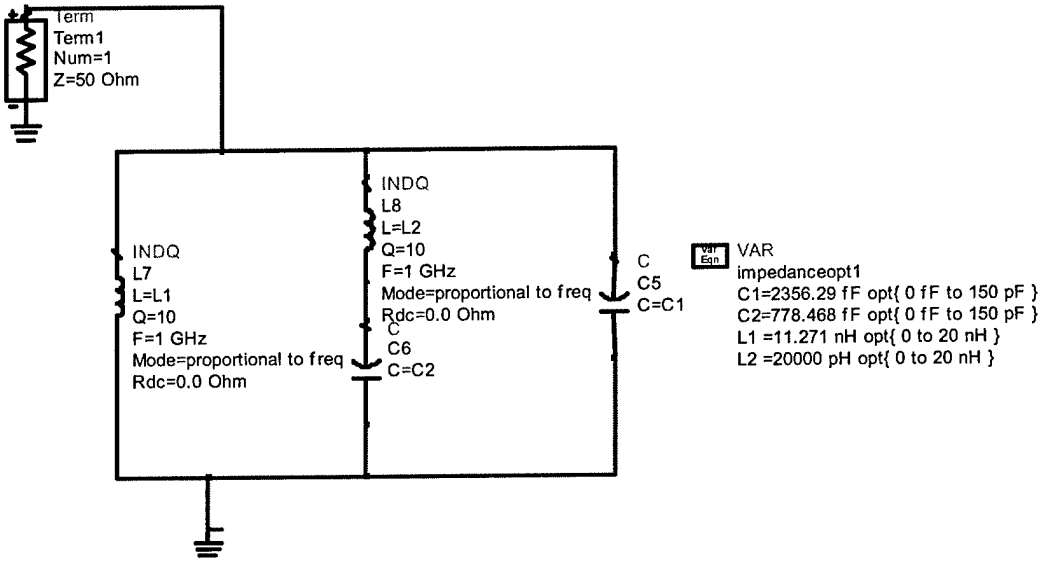


Figure 5.2.7: Circuit Topology of a Proposed Emitter Matching Network as part of a Synthesizer Frequency Window from 800 MHz to 1 GHz

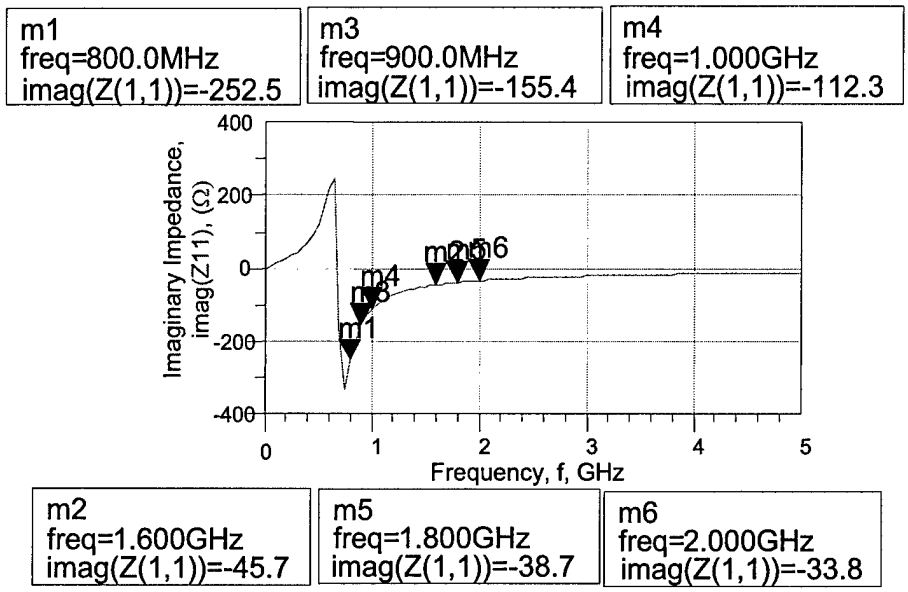


Figure 5.2.8: Imaginary Frequency Response of Final Emitter Matching Network as part of a Synthesizer Frequency Window from 800 MHz to 1 GHz

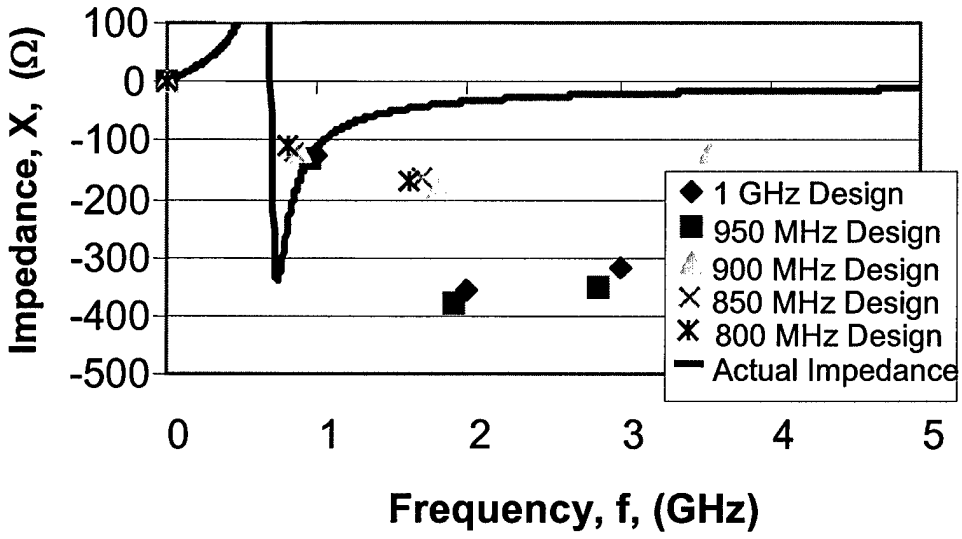


Figure 5.2.9: Theoretical optimum impedances and actual impedances for the emitter matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

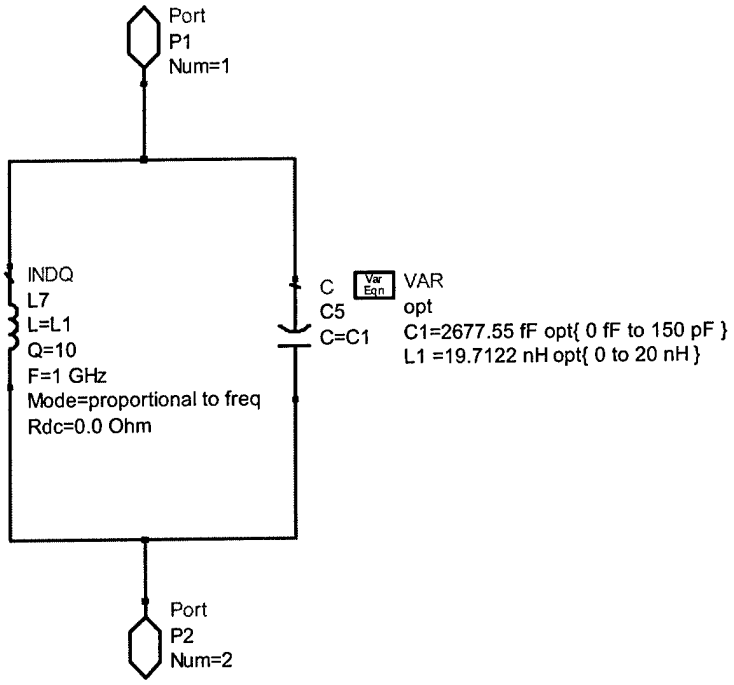


Figure 5.2.10: Circuit topology of final emitter matching network as part of a synthesizer frequency window from 800 MHz to 1 GHz

These networks are then applied to individual resonators to predict the performance of the frequency synthesizer across its range of operation. In practice these resonators would be selected by a solid state or micro-electro mechanical switch. These networks provide a range of possible frequencies of oscillation from 800 MHz to 1 GHz. Using the topologies shown above, many combinations of component values were considered. These values were generated by varying the frequency within the range where each of the networks was optimized, varying the base current, and varying the static negative impedance seen through the transistor. Simulations were then run across its operational range to determine performance for each combination of component values generated by adjusting the design variables.

In order for oscillation to build, the magnitude of *S11* looking into the transistor must be greater than 2 when referenced to the impedance of the resonator, which is 189 Ω [7]. The magnitude of *S11* is quite sensitive to the real impedance of the load network at the fundamental. As a result, great care had to be taken in designing the collector/load network such that the real impedance was high enough at each of the possible fundamentals

to ensure a large . magnitude of *S11*. In practice this meant designing the collector/load network independently and then varying only the emitter network between designs. Figure 5.2.11 shows the resulting magnitude of *S11* vs. frequency plot of the combined matching networks for a representative design. The base current for this plot is 50 μA.

From the data, a design with a collector network fixed by the magnitude of *S11* constraint and an emitter network optimized for performance at 800 MHz worked best across the synthesizer spectrum. The emitter network must have its resonant frequency close to the bottom of the synthesizer range. The impedance sharply diverges at frequencies lower than its resonant point, making oscillation below the resonant frequency of the emitter network impossible.

Changing the static negative impedance alters the inherent trade-off between efficiency and phase noise. Lower negative static impedance leads to higher efficiency designs, but must not drop below twice the resonator impedance for reliable oscillation. Phase noise performance was more difficult to predict. Typically, good phase noise performance is found at relatively high base currents [11]. The base current can be made high for any design with comparable phase noise performance results. However, to maintain relatively good efficiency along with phase noise performance, increasing the static negative impedance up to approximately three times the resonator impedance is beneficial. This pushes the point of highest efficiency to a higher base current and closer to the optimum base current for phase noise. Increasing beyond three times the resonator's impedance, the negative effect on efficiency outweighs this positive effect. A specific frequency synthesizer design may be optimized for either efficiency or phase noise by selecting different base currents.

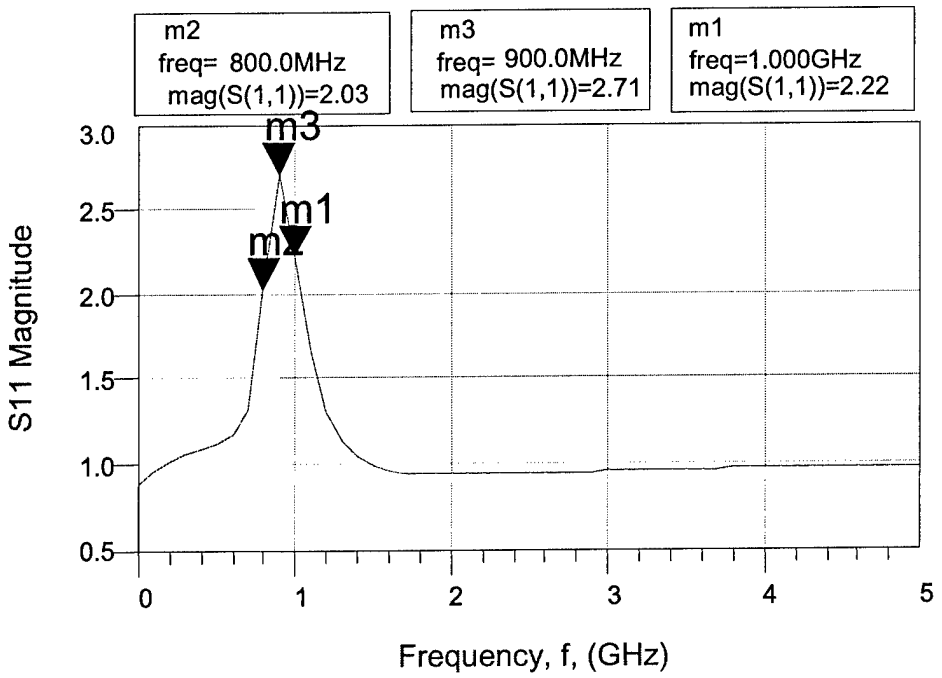


Figure 5.2.11: S11 of combined frequency synthesizer matching networks as part of the 800 MHz to 1 GHz matching window

5.3 Window Frequency Synthesizer Performance

Three variations on the matching networks were considered corresponding to different values of static negative impedance. The collector network remained constant in order to ensure proper oscillation feedback across the range. The values of its components are shown in Table 5.3.1. The emitter network changed with shifting static negative impedance. The values of the three networks used are shown in Table 5.3.2. The most efficient design was found at the lowest examined static negative impedance, $Z11$=-380 Ω. Table 5.3.3 summarizes its performance across its frequency window. The design with the best phase noise performance, while still maintaining reasonable efficiency, was found with $Z11$=-530 Ω. Phase noise performance had the potential to be slightly better than reported, but not without a great cost in efficiency. The design with the lowest phase noise with reasonable efficiency across the frequency range had the performance shown in Table 5.3.4. The complete table of design performances is shown in Table 5.3.5.

Table 5.3.1: Collector matching network component values

Parameter	Value
L1	62.295 nH
L2	215.46 nH
R1	0 Ω
R2	454.731 Ω
C2	132.161 fF

Table 5.3.2: Emitter Matching Network Component Values

Parameters	Case 1	Case 2	Case 3
Impedance (*Z11*)(Ω)	-380	-500	-600
C1 (pF)	2.677	2.425	2.18
L1 (nH)	19.7122	19.7134	19.7654

Table 5.3.3: Matching window frequency synthesizer most efficient design performance

Frequency (MHz)	efficiency	phase noise (dBc/Hz)
800	45.4%	-129.6
900	45.4%	-132.1
1000	44.0%	-124.2

Table 5.3.4: Matching window frequency synthesizer lowest phase noise design performance

Frequency (MHz)	efficiency	Phase Noise (dBc/Hz)
800	34.0%	-159.8
900	37.0%	-159.5
1000	33.0%	-152

Table 5.3.5: Performance variation over the window design space

Z11 = -380							
	Most efficient Base Current				Lowest Phase Noise Base Current		
Frequency	optimum IBB(uA)	efficiency	phase noise @ 10 kHz (dBc/Hz)		optimum IBB(uA)	efficiency	phase noise @ 10 kHz (dBc/Hz)
800	28	45.4%	-129.6		38	37.9%	-159
900	38.5	45.4%	-132.1		56	35.1%	-156
1000	33.5	44.0%	-124.2		60	28.0%	-150
Z = -500							
800	29	38.0%	-130		39	34.0%	-159.8
900	40	43.0%	-132		57	37.0%	-159.5
1000	40	48.0%	-125		65	33.0%	-152
Z=-600							
800	28	32.5%	-133.5		38.5	28.0%	-158
900	41	39.0%	-132.5		59	33.0%	-160
1000	40	48.0%	-125		60	36.5%	-150

5.4 Variable Component Frequency Synthesizer Design

A second frequency synthesizer design uses variable capacitors and resistors within the networks. Using variable components naturally introduces considerable complexity. However, by using these variable components, the selected resonator sees impedances optimized for just its frequency of oscillation. In general, the first method using frequency windows cannot achieve the same level of performance as a design with variable components. A further advantage of using variable components is the selectivity of the matching network. While the window design magnifies oscillation over a 200 MHz range of frequencies, a variable components design only magnifies oscillation over a very small range. If the resonator has spurious modes within the range of the window design which exhibit impedances on the same order as the fundamental mode, the spurious modes could lead to unwanted oscillations and a corrupted output signal. The variable components response is very selective, so the spurious modes of the resonator are not a problem.

Applying variable elements directly to the window-based design yielded only marginally better results. A more effective topology is the one used for the single-frequency oscillator design with the addition of variable capacitors and resistors that change the network impedances to optimize the oscillator at the selected resonator frequency.

Figure 5.4.1 shows the collector matching network topology. C2 and R2 are variable elements and the fixed values of the other elements shown in Table 5.4.1. Figure 5.4.2 shows the emitter matching network topology. C1 and C2 are variable elements and the other elements have the fixed values shown in Table 5.4.2.

The factor that limits the possible range of the frequency synthesizer is the tuning range of the variable components. Current IC technology provides tuning ranges on the order of 2-5 pF or 60% with around 5V control. MEMS variable capacitors or standard nonintegrated capacitors may be able to further extend this range. Table 5.4.3 shows the synthesizer frequency ranges possible as a function of the tuning ranges of the variable components. As can be seen from this table, about a 300 MHz window is possible using standard variable IC components. Using switches it should be possible to achieve an even wider tuning range by switching fixed capacitors in parallel with the varactor, or perhaps just switching in fixed values to perform band switching. Table 5.4.4 shows the predicted values of the key variable capacitors for selected resonator frequencies.

Using design techniques discussed previously in this document, a low phase noise design was developed with the performance shown in Table 5.4.5 across a 200 MHz frequency range. The frequency based schedules for the variable capacitor in the circuit shown in 5.4.1 is parabolic, and the frequency-based schedule for the load resistor is at least piecewise linear and thus both are relatively simple to control. Figure 5.4.3 shows the schedule for the capacitor and Figure 5.4.4 shows the schedule for the resistor. The emitter network shown in Figure 5.4.2 replaced two capacitors (C1 and C2) with variable elements. It may be possible to obtain equal performance by tuning just one of these elements or by placing both of these elements in parallel with one tunable element. In this design iteration both were tuned in order to set up the resonant response at the fundamental and the first harmonic. Again the frequency based schedule shown in Figure 5.4.5 for the capacitors is parabolic and thus relatively simple to control.

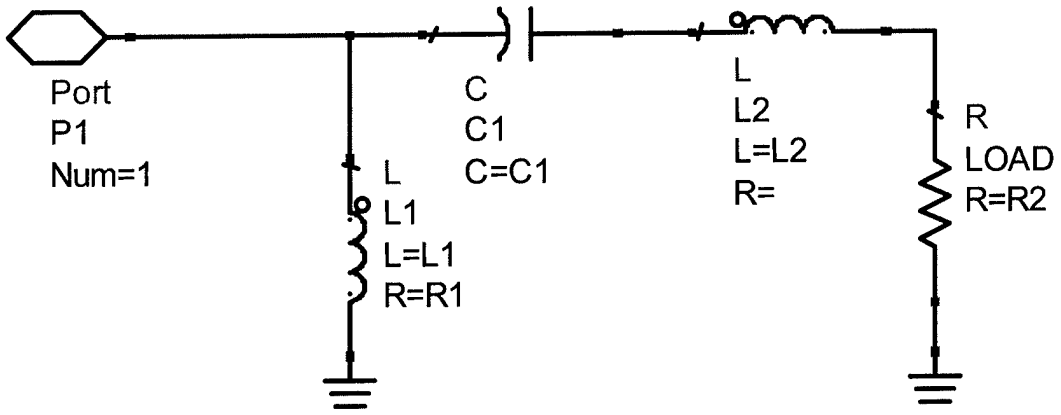


Figure 5.4.1: Circuit topology for collector matching network for variable component frequency synthesizer

Table 5.4.1: Fixed values in collector matching network for variable component frequency synthesizer

Parameters	Values
R1	0 Ω
L1	32.245 nH
L2	389.453 nH

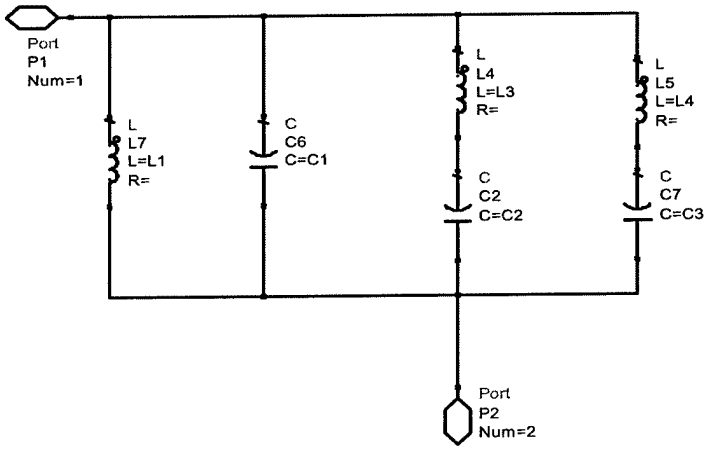


Figure 5.4.2: Circuit topology for emitter matching network for variable component frequency synthesizer

Table 5.4.2: Fixed values in emitter matching network for variable component frequency synthesizer

Parameters	Values
C3	20.13 fF
L1	4.46 nH
L3	9.825 nH
L4	0.445 nH

Table 5.4.3: Variable component frequency synthesizer range based on component tunability

Synthesizer Range (MHz)	1000– 800	1000-600	1000 -400	1000-200
% Tunability for capacitor in Collector Network	32.0	63.9	95.8	127.7
% Tunability for capacitors in Emitter Network	38.6	75.3	112.0	148.6

Table 5.4.4: Optimum variable component values at various selected frequencies

Frequency (MHz)	1000	800	600	400	200
C1(fF) (Collector)	65.31	95.69	177.37	310.34	494.61
C2 (pF) (Emitter)	1.67	2.65	4.84	8.22	12.79

Table 5.4.5: Variable component frequency synthesizer performance from 800 MHz to 1 GHz

Frequency (MHz)	efficiency	Phase noise (dBc/Hz)
800	45.2%	-161.1
850	45.0%	-163.8
900	40.1%	-160.88
950	44.6%	-161.52
1000	40.5%	-161.2

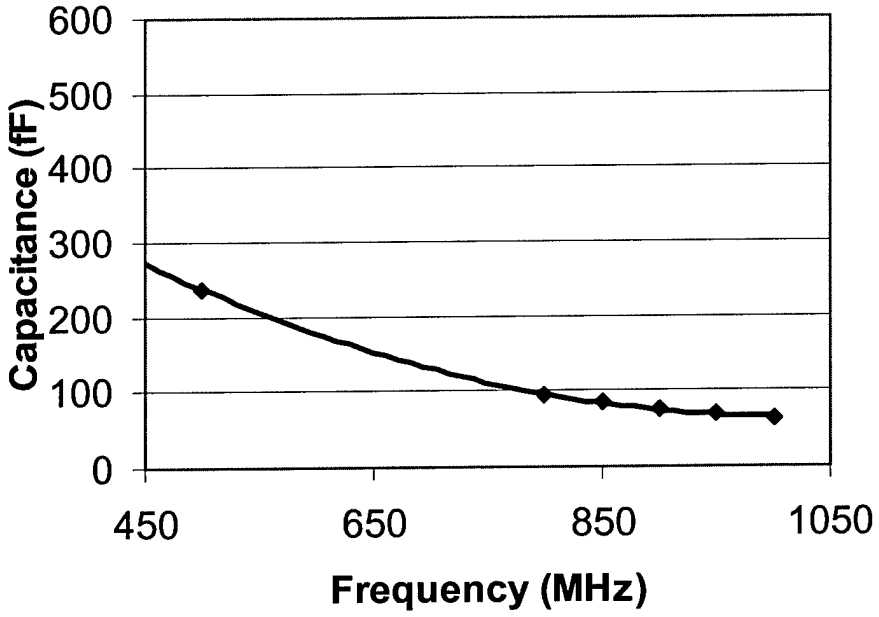


Figure 5.4.3: Capacitance required for collector variable capacitor as a function of frequency

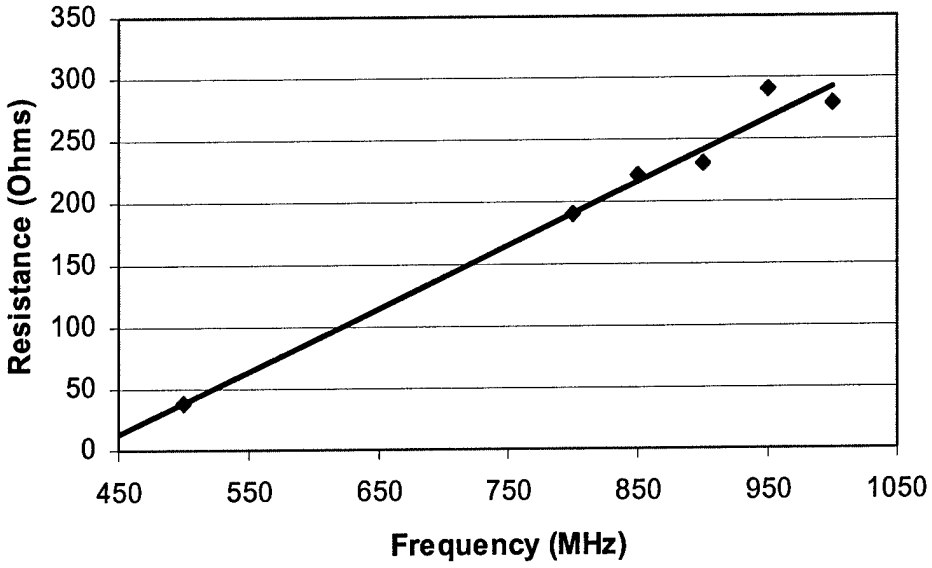


Figure 5.4.4: Load resistance required for collector variable resistor as a function of frequency

Chapter 6
Conclusion and Future Work

6.1 Conclusion

A low phase noise 1 GHz oscillator was designed and simulated using L-Bar MEMS piezoelectric resonators and a single bipolar transistor topology. This design was optimized for efficiency and phase noise. For efficiency, matching networks topologies were designed to minimize power dissipated in higher harmonics through impedance matching. Phase noise performance was enhanced by altering the base current while concurrently adjusting the static negative impedance of the oscillator by changing the component values in the matching networks. This new method of optimization allowed for simultaneous optimization of phase noise and efficiency, which led to a design with predicted performance that was superior to the present state of the art. The resulting design has predicted efficiency in excess of 50% with predicted phase noise less than -158 dBc. Because this oscillator was built around the L-Bar resonator, a standard transistor, and primarily IC compatible matching components, it is extremely small and integratable using standard integrated circuit manufacturing techniques. No other oscillator offers performance in par with the predicted performance of the oscillator presented in this thesis, in such a small, integrated package.

This extremely small, integrated oscillator design opens the door to novel frequency synthesizers using broadband switchable arrays of resonators. Other resonators in existence are not as suitable as the L-Bar resonator for these switchable arrays because they are larger, have a lower quality factor or are not able to be integrated. The novel design

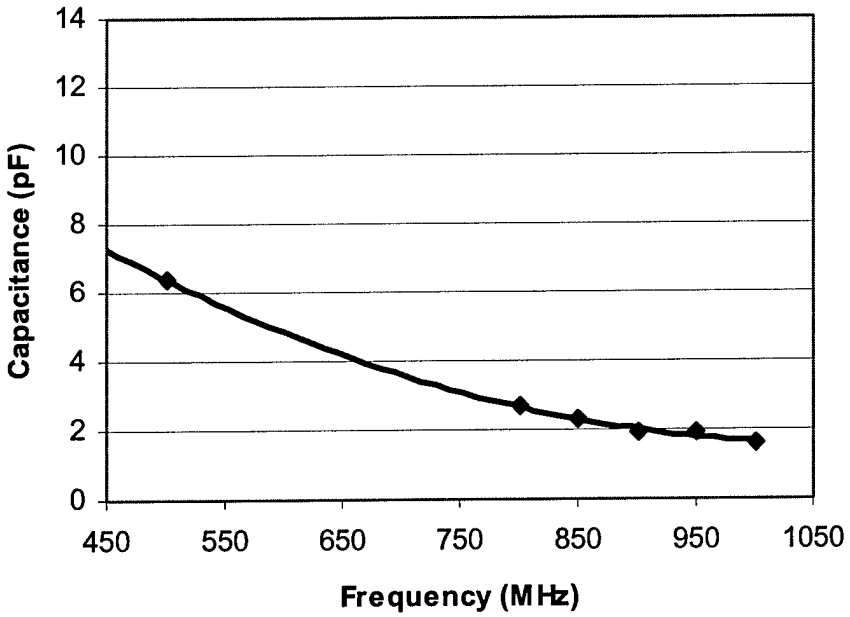


Figure 5.4.5: Capacitance required for emitter variable capacitor as a function of frequency

The variable resistor in the collector network requires that the oscillator to circuit load matching network will have some frequency dependence. This should be relatively straight forward to design based on the specific application.

Further work should be done to examine the synthesizer performance over a wider range. This design concept is promising in that a few sets of matching networks could be used over a wide range of frequencies while maintaining strong performance throughout.

techniques used in the 1 GHz oscillator design are used to enhance the performance of the frequency synthesizers. As a result, the new window and variable components frequency synthesizer designs presented exhibit strong predicted performance across a trial frequency range, while requiring a dramatically smaller chip area than present synthesizers. A frequency synthesizer with at least a 200 MHz range had predicted efficiency greater than 40% with predicted phase noise less than -160 dBc across its operational range.

6.2 Future Work

The strong performances predicted by the simulations motivate continued work on the L-Bar oscillator project leading to building and testing the oscillator and the continued development of the frequency synthesizers. The component values in this thesis are intended to guide component selection, not directly prescribe values. As the resonator model is refined and actual components with losses and parasitics are selected, the methods in this thesis should be iterated. Ultimately the oscillator should be built and tested to verify the simulated performance.

Additional work should also be done to develop suitable switches for the frequency synthesizer. The switched array frequency synthesizer concept is dependent upon rapid, very small, low loss switches that can be integrated along with the rest of the design. The development of these switches will be vital to realizing the frequency synthesizers as presented in this thesis.

Appendix A

Material Parameters of Aluminum Nitride

$\rho = 3.3 \cdot 10^3 \quad \mathrm{kg/m^3}$

$e_{31} = e_{32} = -0.58 \quad \mathrm{C/m^2}$

$e_{33} = 1.55 \quad \mathrm{C/m^2}$

$e_{14} = 1.13 \quad \mathrm{C/m^2}$

$e_{15} = -0.48 \quad \mathrm{C/m^2}$

$c_{11} = 3.45 \cdot 10^{11} \quad \mathrm{N/m^2}$

$c_{13} = 1.20 \cdot 10^{11} \quad \mathrm{N/m^2}$

$c_{33} = 3.95 \cdot 10^{11} \quad \mathrm{N/m^2}$

$c_{44} = 1.18 \cdot 10^{11} \quad \mathrm{N/m^2}$

$c_{66} = 1.10 \cdot 10^{8} \quad \mathrm{N/m^2}$

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