

NAVAL POSTGRADUATE SCHOOL

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THESIS

**DESIGN AND IMPLEMENTATION OF A HIGH-POWER
RESONANT DC-DC CONVERTER MODULE FOR A
REDUCED-SCALE PROTOTYPE INTEGRATED POWER
SYSTEM**

by

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September 2001

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INTEGRATED POWER SYSTEM**

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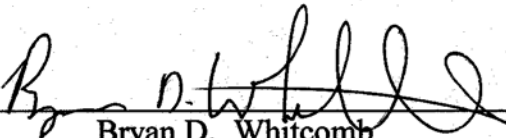
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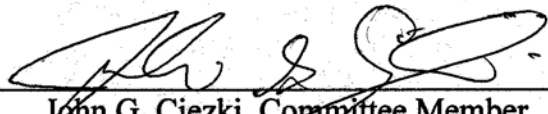
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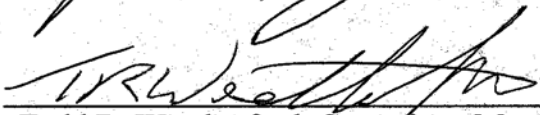
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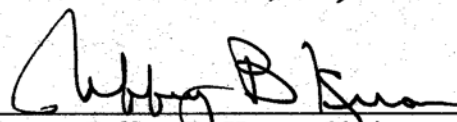

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ABSTRACT

An Integrated Power System (IPS) with a DC Zonal Electrical Distribution System (DC ZEDS) is a strong candidate for the next generation submarine and surface ship. To study the implementation of an IPS with DC ZEDS, members of the Energy Sources Analysis Consortium (ESAC) are currently constructing a reduced-scale laboratory. One fundamental component of DC ZEDS is the Ships Service Converter Module (SSCM), commonly known as a buck DC-DC converter. This thesis documents the design, simulation, construction and testing of a 500V/400V, 8kW resonant soft-switched DC-DC converter. In theory, resonant converters will operate more efficiently and generate less Electromagnetic Interference (EMI) when compared to a standard hard-switched converter. In this thesis, the resonant converter is tested and compared to a hard-switched DC-DC converter that was designed for ESAC's reduced-scaled IPS. The results verify that the resonant DC-DC converter realizes significant efficiency and EMI generation improvements over the hard-switched converter at the cost of a more complex control system and power section.

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EXECUTIVE SUMMARY

The Navy is currently investigating the feasibility of using an Integrated Power System (IPS) with a DC Zonal Electrical Distribution System (DC ZEDS) in future submarines and surface ships. An IPS is a ship design concept where both an electric propulsion system and ship's service electrical system are powered from a common set of electrical power sources. A ship designed with an IPS is able to rapidly distribute power between the propulsion and combat systems based on the current operational situation. In addition, an IPS employing a DC distribution can conduct fault isolation in microseconds compared to fault-isolation times in the milliseconds for a conventional AC distribution system. The Energy Sources Analysis Consortium (ESAC), consisting of researchers from Naval Postgraduate School, Purdue University, University of Missouri-Rolla, University of Wisconsin-Milwaukee and the United States Naval Academy, have proposed the design and construction of a reduced-scale IPS with DC ZEDS. Building a reduced-scale IPS laboratory would allow researchers to investigate new power converter designs, control systems and stabilization algorithms.

A key component of DC ZEDS is the Ship Service Converter Module (SSCM). In its simplest form, a SSCM consists of a feedback-controlled buck DC-DC converter. The DC-DC converter serves as a buffer between the main DC power source and inter-zonal loads, such as DC-AC inverters and motor controllers. A basic schematic of a DC-DC converter is illustrated in Figure (1).

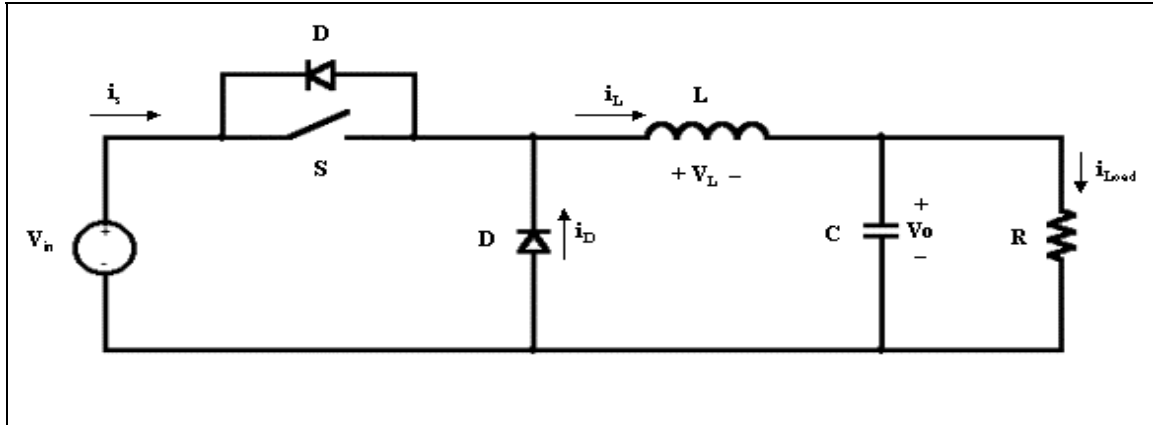


Figure 1. Classical Buck DC-DC Converter.

By controlling the duty cycle of switch S , a voltage V_o , which is proportional to V_{in} , is developed across the load R (for continuous-conduction mode operation). To minimize filter size and audible noise and to maximize control bandwidth, the switch is typically operated at frequencies in excess of 20 kHz.

All real semiconductor switches (IGBTs, MOSFETs and BJTs) have conduction and switching losses. The conduction losses are constant for varying switching frequencies, given that the load and duty cycle are constant. Conversely, the switching losses are proportional to the switching frequency for a constant load and duty cycle. The switching losses place an upper limit on the maximum frequency that a device can be operated at without exceeding thermal limits. Each time a switch is gated "on" with a voltage across it, losses occur as the switch begins to conduct current. When the switch is subsequently gated "off," current will continue to flow until the voltage across the switch builds up to the blocking voltage. In order for high-frequency switching converters to be viable options, resonant soft-switching converter topologies have been developed by a number of authors. A 500V/400V, 8kW, 20 kHz resonant soft-switching DC-DC converter has been developed to support ESAC's ongoing research in the area of IPS with DC ZEDS. The resonant converter was compared to a hard-switched DC-DC converter with similar ratings, so that performance, efficiency and Electromagnetic Interference (EMI) improvements could be documented.

The objectives of this research were to:

- Select a suitable resonant converter topology,
- Describe the modes of operation and develop appropriate dynamic equations,
- Design the resonant converter based on the dynamic equations,
- Conduct a detailed PSPICE simulation of resonant converter,
- Build the resonant converter based on the design results,
- Test the resonant converter to verify performance, efficiency and EMI,
- Optimize the design for efficiency using PSPICE and MATLAB,
- Test the resonant converter to verify efficiency gains and EMI,
- Compare the testing results to the hard-switched converter and make recommendations as to whether the resonant converter should be selected for use in an IPS DC ZEDS.

A resonant converter (also called a soft-switching converter) is broadly defined as a converter that uses LC resonances to create a zero-voltage across a switch or a zero-current through a switch before the switch is operated in order to reduce or eliminate switching losses. Several published topologies were analyzed for expected efficiency, ease of control and complexity. The topology selected for this research is illustrated in Figure (2). The Joung topology has a major advantage in that it is simply a classical DC-DC converter with additional resonant components added to create the Zero-Voltage Switching (ZVS) and Zero-Current Switching (ZCS) conditions necessary to reduce switching losses. No additional components are added in the main current path, thus ensuring maximum efficiency. The additional resonant components are included inside the dashed area in Figure (2), where C_{r1} is simply the body-capacitance of the main switch.

To understand the operation of the selected topology, eight distinct modes of operation were identified, compared to the two modes of operation for the basic DC-DC

converter. Each mode of operation was described with differential equations, which would later be used to design and then optimize the converter.

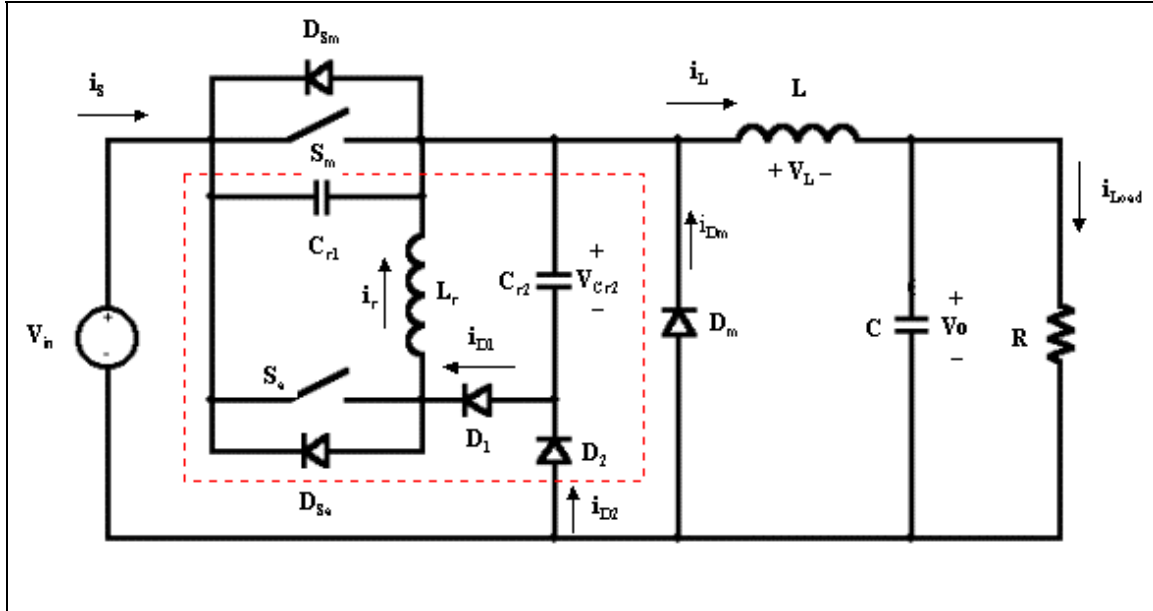


Figure 2. Joung Resonant Converter Topology.

The converter was designed using the well-known equations for the basic hard-switched buck chopper along with equations developed from the mode analysis. The resonant component values were calculated based on the estimated duration of time that each mode should last. With peak current and voltages now known, the different families of power semiconductor switches were studied to determine the best device for the design. Bipolar Junction Transistors (BJTs), Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide Field-Effect Transistors (MOSFETs) were compared and it was decided that the IGBT was the best choice for this design. IGBTs have both high-voltage blocking capability coupled with high-current ratings. IGBTs also have fairly quick switching times ($\sim 100\text{ns}$), which help reduce switching losses. IGBTs have the disadvantage that significant current, called a "current tail," continues to flow after the device is gated "off," thus increasing turn-off losses. New technologies based on Silicon Carbide (SiC) and Gallium Nitride (GaN) are now in the development phase and they could greatly improve the performance of power converters in the future.

With a switching device selected, a PSPICE simulation was developed using a detailed IGBT model. Several simulations were run for varying load conditions. The voltage and current waveforms were plotted at several points in the circuit, so meaningful comparisons could later be made with the constructed converter. The simulation estimated that the full-load efficiency was 98.4 percent and the minimum-load efficiency was 97.6 percent.

Next, the converter was constructed based on the simulation results. Considerable effort was spent selecting the proper filter capacitors and winding the toroidal-core inductors for the input and output filter sections. The PSPICE voltage and current waveforms were used to estimate the magnitude of the magnetic-flux intensity (H) and the magnetic-flux density (B) that would exist in the resonant-inductor core. An equation to estimate the magnetic force was derived and a toroidal core was selected based on calculations.

The concept of a compact power module was also developed. The resonant converter was designed so that the IGBTs, diodes and resonant components were all located on a printed circuit board. The completed circuit module was then installed on a heat sink for cooling. The design minimized stray inductance, which can cause severe voltage spikes to occur in the paths where high di/dt 's exist. The completed converter with component labels is shown in shown in Figure (3).

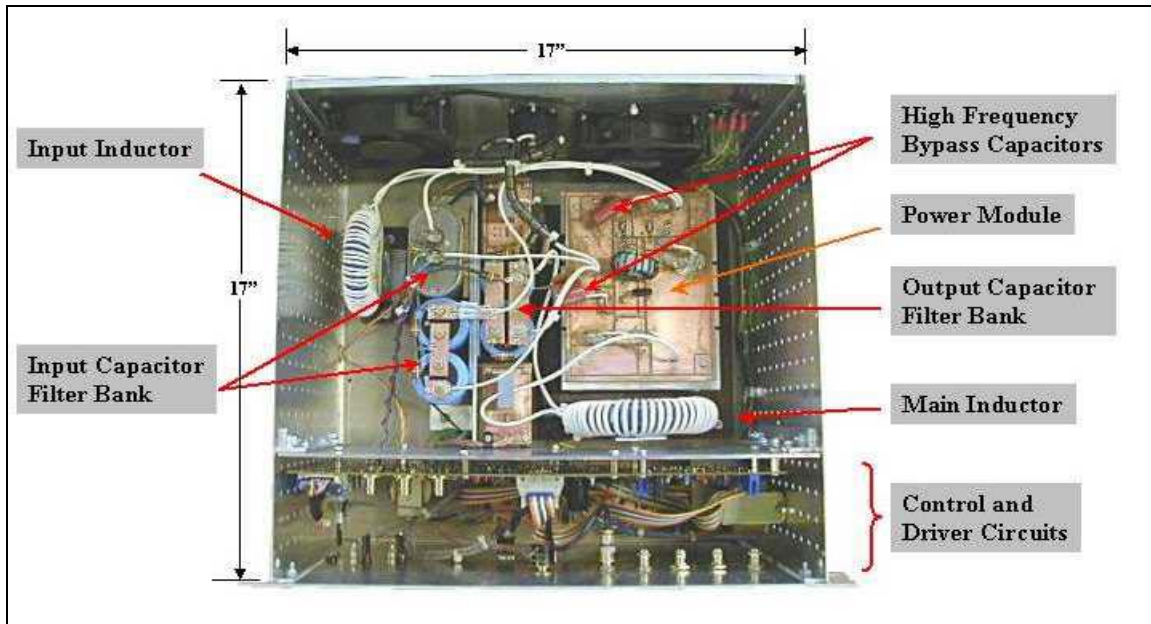


Figure 3. Top View of the Resonant Converter.

The completed converter was thoroughly tested and it was discovered that the PSPICE simulations accurately predicted all of the major waveforms that could be measured. The PSPICE diode models were less than adequate in that they failed to fully predict the reverse recovery aspect of the diodes. The measured full-load efficiency was 97.9 percent and the minimum-load efficiency was 97.5 percent. The differences between the estimated and actual efficiency are due to losses in the core and wiring that are not accounted for in the PSPICE simulation. The testing also demonstrated that the main switch had significant turn-off losses (~50 watts) with the characteristic "current tail" lasting over 1 μ s.

To further improve the converter's efficiency, the eight modes of operation were analyzed and two were identified as causing excessive loss. It was discovered that by picking appropriate values for L_r and C_{r2} in the Joung topology (see Figure (2)), the energy loss in the two modes could be minimized. This optimized efficiency corresponded to the conditions that L_r and C_{r2} have equal energy capacity and C_{r2} is as large as possible so that it can supply the load current momentarily when the main switch is gated "off." A PSPICE simulation was used along with a MATLAB program to estimate the switch losses during turn-off. The switch losses were then plotted as a

function of the resonant capacitance and the minimum energy loss was found to occur when the energy capacity of L_r and C_{r2} were matched as theorized. Upon optimizing the resonant converter, the simulated efficiency increased to 98.8 percent. This 0.4 percent improvement over the earlier simulation is a power-loss reduction of 33 watts in the main and auxiliary switch while supplying 8kW to the load.

The converter was modified using the optimized resonant components and significant improvements in the efficiency were observed. The converter's efficiency was estimated to be 98.3 percent at full load. This is an efficiency increase of 0.4 percent over the pre-optimized converter as predicted by the PSPICE simulation.

Finally, the conducted EMI for the hard-switched converter and the resonant soft-switching converter was measured for a frequency range of 100 kHz to 100 MHz. The conducted EMI was also measured before and after optimization. A power converter can generate significant amounts of high-frequency EMI due to the inherently high di/dt 's and dv/dt 's that exist in the circuit paths. The EMI testing demonstrated that both the hard-switched and soft-switched DC-DC converters generate significant amounts of EMI that could disrupt other equipment connected to the same power lines. The measurements also revealed that high enough currents existed on the DC input and output power lines that a radiated EMI problem could occur, thus disrupting equipment not connected through power lines.

One of the frequently advertised advantages of a resonant converter is the reduction in EMI generation. The research showed that the pre-optimized converter had a more severe EMI problem on the DC output power line compared to the hard-switched converter. Not until the resonant converter was optimized were significant improvements in the EMI spectrum observed. After optimization, the EMI bandwidth was reduced from 45 MHz to 5 MHz and the peak current dropped from 40mA to 890 μ A (~33dB).

The objectives of this research were met: a robust and efficient resonant DC-DC was designed, simulated, constructed and tested. The optimized resonant converter had an efficiency improvement of 0.7 percent over the hard-switched converter and

significantly reduced EMI generation on the DC output power line. All three converters had similar EMI bandwidths and spectrum magnitudes on the DC input power line.

The resonant converter has some disadvantages when compared to the hard-switching converter, such as:

- The control circuit complexity increases because of the addition of an auxiliary switch along with more stringent timing criteria;
- The required development of fast driver boards which are able to drive the IGBTs "on" and "off" rapidly (no suitable Commercial-Off-The-Shelf (COTS) driver boards available);
- It is more difficult to acquire suitable resonant capacitors and build resonant inductors as converter power levels increase.

This research demonstrated that the Joung resonant DC-DC converter is a viable option for use in the DC ZEDS of a modern warship. To further refine the converter's design and performance, the following additional research is required:

- The further study of EMI problem including research on how to best reduce EMI with converter layout and filtering;
- The refinement of PSPICE IGBT and diode models, so that designers can reliably simulate converters operating at power levels exceeding 100kW;
- The design and development of a Digital Signal Processing (DSP) based control and protection circuit;
- The construction of a reduced-scale IPS at NPS, so that professors and students can study converter interfacing, paralleling and stability issues.

Given that future submarines and surface ships will have some form of a DC ZEDS on board, it is imperative that more research be conducted in the area of power converters to ensure that efficient and reliable systems are delivered to the fleet.

I. INTRODUCTION

A. INTEGRATED POWER SYSTEM FOR FUTURE WARSHIPS

The naval vessels of tomorrow will differ greatly from the ships of today. With limited defense dollars, the Navy is interested in developing cost-effective combatants that use high-technology Commercial-Off-The-Shelf (COTS) equipment to improve producibility, operational flexibility and survivability [1]. Future combatants will have fewer personnel who must operate and maintain the complex systems and any additional power systems that will be required. As ship designs have progressed, there was always a need to maintain or reach higher speeds, so available propulsion power obviously had to increase. Based on the current level of propulsion power available, hull weight, hydrodynamics and quieting considerations, ships cannot go much faster. At the same time there is a continual increase in the amount of electrical power required with the advent of modern combat systems, pulsed energy weapons and Electromagnetic Aircraft Launching Systems (EMALS) [2]. Figure (1-1) illustrates the shaft horsepower required over time as ship designs have progressed and contrasts the trend in the electrical power requirements.

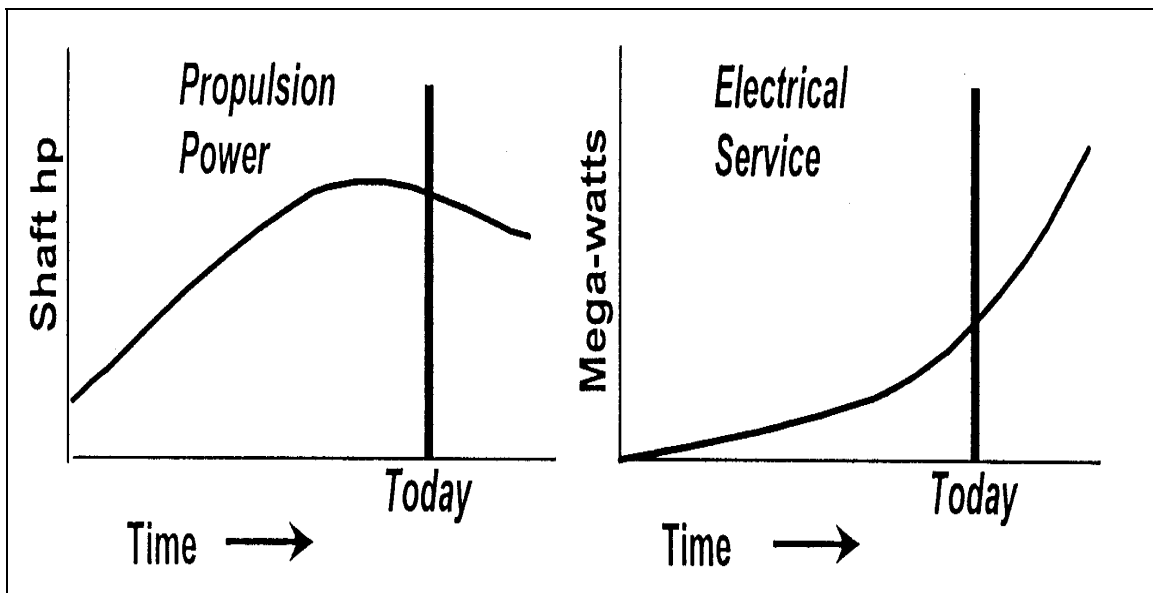


Figure 1-1. Shaft Horsepower and Electrical Power Needs (from ref. [3]).

Figure (1-1) shows that the amount of electrical power required is growing exponentially, while the required propulsion power is decreasing at a slower rate as ship designs progress. Modern combatants will be similar in size when compared to the current platforms, thus room for additional power generation systems will be at a premium. With power generation capability at its limits, the necessity to optimally redesign the electrical distribution system arises. Because of this growth in power requirements, the concept of an Integrated Power System (IPS) with a DC Zonal Electric Distribution System (DC ZEDS) has been developed.

1. IPS With DC ZEDS

An IPS is an electric power system which integrates power generation, electric propulsion, ship service distribution, combat system support and power management systems [3]. A block diagram of a basic IPS system is shown in Figure (1-2).

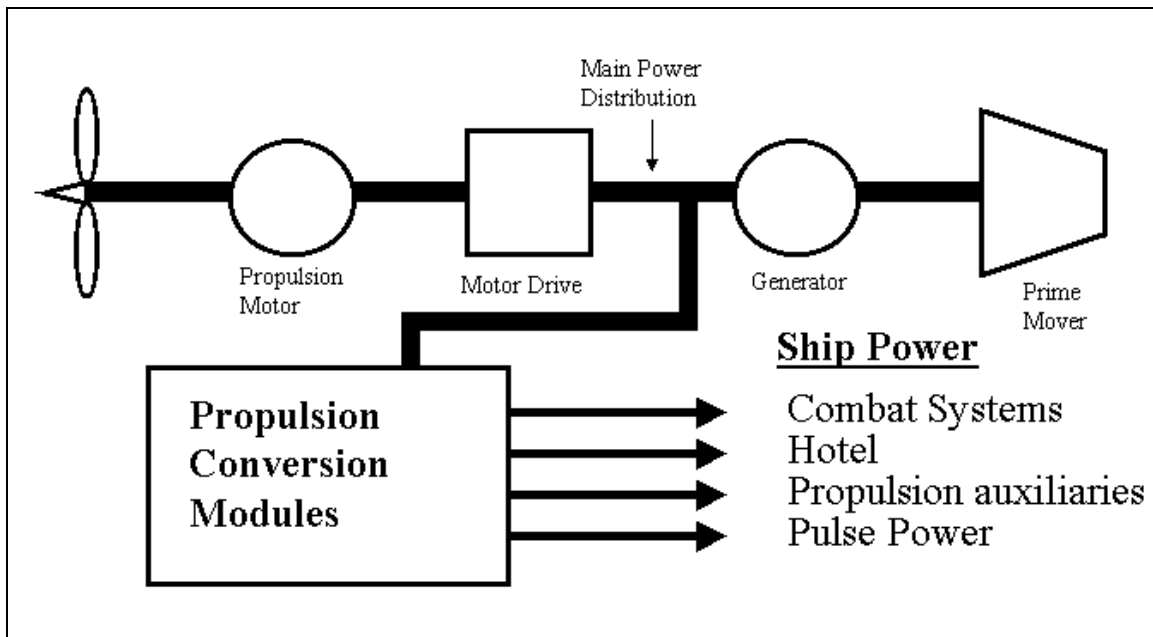


Figure 1-2. Block Diagram of Representative IPS System (after ref. [3]).

In a DC ZEDS IPS system, a standard prime mover such as a gas turbine or steam driven turbine drives an AC generator. The generator supplies multi-phase power that is

transformed and phase-control rectified to make DC power. The AC generator will also directly supply the propulsion converter, which will then rectify the multi-phase AC power and phase-invert back to a multi-phase variable-frequency AC for precise propulsion motor control. The rectified DC power then supplies the Power Conversion Modules (PCMs), which then deliver power to the remaining ship systems. The PCMs are made up of Ship Service Converter Modules (SSCM), which are DC-DC converters, and Ship Service Inverter Modules, which are DC-AC converters. DC power is distributed on port and starboard buses throughout the ship, conditioned by SSCMs and then converted to single-phase or three-phase AC power by SSIMs in the various zones depending on system power requirements.

The authors in reference [2] have recommended a DC distribution system over the common AC radial distribution system, due to the significant reductions in weight, quicker fault detection and improvements in continuity of power. The SSCMs in a particular zone will be diode-auctioneered together, thus providing fault isolation times in microseconds compared to isolation times of milliseconds for AC distribution systems using breakers. A ship designed around a DC ZEDS IPS system will also be able to rapidly shift power away from the propulsion system to supply large loads, such as pulse weapon system, and then shift power back to the propulsion system before the ship slows down. The flexibility of such a power system allows the commanding officer to direct the energy where it is needed operationally, instead of having a majority of the available power reserved for propulsion as with current ship designs.

The Naval Postgraduate School (NPS) has teamed with Purdue University, University of Missouri-Rolla, University of Wisconsin-Milwaukee and the United States Naval Academy to form the Energy Sources Analysis Consortium (ESAC). The ESAC researchers are presently interested in the study of DC ZEDS and other alternate power distribution systems such as high-frequency AC zonal distribution.

2. Laboratory-Scale DC ZEDS Research

The ESAC researchers have outlined the design of a reduced-scale laboratory DC ZEDS in reference [4]. The researchers proposed the construction of a three-zone

distribution system with a rating of 15kW. The laboratory-scaled DC ZEDS diagram is illustrated in Figure (1-3).

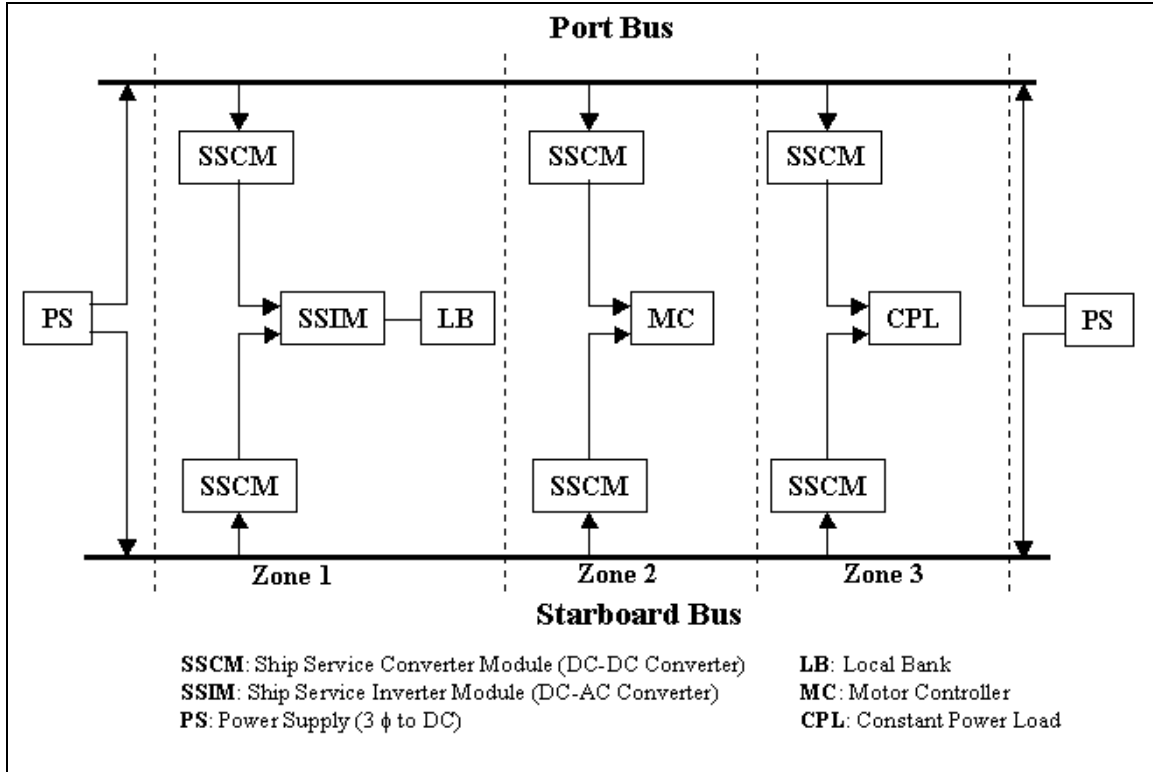


Figure 1-3. Laboratory-Scale DC ZEDS (from ref. [4]).

Each zone in Figure (1-3) performs a task similar to what a typical full-scale DC ZEDS would perform. In zone 1, DC power from the port and starboard bus is conditioned to a lower voltage level by SSCMs and converted to three-phase AC by the SSIM. The SSIM then supplies a load bank, which allows the researcher to study the effects of varying load condition and the interaction between the two types of converters. In zone 2, DC power from the port and starboard buses is once again conditioned by SSCMs and the voltage is lowered to supply a motor controller. The motor controller can then drive a motor representative of what would be used in the ship's hydraulic or high-pressure air systems. Finally, zone 3 uses SSCMs to drive a constant power load so that SSCM stability and paralleling issues can be addressed.

Researchers at the Naval Postgraduate School have conducted extensive research in the area of DC-DC converters and, as a result, NPS was selected to develop the SSCM for the reduced-scale DC ZEDS. A hard-switched SSCM was designed, built and tested at NPS for ESAC's reduced-scale prototype DC ZEDS and the results are documented in reference [5].

3. SSCM Description

The SSCM serves as an interface between the main DC supply and zonal loads and regulates the output voltage at a level required by the SSIMs. Since the output voltage of the SSCM will always be less than the input voltage, a buck chopper (buck DC-DC converter) configuration is required. The classical buck chopper circuit is illustrated in Figure (1-4).

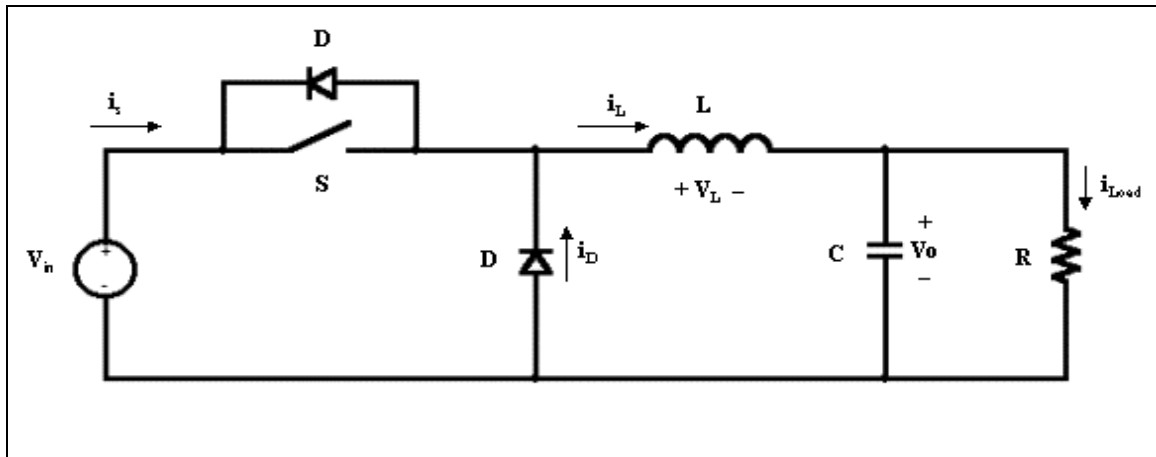


Figure 1-4. Classical Buck Chopper (DC-DC Converter).

A voltage, V_o , proportional to the input voltage is developed across the load by controlling the duty cycle of switch S and selecting appropriate component values for inductor L and capacitor C . To minimize filter size and audible noise and to maximize control bandwidth, the switch is typically operated at frequencies in excess of 20 kHz [2]. All real semiconductor switches have conduction losses and switching losses. The conduction losses remain constant for a given load, but the switching losses increase

proportionately with the switching frequency. Each time a switch is closed with a voltage across it, losses occur as the switch begins to conduct current. When the switch is opened again, current will continue to flow until the voltage across the switch builds up to the blocking voltage. For both the turn-on and turn-off case, significant power loss occurs, which can easily exceed the conduction loss as the switching frequency is increased. In the pursuit of a smaller more compact converter design, a point is reached where the switching losses become excessive and soft-switching converter topologies become viable options.

4. Soft-Switching SSCM Overview

A soft-switching converter (also called a resonant converter) is broadly defined as a converter where additional switches, diodes, capacitors and/or inductors are added to create a zero voltage or current condition by LC resonance action before the switch is operated. All resonant DC-DC converters can be placed in either of the two following classes of converters:

- Load-resonant converters, and
- Resonant-switch converters.

Load-resonant converters control the power flow to the load by resonant tank impedance, which is in turn controlled by the switching frequency or the resonant frequency [6]. Having to design a control system that changes the switching frequency as a function of loading is difficult and, as such, these classes of converters are not attractive for DC ZEDS. The component-fixed resonant frequency is even more difficult to change.

Conversely, resonant-switch converters use an LC resonance to shape the voltage and current waveforms to minimize the turn-on and turn-off losses. Reference [6] further divides the resonant-switch converter into the following categories:

- Zero-Voltage Switching (ZVS)
- Zero-Current Switching (ZCS)
- Zero-Voltage Switching, Clamped Voltage (ZVS-CV).

Resonant-switch converters have the advantage that they are less sensitive to load changes and fixed-frequency Pulse-Width-Modulation (PWM) control schemes can be used on a number of these topologies.

5. Soft-Switching Converter Literature Overview

The authors in references [7] and [8] conducted a comprehensive study of many different resonant-switch DC-DC converters and ranked them on their ease of control, estimated efficiency and simplicity. Converter topologies that simply added external components to the classical converter illustrated in Figure (1-4) received consideration, as did converters requiring a constant or varying switching frequency control scheme. The dual source converter described in reference [9] offered a good design, but was not considered for this thesis, as the DC ZEDS will be a single source power system. The most notable single source converter topologies considered are listed in order of their publication date.

- A two-switch PWM ZVS-ZCS converter that uses a feedback auxiliary circuit that feeds off of the load [10].
- A two-switch PWM ZVS converter with two switches in the main current path and the capability to operate over wide load ranges [11].
- A two-switch ZVS quasi-resonant where the output voltage is regulated by the freewheeling period of the resonant inductor [12].
- A single-switch ZVS-CV requiring frequency control [13].
- A two-switch PWM ZVS-ZCS converter that achieves ZVS in the main switch and ZCS in the auxiliary switch [14].
- A two-switch PWM ZVS converter with both a diode and switch in the main current path [15].

The Joung converter described in reference [14] has the advantage that no resonant components are placed in series with the main switch and that the topology is a simple extension of the basic buck converter. The converter also has the added benefit

that constant frequency PWM control is feasible. In reference [8], a low-power simulation of the Joung converter was conducted with good results. The converter was also built and tested using bulky lab inductors and capacitors with a low switching frequency of 2 kHz and efficiencies between 94 to 95% were documented.

6. Joung Resonant Converter Topology

The Joung resonant converter circuit is shown in Figure (1-5). The design is a simple extension of the classical buck converter of Figure (1-4) with no additional resonant components in the main current path. All of the additional resonant components are contained in the dotted box.

The main switch S_m is operated in a ZVS condition and the auxiliary switch S_a is operated in a ZCS condition. The design is easily controlled with a constant-frequency PWM control system and should yield good efficiencies with only one switch in the main current path. Based on the review of many resonant topologies and the past research at NPS, the Joung converter has been selected as the topology of choice for the research in this thesis.

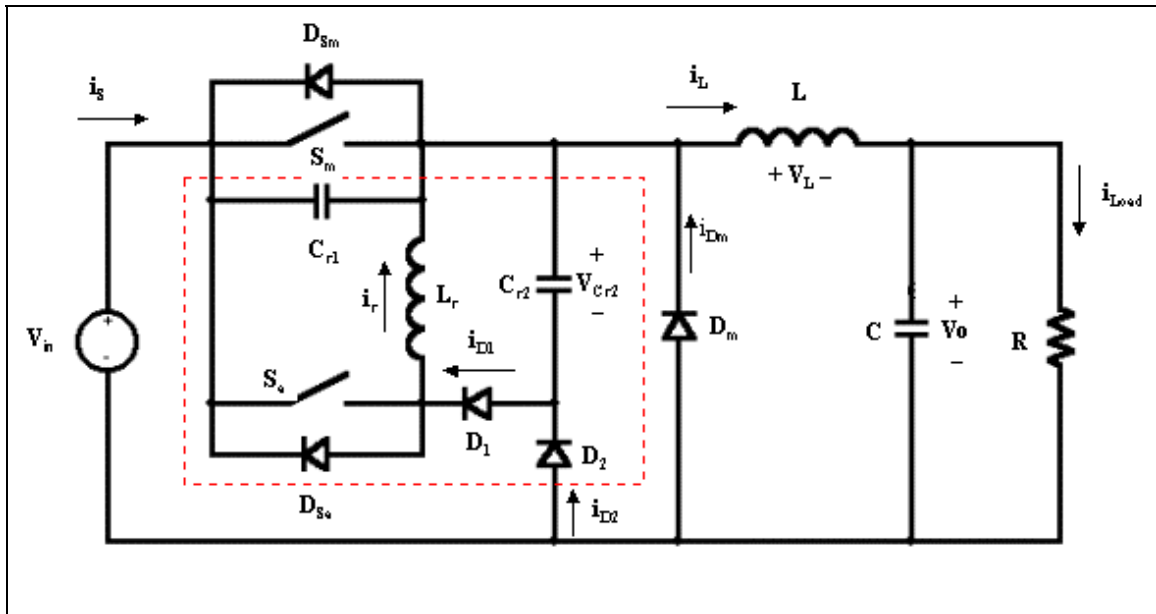


Figure 1-5. Joung Resonant Converter Topology.

B. THESIS OBJECTIVES

The objective of this thesis is to design, construct and test a resonant soft-switching DC-DC converter and compare the results obtained for the hard-switched DC-DC converter in reference [5]. In theory, the resonant converter should yield a more compact design with the capability of higher power densities due to an increase in efficiency. The conducted Electromagnetic Interference (EMI) will also be measured and compared to the hard-switched converter to see if the common belief that soft-switched converters have reduced EMI is correct for this topology. Based on the results, a recommendation will be made as to whether the design is a suitable replacement for the simpler hard-switched DC-DC converter for use as the SSCM in the reduced-scale DC ZEDS laboratory.

C. CHAPTER OVERVIEW

In Chapter II, the resonant converter design is described mathematically using differential equations, and circuit operation is broken down into the different modes of operation. Chapter III contains a description of the circuit design based on the dynamics of Chapter II, and a detailed circuit simulation is performed to verify the circuit theory. The simulation will also be used to estimate the converter's efficiency. Next, the converter construction and testing results are covered in Chapter IV. The results in Chapter IV will show that optimization is warranted, and Chapter V documents the optimization methodology and test results. Chapter VI covers the EMI testing performed on the hard-switched and soft-switched converter. EMI testing is also conducted on the optimized resonant converter and the results are compared to the earlier tests. Chapter VII contains the concluding remarks and recommendations based on the testing in Chapters IV, V and VI.

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II. PRINCIPLES OF OPERATION

A. ANALYSIS OF OPERATING MODES

To best understand the Joung resonant converter [14], the steady-state circuit operation can be broken down into eight distinct operational modes, which occur in one switch cycle. Each mode of operation will be explained and then, in section B, differential equations will be written to mathematically describe the circuit operation. For the following figures in Section A, a red trace depicts a principle current path and a light gray trace indicates an inactive circuit path.

1. Mode 1

The first mode is depicted in Figure (2-1). In this mode, both the main switch S_m and the auxiliary switch S_a are "off." The main diode D_m is conducting and the inductor current is ramping downward with approximately $-V_C$ across it. Since D_m is conducting, the top rail to the left of the main inductor is essentially at ground potential, and thus, C_{r1} is charged to V_{dc} . The resonant inductor L_r has no current flowing through it and C_{r2} is fully discharged. Mode 1 continues until $i_L = I_{L,min}$ and the auxiliary switch is activated

2. Mode 2

With the closing of S_a , while D_m is still conducting, the voltage across L_r is approximately V_{dc} . With an inductor in series, S_a is closed in a Zero-Current Switching (ZCS) condition. Since $\frac{d}{dt}i_r = \frac{V_{dc}}{L_r}$, i_r quickly ramps up until $i_r = i_L$, which is close to $I_{L,min}$. The main diode, D_m , is now starved of current and turns "off." The node to the left of the main inductor is no longer tied to ground potential, thus C_{r1} is no longer tied to the ground rail and V_{Cr1} is free to change. Mode 2 operation is shown in Figure (2-2).

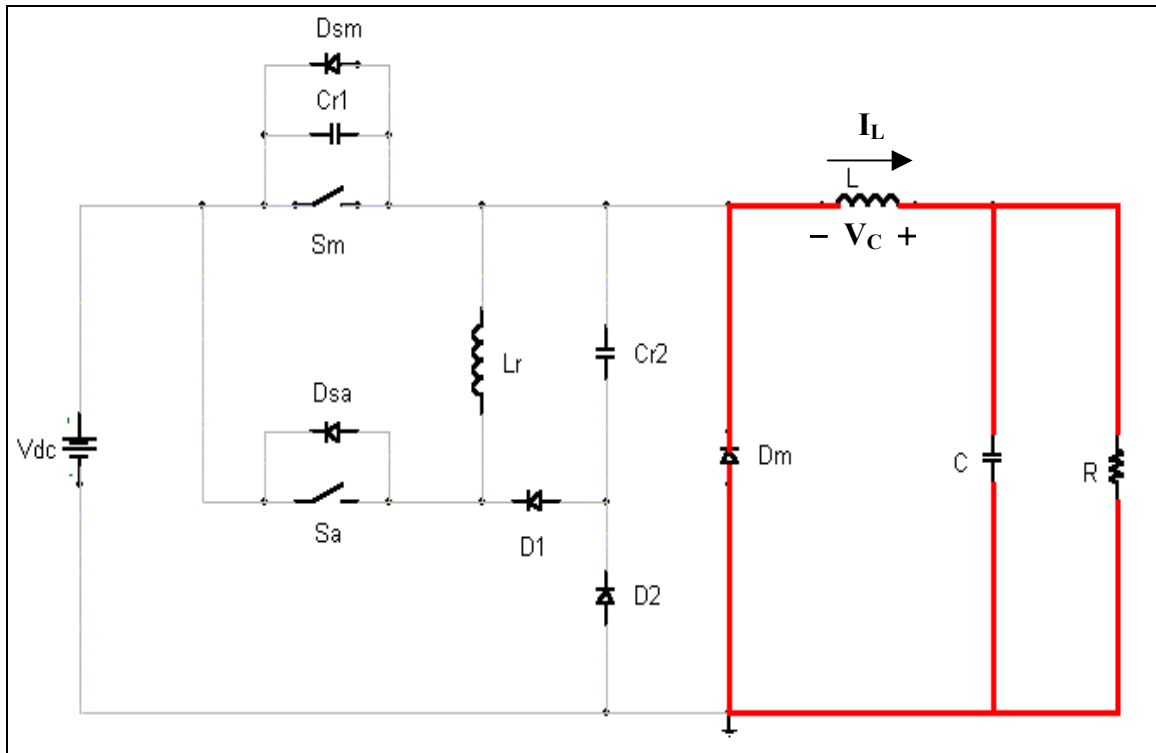


Figure 2-1. Mode 1 Operation.

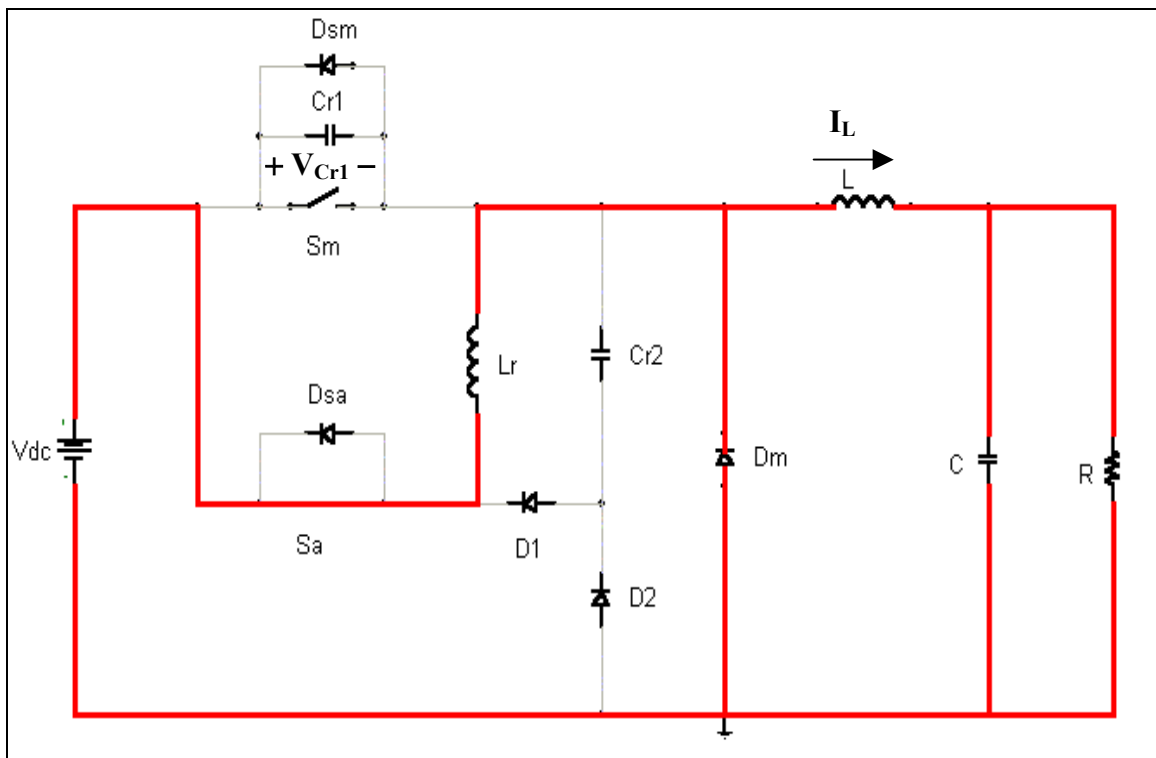


Figure 2-2. Mode 2 Operation.

3. Mode 3

With V_{Cr1} free to change, a resonant condition is set up between C_{r1} and L_r as illustrated in Figure (2-3). The resonant action between C_{r1} and L_r drives V_{Cr1} down to 0V. As the resonant action tries to recharge C_{r1} , diode D_{Sm} clamps the voltage at approximately -1 volt, so V_{Cr1} ends up being no greater than 1 volt as illustrated in Figure (2-4). The zero-voltage condition for turn-on is now established for the main switch.

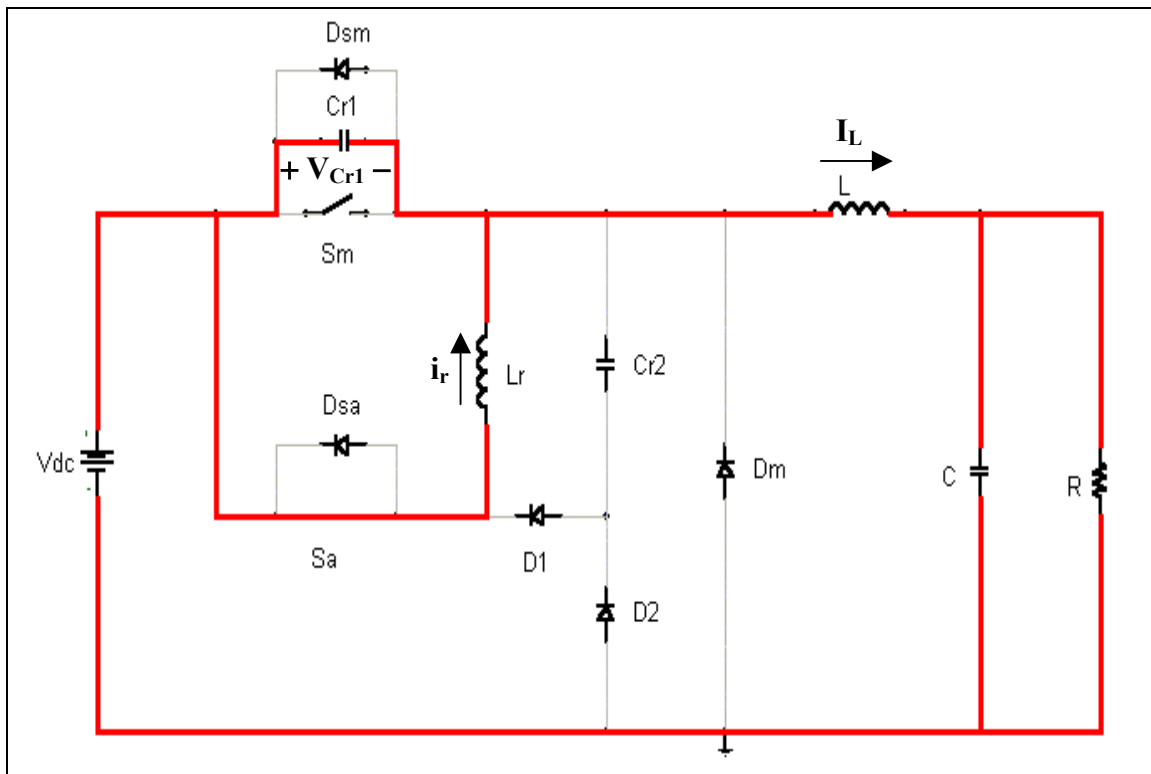


Figure 2-3. Mode 3 Operation.

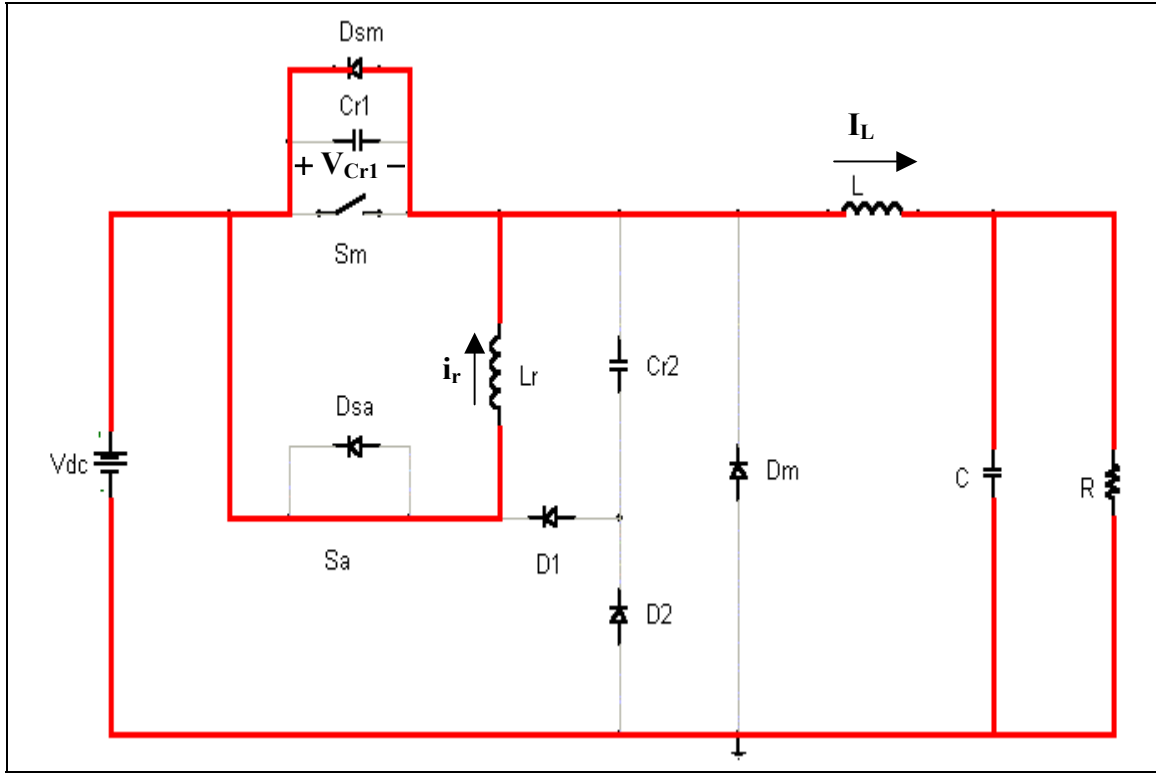


Figure 2-4. Mode 3 Operation (clamping of V_{Cr1}).

4. Mode 4

The main switch, S_m , is now closed with V_{Cr1} at approximately zero volts. This mode is depicted in Figure (2-5). With S_m conducting, C_{r1} is clamped at near zero volts and S_m starts to assume conduction of a small portion of I_L . Since L_r is effectively in parallel with a closed switch, the voltage across the inductor is approximately zero and thus i_r is held constant. This ensures that I_{Sm} will linearly follow the buildup in I_L . With S_m gated "on" with zero volts across it, the auxiliary switch, S_a , can now be turned "off."

5. Mode 5

The auxiliary switch S_a is now opened transferring the remainder of I_L to the main switch. Since i_r cannot change instantaneously, diode D_1 is forward biased "on" and L_r starts to charge C_{r2} . The resonant loop formed by L_r and C_{r2} drives i_r to zero and D_1 is starved of current. At this time, all of the main inductor current is carried by S_m . Mode 5 operation is shown in Figure (2-6).

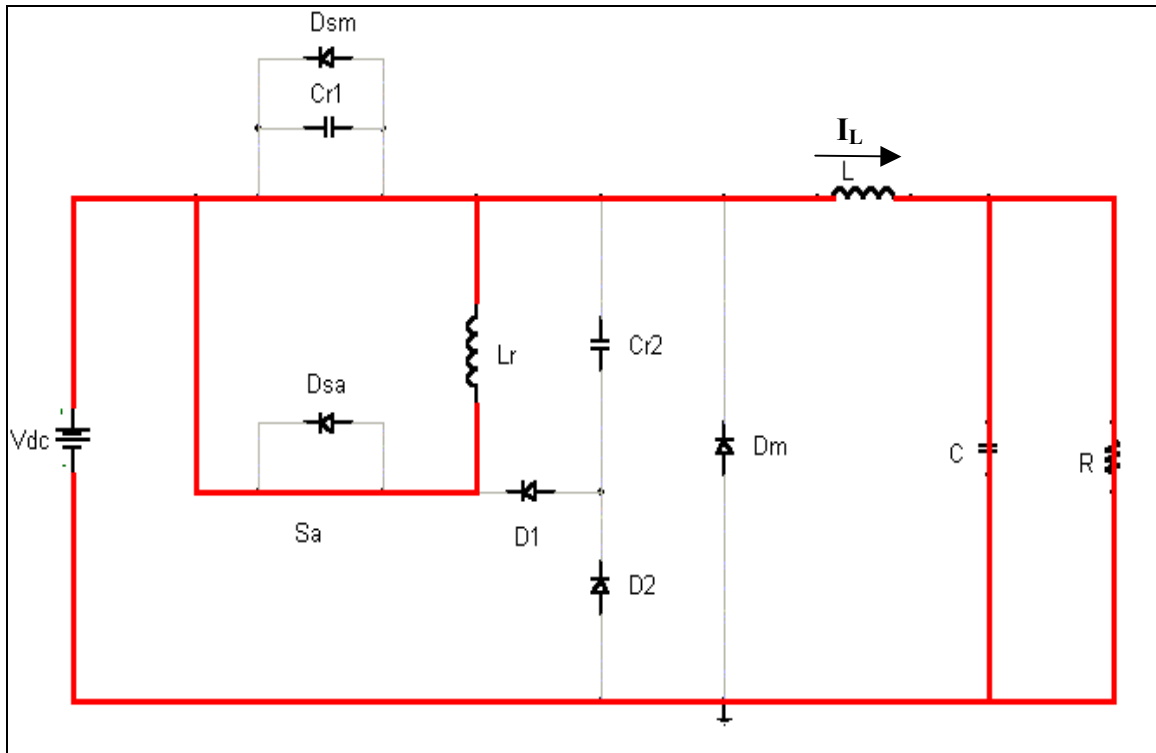


Figure 2-5. Mode 4 Operation.

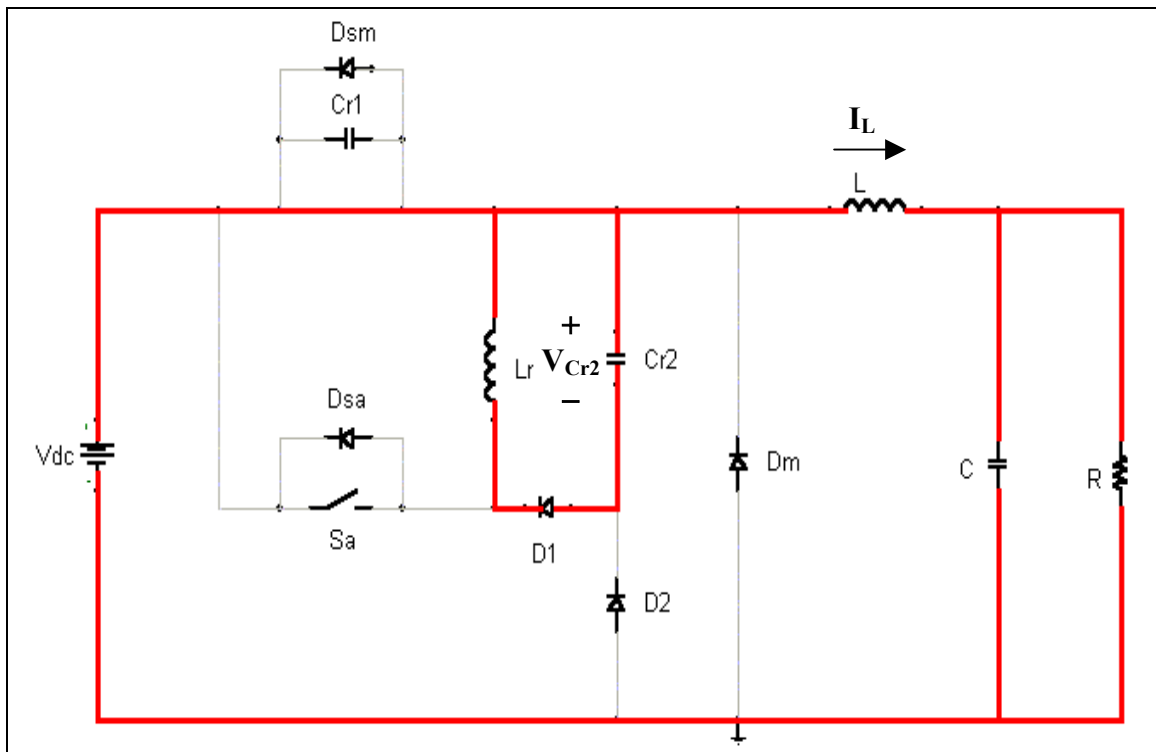


Figure 2-6. Mode 5 Operation.

6. Mode 5x

If the resonant action of L_r and C_{r2} tries to charge C_{r2} above V_{dc} , diode D_2 is forward biased and the equation $\frac{d}{dt}i_r = \frac{-V_{dc}}{L_r}$ holds true. The resonant current quickly decays to zero and V_{Cr2} is frozen at approximately V_{dc} . This mode is depicted in Figure (2-7).

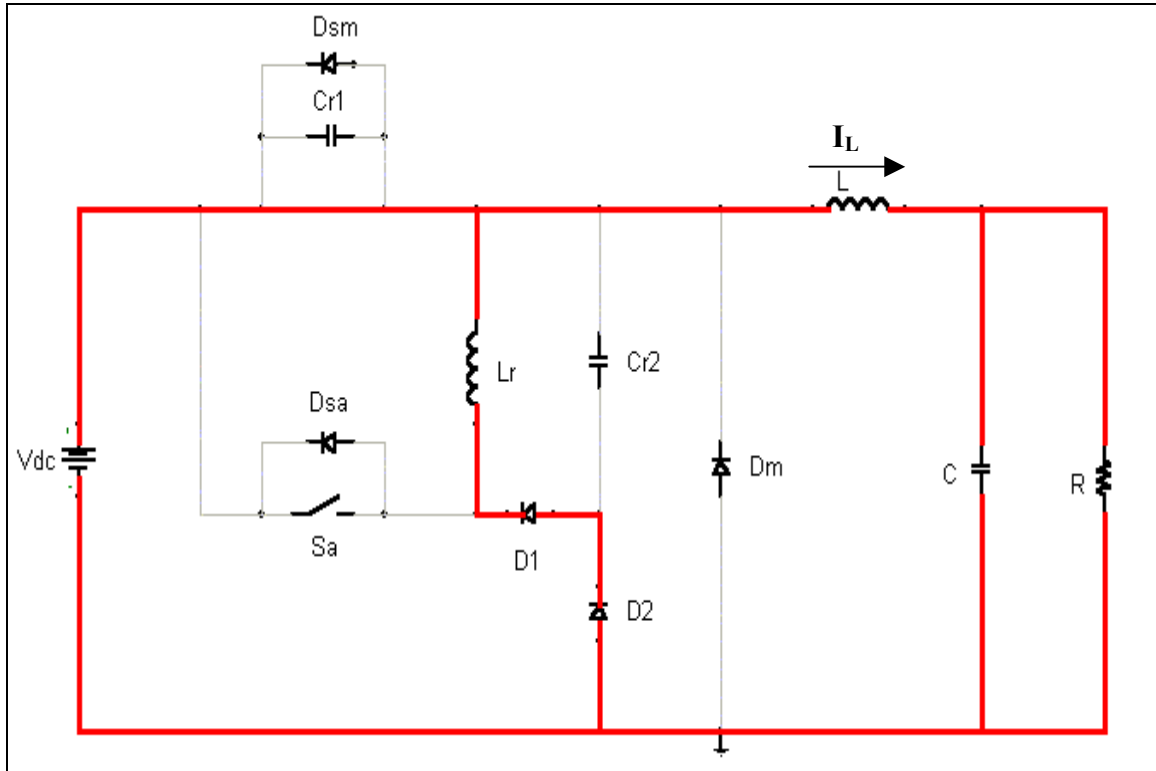


Figure 2-7. Mode 5x Operation.

7. Mode 6

In mode 6, the current paths are shown in Figure (2-8). This mode corresponds to the time period when S_m carries the inductor current as dictated by the duty cycle. Mode 6 operation in the resonant buck converter is the same as in a hard-switched buck converter when the main switch is conducting. The resonant capacitor voltage V_{Cr2} is charged to a value between zero and V_{dc} and the resonant inductor current is zero. Mode 7 or 8 occurs next when the main switch S_m is opened and the circuit transitions to a state

required for the subsequent firing of the auxiliary switch S_a . If V_{Cr2} is less than V_{dc} , operation is described by mode 7; otherwise, mode 8 operation occurs.

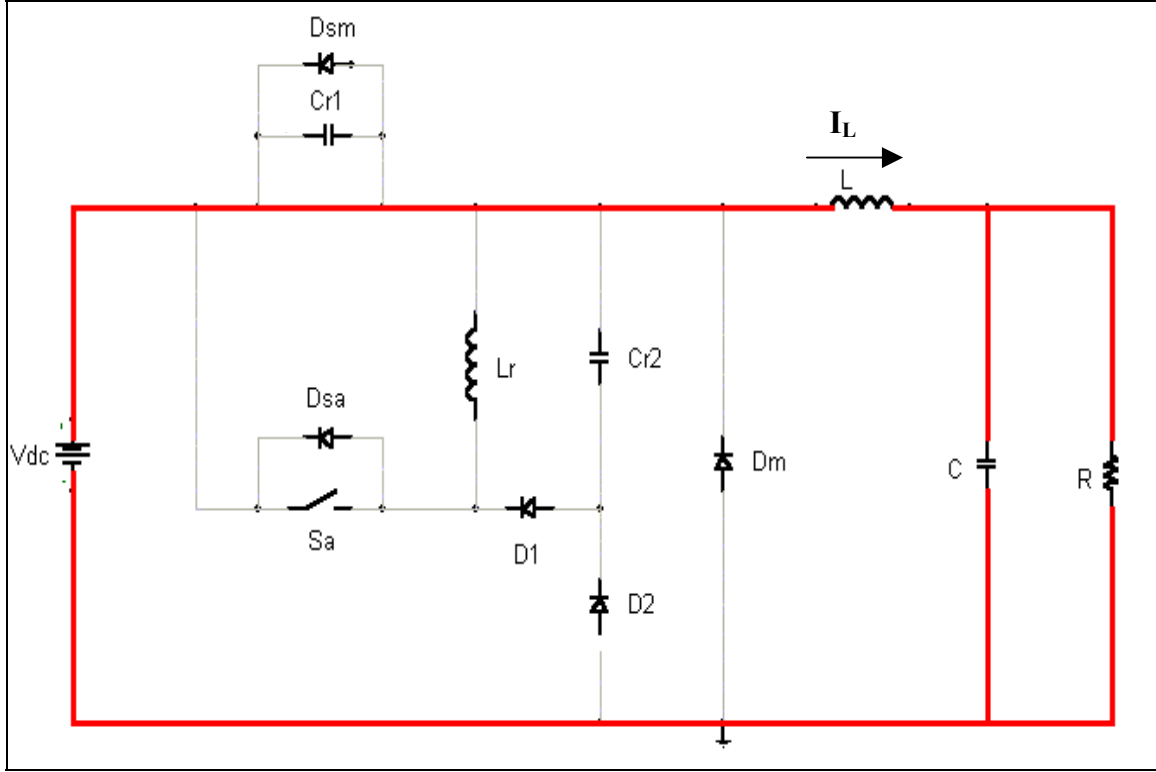


Figure 2-8. Mode 6 Operation.

8. Mode 7

Just before the main switch is opened, the resonant capacitor, C_{r1} , has zero volts across it. When S_m is opened, the main inductor current must remain the same and thus the current flows through C_{r1} . Since $V_{D2} = V_{Cr1} + V_{Cr2} - V_{dc}$, the charging of C_{r1} will eventually cause D_2 to become forward biased as seen in Figure (2-9). When D_2 is forward biased, the circuit operation transitions to mode 8.

9. Mode 8

Now that $V_{D2} = V_{Cr1} + V_{Cr2} - V_{dc}$ with C_{r1} charging and D_2 conducting, the circuit paths of Figure (2-10) govern operation. Using Kirchhoff's voltage law, $V_{Cr1} + V_{Cr2} = V_{dc}$, so as C_{r1} is charging, C_{r2} must be discharging. Mode 8 completes when V_{Cr1} charges slightly past V_{dc} and V_{Cr2} is approximately zero volts. Mode 1 operation commences when C_{r1} charges past V_{dc} and the main diode D_m is forward biased since $V_{Dm} = V_{Cr1} - V_{dc}$. The main diode picks up all of the main inductor current and mode 1 recommences.

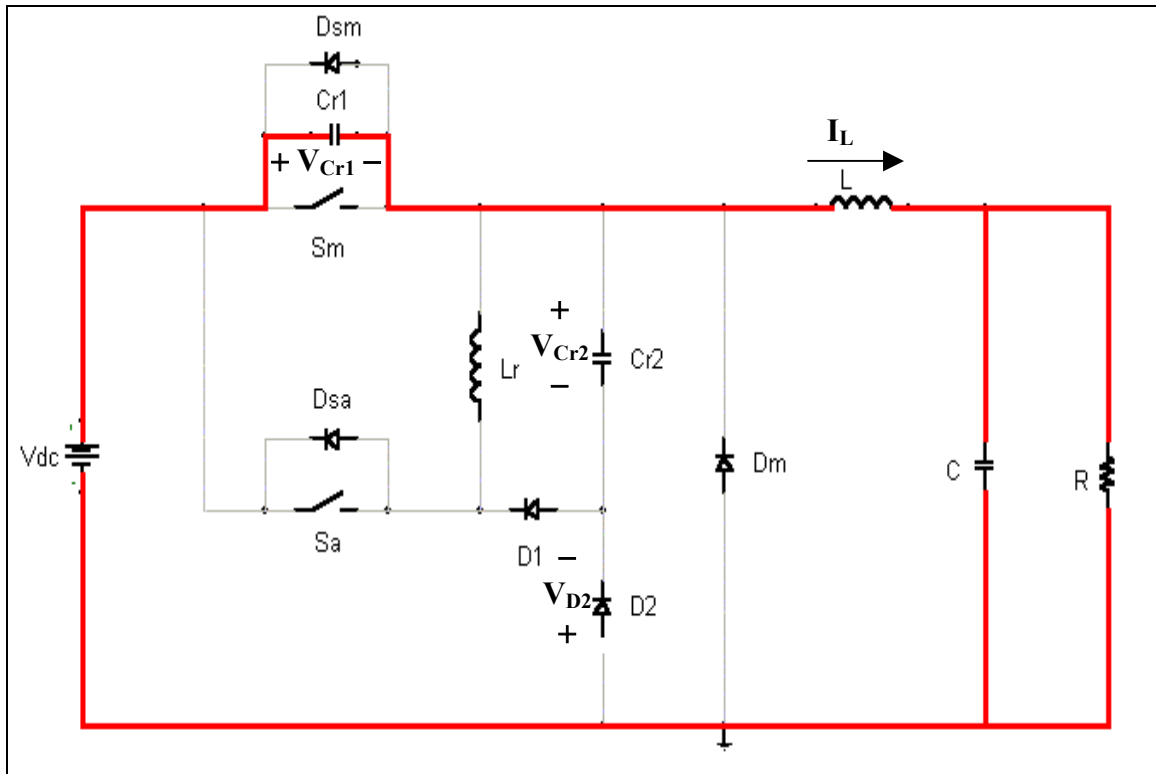


Figure 2-9. Mode 7 Operation.

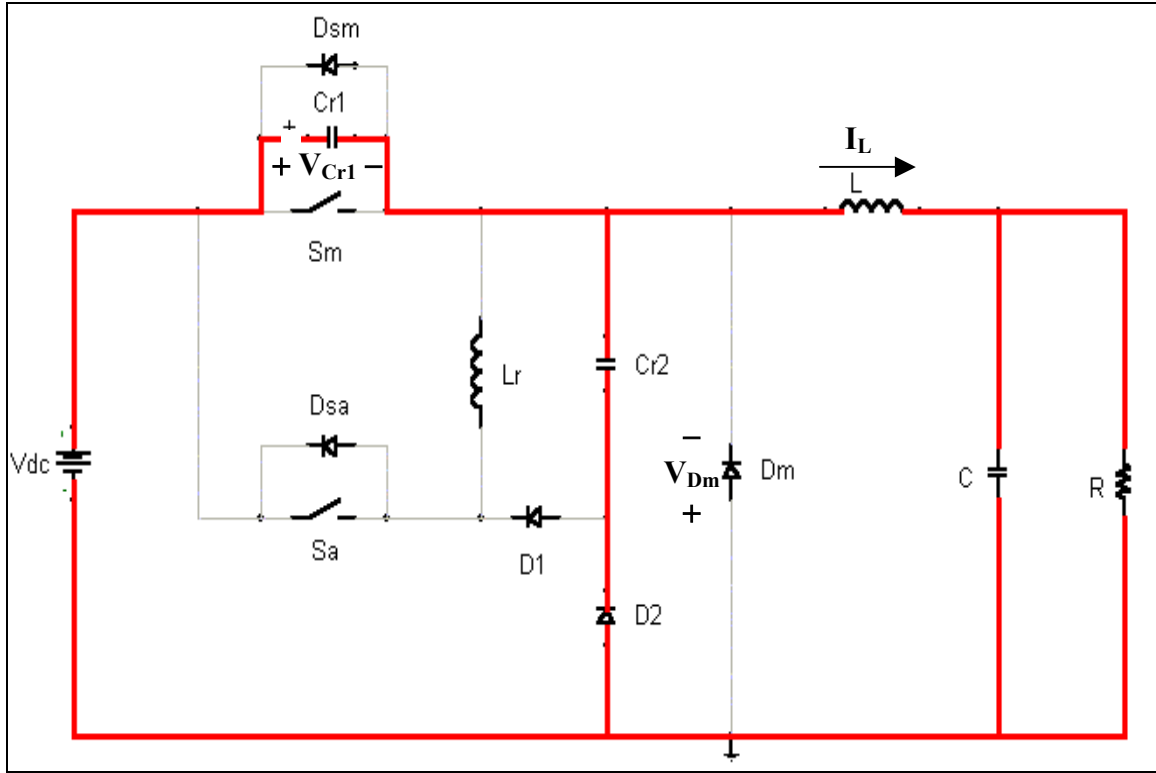


Figure 2-10. Mode 8 Operation.

B. DYNAMIC MODEL ANALYSIS

In order to fully understand the operation of the Joung soft-switching converter, differential equations for each of the eight modes are developed. Developing these equations is imperative if one wants to model the buck converter in a software package like the Advanced Continuous Simulation Language (ACSL). The differential equations are also needed to design the resonant converter on paper, so that proper component values can be calculated. In this thesis, the converter was modeled and simulated using PSPICE, since an estimate of switch loss and overall efficiency was needed. No ACSL simulation was performed, as it would only give qualitative plots of the input and output signals and not the detailed results of a good PSPICE simulation. In a paper written by Ciezki and Ashton [7], the authors conducted a simulation of this circuit and were only able to verify the gross attributes using ACSL and later used a PSPICE simulation to model the circuit. An ACSL or Simulink simulation would be beneficial in analyzing a control system interfaced with this converter as was done for a hard-switched buck converter in reference [5].

1. Mode 1

The dynamics of mode 1 are developed from the circuit in Figure (2-1), which is when the main diode is forward biased "on" for the period determined by the duty cycle.

$$\frac{d}{dt} i_L = -\frac{V_c}{L} \quad (2-1)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-2)$$

$$\frac{d}{dt} i_r = 0 \quad (2-3)$$

$$\frac{d}{dt} V_{Cr1} = 0 \quad (2-4)$$

$$\frac{d}{dt} V_{Cr2} = 0 \quad (2-5)$$

2. Mode 2

The dynamics of mode 2 are now derived by analyzing Figure (2-2). In this mode, the auxiliary switch, S_a , has now been gated "on." The following equations represent the circuit operation until $i_r = i_L$ at which time mode 3 operation occurs.

$$\frac{d}{dt} i_L = -\frac{V_c}{L} \quad (2-6)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-7)$$

$$\frac{d}{dt} i_r = \frac{V_{dc}}{L_r} \quad (2-8)$$

$$\frac{d}{dt} V_{Cr1} = 0 \quad (2-9)$$

$$\frac{d}{dt} V_{Cr2} = 0 \quad (2-10)$$

3. Mode 3

With S_a fully "on" and D_m starved of current, V_{Cr1} is now free to change and will resonate with L_r . This is depicted in Figure (2-3) and the following equations model this mode.

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c - V_{Cr1}}{L} \quad (2-11)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-12)$$

$$\frac{d}{dt} i_r = \frac{V_{Cr1}}{L_r} \quad (2-13)$$

$$\frac{d}{dt} V_{Cr1} = \frac{i_L - i_r}{C_{r1}} \quad (2-14)$$

$$\frac{d}{dt} V_{Cr2} = 0 \quad (2-15)$$

4. Mode 4

The closure of the main switch as dictated by the duty cycle initiates mode 4. The dynamics are derived using Figure (2-5).

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c}{L} \quad (2-16)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-17)$$

$$\frac{d}{dt} i_r = 0 \quad (2-18)$$

$$\frac{d}{dt} V_{Cr1} = 0 \quad (2-19)$$

$$\frac{d}{dt} V_{Cr2} = 0 \quad (2-20)$$

5. Mode 5

Mode 5 is initiated when the auxiliary switch is opened as shown in Figure (2-6). The turn-off time may be based on the value of a sensed variable or timing criterion. Chapter III of this thesis will discuss choosing turn-off times based on circuit timing. The dynamics are developed using Figure (2-6).

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c}{L} \quad (2-21)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-22)$$

$$\frac{d}{dt} i_r = -\frac{V_{Cr2}}{L_r} \quad (2-23)$$

$$\frac{d}{dt} V_{Cr1} = 0 \quad (2-24)$$

$$\frac{d}{dt} V_{Cr2} = \frac{i_r}{C_{r2}} \quad (2-25)$$

The dynamics of mode 5 govern until i_r decays to zero or if V_{Cr2} reaches V_{dc} . If V_{Cr2} reaches V_{dc} , then the dynamics of mode 5x dictate operation as shown in Figure (2-7).

6. Mode 5x

If V_{Cr2} tries to rise above V_{dc} , V_{Cr2} will be clamped to V_{dc} and Equations (2-26) and (2-27) will model the dynamics.

$$\frac{d}{dt} V_{Cr2} = 0 \quad (2-26)$$

$$V_{Cr2} = V_{dc} \quad (2-27)$$

As L_r continues to discharge into the circuit, Equation (2-28) still holds true.

$$\frac{d}{dt} i_r = -\frac{V_{Cr2}}{L_r} \quad (2-28)$$

Mode 5x continues until i_r goes to zero.

7. Mode 6

Mode 6 is characterized as the mode where the main switch carries the full load current. The following equations are derived from Figure (2-8).

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c}{L} \quad (2-29)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-30)$$

$$\frac{d}{dt} i_r = 0 \quad (2-31)$$

$$\frac{d}{dt} V_{Cr1} = 0 \quad (2-32)$$

$$\frac{d}{dt} V_{Cr2} = 0 \quad (2-33)$$

The voltage across C_{r2} remains constant between zero and V_{dc} and i_r continues to equal zero. Mode 6 continues until the main switch is opened.

8. Mode 7

As shown in Figure (2-9), if V_{Cr2} is less than V_{dc} when the main switch is opened, then the following dynamic equations hold true.

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c - V_{Cr1}}{L} \quad (2-34)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-35)$$

$$\frac{d}{dt} i_r = 0 \quad (2-36)$$

$$\frac{d}{dt} V_{Cr1} = \frac{i_L}{C_{r1}} \quad (2-37)$$

$$\frac{d}{dt} V_{Cr2} = 0 \quad (2-38)$$

These dynamics continue until $V_{Cr1} + V_{Cr2} = V_{dc}$. When this occurs, diode D_2 is forward biased, begins to conduct, and the equations of mode 8 govern operation.

9. Mode 8

The following dynamic equations were found upon analyzing Figure (2-10).

$$\frac{d}{dt} i_L = \frac{V_{Cr2} - V_c}{L} \quad (2-39)$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \quad (2-40)$$

$$\frac{d}{dt} i_r = 0 \quad (2-41)$$

$$\frac{d}{dt} V_{Cr1} = \frac{i_L}{C_{r1} + C_{r2}} \quad (2-42)$$

Since D_2 is forward biased, V_{Cr2} is constrained by $V_{Cr2} = V_{dc} - V_{Cr1}$ until $V_{Cr1} = V_{dc}$ at which point circuit operation shifts back to mode 1 as shown in Figure (2-1).

C. CHAPTER SUMMARY

In this chapter, the 8 basic modes of operations were developed along with the dynamic equations. Next, these results are used to derive an initial design, which will then be verified with a PSPICE simulation. Different families of semiconductor switches are investigated and a suitable device will be chosen for this design.

III. INITIAL DESIGN AND SIMULATION

A. SPECIFICATIONS

As stated in Chapter I, the goals of this thesis are to design, build and test a resonant soft-switching DC-DC converter, which could meet the specifications outlined in reference [4]. This reference called for the construction of a reduced-scale DC ZEDS test bed with three zones as depicted in Figure (1-3). A major component of the DC ZEDS is the Ship Service Converter Module (SSCM), which is a DC-DC buck converter. A recent thesis described in detail the design and construction of a hard-switched SSCM [5]. The resonant SSCM described in this thesis was designed, built and tested along with the hard-switched SSCM so that some meaningful comparisons could be documented. The specifications for the resonant SSCM are listed in Table (3-1).

Parameter:	Specification:
Rated Continuous Output Power	8kW
Switching Frequency (f_s)	20kHz
Input Voltage (V_{dc})	500 V_{dc}
Output Voltage (V_c)	400 V_{dc} (duty cycle=80%)
Continuous-Conduction Load Range	10% ($R_L=200\Omega$) to 100% ($R_L=20\Omega$)
Steady-State Output Voltage Ripple (V_{pp})	< 1%

Table 3-1. SSCM Specifications.

B. RESONANT CONVERTER DESIGN

For the resonant buck converter, the designer must choose the correct component values so that proper circuit operation occurs. The components can be divided into two groups: the ones that make up the core of the soft-switching circuitry and the other components necessary for the classical hard-switched buck converter. The resonant converter is shown in Figure (3-1). The additional resonant components are contained

inside the dashed area of Figure (3-1), where C_{r1} is simply the body capacitance of the main switch.

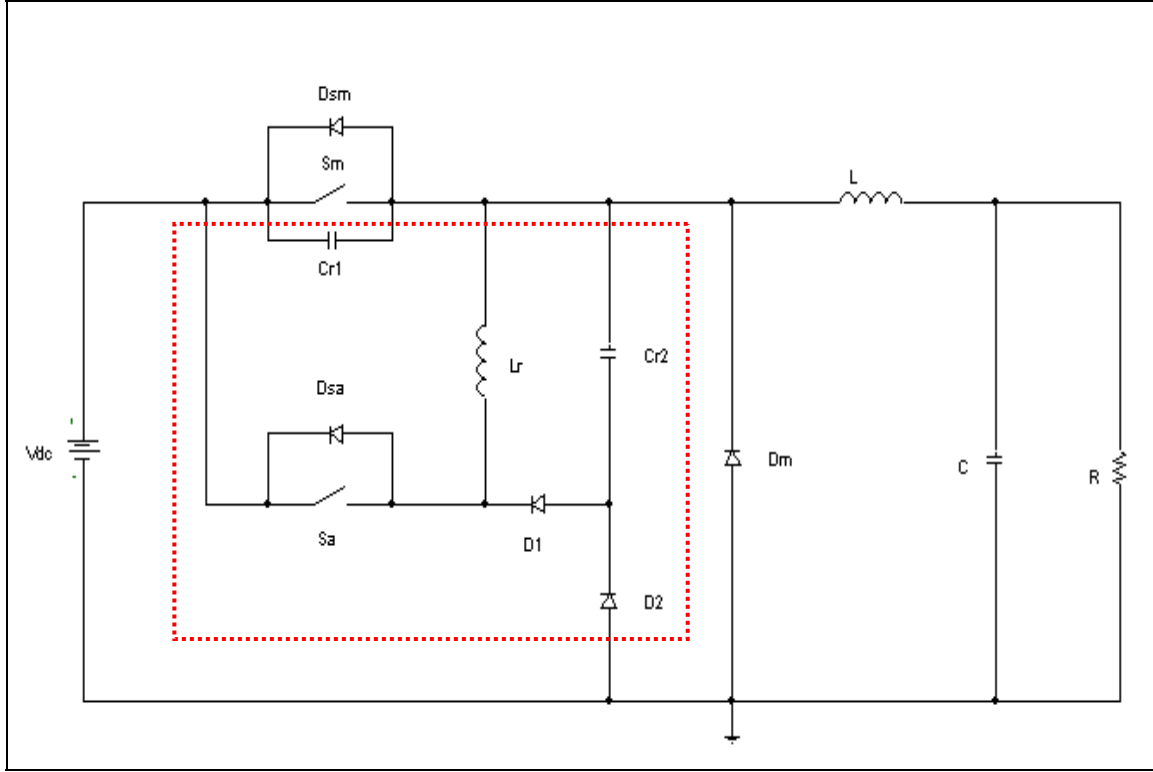


Figure 3-1. Resonant Converter Circuit.

Since this converter design is much the same as the basic buck converter with an additional switch, resonant capacitors and a resonant inductor, the proper place to initiate the design process is the selection of the proper values of the main inductor and capacitor.

1. Selection of Main Inductor and Main Capacitor

The determination of the main inductor L and capacitor C is well understood and the requirements are based on switching frequency, load resistance, duty cycle and maximum ripple voltage. The duty cycle is defined by dividing the desired output voltage by the anticipated input voltage to the converter.

$$D = \frac{V_{out}}{V_{dc}} = \frac{400}{500} = 0.8 \quad (3-1)$$

The critical load resistance is defined as being the load that will demand 10 percent of the full-load power. The range of load resistance values is listed in Table (3-1).

$$R_{\text{crit}} = 10R_{\text{rated}} = 200\Omega \quad (3-2)$$

The critical inductance is the minimum inductance required so that continuous-current operation occurs. The more limiting case is when the load power is 10 percent of full load and $R=R_{\text{crit}}$. The critical inductance for the minimum loading condition is found to be

$$L_{\text{crit}} = \frac{R_{\text{crit}}}{2f_s}(1-D) = 1.0\text{mH} \quad (3-3)$$

where f_s is the switching frequency. The minimum filter capacitance is found by using Equation (3-4),

$$C_{\text{min}} = \frac{D}{8Lf_s^2\Delta V_{\text{out}}}[V_{\text{dc}} - V_{\text{out}}] = 6.25\mu\text{F} \quad (3-4)$$

where ΔV_{out} is the allowed 1 percent of the output voltage steady-state peak-to-peak ripple. This is a rather small amount of filtering capacitance and a greater amount of capacitance is required to handle load transients. Selecting too large a value of capacitance will cause the control circuit duty cycle signal to oscillate between a full-on and full-off condition whenever a load variation occurs. An output filtering capacitance of $500\mu\text{F}$ was selected as it is a reasonable value and provides a good energy capacity match with the main inductor.

Another important parameter needed for selecting the proper filtering capacitor and the resonant components is the main inductor ripple current. For rated load, the minimum steady-state inductor current is found using Equation (3-5). For Equations (3-5) and (3-6), a value of $500\mu\text{H}$ is used for L , as a 50 percent reduction in inductance occurs at full load. This decrease in inductance is discussed in Chapter IV.

$$I_{L,\text{min}} = \frac{V_{\text{out}}}{R_{\text{rated}}} \left[1 - \frac{R}{2Lf_s}(1-D) \right] = 16.0\text{A} \quad (3-5)$$

The maximum steady-state inductor current is found using Equation (3-6)

$$I_{L,max} = \frac{V_{out}}{R_{rated}} \left[1 + \frac{R}{2Lf_s} (1-D) \right] = 24.0A \quad (3-6)$$

A suitable output capacitor must be chosen to handle the peak-to-peak ripple current $I_{L,max} - I_{L,min} = 8A$ supplied when the main switch is "off."

2. Selection of Resonant Inductor and Capacitors

Using the above results and the dynamic equations for the 8 modes enables the designer to calculate the proper resonant component values. In a standard buck converter, the switch will be "on" for $D \cdot T_s$ seconds and "off" for $(1-D)T_s$ seconds. For a switching frequency of 20kHz, this is an on-time of 40μs and an off-time of 10μs. In the case of the resonant converter there are 6 additional modes to account for which will take a finite amount of time to complete. Mode 6 of the resonant converter is the same as the "switch on" mode of the buck converter and mode 1 is the same as the "switch off" mode of the buck converter. Obviously for a given f_s , mode 6 or mode 1 must be shortened in length to account for the other modes so that the total time still adds up to T_s . As a result, the designer must choose mode duration times that are a magnitude or more shorter than mode 1 or 6.

To select the proper value for the resonant inductor L_r , the dynamics of mode 2 in Figure (2-2) are used. In mode 2, the auxiliary switch S_a is closed with the initial resonant inductor current i_r equal to zero. With the main diode D_m still forward biased "on," L_r has approximately V_{dc} volts across it and i_r quickly ramps up in accordance with Equation (3-7),

$$i_r = \frac{V_{dc}}{L_r} t \quad (3-7)$$

where t is the desired time to reach current i_r . The current i_r is approximately equal to $I_{L,min}$ at the instance S_a is closed. Since all values in Equation (3-7) are known, the designer can pick a time t and solve for the required inductance L_r . In this design, a time

of $1\mu\text{s}$ was selected which makes $L_r=27.8\mu\text{H}$. This is an adequate amount of inductance to minimize the time it takes to complete mode 2 and at the same time allow S_a to be turned "on" in a ZCS mode.

Next, for the calculation of capacitors C_{r1} and C_{r2} , the dynamics of mode 3 from Figure (2-3) and mode 8 from Figure (2-10) are used. During mode 3, C_{r1} is resonating with L_r and Equation (3-8) can be written to find V_{cr1} .

$$V_{cr1} = V_{dc} \cos \left[\frac{1}{\sqrt{L_r C_{r1}}} t \right] \quad (3-8)$$

The resonant inductor current builds up according to

$$i_r = I_{L,\min} + V_{dc} \sqrt{\frac{C_{r1}}{L_r}} \sin \left[\frac{1}{\sqrt{L_r C_{r1}}} t \right] \quad (3-9)$$

From (3-8) it will take a quarter of a cycle for V_{cr1} to decay to zero. If a suitable value of time t is chosen, the value of C_{r1} can be found. If $t = 0.1\mu\text{s}$,

$$\frac{\pi}{2} \sqrt{L_r C_{r1}} = 0.1\mu\text{s} \quad (3-10)$$

which results in

$$C_{r1} = 146\text{pF}. \quad (3-11)$$

Later it will be shown that if an Insulated Gate Bipolar Transistor (IGBT) or MOSFET is used as the switch, the body capacitance is close to the calculated value of C_{r1} and no external capacitor is needed.

Using the dynamics of mode 8, Equation (3-12) can be used to find C_{r2} .

$$V_{Cr1} = \frac{I_{L,\max}}{C_{r1} + C_{r2}} t \quad (3-12)$$

Since C_{r1} must charge up to V_{dc} , by picking a value of time t , the required value of C_{r2} can be found. For $t=0.1\mu\text{s}$,

$$C_{r2}=4.25\text{nF} . \quad (3-13)$$

The next standard value capacitor available in the power lab was 1nF, so this value of capacitance was used. Letting $C_{r2}= 1\text{nF}$ and solving for t in Equation (3-12) yields approximately 26 ns.

Now that values for C_{r1} and C_{r2} have been determined, the dynamics of mode 5 and 5x must be analyzed to determine if mode 5x occurs. Mode 5 and 5x are shown in Figures (2-6) and (2-7), respectively. In this analysis it is assumed that t is zero at the beginning of mode 5. The equations governing mode 5 are given by:

$$V_{Cr2}=i_{r,\max}\sqrt{\frac{L_r}{C_{r2}}}\sin\left[\frac{1}{\sqrt{L_r C_{r2}}}t\right] \quad (3-13)$$

and

$$i_r=i_{r,\max}\cos\left[\frac{1}{\sqrt{L_r C_{r2}}}t\right] \quad (3-14)$$

where,

$$i_{r,\max}=I_{L,\min}+V_{dc}\sqrt{\frac{C_{r1}}{L_r}}=17.14\text{A} . \quad (3-15)$$

Equation (3-15) occurs during the quarter cycle of mode 3 when C_{r1} decays to zero volts. Solving Equation (3-13) for the time it takes C_{r2} to charge to 500 volts during mode 5 yields:

$$t_5=29.3\text{ns} . \quad (3-16)$$

During t_5 , Equation (3-14) predicts that i_r decays down to:

$$i_{r5}=16.88\text{A} . \quad (3-17)$$

Since the resonant inductor current did not decay to zero, the circuit enters mode 5x. In mode 5x, the resonant inductor decays through D_1 and D_2 and Equation (3-7) can be rearranged to solve for the decay time.

$$t_{5x} = \frac{i_{r5} L_r}{V_{dc}} = 0.945 \mu s \quad (3-18)$$

The above analysis shows that mode 5x is a significant amount of time. In Chapter V, this will be addressed when the converter design is optimized.

3. Semiconductor Switch Characteristics

So far in all of the analysis, it was assumed that both the main and auxiliary switches were ideal devices with the following characteristics:

- Zero current flow when blocking large voltages,
- Zero voltage drop when conducting large currents,
- Device can be switched "on" and "off" instantaneously when triggered,
- Triggering device requires no power.

As expected, no devices exist with these characteristics, but different device families are available with relative advantages over each other in these areas. Currently, the controllable turn on/off devices in use today for power converters are the Metal-Oxide Field Effect Transistor (MOSFET), Bipolar Junction Transistor (BJT) and the Insulated Gate Bipolar Transistor (IGBT). Many other families based on the thyristor exist, but they were not considered, since they are typically a controlled-turn-on device only. Other variants of thyristors such as the Gate-Turn-Off (GTO) are controlled-turn-off devices, but were not considered due to their slow switching speeds.

All real switching devices will have switching characteristics similar to Figure (3-2). During one complete cycle of the switch there will be energy loss during turn-on, turn-off and steady-state conduction. When a gating signal is applied as shown in Figure 3-2a), a real semiconductor switch will not react instantaneously and will have delays associated with charge buildup in the device.

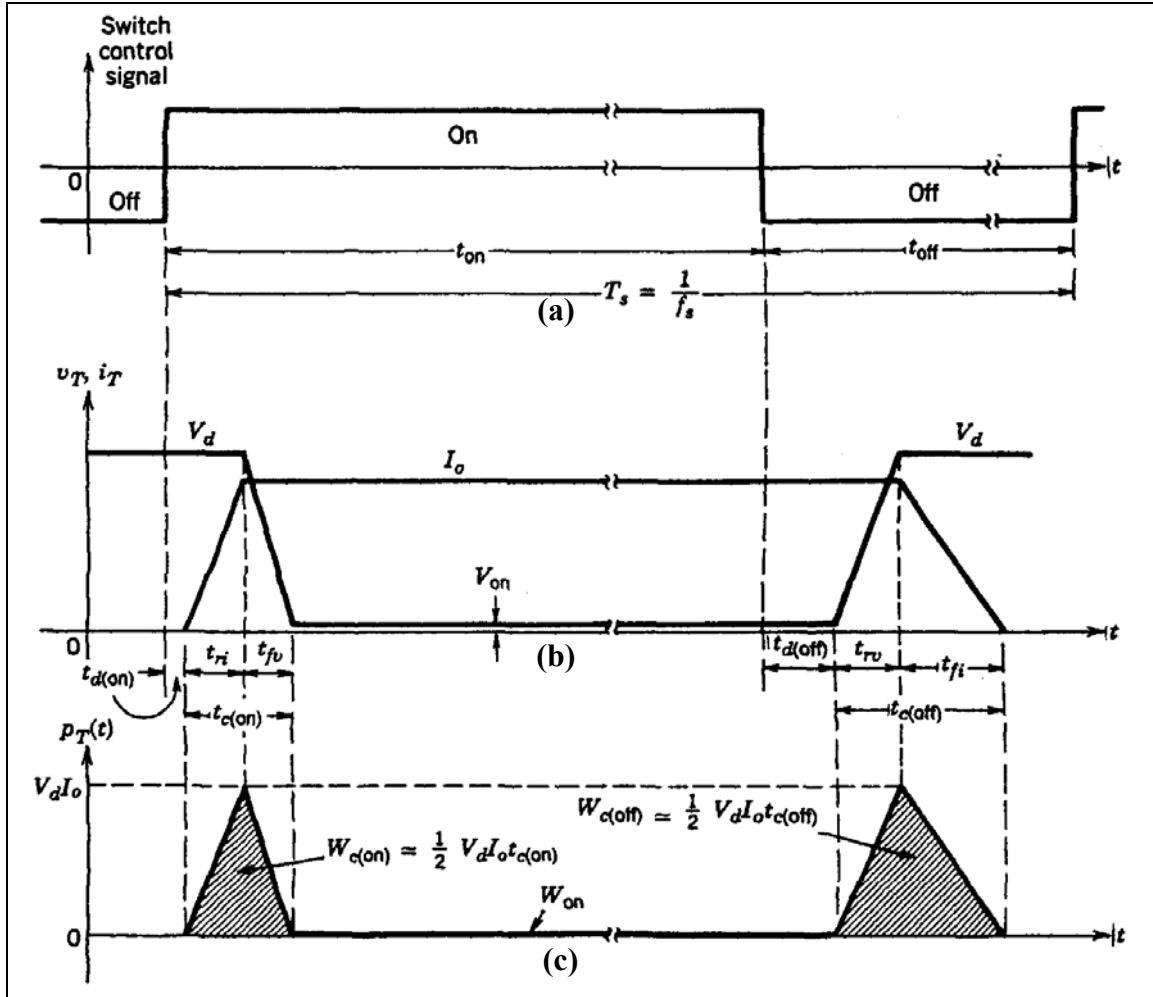


Figure 3-2. Generalized Switching Waveforms: (a) Gate Waveform, (b) IGBT Current and Voltage Waveforms, (c) Instantaneous Switch Power Loss (from ref. [6]).

The reverse recovery of a diode circuit will also increase the turn-on losses, because the switch current must reach the diode current with system voltage still applied across the switch before the diode is starved of current. The main switch, S_m , paired with diode D_m in Figure (3-1) illustrates this turn-on loss. When the gate signal is applied, D_m is forward biased and S_m has V_{dc} across its terminals. The current rapidly builds up through S_m , but the voltage across S_m remains at V_{dc} until D_m is starved of current and becomes reversed biased.

Following turn-on, the switch undergoes a period of steady-state conduction loss due to its internal resistance and current flow. Typical power transistors will have

voltage drops of 2 to 5 volts during a full-on conduction stage and this will add to the total power loss.

Finally, when a switch is gated "off," charge must be removed from the gate/base region and in some cases recombination has to occur before the current decays to zero. As in the turn-on case, full voltage will be across the device while this transition occurs, thus power loss will again happen.

The switching losses can be estimated by treating the total area under the voltage-current curve of Figure (3-2) as a triangle. The following energy loss equation can be written based on this simple geometry.

$$W_{on} = \frac{1}{2} V_d I_o t_{c(on)} \quad (3-19)$$

$$W_{off} = \frac{1}{2} V_d I_o t_{c(off)} \quad (3-20)$$

$$W_{conduction} = V_d I_o t_{on} \quad (3-21)$$

With a switching frequency of f_s , the above amounts of energy loss occur f_s times in a second and thus:

$$P_{on} = \frac{1}{2} V_d I_o t_{c(on)} f_s, \quad (3-22)$$

$$P_{off} = \frac{1}{2} V_d I_o t_{c(off)} f_s, \quad (3-23)$$

$$P_{conduction} = V_d I_o t_{on} f_s, \quad (3-24)$$

and

$$P_{total} = P_{on} + P_{off} + P_{conduction}. \quad (3-25)$$

In Chapter V, simulation results from PSPICE are analyzed using MATLAB to estimate the power loss in the Joung converter and the results are used to verify the optimization.

4. Semiconductor Switch Selection

Each of these devices will now be assessed and the advantages and disadvantages will be analyzed to determine the best device for the resonant converter in this thesis. Figure (3-3) illustrates the more common devices in use today and their relative voltage, current and switching frequency capabilities.

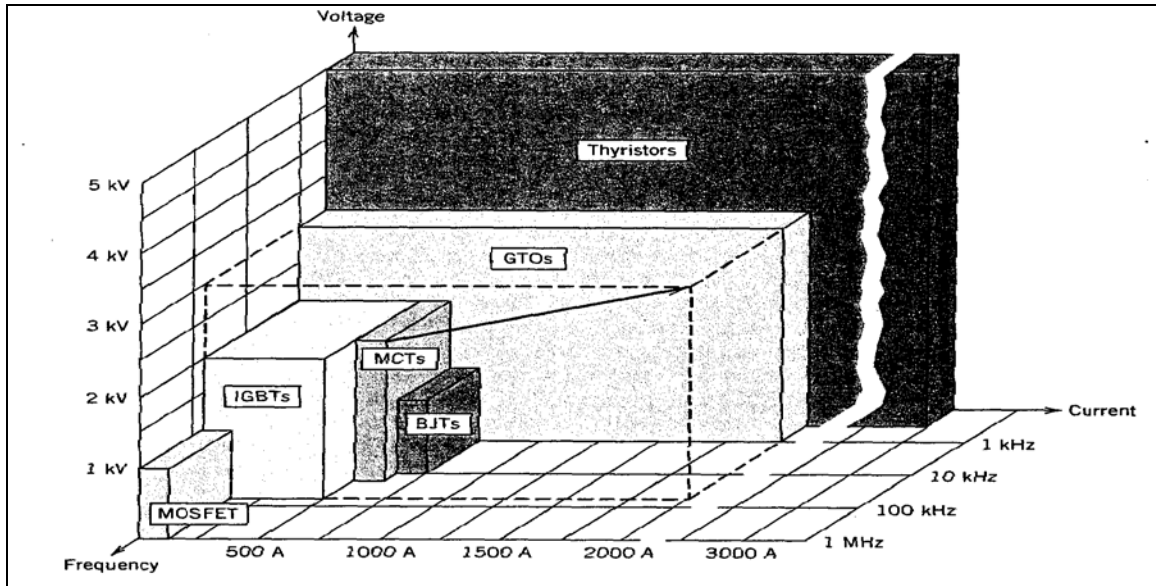


Figure 3-3. Summary of Semiconductor Switching Devices (from ref. [6]).

The first device considered was the Bipolar Junction Transistor (BJT). The BJT is a current-controlled device with a negative temperature coefficient. A negative temperature coefficient is considered a disadvantage as the device is prone to thermal runaway problems and makes device paralleling difficult. The base region in power transistors tends to be wider, which drastically reduces the current gain β in comparison to a small signal transistor [16]. The result is that the base current, i_b , is no longer insignificant and is a large fraction of the emitter current. The large base current makes the design of the driver circuitry difficult. To increase β , power transistors are connected in a Darlington configuration or even a tripton configuration, at the cost of decreased switching speeds [6]. The development of power BJTs has all but stopped due to the advancement of voltage-controlled transistors such as the IGBT.

The next device considered for this design is the MOSFET. The most notable advantage of this device is that it is voltage controlled, thus making the driver circuit easier to design. The MOSFET is also a positive temperature coefficient device, which makes it more thermally stable and appropriate for device paralleling. Unlike the BJT, the MOSFET only has one charge carrier and does not suffer from delay times due to charge recombination as in the base region of the BJT. As a result, the MOSFET can switch "on" and "off" at significantly higher speeds and hence the MOSFET is used almost exclusively for low-power converters. The drawback of the MOSFET is that the on-state resistance R_{DS} increases rapidly with the device blocking voltage rating and this is shown in Equation (3-19).

$$R_{DS} \approx kV_{DS}^{2.6} \quad (3-26)$$

As a result, MOSFETs are available with voltage blocking ratings up to about 1000 volts, but with small current ratings (~10 amps) and up to 100 amps with small voltage blocking ratings (~100 volts). In reference [17], the authors found that a suitable MOSFET device would have a die size 3 to 4 times the area of a bipolar transistor in order to reduce the conduction losses to an acceptable level. A search was performed for a MOSFET that would work in this design and no such device was found that could handle both 1200 volts DC and 50 amps of current. Because of the high conduction losses, the MOSFET was not used in this design, thus leaving only the IGBT for the task.

The IGBT switch is a bipolar transistor with a MOSFET transistor driving the base in a Darlington configuration. This device has many of the advantages of the MOSFET and BJT and is now the preferred choice when designing power converters. The IGBT is a voltage-controlled device with a main body region similar to a BJT transistor. A physical makeup of the IGBT is illustrated in Figure (3-4).

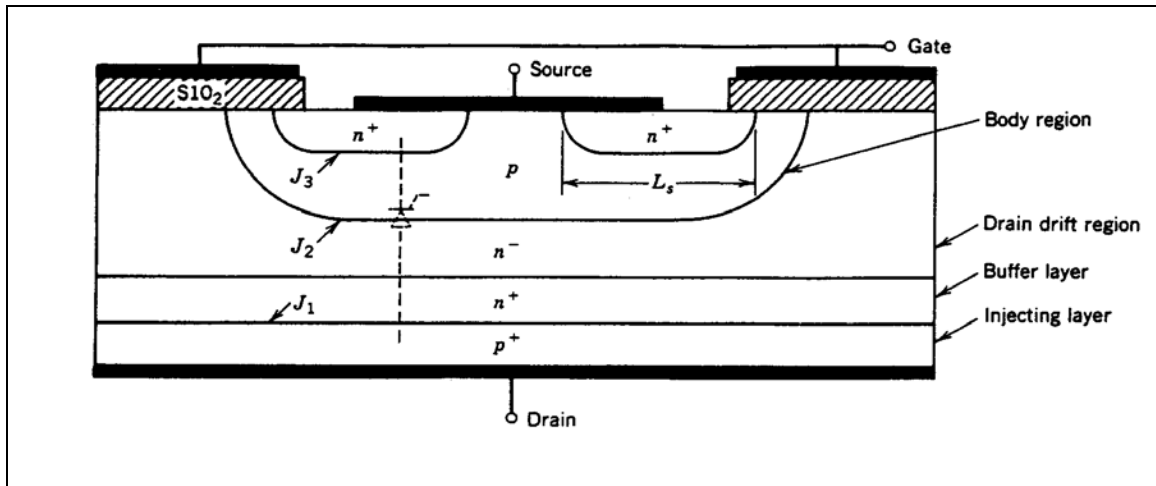


Figure 3-4. Vertical Cross Section of IGBT (from ref. [6]).

During the blocking state, the gate voltage is below the threshold voltage and the circuit voltage is dropped across the depletion region with little leakage current flowing. When the gate voltage exceeds the threshold, an inversion layer forms beneath the gate and shorts the n^+ region to the n^- region. The current that flows causes hole injection from the p^+ region into the n^- region. The injected holes continue to the p-body region via drift and diffusion, and the excess holes attract electrons from the source connection. This process continues until the gate voltage returns to a value less than the threshold voltage, and the device transitions to the off-state. Based on the explanation of the operation of the IGBT, the equivalent circuit depicted in Figure (3-5) can be used.

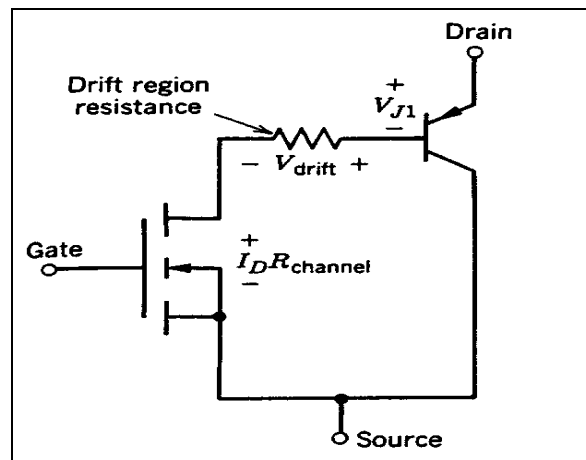


Figure 3-5. Equivalent IGBT Circuit (from ref. [6]).

To further simplify Figure (3-5), the symbol in Figure (3-6) is most commonly used and will be used for the duration of this thesis.

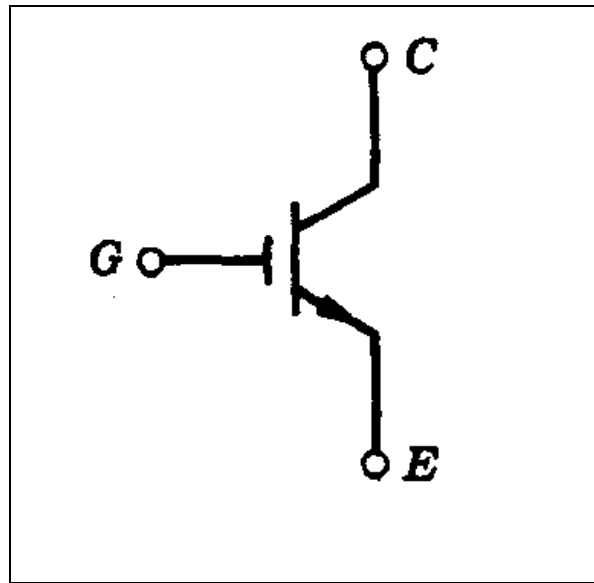


Figure 3-6. IGBT Symbol.

Even though the mating of the MOSFET and BJT transistor makes a device with many of the advantages of the two devices alone, a few drawbacks do emerge in the IGBT. During the turn-on transient, the IGBT behaves similar to a MOSFET as expected since the internal MOSFET must be gated "on" before the BJT is biased "on." During turn-off, the IGBT is significantly slower since a negative bias is not applied to the base region to pull out charge as would normally be done when turning "off" a power BJT transistor. Just before turn-off, the fraction of current flow in the MOSFET channel is substantial, since the current gain β of the internal BJT is low. When the gate voltage goes negative, the gate charge is pulled out quickly and the channel closes. The current flow in the internal BJT transistor falls off more slowly, since the carriers are eliminated by recombination. As a result, a characteristic called a "current tail" occurs [16]. Since the high off-state voltage will already be across the device when this tail current is flowing, the current tail is the major source of switching losses in IGBTs. A graphical picture of the current tail is shown in Figure (3-7).

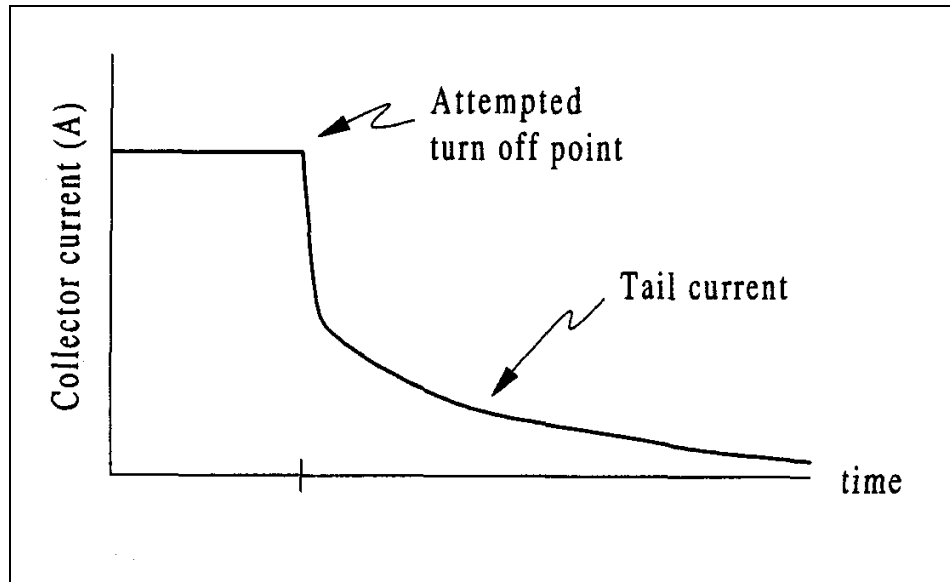


Figure 3-7. IGBT Current Tail During Turn-Off (from ref. [16]).

This current trace is quite different than the more simplistic current trace in Figure (3-2), and PSPICE along with a MATLAB program will be used to calculate IGBT switch losses using a numerical integration technique in Chapter V.

5. Future Semiconductor Material

Recently, diodes have been built using silicon carbide (SiC) instead of silicon (Si). The experimental results show that SiC devices have significantly reduced reverse recovery times ($\sim$ factor of $1/10^{\text{th}}$) with $1/10^{\text{th}}$ the on-state resistance of Si diodes. The SiC devices have a band-gap energy roughly 3 times that of Si devices and, as a result, the SiC devices can operate at a temperature of 300°C versus 150°C for Si devices [18]. If this technology is used in transistors in the future, the devices will have reduced switching times with less on-state resistance at higher temperatures. With reduced switching times, higher switching frequencies will be possible and smaller filtering components can be used. Overall, power converters using these devices will have significant improvements in efficiency and will be able to operate at higher temperatures.

6. IGBT Selection

Currently, IGBTs are available with blocking voltage ratings of 1700 volts at over 500 amps. These devices are packaged in bolt-on modules with a large surface area for heat dissipation. In the hard-switched converter [5], a Semikron SKM 100GB 124D was used as the switch. This device has a pair of IGBT transistors in a 1.25-inch by 3.5-inch package with a total power dissipation rating of 700 watts at a case temperature of 25°C. In the hard-switched configuration, it was estimated that the IGBT was dissipating approximately 200 watts, so the device is well under its thermal limits.

In the resonant converter design, the power loss in theory should be less, so a smaller IGBT switch in a TO-247 package was used. The TO-247 package is not much bigger than the standard TO-220 case. A search through manufacturer's data sheets was completed and International Rectifier's IRG4PH50UD IGBT was selected. The device was similar to all the other manufacturer's products and was mainly selected because it was available through DigiKey Corporation. The cost of each device was fifteen dollars, which is significantly cheaper than the two hundred and seventy dollar SKM 100GB 124D. The IRG4PH50UD is rated for 1200 volts at 45 amps continuous and has a 200-watt power dissipation rating at a case temperature of 25 °C. The complete data sheet for the IRG4PH50UD is located in Appendix A.

C. PSPICE ANALYSIS

Given a preliminary converter design, the next phase in the research effort required the development of a computer simulation to both verify and optimize the circuit performance. This resonant converter, unlike other hard-switched converters, will transfer considerable energy through rather small components. If any portion of the circuit fails to work properly, the components will be easily stressed beyond the maximum ratings with devastating results. The simulation program of choice was Microsim PSPICE release 8.0 as it was readily available and has a vast library of components. Most of the power semiconductor manufacturers provide models for their devices that can be downloaded off of the Internet and inserted in circuits. Presumably these models were developed based on device testbed results, but the designer should

never fully trust the models and should study the simulation result to see if they make sense. Berning and Hefner [19] made a major break through when they developed accurate IGBT models based on realistic hard and soft-switching testbeds. The National Institute of Standards and Technology (NIST) adopted the models and they were transferred to industry, thus improving the vendor's IGBT models.

1. PSPICE Simulation

The PSPICE simulation package allows the designer to model complex circuits at the component level. In earlier mathematical analysis, the transistor switches and diodes were treated as short circuits while conducting and open circuits while blocking and no high-order device effects were considered. With PSPICE, the components are represented in detail and the non-linear characteristics of each device are included if an appropriate model is used. In the simulation, soft-switching will be verified and the overall efficiency will be estimated. The estimated efficiency is important, as it will support the cooling system design and provide direction as to whether component ratings are adequate.

Figure (3-8) is the model schematic for the resonant converter. All parts on the schematic are from the built-in library with the exception of the International Rectifier IRG4PH50UD IGBT and the DSEI60 ultra-fast-recovery diode made by IXYS Corporation. The model data for the DSEI60 was downloaded from the IXYS Corporation's web site and inserted into a standard PSPICE diode model [20]. The IGBT model is more complex and required a subcircuit model to represent the device. The text file for the IGBT was downloaded from the International Rectifiers web site and a subcircuit was manually drawn based on the components and node connections in the file [21]. The text file for the IRG4PH50UD model is contained in Appendix B and the subcircuit is illustrated in Figure (3-9).

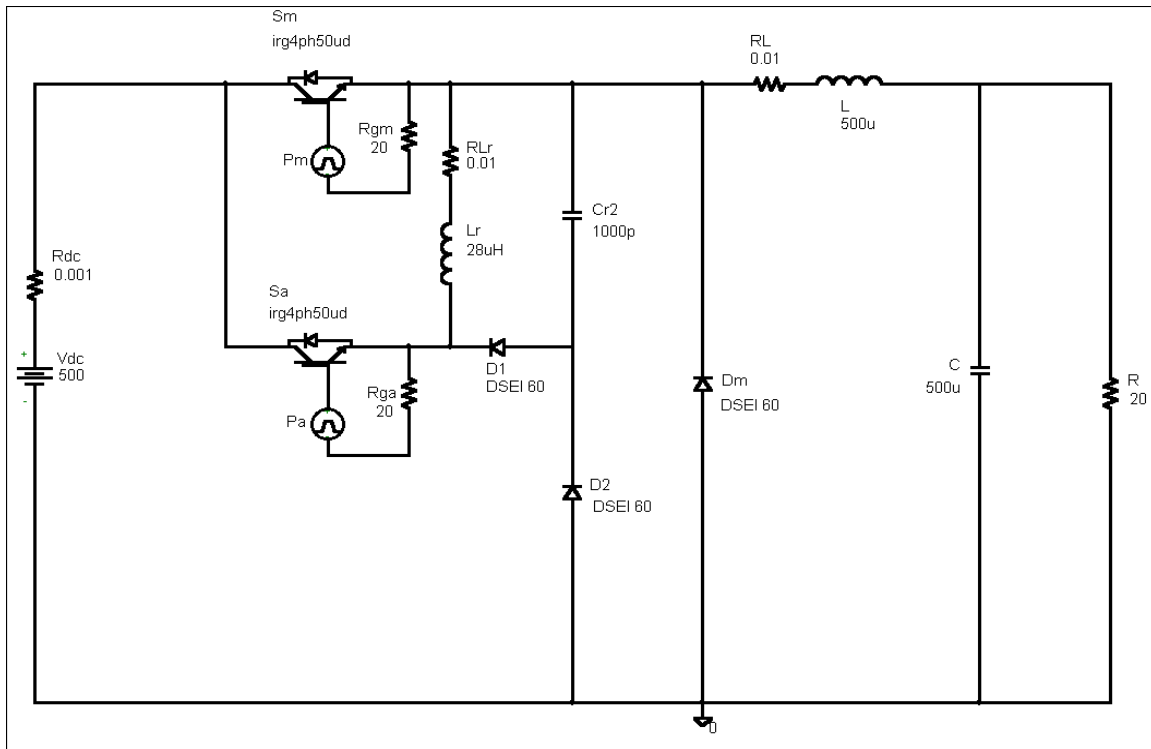


Figure 3-8. PSPICE Model of Resonant Converter.

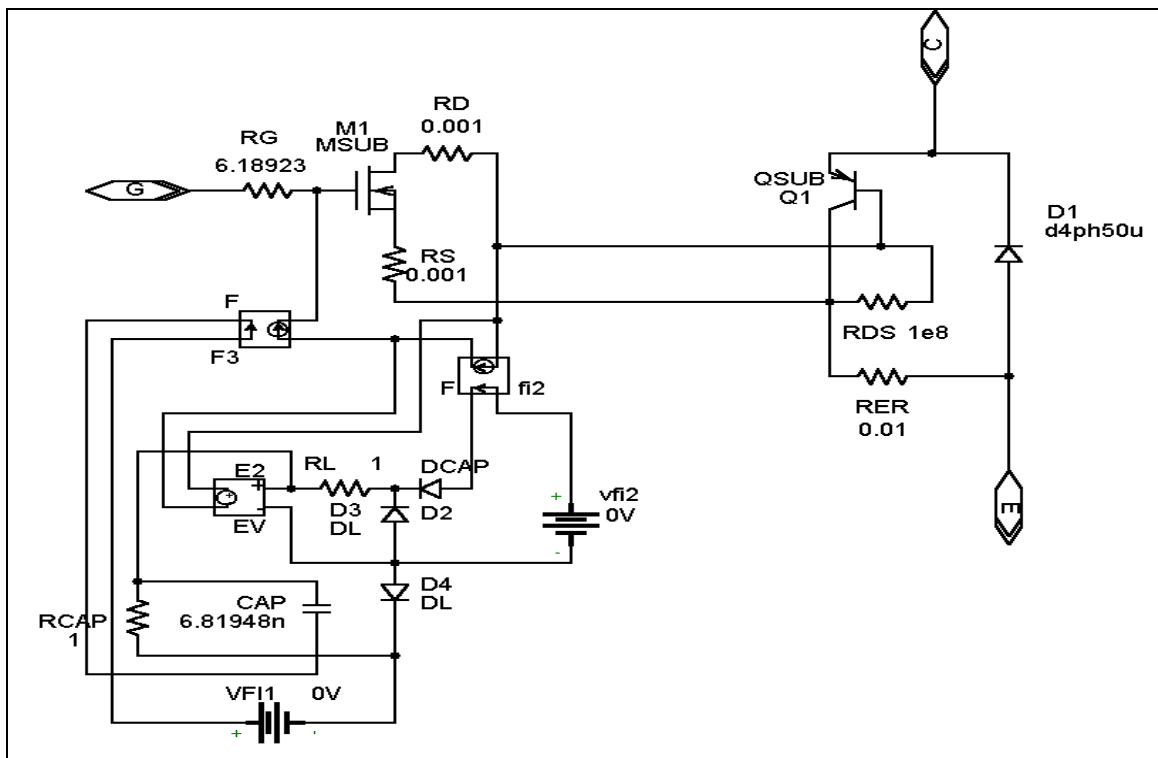


Figure 3-9. IGBT Subcircuit Model.

To stabilize the circuit simulation and add realism, small resistance was added in series with both of the inductors and the power source. During the early simulations, PSPICE failed to converge on a solution on a number of occasions. Adding the resistors limited the circuit current during transients and prevented the simulation from exceeding the time step limits. The rise times on both of the gate drivers were also set to realistic values ($\sim 10\text{ns}$) instead of zero to prevent sudden discontinuities. In Figure (3-8), the value of the main inductor is set to $500\mu\text{H}$ instead of the calculated 1mH . This was done knowing that the actual permeability of the core is approximately 50 percent of the initial permeability due to the large amount of DC current bias ($\sim 20\text{ amps}$). Initial conditions for the main inductor and output capacitor were also set to accelerate the simulation. The initial inductor current was set to an average value of 20 amps and the output capacitor voltage was set to 400 volts. Setting the initial conditions allowed the simulation to reach steady-state in half the time.

1. PSPICE Results for Maximum Load

When simulating the resonant converter, the proper sequencing of the IGBTs must occur. From Equation (3-7), the resonant inductor current takes approximately $1\mu\text{s}$ to reach $I_{L,\text{min}}$ and an additional $0.1\mu\text{s}$ for C_{r1} to decay to zero volts in mode 3. Adding these two times together, the auxiliary switch S_a must be on for $1.1\mu\text{s}$ before the main switch is closed in mode 4. An additional $0.4\mu\text{s}$ of time was added to the main switch delay to determine when to gate S_a "off." Figure (3-10) shows the proper sequencing during turn-on for the gating signals P_a and P_m of Figure (3-8).

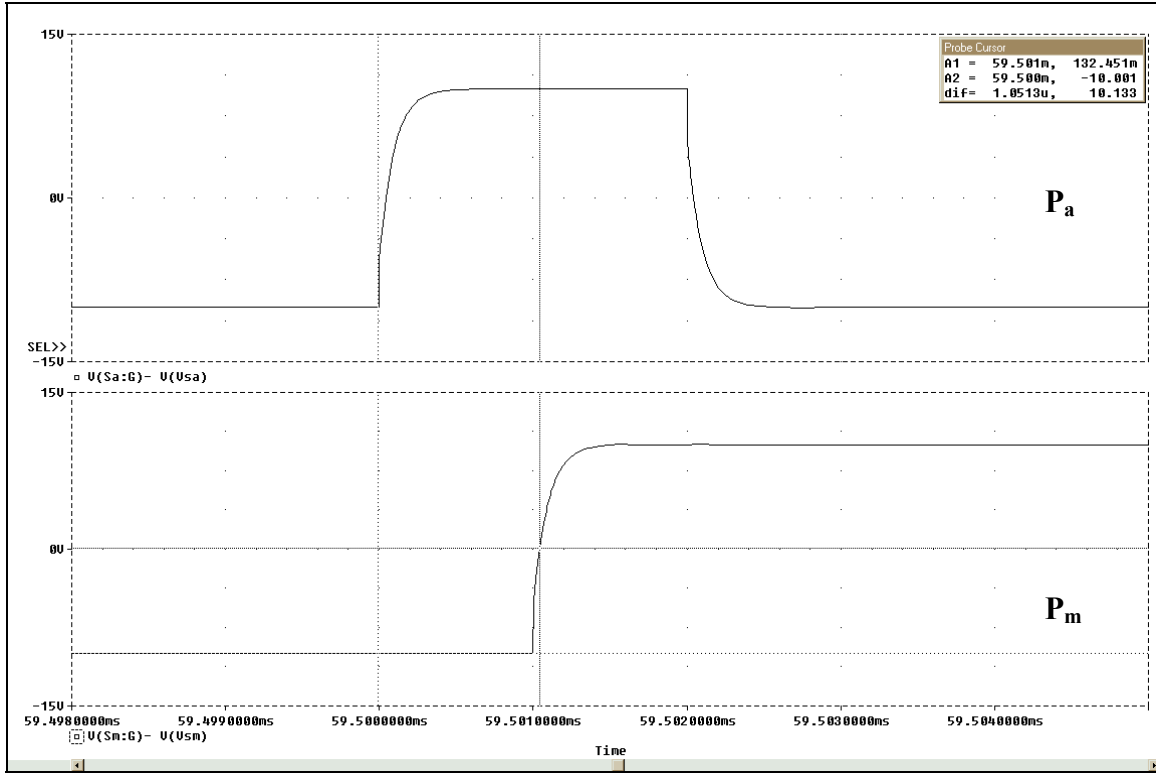


Figure 3-10. Auxiliary Switch Pulse P_a and Main Switch Pulse P_m .

Next the output load voltage was verified to be 400 volts, which was obtained from $D = 0.8$ and $V_{dc} = 500$ volts in Equation (3-1). The resulting plot of output load voltage is shown in Figure (3-11).

Another signal of interest that demonstrates basic buck converter operation is the main inductor current. From Equations (3-5) and (3-6) and the analysis of mode 1 and 6 in Chapter II, the main inductor current waveform will be triangular shaped with $I_{L,min} = 16$ amps and $I_{L,max} = 24$ amps. Mode 6 is characterized by the positive-slope portion of the inductor current in Figure (3-12) when the main switch is "on" and V_{dc} is supplying power to the load through the main inductor. After the main switch is opened in mode 7/8 and the circuit transitions to mode 1, the main diode D_m is forward biased, thus allowing the main inductor to continue supplying energy to the load. Mode 1 is characterized by the negative-slope portion of Figure (3-12). The voltage and current waveforms for D_m are shown in Figure (3-13).

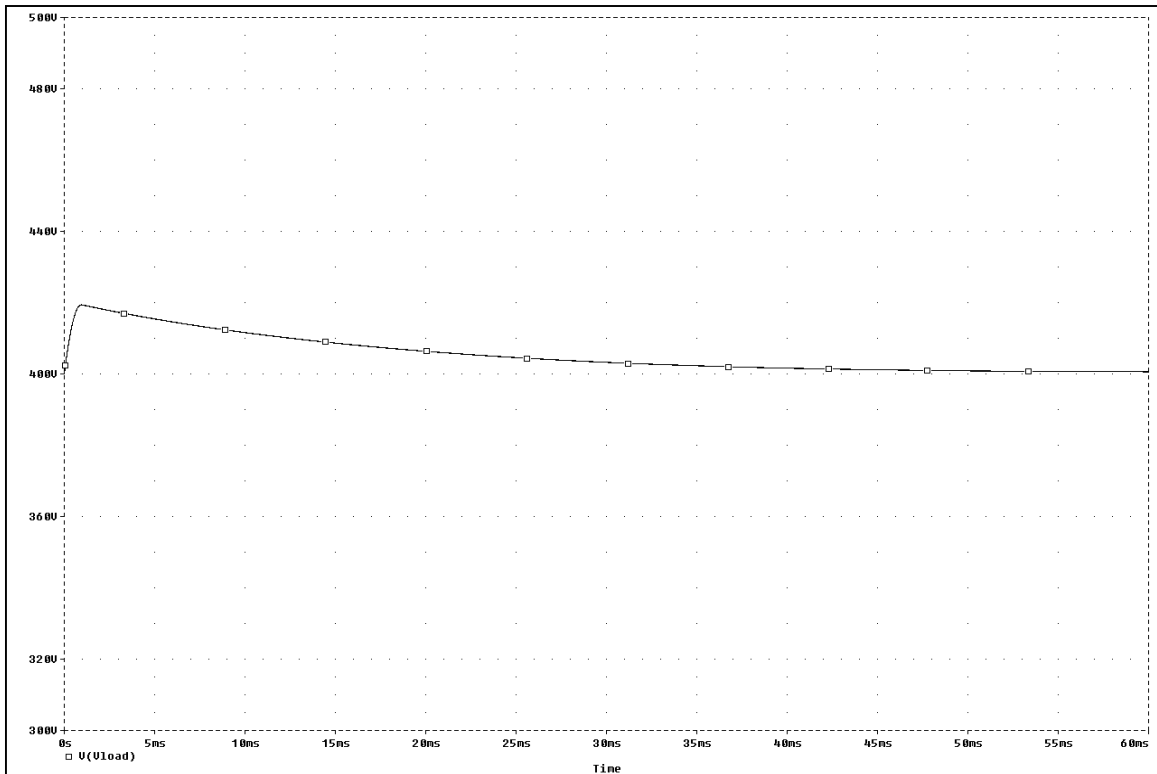


Figure 3-11. Output Load Voltage V_c .

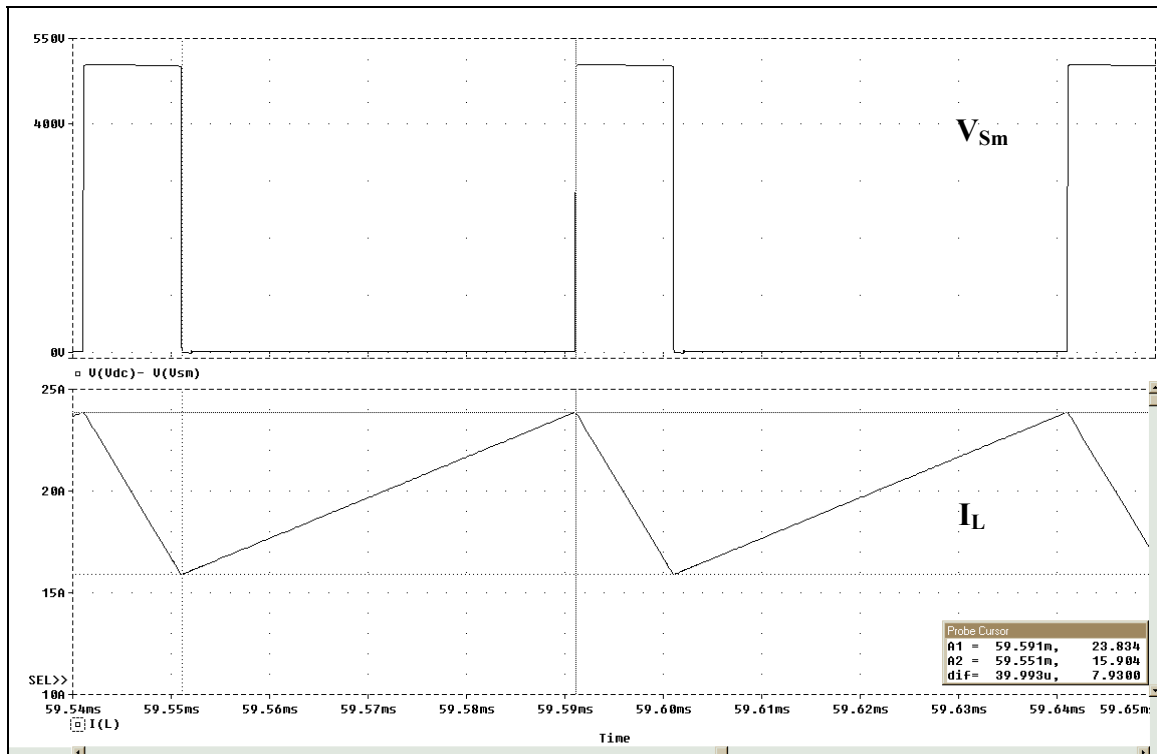


Figure 3-12. Main Switch Voltage and Main Inductor Current.

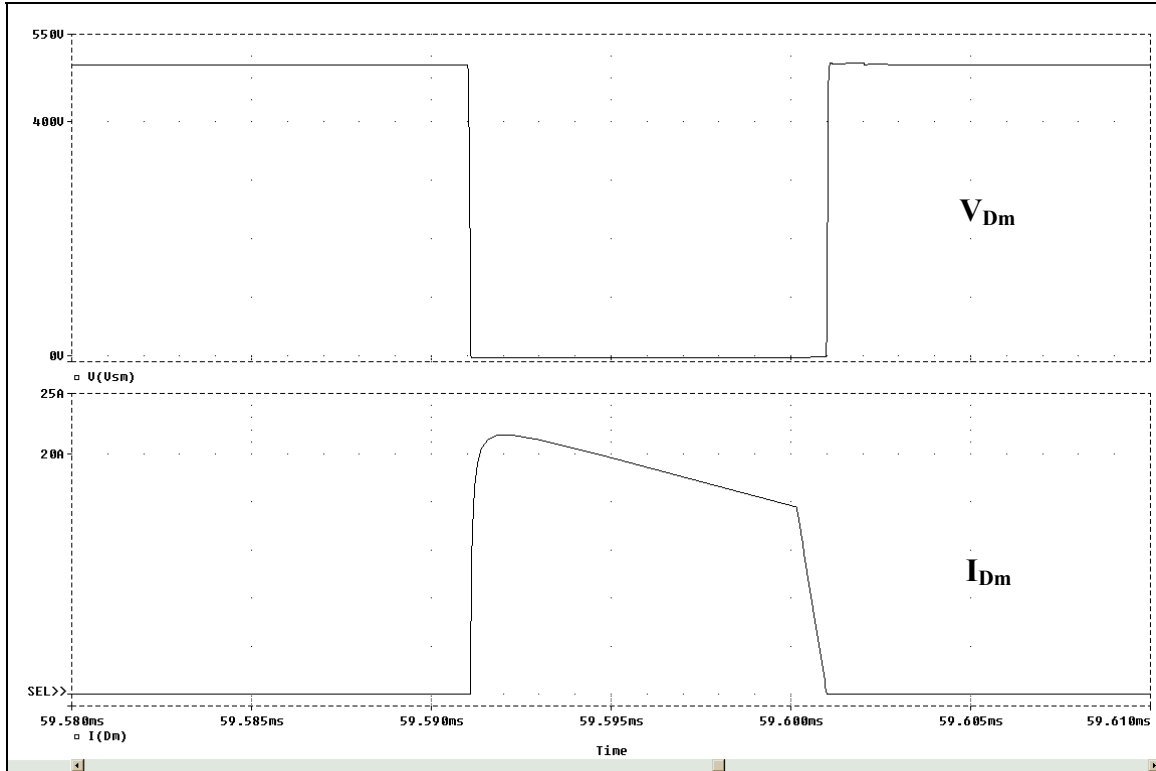


Figure 3-13. Main Diode Voltage and Current.

Now that the basic qualities of the resonant buck converter have been verified, the remaining current and voltage waveforms of the resonant components and diodes were analyzed to verify soft switching. In Figure (3-14), the voltages and currents for the main and auxiliary switch during turn-on are shown. Figure (3-14) illustrates that the main switch is clearly undergoing ZVS and the auxiliary switch is turned "on" with ZCS. The auxiliary switch current i_r builds up linearly as predicted by mode 2 analysis and the main switch voltage decays to zero as the circuit enters mode 3. When the auxiliary switch is turned "off" the following responses are seen. First, there is a small current pulse in the main switch and then a linear buildup as the main switch assumes the full load current. In the auxiliary switch, a similar current pulse occurs in the negative direction and then the current waveform decays with a current tail as discussed earlier in Chapter III.

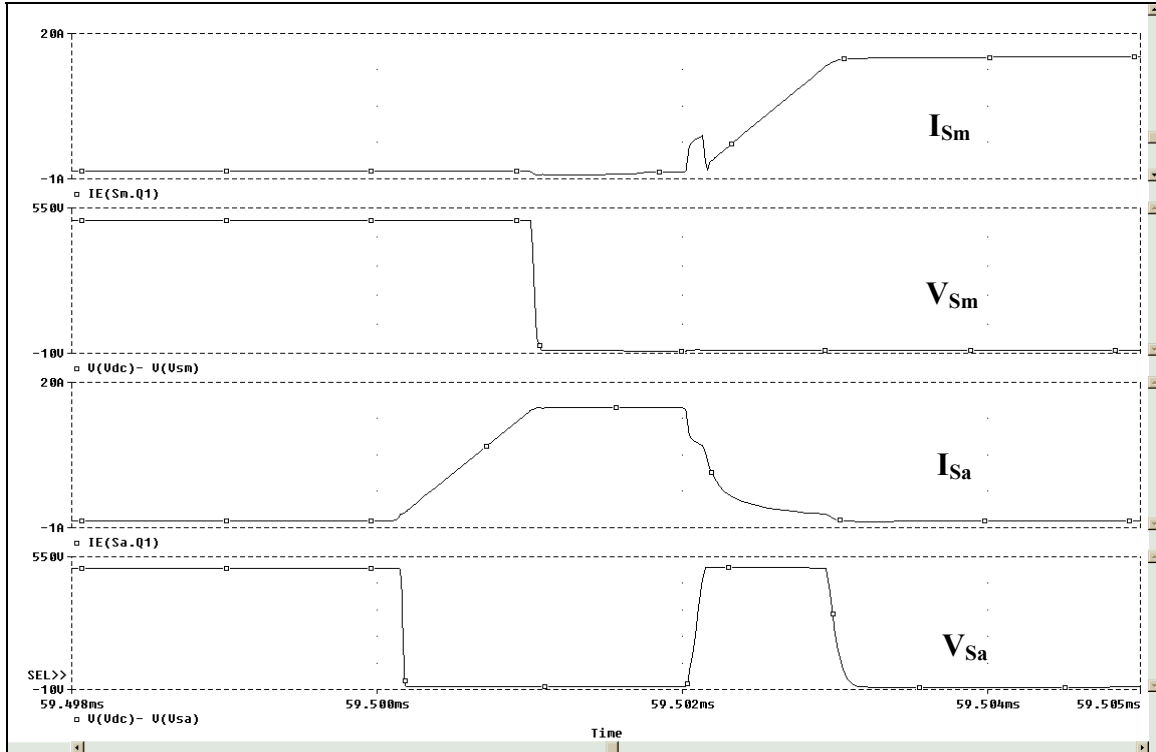


Figure 3-14. Main and Auxiliary Switch Currents and Voltages During Turn-On.

The small current pulse during the main switch turn-on can be explained by analyzing Figure (3-8) using Kirchhoff's current law. The instant that the auxiliary switch is gated "off," the current continues to flow, but decreases with the characteristic current tail. Since i_r cannot change instantly, D_1 forward biases "on," thus placing C_{r2} in parallel with L_r . As L_r and C_{r2} begin to resonate with each other, the main inductor L demands that the current remain constant and thus the current now charging up C_{r2} must be replaced by an equal amount from the source through the main switch. Thus, the current through the main switch will have the same amplitude shape as I_{Cr2} until the linear buildup begins.

During mode 5x with D_1 and D_2 forward biased and C_{r2} fully charged, the emitter of the auxiliary switch is at ground potential and the voltage across the switch is approximately V_{dc} . This is undesirable as a significant amount of current is still flowing through the switch with full voltage applied across the switch, thus causing an

appreciable amount of turn-off losses. Chapter V will address this issue and the design will be optimized to reduce turn-off losses.

The turn-on current waveforms for L_r , D_1 , D_2 are shown in Figure (3-15) along with S_a for reference. The current waveform for i_r in Figure (3-15a) has both a linear buildup and decay as expected. The waveform for D_1 shows the resonance between L_r and C_{r2} the instant S_a is gated "off" and then D_2 is forward biased "on" a short time later when mode 5x commences. All waveforms in Figure (3-15) appear as expected.

Next, the variables depicted in Figure (3-14) are plotted during turn-off in Figure (3-16). In Figure (3-16a), the main switch now has a sudden drop in current with a characteristic look of a discharging capacitor. Capacitor C_{r2} causes this current drop as it discharges in mode 8 and then the current tail portion of the waveform commences. A definite slope in the main switch voltage is seen and this stems from Equation (3-12), where C_{r1} and C_{r2} set the slope. The auxiliary switch current in Figure (3-16c) has a small current spike as V_{dc} is reapplied across it, thus charging the small amount of body capacitance.

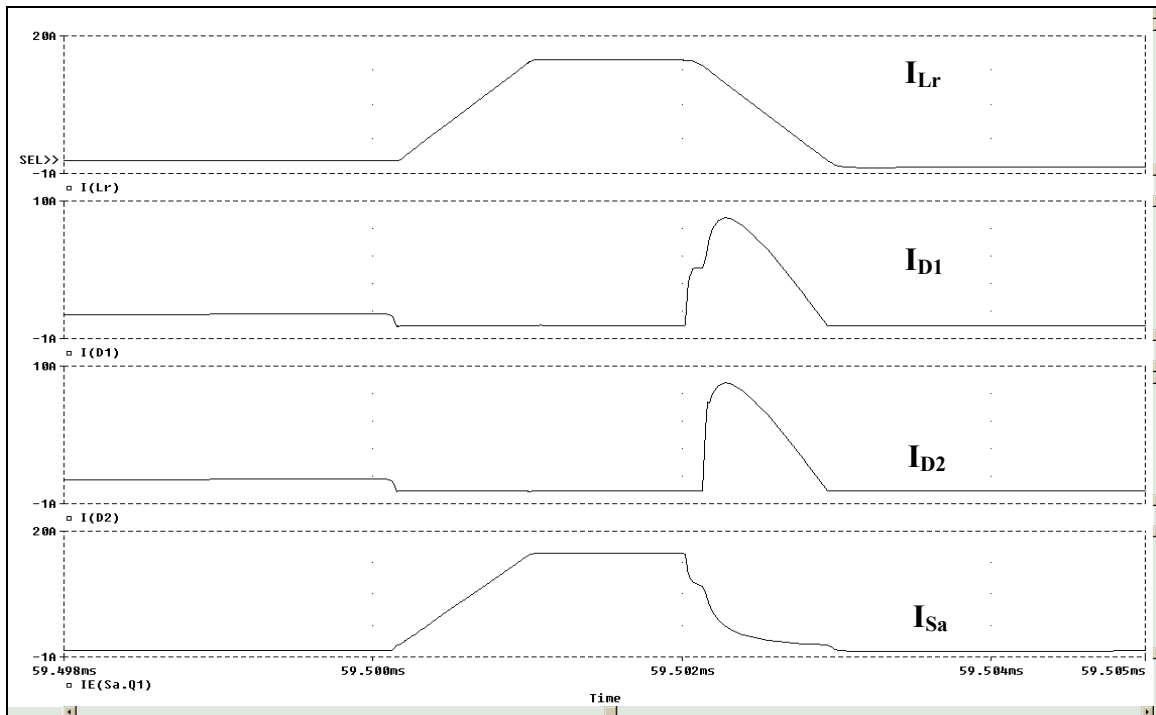


Figure 3-15. Current through L_r , D_1 , D_2 and S_a During Turn-On.

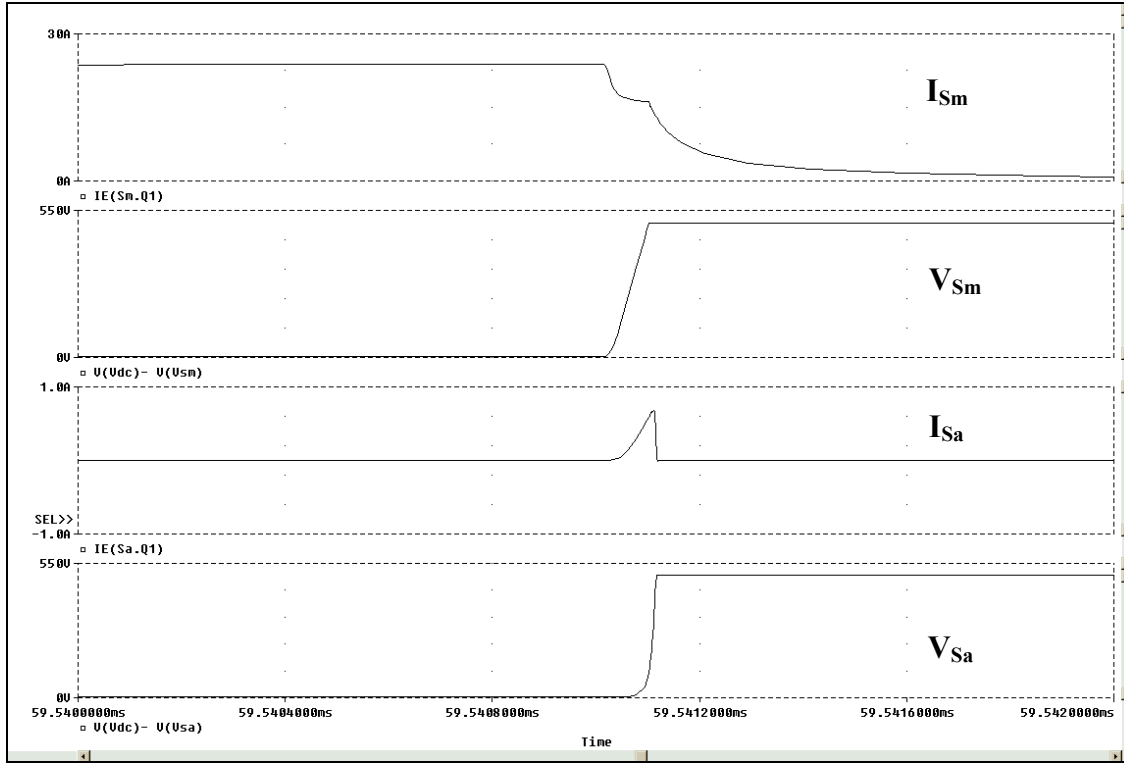


Figure 3-16. Voltage Across Main and Auxiliary Switch and Current Through Main and Auxiliary Switch During Turn-Off.

The turn-off waveforms for D_1 , D_2 and C_{r2} are shown in Figure (3-17). In Figures (3-17b) and (3-17c), the discharge current of C_{r2} is seen along with the decay of V_{Cr2} in Figure (3-17d). The decay slope of V_{Cr2} is algebraically related to the charging of C_{r1} , since

$$V_{Cr2} = V_{dc} - V_{Cr1} \quad (3-27)$$

from mode 8 analysis.

One anomaly seems to be occurring during the turn-off sequence. In Figure (3-17), a small positive current is flowing through D_1 and D_2 after C_{r2} is fully discharged. Mode 1 operation is occurring and D_m is conducting the main inductor current. Since the forward voltage drop across D_m increases as the conducted current increases, it is possible that the voltage drop across D_m is forward biasing D_1 and D_2 . The diodes D_1 and D_2 would then conduct a small portion of the inductor current and D_m would conduct the

remaining current. The current-voltage curves for the DSEI60 in Appendix A show how this anomaly could occur.

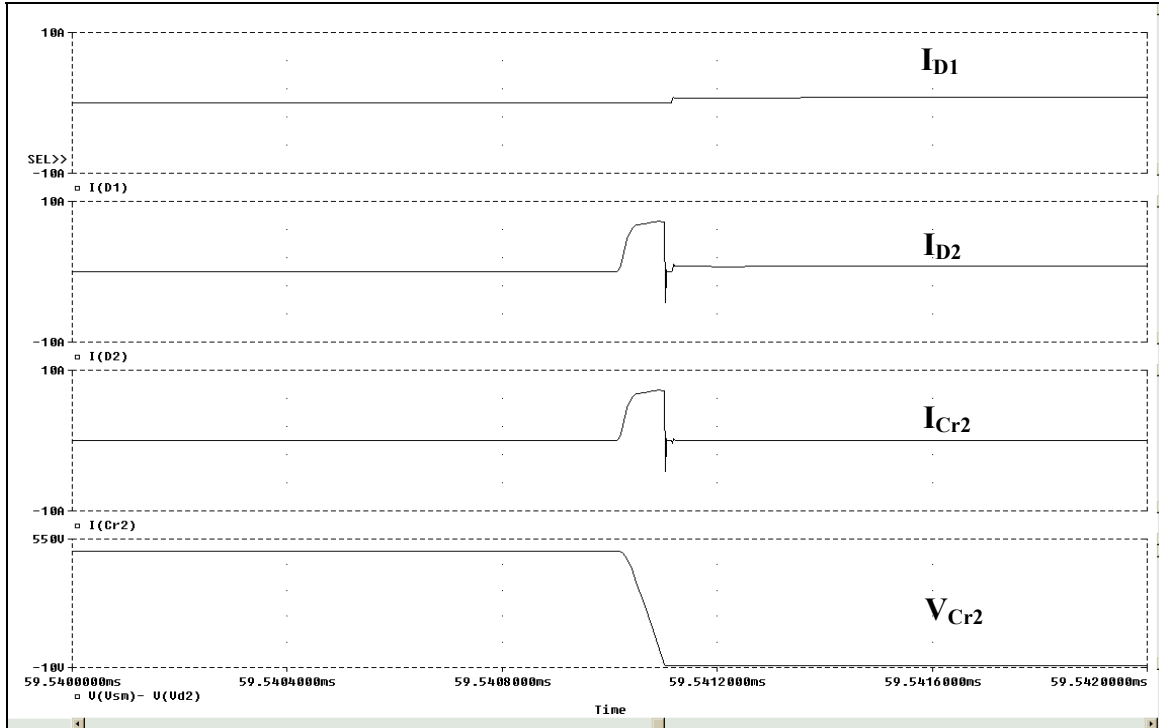


Figure 3-17. Current Through D₁, D₂, and C_{r2} and Voltage Across C_{r2} During Turn-Off.

The voltages across S_a, D₂, D₁ and C_{r2} are shown in Figure (3-18). The dashed lines in Figure (3-18) delineate where modes 1 through 8 occur.

Finally, the efficiency of the resonant converter for the full-load condition was estimated by plotting the average output power divided by the average input power. Figure (3-19) shows the efficiency reaching approximately 98.4 percent at steady-state. The 20 kHz ripple in the efficiency plot is caused by the voltage ripple of the output capacitor. With an output power of 8kW, just over 130 watts are lost in the circuit. With an estimate of power loss now known, thermal analysis can be performed to select an adequate cooling system. The thermal analysis for this design is documented in Appendix C.

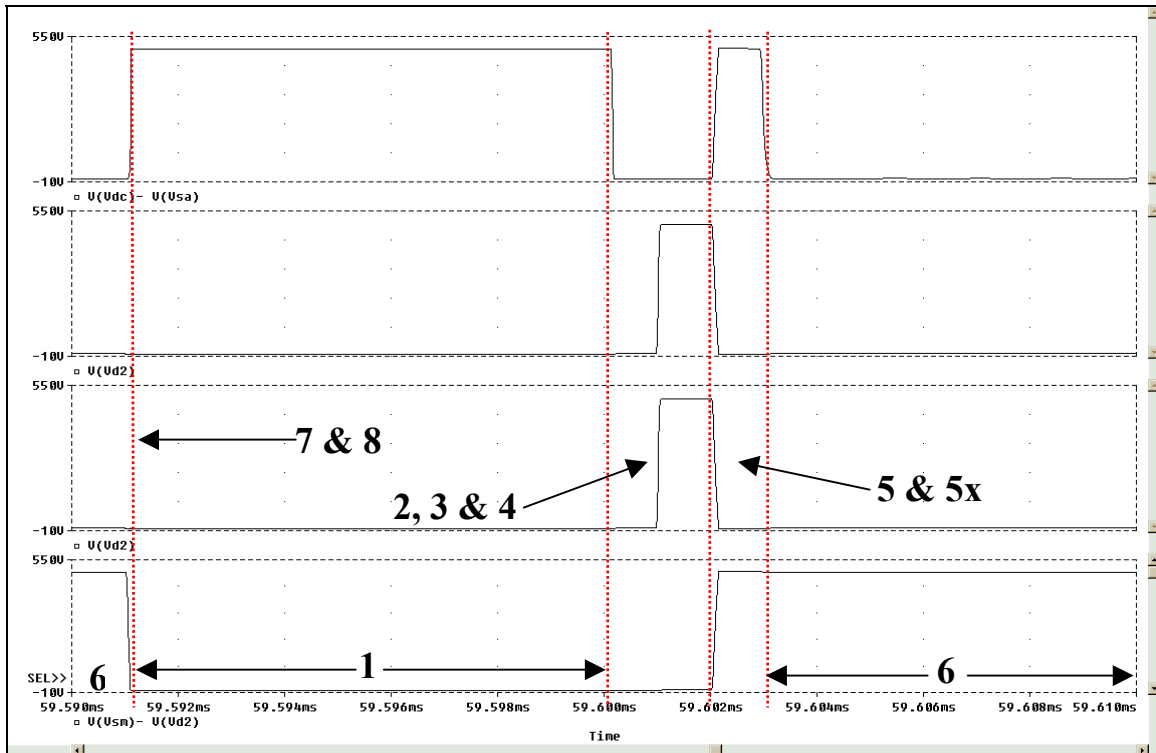


Figure 3-18. Comparison of the Voltages Across S_a , D_2 , D_1 and C_{r2} During Modes 1 Through 8.

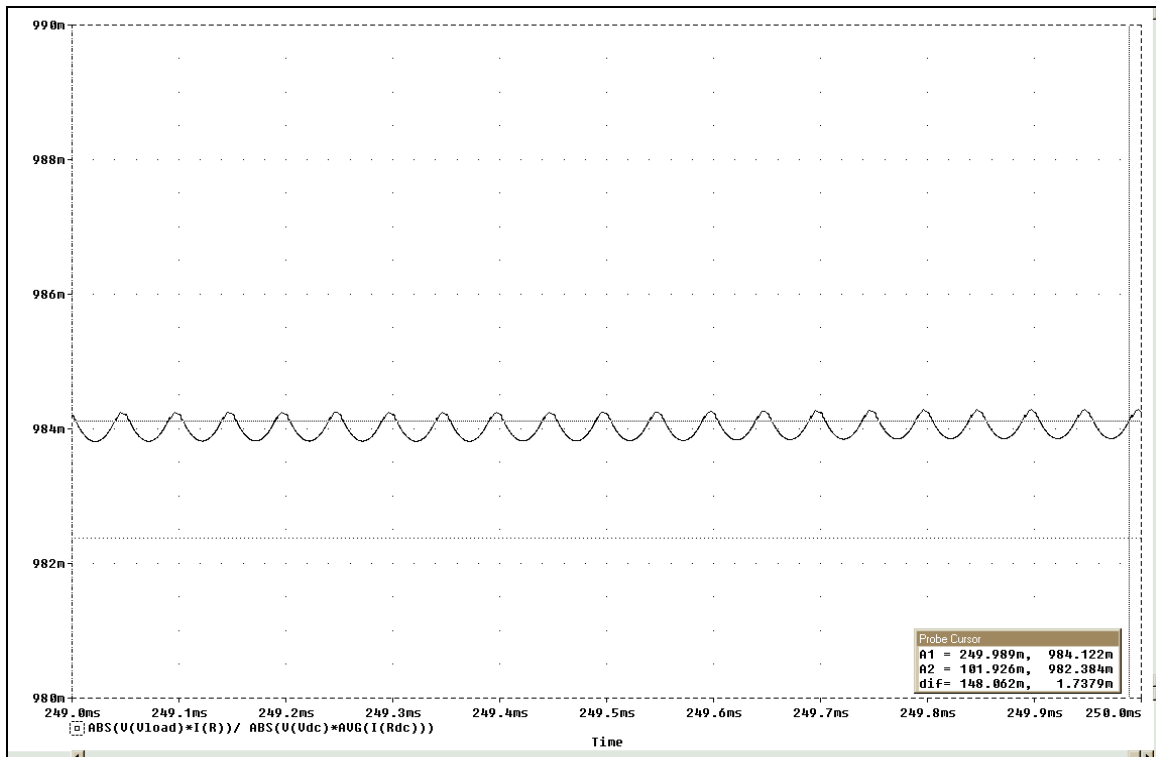


Figure 3-19. Estimated Efficiency of Resonant Converter.

2. PSPICE Results for Minimum Load

The PSPICE simulation was repeated for the minimum load case of $R = 200\Omega$. The voltage V_{Sm} is compared to the current I_L in Figure (3-20). The inductor current is greater than zero at the minimum point ($\sim 258\text{mA}$) and thus meets the requirement for continuous conduction mode operation. Using Equations (3-5) and (3-6) with $L = 1\text{mH}$, the expected minimum and maximum currents are:

$$I_{L,\min} = \frac{V_{\text{out}}}{R_{\text{rated}}} \left[1 - \frac{R}{2Lf_s} (1-D) \right] = 0\text{A} \quad (3-28)$$

and

$$I_{L,\max} = \frac{V_{\text{out}}}{R_{\text{rated}}} \left[1 - \frac{R}{2Lf_s} (1-D) \right] = 4.0\text{A} . \quad (3-29)$$

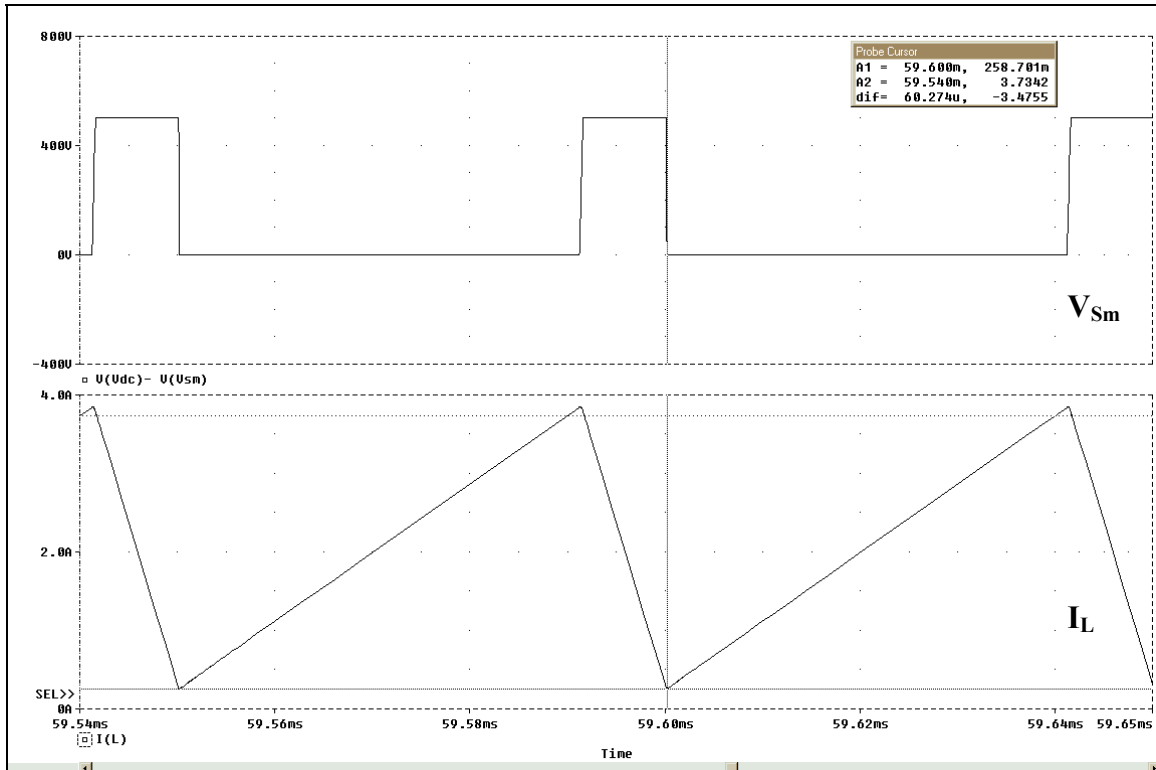


Figure 3-20. Main Switch Voltage and Main Inductor Current.

The voltage V_{Dm} and current I_{Dm} are shown in Figure (3-21). As expected, I_{Dm} decays to a value above zero amps when D_m is reversed biased.

The turn-on voltages and currents for S_m and S_a are illustrated in Figure (3-22). With $I_{L,min}$ at approximately zero amps and D_m forward biased, the resonant inductor current overshoots $I_{L,min}$ during mode 2. This overshoot is expected as energy from C_{r1} was transferred to L_r . Additional energy was stored in L_r during the reverse recovery of D_m . During mode 3, the resonance action between C_{r1} and L_r tries to return the energy back to C_{r1} and a negative current circulates through the anti-parallel diode of S_m . The same negative current is seen in Figure (3-14), but it is less pronounced as the y-axis scale goes from -1 amp to 20 amps.

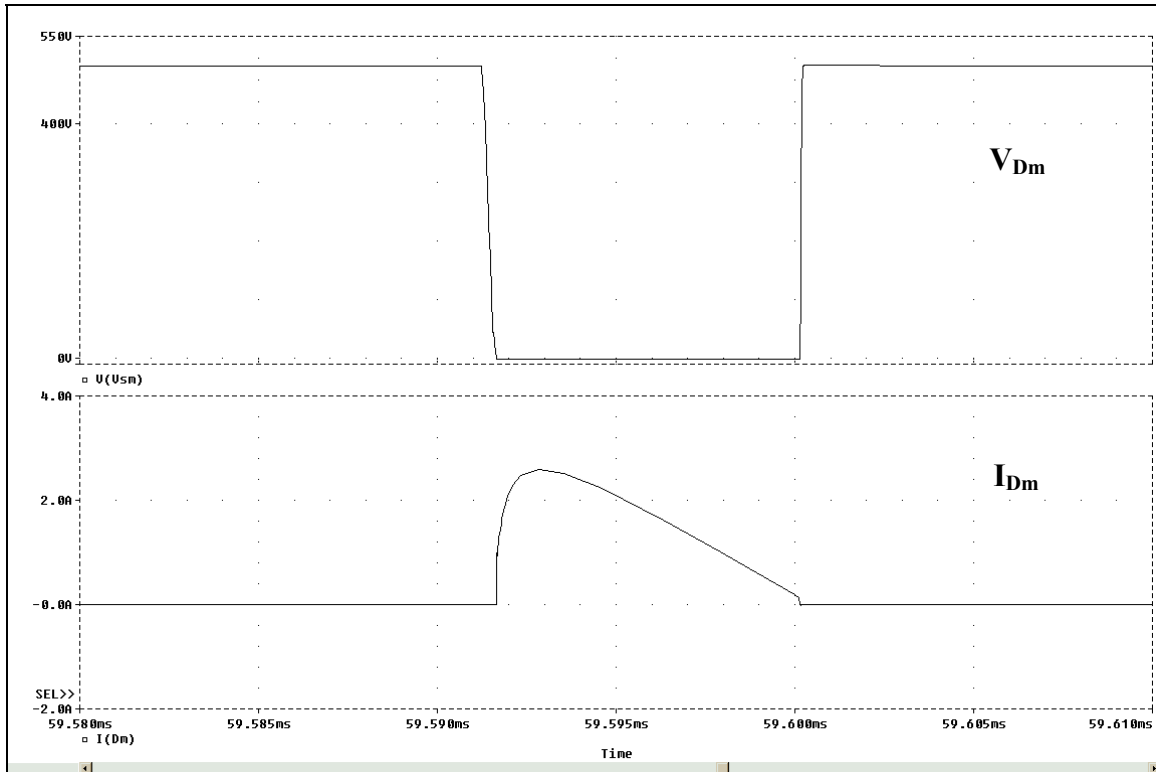


Figure 3-21. Main Diode Voltage and Main Diode Current.

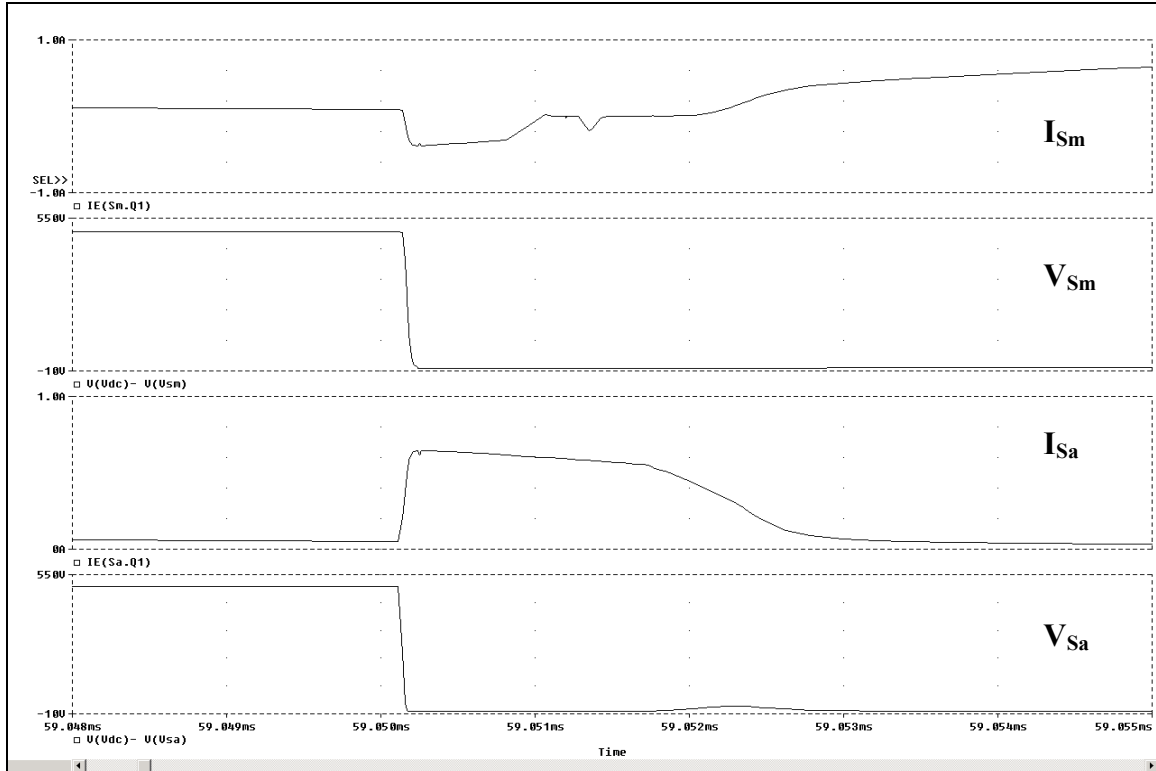


Figure 3-22. Main and Auxiliary Switch Currents and Voltages During Turn-On.

The turn-off voltages and currents for S_m and S_a are shown in Figure (3-23). The main switch still has a significant current tail, but the current amplitude is dramatically reduced when compared to the full-load case. When V_{dc} is reapplied across S_a , a current pulse occurs from the charging of the body capacitance. After the occurrence of the pulse, the current remains at a positive value ($\sim 150\text{mA}$) and slowly decays until the switch is gated "on" again. From the IRG4PH50UD data sheet in Appendix A, the maximum expected leakage current is 6.5mA . The auxiliary IGBT current, flowing during the gating "off" of the main IGBT, was determined to be only 3.5mA for the full-load simulation. It is believed that this current is a PSPICE anomaly, but it will be difficult to measure the auxiliary IGBT current to prove otherwise.

Finally, the efficiency for the minimum load case was estimated to be 97.6 percent, which is lower than the maximum load case. This was expected as the soft-switching calculations were based on maximum loading. At minimum loading, the power loss is only 16 watts, so the IGBTs are not stressed in any way.

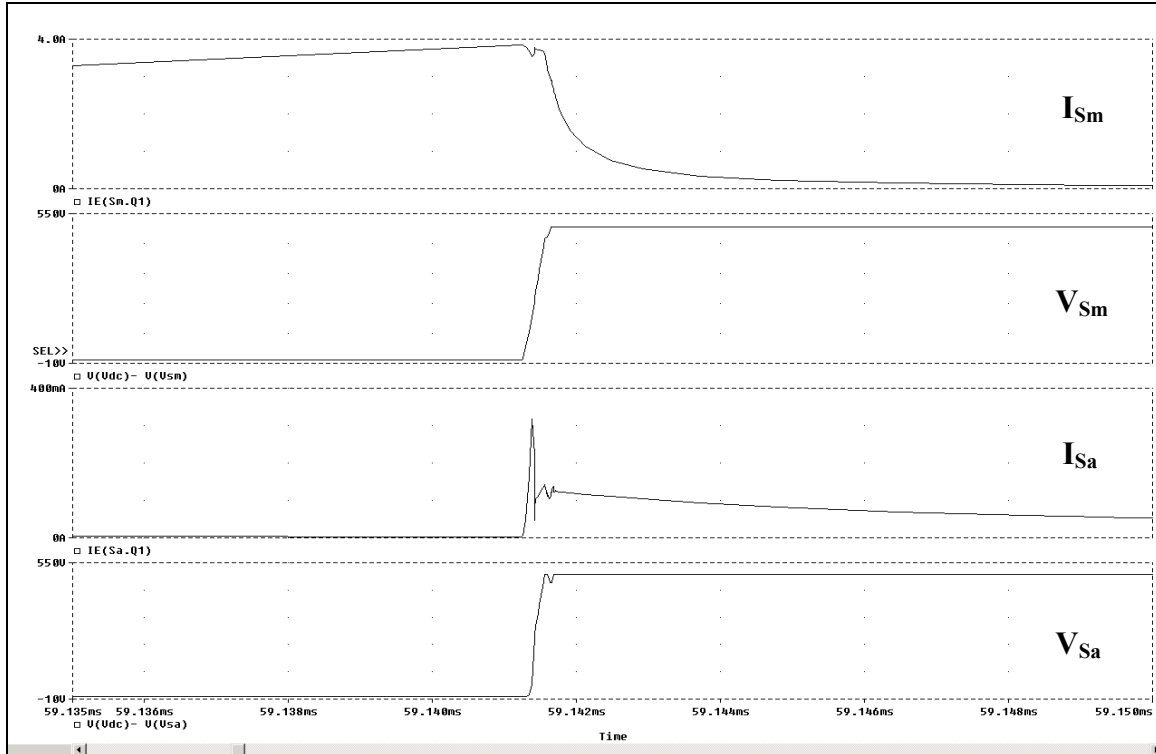


Figure 3-23. Voltage Across Main and Auxiliary Switch and Current Through Main and Auxiliary Switch During Turn-Off.

D. CHAPTER SUMMARY

In this chapter, the specifications for the resonant converter were listed and resonant component values were calculated based on the specifications. The concept of a semiconductor switch was presented and different families of power semiconductors were analyzed. The IGBT was selected for this design and a detailed PSPICE simulation was conducted for the maximum and minimum loading case.

In Chapter IV, the fabrication of the resonant converter is documented and test data is presented to verify the simulation results in this chapter.

IV. RESONANT CONVERTER CONSTRUCTION AND VALIDATION

A. CONVERTER CONSTRUCTION

This chapter contains a description of the construction of the overall converter, the power module and the testing performed to verify soft switching. In the discussion, the importance of component layout to minimize stray inductance is covered, as is the concept of a compact power module. The majority of the testing will be done at a full-load condition with an 80 percent duty cycle as specified in Table (3-1). The converter will also be tested at 10 percent of rated load to document performance near the transition to discontinuous current conduction mode. The results from the testing will uncover some unpredicted circuit behavior and the need to optimize the design to minimize switch losses.

When Naval Postgraduate School thesis students built power converters in the past, the circuits were laid out on a flat sheet of aluminum plate [22,23]. This layout technique had the advantage of being easy to build and maintain since all components were adjacent to each other with adequate clearance. In this design, the converter is part of a larger proposed power system and as such needed to be constructed in a typical 19-inch rack mount chassis. With the converter constructed in a 17-inch wide by 17-inch deep by 10-inch tall chassis, space was at a premium and the importance of cooling paramount. With a specified power rating of 8000 watts at 400 volts out, filter components become bulky making it even more difficult to build a converter in a small volume. The picture in Figure (4-1) shows all of the major components of the fabricated resonant converter. All of the major components of the converter are discussed in Chapter IV with the exception of the control and driver circuits, which are described in Appendix D.

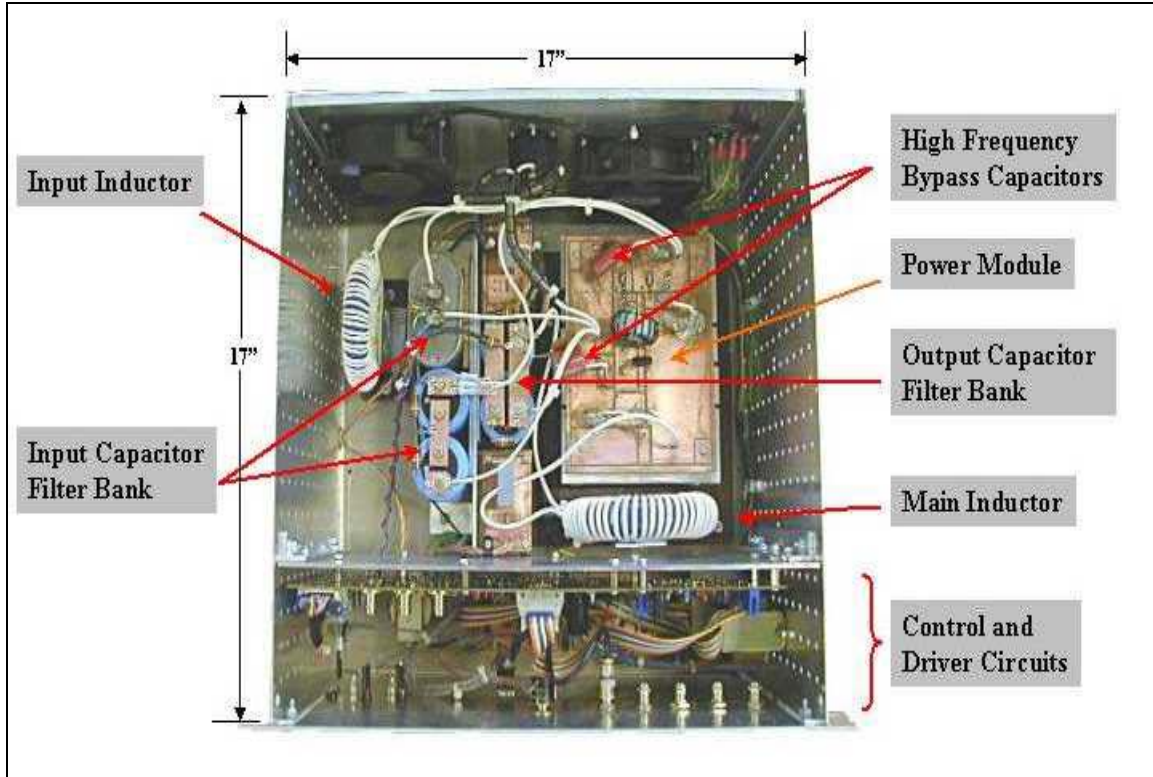


Figure 4-1. Top View of the Resonant Converter.

1. Input and Output Filter Component Selection

In addition to the circuit components discussed in Chapter III, an input filter section is required to isolate the converter input from the DC power source. The input filter section was not included in the Chapter III simulations as the source was ideal and does not suffer from the effects of large current changes with rich harmonic content. The completed power circuit is shown in Figure (4-2).

The input filter section is a standard LC design with the addition of a damping RC network. The filter was designed to have a pole pair (~ 450 Hz) above the 360 Hz ripple of the six-pulse rectified DC supply but well below the 20 kHz switching frequency. The 360 Hz ripple is allowed to pass through the converter so that DC stability analysis can be performed. Researchers working with the Energy Sources Analysis Consortium (ESAC) are interested in testing a nonlinear stabilizing control architecture and do not want the DC ZEDS test bed to be unconditionally stable due to large amounts of capacitance on the DC bus [4].

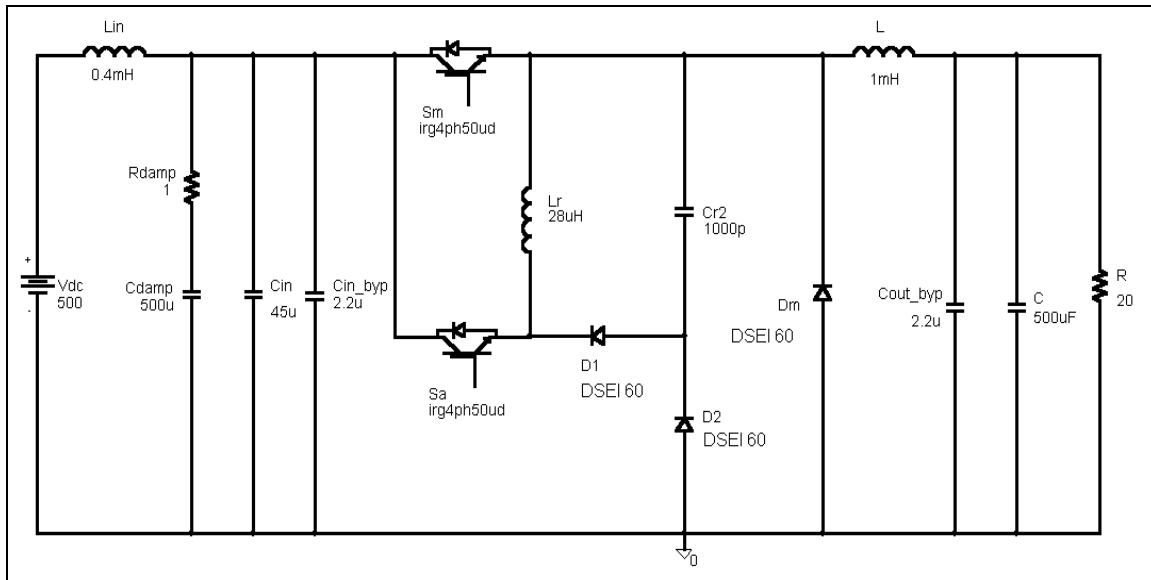


Figure 4-2. Complete Converter Circuit With Input Filtering Included.

The damping network was designed using the guidance provided in reference [24] and its function is to lower the resonant peak that would otherwise occur with a standard LC filter. The input inductor was wound on a 4-inch O.D. $\mu=60$ core for an inductance of 0.4mH. With approximately 16 amps of direct current flowing at rated power, the core will have an effective permeability of 40-60 percent yielding an inductance of approximately 250uH and a 3dB filter cutoff of 450 Hz. The construction of toroidal core inductors is a well-understood science and is documented in reference [25] and thoroughly demonstrated in reference [5]. The main inductor was also designed using the guidance of reference [25] and was wound on a 5.2-inch $\mu=147$ core. As discussed in Chapter III along with the input filter inductor discussion above, the large DC output bias current (20A at full-load) reduces the permeability by 50 percent thus doubling the expected peak-to-peak ripple current. Each of these hand-wound inductors will however approximate its designed value at minimum load (10%).

The selection of the input and output filter capacitors is also critical. The designer must carefully choose the proper type of capacitor for service in converters and be aware of the working voltage and ripple current ratings. Normally, electrolytic capacitors are used in converters because a large amount of filtering capacitance is required. Different

grades of electrolytic capacitors exist and choosing the wrong one for this design would be disastrous. The grade of capacitor chosen for this design is commonly called the switch-grade electrolytic. This capacitor has been designed to handle a high amount of ripple current without overheating over an extended life. To qualify as a good high-frequency switching capacitor, the capacitor must have a low Equivalent Series Resistance (ESR) and low Equivalent Series Inductance (ESL) [26]. All real capacitors have some amount of series and leakage resistance along with a small amount of series inductance.

An equivalent circuit used to model a real capacitor is shown in Figure (4-3). The ESR is a combination of the resistance of the internal wire resistance and a frequency dependant leakage term. The amount of ESR that a capacitor has determines the amount of ripple current that can flow through the capacitor without causing a significant amount of I^2R heat buildup.

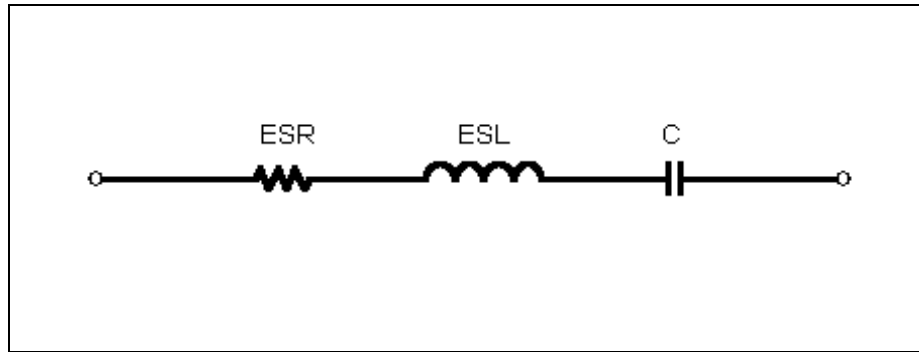


Figure 4-3. Equivalent Capacitor Circuit.

The ESR of a capacitor is given by Equation (4-1).

$$ESR = R_w + \frac{1}{\omega^2 R_{leak} C^2} \quad (4-1)$$

Equation (4-1) illustrates that as the ripple frequency increases, the ESR of the capacitor decreases. In this design, a series-pair of Mallory CGH102T450V3L 1000 μ F capacitors was used for a total working voltage of 900 V_{dc} at 500 μ F. At 120 Hz, the ESR is

83.4m Ω and at 20 kHz the ESR is 53.4 m Ω , which allows the capacitor to handle 35 percent more ripple current at the higher switching frequency. As an example, a standard Mallory computer-grade capacitor with the same voltage rating and capacitance has an ESR of 103 m Ω at 120 Hz, resulting in a ripple current rating roughly 80 percent of the switching-grade capacitor. The computer-grade capacitor does not have a ripple current rating for 20 kHz. The data sheets for both the switching and computer grade capacitors are provided in Appendix A. The other capacitor used in the input filter section is a 45 μ F AC motor-starting capacitor, which has a very low ESR and is not a limiting component in the design.

Another equally important parameter of the capacitor is the equivalent series inductance (ESL). Analysis of the circuit in Figure (4-3) shows that at some frequency a resonance condition will occur and above this frequency the capacitor will look like an inductor! The switching-grade capacitors have a lower ESL than standard computer-grade capacitors and as a result, the switching-grade capacitors are required for higher switching frequencies. A large electrolytic capacitor might have a resonant frequency as low as 20 kHz. Above the resonant frequency, the electrolytic capacitor will look inductive; therefore, additional capacitors must be used to bypass high-frequency noise spikes. Suitable bypass capacitors have mica, ceramic or polyester dielectrics with voltage ratings that exceed V_{dc} and at least 1.0 μ F of capacitance. In this design, 2.2 μ F 630 volt polyester capacitors were used and they are labeled in Figures (4-1) and (4-9).

2. Power Module Design and Layout

In any power converter design, the engineer must always strive to minimize stray inductance. All power converters have circuit paths that undergo large current changes, which can result in the buildup of large voltages if an inductance is present. This is demonstrated by Equation (4-2).

$$V = L_{\text{stray}} \frac{di}{dt} \quad (4-2)$$

In this converter design, PSPICE simulations have demonstrated that extremely high current rate changes occur throughout the circuit. In the path between the main switch and the main diode, the current changes over 100 amps in a microsecond. Equation (4-2) confirms that a small amount of inductance undergoing this di/dt can develop a large voltage transient and the IGBT switches can be destroyed. In the resonant converter there are five such nodes where the stray inductance must be minimized to ensure proper circuit operation. Figure (4-4) enumerates the five critical nodes, which are the red circuit traces.

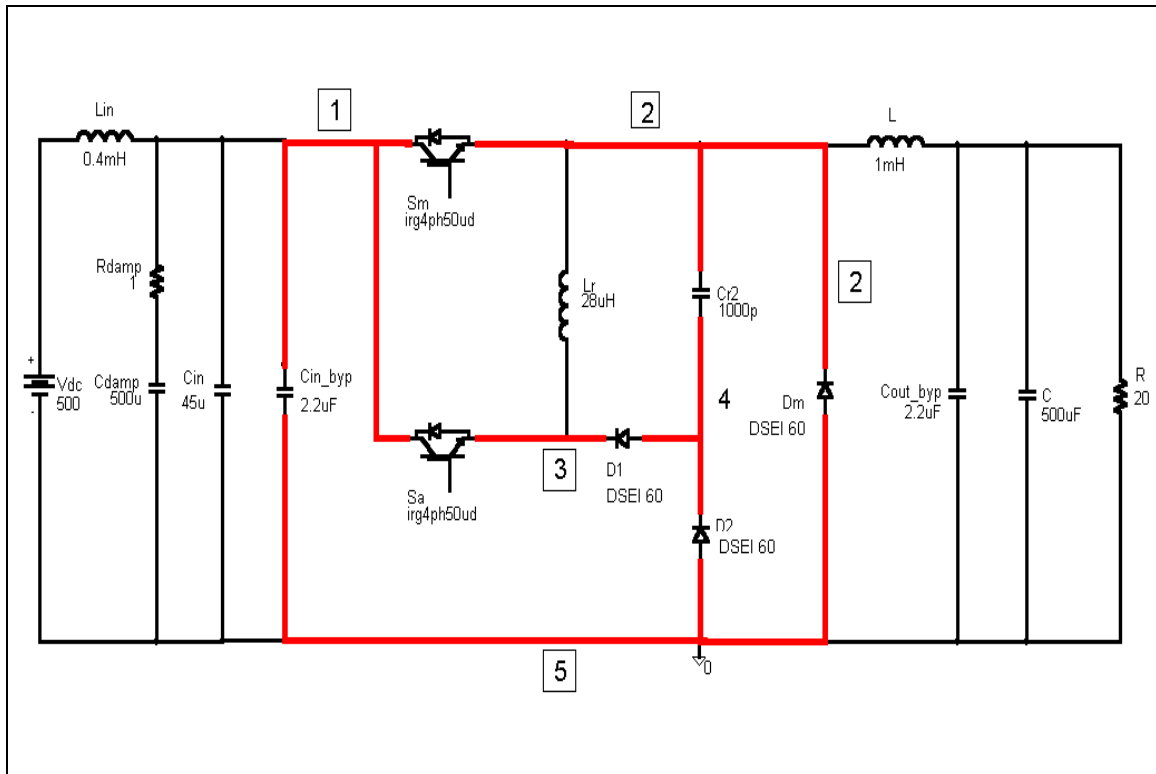


Figure 4-4. Resonant Converter Schematic Showing Critical Nodes.

Standard IGBTs such as the Semikron SKM100GB124D have an additional built-in switch along with an anti-paralleling diode. In reference [5], the secondary switch gate was left shorted and the additional anti-paralleling diode was used as the freewheeling diode. The freewheeling diode serves in the same capacity as the main diode D_m of the resonant converter design. This path between S_m and D_m is the most critical stray

inductance path and manufacturers design the power IGBT modules with this in mind. Since the design in this thesis uses discrete diodes and IGBTs, the stray inductance problem is even more difficult to overcome with the addition of the four other critical paths. To solve the problem, all circuit paths within the dashed lines of Figure (4-4) are laid out on a single-sided pc board much like an RF circuit design. Using this construction technique minimizes stray inductance and capacitance and enables the designer to build a high-powered converter in a small volume.

The circuit overlay was designed using Easytrax version 2.06 and the single-sided glass epoxy board was cut using the LPKF router/milling system. The power module circuit board overlay is shown in Figure (4-5) along with the labeled component locations.

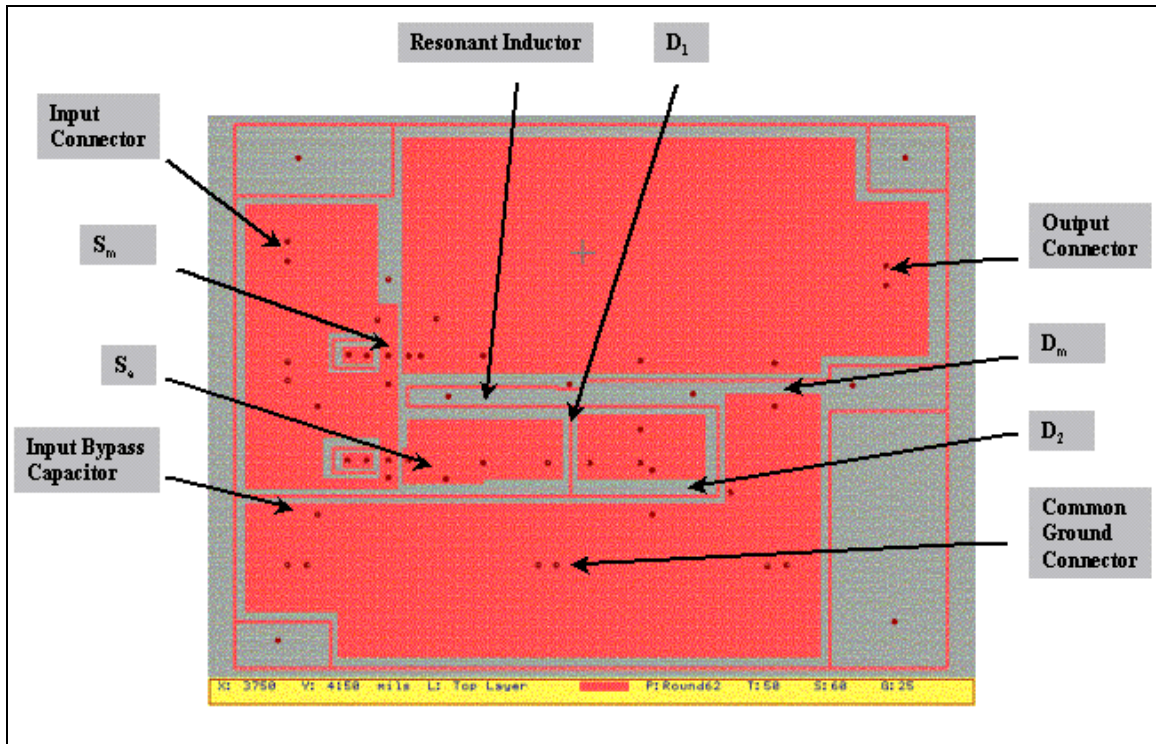


Figure 4-5. Power Module Circuit Overlay.

The wide traces used in the circuit board in Figure (4-5) serve two purposes. First, wide traces are required to handle the large current densities that exist. All of the

wiring in the high-current paths external to the power module was completed using #14 Teflon insulated wire. From reference [16], #14 wire has a cross-sectional area of approximately 2.08 mm^2 and can safely handle a current density of 1000 amps/cm^2 if properly cooled. The current paths in the module must handle a maximum of 20 amps; therefore, a copper trace of the proper width must be used with an effective cross-sectional area of at least 2.08 mm^2 . Since 1oz copper glass epoxy board has a thickness of 0.0014-inches, trace widths of 2.3-inches will meet the current density requirements.

$$20\text{amps} \times \frac{1}{2.3\text{inches}} \times \frac{1}{0.0014\text{inches}} \times \frac{1\text{inch}^2}{6.45\text{cm}^2} = 962.7 \frac{\text{amps}}{\text{cm}^2} \quad (4-3)$$

The completed circuit board is illustrated in Figure (4-6). All of the thin red traces of Figure (4-5) are isolation traces and were later ground away using a Dremel cutting tool in order to improve voltage isolation between the input, output and ground.

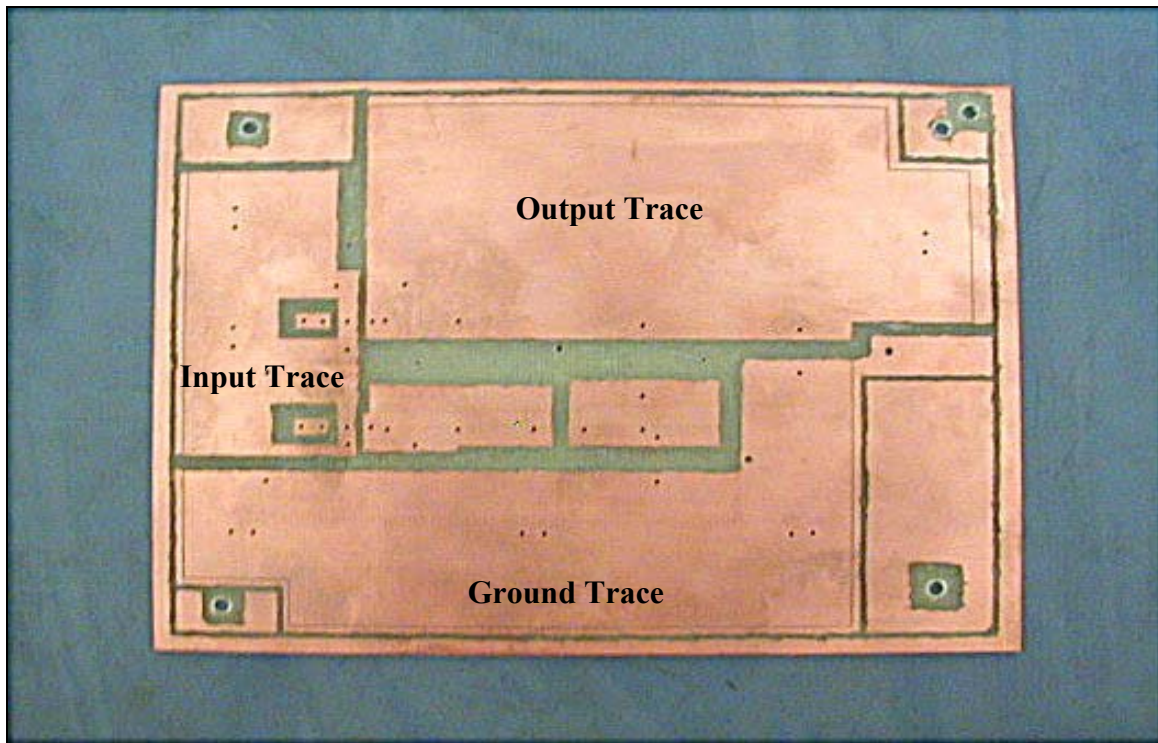


Figure 4-6. Photograph of Circuit Board After Milling Process.

With the circuit board cut, the heat sink assembly was constructed based on the thermal calculations listed in Appendix C. In order to improve thermal performance, no mica insulators were used and the heat sink was sliced up to isolate the different stages. The main and auxiliary IGBTs are on the same heat sink since both of the collectors are at the same potential. The sections of heat sink were then mounted on a fiberglass sheet and spaced properly for isolation. Figures (4-7) and (4-8) show the front and top view of the heat sink with the IGBTs and diodes installed.

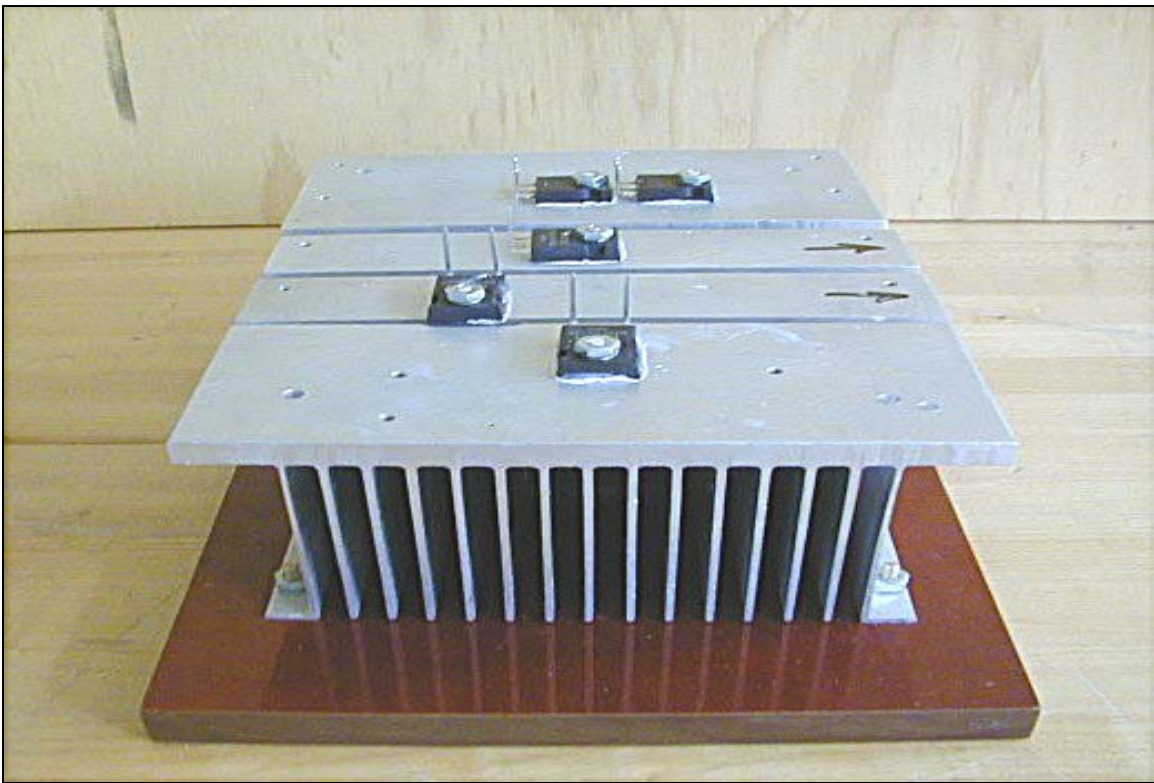


Figure 4-7. Front View of Heat Sink.

Next, the capacitors, Metal-Oxide Varistors (MOVs) and resonant inductor were soldered to the power module board. The 850-volt MOVs were placed across both IGBTs to protect the switches from an over-voltage failure. The completed circuit board was then placed on top of the heat sink assembly using standoff spacers, and the diode and IGBT leads were soldered to the circuit board. The completed power module is depicted in Figure (4-9).

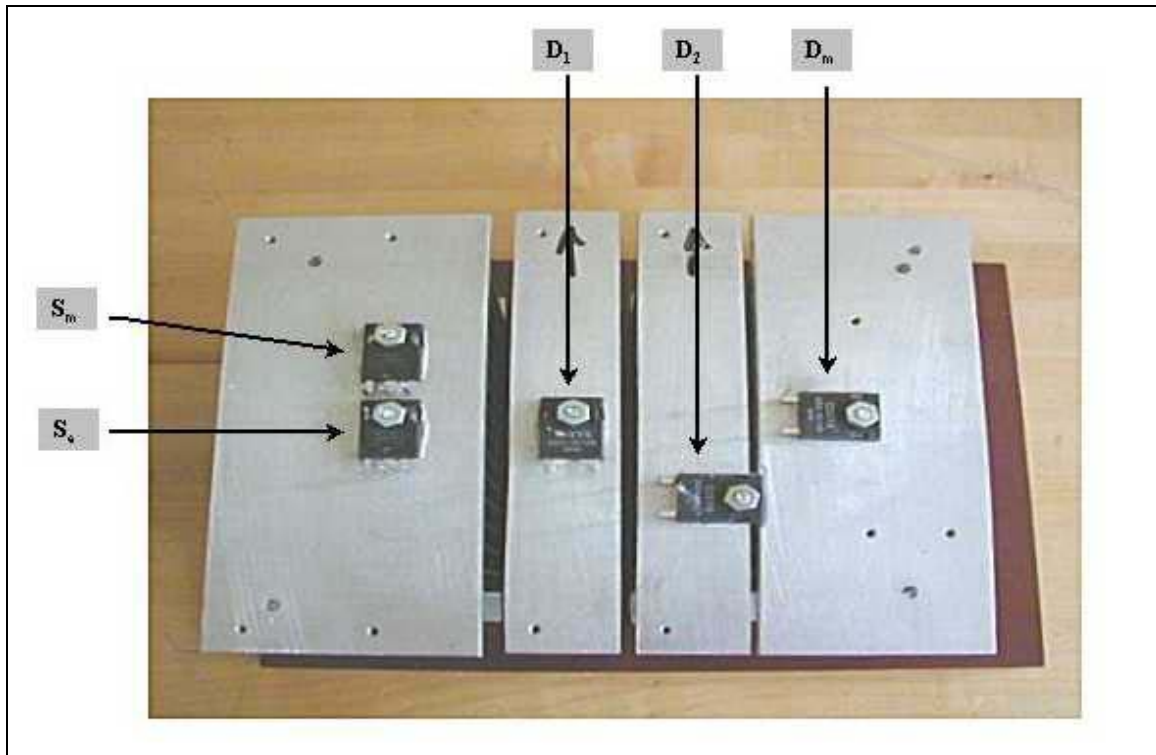


Figure 4-8. Top View of Heat Sink Assembly.

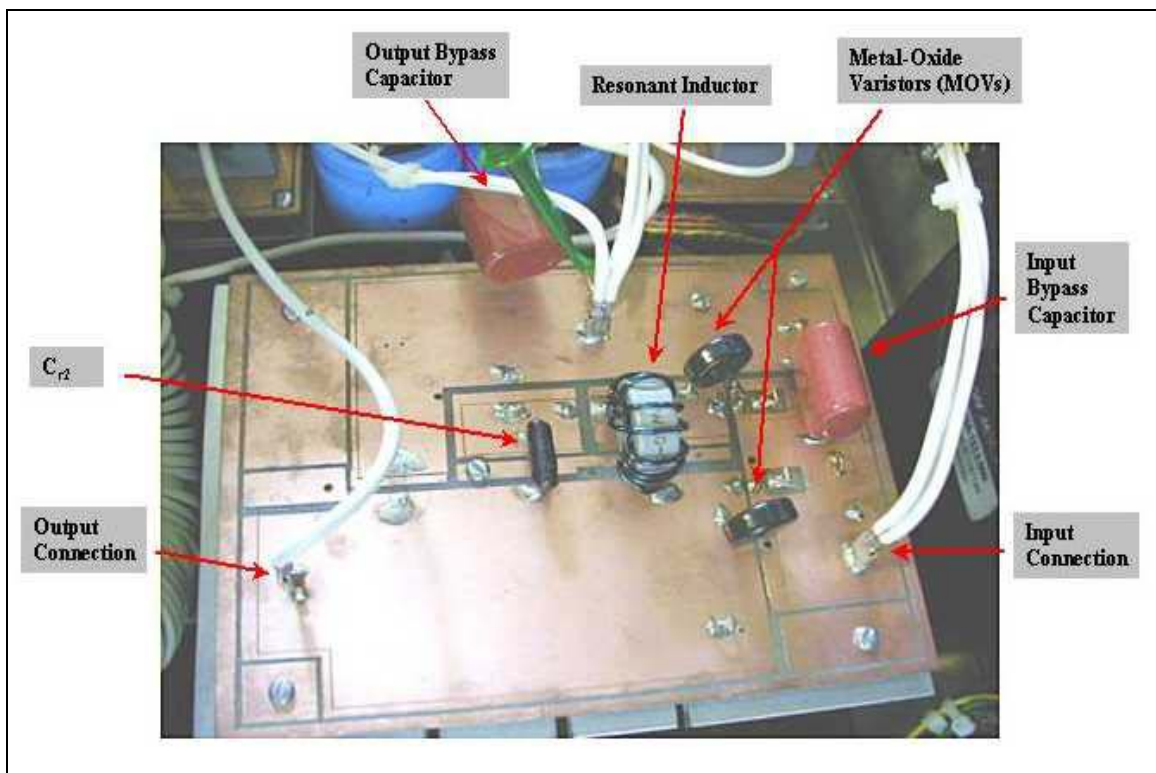


Figure 4-9. Completed Power Module.

3. Resonant Inductor Design

The resonant inductor is a critical component in the converter and choosing the wrong core material or size can be disastrous. The designer must calculate the maximum expected magnetic flux density ($B_{\max}$) in order to pick the proper core size. To design the resonant inductor, the inductor's current and voltage waveforms from PSPICE were used along with magnetic theory to determine $B_{\max}$. The waveforms in Figure (4-10) are based on an ideal inductor model, but will still yield accurate results as will be later demonstrated during testing.

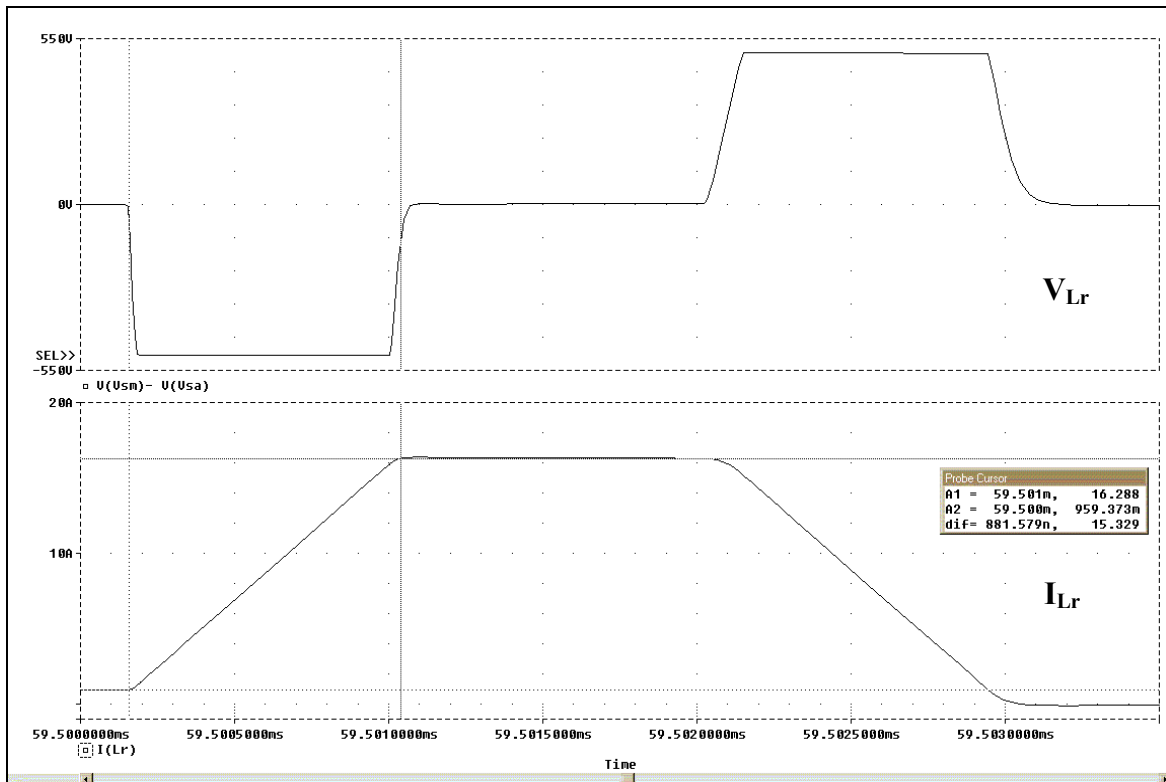


Figure 4-10. Resonant Inductor Voltage and Current Waveforms.

Several different toroidal cores were available in the NPS Power Laboratory, so a 1.57-inch $\mu=125$ iron powder core made by Arnold Engineering was selected. Normally a core size is chosen first, since the number of turns needed to yield the required inductance must be known before $B_{\max}$ can be calculated. If the calculations show that

the selected core is inadequate, the design process is repeated until a suitable core is found.

Using the effective core area (A_e), effective path length (l_e), relative permeability (μ) and inductance (L), the required number of turns (N) is found using Equation (4-4).

$$N = \sqrt{\frac{L l_e}{4\pi\mu A_e}} \quad (4-4)$$

Using the values from the A-254168-2 core data sheet in Appendix A and Equation (4-4), the required number of turns is 13 for an inductance of 28 μ H. With the number of turns known, the maximum magnetic flux is now calculated.

From Faraday's Law, the time-varying flux linkage ($N\phi$) of an inductor is related to the induced voltage by Equation (4-5).

$$V = N \frac{d\phi}{dt} \quad (4-5)$$

Using the voltage waveform of Figure (4-10), the maximum flux ($\phi_{\max}$) is found by integrating both sides of Equation (4-5) over the time that the inductor has a voltage across it. Since the inductor has both a negative and positive voltage pulse, only one of the pulses needs to be integrated as the other will cause a magnetic flux peak in the opposite direction. Using the voltage and pulse width in Figure (4-10), the maximum flux is found as follows:

$$\phi_{\max} = \frac{1}{N} \int_0^t V dt = \frac{1}{13} \int_0^{.881\mu s} 500 dt = 33.9e^{-6} \text{ Wb} \quad (4-6)$$

Using,

$$\phi = B A_e \quad (4-7)$$

Where A_e is the effective core cross-sectional area; the magnetic flux density B in units of Teslas is,

$$B_{\max} = \frac{\phi_{\max}}{A_e} = \frac{33.9e^{-6} \text{ Wb}}{107.2e^{-6} \text{ m}^2} = 0.316 \text{ T} \quad (4-8)$$

Since most published B-H curves use magnetic flux density in units of Gauss, the result is multiplied by 10^4 to convert from Teslas to units of Gauss.

$$B_{\max} = 3163.0 G \quad (4-9)$$

The calculated value of $B_{\max}$ is then found on a normalized B-H curve depicted in Figure (4-11) to see if the core is saturated.

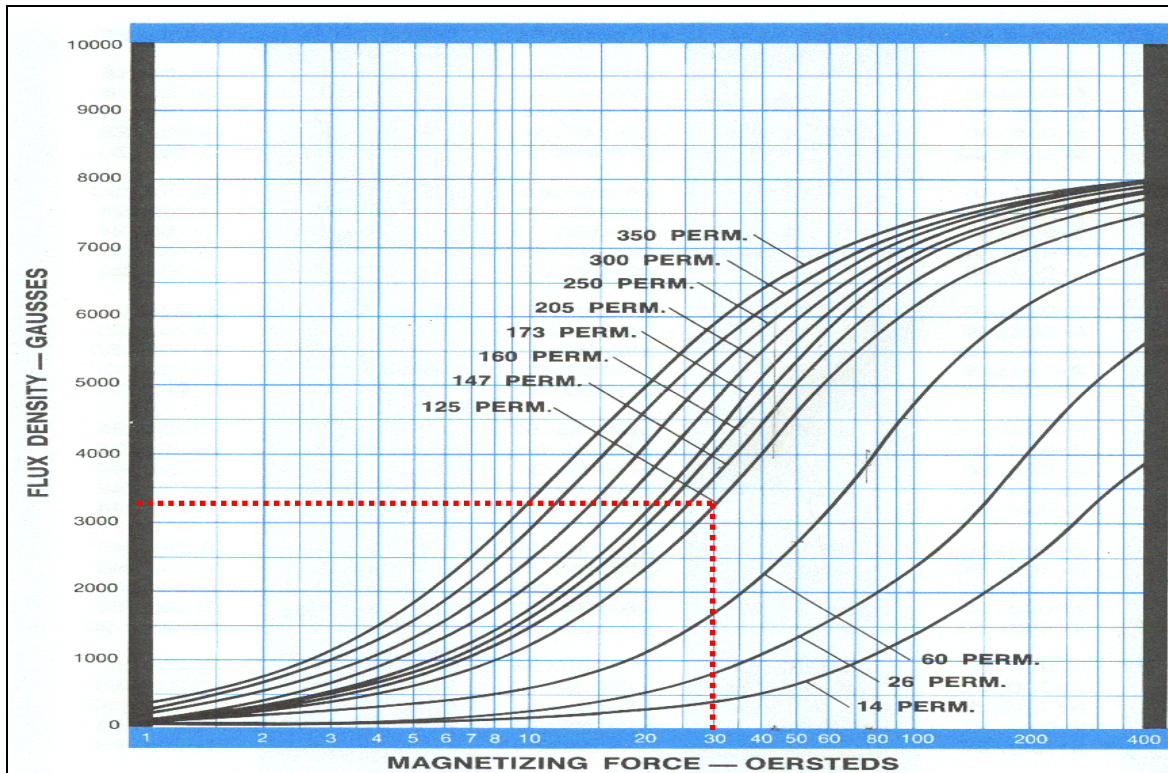


Figure 4-11. Normalized B-H Curve (from ref. [25]).

Inspecting Figure (4-11), the resulting magnetic flux density is half way up the $\mu=125$ curve in the linear region yielding a magnetizing force of 30 Oersteds. Based on the above calculations, a more compact equation is developed which returns a magnetic flux density in units of Gauss for the pulsed voltage case. The effective cross-sectional area is in cm^2 and the 10^8 term converts the cross-sectional area to m^2 and shifts the units from Teslas to Gauss.

$$B_{\max} = \frac{V \Delta t (10^8)}{A_e N} \quad (4-10)$$

The analysis shows that the selected core is adequate for this design and the waveforms of Figure (4-10) will be verified during the testing phase.

B. CONVERTER TESTING AND VALIDATION

The testing of the resonant converter for both maximum and minimum load as specified in Table 3-1 of Chapter III is described in this section. For both loading conditions, many of the voltage and current waveforms were measured and compared to the simulations of Chapter III. A schematic diagram of the basic test system is shown in Figure (4-12).

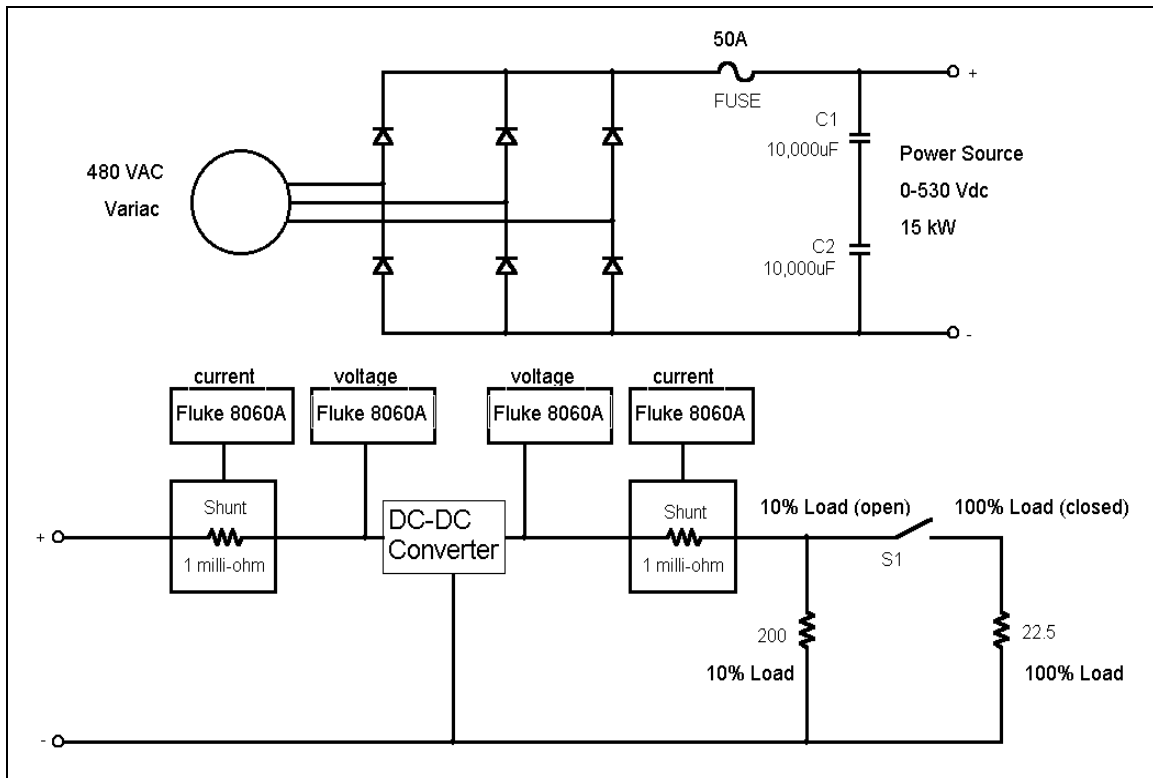


Figure 4-12. Basic Test Setup.

1. Test Setup

To test the converter, a DC power source capable of supplying a minimum of 8 kW was required. To meet the requirements, a 15 kW DC supply was constructed using a 480-volt 33kVA three-phase variac, coupled to a three-phase six-pulse rectifier bridge and a 5000 μ F capacitor filter bank. To monitor input and output DC current, a pair of 1m Ω current shunts with Fluke 8060A multimeters were used. Two other Fluke 8060A multimeters were also used to measure the input and output voltage. The remaining equipment used in the testing is listed in Table (4-1) and will be described in detail in the section where it was used.

Equipment	Manufacturer	Model Number	Ratings
Variac	Staco Energy Products	6020-3Y	3 ϕ /60Hz, 33 kVA
Power Diode Rectifier	INVER Power Controls LTD	P101 DM	50A
Filter Capacitors	INVER Power Controls LTD	P106 FC	10,000 MFD, 350 WVDC
Resistor Load bank	INVER Power Controls LTD	P108-RL	3000 Watts
Non-Inductive Current Shunts	INVER Power Controls LTD	P109-NIS	1m Ω
Digital Multimeter	Fluke	8060A	750 volts DC
Digital Oscilloscope	Tektronix	TDS 540	500 MHz , 4 channel
HV Differential Probe	Tektronix	P5200	1300 volts DC
Current Probe Amplifier	Tektronix	AM503A	N/A
Current Probe	Tektronix	A6303	100 A
Current Probe	Tektronix	A6302	20 A
DC Supply	Tektronix	PS280	0-30 volts DC/1A
LC Meter	Sencore	LC53	1pF-0.2F / 1uH-10H
Printer	Hewlett-Packard	Laserjet 5	N/A

Table 4-1. Laboratory Equipment Used During Testing.

2. Full-Load Efficiency Testing

Before any specific voltage or current waveforms were verified, the efficiency as a function of duty cycle was measured using the Fluke 8060A meters. Table (4-2) lists the voltage and currents measured and the calculated power loss and efficiency. Table (4-2) also compares the soft-switching efficiency to the hard-switching converter from reference [5].

Duty Cycle (%)	Soft-Switching Data						Efficiency η Soft-Switched Percent	Efficiency η Hard-Switched Percent
	V_{in}	I_{in}	V_{load}	I_{load}	P_{in}	P_{out}		
	Volts	Amps	Volts	Amps	Watts	Watts		
10	500.4	0.35	54.3	2.72	175.1	147.7	84.3	82.5
20	500.3	1.11	101.8	5.08	555.3	517.1	93.1	91.1
30	500.4	2.47	153.8	7.67	1236.0	1179.6	95.4	93.7
40	500.5	4.32	204.7	10.19	2162.2	2085.9	96.5	95.3
50	500.3	6.55	252.8	12.59	3277.0	3182.8	97.1	96.1
60	500.5	9.33	302.5	15.05	4669.7	4552.6	97.5	96.8
70	500.5	12.49	350.4	17.43	6251.3	6107.5	97.7	97.2
80	500.8	16.25	400.3	19.90	8138.0	7966.0	97.9	97.6

Table 4-2. Soft and Hard-Switched Converter Full-Load Efficiency for Duty Cycles Ranging Between 10% and 80%.

The data confirms that the soft-switched efficiency at 80 percent duty cycle is 0.3 percent better than the hard-switched converter. This is a power dissipation difference of only 25 watts while supplying 8000 watts to the load. The estimated soft-switching efficiency in the Chapter III PSPICE simulation was 98.4 percent, yielding a difference of 41.5 watts when compared to the measured efficiency. The converter efficiency is excellent throughout the duty cycle range and does not drop off significantly until a duty cycle of 10 percent. The power levels at $D=0.1$ are so low that the reduced efficiency is of no

practical concern. A plot of the soft and hard-switched converter efficiency versus duty cycle is shown in Figure (4-13).

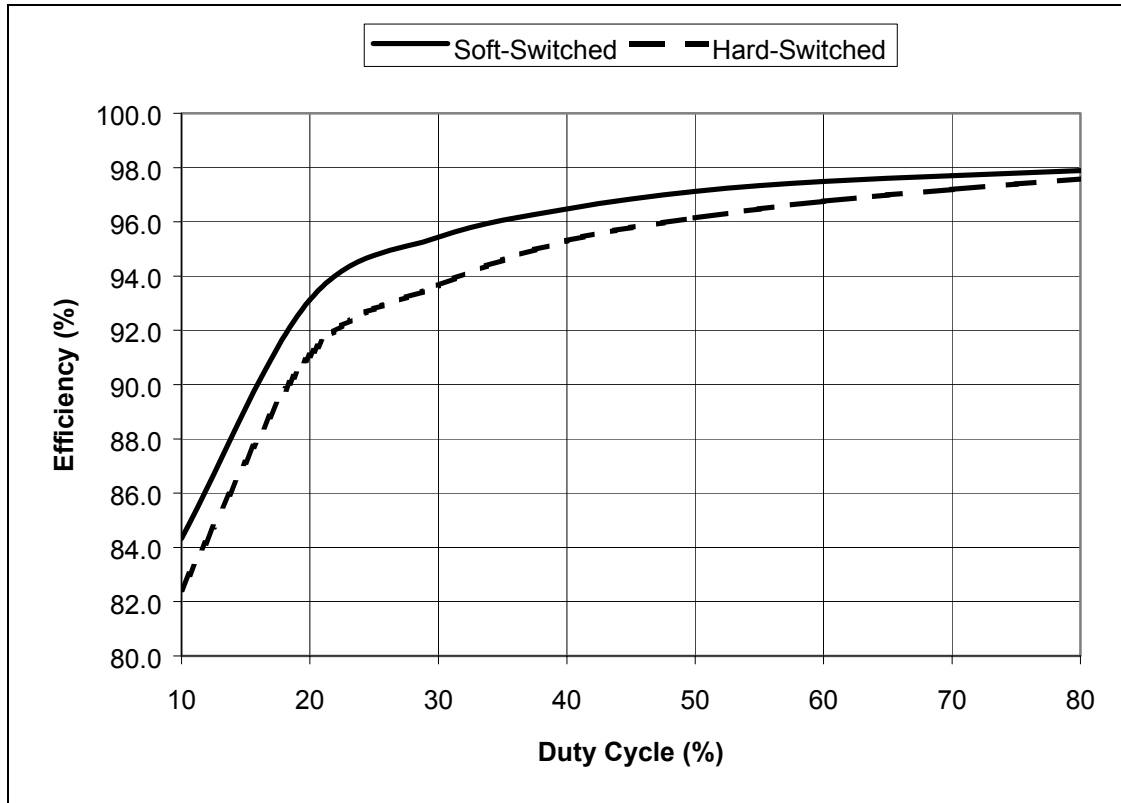


Figure 4-13. Efficiency Versus Duty Cycle for Hard and Soft-Switched Converters.

3. Full-Load Waveform Analysis

To complete the full-load testing, the testing diagram in Figure (4-12) was used along with a Tektronix TDS-540 oscilloscope, P5200 high-voltage differential probes, AM503A current probe amplifier and A6303/A6302 current probes. With the basic characteristics of the converter verified, the various voltages and currents were observed and compared to the PSPICE simulation. Measurement of the circuit currents was difficult, as all of the paths, with the exception of the main inductor and input/output current, exist on the circuit board. During the testing phase, several of the traces were cut and bridged with #14 Teflon insulated wire in an attempt to analyze the current waveform using a current probe. The Tektronix A6302 current probe inserts approximately $0.5\mu\text{H}$ of stray inductance, which was verified on the Sencore LC53 inductance meter. The

power module layout dictated that the auxiliary current be measured on the input to the switch and the stray inductance of the current probe upset the circuit operation. In the end, the currents through the main switch S_m , main diode D_m , resonant inductor L_r and diode D_2 were measured. The circuit layout also prevented the measurement of the currents through diode D_1 and capacitor C_{r2} . The circuit paths measured are critical stray inductance paths as defined in Figure (4-4) and subsequent oscilloscope plots confirm that the probe's inductance did change the voltage waveforms.

The gating signals measured directly at the IGBTs are shown in Figure (4-14). The gating signals closely match the simulated waveforms illustrated in Figure (3-10). The effects of gate-capacitance-charge-up are depicted as discussed in reference [6] and the shut-off transient from the auxiliary driver circuit is coupled into the main driver circuitry. The design of the driver circuitry is discussed in Appendix D.

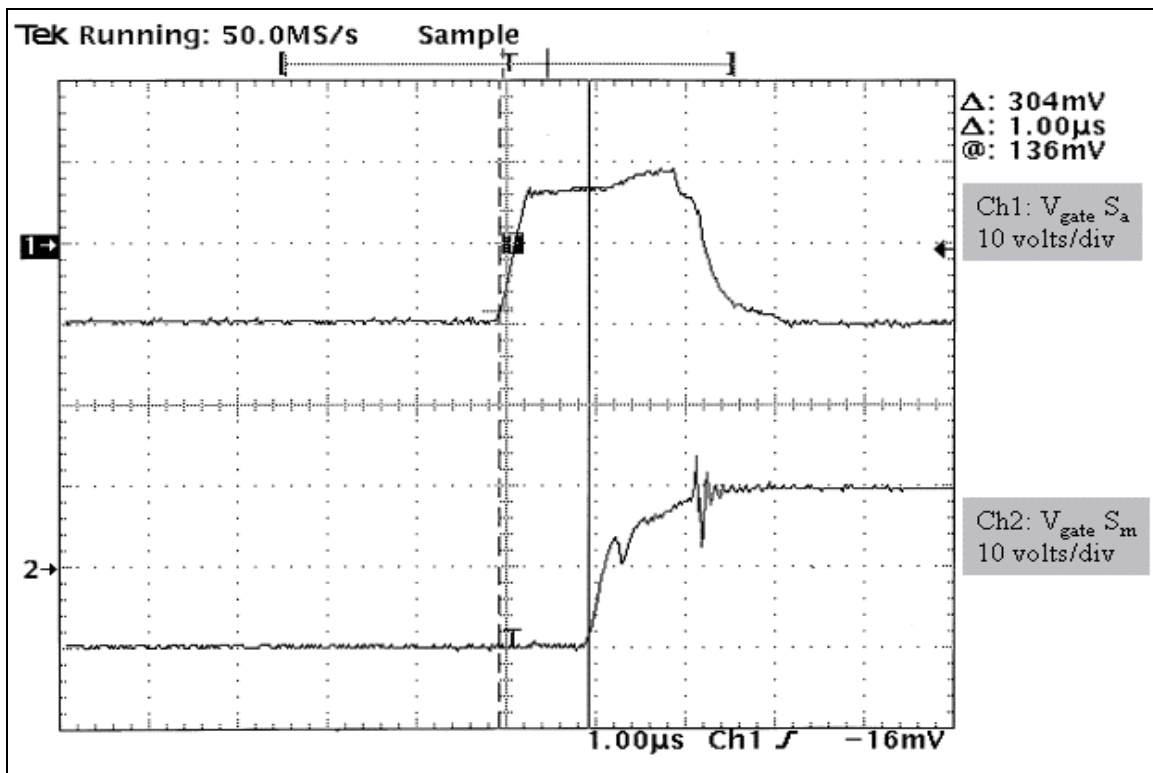


Figure 4-14. Auxiliary and Main IGBT Gating Signals (1µs/div).

Next, the voltage across S_m is compared to the current through the main inductor in Figure (4-15). As expected, when the voltage across S_m is at $V_{ce(sat)}$, the current through L builds linearly. When S_m is gated "off," D_m forward biases "on" and the current through L decreases linearly. As predicted in Chapter III, the ripple current $I_{L,max}-I_{L,min}$ is verified to be 8 amps with an average current of 20 amps. The transients occurring at the bottom of the inductor current trace are associated with the gating "on" of S_a and the subsequent current buildup through L_r .

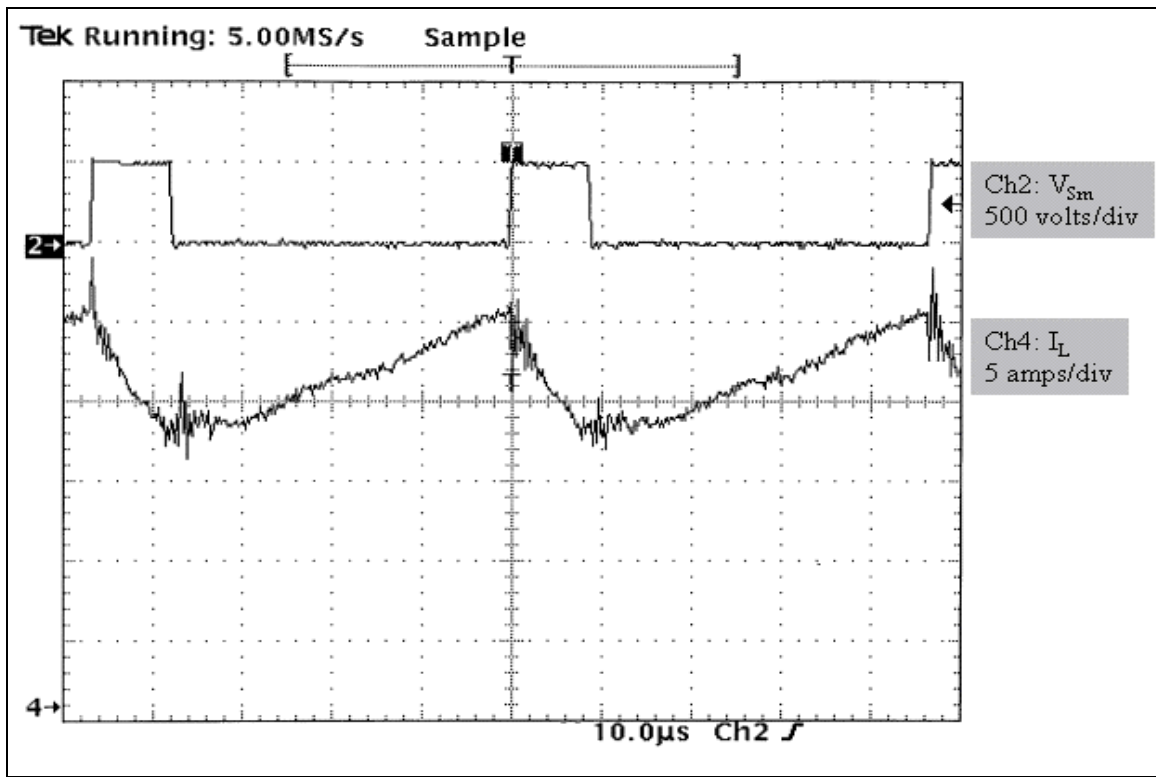


Figure 4-15. Voltage Across Main Switch and Current Through Main Inductor (10 μ s/div).

The voltage and current waveforms for the main diode D_m are shown in Figure (4-16). With V_{Dm} going to zero (S_m gated "off"), D_m is forward biased "on" to maintain the current through the main inductor. The current through D_m quickly reaches $I_{L,max}$ and then linearly decreases as it transfers energy to the load. Figure (4-17) shows the forward recovery of D_m as V_{Dm} decreases at a rate of 3000 V/ μ s. During the forward recovery

period of 117ns, I_{Dm} reaches approximately 2.5 amps. From reference [24], the forward recovery charge is given by:

$$Q_{fr} = \frac{1}{2} I_{RM} \tau_{fr} = 146nC. \quad (4-11)$$

The parasitics caused by the inductance of the current probe made it impossible to measure the reverse recovery of D_m . Parasitic oscillations are clearly seen in Figure (4-16) during the linear portion of I_{Dm} and again in Figure (4-17) when D_m is starved of current.

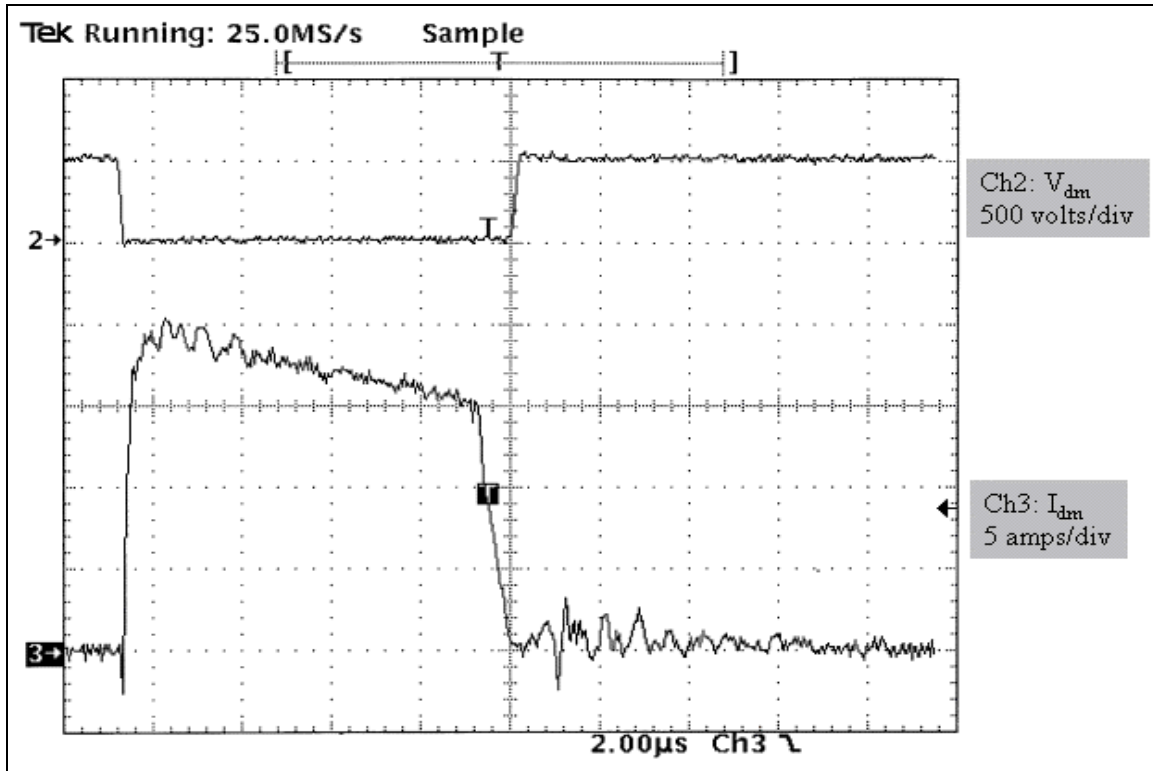


Figure 4-16. Voltage Across Main Diode and Current Through Main Diode (2µs/div).

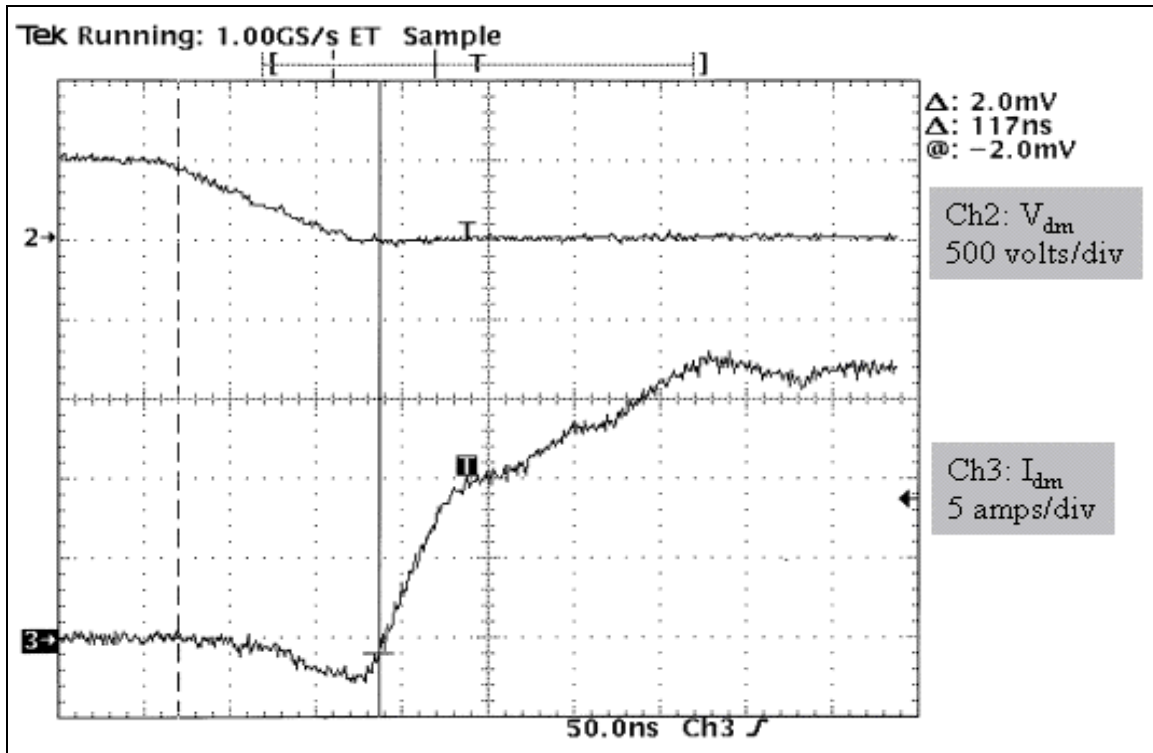


Figure 4-17. Forward Recovery of the Main Diode (50ns/div).

Next, Figure (4-18) illustrates the voltage across and current through the main switch during turn-on. As a comparison, the voltage across the auxiliary switch and the current through the resonant inductor is shown in Figure (4-19). Figure (4-18) verifies that S_m undergoes ZVS during turn-on. When V_{sm} reaches approximately zero volts, a negative current flows back to the source through D_{sm} . The duration of the negative current is approximately $1\mu s$ and the subsequent positive buildup of the current coincides with the gating "off" of S_a as shown in Figure (4-19). In the PSPICE simulation results shown in Figure (3-14), a similar negative current through D_{sm} occurs, but the amplitude is somewhat smaller.

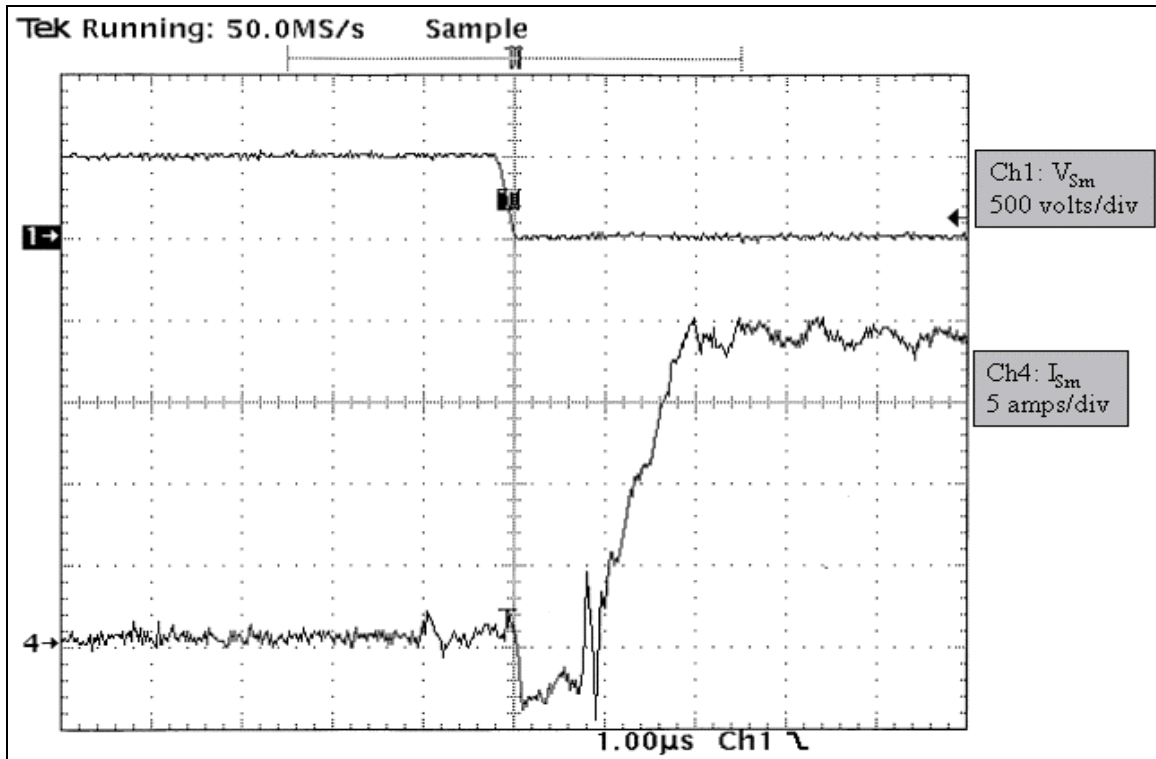


Figure 4-18. Voltage Across S_m and Current Through S_m During Turn-On (1μ s/div).

Upon inspection of Figure (4-19), it is seen that S_m is gated "on" just as the current through L_r reaches a maximum of roughly 20 amps. From Figure (4-15), the main inductor reaches a minimum of approximately 17 amps during the same period, so a current mismatch occurs. The resonant inductor wants the current flow to remain the same and thus back flows this difference through D_{S_m} for a short time. The resonant inductor current overshoots $I_{L,min}$ of the main inductor partly due to the energy transferred from C_{r1} (mode 3) and more from the energy buildup during the recovery of D_m . Since C_{r1} is on the order of 100pF, the resulting energy transferred to L_r is small and the majority of the excess energy is from the recovery of D_m . Apparently, the PSPICE model used for the diodes is not completely adequate as it fails to predict such a large reverse current.

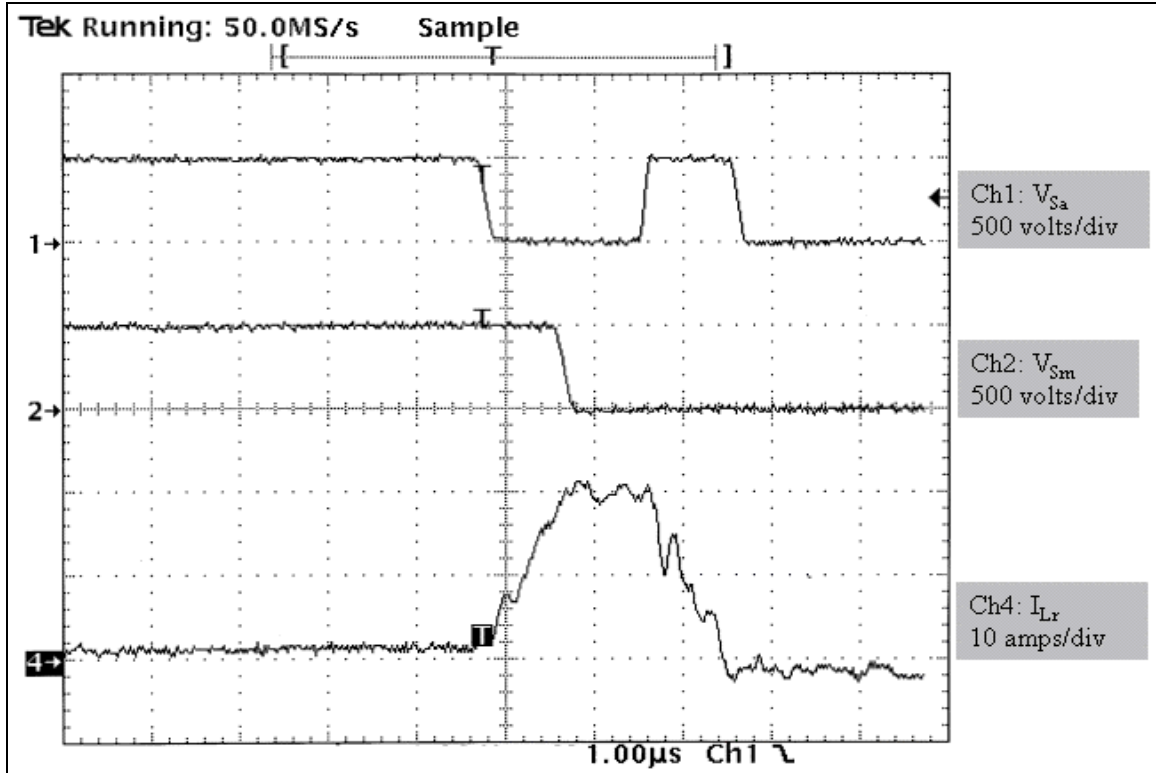


Figure 4-19. Voltage Across S_m and S_a and Current Through L_r (1 μ s/div).

In Figure (4-19), I_{Lr} has a slope of approximately 20 A/ μ s during the current buildup. With V_{dc} equal to 500 volts, this equates to an inductance of 25 μ H.

$$L = V \frac{\Delta t}{\Delta i} = 25 \mu\text{H} \quad (4-12)$$

During construction, the resonant inductor was verified to be 28 μ H using the Sencore LC53 inductance meter. The reduction in the resonant inductance is most likely due to non-linearities in the B-H curve as a large dv/dt is placed across a fairly small core.

Figure (4-20) compares the auxiliary switch voltage to the voltage across diode D_2 and the current through D_2 .

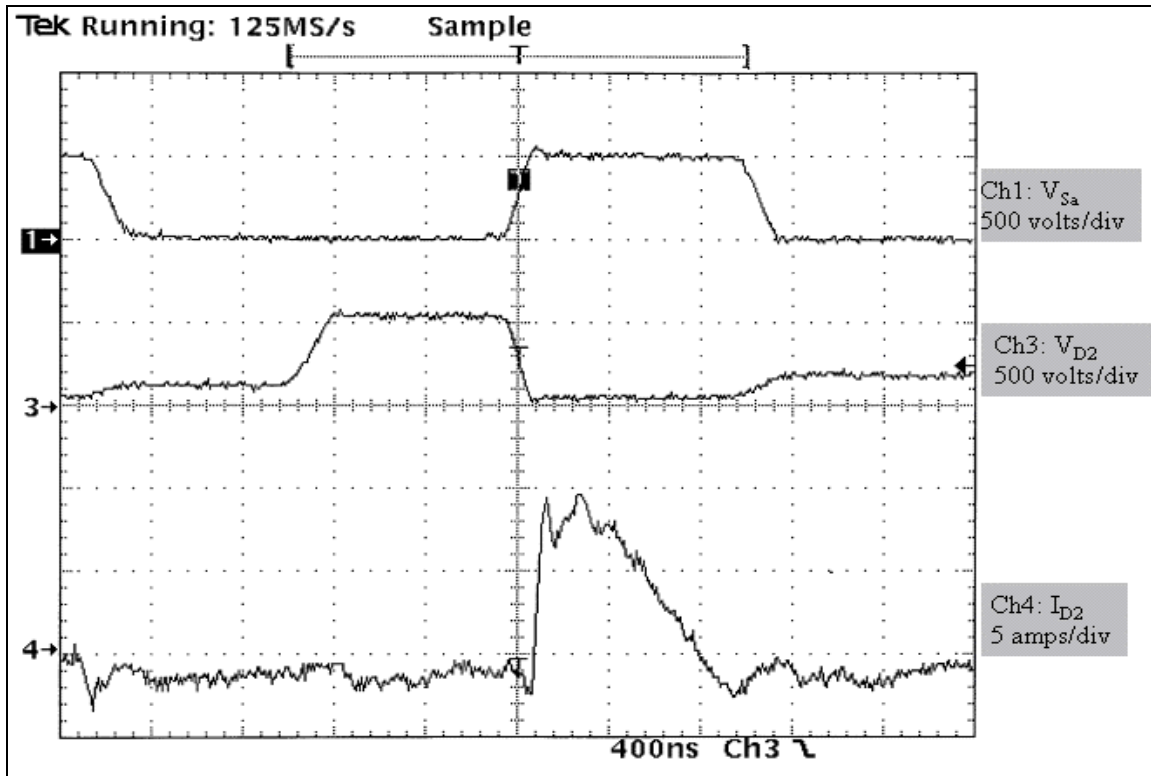


Figure 4-20. Voltage Across S_a and D_2 and Current Through D_2 (400ns/div).

When S_a is gated "off," Figure (4-20) shows that D_2 is almost immediately forward biased "on." From the analysis of Chapter II, D_2 is forward biased only if mode 5x occurs and then later during mode 7 when C_{r2} discharges as S_m is gated "off." During mode 5x, the current I_{D2} rapidly builds up and then decreases linearly as the energy leaves L_r . Chapter V will address the excessive length of mode 5x and discuss the importance of minimizing this mode.

Figure (4-21) compares the voltage across S_a , D_2 , D_1 and C_{r2} during all modes of operation. The PSpice simulation illustrated in Figure (3-18) predicted the basic shape and timing of the waveforms, but failed to predict the voltage changes across D_1 , D_2 and C_{r2} as the converter transitions into mode 6.

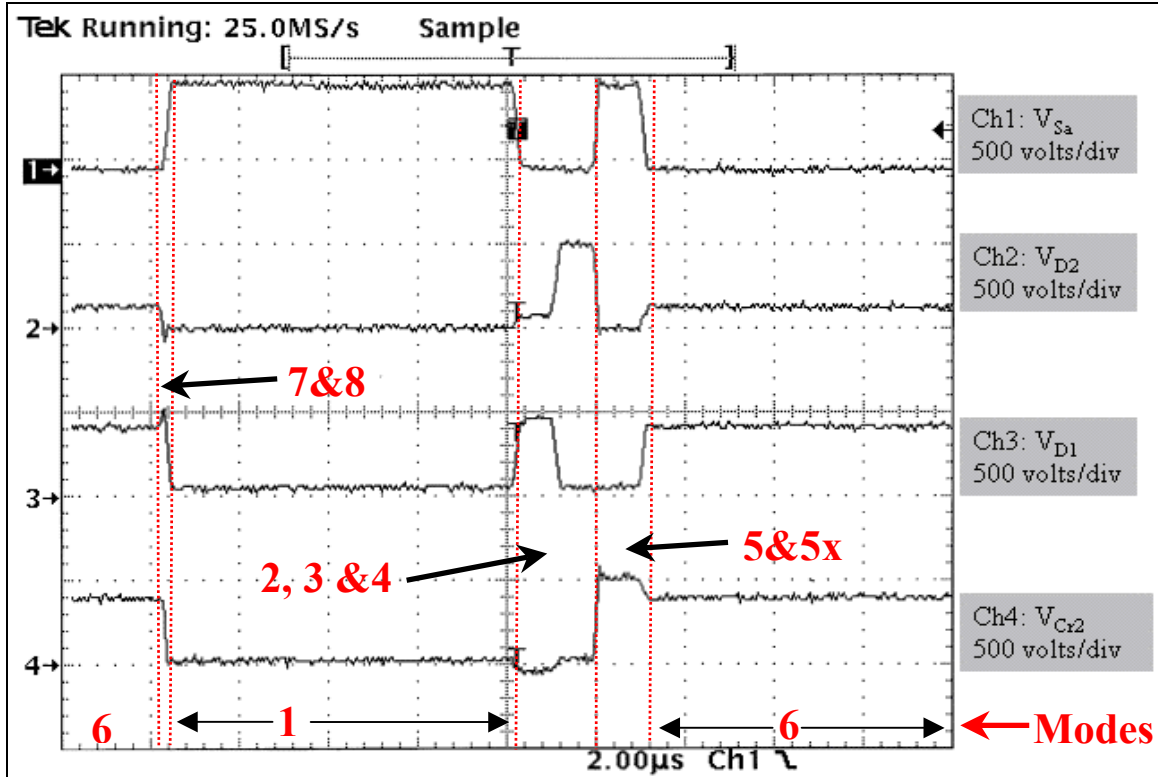


Figure 4-21. Comparison of the Voltages Across S_a , D_2 , D_1 and C_{r2} During Modes 1 Through 8 (2µs/div).

During mode 1, all waveforms match the simulations in Chapter III. When mode 2 commences, V_{Sa} goes low, V_{D1} increases to approximately V_{dc} , and V_{Cr2} goes slightly negative since S_m is still gated "off." When S_m is gated "on" in mode 4, V_{D1} goes low and V_{D2} increases to V_{dc} , and V_{Cr2} returns to zero. At the end of mode 4, S_a is gated "off" and mode 5 and 5x commence and V_{Cr2} rises to V_{dc} . Mode 5x is dominant and V_{D2} immediately goes to zero. When D_1 and D_2 are starved of current, a reverse recovery process occurs, which causes D_1 and D_2 to have unequal voltage drops, although their sum must equal V_{dc} . Since V_{Cr2} was originally equal to V_{dc} , C_{r2} discharges until $V_{Cr2} + V_{D2} = V_{dc}$. Figure (4-22) shows an expanded view of V_{Sa} and I_{Lr} and the characteristics of the reverse recovery of D_1 and D_2 .

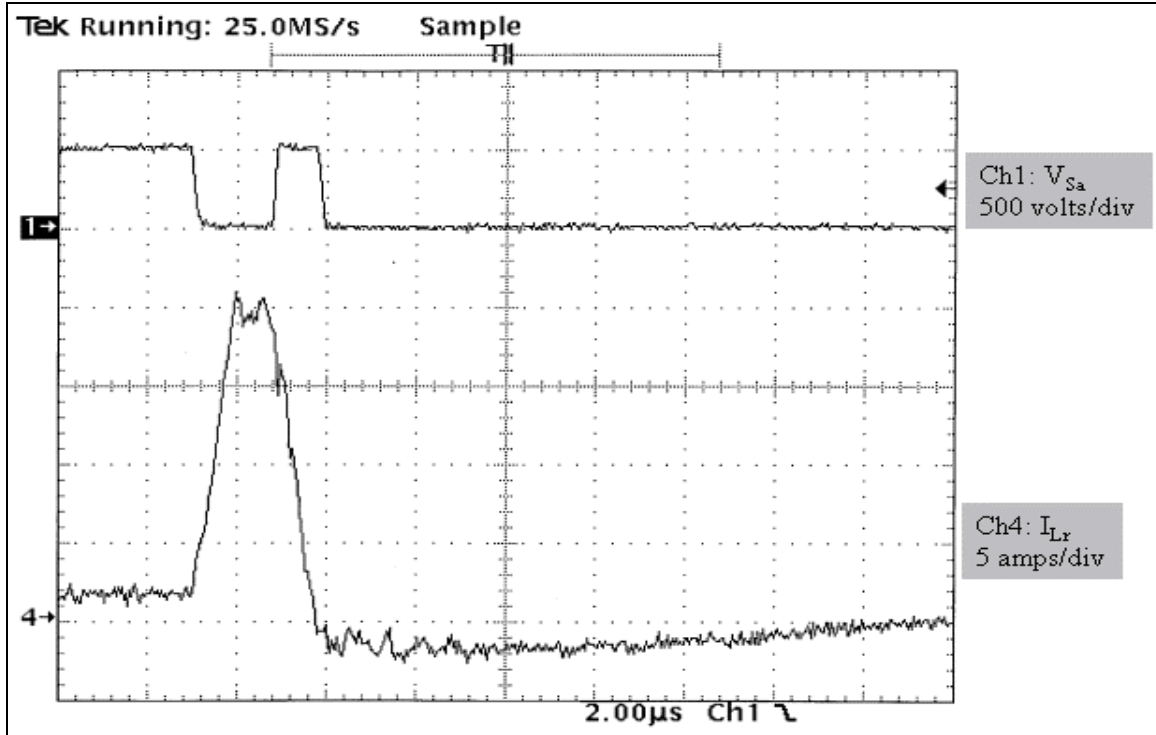


Figure 4-22. Voltage Across S_a and Current Through L_r (2μs/div).

After the negative slope of I_{Lr} in Figure (4-22), the current overshoots zero and reaches a minimum of approximately 1.5 amps over the recovery period of 11μs. Using the triangle area approximation of Equation (4-11), the total charge between D_1 and D_2 is:

$$Q_{rr} = \frac{1}{2} I_{rm} \tau_{rr} = 8.5 \mu C \quad (4-13)$$

Using a slope of $-20A/\mu s$, the DSEI60 data sheet in Appendix A predicts that each diode will have a recovered charge of only 1μC for a total of 2μC. The resonant inductor is in series with this current path and is forcing the diodes to recover slower.

Figures (4-19) and (4-22) also show that approximately 1 amp flows through L_r during mode 6 before S_a is gated "on." The forward current (I_f) plot versus forward voltage (V_f) drop curves in Appendix A for the DSEI60 show that D_m has a forward drop of 2.3 volts while conducting 20 amps. Since this voltage is impressed across D_1 and D_2 in the forward bias direction, the two diodes are biased "on." With 1.15 volts across D_1 and D_2 , the I_f versus V_f curves for the DSEI60 show that approximately 1 amp of current

will flow. The PSPICE simulations of Chapter III predicted that this current would be displaced away from D_m during mode 1.

Figure (4-23) shows the voltage across and current through the resonant inductor. A comparison of Figures (4-23) and Figure (4-10) validates that PSPICE accurately predicted the voltage and current waveforms for L_r . The current waveform has both a linear rise and drop, which indicates that the core is not being saturated.

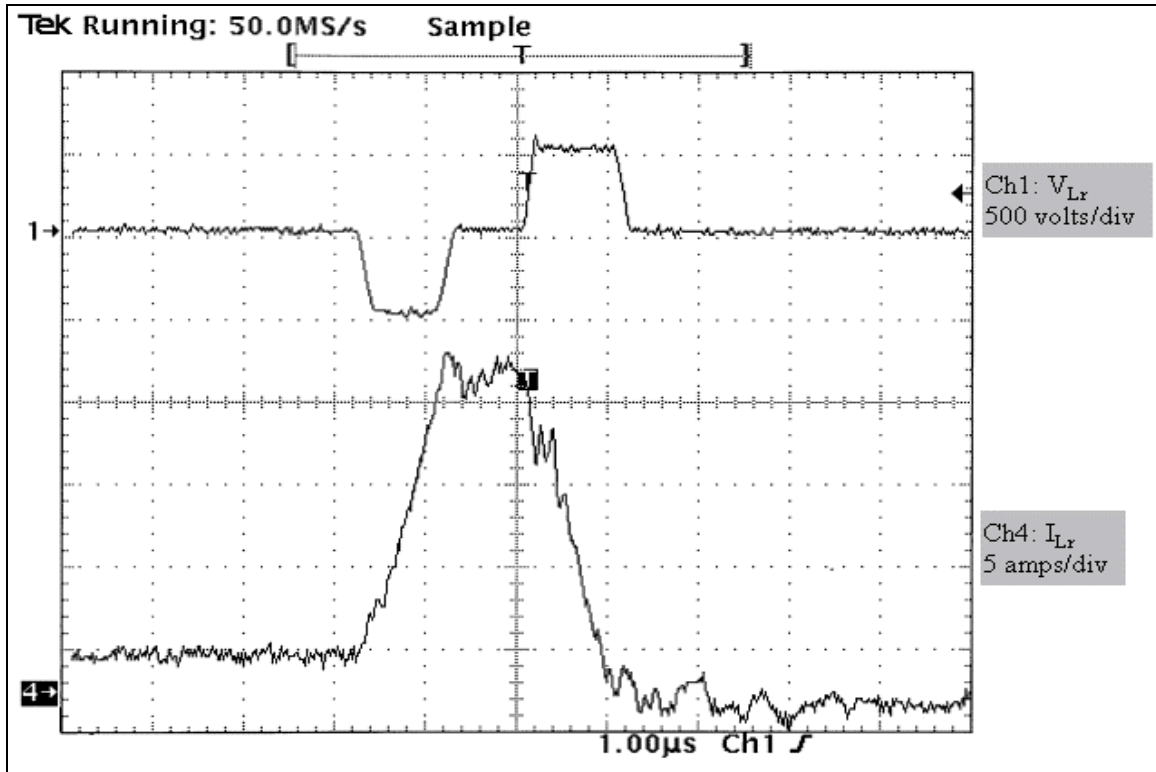


Figure 4-23. Voltage Across L_r and Current Through L_r ($1\mu\text{s}/\text{div}$).

Finally, the voltage across S_m and current through S_m during turn-off is shown in Figure (4-24). A significant amount of current flows for over $1\mu\text{s}$, while the voltage across S_m is V_{dc} . Unfortunately, the Tektronix TDS 540 oscilloscope in the NPS Power Lab does not have the ability to output the measured data. To estimate losses during turn-off, the current and voltage waveforms will be treated as simple geometric shapes and the products will be integrated over the duration of the current tail.

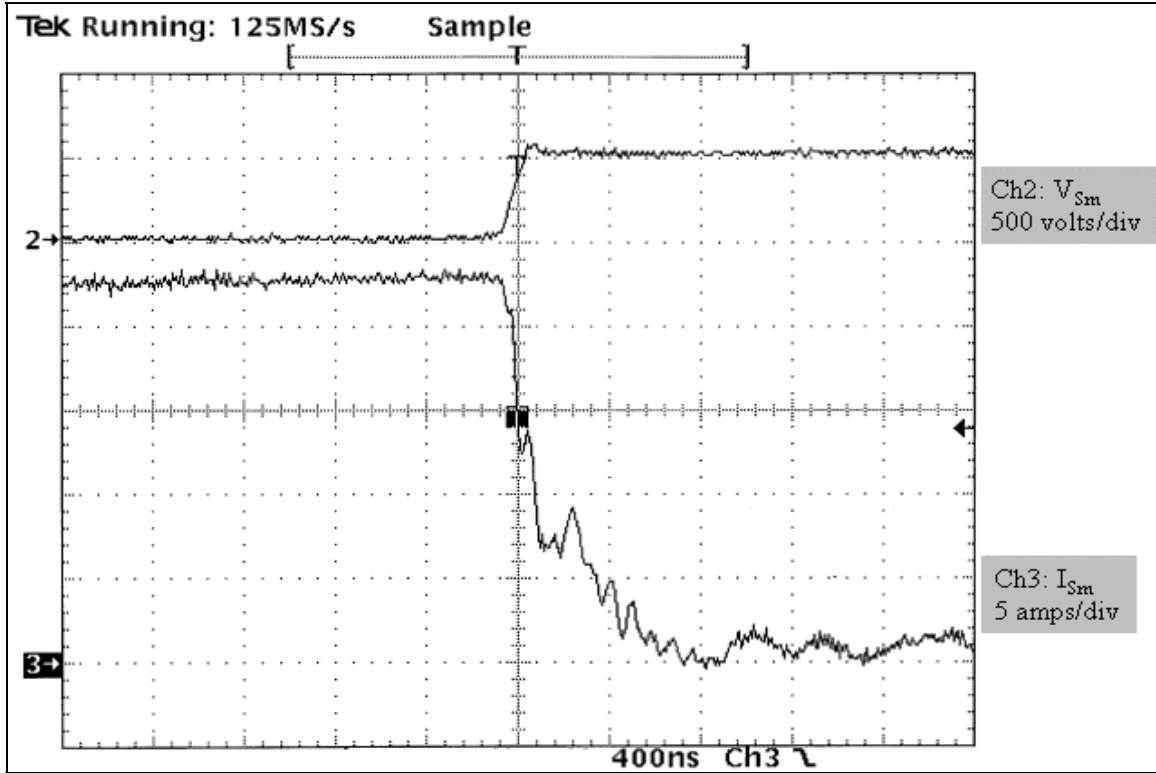


Figure 4-24. Voltage Across S_m and Current Through S_m During Turn-Off (400ns/div).

By treating the current tail as a right-sided triangle with a height of 10 amps and base of $1\mu\text{s}$, an approximation is calculated in Equations (4-14) and (4-15). It is assumed that the full 500 volts is applied during the $1\mu\text{s}$ period.

$$i_{S_m} = -10^6 t + 10 \quad (4-14)$$

$$E_{\text{loss}} = \int_0^t i_{S_m} V_{\text{dc}} dt = \int_0^{1\mu\text{s}} 500 (-10 \times 10^6 t + 10) dt = 2.5 \text{ mJ} \quad (4-15)$$

Since this energy loss occurs each cycle, the power loss during turn-off is given by Equation (4-16), where f_s is the switching frequency (20 kHz).

$$P_{\text{loss}} = E_{\text{loss}} f_s = 50 \text{ W} \quad (4-16)$$

Energy loss calculations are discussed in detail in Chapter V. Further, the results obtained here are compared to PSPICE simulations and the optimized converter.

4. Minimum-Load Analysis

The test diagram in Figure (4-12) was switched so that the load resistance equaled 200Ω . During minimum-load testing, the efficiency was only measured for $D=0.8$ for reasons described next. The recorded voltages and currents and calculated power values are listed in Table (4-3). Note that the efficiency closely matches the value estimated in Chapter III. This is somewhat expected as less current is flowing in the circuitry and therefore less I^2R loss needs to be accounted for. The soft-switching converter also has a 1.2 percent efficiency improvement over the hard-switched converter.

Soft-Switching Data								
Duty Cycle (%)	V_{in}	I_{in}	V_{load}	I_{load}	P_{in}	P_{out}	Efficiency η Soft-Switched	Efficiency η Hard-Switched
	Volts	Amps	Volts	Amps	Watts	Watts	Percent	Percent
80.00	501.4	1.67	399.3	2.04	832.3	814.6	97.5	96.3

Table 4-3. Minimum-Load Efficiency for a Duty Cycle of 80%.

From the analysis in Chapter III, as the duty cycle decreases, the converter operates closer to discontinuous current conduction mode. With the load resistance equal to 200Ω and $D=0.8$, the converter is operating right on the boundary between continuous and discontinuous, so the duty cycle was not reduced during efficiency testing. As introduced in Chapter III, in continuous mode, the main inductor is never exhausted of energy and hence will have a $I_{L,min}$ greater than or equal to zero. Figure (4-25) shows that the inductor current just reaches zero as the main switch is gated "on." Figure (4-26) shows that D_m is starved of current for approximately $1\mu s$ during the end of mode 1. Between Figures (4-25) and (4-26) it is hard to determine whether the converter is going into discontinuous operation. Figures (4-27) and (4-29) show that, like the full-load condition, D_1 and D_2 are forward biased during mode 1 and they carry a large percentage of the total load current. The current I_{Lr} never reaches zero in Figures (4-27) and (4-28),

so between the current paths through D_m , D_1 and D_2 , the main inductor always has current flow.

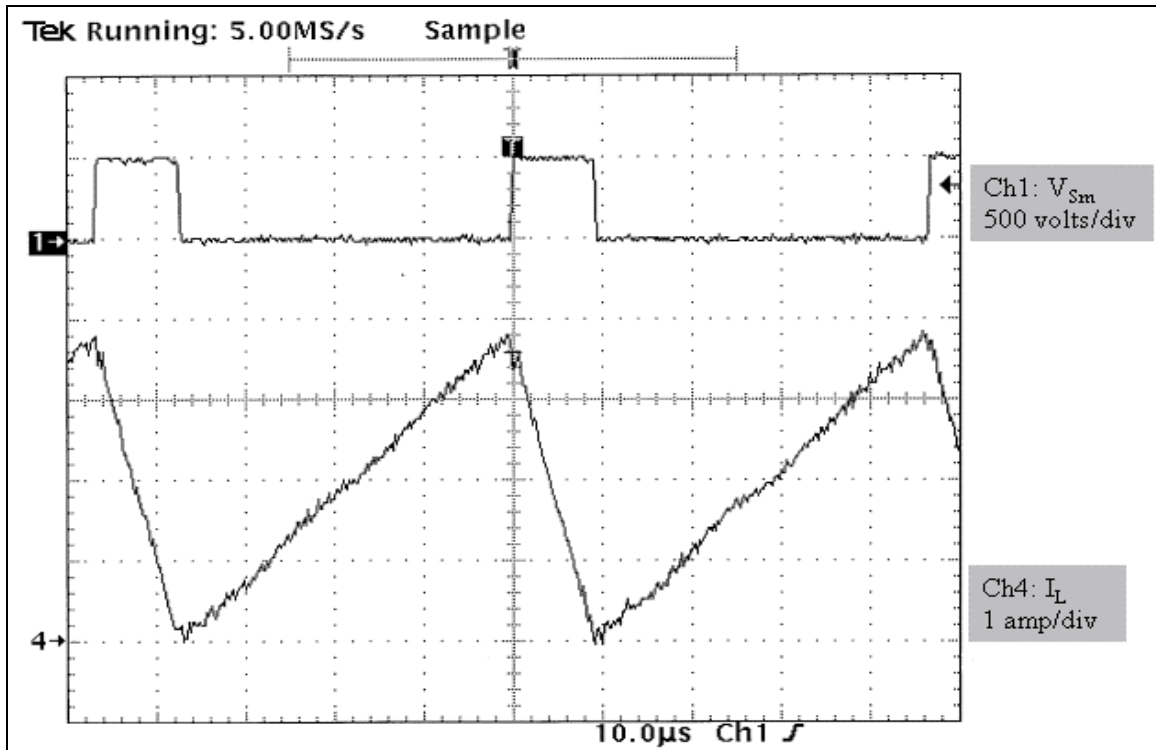


Figure 4-25. Voltage Across S_m and Current Through L (10 μ s/div).

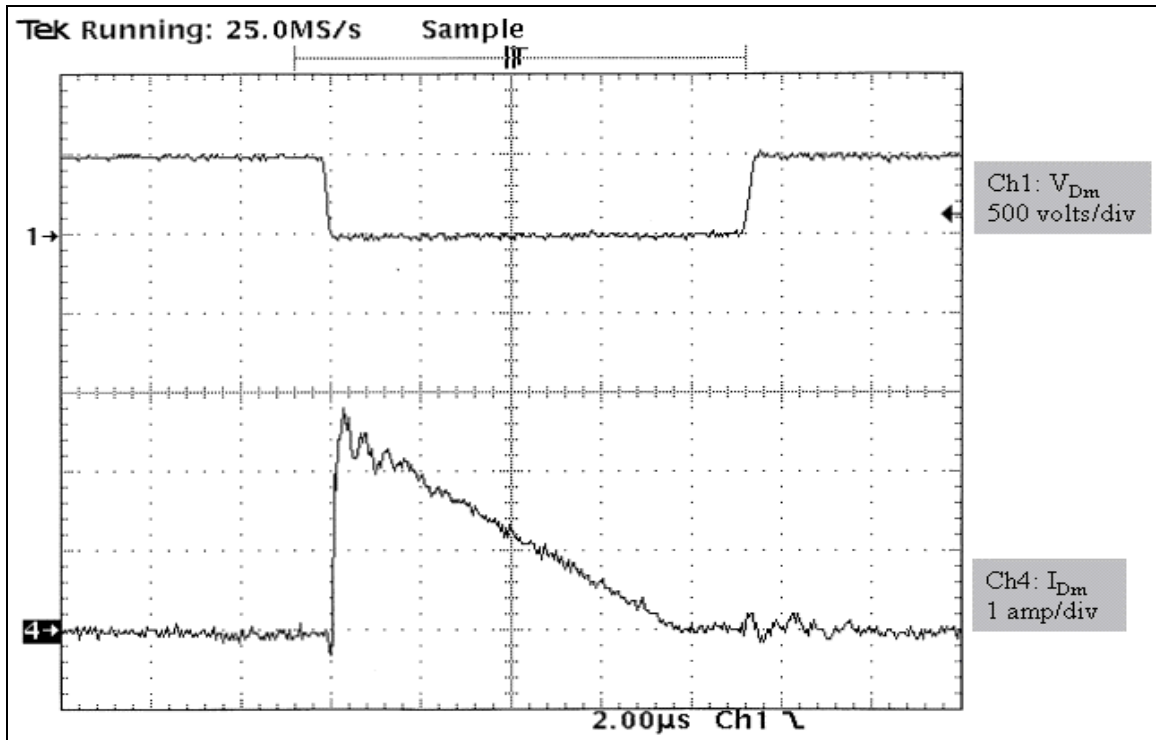


Figure 4-26. Voltage Across D_m and Current Through D_m ($2\mu s/\text{div}$).

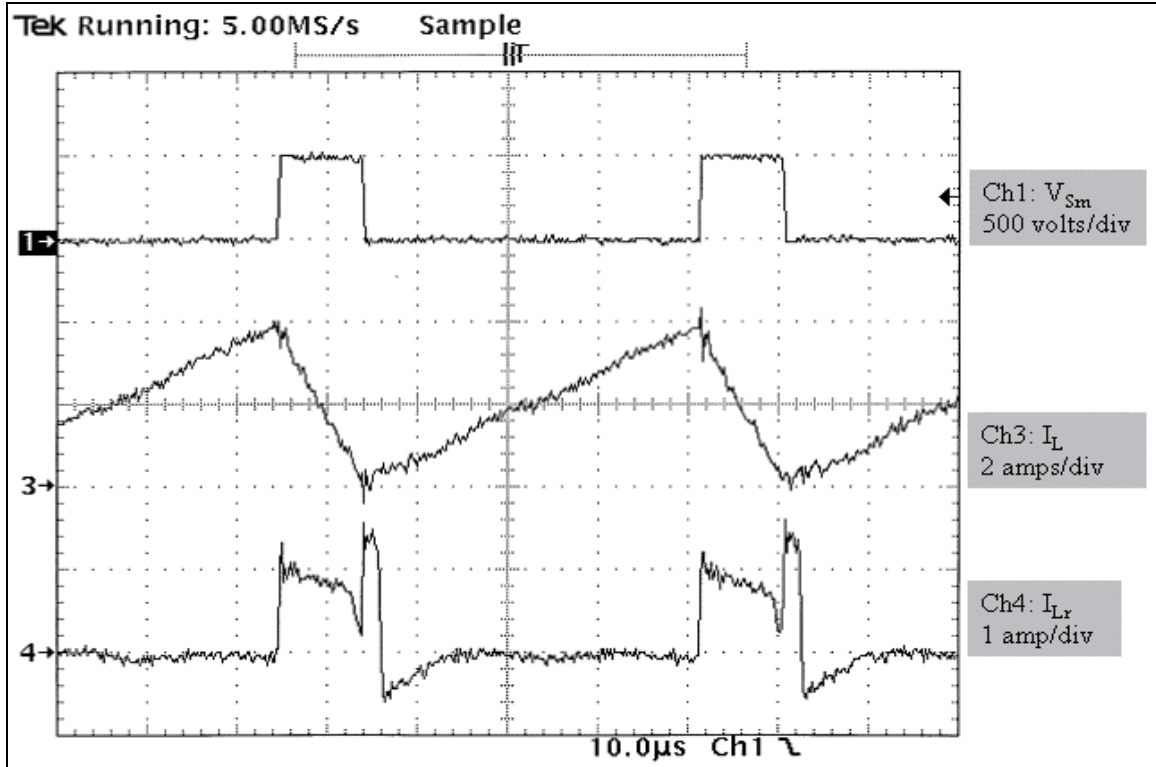


Figure 4-27. Voltage Across S_m and Current Through L and L_r ($10\mu s/\text{div}$).

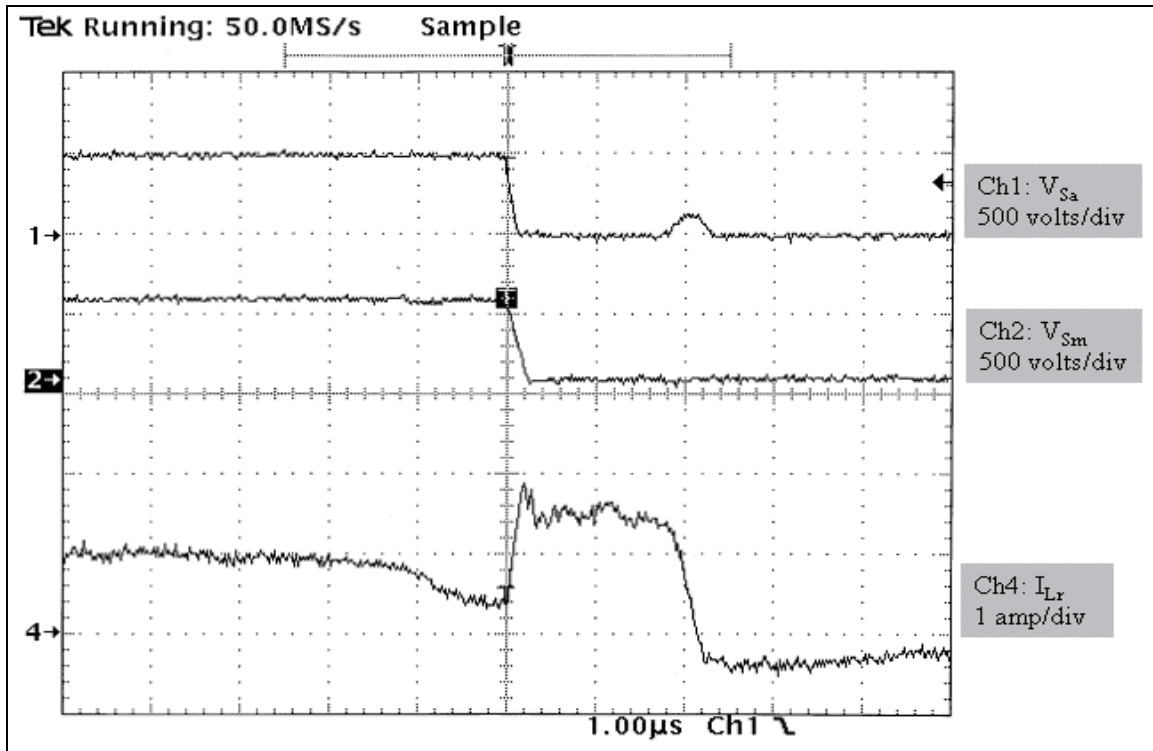


Figure 4-28. Voltage Across S_a and S_m and Current Through L_r (1µs/div).

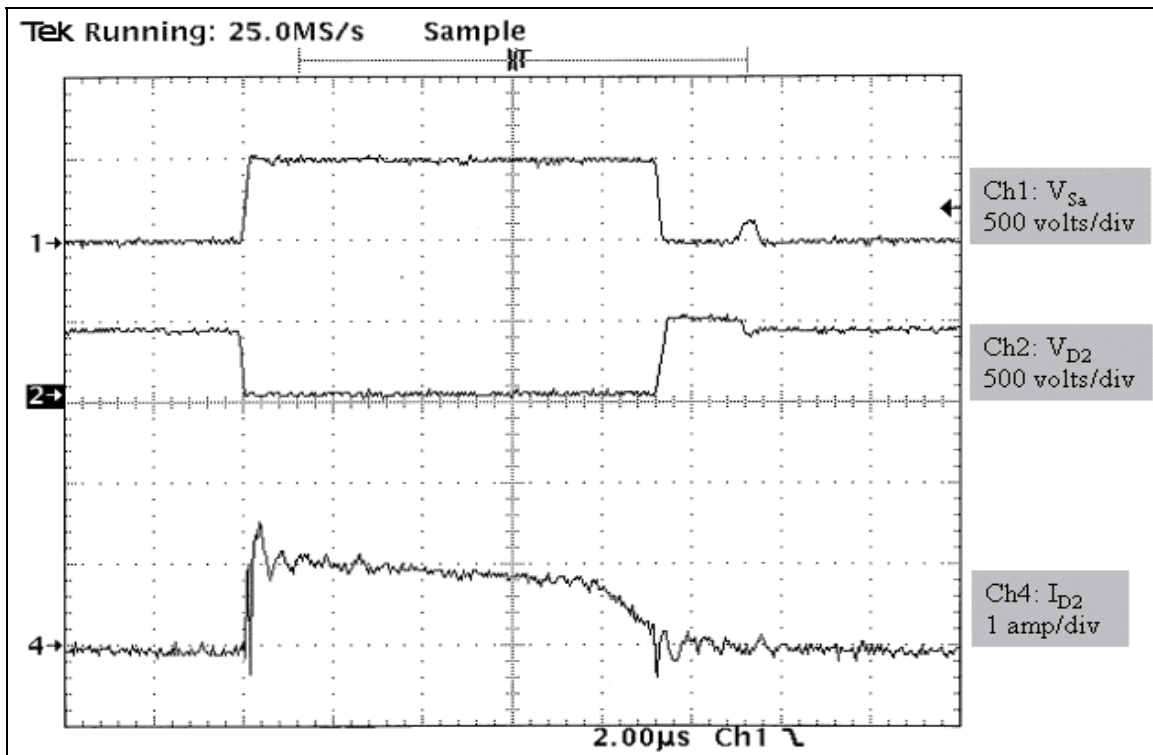


Figure 4-29. Voltage Across S_a and D_2 and Current Through D_2 (2µs/div).

In the minimum-loading case, S_a is gated "on" with the main inductor current at zero. Energy is stored in the resonant inductor as the main diode is starved of current and, like the full-load case, a negative current flows back to the supply through S_m . The resulting negative current pulse through S_m in Figure (4-30) looks like the inverted current pulse of L_r in Figure (4-28).

In Figure (4-30), current flow through S_m occurs with V_{S_m} greater than $V_{ce(sat)}$. The switch is no longer gating "on" in a ZVS condition, but the power level is so small that the extra loss is of no concern. The turn-off losses are also significantly reduced as illustrated in Figure (4-31). With a smaller load current flowing, the current tail is reduced in size and decays quicker. The turn-off losses will not be calculated for the minimum-load case.

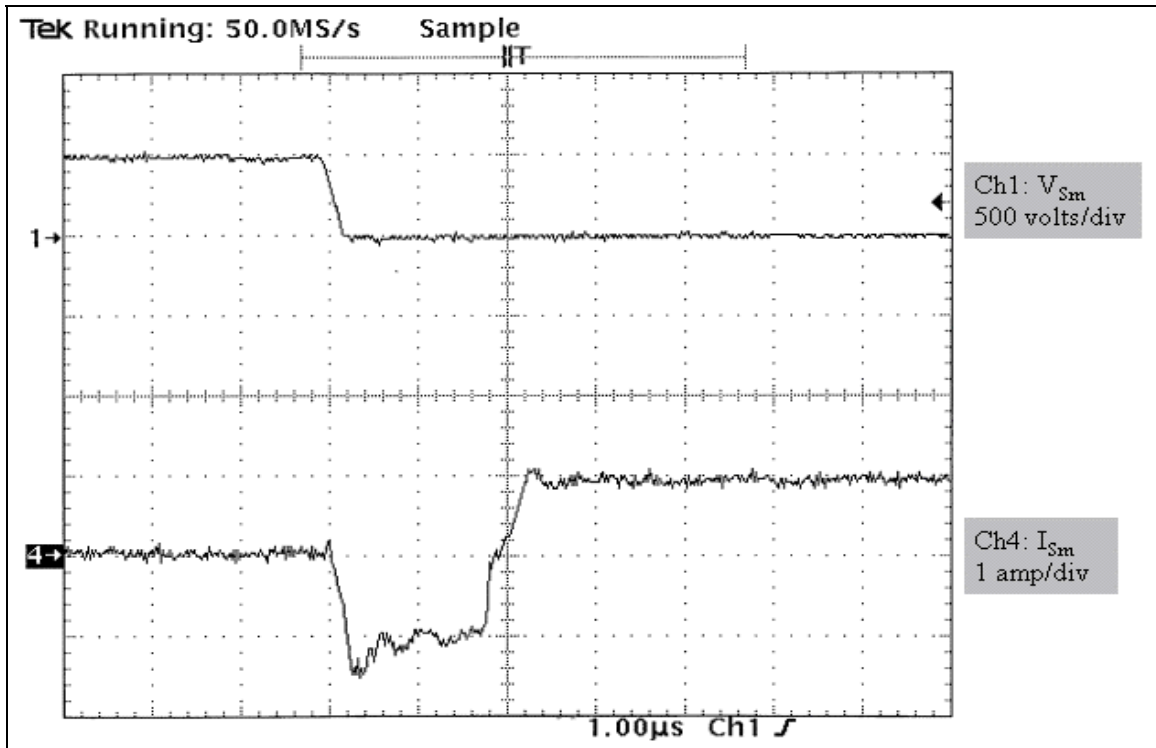


Figure 4-30. Voltage Across S_m and Current Through S_m During Turn-On ($1\mu s/\text{div}$).

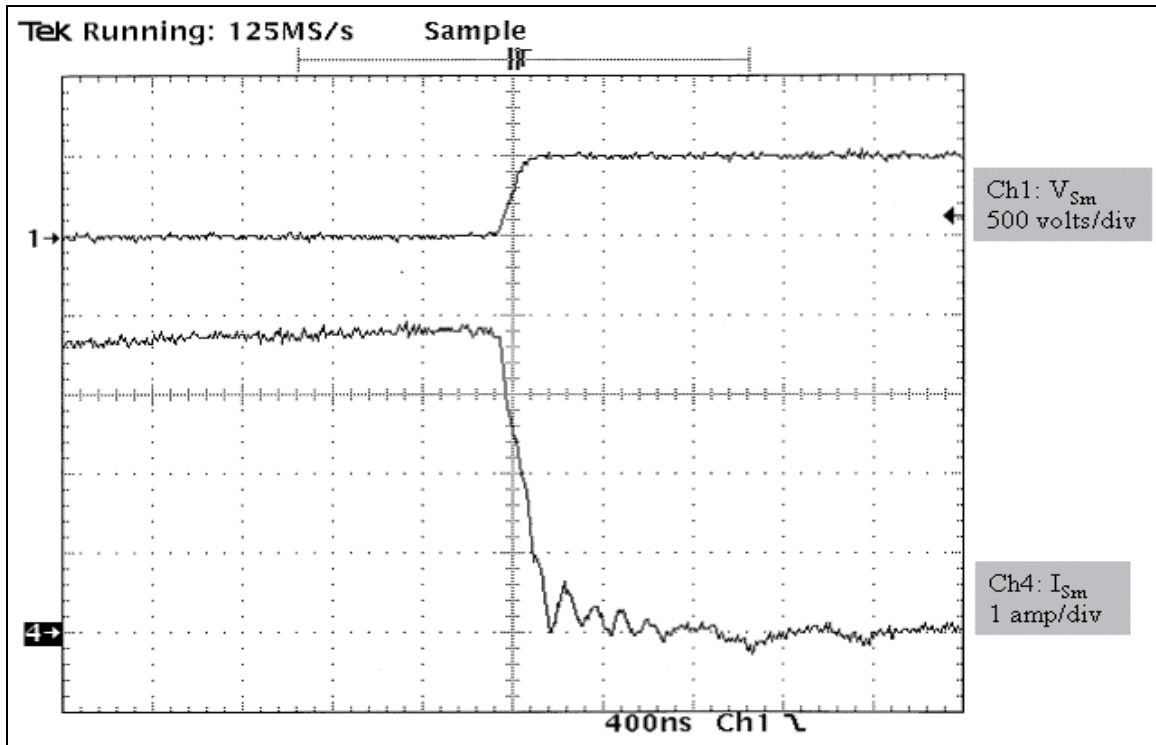


Figure 4-31. Voltage Across S_m and Current Through S_m During Turn-Off (400ns/div).

C. CHAPTER SUMMARY

Chapter IV provided a description of the construction of the resonant converter and, in more detail, the design and construction of the power module. Full-load converter testing was then reported and the resultant studies compared to the PSPICE runs of Chapter III. The converter was also tested in a minimum-loaded condition, which showed that the converter barely operates in the continuous current mode at the reduced load.

One of the important points discovered in Chapter IV is that the PSPICE model accurately predicted the wave shapes and timing, but failed to predict the magnitudes of the diode reverse recovery. From the comparison between the measured and simulated waveforms, the PSPICE model for the diodes is probably the lone cause of the inaccuracies.

Lastly, the significance of the turn-off losses was documented in the full-load condition. In Chapter V, it will be shown that turn-off losses limit the IGBT's capabilities and optimization will be used to reduce the losses.

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V. RESONANT CONVERTER OPTIMIZATION

A. CONVERTER POWER LOSS ANALYSIS

In the previous chapters, both PSPICE simulations and actual testing show that the main switch undergoes significant power loss. Figure (3-2) had introduced that IGBT power losses are comprised of turn-on, conduction and turn-off components. In both the simulations and actual testing, it was verified that near perfect ZVS turn-on of the main switch occurs. The main switch will also have a conduction loss based on the duty cycle and current density. During turn-off, the main switch has a significant amount of loss that increases linearly with the switching frequency. Conversely, the auxiliary switch is gated "on" in a ZCS condition for a short period of time ($\sim 2\mu\text{s}$), and thus the conduction losses are negligible. The auxiliary switch also undergoes significant turn-off losses and it can be assumed that all of the auxiliary switch losses occur during turn-off. In Chapter V, the turn-off loss mechanism is analyzed using PSPICE and MATLAB. A new converter model will be simulated to verify the calculations and, finally, the actual converter will be modified and tested with a new set of optimized resonant components.

1. Mode Loss Analysis

Since the conduction losses can only be controlled by duty cycle and current density, the reduction of the turn-off losses is the main objective. The turn-off losses are a function of the current waveform and the applied voltage waveform as the device is gated "off." It has already been demonstrated that IGBTs have a current tail, which lasts up to a few microseconds after turn-off. In the previous results, the voltage across the main switch was allowed to buildup quickly, thus resulting in a substantial instantaneous power loss. If the current waveform shape and rate of change of the applied voltage is controlled, the turn-off losses can be significantly reduced.

To control the dv/dt across the main switch during turn-off, the analysis of modes 7 and 8 must be revisited. When S_m is gated "off," the converter enters mode 7 if V_{Cr2} is less than V_{dc} and mode 8 otherwise (see Figure (2-9)). Equation (5-1) characterizes the dynamics of the voltage buildup across S_m during mode 7.

$$\frac{dV_{Cr1}}{dt} = \frac{i_L}{C_{r1}} \quad (5-1)$$

The dynamics of mode 8 are governed by Equation (5-2).

$$\frac{dV_{Cr1}}{dt} = \frac{i_L}{C_{r1} + C_{r2}} \quad (5-2)$$

Upon comparison, it is obvious that the rate of change of V_{Cr1} will be greater in mode 7 than mode 8. The capacitor C_{r2} will typically be an order of magnitude greater than C_{r1} ; hence, mode 8 will have a significantly reduced $\frac{dV_{Cr1}}{dt}$. With this knowledge, resonant circuit components must be picked to minimize the occurrence of mode 7. If proper L_r and C_{r2} values are selected, C_{r2} will charge to V_{dc} and mode 7 will not occur.

With a typical current tail lasting $1\mu s$, a reasonable voltage rate across S_m is $500 V/\mu s$. A voltage buildup from $V_{ce(sat)}$ to V_{dc} during the time it takes the current tail to decay would provide such a dv/dt . Assuming $C_{r2} \gg C_{r1}$, Equation (5-3) represents a good approximation of the governing dynamics. With $I_{L,max}$ equal to 24 amps, an approximate value of C_{r2} is given by the calculation in Equation (5-3).

$$C_{r2} \approx I_{L,max} \frac{dt}{dV} = 48nF \quad (5-3)$$

With a value of C_{r2} specified, the proper inductance value for L_r must now be selected so that V_{Cr2} reaches V_{dc} . If the energy capacity of C_{r2} and L_r are matched for a given voltage and current, the energy from L_r is transferred to C_{r2} during mode 5. This energy balance will only hold true for a specific load condition.

All optimization will be performed for the full-load case with $D=0.8$, since this operating point is where an efficiency improvement is most needed. The minimum-load results in Chapter IV demonstrate that the power loss is a magnitude lower than the full-load case. As the loading decreases towards the minimum-load case with a constant duty cycle, less energy is stored in L_r , and V_{Cr2} will not reach V_{dc} . Mode 5x will not occur, as all of resonant inductor's energy will be transferred to C_{r2} . The mitigation of mode 5x is an added benefit as extra conduction losses occur as D_2 is forward biased during this

time. Conversely, mode 7 will be more prominent as the loading decreases and V_{Cr2} will always be less than V_{dc} . With reduced loading and thus reduced current flow, the switch losses are also lessened. Minimizing losses at the maximum-loading condition will guarantee that the IGBT switches will not be thermally stressed as the load decreases.

Setting the energy Equations (5-4) and (5-5) equal to each other, the following value of inductance is determined in Equation (5-6).

$$E_{\text{capacitor}} = \frac{1}{2}CV^2 \quad (5-4)$$

$$E_{\text{inductor}} = \frac{1}{2}LI^2 \quad (5-5)$$

$$L_r = \frac{C_{r2}V_{dc}^2}{i_{r,\max}^2} = \frac{(48\text{nF})(500\text{V})^2}{(19\text{A})^2} = 33\mu\text{H} \quad (5-6)$$

The value for $i_{r,\max}$ in Equation (5-6) is based on actual testing. In Chapter III, the current was calculated to be 17 amps with $I_{L,\min}$ equal to 16 amps, which is the current peak that PSPICE also estimated. Upon inspection of Equation (3-15), the most likely cause of the additional 2 amps of current in the resonant inductor is a higher value of C_{r1} than estimated. The IGBT capacitance is highly nonlinear and varies with the voltage applied across the device. Some additional stray capacitance might be caused by the large heat sink assembly, which is connected directly to the collectors of the main and auxiliary switches. The plot of the IGBT's capacitance as a function of V_{CE} is listed in the IRG4PH50UD data sheet in Appendix A. The IGBT's body capacitance can range from a maximum of 3700pF with a V_{ce} of 1 volt to a minimum of 100pF with a V_{ce} of 500 volts.

2. Optimization Analysis Using PSPICE

Next, the parametric sweep function in PSPICE was used to study the effect of changing the resonant capacitor and inductor. For inductor values of 10uH, 28uH and 46uH, the resonant capacitor, C_{r2} , was swept from 1nF to 100nF. For $L_r = 28\mu\text{H}$, various plots were made to support the discussion from Section A-1 of this chapter. Later, the

voltage and current data from PSPICE will be used to plot switch energy loss curves as a function of capacitance.

Figure (5-1) shows I_{Sm} and V_{Sm} during turn-off for C_{r2} equal to 1nF, 10nF, 20nF, 30nF, 40nF and 50nF. Notice that any increase in capacitance above 1nF significantly reduces the magnitude of the current tail. At the same time, the slope of the voltage buildup across the IGBT is also reduced. A point is reached ($C_{r2} \approx 30$ nF) where the energy capacity of the capacitor exceeds the inductor and mode 7 operation starts to occur.

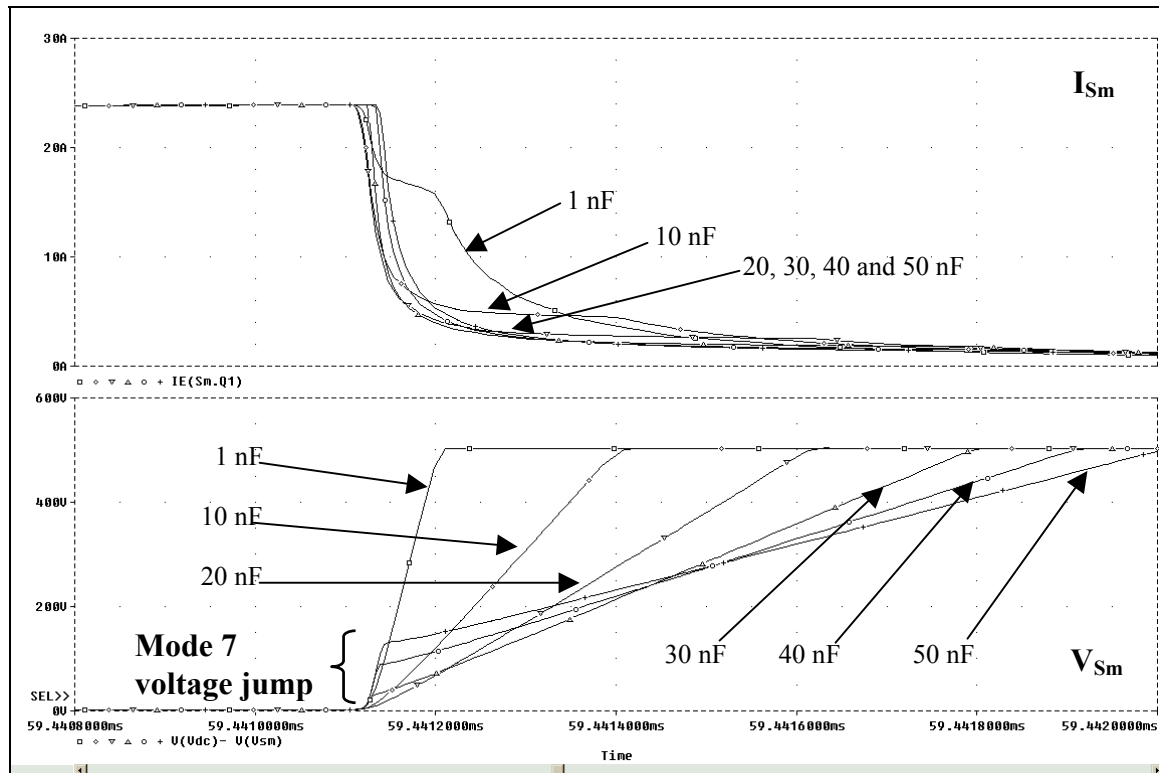


Figure 5-1. I_{Sm} and V_{Sm} During Turn-Off for $C_{r2}=1, 10, 20, 30, 40$ and 50 nF.

With mode 7 occurring for C_{r2} equal to 30, 40 and 50nF, additional loss will occur, but it is difficult to estimate overall switch losses since each successive voltage plot also has a reduced slope.

For C_{r2} equal to 1, 10 and 20nF, the resonant inductor has excess energy and mode 5x occurs. Extra energy loss occurs in this mode, but the occurrence of mode 5x guarantees that V_{Cr2} has reached V_{dc} , thus preventing mode 7. The relationship between mode 5x and mode 7 are shown in Figure (5-2). As predicted, for the first three capacitor values, mode 5x occurs and D_2 is forward biased. For the remaining three capacitor values, V_{Cr2} never reaches V_{dc} and D_2 remains reversed biased.

The auxiliary switch current and voltage is shown in Figure (5-3). The faster that L_r is able to transfer its energy into C_{r2} , the quicker the current tail decays. As an added benefit, the voltage across S_a builds up slowly provided D_2 is not forward biased in mode 5x. With an increased value of C_{r2} , S_a is able to turn "off" in a ZVS condition and the total auxiliary switch losses are significantly reduced.

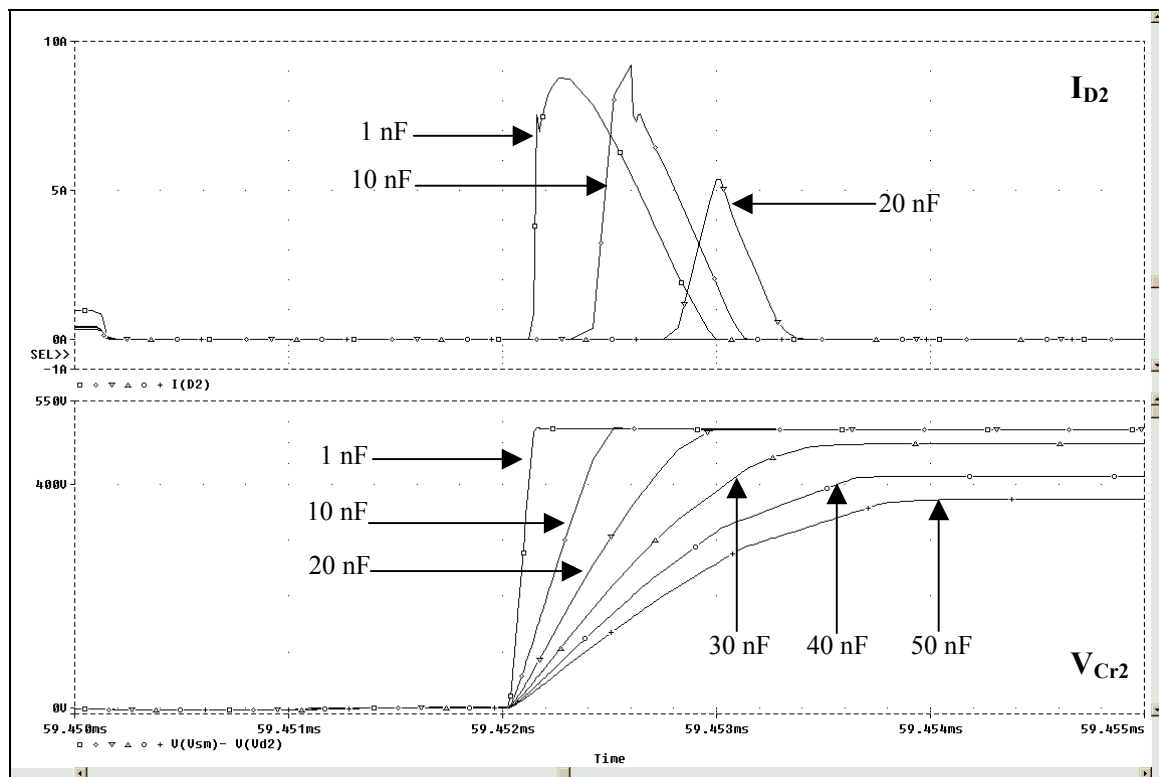


Figure 5-2. I_{D2} and V_{Cr2} During Mode 5/5x for C_{r2} = 1, 10, 20, 30, 40 and 50nF.

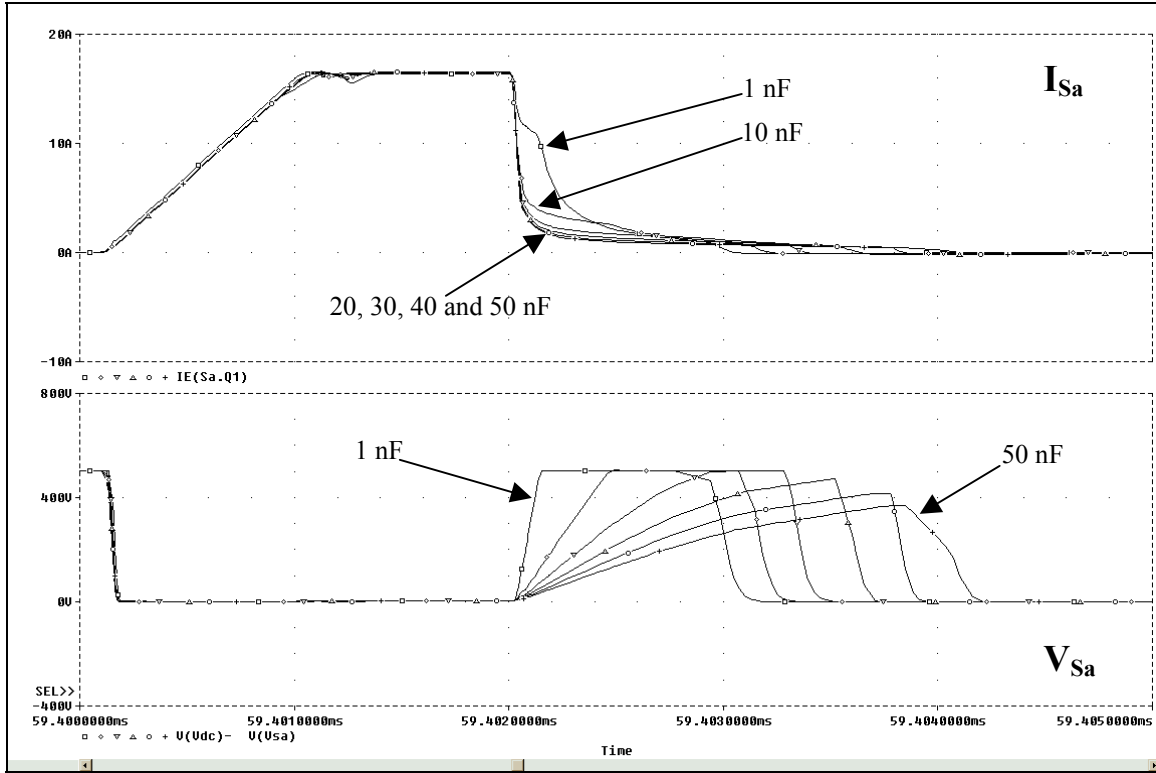


Figure 5-3. I_{Sa} and V_{Sa} During Turn-Off for $C_{r2}=1, 10, 20, 30, 40$ and 50 nF.

3. Energy Loss Analysis Using MATLAB

Now that the method of reducing the energy loss in S_m and S_a is known, energy and power loss curves are used to identify the optimized design. In the previous section, a parametric sweep of C_{r2} was performed and the voltages and currents as a function of time were copied and formatted in EXCEL. The formatted data was then read into a MATLAB program so that losses could be estimated. The MATLAB program calculates the instantaneous power for each time step and then performs a trapezoidal method of numerical integration to find the energy loss of the device. The energy loss is then plotted as a function of capacitance C_{r2} . Since the conduction loss is constant for a given duty cycle and the turn-on loss is virtually zero, the conduction loss can be subtracted from the total calculated loss to estimate the turn-off loss. The MATLAB code is listed in Appendix E.

Figure (5-4) demonstrates the energy loss during a $50\mu\text{s}$ cycle for S_a , S_m , D_m and the total energy loss. Figure (5-5) is similar to Figure (5-4), but the energy loss is converted to a power loss by multiplying by the switching frequency f_s (20kHz).

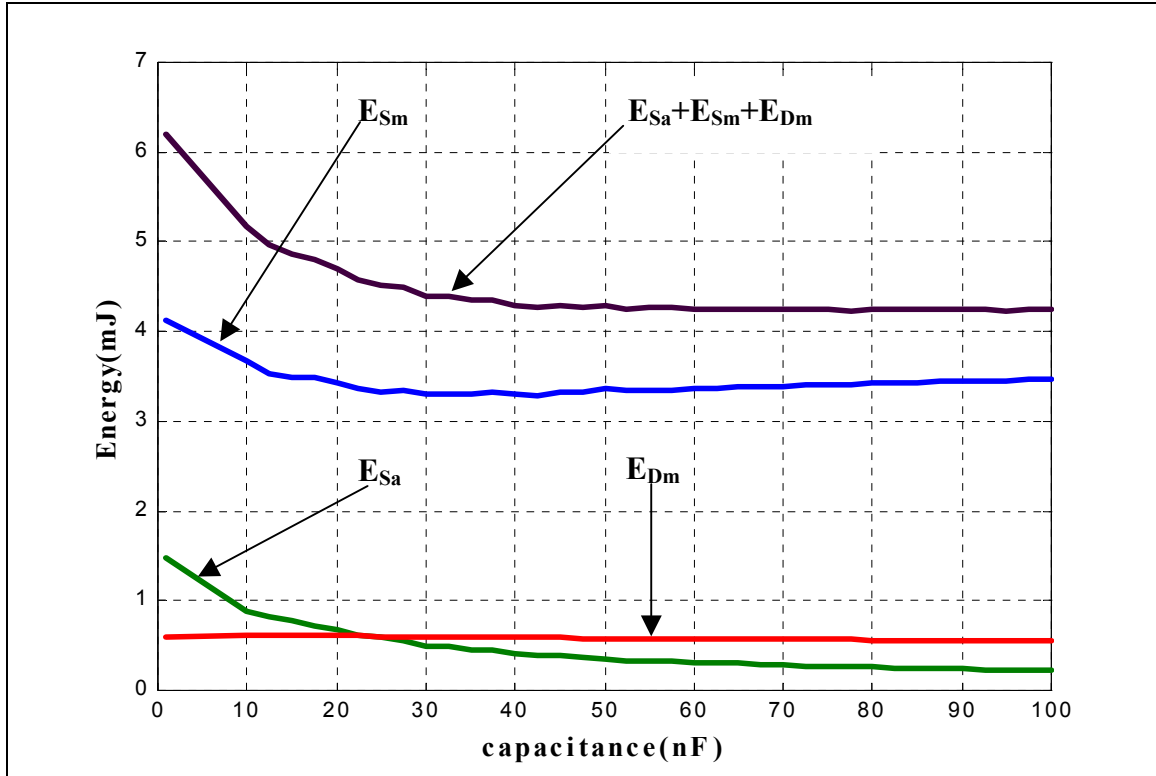


Figure 5-4. Energy Loss as a Function of Capacitance C_{r2} .

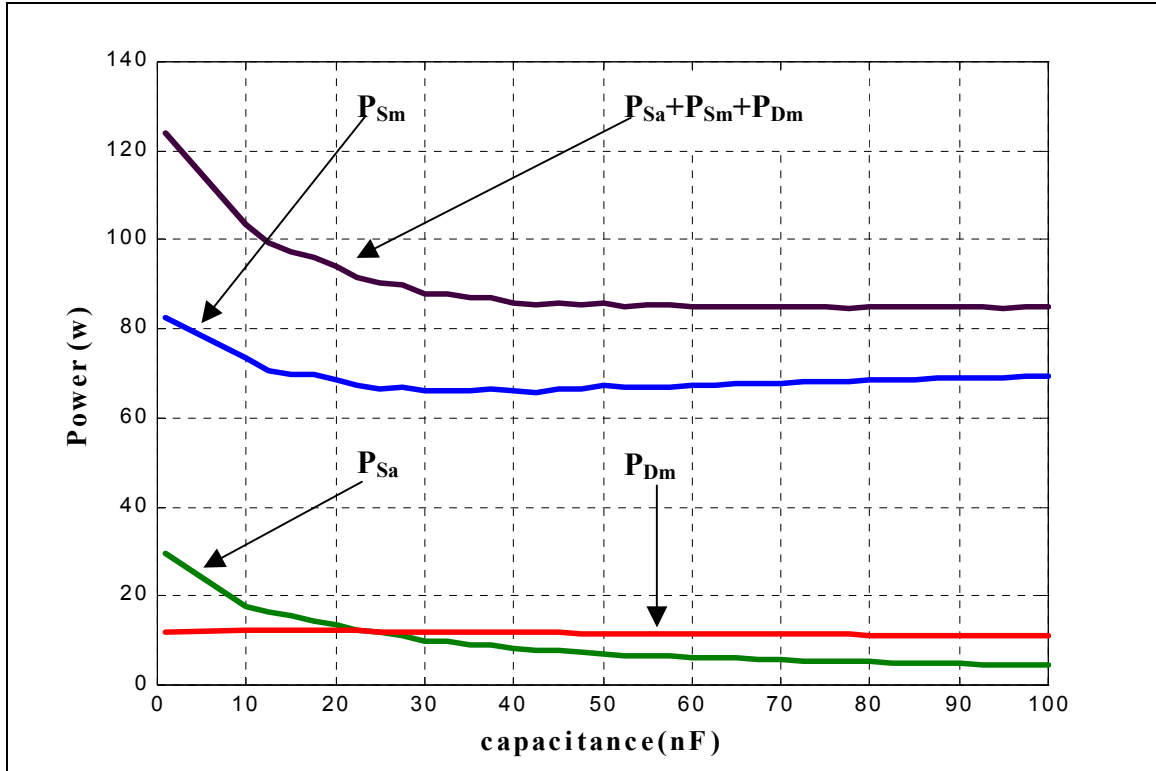


Figure 5-5. Power Loss as a Function of Capacitance C_{r2} .

Figures (5-4) and (5-5) clearly illustrate that S_m has a minimum loss between 30 and 40nF. The total loss for S_m , S_a and D_m drops significantly between 1 and 30nF and flattens near 50nF as the increase in P_{S_m} is cancelled by the decrease in P_{S_a} . The energy loss for D_m is constant through out the capacitance range and this is probably due to a combination of an over-simplified diode model and the fact that the diode is soft recovered through L_r . The expanded loss curves for S_m , S_a and D_m are shown in Figures (5-6) and (5-7). The turn-off loss curve for S_m has a well-defined minimum of approximately 32 watts between 30 and 40nF. The turn-off power loss for 1nF is 48.5 watts, which closely matches the turn-off power loss of 50 watts measured and reported in Chapter IV. For a duty cycle of 80 percent and a saturation voltage drop of 2.13 volts, the expected conduction power loss for S_m is:

$$P_{\text{conduction}} = V_d I_o t_{\text{on}} f_s = 34 \text{ watts} \quad (5-7)$$

Using this value for the conducted loss, the total expected power loss for S_m is 66 watts assuming that the turn-on loss is zero.

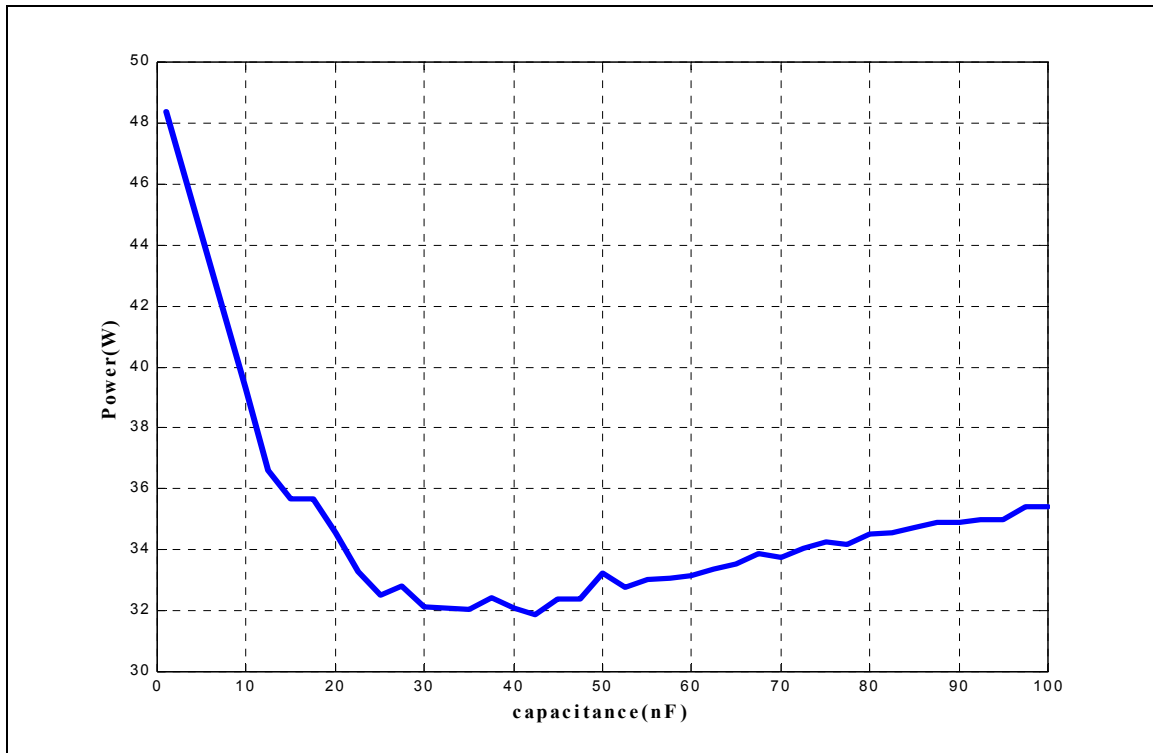


Figure 5-6. Turn-off Power Loss for S_m as a Function of Capacitance C_{r2} .

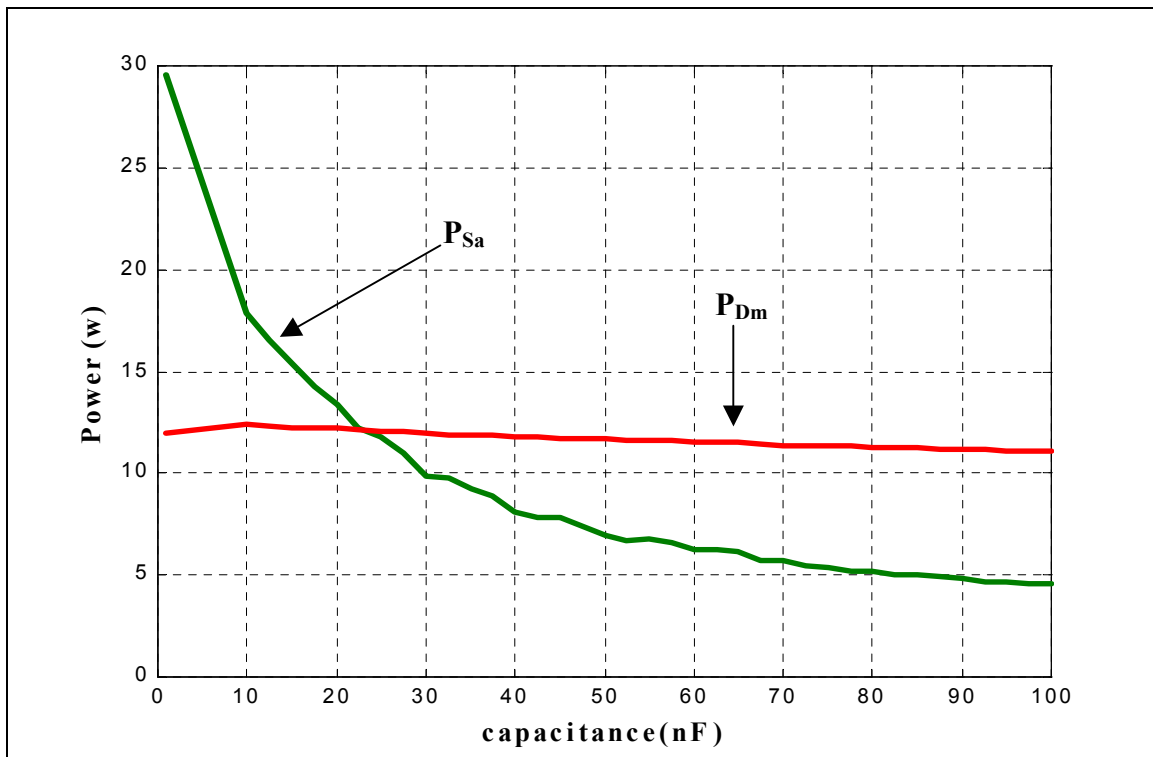


Figure 5-7. Power Loss For S_a and D_m as a Function of Capacitance C_{r2} .

In Figure (5-7), the power loss in S_a falls off significantly and converges on the conduction loss for the $2\mu\text{s}$ that the switch is "on."

The turn-off losses for S_m are documented in Figure (5-8) for L_r equal to $10\mu\text{H}$, $28\mu\text{H}$ and $46\mu\text{H}$ as a function of C_{r2} .

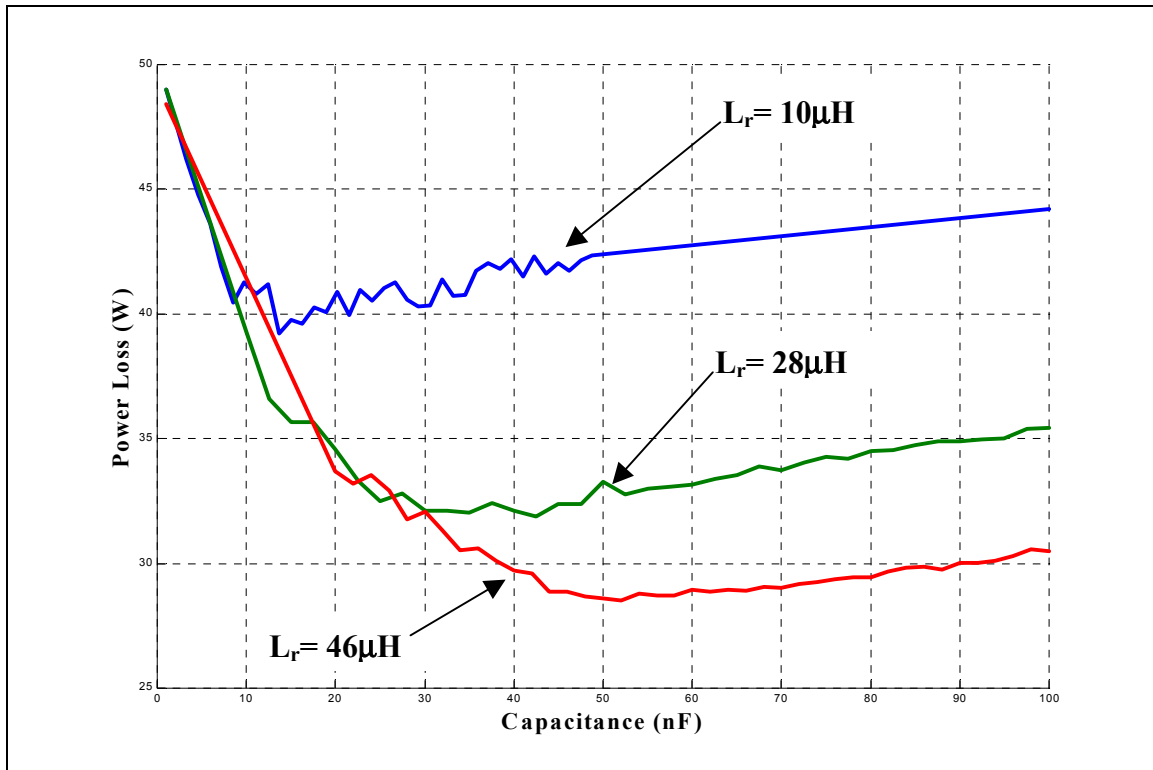


Figure 5-8. Turn-off Loss for S_m as a Function of L_r and C_{r2} .

As expected, as more energy is stored in L_r and transferred to C_{r2} , the turn-off losses in S_m decrease. Recall that this simulation is based on a peak inductor current of 17 amps. In actuality the peak current is closer to 19 amps, which yields a resonant inductance of $33\mu\text{H}$ for a capacitance of 48nF . The maximum usable inductance is approximately $46\mu\text{H}$, as the resonant frequency quickly approaches only one order of magnitude above the switching frequency. For the remainder of the testing, a $28\mu\text{H}$ inductor is used as it is close to the optimum value of inductance and it would be difficult to wind a $46\mu\text{H}$ inductor on the small 1.57-inch diameter toroidal core. For this amount of inductance, a

capacitance of 30nF will be used for the initial testing and then other values will be used to verify the results obtained in this section.

4. Estimation of Efficiency For $L_r=28\mu\text{H}$ and $C_{r2}=30\text{nF}$

Just as in Chapter III, the PSPICE simulation was used to estimate the resonant converter efficiency. Figure (5-9) illustrates a plot of the average output power over the average input power. The 20 kHz ripple in the efficiency plot is due to the capacitor voltage ripple across the load. The efficiency is estimated to be approximately 98.8 percent. The actual measured efficiency is expected to be lower, since PSPICE does not account for losses in the inductor cores and wiring I^2R losses.

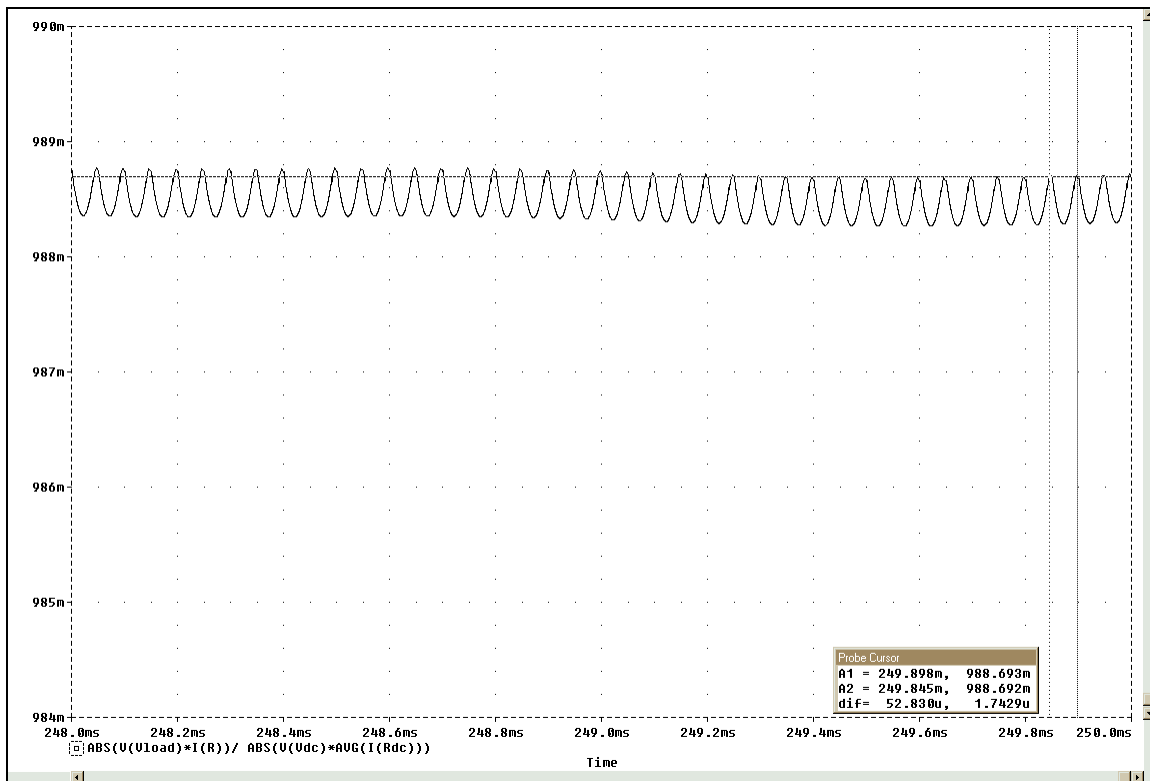


Figure 5-9. Estimated Efficiency of the Optimized Converter.

B. OPTIMIZED CONVERTER RESULTS

This section contains a description of the testing results for the maximum-load case. The maximum-load condition is where the components are stressed the greatest and a higher efficiency is particularly needed to reduce thermal stresses. The test setup was identical to Figure (4-12) in order for a meaningful comparison to be made. The equipment listed in Table (4-1) was also used.

1. Full-Load Efficiency Testing

As reported in Chapter IV, the converter efficiency was measured as a function of duty cycle. Table (5-1) lists the voltages, currents, calculated power loss and efficiency for the optimized resonant converter. The efficiencies for the pre-optimized resonant converter are included for reference.

Optimized Soft-Switching Converter Data								
Duty Cycle (%)	V _{in}	I _{in}	V _{load}	I _{load}	P _{in}	P _{out}	Efficiency η optimized	Efficiency η Pre-optimized
	Volts	Amps	Volts	Amps	Watts	Watts	Percent	Percent
10	500.8	0.38	57.5	2.87	190.3	165.0	86.7	84.3
20	500.6	1.12	102.9	5.13	560.7	527.9	94.2	93.1
30	500.8	2.51	155.7	7.76	1257.0	1208.2	96.1	95.4
40	500.6	4.39	207.1	10.32	2197.6	2137.3	97.3	96.5
50	500.2	6.74	257.1	12.80	3371.4	3290.9	97.6	97.1
60	500.0	9.34	303.1	15.09	4670.0	4573.8	97.9	97.5
70	500.7	12.88	356.7	17.75	6449.0	6331.4	98.2	97.7
80	500.9	16.42	403.4	20.05	8224.8	8088.2	98.3	97.9

Table 5-1. Full-Load Efficiency for Duty Cycles Ranging Between 10% and 80%.

The efficiency as a function of duty cycle is plotted in Figure (5-10) for the optimized, pre-optimized and hard-switched converter designs. The difference between the two soft-switched converter efficiencies is shown in Figure (5-11). Figures (5-10) and (5-11) confirm that the optimized design is more efficient over the range of duty cycles. At an 80 percent duty cycle, the efficiency difference between the resonant converters is 0.453 percent, which is approximately 37.6 watts with 8000 watts dissipated into the load. The efficiency difference between the optimized resonant converter and the hard-switched converter is 0.74 percent, which equates to a 62.5-watt reduction in switch losses. Figures (5-6) and (5-7) confirm that if the new estimated power losses for S_m and S_a at 30 nF are subtracted from the values at 1 nF, a difference of approximately 35.5 watts is found. This power difference is significant in that the power loss estimation closely matches the measured results described above. Figure (5-11) also shows that the difference between the efficiencies is relatively constant once the duty cycle is above 50 percent.

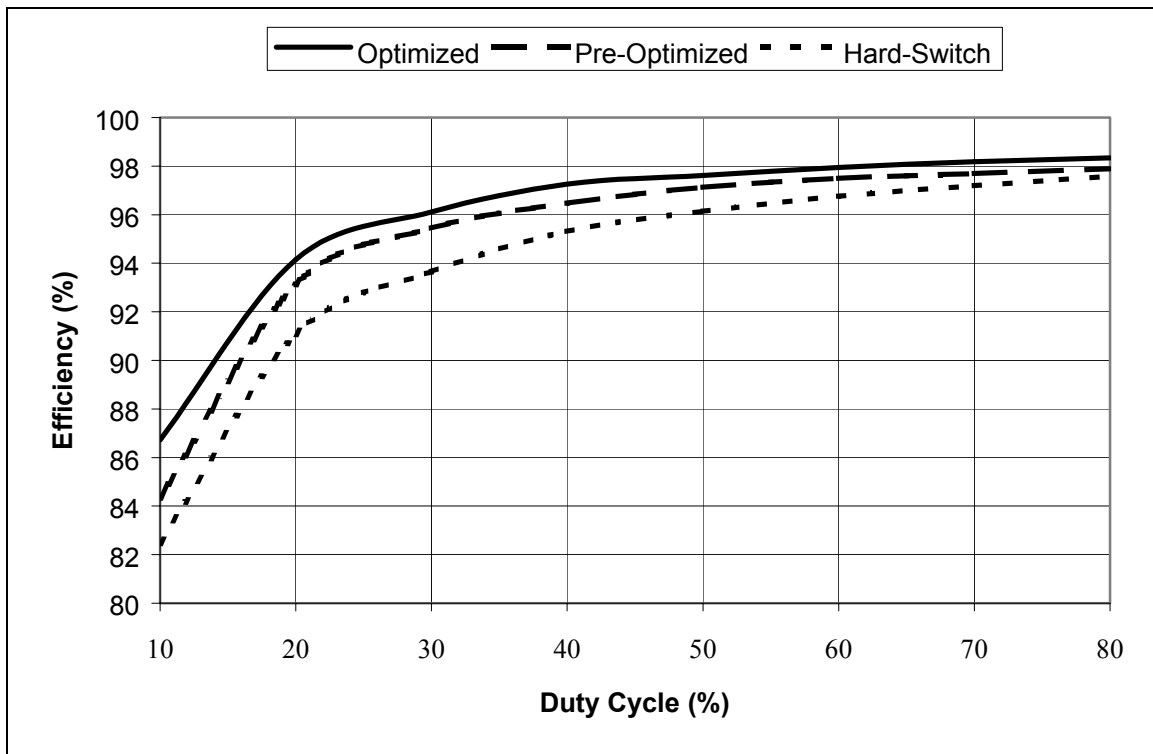


Figure 5-10. Comparison of Efficiency Between the Optimized, Pre-Optimized and Hard-Switched Converters.

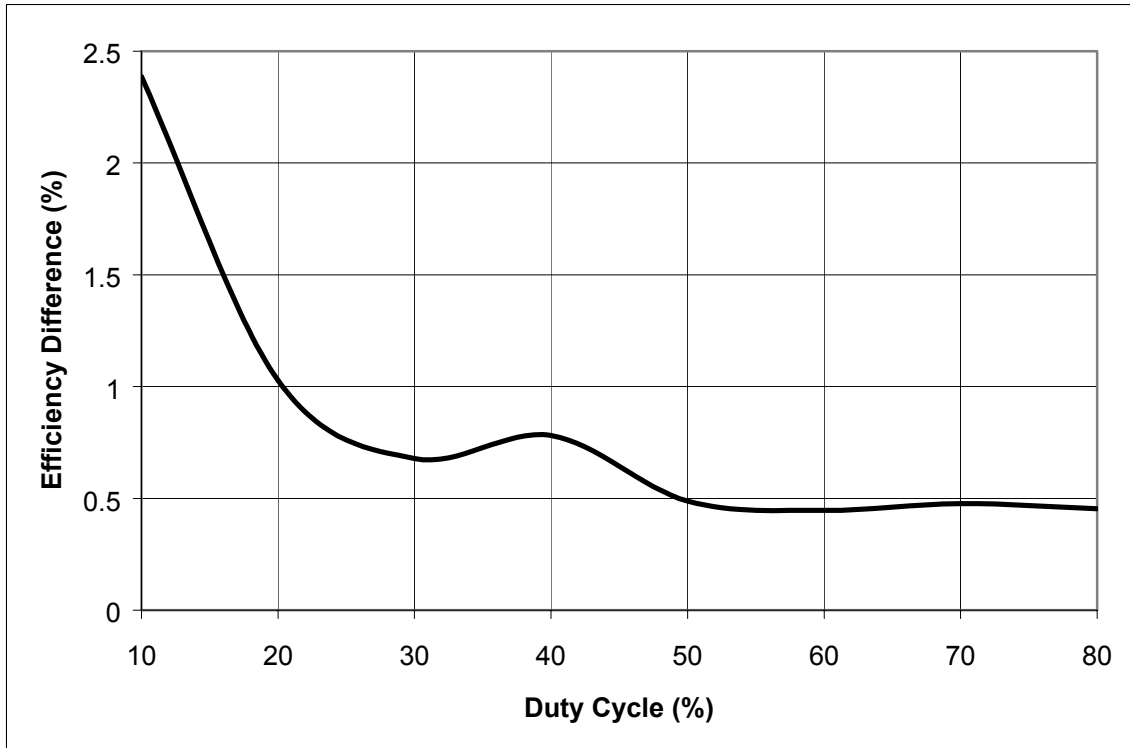


Figure 5-11. Differential Efficiency Between the Optimized and Pre-Optimized Resonant Converters.

The difference between the estimated and actual efficiency for the optimized and pre-optimized design are 0.47 and 0.51 percent at an 80 percent duty cycle, respectively. These differences equate to losses of 39 and 42 watts, which are not accounted for in the PSPICE simulation. Assuming that the power loss is 40 watts with an average current of 20 amps, the loss equates to a resistance of 0.1Ω . The results obtained in this section demonstrate that the PSPICE simulation predicted the converter's performance quite accurately. In the future, PSPICE should prove to be an invaluable tool in predicting the performance of converters in the 100kW range.

2. Optimized Converter Waveform Analysis

In this section, only waveforms that pertain to improvement in efficiency are analyzed. The waveforms illustrated in Figures (4-14) through (4-16) show basic characteristics of any buck converter and will not be repeated. Only full-load waveforms are examined as discussed earlier.

The voltage across S_a and S_m and the current through L_r are shown in Figure (5-12). When S_a is gated "off," the voltage builds up significantly slower and drops abruptly when L_r is exhausted of energy as compared to Figure (4-19). The PSPICE simulation study depicted in Figure (5-3) predicted the measured results accurately. Voltage V_{S_a} in Figure (4-19) builds up rapidly and remains at V_{dc} while mode 5x occurs. Mode 5x does not occur in the optimized design, as $V_{C_{r2}}$ approaches to within a few volts of V_{dc} . Figure (5-13) shows the large current pulse through D_2 as C_{r2} discharges during mode 8. After the current pulse, the small current through D_1 , D_2 and L_r due to the voltage across D_m occurs as before. When S_m is gated "on" and S_a is subsequently gated "off," no mode 5x current pulse through D_2 is seen.

Figure (5-14) documents the voltage across S_a , S_m , D_1 and C_{r2} for all of the modes. Comparing the results to Figure (4-21), it is seen that $V_{C_{r2}}$ no longer falls off after mode 5 due to the reverse recovery of D_1 and D_2 . Since $V_{C_{r2}}$ does not completely reach V_{dc} , mode 7 occurs briefly and the sudden voltage jump is labeled in Figure (5-14).

The voltage across and current through S_m is depicted in Figure (5-15). As expected, the IGBT is gated "on" in a ZVS condition with no changes when compared to Figure (4-18). No changes were expected, as the optimization only affected S_m during turn-off.

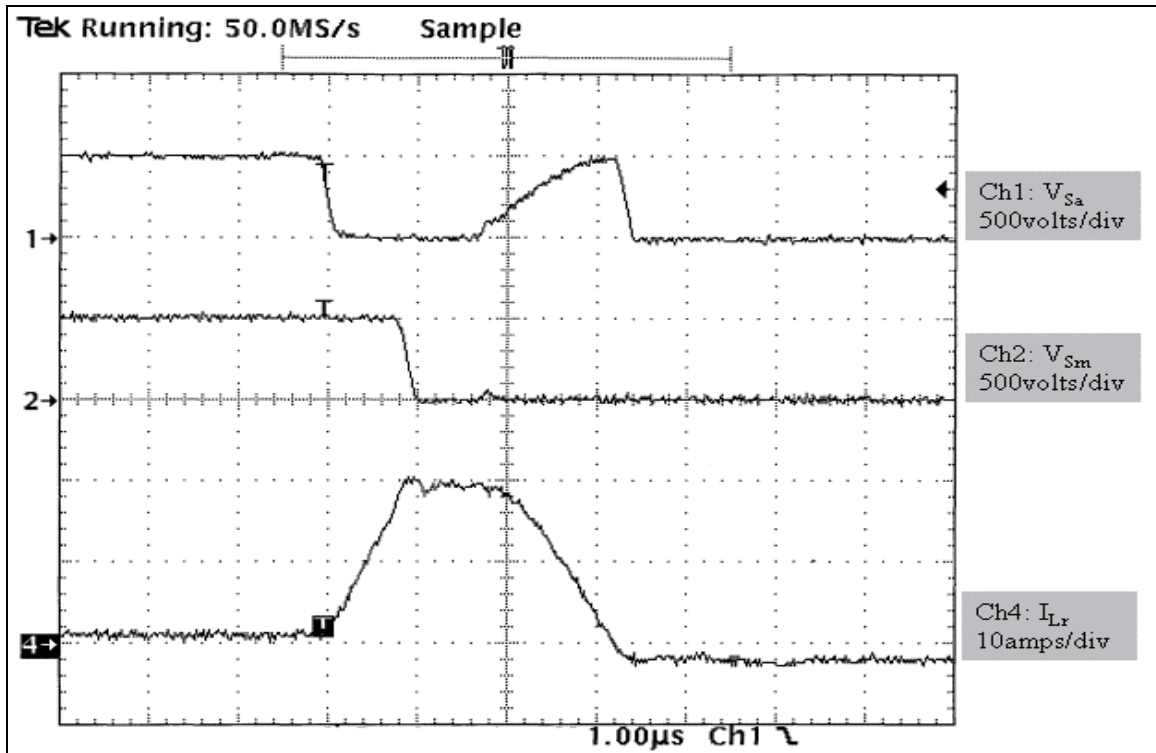


Figure 5-12. V_{Sa} , V_{Sm} and I_{Lr} During Turn-On (1μs/div).

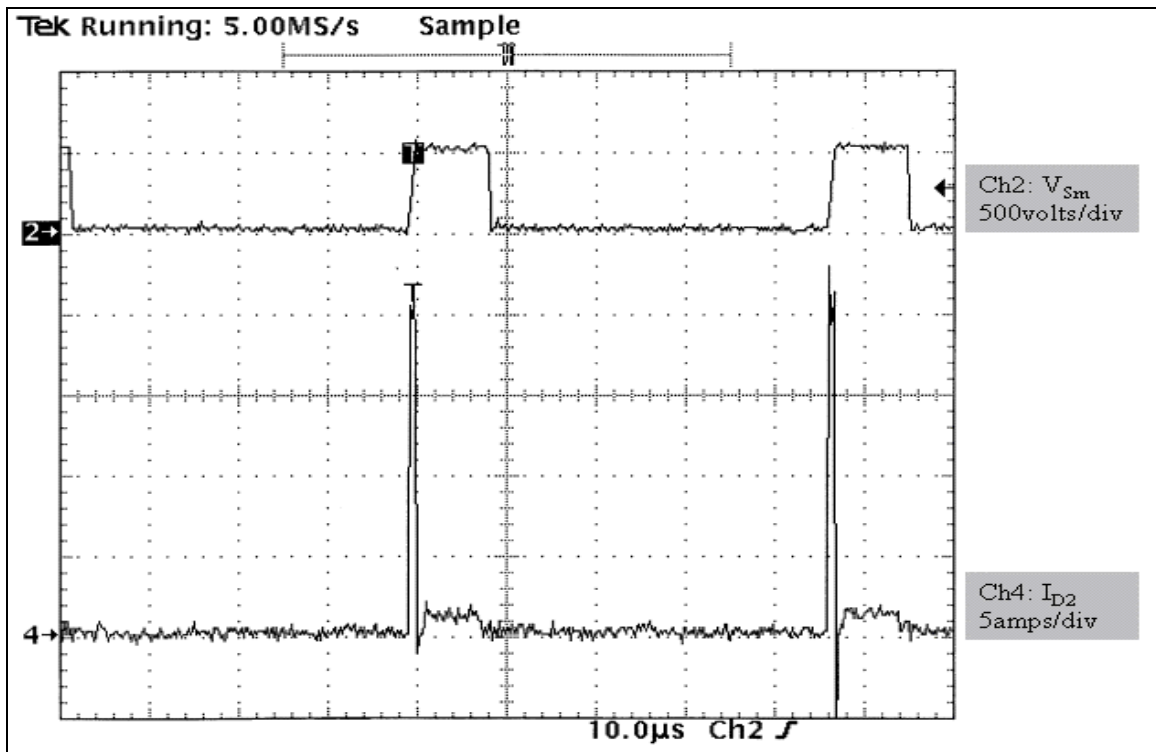


Figure 5-13. V_{Sm} and I_{D2} for Modes 1 Through 8 (10μs/div).

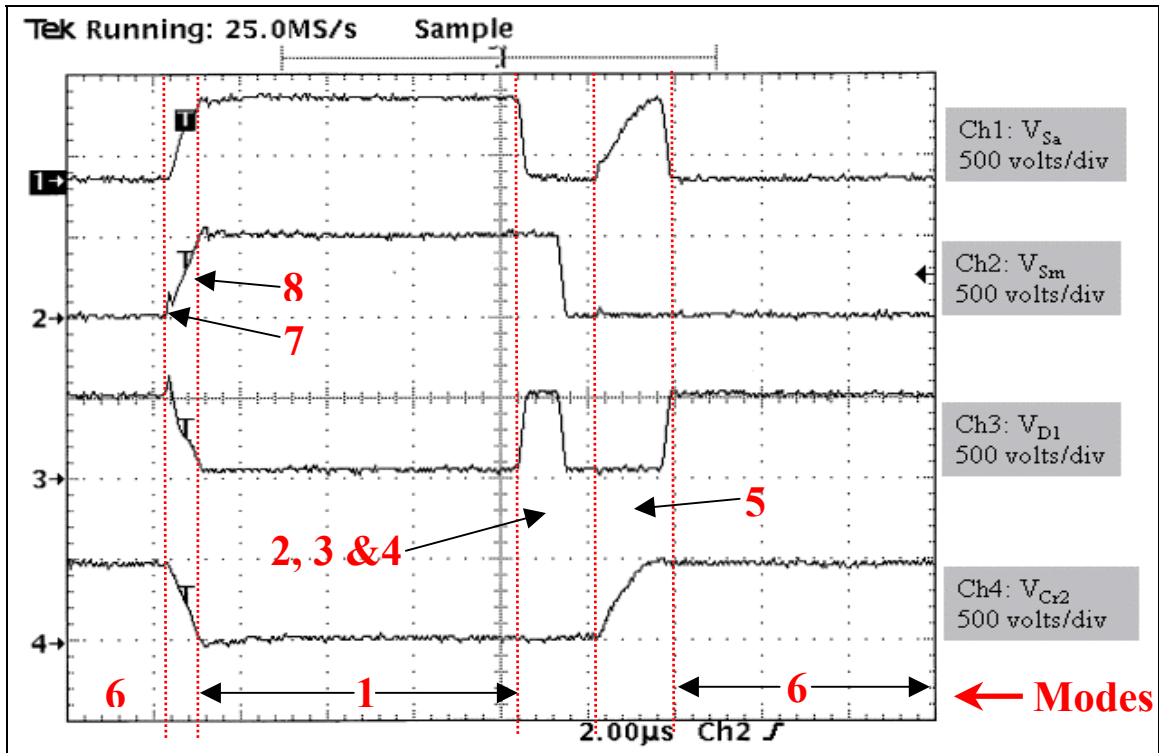


Figure 5-14. Comparison of V_{Sa} , V_{Sm} , V_{D1} and V_{Cr2} During Modes 1 Through 8 (2µs/div).

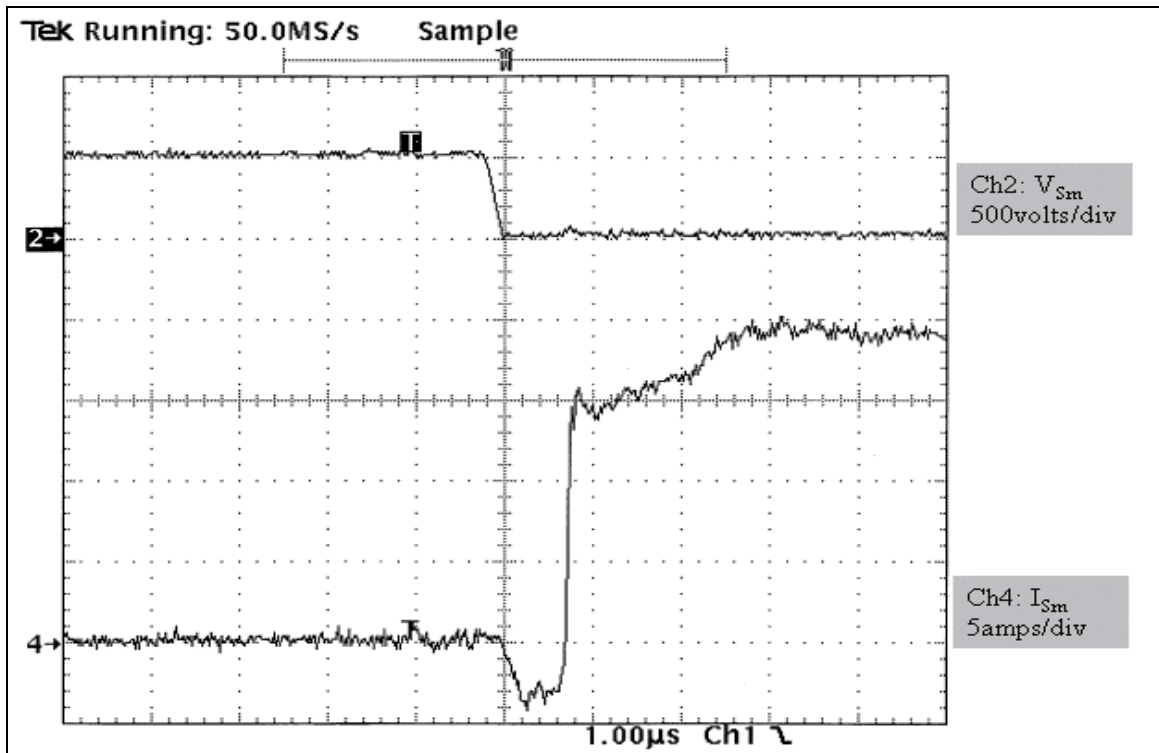


Figure 5-15. V_{Sm} and I_{Sm} During Turn-on (1µs/div).

The voltage V_{Sm} and current I_{Sm} during turn-off is shown in Figure (5-16). Significant reductions in turn-off losses are observed as the voltage across the switch rises much slower, while the current falls off quicker (Figure (4-24) may be referred to for comparisons with the original design). The power loss can be estimated by treating the voltage waveform as a right-sided triangle with a height of 500 volts and the current waveform as a triangle with a base of 800ns and height of 5 amps. Using the geometries in an EXCEL spreadsheet, the loss is estimated to be 15 watts. This estimate does not include the loss during the mode 7 voltage jump when the current is still quite high. If the actual data was available from the oscilloscope, it is believed that the calculated losses would approach 30 watts as estimated in the simulation.

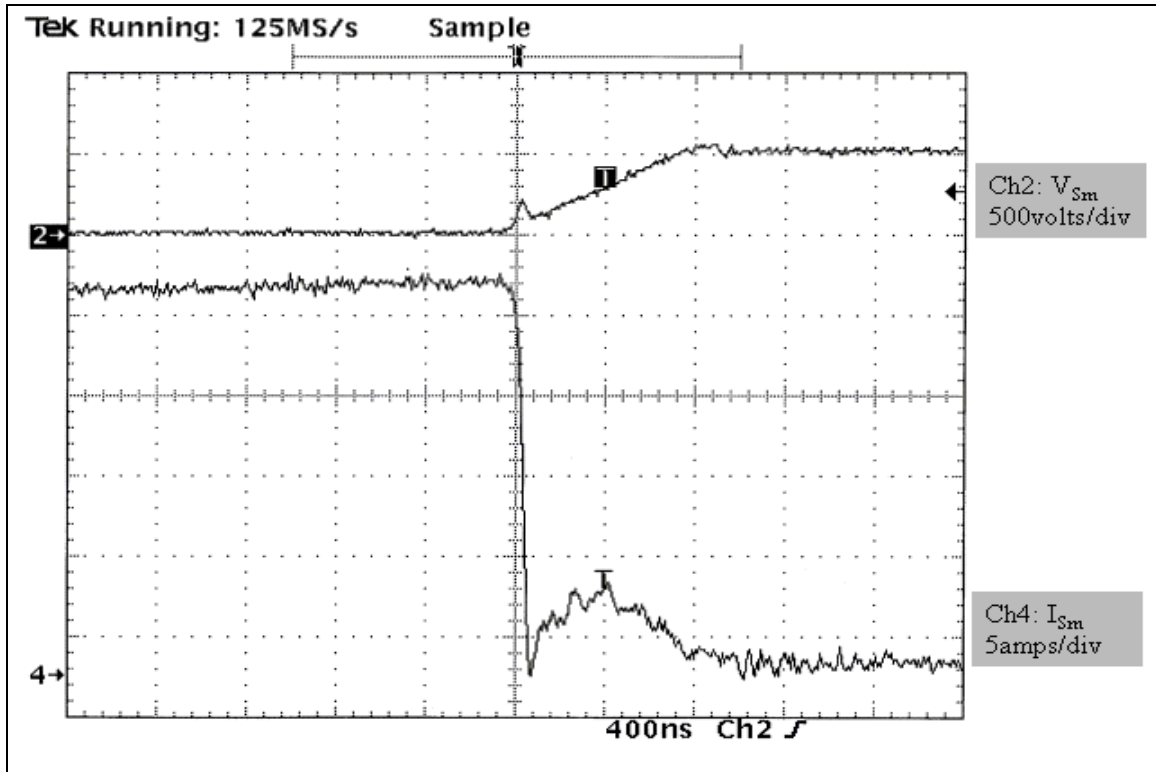


Figure 5-16. V_{Sm} and I_{Sm} During Turn-Off (400ns/div).

The results in Chapter V also agree with what Wang, Lee and Borojovic found in reference [27]. The authors found that the best reduction in turn-off losses in a ZVS IGBT is approximately 50 percent due to the ever-present current tail. In their research

they found that the current tail actually looks like a "bump" when using large amounts of capacitance. The current "bump" can never be eliminated in a ZVS scheme due to the necessity for recombination. As a result, the ZVS design can never produces a lossless turn-off, but significant improvements are made compared to a hard-switched converter.

3. Converter Performance as a Function of C_{r2}

In the final testing of the optimized converter, three other values of C_{r2} were investigated to assess the impacts on efficiency. Values of 20nF, 40nF and 50nF were tried and compared to the results obtained with the 30nF capacitor. In each case the efficiency hovered around 98.3 percent and it was difficult to see any appreciable differences. Figures (5-17) through (5-20) compare V_{Sm} , V_{Sa} and V_{Cr2} for the different values of C_{r2} . The figures show the growth of mode 7 as C_{r2} increases. In the case of Figure (5-17), mode 5x occurs since the energy in the resonant inductor exceeds the energy in C_{r2} .

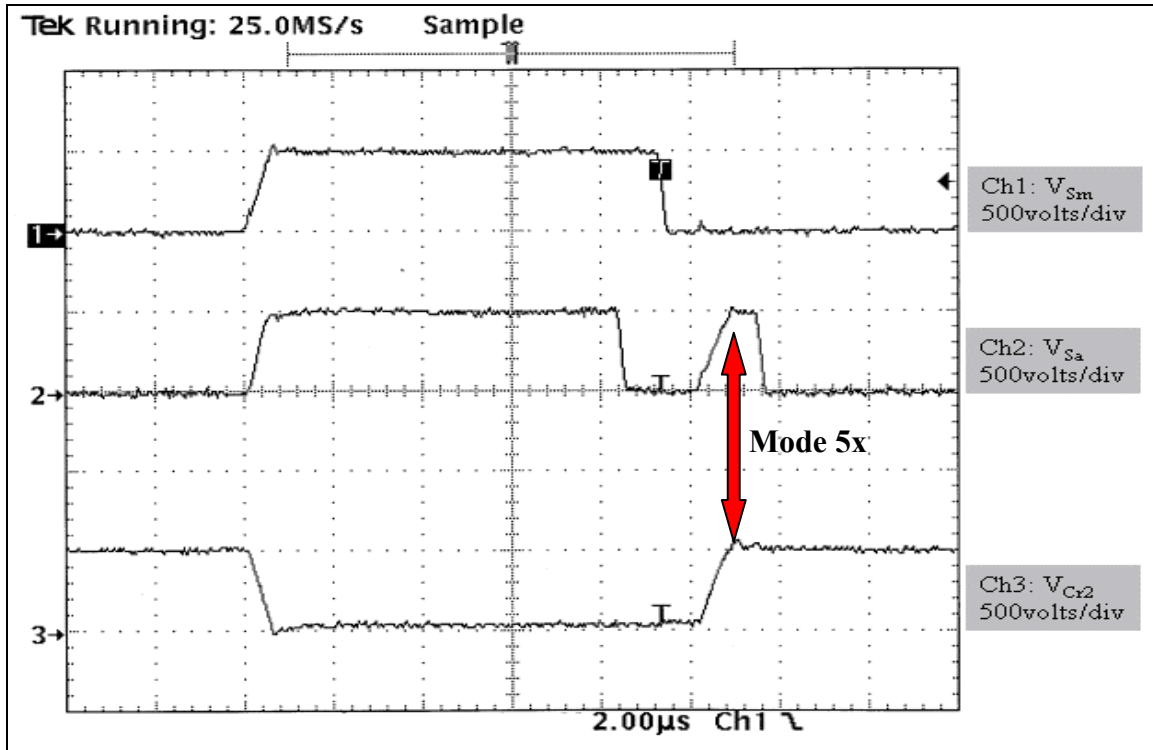


Figure 5-17. Voltages V_{Sm} , V_{Sa} and V_{Cr2} for $C_{r2}= 20\text{nF}$ ($2\mu\text{s/div}$).

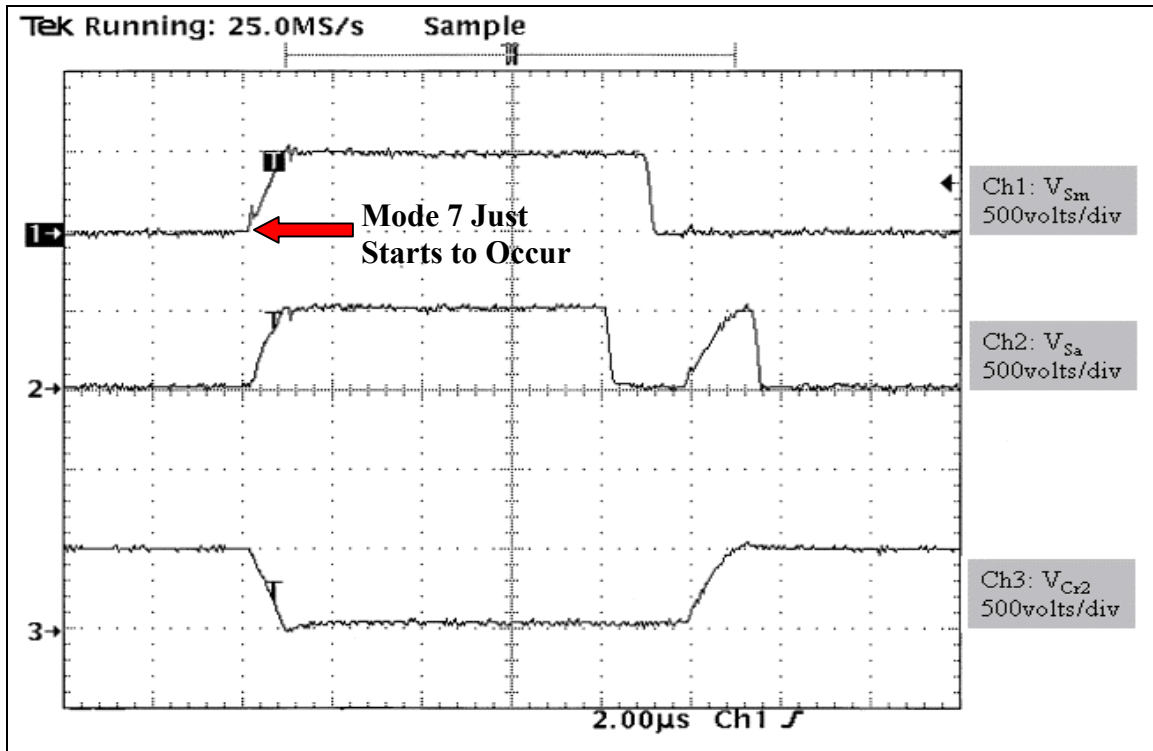


Figure 5-18. Voltages V_{Sm} , V_{Sa} and V_{Cr2} for $C_{r2}=30\text{nF}$ ($2\mu\text{s}/\text{div}$).

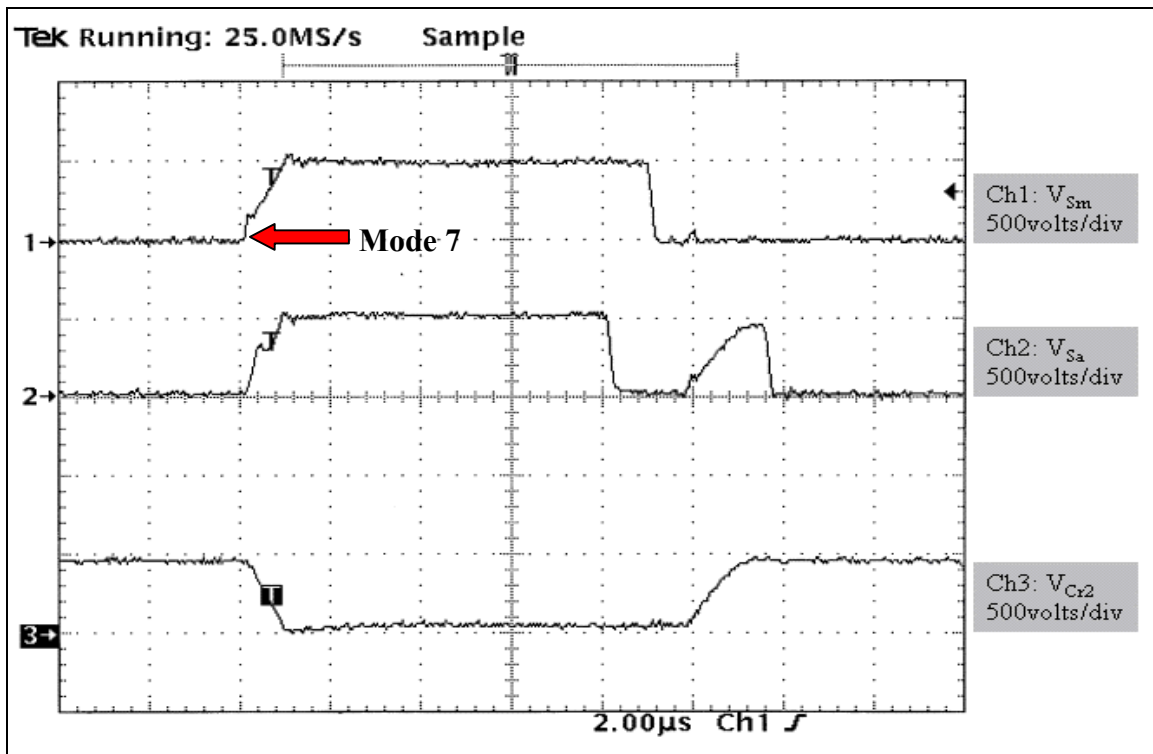


Figure 5-19. Voltages V_{Sm} , V_{Sa} and V_{Cr2} for $C_{r2}=40\text{nF}$ ($2\mu\text{s}/\text{div}$).

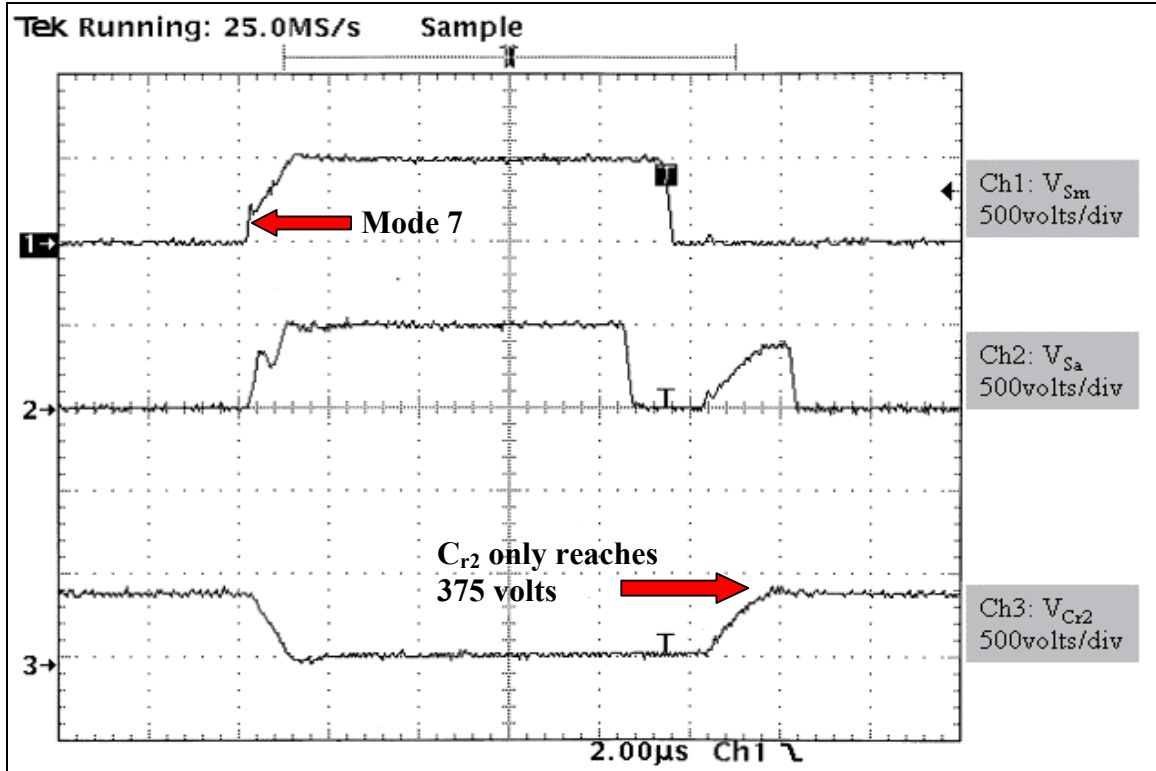


Figure 5-20. Voltages V_{Sm} , V_{Sa} and V_{Cr2} for $C_{r2}=50\text{nF}$ ($2\mu\text{s/div}$).

Upon inspection of Figures (5-17) through (5-20), it appears that the choice of 30nF for C_{r2} was the best possible. For $C_{r2}=30\text{nF}$, mode 7 just starts to occur and mode 5x cannot occur since V_{Cr2} is less than V_{dc} .

C. CHAPTER SUMMARY

The results in Chapter V demonstrate that significant improvements in the converter's efficiency can be realized with simple component changes. By optimizing the converter, the power dissipation between S_m and S_a was reduced by over 35 watts. This reduction not only improved the efficiency, but also allows the IGBTs to operate at a cooler temperature for a given size of heat sink. If this design is a candidate for a 100 kW converter in the future, optimization might allow a smaller IGBT to be used that otherwise could not handle the power dissipation. In the next chapter, the Electromagnetic Interference (EMI) emanating from the converter is studied and that data is compared to that obtained for the hard-switched converter.

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VI. ELECTROMAGNETIC INTERFERENCE

A. ELECTROMAGNETIC INTERFERENCE THEORY

With the advent of switching power converters, Electromagnetic Interference (EMI) generation has become more of a problem due to the rapid voltage and current changes inherent in converters. From Fourier theory, it is known that any signal with sharp rise times will generate a frequency spectrum rich in harmonics. The generated EMI can effect the proper operation of other equipment in the system or upset its own operation. The EMI can be transmitted by either radiation or conduction. Radiated EMI is significantly reduced by radio-frequency (RF) tight enclosures and will not be discussed or measured in this thesis. Conversely, conducted EMI flows on the power input and output lines and can interfere with other equipment connected to the power lines. Furthermore, the power lines can look like an antenna and the conducted EMI will then radiate RF energy and upset equipment not even fed by the same power lines. As a consequence, a bad EMI problem is expensive to repair and difficult to predict when building a system of several converters. The best prevention is to minimize a converter's EMI before it is placed in a larger system such as a DC ZEDS.

Conducted EMI can further be broken down into differential-mode interference and common-mode interference. The differential-mode interference is associated with the harmonics of the current waveforms in the converter, for example, the switch or main inductor current. In contrast, common-mode interference is strictly due to the stray capacitance between circuit paths and ground and the electric and magnetic fields produced in these circuit paths [6]. The conducted EMI components for the DC-DC converter are depicted in Figure (6-1).

Figure (6-1) illustrates that current flowing through the common-mode paths is directly proportional to the dv/dt across the stray capacitance and the differential-mode current is proportional to the di/dt of the circuit path. If these voltage and current rates of change are decreased, in theory, the conducted EMI levels at the higher frequencies will also decrease. The easiest way to decrease the voltage and current rates is to use a resonant soft-switching converter design.

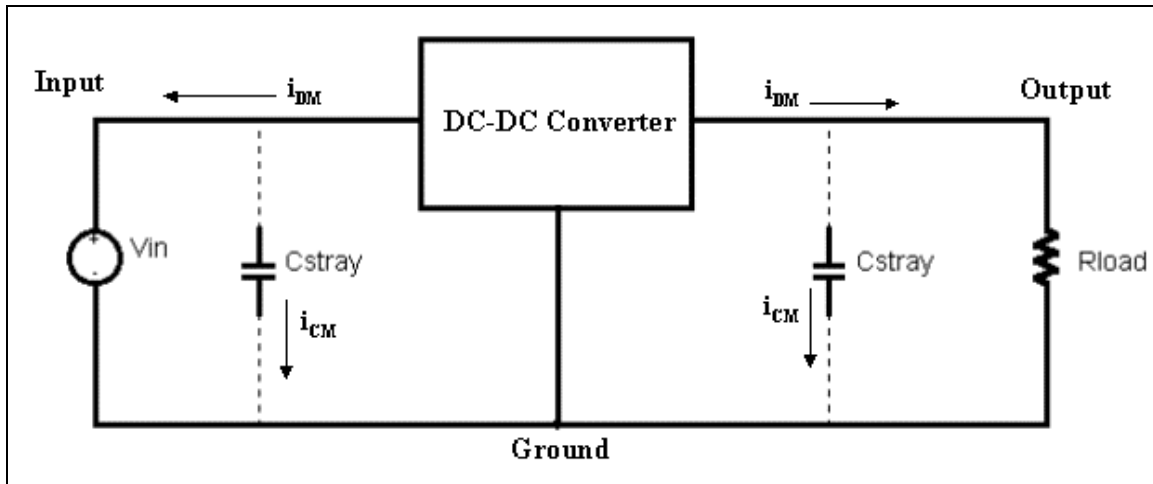


Figure 6-1. Conducted EMI Components.

1. Predicting EMI Performance

Several papers have been written which describe different techniques to estimate the amount of conducted EMI a converter will generate. The authors in reference [28] use complex component models to simulate an inverter. The component models were accurately developed to account for stray capacitance and inductance. Simulations were run and a Fast Fourier Transform (FFT) was used to estimate the EMI spectrum from the time-domain data.

The authors in reference [29] describe a simpler method. The authors treated the converter as a linear network and estimated the spectrum envelope by multiplying the Fourier transform of the current waveform by the transfer function of the input and output filter networks. This technique quickly produces an estimate of the EMI spectrum envelope, but fails to account for the stray reactances and thus the common-mode interference. Since the stray components are closely tied with the construction layout, it would be difficult to estimate the EMI prior to actual testing. A designer with experience could estimate the magnitude and position of the stray components and derive a more accurate model.

The author in reference [30] offered another approach. Instead of simulating the converter, which is difficult in that all stray components must be accounted for, the authors built a converter and studied how circuit layout affected the EMI performance.

The authors built a full-bridge DC-AC converter and changed parameters, such as wire length, inductor self-capacitance and heat sink position and then compared the results. The experiment did not predict EMI performance, but rather showed how circuit layout can minimize the amount of EMI that a converter generates. In the experiment, the authors proved that if the inductor self-capacitance is minimized along with current-loop area and stray capacitance, significant reductions in EMI could be achieved.

No attempt was made to predict the EMI performance of the converter described in this thesis, but the resonant frequencies of the capacitors and inductors were measured to better understand how they will affect the filter frequency response and hence the EMI spectrum. The updated resonant converter design with the non-ideal equivalent capacitor and inductor circuits is shown in Figure (6-2). All real inductors have a self-capacitance between the windings and capacitors have an equivalent series inductance (ESL) component as discussed in Chapter IV. The self-resonances of the main inductor and bypass capacitors were measured in the laboratory. To measure the self-impedances, a test circuit was built using the component under test (capacitor or inductor), an external resistor, a signal generator and an oscilloscope. The test circuit is illustrated in Figure (6-2). The signal generator frequency was changed until a distinct dip in the voltage across the measurement point was seen. Based on the frequency of the resonance-dip, a self-capacitance or inductance was calculated using either Equation (6-1) or (6-2).

$$C_L = \frac{1}{(2\pi f_r)^2 L} \quad (6-1)$$

$$L_{C_{bypass}} = \frac{1}{(2\pi f_r)^2 C_{bypass}} \quad (6-2)$$

The corresponding self-resonant frequencies and self-component values are listed in Table (6-1).

To demonstrate the affect of the non-ideal capacitors and inductor, a PSPICE simulation was conducted to estimate the frequency response of the output LC filter section. The simulated output LC filter section is inside the dashed box in Figure (6-3).

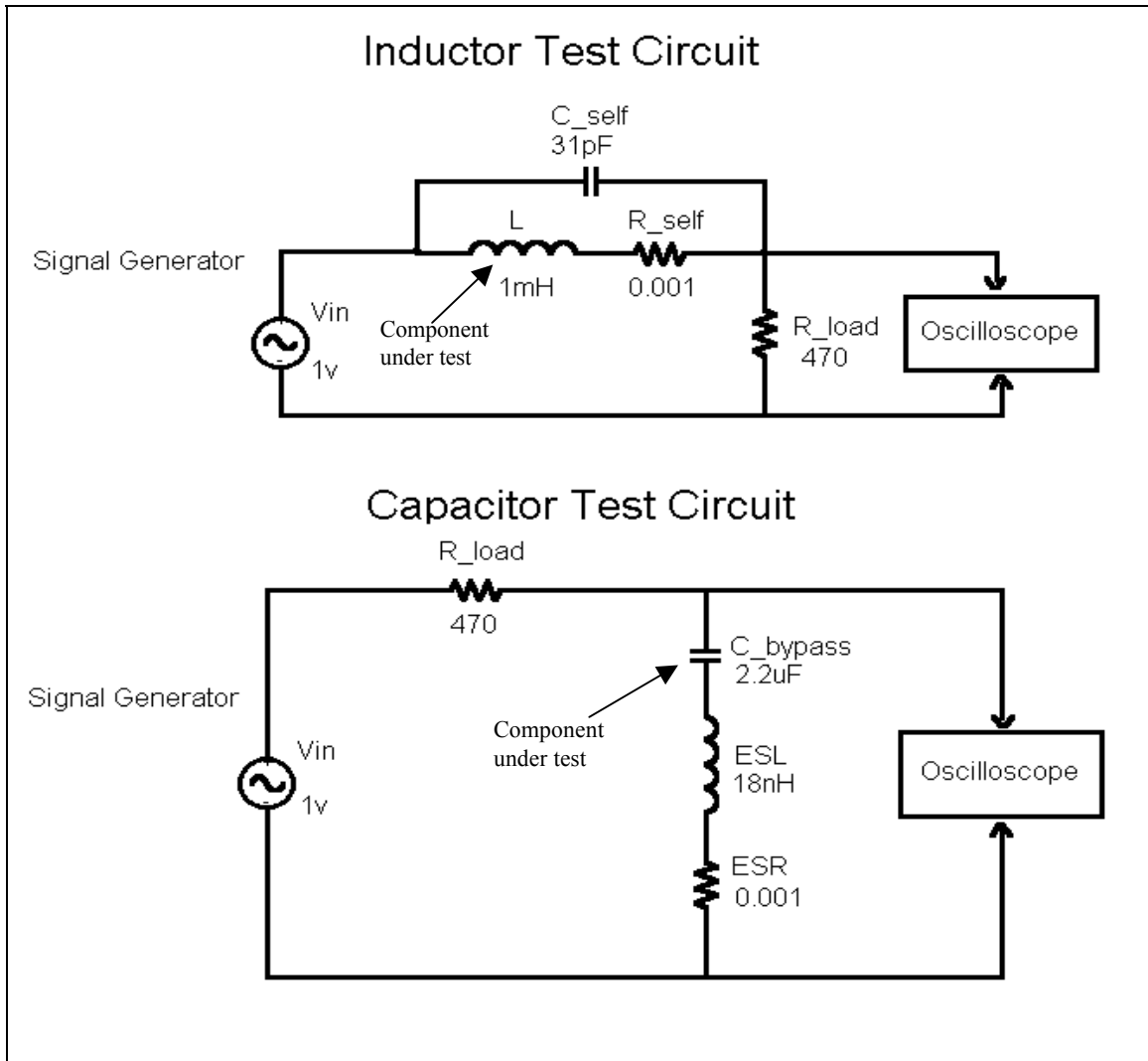


Figure 6-2. Test Circuit Used to Measure Self-Capacitance and Inductance.

Component	Value	Type	Self Capacitance or Inductance	Resonant Frequency
L	1 mH	5.2-inch toroid	31pF	918.9 kHz
C	500 μ F	Electrolytic	40nH	35.6 kHz
C _{bypass}	2.2 μ F	Polyester	18nH	800.0 kHz

Table 6-1. Output Filter Component Values and Self-Resonant Frequencies.

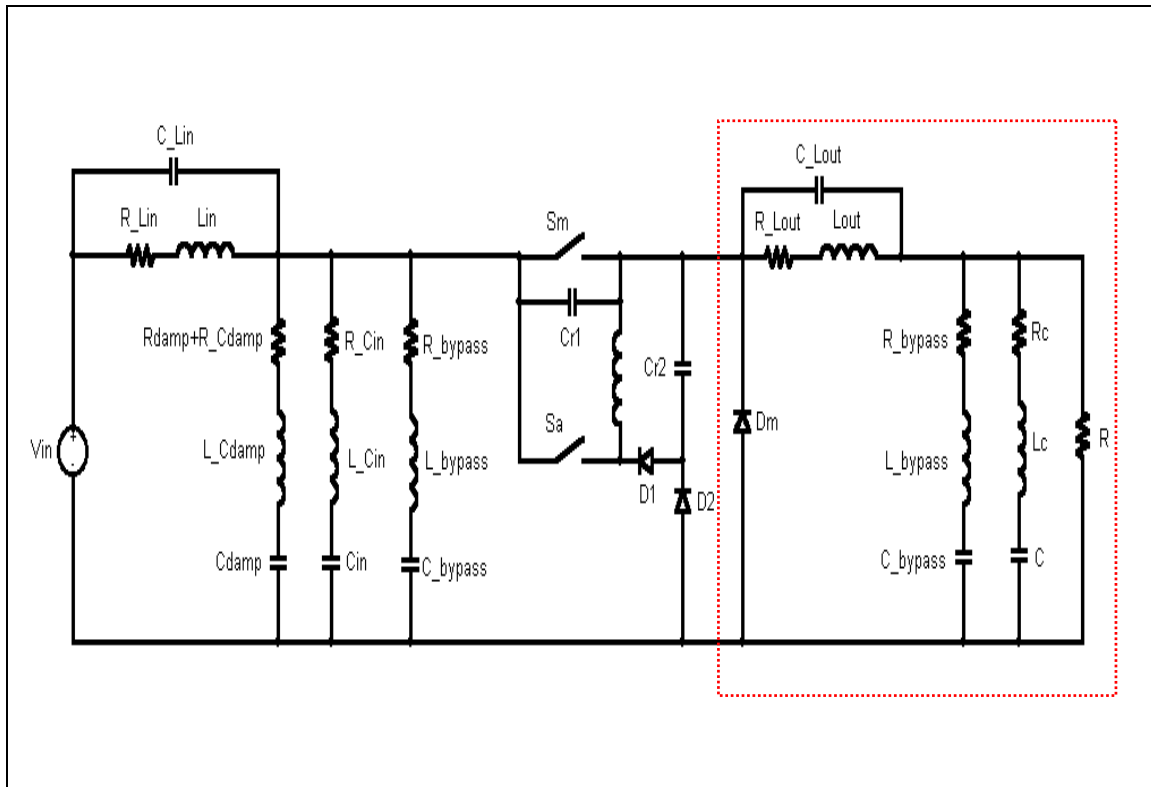


Figure 6-3. Resonant Converter Circuit with Additional Self Inductances and Capacitances.

Figure (6-4) shows that substantial attenuation still occurs above the switching frequency, but considering the amplitude of the voltages and currents involved, significant harmonic currents will still flow in the load depending on the spectrum of the wave shapes. Figure (6-4) also shows a +40 dB per decade trend after 1 MHz. This will not occur, as stray capacitances will supply additional poles above 1 MHz resulting in a net negative magnitude slope. The location of these high-frequency parasitic poles is unknown. The notches in the frequency response correspond to the resonant frequencies of the parallel and series LC circuits. The tank circuit formed by L and its self-capacitance and the series-resonant circuit formed by the bypass capacitor C_{bypass} and its self-inductance cause the notches near 1 MHz. The sharp resonant peaks are not expected to occur, as the actual circuit will have a significantly reduced quality factor due to circuit losses.

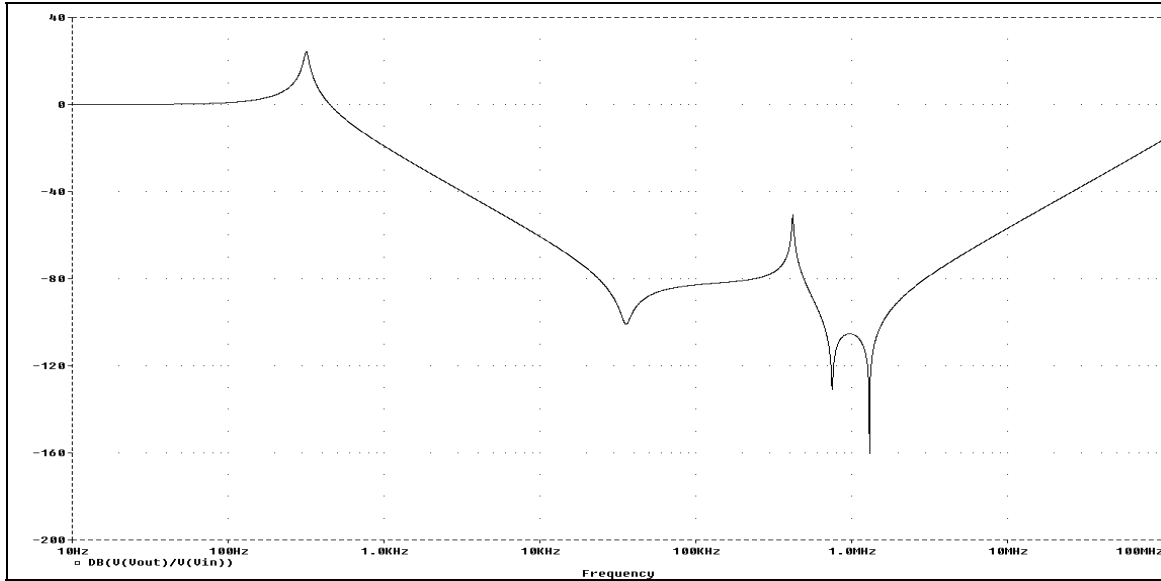


Figure 6-4. Frequency Response of the Converter Output Filter.

B. ELECTROMAGNETIC INTERFERENCE TESTING

One of the frequently advertised advantages of a resonant converter is the reduction in EMI generation. With a reduced dv/dt and di/dt , the resonant converter should have a narrower EMI spectrum at a minimum. If the auxiliary circuit layout is improperly constructed, it is possible that a resonant converter will have an aggravated EMI problem when compared to a hard-switched converter [31]. These auxiliary circuit problems could stem from either an excessive enclosed loop area or capacitive coupling into the surrounding circuitry or chassis. In the Joung resonant converter, large circulating currents exist between L_r , C_{r1} and C_{r2} and it is unknown if these resonances will cause unwanted peaks in the EMI spectrum.

Since the resonant converter was built at the same time as the hard-switched converter [5], a unique opportunity to compare the EMI generation between the two converters existed. Both converters were also constructed with identical input and output filter sections, which makes the comparison even more meaningful.

Andrew Parker and Ray Vincent of Naval Postgraduate School's Signal Enhancement Laboratory donated their time and equipment to complete the EMI testing. The Signal Enhancement Laboratory is concerned with maximizing the Signal-to-Noise

(SNR) performance of communication sites by finding sources of interference and making recommendations on how to alleviate the problem. Since switching type converters and Uninterruptible Power Supplies (UPS) are becoming more common in the military, the laboratory personnel were interested in obtaining data needed to evaluate the impact of EMI from such devices on other shipboard systems. They were also interested in gathering EMI information to serve as an aid in designing power converters in the future. The authors published their results on the pre-optimized resonant converter [32].

This chapter will document the EMI testing of the hard-switched and the resonant converter before and after optimization. In [32], the authors measured the EMI spectrum from 10 Hz to 100 kHz and 50 kHz to 100 MHz. The majority of the EMI problems in the low-frequency spectrum were associated with harmonics of the three-phase rectified DC source and the results will not be repeated here. The other major EMI frequencies below 100 kHz were at the switching frequency (20 kHz) and its even harmonics (40, 60 kHz, etc.). Since both converters have identical filtering networks and operate at the same power level, each converter produces similar energy at the switching fundamental and its harmonics. As a result, the low-frequency EMI measurements between the hard and soft-switched converter were nearly identical (Refer to reference [32] for the low-frequency EMI results). The differences between the hard and soft-switched converter's EMI show up in the frequency range between 100 kHz to 100 MHz. The EMI results for this frequency range are documented in this chapter.

1. EMI Test Setup

A block diagram of the high-frequency EMI measurement system is illustrated in Figure (6-5). The converter's input or output wire is passed through the current probe and the inductively-coupled signal is then amplified and sent to the spectrum analyzer. The spectrum analyzer output is then sent to a 3-axis display monitor so that time variation in the frequency spectrum can be observed and stored. An oscilloscope camera is then used to record the EMI spectrum. The equipment used in the EMI testing is listed in Table (6-2).

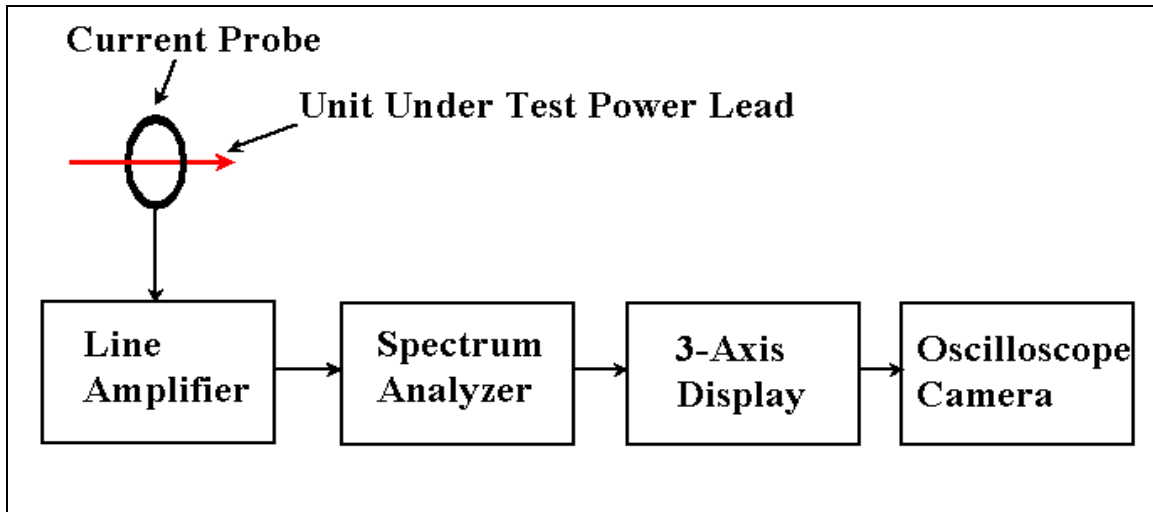


Figure 6-5. Block Diagram of High-Frequency EMI Measurement System (after ref. [32]).

Equipment	Manufacturer	Model Number
Spectrum Analyzer	Hewlett-Packard	141
3-Axis Display	ELF Engineering	7200B
Line Amplifier	Olektron	B-HIA-20-HF
Current Probe	Fischer	70
Camera	Tektronix	C-5C

Table 6-2. High-Frequency EMI Measurement Equipment.

The converters were tested at full power (8 kW output) as described Chapter IV and V using the test setup of Figure (4-12). The setup was not altered during the testing phase so that the results obtained for the hard-switched and soft-switched converter could be compared.

The EMI test setup described in this thesis differs from test procedures outlined in MIL-STD-461E and ANSI/IEEE C63.4 in that a Line Impedance Stabilization Network (LISN) was not used. A LISN isolates the Unit Under Test (UUT) from the power source, thus ensuring that any EMI seen with the spectrum analyzer is from the UUT and not the power source. The standards specify the component values and frequency response characteristics for the LISN. Using a LISN, as defined in the standards, assures

that the measurements are repeatable, so that different testing facilities can duplicate the results. Using a LISN is a disadvantage in that artificial impedances are added between the UUT and the power source. It would also be difficult to build a LISN that could handle high power levels over a wide bandwidth, without having problems from the non-ideal characteristics of inductors and capacitors. The test setup illustrated in Figure (6-4) has the advantage that it more accurately represents the conditions the converter will "see" on a ship. The consistency in the NPS Power Laboratory EMI test setup ensures that the data for both converters can be compared, but not with other published results in the technical journals. No attempt will be made to compare the results here to MIL-STD-461E or ANSI/IEEE C63.4, since they define the measurement point at a low impedance tap in the LISN and state the limits in units of dB μ V (dB referenced to 1 μ V). The EMI spectral amplitude data from the test setup of Figure (6-5) is in units of micro amps and cannot be compared to a voltage measured in a low impedance point in the LISN.

2. High-Frequency EMI Test Results

The conducted EMI on the DC input power line was analyzed first. The input EMI spectrum for the hard and soft-switched converter is shown in Figure (6-6). To see how the optimization affected the EMI, the pre-optimization and post-optimization EMI spectrum pictures are included in Figure (6-6). In each converter's EMI spectrum, considerable high-frequency energy is being conducted into the input power line leading to the three-phase six-pulse rectified DC supply.

To make comparisons between the plots, the amplitudes are scaled in 20dB steps. The Fischer model 70 current probe is calibrated so that -60dBm equals a current of $224\mu\text{A}$ over a bandwidth of 100 kHz to 100 MHz. To make bandwidth comparisons between the EMI spectrums, a level of -80dBm or $22.4\mu\text{A}$ was arbitrarily chosen as the threshold level. In [32], the authors have found that EMI currents as small as $10\mu\text{A}$ between 100 kHz and 100 MHz can degrade communication systems.

In Figure (6-6a), the hard-switched converter has EMI which exceeds $22.4\mu\text{A}$ out to approximately 35 MHz. The hard-switched converter also has a maximum peak of

700 μ A centered at 2 MHz. In Figure (6-6b), the pre-optimized resonant converter remains above 22.4 μ A until approximately 15 MHz. The response then experiences a deep null and appears to crest at 22.4 μ A at a frequency of 20 MHz. The maximum amplitude is 2.24mA at a frequency of 5 MHz. The current response of the optimized converter in Figure (6-6c) remains above 22.4 μ A until approximately 38 MHz with a maximum peak of 1.26mA at 3 MHz.

Figure (6-6) shows that the hard and soft-switched converters generate significant high-frequency energy on the DC input power line. The hard-switched converter has the lowest maximum amplitude ($\sim$ 700 μ A), but has significantly higher EMI from 20 to 30 MHz. For both cases of the resonant converter, the spectrum looks similar, but the optimized converter has slightly stronger EMI around 30 MHz. The overall amplitude spectrum of Figure (6-6b) appears reduced compared to Figures (6-6a) and (6-6c) due to a 10dB higher spectrum analyzer reference level.

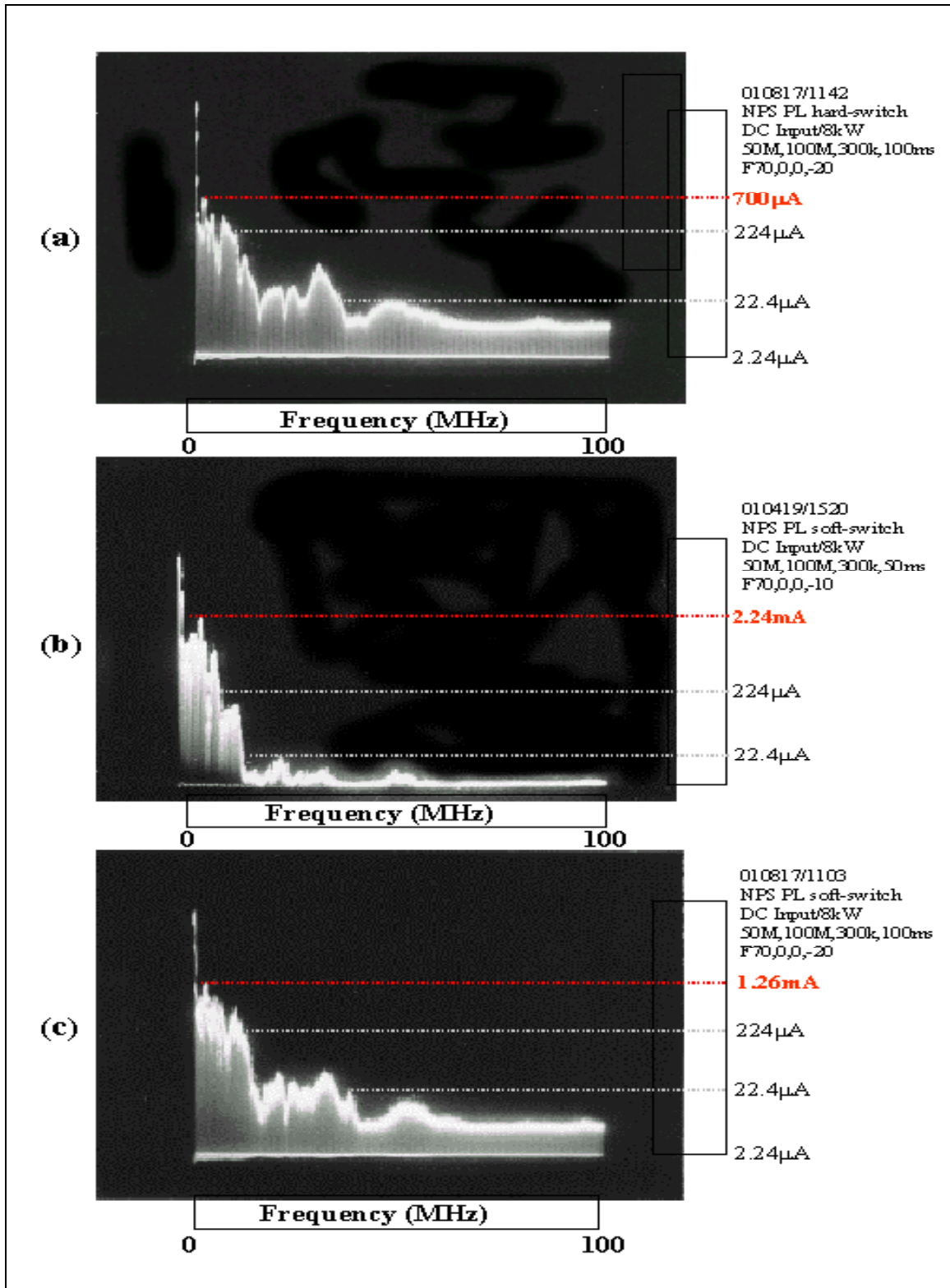


Figure 6-6. DC Input Conducted EMI Spectrum for the (a) Hard-Switched Converter, (b) Pre-Optimized Soft-Switched Converter and (c) Optimized Soft-Switched Converter (Bandwidth 0-100MHz).

The hard and soft-switched converter EMI spectrum measured at the DC output power line is illustrated in Figure (6-7). The hard-switched EMI spectrum in Figure (6-7a) exceeds 22.4 μ A all the way to 40 MHz. The hard-switched EMI spectrum has a maximum current of 7mA at 2 MHz. The pre-optimized resonant converter's EMI spectrum is even fuller with the response remaining above 22.4 μ A until approximately 45 MHz. Even more astonishing is the maximum peak of 40mA at 3 MHz. The optimized resonant converter EMI spectrum has a significantly reduced bandwidth and maximum amplitude. The amplitude falls below 22.4 μ A at 5 MHz with a peak of 890 μ A at 2 MHz. The peak EMI amplitude for the post-optimization resonant converter is 33dB below the EMI amplitude for the pre-optimized resonant converter!

The EMI results in Figure (6-6) and (6-7) are best understood if Figures (4-18), (4-24), (5-15) and (5-16) are reviewed. In Figures (4-18) and (4-24), the voltage across S_m rises and falls in about the same amount of time (~ 160 ns). During the turn-on process, the current from the source builds up through S_a and L_r ; hence, for a given load condition, the source current will have a constant rise-time ($\sim 1\mu$ s). For the pre-optimized resonant converter, the current through S_m also falls off in approximately 1μ s due to recombination. Based on these observations and knowledge of Fourier theory, it appears that for the pre-optimized case the DC input and output should have similar EMI spectrum. Not considering the deep null at 15 MHz in Figure (6-6b), both spectrums in Figures (6-6b) and (6-7b) have similar bandwidths and frequency content including the spectral hump at 50 MHz.

Conversely, the voltage across S_m has appreciably different fall and rise-times in Figures (5-15) and (5-16) (160ns versus 1μ s). The current buildup through S_a will still take approximately 1μ s during mode 2. Figure (5-16) illustrates that the current falls off rapidly as S_m is gated "off" and C_{r2} supplies its energy to keep the node voltage constant in mode 8. From a source current perspective, the turn-on di/dt is similar in both the pre-optimized and optimized converter as well as the turn-on dv/dt across S_m .

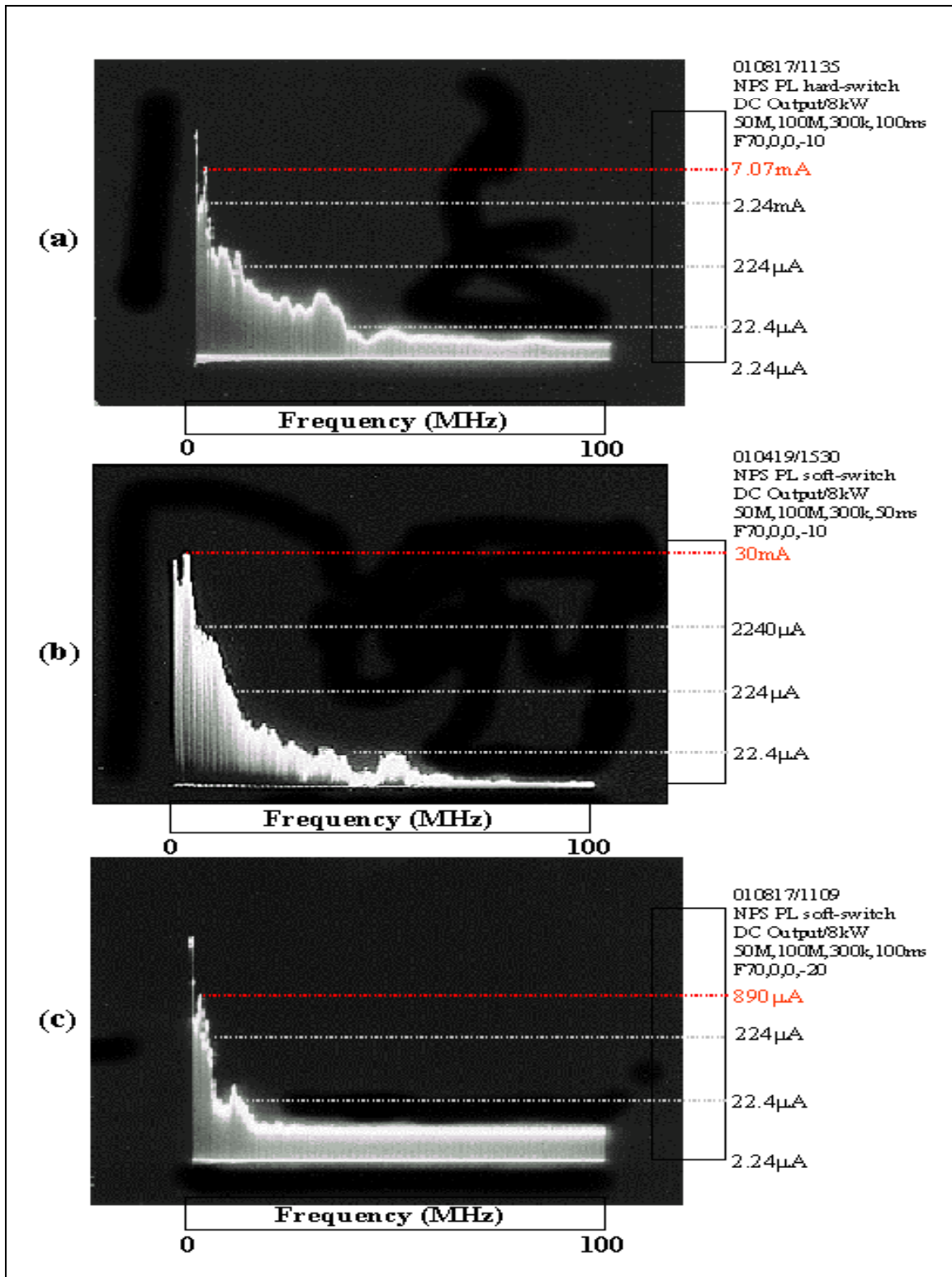


Figure 6-7. DC Output Conducted EMI Spectrum for the (a) Hard-Switched Converter, (b) Pre-Optimized Soft-Switched Converter and (c) Optimized Soft-Switched Converter (Bandwidth 0-100MHz).

From this observation, the input EMI spectrums should look similar and in fact the DC input spectrums in Figures (6-6b) and (6-7c) are comparable. The hard-switched converter has a higher di/dt from the source, but again the EMI spectrum is similar to the resonant converter.

During the turn-off of S_m in the optimized resonant converter, the voltage V_{sm} reaches V_{dc} in $1\mu s$ versus the 160ns of Figure (4-24). Since the voltage on the node connected to the emitter of S_m changes more slowly, any common-mode EMI components will be significantly reduced. Figure (6-6c) shows that the EMI bandwidth is greatly reduced from 45 MHz in Figure (6-7b) down to 5 MHz. This magnitude of reduction in EMI bandwidth is not surprising as the dv/dt between S_m and the main inductor has increased by almost a factor of ten in the optimized resonant converter.

C. CHAPTER SUMMARY

The results in this chapter demonstrate that both the hard and soft-switched converters generate significant amounts of EMI. To the common engineer or product manager, EMI currents in the range of micro amps might seem small, but these levels are substantial. Modern communications receivers have noise floors on the order of -140 dBm ($\sim 10^{-18}$ watts). EMI (radiated and conducted) from a power converter described in this thesis could severely deteriorate a communication system's performance if the two were operated near each other or if the power cables crossed near the receiver or antennas. From experience, the authors in [32] found that EMI currents as small as 2mA in frequencies between 100 Hz to 10 kHz and $10\mu A$ in frequencies between 100 kHz to 100mHz will deteriorate a shore communication facility.

There is little data on susceptibility of ship systems, but one can only assume that similar results will occur as more switching converters are used onboard ships. A future DC ZEDS zone might have ten SSCMs (DC-DC converters) operating at power levels of 100 kW each. If the EMI data in this chapter is directly scaled to these power levels, one might expect conducted current levels of a few hundred milliamps for each zone.

The data in this chapter shows that resonant soft-switching converters can reduce the EMI when compared to the more basic hard-switching converter. Obviously, this data and conclusions are based on a specific converter design, but in general, resonant converter topologies will have reduced EMI. It is interesting to note that the pre-optimized resonant converter has excellent Zero-Voltage Switching (ZVS) characteristics on turn-on with marginal ZVS performance on turn-off, yet the EMI generation is similar to the hard-switched converter. Not until the circuit was optimized for efficiency did significant improvements in EMI reduction occur. The results described in this thesis show that one must not totally assume that a resonant converter will have superior EMI performance unless testing and optimization is performed.

To reduce EMI levels further, common-mode filters need to be installed on both the input and output power lines. An EMI filter that can handle these power levels will be bulky and might also require a cooling system, thus reducing system efficiency. Of additional concern is that COTS EMI filters that are rated for greater than 100 kW at voltages exceeding 1000 volts DC are not available.

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VII. CONCLUSIONS

A. SUMMARY OF FINDINGS

This research documented the design, construction and testing of an 8kW resonant soft-switching DC-DC converter. The converter was designed so that it met the specifications set forth by ESAC for the reduced-scale IPS laboratory. The converter was constructed and tested concurrently with an 8kW hard-switched converter so that meaningful comparisons of performance, efficiency and EMI generation could be made. The key areas covered in this thesis are:

- Description of DC Zonal Electric Distribution System (DC ZEDS),
- Description of DC ZEDS components including SSCMs and SSIMs,
- Selection of suitable resonant converter topology,
- Detailed modes of operation analysis,
- Development of modal dynamic equations,
- Design of a resonant converter based on the dynamic equations,
- Detailed PSPICE simulation of the resonant converter,
- Construction of the resonant converter,
- Testing of the resonant converter to verify operation and efficiency,
- Development of an optimized design using PSPICE and MATLAB,
- Testing of the optimized resonant converter to verify improvements in efficiency, and
- Electromagnetic Interference (EMI) testing of the hard-switched, pre-optimized resonant converter and optimized resonant converter.

After the role of a DC ZEDS in future surface and submerged vessels was outlined, the basic components of the IPS were explained. This thesis focused on the Ships Service Converter Module (SSCM), which, in its most basic form, is simply a buck

chopper or DC-DC converter. Chapter I covered the past work completed at NPS in the area of DC-DC converters and explained the importance of developing resonant converters to improve efficiency and reduce EMI generation. Several topologies were investigated and the Joung topology was selected as the best candidate for this design.

In Chapter II, the selected topology was analyzed and the circuit operation was divided up into eight distinct operating modes. Mathematical models were also developed to aid in designing the converter.

Chapter III covered the design of the resonant converter and the detailed PSPICE simulations that were conducted for the maximum-load and minimum-load conditions. The efficiency was estimated to be 98.3 percent for full load and 97.6 percent for minimum load.

Chapter IV contained a description of the construction and testing of the resonant converter. The concept of a compact power module was presented as a method to reduce stray inductance. The testing demonstrated that the PSPICE simulations in Chapter III accurately predicted the converter's performance. However, during testing, it was discovered that the PSPICE diode models were less than adequate. In particular, simulation studies indicated that the reverse recovery energies were not fully predicted. The full-load efficiency was determined to be 97.9 percent, which is an improvement of 0.3 percent over the hard-switched converter. For the minimum-load condition, the efficiency was 97.5 percent, which is a 0.8 percent improvement over the hard-switched converter.

Chapter V described the optimization of the resonant converter in detail. The concept of minimizing the voltage and current rates of change was covered along with a loss analysis of modes 5x and 7. A PSPICE simulation was used along with a MATLAB program to estimate switch losses during turn-off. The estimated losses were then plotted as a function of the resonant capacitance. PSPICE simulations were then implemented on the optimized converter and the efficiency was estimated to be 98.8 percent. The resonant converter was modified and retested to verify the improvements in efficiency. The optimized resonant converter efficiency was measured to be 98.3 percent, which is a

0.4 percent improvement over the pre-optimized converter and an improvement of 0.7 percent over the hard-switched converter. The 0.7 percent improvement equates to a power loss reduction of 62.5 watts in the switches while supplying 8kW to the load.

Finally, Chapter VI described the theory of EMI and how a resonant soft-switching converter can be used to reduce EMI levels. EMI measurements were conducted on the hard-switched and resonant converter. Further EMI measurements were done before and after optimization. The EMI testing showed that one cannot assume that a resonant converter will have superior EMI reduction. The pre-optimized resonant converter had significant EMI generation and performed less effectively than the hard-switched converter in the case of the DC output line. The optimized converter had significant reductions in the EMI levels on the DC output line, but similar DC input EMI levels when compared to the other converter measurements. The results in Chapter VI demonstrated that improving efficiency also reduces EMI generation drastically.

The objectives of the thesis as outlined in Chapter I were met. A resonant converter was designed, simulated, constructed and tested and substantial improvements over the hard-switched converter in the area of efficiency and EMI generation were achieved. The resonant converter has some disadvantages when compared to the hard-switched converter, such as:

- The control circuit complexity increases because of the addition of an auxiliary switch along with more stringent timing criteria;
- The required development of faster driver boards with short-circuit and minimum-pulse protection (no suitable COTS driver boards available);
- The auxiliary switch must handle maximum converter current and voltage at any given time and, therefore, the auxiliary switch must have the same ratings as the main switch;
- It is more difficult to acquire suitable resonant capacitors and build resonant inductors as converter power levels increase.

If DC ZEDS simply required a converter to operate at the 8kW level, the hard-switched converter would be the best choice. The converter displayed adequate efficiency and has the added benefit that commercially made driver boards are available. The driver boards have desirable safety features and make it easy to interface an IGBT switch to a digital control system.

As the specified converter power rating is increased, a resonant converter will enable the designer to use a smaller IGBT than would otherwise be needed for a hard-switched converter. The IGBT in the hard-switched converter was dissipating approximately 200 watts, while supplying 8kW to the load. The IGBT was rated for a power dissipation of 700 watts, so theoretically a hard-switched converter switching at 20 kHz could supply 28kW to a load using this device. A resonant converter could be designed using the same IGBT for the main and auxiliary switch. With a 40 percent reduction in device losses, the converter could supply almost 40kW to the load. This is a hypothetical comparison and the designer would need to account for the IGBT thermodynamic requirements at such power levels. This thesis did demonstrate that small IGBTs could be used at high power levels.

B. FUTURE WORK

This thesis has demonstrated that the resonant DC-DC converter is a viable option for the DC ZEDS in a modern warship. The following issues need to be addressed further to ensure that the best possible DC-DC converter design is used in the DC ZEDS of the future:

- The further study of EMI problem including research on how to best reduce EMI with converter layout and filtering;
- The refinement of PSPICE IGBT and diode models, so that designers can reliably simulate converters operating at power levels exceeding 100kW;
- The design and development of a Digital Signal Processing (DSP) based control and protection circuit;

- The construction of a reduced-scale IPS at NPS, so that professors and students can study converter interfacing, paralleling and stability issues.

Given that future submarines and surface ships will likely have some form of a DC ZEDS on board, it is imperative that more research be conducted in the area of power converters to ensure that efficient and reliable systems are delivered to the fleet.

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APPENDIX A. COMPONENT DATA SHEETS

A. INTERNATIONAL RECTIFIER IRG4PH50UD

International
IR Rectifier

INSULATED GATE BIPOLAR TRANSISTOR WITH
ULTRAFAST SOFT RECOVERY DIODE

Features

- UltraFast: Optimized for high operating frequencies up to 40 kHz in hard switching, >200 kHz in resonant mode
- New IGBT design provides tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

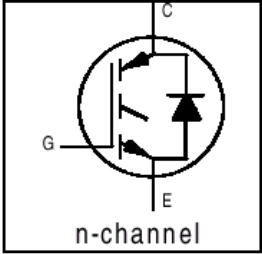
Benefits

- Higher switching frequency capability than competitive IGBTs
- Highest efficiency available
- HEXFRED diodes optimized for performance with IGBT's. Minimized recovery characteristics require less/no snubbing

PD 91573A

IRG4PH50UD

UltraFast CoPack IGBT

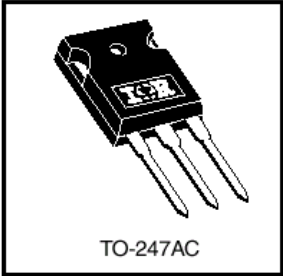


n-channel

$V_{CES} = 1200V$

$V_{CE(on)} \text{ typ.} = 2.78V$

@ $V_{GE} = 15V, I_C = 24A$



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	45	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	24	
I_{CM}	Pulsed Collector Current ①	180	
I_{LM}	Clamped Inductive Load Current ②	180	
$I_F @ T_C = 100^\circ C$	Diode Continuous Forward Current	16	A
I_{FM}	Diode Maximum Forward Current	180	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	200	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	78	
T_J	Operating Junction and	-55 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.64	$^\circ C/W$
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage ^③	1200	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.20	—	V/ $^\circ\text{C}$	$V_{GE} = 0V, I_C = 1.0mA$
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.56	3.5	V	$I_C = 20A$ $V_{GE} = 15V$
		—	2.78	3.7		$I_C = 24A$
		—	3.20	—		$I_C = 45A$ See Fig. 2, 5
		—	2.54	—		$I_C = 24A, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/ $^\circ\text{C}$	$V_{CE} = V_{GE}, I_C = 250\mu A$
g_{fe}	Forward Transconductance ^④	23	35	—	S	$V_{CE} = 100V, I_C = 24A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 1200V$
		—	—	6500		$V_{GE} = 0V, V_{CE} = 1200V, T_J = 150^\circ\text{C}$
V_{FM}	Diode Forward Voltage Drop	—	2.5	3.5	V	$I_C = 16A$ See Fig. 13
		—	2.1	3.0		$I_C = 16A, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	160	250	nC	$I_C = 24A$ $V_{CC} = 400V$ See Fig. 8 $V_{GE} = 15V$
Q_{ge}	Gate - Emitter Charge (turn-on)	—	27	40		
Q_{gc}	Gate - Collector Charge (turn-on)	—	53	80		
$t_{d(on)}$	Turn-On Delay Time	—	47	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 24A, V_{CC} = 800V$ $V_{GE} = 15V, R_G = 5.0\Omega$ Energy losses include "tail" and diode reverse recovery. See Fig. 9, 10, 18
t_r	Rise Time	—	24	—		
$t_{d(off)}$	Turn-Off Delay Time	—	110	170		
t_f	Fall Time	—	180	260		
E_{on}	Turn-On Switching Loss	—	2.10	—	mJ	See Fig. 9, 10, 18
E_{off}	Turn-Off Switching Loss	—	1.50	—		
E_{ts}	Total Switching Loss	—	3.60	4.6		
$t_{d(on)}$	Turn-On Delay Time	—	46	—	ns	$T_J = 150^\circ\text{C}$, See Fig. 11, 18 $I_C = 24A, V_{CC} = 800V$ $V_{GE} = 15V, R_G = 5.0\Omega$ Energy losses include "tail" and diode reverse recovery.
t_r	Rise Time	—	27	—		
$t_{d(off)}$	Turn-Off Delay Time	—	240	—		
t_f	Fall Time	—	330	—		
E_{ts}	Total Switching Loss	—	6.38	—	mJ	
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3600	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ See Fig. 7 $f = 1.0MHz$
C_{oes}	Output Capacitance	—	160	—		
C_{res}	Reverse Transfer Capacitance	—	31	—		
t_{rr}	Diode Reverse Recovery Time	—	90	135	ns	$T_J = 25^\circ\text{C}$ See Fig. 14
		—	164	245		$T_J = 125^\circ\text{C}$
I_{rr}	Diode Peak Reverse Recovery Current	—	5.8	10	A	$T_J = 25^\circ\text{C}$ See Fig. 15
		—	8.3	15		$T_J = 125^\circ\text{C}$
Q_{rr}	Diode Reverse Recovery Charge	—	260	675	nC	$T_J = 25^\circ\text{C}$ See Fig. 16
		—	680	1838		$T_J = 125^\circ\text{C}$
$di_{(rec)}/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	120	—	A/ μs	$T_J = 25^\circ\text{C}$ See Fig. 17
		—	76	—		$T_J = 125^\circ\text{C}$

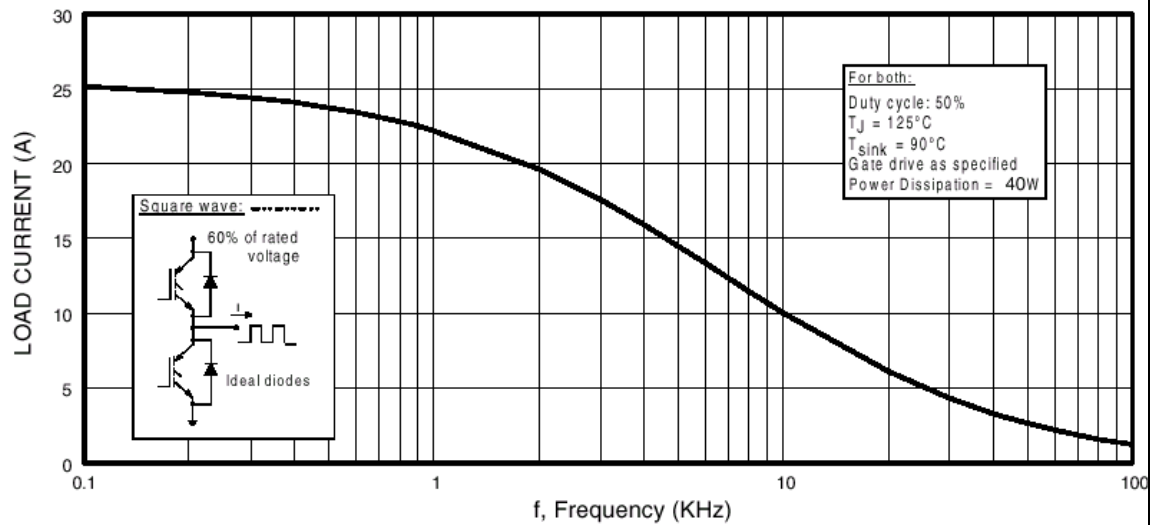


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

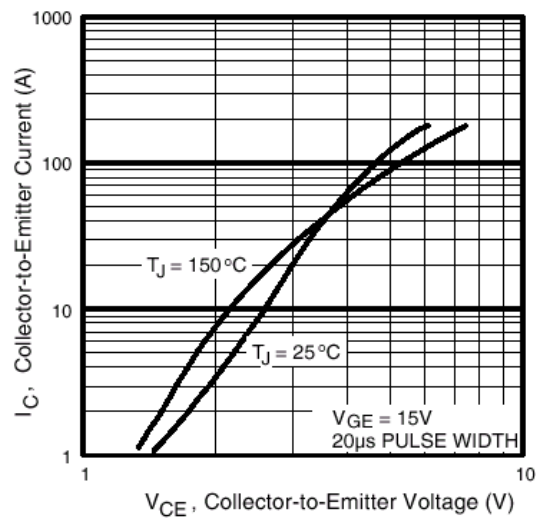


Fig. 2 - Typical Output Characteristics

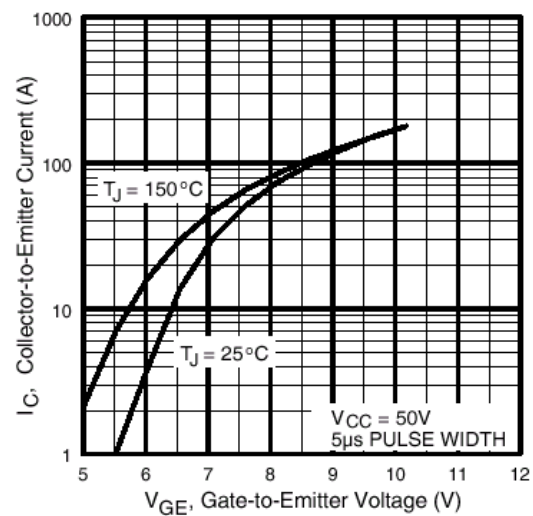


Fig. 3 - Typical Transfer Characteristics

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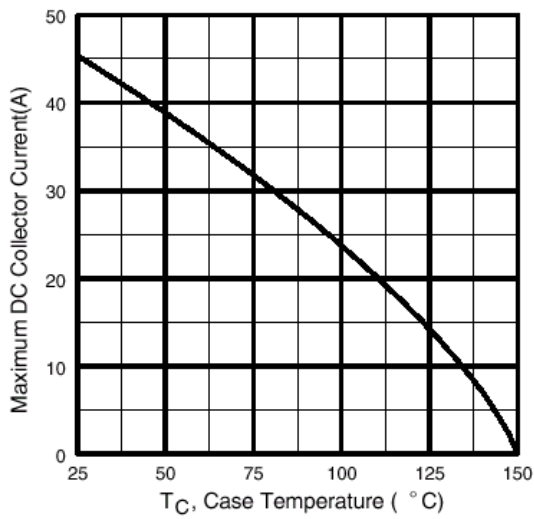


Fig. 4 - Maximum Collector Current vs. Case Temperature

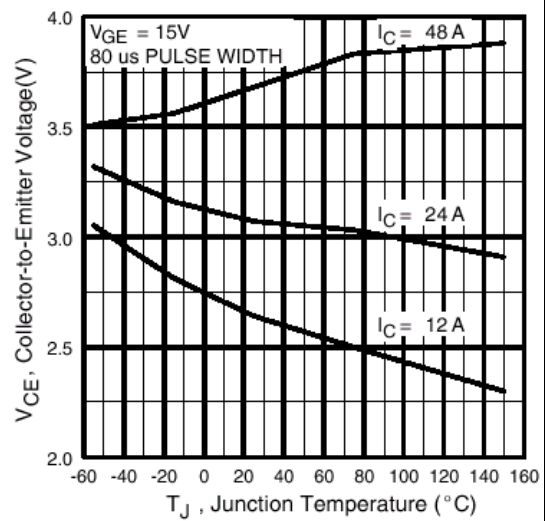


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

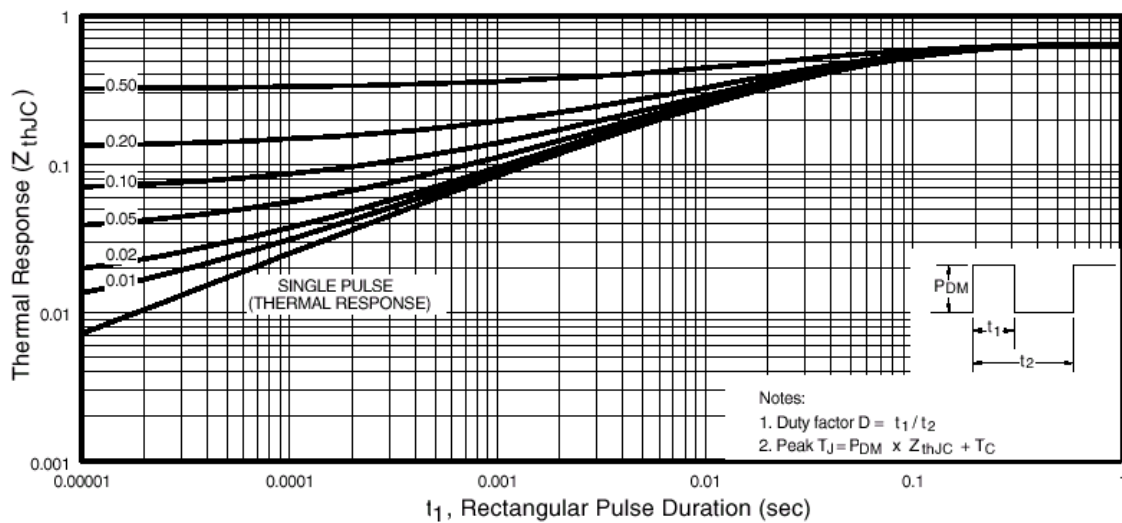


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

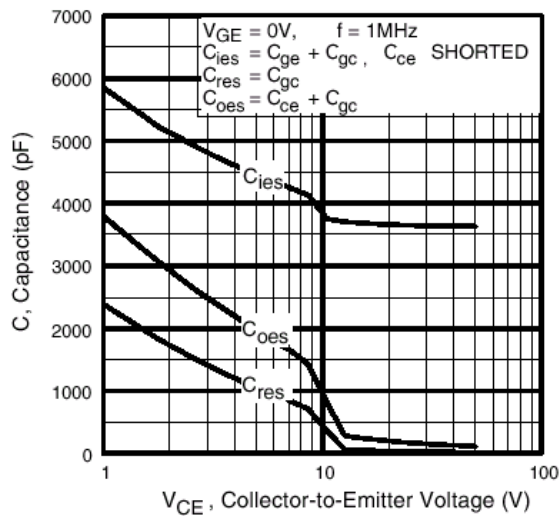


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

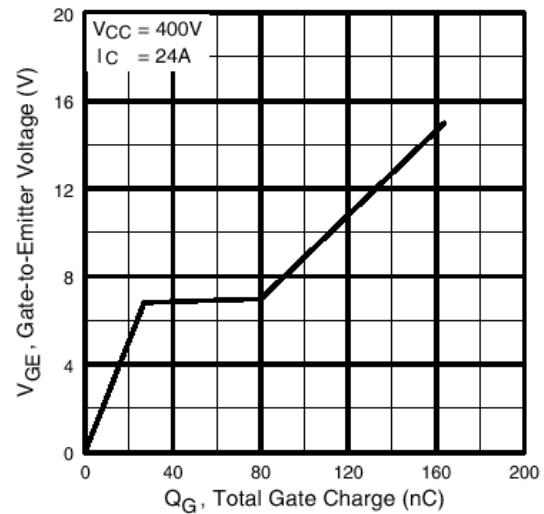


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

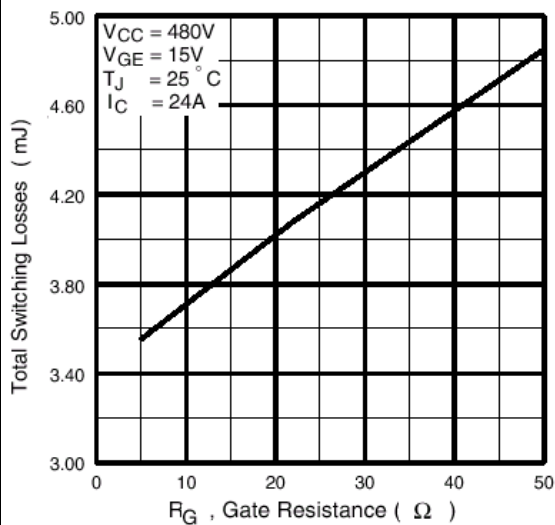


Fig. 9 - Typical Switching Losses vs. Gate Resistance

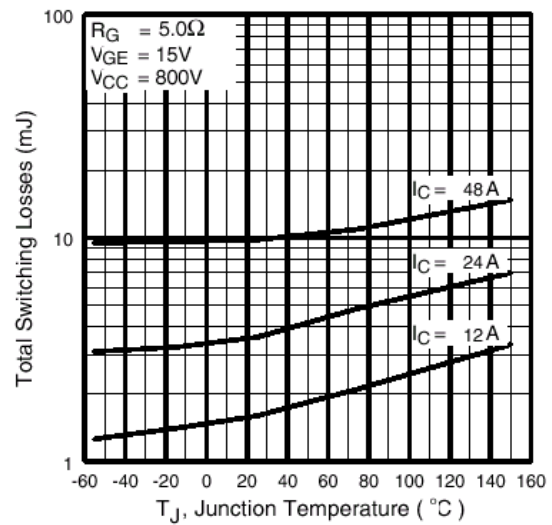


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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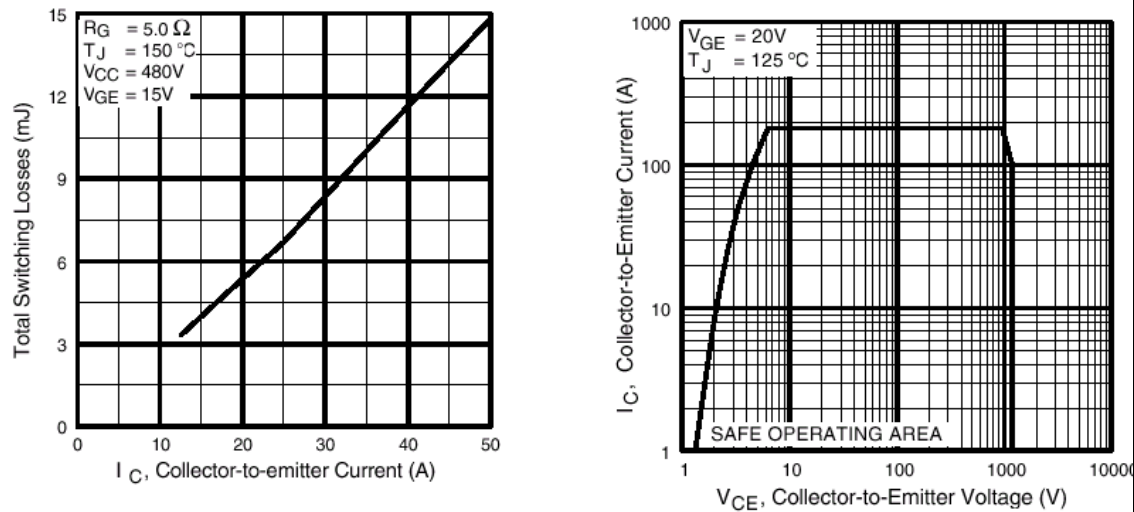


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

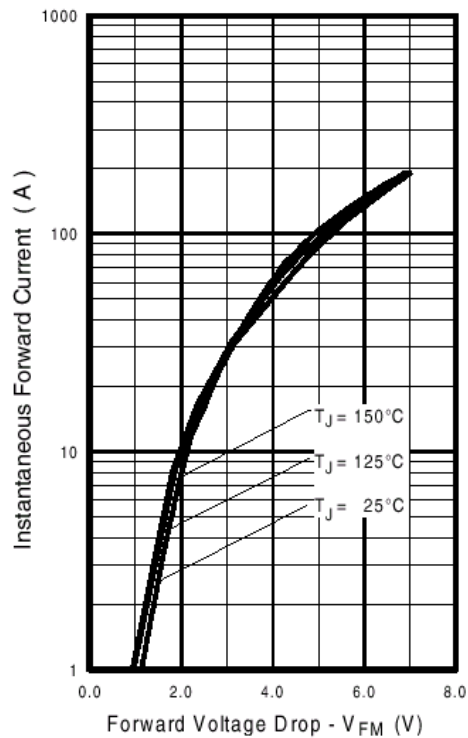


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

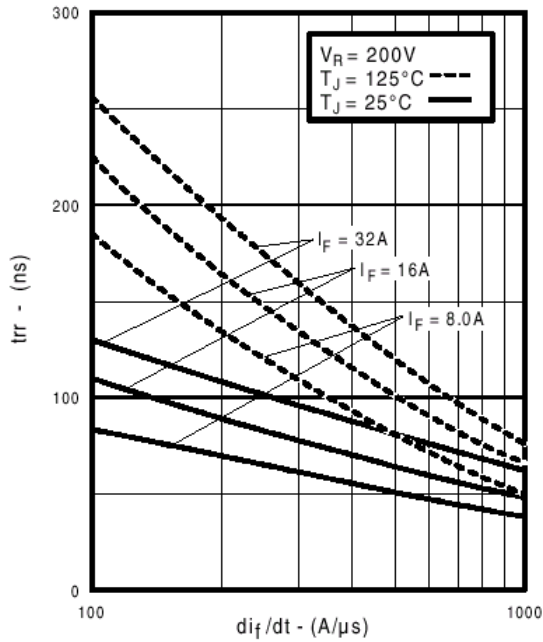


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

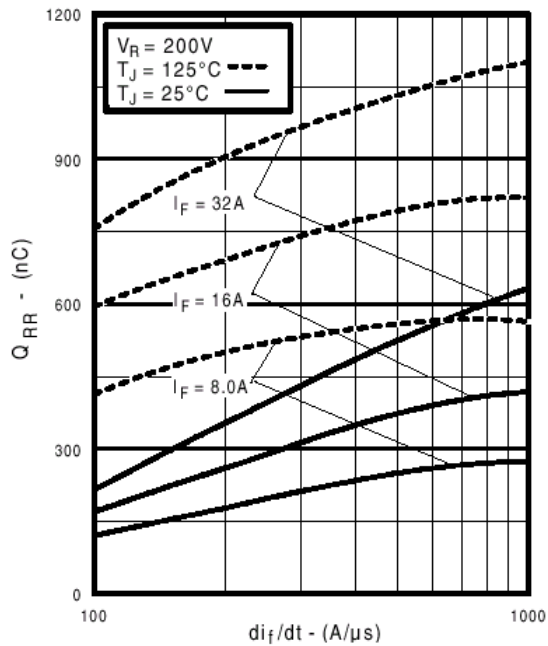


Fig. 16 - Typical Stored Charge vs. di_f/dt
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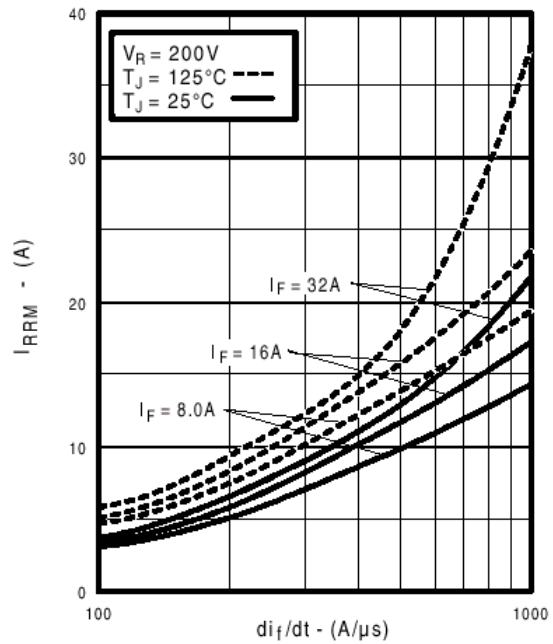


Fig. 15 - Typical Recovery Current vs. di_f/dt

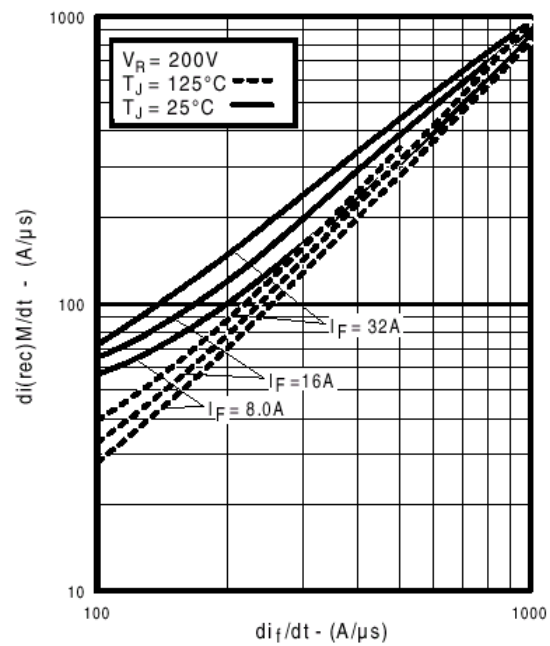


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

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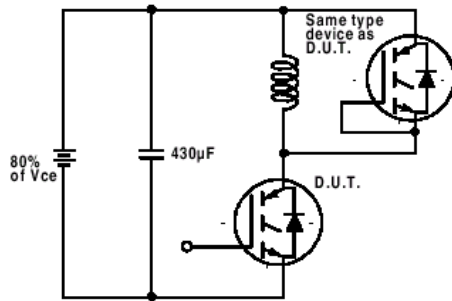


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

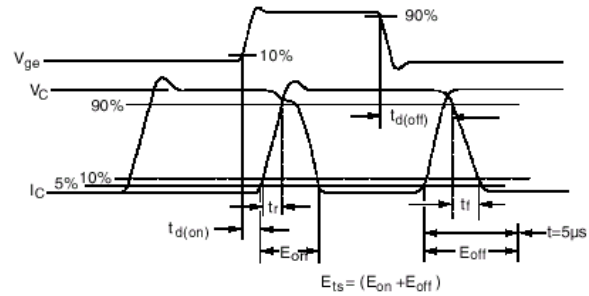


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

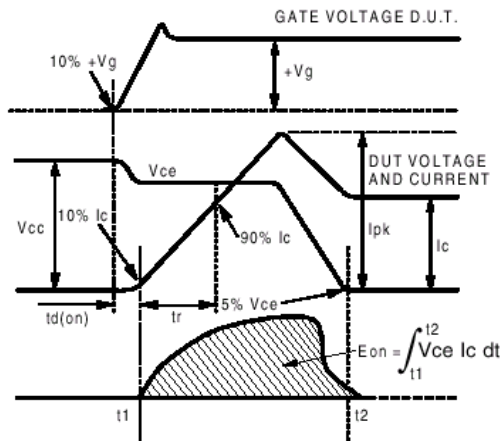


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

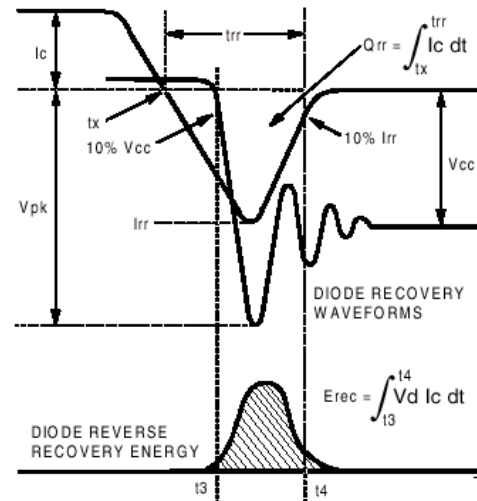


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

B. IXYS CORPORATION DSEI60

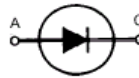


Fast Recovery Epitaxial Diode (FRED)

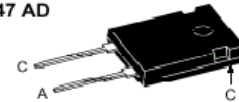
DSEI 60

$$\begin{aligned} I_{FAVM} &= 52 \text{ A} \\ V_{RRM} &= 1200 \text{ V} \\ t_{rr} &= 40 \text{ ns} \end{aligned}$$

V_{RSM} V	V_{RRM} V	Type
1200	1200	DSEI 60-12A



TO-247 AD



A = Anode, C = Cathode

Symbol	Test Conditions	Maximum Ratings	
I_{FRMS} I_{FAVM} ① I_{FRM}	$T_{VJ} = T_{VJM}$ $T_C = 60^\circ\text{C}$; rectangular, $d = 0.5$ $t_p < 10 \mu\text{s}$; rep. rating, pulse width limited by T_{VJM}	100 52 800	A A A
I_{FSM}	$T_{VJ} = 45^\circ\text{C}$; $t = 10 \text{ ms}$ (50 Hz), sine $t = 8.3 \text{ ms}$ (60 Hz), sine	500 540	A A
	$T_{VJ} = 150^\circ\text{C}$; $t = 10 \text{ ms}$ (50 Hz), sine $t = 8.3 \text{ ms}$ (60 Hz), sine	450 480	A A
P_t	$T_{VJ} = 45^\circ\text{C}$; $t = 10 \text{ ms}$ (50 Hz), sine $t = 8.3 \text{ ms}$ (60 Hz), sine	1250 1200	A ² s A ² s
	$T_{VJ} = 150^\circ\text{C}$; $t = 10 \text{ ms}$ (50 Hz), sine $t = 8.3 \text{ ms}$ (60 Hz), sine	1000 950	A ² s A ² s
T_{VJ} T_{VJM} T_{sig}		-40...+150 150 -40...+150	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$
P_{tot}	$T_C = 25^\circ\text{C}$	189	W
M_d	Mounting torque	0.8...1.2	Nm
Weight		6	g

Features

- International standard package JEDEC TO-247 AD
- Planar passivated chips
- Very short recovery time
- Extremely low switching losses
- Low I_{RM} -values
- Soft recovery behaviour
- Epoxy meets UL 94V-0

Applications

- Antiparallel diode for high frequency switching devices
- Anti saturation diode
- Snubber diode
- Free wheeling diode in converters and motor control circuits
- Rectifiers in switch mode power supplies (SMPS)
- Inductive heating and melting
- Uninterruptible power supplies (UPS)
- Ultrasonic cleaners and welders

Advantages

- High reliability circuit operation
- Low voltage peaks for reduced protection circuits
- Low noise switching
- Low losses
- Operating at lower temperature or space saving by reduced cooling

Symbol	Test Conditions	Characteristic Values	
		typ.	max.
I_R	$T_{VJ} = 25^\circ\text{C}$ $V_R = V_{RRM}$ $T_{VJ} = 25^\circ\text{C}$ $V_R = 0.8 \cdot V_{RRM}$ $T_{VJ} = 125^\circ\text{C}$ $V_R = 0.8 \cdot V_{RRM}$	2.2 0.5 14	mA mA mA
V_F	$I_F = 60 \text{ A}$; $T_{VJ} = 150^\circ\text{C}$ $T_{VJ} = 25^\circ\text{C}$	2.0 2.55	V V
V_{T0}	For power-loss calculations only	1.65	V
r_T	$T_{VJ} = T_{VJM}$	8.3	m Ω
R_{thJC} R_{thCK} R_{thJA}		0.66 35	K/W K/W K/W
t_{rr}	$I_F = 1 \text{ A}$; $-di/dt = 200 \text{ A}/\mu\text{s}$; $V_R = 30 \text{ V}$; $T_{VJ} = 25^\circ\text{C}$	40	ns
I_{RM}	$V_R = 540 \text{ V}$; $I_F = 60 \text{ A}$; $-di_F/dt = 480 \text{ A}/\mu\text{s}$ $L \leq 0.05 \mu\text{H}$; $T_{VJ} = 100^\circ\text{C}$	32	A

① I_{FAVM} rating includes reverse blocking losses at T_{VJM} , $V_R = 0.8 V_{RRM}$, duty cycle $d = 0.5$

Data according to IEC 60747

IXYS reserves the right to change limits, test conditions and dimensions

036

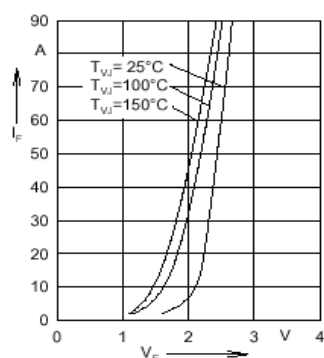


Fig. 1 Forward current versus voltage drop.

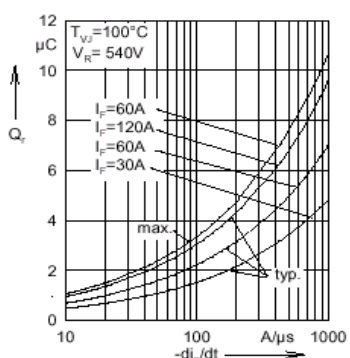


Fig. 2 Recovery charge versus $-di_F/dt$.

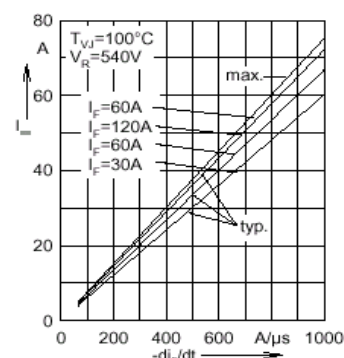


Fig. 3 Peak reverse current versus $-di_F/dt$.

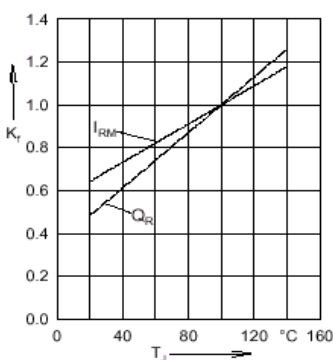


Fig. 4 Dynamic parameters versus junction temperature.

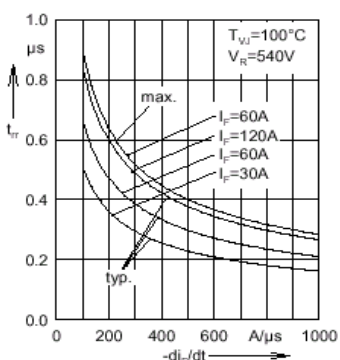


Fig. 5 Recovery time versus $-di_F/dt$.

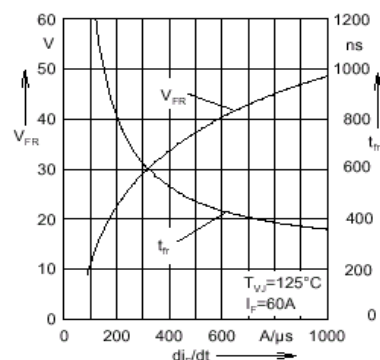


Fig. 6 Peak forward voltage versus di_F/dt .

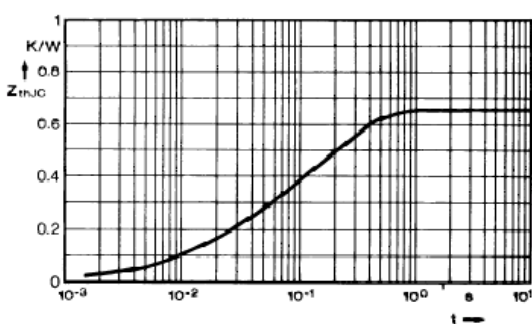
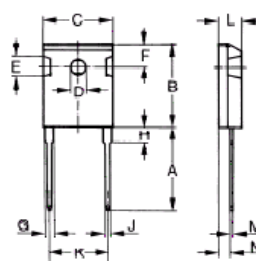


Fig. 7 Transient thermal impedance junction to case.

Dimensions



Dim.	Millimeter Min. Max.	Inches Min. Max.
A	19.81 20.32	0.780 0.800
B	20.80 21.46	0.819 0.845
C	15.75 16.26	0.610 0.640
D	3.55 3.65	0.140 0.144
E	4.32 5.49	0.170 0.216
F	5.4 6.2	0.212 0.244
G	1.65 2.13	0.065 0.084
H	- 4.5	- 0.177
J	1.0 1.4	0.040 0.055
K	10.8 11.0	0.426 0.433
L	4.7 5.3	0.185 0.209
M	0.4 0.8	0.016 0.031
N	2.2 2.54	0.087 0.102

C. MALLORY ELECTROLYTIC CAPACITORS

NACC Specification Sheet
For Reference Only



Part Number: CGH102T450V3L
Capacitance (μF): 1,000
Working Volts (WVDC): 450
Tolerance (±%): -10% +75%
Sleeve Material: Blue PVC

Product Type: CGH
Operating Temperature (°C): -40 to +85
Surge Volts (SVDC): 525
Thickness: .008"

Max ESR @ 120Hz - 25°C (MOhms): 83.4

Max ESR @ 20KHz - 25°C (MOhms): 53.4

Max Iac @ 120Hz - 85°C (RMS Amps): 4.8

Max Ripple @ 20KHz - 85°C (RMS Amps): 6.0

Max DC Leakage Current:

$I = .006 \sqrt{CV}$ after 5 Minutes

Not to exceed 6 mA

- C = Capacitance in μF
- V = Rated Voltage
- I = Leakage Current in mA

Dimensions		
	Millimeters	Inches
D		2.000
L		3.625
C		
E		

Performance Specifications

After application of rated DC voltage for 1000 hours at + 85°C.

- CAP ≤10 % from initial measurement
- DF ≤175 % from initial measurement
- DCL initial specified limits

Ripple Multipliers

The maximum ripple current at 85°C and 120 Hz is shown in the Stanard Rating Table.
Maximum ripple current may be adjusted by the multipliers in the following tables.

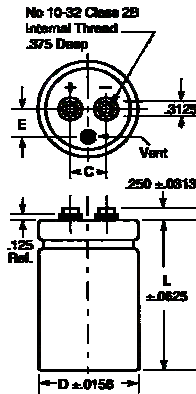
Rated WVDC	Ripple Multipliers				
	120Hz	400Hz	1KHz	2.5KHz	10KHz
250 to 500	1.000	1.080	1.113	1.175	1.230

Ambient Temp.	Ripple Multiplier	Ambient Temp.	Ripple Multiplier
+85°C	1.00	+55°C	2.00
+75°C	1.40	+45°C	2.25
+65°C	1.70	+35°C	2.45

NACC Specification Sheet
For Reference Only



Part Number:	CGS102T450R5L	Product Type:	CGS
Capacitance (μF):	1,000	Operating Temperature (°C):	-40 to +85
Working Volts (WVDC):	450	Surge Volts (SVDC):	525
Tolerance (±%):	-10% +75%(6.3 - 150 WVDC); -10% + 50%(200 - 500 WVDC)		
Sleeve Material:	Blue PVC	Thickness:	.008"



Max ESR @ 120 Hz - 25°C (Ohms): 0.103

Max Ripple @ 120 Hz - 85°C (RMS Amps): 4.0

Max DC Leakage Current:

$I = .006\sqrt{CV}$ after 30 Minutes
 Not to exceed 6 mA

- C = Capacitance in μF
- V = Rated Voltage
- I = Leakage Current in mA

Dimensions		
	Millimeters	Inches
D		1.375
L		5.625
C		
E		

Performance Specifications

After application of rated DC voltage for 1000 hours at + 85°C.

- CAP ≤10 % from initial measurement
- DF ≤175 % from initial measurement
- DCL initial specified limits

Ripple Multipliers

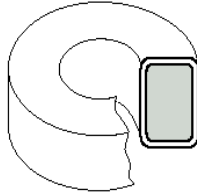
The maximum ripple current at 85°C and 120 Hz is shown in the Stanard Rating Table.
 Maximum ripple current may be adjusted by the multipliers in the following tables.

Rated WVDC	Ripple Multipliers				
	60Hz	120Hz	400Hz	1KHz	2.5KHz
3 to 50	.80	1.00	1.05	1.10	1.14
51 to 150	.80	1.00	1.08	1.13	1.16
151 & Up	.80	1.00	1.15	1.21	1.25

Ambient Temp.	Ripple Multiplier
+85°C	1.0
+75°C	1.4
+65°C	1.7
+55°C	2.0
+45°C	2.2

D. ARNOLD TOROIDAL CORES

o.d. 1.570
i.d. 0.950/ht. 0.570



CORNERS:
0.094 Approx.
Radius (Typical)

Dimensions

	Outside Diameter	Inside Diameter	Height
Before Coating Nominal	1.570 in 39.88 mm	0.950 in 24.13 mm	0.570 in 14.48 mm
After Coating (Blue Epoxy)	1.602 in Max. 40.69 mm Max.	0.918 in Min. 23.32 mm Min.	0.605 in Max. 15.37 mm Max.

Physical Specifications

Effective Cross Sectional Area of Magnetic Path, A_e (Reference)	Effective Magnetic Path Length, l_e (Reference)	Effective Core Volume, V_e (Reference)	Minimum Window Area (Reference)	Approximate Weight of Finished 125 μ MPP Core	Approximate Mean Length of Turn for Full Winding (Half of I.D. Remaining)
0.1662 in ² 1.072 cm ²	3.877 in 9.848 cm	0.6449 in ³ 10.5485 cm ³	0.6619 in ² 4.2702 cm ² 842,724 cmil	0.206 lbs 92 g	1.87 in 4.76 cm

Electrical Specifications

Nominal Permeability	Inductance Factor, mH +/- 8% for 1000 turns	Approximate Ratio of DC Resistance to Inductance for Full Winding (Half of I.D. Remaining), Ω /mH	Part Numbers		
			Molypermalloy	HI-FLUX	SUPER-MSS
14 μ	19	0.24	A-086019-2	HF-157014-2	—
26 μ	35	0.13	A-085035-2	HF-157026-2	MS-157026-2
60 μ	81	0.060	A-083081-2	HF-157060-2	MS-157060-2
75 μ	101	0.045	—	—	MS-157075-2
90 μ	121	0.038	—	—	MS-157090-2
125 μ	168	0.027	A-254168-2	HF-157125-2	MS-157125-2
147 μ	198	0.023	A-151198-2	HF-157147-2	—
160 μ	215	0.021	A-306215-2	HF-157160-2	—
173 μ	233	0.019	A-179233-2	—	—
205 μ	276	0.016	A-214276-2	—	—

Heavy Film Magnet Wire Winding Data (Approximate)

AWG	Full Winding (Half of I.D. Remaining)			Single Layer Winding		
	Turns	R_{dc} Ω		Turns	R_{dc} Ω	l_w ft.
10	—	—		22	0.00389	3.89
11	—	—		25	0.00545	4.32
12	65	0.01803		28	0.00762	4.80
13	81	0.0281		31	0.0107	5.33
14	101	0.0438		35	0.0148	5.88
15	126	0.0683		40	0.0208	6.55
16	158	0.1071		45	0.0292	7.27
17	197	0.1662		50	0.0408	8.08
18	247	0.260		57	0.0574	8.98
19	307	0.406		64	0.0804	9.99
20	383	0.632		71	0.112	11.1
21	477	0.986		80	0.158	12.4
22	597	1.557		90	0.223	13.8
23	739	2.40		100	0.309	15.2
24	921	3.77		112	0.435	16.9
25	1145	5.88		125	0.611	18.9
26	1429	9.26		140	0.862	21.0
27	1767	14.31		155	1.20	23.3

E. TOSHIBA TLP250 OPTICAL ISOLATOR

SEMICONDUCTOR TOSHIBA TECHNICAL DATA

TOSHIBA PHOTOCOUPLER TLP250 GaAs IRED & PHOTO-IC

(TLP250)

TRANSISTOR INVERTER
INVERTER FOR AIR CONDITIONER
IGBT GATE DRIVE
POWER MOS FET GATE DRIVE

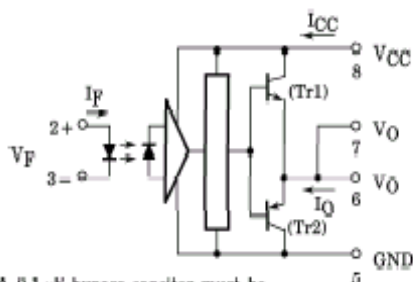
The Toshiba TLP250 consists of a GaAs light emitting diode and a integrated photodetector.
This unit is 8-lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input Threshold Current : $I_F = 5\text{mA}$ (Max.)
- Supply Current (I_{CC}) : 11mA (Max.)
- Supply Voltage (V_{CC}) : $10\text{--}35\text{V}$
- Output Current (I_O) : $\pm 0.5\text{A}$ (Min.)
- Switching Time (t_{pLH}/t_{pHL}) : $0.5\mu\text{s}$ (Max.)
- Isolation Voltage : 2500V_{rms} (Min.)
- UL Recognized : UL1577, File No.E67349
- Option (D4) type
VDE Approved : DIN VDE0884/08.92, Certificate No.76829
Maximum Operating Insulation Voltage : 630V_{pk}
Highest Permissible Over Voltage : 4000V_{pk}

(Note) When a VDE0884 approved type is needed,
please designate the "Option (D4)"

- Creepage Distance : 6.4mm (Min.)
- Clearance : 6.4mm (Min.)

SCHEMATIC

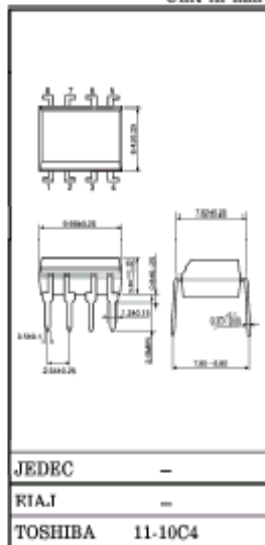


A $0.1\mu\text{F}$ bypass capacitor must be connected between pin 8 and 5 (See more 5).

TRUTH TABLE

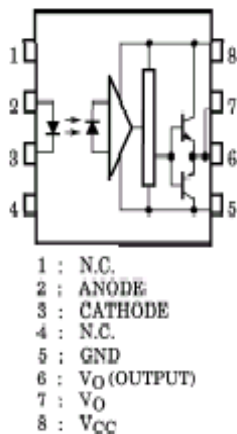
	Tr1	Tr2
Input LED ON	ON	OFF
Input LED OFF	OFF	ON

Unit in mm



Weight : 0.54g

PIN CONFIGURATION (TOP VIEW)



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①

TLP250 - 1
1996 - 4 - 8
TOSHIBA CORPORATION

(TLP250)

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	I _F	20	mA
	Forward Current Derating (Ta ≥ 70°C)	ΔI _F / ΔTa	-0.36	mA / °C
	Peak Transient Forward Current (Note 1)	I _{FPT}	1	A
	Reverse Voltage	V _R	5	V
	Junction Temperature	(T _j)	125	°C
DETECTOR	"H" Peak Output Current (P _W ≤ 2.5μs, f ≤ 15kHz)(Note 2)	I _{OPH}	-1.5	A
	"L" Peak Output Current (P _W ≤ 2.5μs, f ≤ 15kHz)(Note 2)	I _{OPL}	+1.5	A
	Output Voltage	V _O	35	V
			24	
	Supply Voltage	V _{CC}	35	V
			24	
	Output Voltage Derating (Ta ≥ 70°C)	ΔV _O / ΔTa	-0.73	V / °C
	Supply Voltage Derating (Ta ≥ 70°C)	ΔV _{CC} / ΔTa	-0.73	V / °C
	Junction Temperature	(T _j)	125	°C
Operating Frequency (Note 3)		f	25	kHz
Operating Temperature Range		T _{opr}	-20~70	°C
Storage Temperature Range		T _{stg}	-55~125	°C
Lead Solder Temperature (10s)		T _{sol}	260	°C
Isolation Voltage (AC, 1min., R.H. ≤ 60%, Ta = 25°C) (Note 4)		BV _g	2500	Vrms

Note 1 : Pulse width P_W ≤ 1μs, 300pps

Note 2 : Exponential Waveform

Note 3 : Exponential Waveform, I_{OPH} ≤ -1.0A (≤ 2.5μs), I_{OPL} ≤ +1.0A (≤ 2.5μs)

Note 4 : Device considered a two terminal device : pins 1,2,3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 5 : A ceramic capacitor (0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current, ON	I _F (ON)	7	8	10	mA
Input Voltage, OFF	V _F (OFF)	0	—	0.8	V
Supply Voltage	V _{CC}	15	—	30 20	V
Peak Output Current	I _{OPH} / I _{OPL}	—	—	±0.5	A
Operating Temperature	T _{opr}	-20	25	70 85	°C

TLP250-2
199b-4-8
TOSHIBA CORPORATION

(TLP250)

ELECTRICAL CHARACTERISTICS (Ta = -20~70°C, Unless otherwise specified)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.*	MAX.	UNIT
Input Forward Voltage		V _F	—	I _F = 10mA, T _a = 25°C			1.6	1.8	V
Temperature Coefficient of Forward Voltage		ΔV _F / ΔT _a	—	I _F = 10mA		—	−2.0	—	mV / °C
Input Reverse Current		I _R	—	V _R = 5V, T _a = 25°C			—	10	μA
Input Capacitance		C _T	—	V = 0, f = 1MHz, T _a = 25°C		—	45	250	pF
Output Current	"H" Level	I _{OPH}	3	V _{CC} = 30V (*1)	I _F = 10mA V _{GS} = 4V	−0.5	−1.5	—	A
	"L" Level	I _{OPL}	2		I _F = 0 V _{GS} = 2.5V	0.5	2	—	
Output Voltage	"H" Level	V _{OH}	4	V _{CC1} = +15V, V _{EE1} = −15V R _L = 200Ω, I _F = 5mA		11	12.8	—	V
	"L" Level	V _{OL}	5	V _{CC1} = +15V, V _{EE1} = −15V R _L = 200Ω, V _F = 0.8V		—	−14.3	−12.5	
Supply Current	"H" Level	I _{CCH}	—	V _{CC} = 30V, I _F = 10mA T _a = 25°C		—	7	—	mA
			—	V _{CC} = 30V, I _F = 10mA		—	—	11	
	"L" Level	I _{CCL}	—	V _{CC} = 30V, I _F = 0mA T _a = 25°C		—	7.5	—	
			—	V _{CC} = 30V, I _F = 0mA		—	—	11	
Threshold Input Current	"Output L→H"	I _{FLH}	—	V _{CC1} = +15V, V _{EE1} = −15V R _L = 200Ω, V _O > 0V		—	1.2	5	mA
Threshold Input Voltage	"Output H→L"	V _{FHL}		V _{CC1} = +15V, V _{EE1} = −15V R _L = 200Ω, V _O < 0V		0.8	—	—	V
Supply Voltage		V _{CC}	—			10	—	35	V
Capacitance (Input-Output)		C _S	—	V _S = 0, f = 1MHz T _a = 25°C		—	1.0	2.0	pF
Resistance (Input-Output)		R _S	—	V _S = 500V, T _a = 25°C R.H. ≤ 60%		5 × 10 ¹³	10 ¹⁴	—	Ω

* All typical values are at Ta = 25°C (*) : Duration of I_O time ≤ 50μs

TLP250-3

1996-4-8

TOSHIBA CORPORATION

(TLP250)

SWITCHING CHARACTERISTICS (Ta = -20~70°C, Unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT
Propagation Delay Time	L→H	t _{PLH}	I _F = 8mA V _{CC1} = +15V, V _{EE1} = -15V R _L = 200Ω	—	0.15	0.5	μs
	H→L	t _{PHL}		—	0.15	0.5	
Output Rise Time	t _r			—	—	—	
Output Fall Time	t _f			—	—	—	
Common Mode Transient Immunity at High Level Output	C _{MH}	7	V _{CM} = 600V, I _F = 8mA V _{CC} = 30V, Ta = 25°C	-5000	—	—	V / μs
Common Mode Transient Immunity at Low Level Output	C _{ML}	7	V _{CM} = 600V, I _F = 0mA V _{CC} = 30V, Ta = 25°C	5000	—	—	V / μs

* All typical values are at Ta=25°C

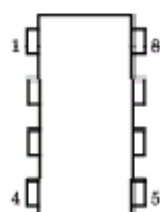
TLP250-4

1996-4-8

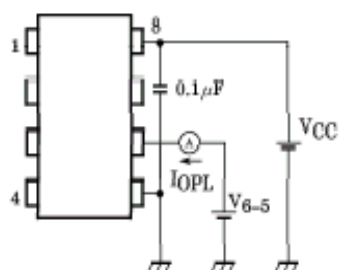
TOSHIBA CORPORATION

(TLP250)

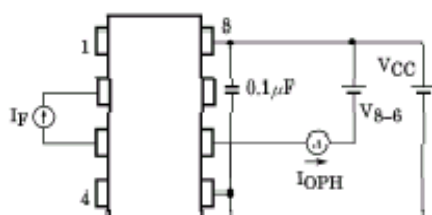
TEST CIRCUIT 1 :



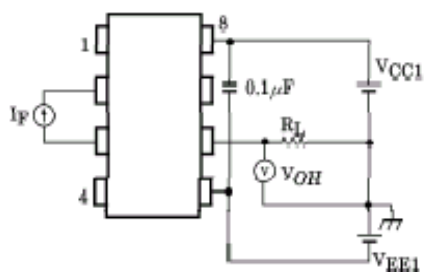
TEST CIRCUIT 2 : IOPL



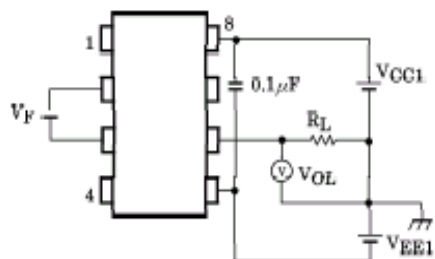
TEST CIRCUIT 3 : IOPH



TEST CIRCUIT 4 : VOH



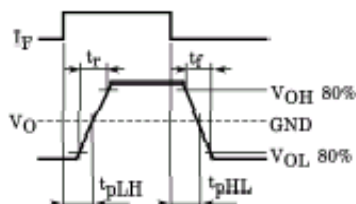
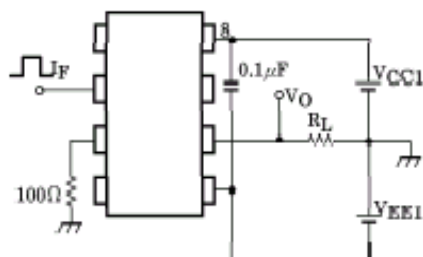
TEST CIRCUIT 5 : VOL



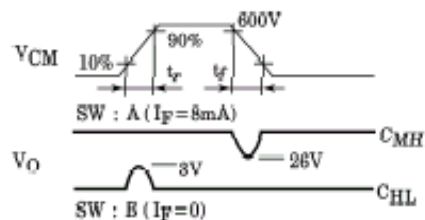
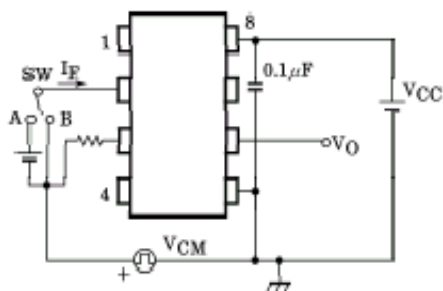
TLP250 - 5
199b - 4 - 8
TOSHIBA CORPORATION

(TLP250)

TEST CIRCUIT 6 : t_{pLH} , t_{pHL} , t_r , t_f



TEST CIRCUIT 7 : C_{MH} , C_{ML}

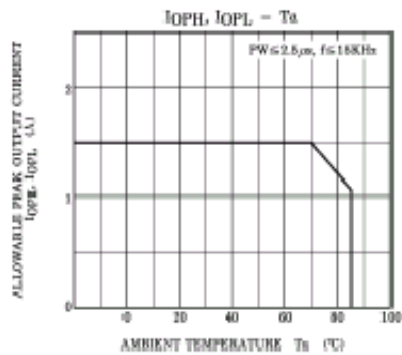
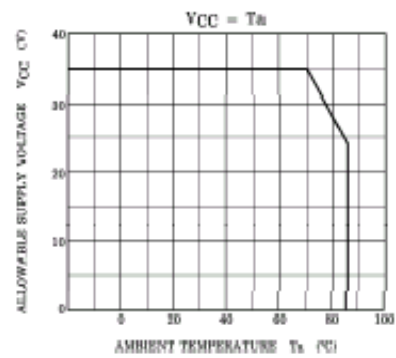
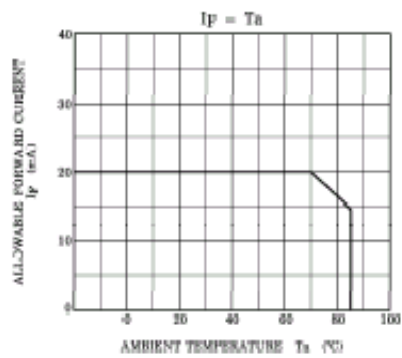
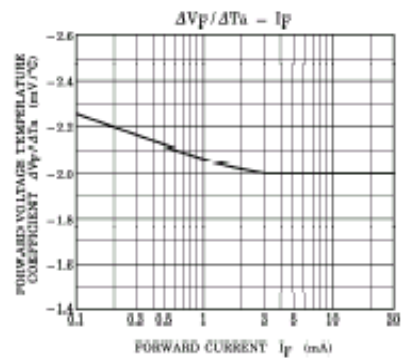
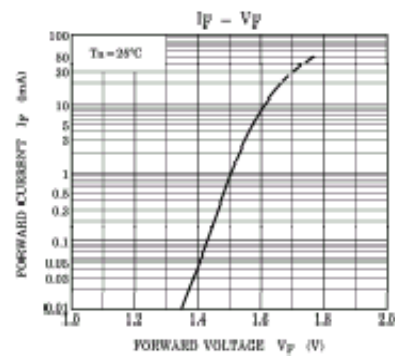


$$C_{ML} = \frac{480(V)}{t_r(\mu s)}$$

$$C_{MH} = \frac{480(V)}{t_f(\mu s)}$$

C_{ML} (C_{MH}) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

(TLP250)



TLP250-7*
199b-4-8
TOSHIBA CORPORATION

APPENDIX B. PSPICE NETLIST FILES

A. IRG4PH50UD NETLIST

```
.SUBCKT irg4ph50ud 1 2 3
*****
*   Model Generated by MODPEX   *
*Copyright(c) Symmetry Design Systems*
*   All Rights Reserved   *
* UNPUBLISHED LICENSED SOFTWARE *
* Contains Proprietary Information *
* Which is The Property of   *
* SYMMETRY OR ITS LICENSORS   *
*Commercial Use or Resale Restricted *
* by Symmetry License Agreement *
*****
*Model generated on Dec 2, 97
* MODEL FORMAT: SPICE3
*Symmetry IGBT Model (Version 1.0)
*External Node Designations
*Node 1 -> C
*Node 2 -> G
*Node 3 -> E
M1 9 6 8 8 MSUB L=100u W=100u
* Default values used in MSUB:
* The voltage-dependent capacitances are
* not included. Other default values are:
* RD=0 RS=0 LD=0 CBD=0 CBS=0 CGBO=0
.MODEL MSUB NMOS LEVEL=1
+VTO=4 KP=0.5 LAMBDA=0 CGSO=3.65971e-05
RD 7 9 0.001
RS 4 8 0.001
D1 3 1 d4ph50u
.MODEL d4ph50u d
+IS=3.82367e-11 RS=0.105288 N=2 EG=1.19013
+XTI=0.5 BV=1200 IBV=0.00025 CJO=1e-11
+VJ=0.7 M=0.5 FC=0.5 TT=1e-09
+KF=0 AF=1
Q1 4 7 1 QSUB OFF
.MODEL QSUB PNP
+IS=1e-16 BF=10 NF=1 VAF=100
+IKF=1000 ISE=1e-11 NE=2 BR=1
+NR=1 VAR=100 IKR=1000 ISC=1e-11
+NC=2 RB=0.1 IRB=1000 RBM=0.01
+RE=0.001 RC=0.001 XTB=0 XTI=3
+EG=1.16989 CJC=3.64714e-09 VJC=0.878241 MJC=0.9
```

```

+CJE=7.29428e-08 VJE=0.4 MJE=0.9 TF=3.04597e-11
RDS 7 4 1e8
RER 4 3 0.01
RG 6 2 6.18923
RL 10 11 1
D2 12 11 DCAP
* Default values used in DCAP:
* RS=0 EG=1.11 XTI=3.0 TT=0
* BV=infinite IBV=1mA
.MODEL DCAP D IS=1e-32 N=50
+CJO=5.60567e-09 VJ=0.4 M=0.9 FC=0.5
D3 0 11 DL
* Default values used in DL:
* EG=1.11 XTI=3.0 TT=0 CJO=0
* RS=0 BV=infinite IBV=1mA
.MODEL DL D IS=1e-10 N=0.4
VFI2 12 0 0
FI2 6 7 VFI2 -1
EV 10 0 7 6 1
CAP 10 13 6.81948e-09
RCAP 10 14 1
D4 0 14 DL
VFI1 13 14 0
FI1 6 7 VFI1 -1
.ENDS irg4ph50ud

```

APPENDIX C. THERMAL ANALYSIS

A. POWER SEMICONDUCTOR THERMODYNAMICS

From the PSPICE simulation in Chapter III, it was estimated that the resonant converter efficiency was 98.4 percent. With the output power equal to 8000 watts, the converter has a power loss of approximately 130 watts. In the simulation the inductors and capacitors were treated as ideal components, so all of the losses are due to the power semiconductors. From the test results in Chapter IV and the optimization documented in Chapter V, the majority of the power loss is confirmed to be in the main and auxiliary switches. Diodes D_1 and D_2 have insignificant heat dissipation and, in the worst case, D_m only dissipates 12 watts. For the thermal analysis it will be assumed that the combined dissipation of D_1 , D_2 and D_m is 15 watts leaving the remaining 115 watts for the main and auxiliary switches. A thermodynamic model will be used to estimate the required size of the heat sink to keep the steady-state and transient junction temperature of the IGBTs less than the maximum ratings.

1. Steady-State Analysis

To solve this thermodynamic problem, the familiar series electrical circuit equivalent will be used. Knowing the maximum junction temperature (T_j) allowed and the thermal resistances of the junction-to-case ($R_{\theta_{jc}}$) and case-to-sink ($R_{\theta_{cs}}$), the maximum sink-to-ambient ($R_{\theta_{sa}}$) resistance can be calculated. The thermal resistance has units of degrees Celsius per watt ($^{\circ}\text{C}/\text{W}$), so all temperatures used will be in Celsius. In all cases it will be assumed that the ambient temperature T_a is 25 $^{\circ}\text{C}$. This is not always a good assumption, as a typical converter will operate in an equipment rack where the ambient temperature could reach 40 $^{\circ}\text{C}$. Figure (C-1) shows a cut away view of the IGBT and heat sink.

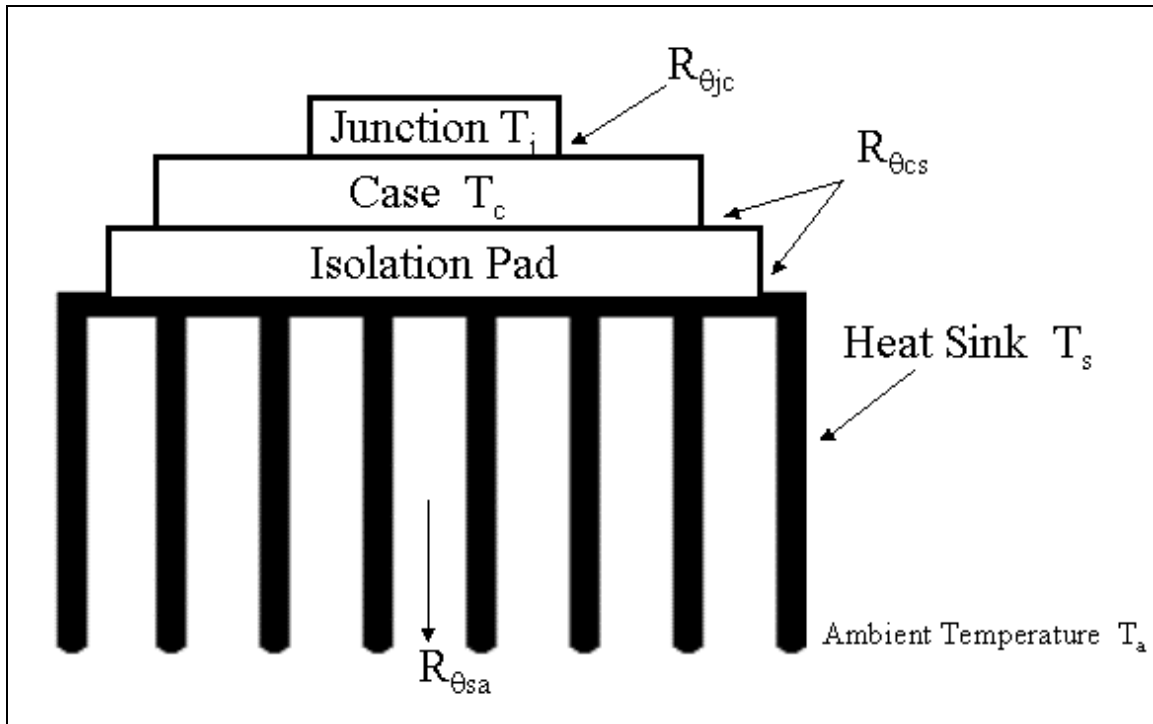


Figure C-1. Cut Away View of IGBT and Heat Sink.

Using Figure (C-1), an equivalent series resistive circuit is developed and shown in Figure (C-2).

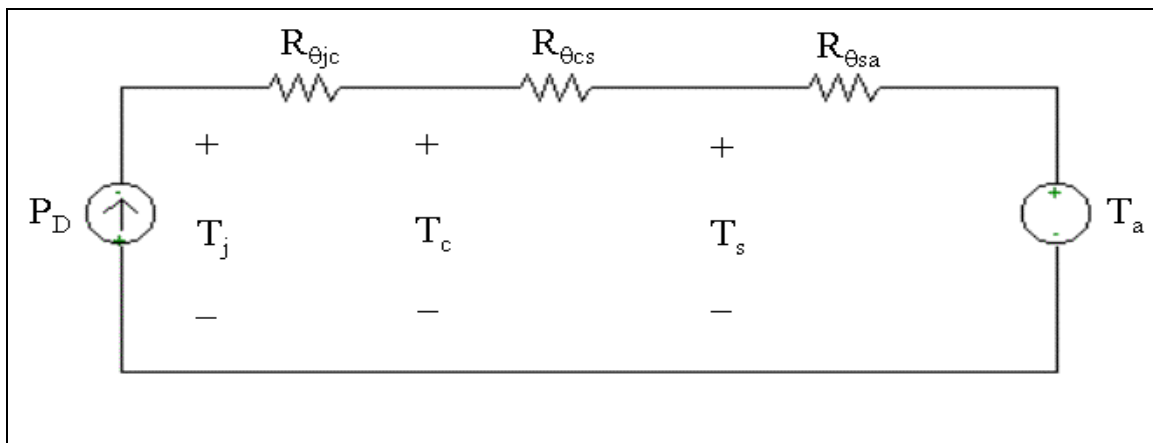


Figure C-2. Equivalent Circuit Based on Thermal Resistances.

Using Figure (C-2), Equation (C-1) can be written.

$$T_j = T_a + P_D (R_{\theta_{jc}} + R_{\theta_{cs}} + R_{\theta_{sa}}) \quad (C-1)$$

The thermal resistances and maximum junction temperature are obtained from the IRG4PH50UD data sheet in Appendix A and are listed in Table (C-1).

Parameter	Maximum Value
Junction Temperature T_j	150°C
Junction-to-Case	0.64 °C/W
Case-to-Sink	0.24 °C/W

Table C-1. Thermal Parameters for IRG4PH50UD IGBT.

If the parameters from Table (C-1) are used along with the known power dissipation and ambient temperature, the maximum $R_{\theta_{sa}}$ can be found by rearranging Equation (C-1).

$$R_{\theta_{sa}} \leq \frac{T_j - T_a}{P_D} - (R_{\theta_{jc}} + R_{\theta_{cs}}) \leq 0.207 \frac{^{\circ}\text{C}}{\text{W}} \quad (C-2)$$

This is quite a low value of thermal resistance and will be difficult to obtain with a reasonable-sized heat sink. Since the IGBT is not conducting continuously, the maximum $R_{\theta_{sa}}$ will be slightly higher using transient thermal analysis.

2. Transient Thermal Analysis

From Chapter III, it is known that the specified duty cycle D is 80 percent and, therefore, Equation (C-1) must be modified for periodic pulses. Since the heat is produced in the junction, the junction-to-case thermal resistance is modified with a factor, $r(t)$, known as the normalized thermal resistance [24]. Equation (C-1) becomes:

$$T_j = T_a + r(t)P_D (R_{\theta_{jc}} + R_{\theta_{cs}} + R_{\theta_{sa}}). \quad (C-3)$$

The factor $r(t)$ is usually read from a data sheet curve and the values are based on the duty cycle and pulse width. The normalized thermal resistance curves for the IRG4PH50UD are shown in Figure (C-3).

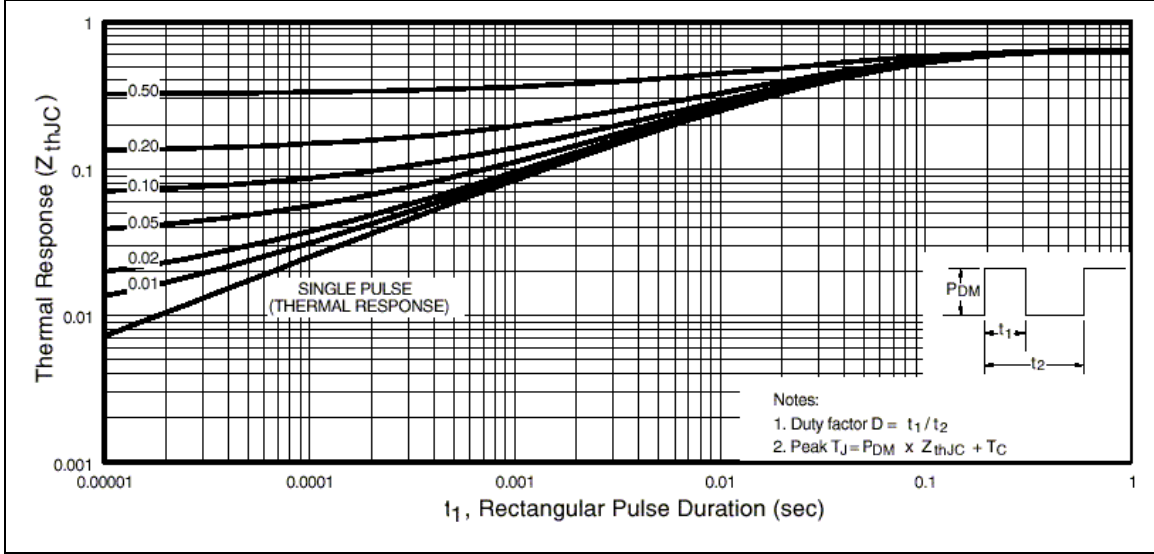


Figure C-3. Normalized Transient Thermal Impedance (from ref. [33]).

With $f_s = 20$ kHz and $D = 0.8$,

$$r(t) \approx 0.83. \quad (C-4)$$

Notice that Figure (C-3) does not have a $D = 0.8$ curve, so the $D = 0.2$ curve is used and subtracted from unity. Using the value for $r(t)$, a new maximum sink-to-air thermal resistance is found.

$$R_{\theta_{sa}} \leq \frac{T_j - T_a}{r(t)P_D} - (R_{\theta_{jc}} + R_{\theta_{cs}}) \leq 0.43 \frac{^{\circ}\text{C}}{\text{W}} \quad (C-5)$$

Next, a heat sink that is already available is analyzed to see if $R_{\theta_{sa}}$ meets the minimum requirements.

3. Estimation of Sink-to-Air Thermal Resistance

Calculating the thermal resistance of an aluminum heat sink is difficult and adding the effects of forced-air cooling makes the problem even harder. To come up with a quick solution, a windows-based program developed by AAVID Thermal Products Inc., a well-known heat sink manufacturer, was used [34]. The program, CoolCat™, allows the designer to enter the dimensions of the heat sink, flow rate, junction resistances and power dissipated. Using the entered data, the program plots performance curves including temperature drop and thermal resistance versus volumetric airflow.

In this design, the power module is approximately 9-inches long and 4-inches wide. The available heat sinks in the power research lab are 4-inches wide and 2.5-inches high with fifteen fins. For reasons discussed in Chapter IV, the heat sink was cut into sections for isolation and the IGBT section is only 3-inches long. A 125 CFM muffin fan is mounted on the end of the power module, but because of the heat sink height, approximately 50 percent of the air flows through the fins and the rest flows across the top of the power module to cool the resonant inductor. The estimated volumetric flow rate must be combined with the cross-sectional area of the heat sink to come up with linear airflow in units of feet per minute. Linear airflow is used in all of the forced convection curves.

$$LAF\left(\frac{\text{ft}}{\text{min}}\right)=125\frac{\text{ft}^3}{\text{min}}\times\frac{1}{10\text{in}^2}\times\frac{144\text{in}^2}{1\text{ft}^2}=1800\frac{\text{ft}}{\text{min}} \quad (\text{C-6})$$

Since 50 percent of the flow crosses through the heat sink,

$$LAF\left(\frac{\text{ft}}{\text{min}}\right)=900\frac{\text{ft}}{\text{min}}. \quad (\text{C-7})$$

For the 4-inch wide by 3-inch long by 2.5-inch tall heat sink, Figures (C-4) and (C-5) were obtained using the CoolCat program.

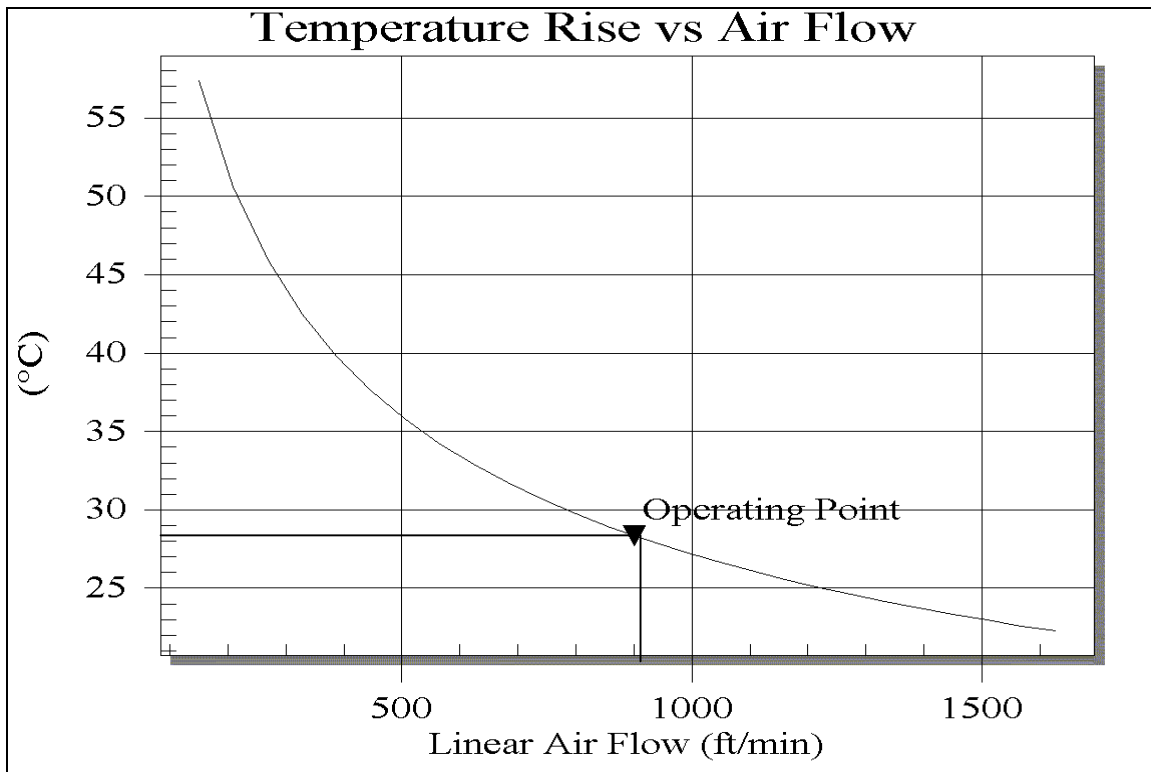


Figure C-4. Heat Sink Temperature Rise Versus Linear Air Flow.

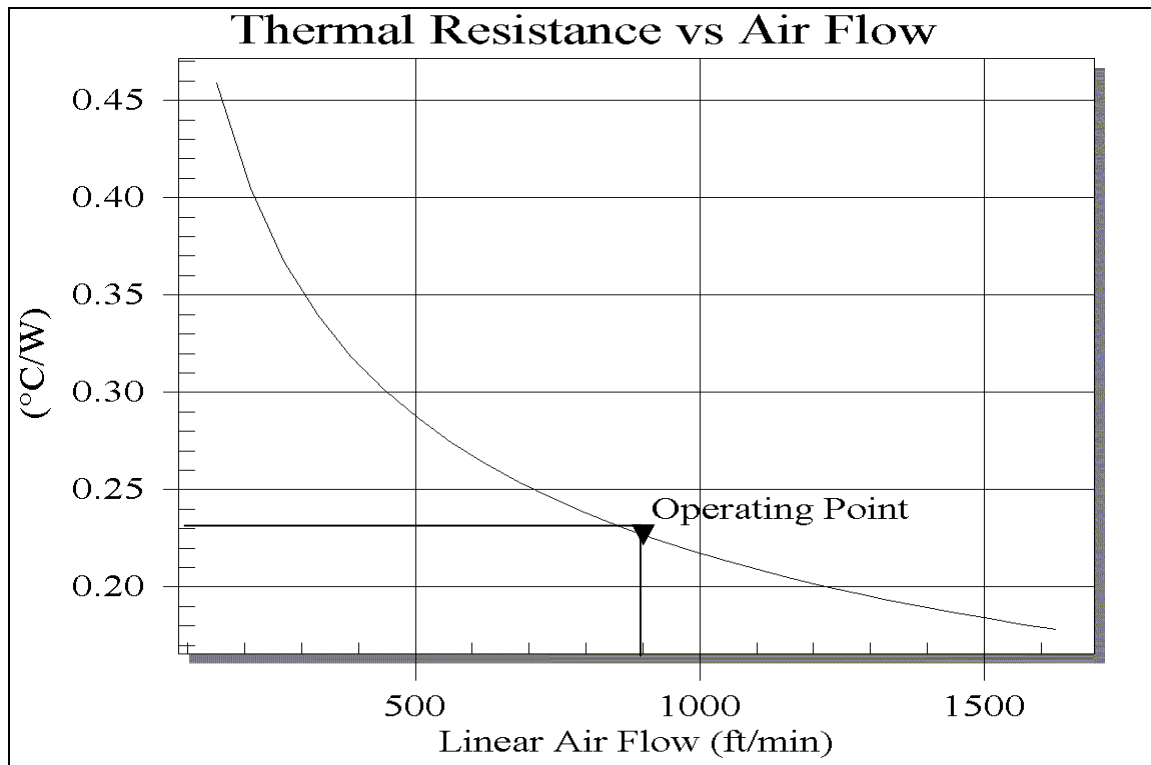


Figure C-5. Heat Sink Thermal Resistance Versus Linear Air Flow.

Based on Figures (C-4) and (C-5), with a linear airflow of 900 ft/min the temperature rise across the heat sink is 28°C with a thermal resistance equal to 0.225 °C/W. The thermal resistance $R_{\theta_{sa}}$ is less than the maximum transient values given in Equation (C-6). Now that a value for $R_{\theta_{sa}}$ is known, Equation (C-3) is used to find the junction temperature T_j .

$$T_j = T_a + r(t)P_D (R_{\theta_{jc}} + R_{\theta_{cs}} + R_{\theta_{sa}}) = 130^\circ\text{C} \quad (\text{C-8})$$

This amount of junction temperature is quite high and a better heat sink combination is needed before this converter could operate in a typical environment. The limiting factor is the junction-to-case thermal resistance and this analysis shows that this design is operating close to the power limits of the IRG4PH50UD. The TO-247 case has a small thermal footprint and is not efficient at transferring heat away from the junction. As a comparison, the Semikron SKM 100GB 124D used in the hard-switched converter [5] has a 1.25-inch by 3.5-inch footprint and a significantly reduced $R_{\theta_{jc}}$ equal to 0.18 °C/W. Operating semiconductors at temperatures close to the maximum rating greatly reduces the device's lifespan [6]. The current tail in IGBTs also increases in size at higher temperatures, which then increases switching losses thus raising the IGBT temperature further [17].

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APPENDIX D. CONTROL INTERFACE AND DRIVER DESIGN

A. CONTROL INTERFACE CIRCUIT

In Appendix D, the design of the control interface and driver boards is described. Recently, a hard-switched buck converter was designed and built for the ESAC test bed to be located at the University of Missouri at Rolla [5]. During the design process, a robust analog control and protection circuit was designed. Significant time was spent analyzing the control and protection system to ensure proper operation through out the full range of loading conditions. The NPS Power Laboratory technicians cut the circuit boards on the LPKF prototype-milling machine and students in the power systems engineering program constructed the boards. Since the resonant converter described in this thesis is electrically equivalent to the simpler hard-switched converter, it was decided that the control and protection circuit board would be used in the resonant converter design as well. The block diagram of the control system, interfaces and driver boards is shown in Figure (D-1).

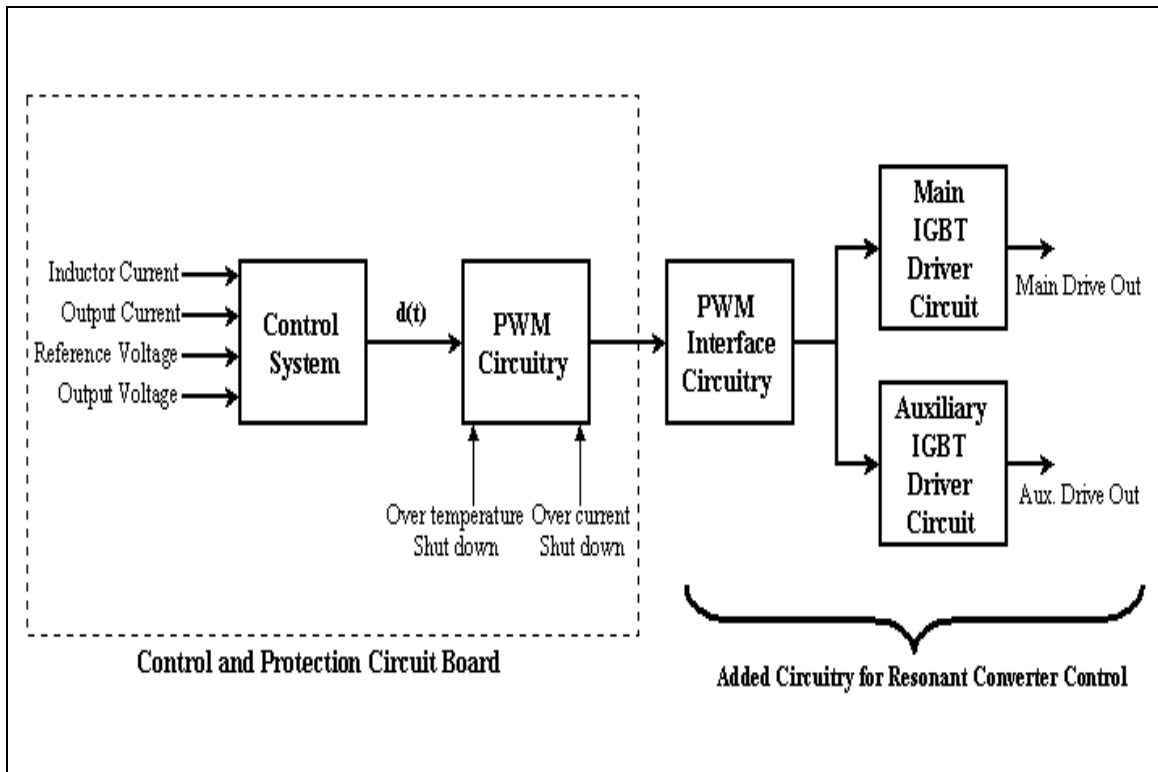


Figure D-1. Block Diagram of Control System, Interface and Driver Circuits.

Figure (D-1) does not show the control loop topology, but rather the circuit connections from the control card to the PWM interface card and then onto the driver boards. Equation (D-1) describes the overall control algorithm, a multi-loop control architecture, which may be viewed as a proportional-integral-derivative (PID) controller.

$$d(t) = -h_v (v_{out} - v_{ref}) - h_n \int (v_{out} - v_{ref}) dt - h_i (i_L - i_{out}) \quad (D-1)$$

The error signal $d(t)$ is made up of a proportional voltage term with gain h_v , an integral voltage term with gain h_n and a proportional capacitor current term with gain h_i . The error signal $d(t)$ then drives a pulse-width-modulation (PWM) circuit, which produces the intermediate IGBT drive signal. The control and PWM circuit is located on the control and protection section of Figure (D-1).

The control and protection circuit card developed for the hard-switched converter has a single IGBT driver signal from the PWM section. The resonant converter has two IGBTs that need to be controlled, so external circuitry was needed to produce the separate driver signals. Since the resonant converter project was internally funded and the finished unit is not planned to immediately be a part of ESAC's DC ZEDS testbed, the PWM interface circuit was designed to be as simple as possible with no protection circuitry. The resonant converter is still protected from an over-current and over-temperature condition in the control and protection board.

Originally the PWM interface circuit was going to drive a commercially made driver card as was done with the hard-switched converter. During the experimental testing phase it was found that the COTS driver boards could not produce a narrow drive signal for the auxiliary switch. A driver board was designed using an opto-isolator, and the final design did not have the short circuit detection and high duty cycle lockout protection like the commercial units. The design of the driver boards is discussed in Section B of this appendix. The PWM interface circuit is shown in Figure (D-2).

1. PWM Interface Circuit Theory of Operation

On the left side of the Figure (D-2), the signal, PWM_In , enters the circuit from the control and protection board. Recall that in steady state, PWM_In is a square wave with a period of $50\mu s$ and pulse width of $40\mu s$ (duty cycle of 80 percent). The pulse is fed to two OR gates, so that the main and auxiliary circuits are isolated from each other. To develop the drive signals, a 555 timer is used in the monostable mode for the auxiliary circuit and in a time delay mode for the main circuit. This discussion will assume that the reader is familiar with this well-known integrated circuit. The top circuit for the auxiliary drive is discussed first.

When PWM_In transitions from a low to a high (15 volts), the output of the OR gate U1A also goes high and Q1 is biased "on." The bottom of R2 is pulled low and a momentary negative-going pulse is coupled through C3 into the trigger of U2A. With a negative trigger received, the output Aux_Drive goes high and the capacitor C5 is no longer discharged by the internal transistor and charges up toward V_{cc} through the variable resistor R3. At $2/3$ of V_{cc} , the threshold is reached; Aux_Drive goes low and the internal transistor discharges C5 for the next cycle. The resistor R3 and capacitor C5 control the charge-up rate and, therefore, the width of the output pulse. The resistor R3 was adjusted until a pulse width of $2\mu s$ was obtained. Equation (D-2) from reference [35] relates the output pulse-width to the values of R3 and C5.

$$t_{pw} = 1.1RC \quad (D-2)$$

For a pulse width of $2\mu s$ and a capacitance of $1000pF$, a resistance of 1800Ω is required.

The bottom two 555 timers make up the main IGBT interface circuit. With the signal PWM_In at a low state, transistor Q3 is biased "on" and capacitor C6 is charged up to V_{cc} . With PWM_In low, the reset pin of U2B is low and the output $Main_Drive$ is disabled low. Upon receiving a high input, Q3 is cut-off and the reset pin of U2B is now high, thus enabling the output. Capacitor C6 discharges into R6 and when the trigger reaches $1/3$ of V_{cc} , the delayed output $Main_Drive$ goes high until PWM_In goes low and the output is once again disabled. Again, Equation (D-2) is used to calculate the delay

time based on R6 and C6. For a delay of 1.5 μ s and 470pF, the required resistance is 2900 Ω .

An additional monostable mode 555-timer circuit was added to ensure that the main IGBT is "on" for at least 3 μ s. When U2B's output goes high, U3 is triggered "on" and the resulting output is ORed with U2B's output so that the main switch is always conducting for the minimum of 3 μ s. If an input pulse with a width less than the delay time of U2B occurs, the auxiliary circuit will still gate, but the main circuit will remain low. The *PWM_In* signal is also sent to the reset pin of U2A, so that a spurious input signal will only momentarily toggle the auxiliary output before the timer is disabled. In the future, a better design is required, which will prevent the auxiliary IGBT from being gated by narrow pulses unless the main IGBT is going to be gated also.

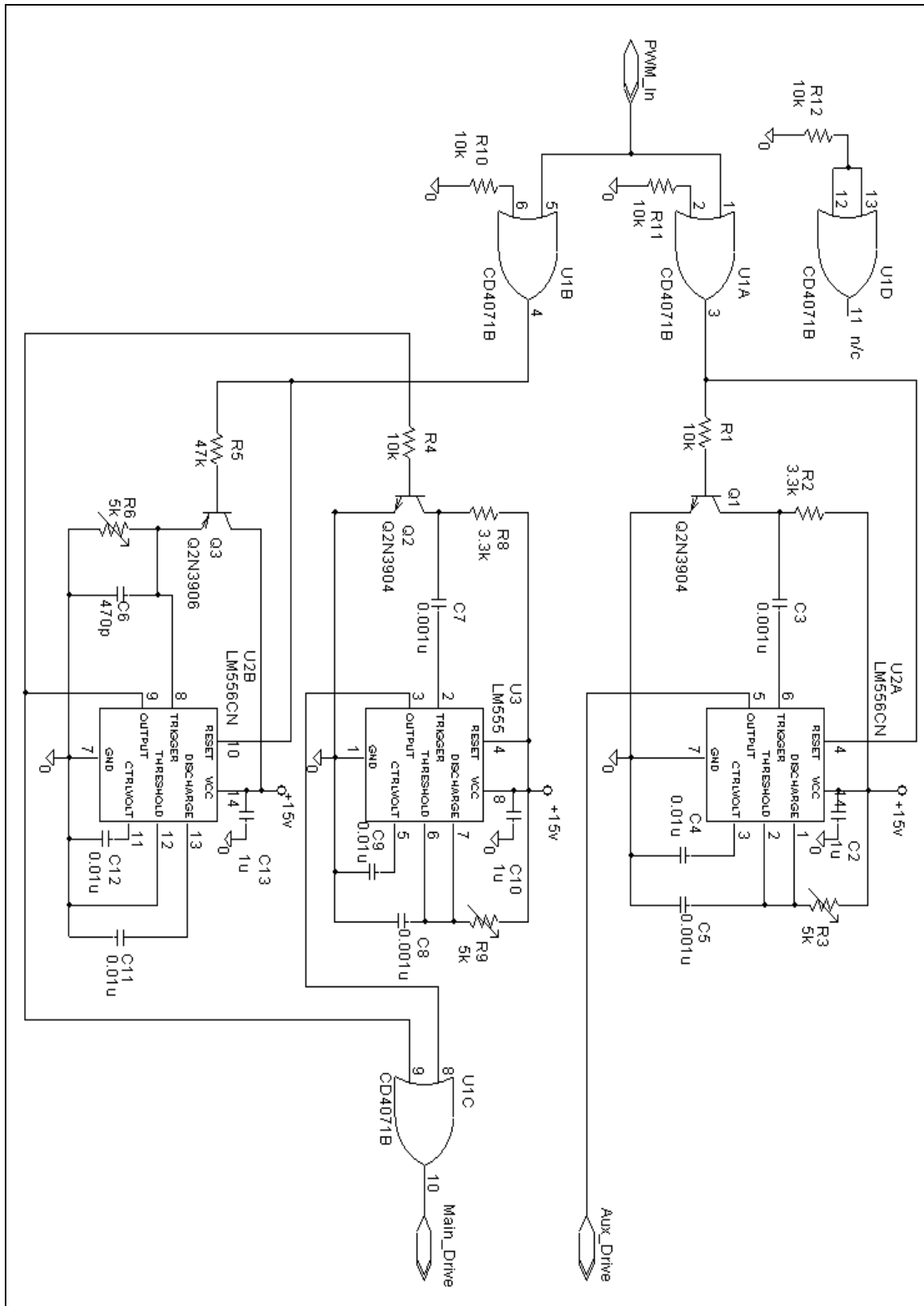


Figure D-2. PWM Interface Circuit.

B. IGBT DRIVER CIRCUIT

As discussed in the previous section, the commercial driver boards were tried in the resonant converter design. Although the drivers had a lot of protection features, they were unable to transition fast enough for the auxiliary IGBT. This limitation in the commercial driver boards is not a design defect and prevents spurious gating of the switches by noise. The commercial driver board will only pass drive command signal with pulse-widths greater than $5\mu\text{s}$. Like the PWM interface board, it was decided that the driver board should be as simple as possible. With that in mind, the driver circuit was designed around the Toshiba TLP250 optical isolator. The TLP250 data sheet is located in Appendix A.

1. IGBT Driver Board Theory of Operation

To control the IGBTs properly, both a positive and negative voltage is needed. The top circuit in Figure (D-3) is a full-wave rectified DC supply, which produces both +10 and -10 volts. The two voltages are fed to the pins on the TLP250 that correspond to the collectors of the internal complimentary transistor pair.

With the input *drive_in* in a low state, the input LED is reverse biased and the bottom transistor of the complimentary pair is biased "on." The signal *drive_out_gate* is pulled to -10 V_{dc} and the respective IGBT is gated "off." If the *drive_in* pin tries to go negative, D_1 will be forward biased, thus protecting the internal LED from exceeding the reverse voltage breakdown of 5 V_{dc} . A negative gate voltage is used vice a zero volt gate signal to aid in pulling the charge out of the IGBT gate circuit. The negative gate voltage shuts the IGBT down faster than simply applying zero volts to the gate.

When the control circuit orders an IGBT to be gated "on," the PWM interface circuit transitions the respective driver signal to a high and the LED in the TLP250 is forward biased. The upper transistor is now biased "on" and the *drive_out_gate* signal transitions to $+10\text{ V}_{\text{dc}}$.

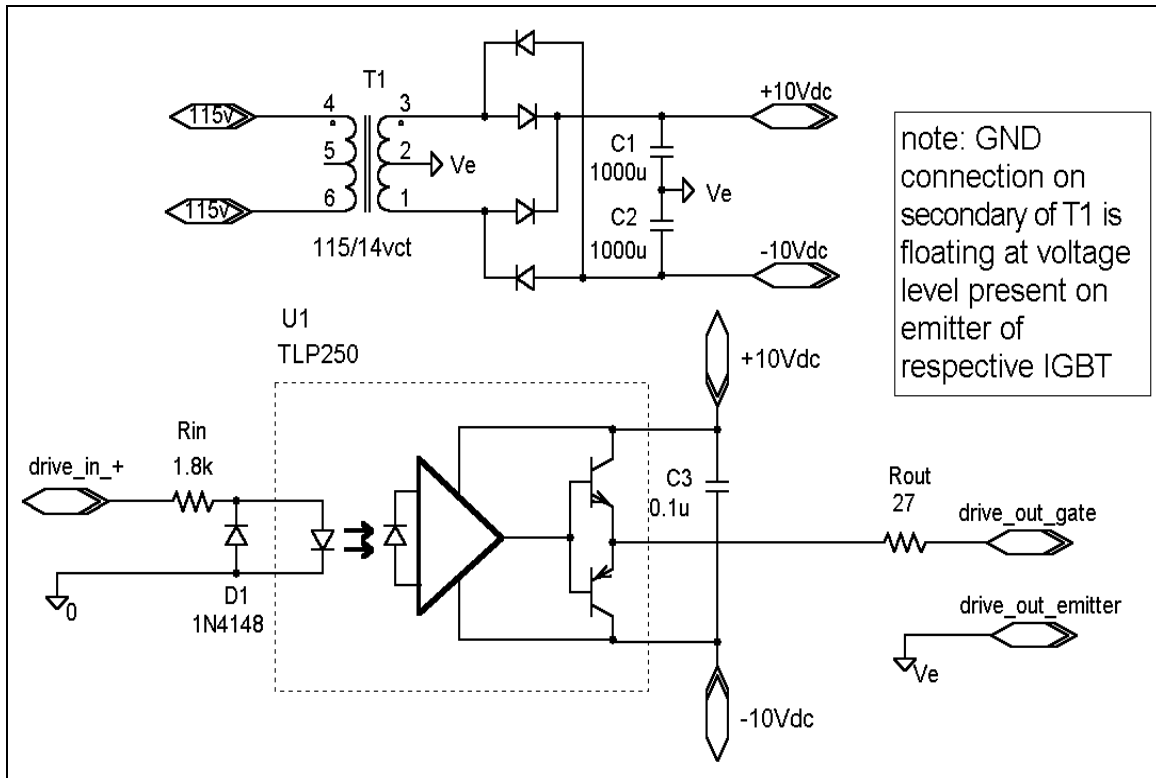


Figure D-3. IGBT Driver Board.

C. APPENDIX SUMMARY

Appendix D describes the basic control system, the PWM interface circuit and the IGBT driver circuit. The PWM interface and driver circuits are adequate for laboratory testing, but lack protection features such as minimum pulse lock-out and $V_{ce(sat)}$ detection. Figures (D-4) and (D-5) show the circuit boards and how they are mounted in the converter chassis. The circuit boards are mounted on an aluminum plate, thus providing metal isolation from the power circuitry.

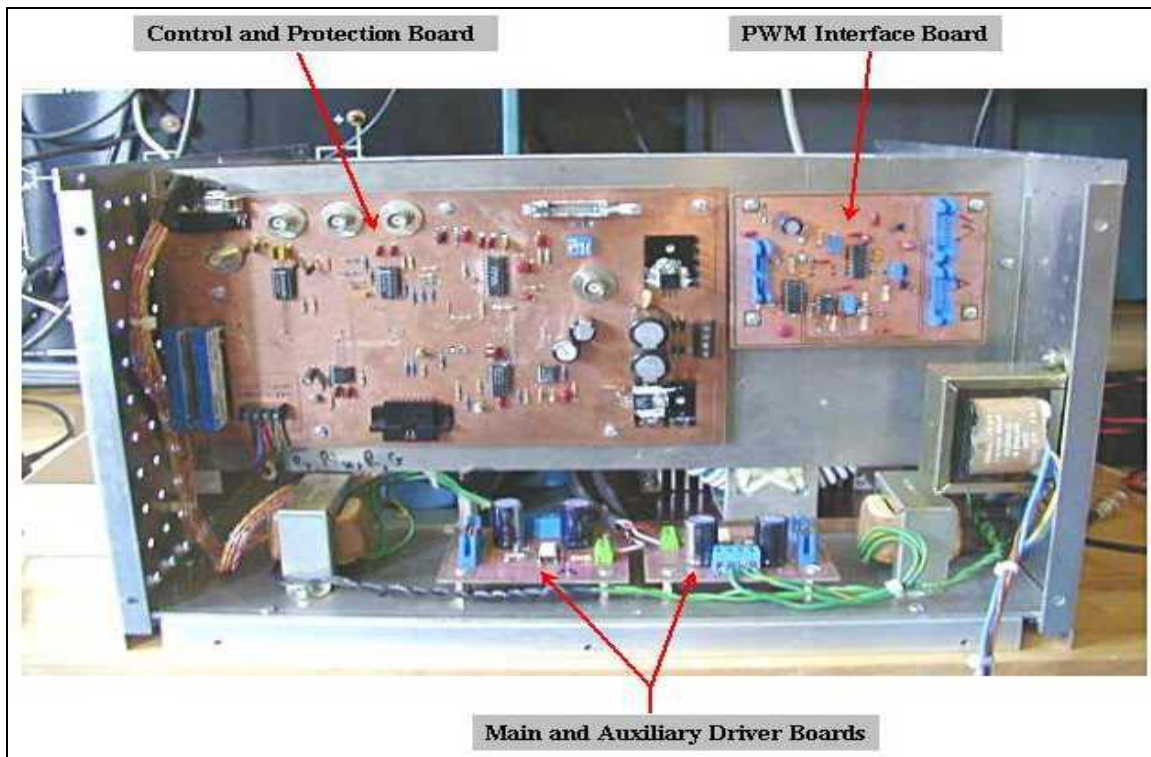


Figure D-4. Control and Protection, PWM Interface and Driver Boards.

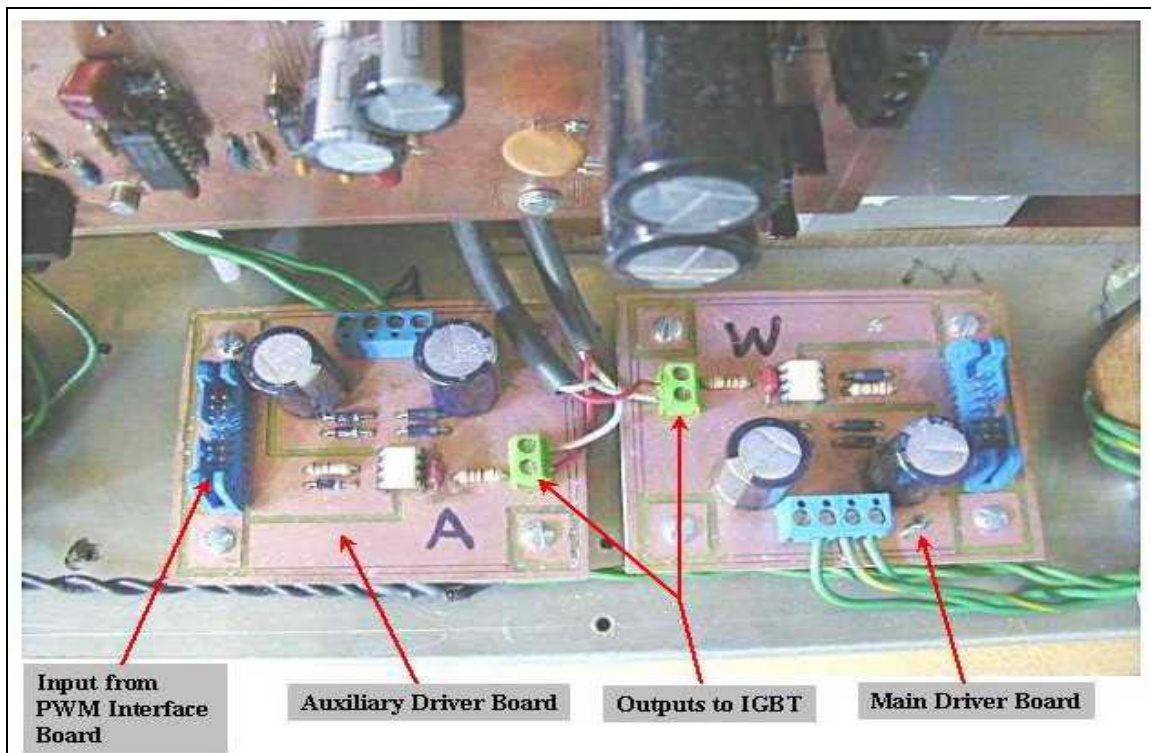


Figure D-5. Close Up View of IGBT Driver Boards.

APPENDIX E. MATLAB CODE

A. MATLAB CODE

```
% Bryan Whitcomb
% 17 May 2001
% Thesis Research
% This m-file takes all of the data from a PSPICE parametric sweep
% run and plots IGBT switch loss as a function of capacitance

clear;
format long;
FS=20e3; % switching frequency

% reading of PSPICE Data from Lotus worksheet format
data=wk1read('c:\matlabr11\work\Sm_sweep');
data_sa=wk1read('c:\matlabr11\work\Sa_sweep');
data_dm=wk1read('c:\matlabr11\work\Dm_sweep');
cols=min(size(data));% finds total # of data columns
rows=length(data);
cols_dm=min(size(data_dm));% finds total # of data columns
rows_dm=length(data_dm);

%Defines different columns as currents and voltages
Ism=data(2:rows,3:cols/2+1);
Vsm=data(2:rows,cols/2+2:cols);
Isa=data_sa(2:rows,3:cols/2+1);
Vsa=data_sa(2:rows,cols/2+2:cols);
Idm=data_dm(2:rows_dm,3:cols/2+1);
Vdm=data_dm(2:rows_dm,cols/2+2:cols_dm);

cap=[1,((1:cols/2-1)*(2.5e-9)+(10e-9)-2.5e-9)/1e-9];

Psm=Ism.*Vsm; % instantaneous power calculations
Psa=Isa.*Vsa;
Pdm=abs(Idm.*Vdm);

% Calculation of Energy Using Trapazoid rule
Esm=[4.12e-3,trapz(data(2:rows,1),Psm)];
Pm=FS*Esm;
Esa=[1.48e-3,trapz(data_sa(2:rows,1),Psa)];
Pa=FS*Esa;
Edm=[6.0e-4,trapz(data_dm(2:rows_dm,1),Pdm)];
```

$P_d = F_S \cdot E_{dm}$;

```
% plotting routines
figure(1)
plot(cap,Esm/1e-3,cap,Esa/1e-3,cap,...
Edm/1e-3,cap,(Esm+Esa+Edm)/1e-3), grid
title('Energy Loss versus Resonant Capacitance for Lr= 28uH')
xlabel('capacitance(nF)')
ylabel('Energy(mJ)')
legend('Esm','Esa','Edm','Etotal')

figure(2)
plot(cap,Pm,cap,Pa,cap,Pd,cap,Pm+Pa), grid
title('Power Loss versus Resonant Capacitance for Lr= 28uH')
xlabel('capacitance(nF)')
ylabel('Power (w)')
legend('Pm','Pa','Pdm','Ptotal')

figure(3)
plot(cap,Pm-34), grid
title('Main Switch Turn-off Loss versus Resonant Capacitance for Lr= 28uH')
xlabel('capacitance(nF)')
ylabel('Power(W)')
```

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