HgCdTe HETEROEPITAXY ON Si SUBSTRATES FOR LOW-COST, LARGE FORMAT, DUAL-BAND INFRARED FOCAL PLANE ARRAYS

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ABSTRACT

Recent advancements in HgCdTe heteroepitaxy on silicon substrates are described. The aim of these efforts is the extension of the spectral response of HgCdTe-on-Si-based devices into the long wavelength infrared region. The achievement of this aim will enable low-cost, third generation infrared focal plane arrays.

1. INTRODUCTION

Critical to Army Transformation are advanced sensors which enhance situational awareness and offer target identification ranges greater than adversarial detection ranges. The Night Vision and Electronic Sensors Directorate (NVESD) is aggressively pursuing such technologies, particularly very large format (~ 1M pixels), staring, dual-band, infrared focal plane arrays (IRFPA) based on the semiconductor alloy HgCdTe. The enabling materials' technology for such sensors is the use of molecular beam epitaxy (MBE) to fabricate epitaxial layers of this material on substrate wafers. Not only does MBE offer precise control of layer thickness, chemical composition (band-gap) and doping of the individual layers, but it is also a scalable process which offers potential cost savings by increasing throughput at all stages of IRFPA manufacturing.

In wafer-scale semiconductor processing, throughput depends strongly on the number of die that can be fabricated on each wafer. As IRFPA formats increase to the megapixel level and beyond, wafer size becomes a crucial cost driver. Currently, CdZnTe wafers, the industrial baseline substrate for HgCdTe epitaxy, are available only in relatively small sizes (~50 cm^2). To exploit the cost savings inherent in MBE, NVESD and others are investigating the use of Si wafers as alternatives to CdZnTe. Si substrates offer numerous advantages: high crystalline quality, large area, very low cost, and ample commercial availability.

However, disparities in fundamental properties of the two materials make the use of Si substrates for HgCdTe epitaxy extremely challenging. First the lattice-parameters of HgCdTe and Si differ by ~19%. Secondly, the thermal expansion coefficients of the two materials differ by a factor of ~3. Thirdly, as is the case with all narrow band-gap semiconductors, the performance of HgCdTe devices is easily degraded by the presence of threading dislocations and other defects introduced by the aforementioned mismatches. In essence, the challenge of HgCdTe/Si epitaxy is one of defect mitigation.

Remarkable progress has been made in HgCdTe/Si epitaxy, leading to detectors for the short wavelength and mid-wavelength infrared (SWIR and MWIR) ($2\mu m < \lambda < 5\mu m$) spectral regions whose performance is equivalent to devices fabricated with HgCdTe/CdZnTe. An excellent status review of MWIR HgCdTe/Si technology was given by deLyon et al., 1999.

We report here on recent materials' science efforts to extend the applicability of the HgCdTe/Si system to the long wavelength infrared (LWIR) ($\lambda \sim 10\ \mu m$) spectral region. NVESD has developed new processes that have produced composite substrates - planar epitaxial CdTe buffer layers on three inch Si wafers - that are suitable for the MBE of LWIR HgCdTe. Values of x-ray diffraction line width less than 70 arc seconds are now routinely obtained and maps of these line widths show excellent spatial uniformity across a three inch wafer. Dislocation density values, revealed by defect-decoration etching, are typically $1\text{-}5 \times 10^6\ cm^{-2}$. In collaboration with Rockwell Scientific Company (RSC), LWIR IRFPAs are fabricated using these substrates. Detector and IRFPA performance results are given and discussed within the context of the limit set by the relatively high values of dislocation density still present.

We also report a novel approach to dislocation defect mitigation, namely the epitaxy of CdTe buffer layers on reticulated Si substrates. For this process Si wafers are patterned using standard photolithographic techniques and

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etched to form mesas using either standard wet-chemical or novel plasma techniques. The concept is depicted schematically in Figure 1, in which a Si substrate is represented by the green area, a CdTe epilayer by the grey area, and threading dislocations as red curved lines. In the case of growth on a planar substrate (Figure 1, top), a threading dislocation can be removed only if it is annihilated by collision with another dislocation. In the case of epitaxy on a reticulated substrate however (Figure 1, bottom), an additional removal mechanism is introduced by the existence of the free surfaces of nearby sidewalls. If the lateral dimension of the mesa is made sufficiently small (~ the thickness of the epitaxial layer), most threading dislocations can be made to bend to intersect the sidewall, and the region near the top of the mesa, where the photodiode will be formed during device processing, will be defect free. Similar techniques have been used successfully in a wide range of other heteroepitaxial materials systems: GaAs/Si (Matyi et al., 1991); SiGe/Si (Fitzgerald, 1989); HgCdTe/CdZnTe (Rhiger et al., 2000, Martinka et al. 2002). For the CdTe/Si system there have been attempts at selective-area epitaxy. (Sporken et al., 2000 and Zhang and Bhat, 2000). Recently, attempts have been made to validate the efficacy of the reticulated substrate concept in the HgCdTe/Si epitaxial system.

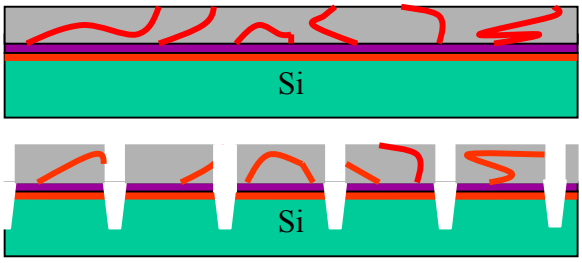

Figure 1. Schematic representation of dislocation reduction utilizing reticulated Si substrates. Standard growth on planar substrate (top). Epitaxy on reticulated Si substrate (bottom).

2. EXPERIMENTAL PROCEDURE

Generally, in order to overcome the extreme differences in the fundamental material properties of HgCdTe epilayers and Si substrates, an appropriate, intervening buffer layer is utilized. In this work thick (> 10 μm) epitaxial CdTe serves as this buffer layer. During the past five years NVESD has been developing and refining epitaxial processes, which have resulted in the highest quality, three-inch diameter, planar CdTe(211)B/Si(211) wafers. RSC has utilized these wafers as composite substrates for HgCdTe MBE and has fabricated diodes in these layers using their advanced planar processing line. Here we present characteristics of these epilayers and diodes. We also report characteristics of CdTe epilayers formed on reticulated Si wafers. At this time no HgCdTe diodes have been fabricated from such buffer layers.

2.1 Baseline CdTe/Si (211) buffer layer procedure

CdTe buffer layers are deposited at NVESD using a commercial 3-inch MBE chamber onto (211) Si wafers. The (211) orientation has previously been found to be optimum for HgCdTe MBE. Most relevant details of the (211)CdTe/Si deposition process are reported elsewhere (Dhar et al. 2000 and Almeida et al. 2001). Indium-free, molybdenum substrate holders are used to secure three-inch, nominal (211) Si substrates, which are hydrogen passivated *ex situ* in a similar manner as described by Taylor et al. 1999. Hydrogen is removed *in situ* by heating the wafers to ~700 °C. At temperatures above 450 °C, surfaces are passivated by exposure to an As_4 flux ~ 10^{-8} mbar.

Following As passivation, the substrate is cooled to ~ 280°C , and a thin (~50 nm) ZnTe layer is grown by alternatively exposing the substrate to elemental Zn and Te fluxes (~10^{-6} and ~10^{-7} mbar, respectively). The ZnTe layer is annealed at ~ 450 °C under elemental Te flux. Growth of CdTe is carried out at substrate temperatures of ~280° C using a dual filament CdTe effusion source, at a growth rate of < 1 μm/hour. Growth is interrupted periodically (~ every 1 μm of deposition) and the epilayer is annealed to ~ 450 °C under Te flux. NVESD has previously reported the efficacy of cyclic annealing as a method of dislocation reduction (Almeida et al. 2001)

CdTe (211)B/Si(211) composite substrates are characterized extensively to determine structural quality. Nomarski microscopy is performed to evaluate surface morphology and macroscopic defect densities. Fourier transform infrared (FTIR) spectroscopy is used to determine epilayer thickness and optical transmission value. A variety of x-ray diffraction measurements are performed to determine crystalline quality and uniformity, wafer bowing, strain relaxation, and lattice parameter value. Selected wafers are etched in a dislocation-decoration solution (Everson et al., 1995), which produces microscopic pits, each a signature of a threading dislocation. Optical microscopy is then used to measure the areal density of the pits.

2.2 Baseline HgCdTe growth and device fabrication

HgCdTe LWIR epilayers are deposited on CdTe/Si composite substrates by RSC. The CdTe mole fraction in each layer, and therefore its electronic band gap, are controlled during MBE growth by spectroscopic ellipsometry (SE). Fluctuations in the Cd content are

compensated by a feedback loop controlling the CdTe and Te source temperatures thus maintaining uniform composition throughout the thickness of the epilayer.

RSC's double layer planar heterostructure (DLPH) architecture is adopted as a baseline. This consists of a HgCdTe absorber layer doped n-type with indium, and a wider band gap cap layer. The formation of the p-on-n junction-diode is achieved by ion-implantation of arsenic through a photoresist window followed by high temperature annealing for cap layer diffusion and carrier activation. The structure is passivated with a CdTe layer.

LWIR HgCdTe(211)B epilayers deposited on CdTe(211)B/Si(211) composite substrates are evaluated at RSC using a variety of techniques. The composition and thickness of each layer are measured at room temperature using FTIR. Carrier concentration and mobility are measured at 77 K using the Van der Pauw technique at a magnetic field of 2000 Gauss. Minority carrier lifetime is measured on select samples using the photoconductive decay method. Void and microvoid defect densities are measured using optical microscopy. Dislocation density is determined by counting the trianguar etch pits revealed by a dislocation etch.

LWIR HgCdTe epilayers which demonstrate sufficiently high quality are selected for subsequent device fabrication. A performance evaluation chip (PEC) consisting of diodes with a variety of junction areas is fabricated on each layer to further evaluate layer quality and its suitability for FPA fabrication. Current-voltage (I-V) characteristics and zero bias impedance/resistance products (R_oA) for diodes with various junction sizes are measured at 78 K and at 40K. Spectral response is measured using FTIR. Quantum efficiency (QE) is measured with a calibrated blackbody source under both spot and flood illumination to extract the effective lateral optical collection length (L_o), which is used to determine the optical collection area A_o.

Wafers screened by fabricating and testing PECs are then processed to produce FPAs. The format selected is 256x256 pixels with each pixel consisting of a 28 μm diameter implant on a 40 μm pitch. FPAs are constructed by hybridizing LWIR HgCdTe detector arrays to TCM2001 direct injection readout integrated circuit chips using indium bump technology.

2.3 Reticulated Si substrate processing and CdTe buffer layer growth

Si (211) substrates are reticulated lithographically using standard photoresist patterning technology. A variety of mesa feature geometries was explored. Mesa sizes ranged from ~10 to 100 μm. Mesa shapes included squares, triangles and parallelograms. Following the work of Martinka et al., 2001, the mesa sidewalls were aligned either parallel or orthogonal to the intersections of the [111] slip planes with the (211) growth surface and therefore had [-231], [-213] and [0-11] orientations. The patterned surfaces are submerged for ~ 6 seconds in a common Si etching solution containing 8 parts hydrofluoric acid, one part nitric acid, one part acetic acid and two parts de-ionized water. This process results in surface features on the Si substrates of ~ 700 nm in height. Following this etching procedure, the substrates are cleaned in acetone, de-ionized water and methanol to remove residual photoresist material. After substrate cleaning, further surface preparation, CdTe epitaxy, and epilayer characterization proceed as described in 2.1.

3. RESULTS AND DISCUSSION

3.1 Materials characteristics

3.1.1 Baseline planar CdTe/Si (211) buffer layer characteristics

The primary figures of merit used to evaluate CdTe(211)B/Si(211) are line widths of x-ray diffraction peaks, EPD, and surface morphology. MBE process optimization consists in efforts to minimize line widths and EPD values, while maintaining a sufficiently smooth surface for subsequent HgCdTe epitaxy. Typical CdTe buffer layer thicknesses are 12-14 μm.FWHM values as low as 65" are measured for 224 reflections from CdTe/Si buffer layers. For some wafers, FWHM values remain below 75" to the wafer edge. A typical map is shown in Figure 2. FWHM values range from ~ 66 to ~ 80 arc seconds, with the vast majority of the wafer area having FWHM values < 70 arc seconds. Radius of curvature values > 20 m are extracted from additional X-ray-diffraction measurements. Such a value corresponds to a total deflection from wafer center to edge of 15-20 μm. This was confirmed using stylus profilometry.

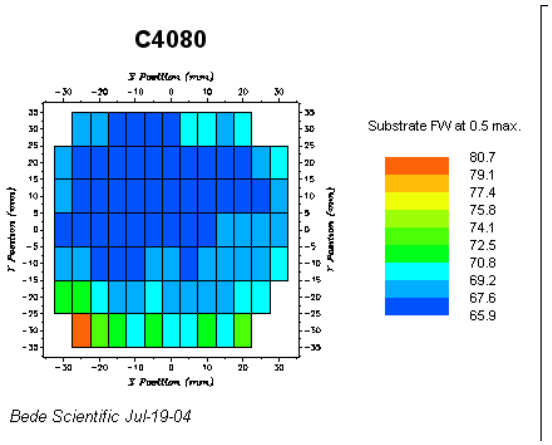

Figure 2. X-ray diffraction rocking curve FWHM values mapped across entire three-inch CdTe/Si wafer.

Typical dislocation-density values for our baseline CdTe (211)B/Si (211) epilayers are in the range 4-10 × 10^6 cm^{-2}.

CdTe surfaces appears mirror-smooth to the eye and show no roughness under Nomarski contrast-enhanced microscopic inspection with 800X magnification. While surface roughness at the microscale is negligible for these wafers, a low density (<1000 cm^{-2}) of large (1-10μm diameter) "flake" defects (see Almeida et al., 2001) continues to be observed on some CdTe buffer layers on Si. Efforts are being made to characterize and reduce the density of these particle defects. Microscopy of the defects suggests polycrystalline material with no preferred orientation with respect to the surrounding material. Potential nucleating sites for these defects could include foreign debris such as dust or droplets introduced by pre-growth wafer cleaning, or small material flakes emitted by hot CdTe or Te effusion cells during the epilayer deposition process. To date, no correlation between surface preparation methods and particle defect density has been observed, and preliminary SEM images taken of buffer cross-sections created by focused ion beam milling indicate that particle defects nucleate during CdTe growth, above the prepared Si growth surface. Supporting this observation, a positive correlation between Te and CdTe effusion cell temperatures and final particle defect density values has recently been observed. Reducing Te cell temperature during cyclic annealing steps, and reducing CdTe growth rates below 1 μm/hr by maintaining low cell temperatures can reduce final defect density counts significantly. Optimized growth recipes have significantly reduced large particle (diameter >1μm) defect densities from greater than ~1000 cm^{-2} to less than 3 cm^{-2}. It is found that these defects are inherited by subsequent HgCdTe layers and give rise to inferior devices. Efforts to reduce the particle defect densities in the buffer layers are therefore expected to increase the operability of IRFPAs fabricated on this material.

3.1.2 Baseline LWIR HgCdTe/CdTe/Si device-layer material characteristics

HgCdTe epilayers deposited at RSC on CdTe(211)B/Si(211) composite substrates are evaluated using standard techniques as described above (section 2.2). Typical epilayers utilized in this study have HgCdTe epilayer thickness of ~10 μm and a Cd content of x = 0.23 ($Hg_{1-x}Cd_xTe$). These values are highly reproducible from run to run - a result of the real-time SE feedback control.

Transport properties are extracted from Hall effect measurements at 77K and a magnetic field of ~2000 Gauss using a Van der Pauw configuration. HgCdTe/Si epilayers exhibit typical carrier concentrations of ~1 × 10^{15} cm^{-3} and mobilities of ~10^5 $cm^2/V{\cdot}sec$. Additionally, minority carrier lifetime was measured on two HgCdTe/CdTe/Si samples. At ~77K minority carrier lifetime is ~1-2 μsec. which is near the theoretical value and is comparable to values measured on LWIR HgCdTe grown on lattice-matched CdZnTe wafers.

Dislocation densities are ~ 4-6 ×10^6 cm^{-2}. These values are consistent with EPD values on the CdTe/Si buffer layers (see section 3.1.1), which indicates that the HgCdTe epitaxial process is substrate limited.

3.1.3 CdTe buffer layer on reticulated Si substrate material characteristics

The steps carried out to produce CdTe epilayers on reticulated Si substrates are identical to those used on planar wafers. (see section 2.1). Optical micrographs show conformal coverage of CdTe over the mesa tops, the sidewalls, and the trenches between the mesas. This is to be expected, given the relatively shallow mesa height (~ 700 nm) compared to the total CdTe epilayer thickness (~10 μm). X-ray FWHM values of 70" are measured in planar regions of CdTe epilayers on reticulated wafers, an indication of the fact that the additional processing steps needed for reticulation do not compromise the Si surface.

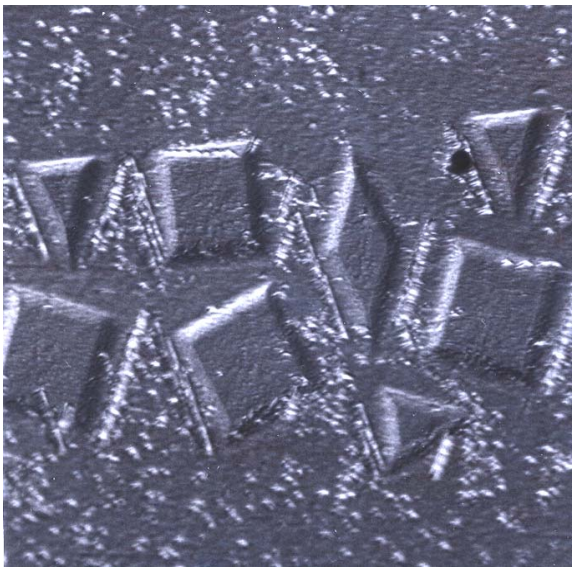

Figure 3. Defect decoration etch of CdTe epilayer on reticulated Si(211) substrate. Square mesas are ~10 μm on a side.

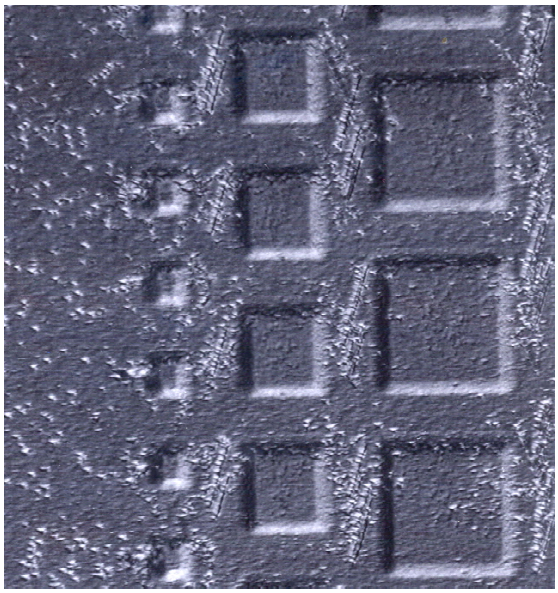

Figure 4. Defect decoration etch of CdTe epilayer on reticulated Si(211) substrate. Square mesas are ~ 5 µm, ~10 µm and ~20 µm on a side.

The most significant difference in epilayers grown on reticulated substrates is the EPD values at the mesa tops. Figures 3 and 4 are micrographs of 10 µm thick CdTe deposited on the mesas. In these micrographs, etch pits appear as white, roughly triangular, features. As can be clearly seen from these micrographs, the density of etch pits is significantly reduced on the mesa tops, compared to areas between the mesas. Figure 4 demonstrates the size requirement for efficient etch pit reduction. For mesas with tops ~ 5-10 µm across, virtually no etch pits are present, whereas for mesas with 20µm tops an occasional etch pit is found and it usually lies at the perimeter of the mesa. Note the high density of pits between mesas, which pits align along crystallographic directions, specifically along [-231] and [-213]. These directions correspond to the intersection of two sets of slip planes (11-1) and (1-11) with the (211) surface.

These observations suggest that growth on reticulated substrates promises to be an effective means of reducing dislocation densities near critical areas (i.e. diode junctions) of HgCdTe photodetectors grown on Si substrates. Additional validation of this concept, particularly the evaluation of the performance of HgCdTe diodes formed on these mesas, is required.

3.2 LWIR HgCdTe/Si device characteristics

Performance of photodiodes fabricated in baseline HgCdTe/CdTe/Si structures was measured at RSC and at NVESD. 78K current-voltage characteristics of diodes of various sizes on a representative LWIR HgCdTe layer are shown in figure 5. 8 and 16 µm (implant area) diameter circular diodes and 26, 46, 125 and 250 µm square diodes

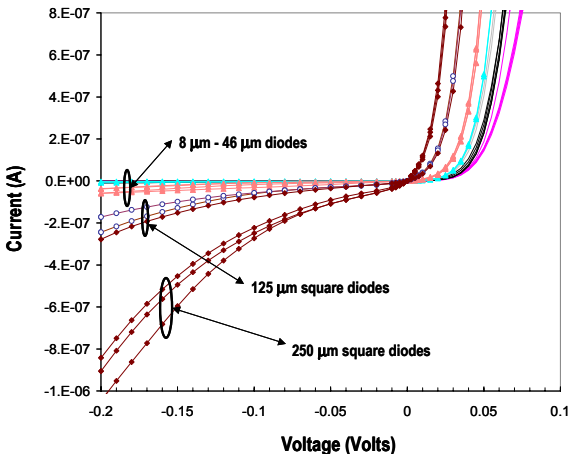

Figure 5. 78 K current-voltage response for diodes with various junction areas.

are represented in Figure 5. Diodes with the smallest junction areas (8 µm and 16µm) are diffusion limited beyond 150 mV of reverse bias and have very low leakage currents. As the junction area of a diode increases, the reverse bias characteristic becomes increasingly "soft", with the largest diodes (125 and 250 µm) starting to show significant leakage currents at reverse bias values less than 0.01 mV.

In figure 6, R_0A_{Opt} is plotted as a function of implant area. For the smallest diodes (10 µm) R_0A_{Opt} values approach 1000 Ω-cm^2. However, there is appreciable spread in the R_oA_o, with most of the larger area diodes centered at an average value of ~100 Ohm-cm^2.

Device characteristics of LWIR HgCdTe/CdTe/Si diodes measured at 78 K are typical of diodes fabricated from high dislocation density LWIR HgCdTe/CdZnTe diodes. Dislocations threading through the junction region reduce the RoA product and increase the reverse bias leakage currents. The variation in leakage currents with diode area is also consistent with high dislocation density LWIR HgCdTe.

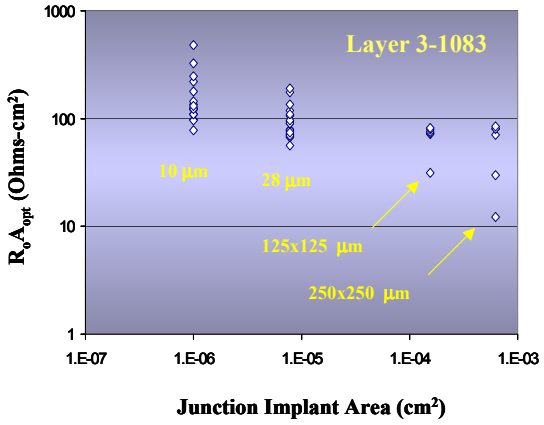

Figure 6. Zero bias impedance area product (R_0A_{Opt}) as a function of junction implant area.

Additional measurements made on the PEC devices, represented in figure 6, include spectral response and quantum efficiency (QE). Spectral response values are comparable to those measured for LWIR HgCdTe/ CdZnTe. The spectral cutoff λ_c (defined as the point where the response per watt drops to 50 % of peak value) measured at 78 K is ~ 10.0 μm. QE for these devices without antireflective coating is 54.8 %.

3.3 LWIR HgCdTe/Si FPA characteristics

Wafers containing the highest performing diodes were selected for FPA fabrication. FPAs were operated at 78K with a 0.32 ms integration time. A 300 K blackbody source illuminated the FPA through an f/2.8 cold aperture and 7.5-10 μm cold filter. Mean dark current per pixel, measured with the cold shutter closed, was 5.9 x 10^9 e-/sec, a value approximately six times lower than the photocurrent of the noise equivalent temperature difference (NEDT) measurement. The magnitude and bias dependence of the dark current are consistent with the R_oA_o values and soft I-V characteristics reported above. The median NEDT of 28 mK exceeds the 16 mK photon noise limit. Possible causes of the excess noise and the high noise tail of the NEDT histogram are 1/f noise associated with the dark current and noise on the ROIC bias lines that determine the detector reverse bias operating point. The percentage of pixels with noise less than twice the median is 92.3%. Two single data frames produced by this FPA operated at 80K in an infrared camera with f/2 optics and a 52Hz frame rate are shown in figure 8. Signals from defective pixels in the images in figure 8 are replaced by the average of their neighbors.

Figure 8. Imagery obtained from LWIR HgCdTe/Si 256x256 IRFPA (F/2 optics, 52 Hz frame rate)

CONCLUSIONS

Silicon wafers offer an attractive alternative to conventional CdZnTe wafers as substrates for HgCdTe epitaxy. Results presented here indicate that, when conventional MBE deposition and standard diode-formation techniques are applied to composite CdTe/Si wafers, IRFPAs with moderately high performance can be obtained despite the high density of threading dislocations present in these materials. Results of initial experiments using reticulated instead of planar Si wafers offer grounds for optimism that a further reduction in dislocation density can be had. This would, in turn, lead to single and dual band IRFPAs with performance approaching that of conventional technology at greatly reduced cost.

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