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Alignment of Nanotube Arrays

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2. First careful electrical measurements on nanotube peapods.
3. Novel technique for imaging local heating in narrow wires.

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Objectives:

Carbon nanotubes have many emerging technological uses, from strengthening lightweight composite materials to reducing voltage requirements in field-emission displays. Companies such as IBM and Intel have substantial research efforts aimed at the more complex task of building transistors and computer processors from nanotubes. Research under this proposal addresses two of the important requirements for achieving that vision. First, we aim to understand and modify electron flow in one-dimensional systems, notably carbon nanotubes. Second, we aim to control the location and orientation of those nanotubes, which would be crucial for building complex circuits. Because of finite resources, we have focused on the first of the two aims, by building a variety of nanotube-based transistors. These include a crossed-nanotube transistor which could, in principle, be shrunk to a length of a few nanometers, an order of magnitude smaller than the transistors in current-generation Pentium chips.

This work benefits from collaboration with the groups of Hongjie Dai (Chemistry) and Paul McIntyre (Material Science and Engineering). Their portion of the collaboration was not, however, funded through this contract.

Status of effort:

As of Dec 31, 2004, we had been funded on this project for two and a half years. For the first six months, much of our effort was focused on single-crystal organic electronics. We then submitted a revised proposal and, with approval from Dr. Harold Weinstock, switched our effort to carbon nanotubes. Hence, this report covers progress through two years of funding. We have progressed on several fronts:

1. After learning to grow tubes by chemical vapor deposition (CVD) in furnaces maintained by the Dai lab, and characterizing the resulting structures using atomic force microscopy, we realized that our research interests were somewhat different from those of the Dai lab. Hence, with encouragement and generous suggestions from the Dai lab, we decided to build our own CVD furnace. We succeeded: our first growth run yielded the desired single-walled nanotubes, and we now synthesize most of our tubes in our furnace.

2. We have reproduced other groups' findings on nanotube transistors, using an oxidized n++ Si substrate as a back gate.

3. We have demonstrated transistors based on crossed nanotubes, with one tube gating another across a thin dielectric. These transistors worked, but to form them we had to rely on accidental crossings of tubes. This resulted in low device yield: 2 working devices from multiple growth runs and tens of hours of searching with AFM. Hence, we have suspended this work until we develop (or adopt) a reliable method for nanotube alignment.

4. We have made nanotube transistors with metal gates, including among the shortest metal gates ever used on such transistors (20-30 nm). This work was initially slow, primarily because our simplest transistor requires four to five steps of electron-beam lithography

and the Stanford e-beam lithography system has not been stable enough to get all those steps to work. Therefore, we have obtained access to more reliable local industrial facilities for lithography. We expect to achieve world-class short-gate nanotube transistors, and to explore new physics on scattering in one-dimensional systems, soon. We have now (April 2005) fabricated the first of these devices, and have shown that they are gatable at room temperature and low temperature, with minimal hysteresis. The new devices greatly benefit from our use of atomic layer deposition (ALD) for depositing thin, conformal oxide dielectrics. We have achieved excellent breakdown voltages of greater than 7 MV/cm over 100x100 micron areas, probably even larger in the narrow gated region of a nanotube.

5. While the short-gate devices were temporarily difficult to fabricate, we have explored "peapods": single-walled carbon nanotubes (the pods) filled with C_{60} buckyballs (the peas). These are a fascinating test case for how carbon nanotube electrical properties might be tuned by chemically modifying the nanotubes. Peapods are expected to show modified band structure due to the nearly-periodic potential modulation produced by the buckyballs. We have made the most careful measurements to date in peapod transistors. Remarkably, our early measurements show electrical properties very similar to those in unfilled nanotubes, suggesting that the electrical coupling between the buckyballs and the outer tube is very weak.

6. We have developed a novel technique for imaging local heating in narrow current-carrying wires. This should be applied to carbon nanotubes in the next 1-2 years.

Accomplishments:

1. First crossed-nanotube transistor with gate dielectric (to our knowledge).

2. First careful electrical measurements on nanotube peapods.

3. Novel technique for imaging local heating in narrow wires.

Personnel supported or associated with work:

Principal Investigator:

David Goldhaber-Gordon, Assistant Professor of Physics; 0.5 mo. summer salary

Graduate students:

Charis Quay, 4th year in Physics: associated (supported primarily by fellowship), working on nanotube transistors and nanotube variants: "peapods".

Joseph Sulpizio, 2nd year in Physics: supported, working on nanotube transistors.

Lindsay Moore, 5th year in Physics: associated in early stages of research.

John Cumings, postdoctoral researcher: associated, working on mapping local heating in narrow current-carrying wires.