

# Silicon-on-Sapphire Technology: A Competitive Alternative for RF Systems

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## INTRODUCTION

Device-quality, thin-film silicon-on-sapphire (TFSOS), obtained by Solid Phase Epitaxy (SPE), has achieved truly outstanding results that are incorporated into present and future high-performance products, such as phase-locked loop integrated circuits (ICs) for wireless communications [1], single-chip Global Positioning System (GPS) receivers, and analog to digital converters (A/DCs) for space applications.

## EXPERIMENTAL STUDY

Table 1 shows the measured performance of a front-end receiver at 2.4 GHz; and voltage-controlled oscillators (VCOs), frequency dividers, and tuned amplifiers at >20 GHz. The n-metal oxide semiconductor (MOS) VCO at 26 GHz [2] has the highest tuned frequency ever achieved among complementary metal-oxide semiconductor (CMOS) VCOs.

Concomitantly, recent advances in SiGe epitaxial growth technology indicate that SiGe-based strained-layer modulation-doped field-effect transistors (MODFETs) may be promising alternatives to III-V metal-semiconductor field-effect transistors (MESFETs) and high-electron mobility transistors (HEMTs) for future high-speed analog communications applications. Electron and hole mobilities well in excess of bulk Si mobilities can be realized in tensile-strained Si quantum wells (QWs) [3] and compressive-strained SiGe [4] or pure Ge QWs [5], respectively. Note that p-MODFETs have demonstrated dc and RF performance figures comparable to n-MODFETs, suggesting the possibility of very-high-speed complementary operation [6], a capability not available in current III-V technology. In this work, we have applied this knowledge to the growth of SiGe relaxed buffer layers and the fabrication of SiGe strained-layer MODFETs on TFSOS. One of the benefits of using insulating substrates, such as sapphire, is the potential solution to the reduction of high losses seen in the microwave frequency regime due to the conducting nature of the silicon substrate. Here, we demonstrate the development of the epitaxial growth of high-mobility, modulation-doped, composite-channel heterostructures on silicon-on-sapphire (SOS) substrates, and describe the resultant outstanding RF characteristics of  $\leq 100$  nm T-gate p-MODFETs fabricated on these layer structures.

The composite-channel heterostructure device has the basic structure shown in Figure 1. This layer structure was grown on an SOS substrate

## ABSTRACT

*We investigated the formation of high-performance, device-quality, thin-film silicon (30 to 50 nm) on sapphire (TFSOS) for application to millimeter-wave communication and sensors. The resulting TFSOS, obtained by Solid Phase Epitaxy (SPE), and the growth of strained silicon-germanium (SiGe) layers on these TFSOS demonstrated enhanced devices and, hence, integrated-circuit performance not achieved previously. We fabricated 250-nm and 100-nm T-gated devices with noise figures as low as 0.9 dB at 2 GHz and 2.5 dB at 20 GHz, with  $G_a$  of 21 dB and 7.5 dB, respectively. 250-nm devices resulted in distributed wideband amplifiers (10-GHz bandwidth [BW], world record) and tuned amplifiers (15-dB, 4-GHz BW). 100-nm devices produced voltage controlled oscillators (VCOs) (25.9-GHz), 30-GHz frequency dividers. We obtained  $f_t$  ( $f_{max}$ ) of 105 GHz (50 GHz) for n-channel and 49 GHz (116 GHz, world record) for p-MODFETs (strained  $Si_{0.2}Ge_{0.8}$  on a relaxed  $Si_{0.7}Ge_{0.3}$  hetero-structure). This paper details our investigation and provides cost comparisons with competing technologies.*

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TABLE 1. Measured performance of various components of a front-end receiver designed to operate near 2.4 and 18 GHz.

Measured	Operating Frequency	Gain	NF (50 $\Omega$ )	IP3 (output)	Power@Vdd
LNA	2.4 GHz	11 dB	2.2 dB	14 dBm	13.2 mW@1.5V
LNA (HEMT, 2 stages)	1.4–2.6 GHz	25 dB	2.3 dB	15 dBm	
Mixer	Center = 2.4 GHz IF = 250 MHz	-5 dB		5 dBm	8.4 mW @1.5V
Mixer (HBT)	1.4–2.6 GHz	-4 dB	15 dB	0 dBm	
VCO	25.9 GHz 0.6-GHz tuning range		-106 dBc/Hz (phase noise)		24 mW @1.5V
Frequency Divider	1.5–20 GHz 5.9–26.5 GHz				29.5 mW (Core) <20 mW (Core)
Tuned Amplifier	23 GHz 4-GHz Bandwidth	6–7 dB			

as well as a bulk Si control wafer. The devices had a gate length,  $L_g$ , of 100 nm.

The room-temperature Hall mobility and sheet carrier density [7] of the composite-channel layer structure grown on an SOS wafer were 800 to 1200  $\text{cm}^2/\text{Vs}$  and  $3.1\text{--}2.5 \times 10^{12} \text{ cm}^{-2}$  at room temperature, respectively, as shown in Figure 2.

The room-temperature output (transfer) characteristic for 100-nm gate-length devices showed practically no difference between devices fabricated on SOS and Si control devices (Figure 3).

Figure 3 also shows that the best SOS transistor had a maximum extrinsic transconductance of 377  $\text{mS}/\text{mm}$ , which is, to the authors' knowledge, the highest ever reported for alloy-channel p-MODFETs. The device had a corresponding output conductance of 25  $\text{mS}/\text{mm}$  leading to a maximum dc voltage gain of 15. The only apparent degradation of the device performance caused by the SOS substrate was roughly an order of magnitude higher gate-leakage current compared to the Si monitor, a result that we again attribute to the increased defect density of the SOS wafers.

Figure 4 shows frequency-dependent plots [8] of the forward current gain ( $|b_{21}|^2$ ) and the maximum unilateral gain (MUG) for a  $0.1 \times 50 \mu\text{m}^2$  p-MODFET on SOS. Values of  $f_T = 49 \text{ GHz}$  and  $f_{\text{max}} = 116 \text{ GHz}$  were obtained after de-embedding the contact pads; the latter value being the highest  $f_{\text{max}}$  ever reported for a SiGe p-MODFET. Figures 5 and 6 illustrate the fact that  $f_t$  and  $f_{\text{max}}$  saturate at a very low bias voltage;  $f_{\text{max}}$  reached 100 GHz at  $V_{\text{ds}} \sim 0.6 \text{ V}$  and remained sustained over a wide bias range. In Figure 7, the small-signal parametric model reveals non-negligible capacitances ( $C_{\text{pg}}$  and  $C_{\text{pd}}$ ) caused by the incomplete removal of the SiGe buffer layer and Si film in the isolation regions. Through the agreement of the raw data and extracted values, Figure 8 demonstrates the accuracy

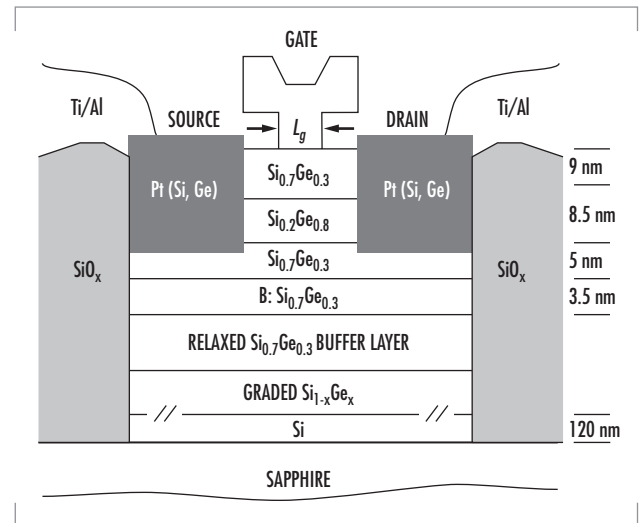


FIGURE 1. Cross-sectional diagram of epitaxial layer structure and p-MODFET device design.

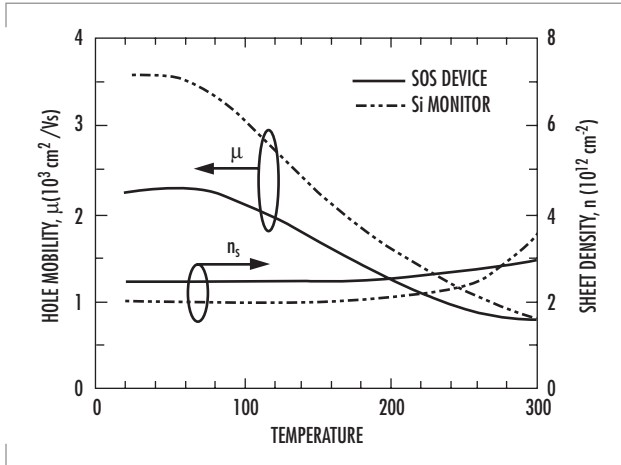


FIGURE 2. Hole mobility and sheet density *vs.* temperature for composite-channel layer structures grown on SOS and Si control wafers.

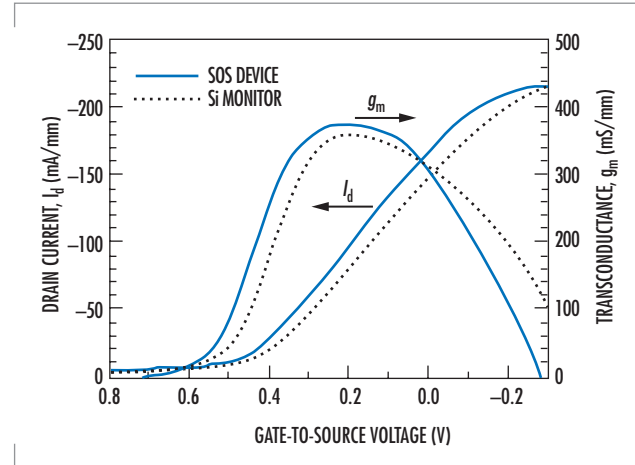


FIGURE 3. Comparison of 0.1- $\mu\text{m}$  composite-channel p-MODFETs on Si and SOS. The bias voltage is  $V_{ds} = -0.6$  V.

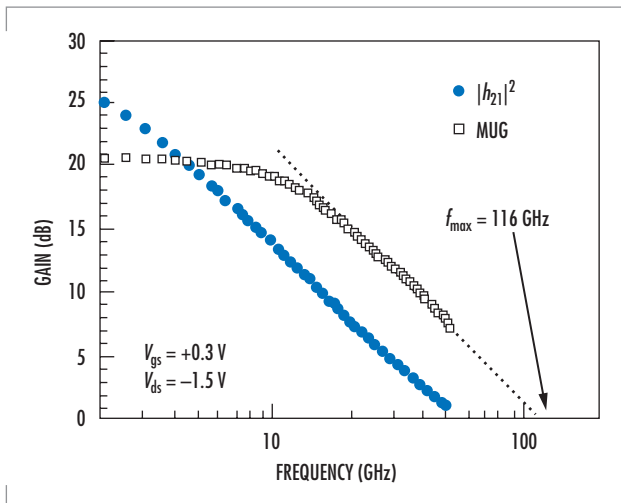


FIGURE 4. Plot of  $|h_{21}|^2$  and MUG *vs.* frequency for a  $0.1 \times 50 \mu\text{m}^2$  composite-channel p-MODFET on SOS. Values of  $f_t = 49$  GHz and  $f_{\text{max}} = 116$  GHz are obtained after open-circuit de-embedding.

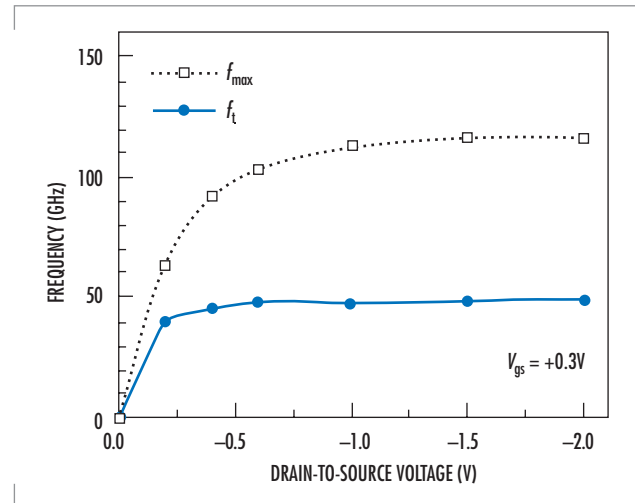


FIGURE 5. Bias dependence of  $f_t$  and  $f_{\text{max}}$ .  $f_t$  and  $f_{\text{max}}$  saturate at a very-low-bias voltage.

of the preliminary device model created from these results. Design of circuits from this model should demonstrate the unprecedented potential of SiGe/TFSOS technology.

Table 2 lists the comparative cost of competing technologies [9, 10, and 11] for the manufacturer and the user.

## CONCLUSION

The incorporation of strained SiGe heterostructures on thin-film silicon-on-sapphire (the device-quality Si film obtained either through SPE or layer bonding) for n- and p-FETs, characterized by superior transport carrier properties, high dynamic performances ( $f_t$ ,  $f_{\text{max}}$ ), and low noise at high frequencies (Figure 9) will enable an entirely new technology. The

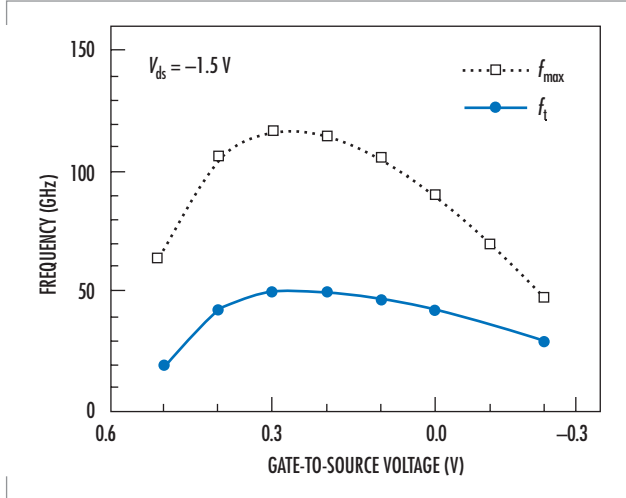


FIGURE 6. Bias dependence of  $f_t$  and  $f_{max}$ . High  $f_{max}$  sustained over wide bias range.

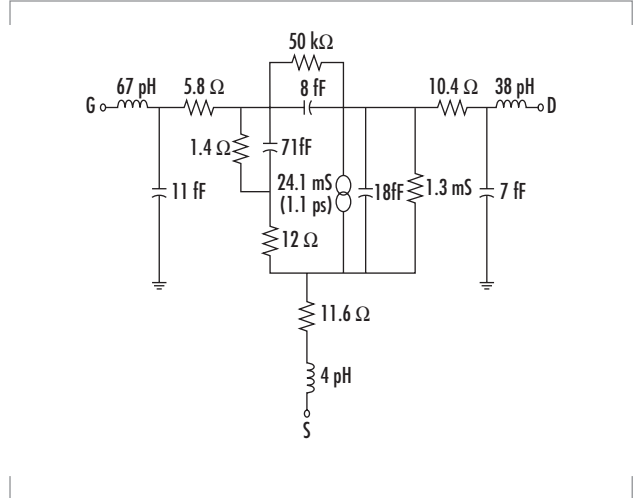


FIGURE 7. Small-signal equivalent circuit. Small-signal parameters reveal non-negligible capacitances ( $C_{pg}$  and  $C_{pd}$ ) from unremoved SiGe buffer layer in isolation regions.

TABLE 2. Relative cost of different technologies as seen by (A) the manufacturer and (B) the user. The difference is due to the different profit margins available to the companies as determined by what the market will bear.

A. Manufacturing Cost [9, 10]					
Si Bulk CMOS	SOS CMOS	Bipolar Si & SOS	SiGe	GaAs MESFET	HBT(GaAs)
1	1.3	3.5		3.5-7	10

B. User Cost [11]	
Technology	Cost per sq. mm (\$US)
Silicon CMOS	0.01
SiGe epitaxy	0.60
GaAs epitaxy	2.00
InP epitaxy	10.00
Tokyo real estate	0.01

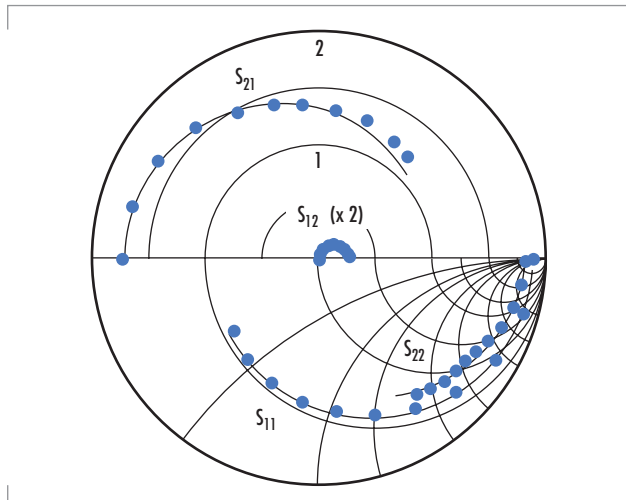


FIGURE 8. Comparison of s-parameter. Good agreement between raw data (points) and extracted values (lines).

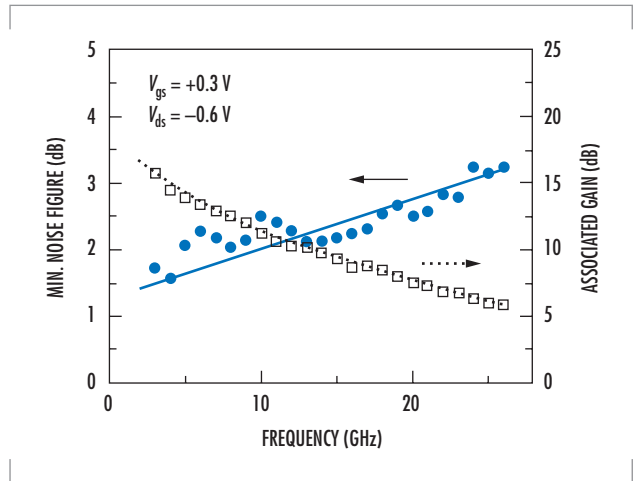


FIGURE 9. Noise parameter results. Values of  $F_{min} = 2.5$  dB and  $G_a = 7.5$  dB obtained at 20 GHz. Low-frequency noise dominated by gate-leakage current.

resulting impact of the combined TFSOS and SiGe technology on the marketplace, both nationally and internationally, will be quite revolutionary because no other material can provide a complementary technology as efficiently, from either the technical or economic aspect.

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