

REPORT DOCUMENTATION PAGE

AFRL-SR-AR-TR-05-

0318

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Service, (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other notice that may appear on this form, it is not intended to impose a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY) 22-07-2005			2. REPORT TYPE Annual Performance Report		3. DATES COVERED (From - To) Sept. 30, 2003 - Sept. 29, 2004	
4. TITLE AND SUBTITLE InAs HVT for extremely low power and high speed applications					5a. CONTRACT NUMBER F49620-01-1-0538	
					5b. GRANT NUMBER F49620-01-1-0538	
					5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S) Wang, Wen I.					5d. PROJECT NUMBER	
					5e. TASK NUMBER	
					5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Columbia University Department of Electrical Engineering 500 W. 120th St. MC 4712 New York, NY 10027					8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) AFOSR/PKC Air Force Office of Scientific Research 875 North Randolph St. Suite 325, Room 3112 Arlington VA 22203 <i>NE</i>					10. SPONSOR/MONITOR'S ACRONYM(S) AFOSR/NE	
					11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release, distribution unlimited.						
13. SUPPLEMENTARY NOTES						
14. ABSTRACT Detailed experiments were carried out to establish the working epitaxial layer structure for the InAs high velocity transistors (InAs HVT). Appropriate InAlAsSb barrier and high purity InAs were incorporated into the final InAs HVT transistor structure. Molecular beam epitaxial (MBE) growth parameters were optimized for the InAs HVT. InAs HVT has been achieved, showing the first such vertical structure with world record transconductance and high speed device parameters. The input, output, and transfer characteristics of an InAs HVT in the common-base configuration were characterized. All the device characteristics were much improved than any previous established results, thus confirming the advantages of the innovative InAs HVT device design.						
15. SUBJECT TERMS						
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON	
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			19b. TELEPHONE NUMBER (Include area code)	

InAs HVT for extremely low power and high speed applications

Annual Performance Report

Contract period: Sept. 30, 2003 - Sept. 29, 2004

Air Force Office of Scientific Research
Contract Number: F49620-01-1-0538

Principal Investigator:

Wen I. Wang
Professor
Department of Electrical Engineering
Columbia University
1312 Mudd, MC 4712
500 W. 120th St.
New York, NY 10027

Summary:

Detailed experiments were carried out to establish the working epitaxial layer structure for the InAs high velocity transistors (InAs HVT). Appropriate InAlAsSb barrier and high purity InAs were incorporated into the final InAs HVT transistor structure. Molecular beam epitaxial (MBE) growth parameters were optimized for the InAs HVT. InAs HVT has been achieved, showing the first such vertical structure with world record transconductance and high speed device parameters. The input, output, and transfer characteristics of an InAs HVT in the common-base configuration were characterized. All the device characteristics were much improved than any previous established results, thus confirming the advantages of the innovative InAs HVT device design.

1. Program Goals

The goals of the program are to achieve extremely high speed (TeraHz) and low power (femto joules) operation of InAs High Velocity Transistor (HVT) by bringing out the best material properties of InAs, including high electron velocity for short transit time and high electron mobility for low base resistance of the transistor.

2. Description of technical work and achievements

During the third year period, i.e., the final year of this program, extensive material efforts by molecular beam epitaxy (MBE) were carried out to achieve suitable device quality MBE layer structures.

The critical barrier material, i.e., InAlAsSb was studied in detail through extensive in-situ reflection high energy electron diffraction and ex-situ X-ray diffraction measurements. Under optimized substrate temperature (460 C), appropriate digital alloy growth produced suitable quality materials for the InAs HVT.

With optimized device design and state-of-the-art quality materials, InAs HVT has been achieved under this program, with device transconductance high than any previous achieved InAs HEMT and HBT-based results. The InAs HVT device parameters achieved under this program are superior than any previous published results for high frequency operation.

The ideal InAs HVT device model are shown in the Fig. 1 (the energy band diagram), Fig. 2 (the equivalent circuit), Fig. 3 (energy band diagram showing partial blocking and partial transmission of the ballistic electrons), and Fig. 4 (output characteristics for the common-base configuration of the InAs HVT).

InAs HVT

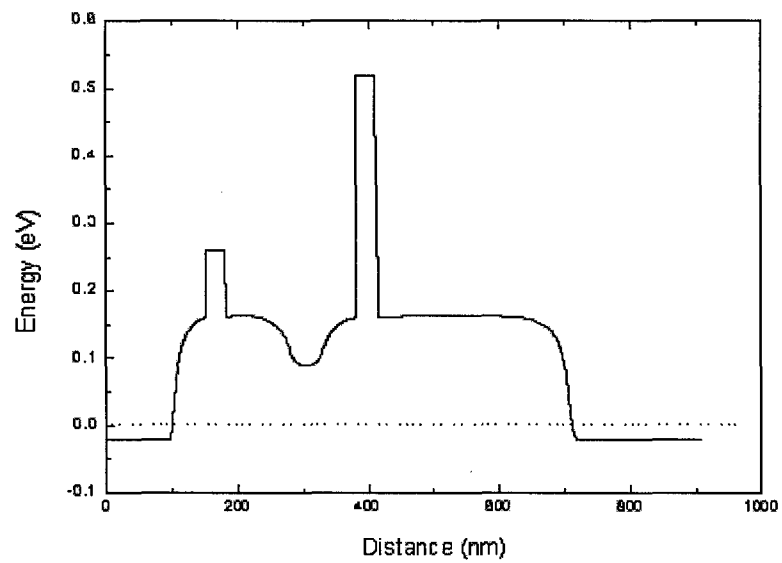


Fig. 1 Energy band diagram of the InAs HVT

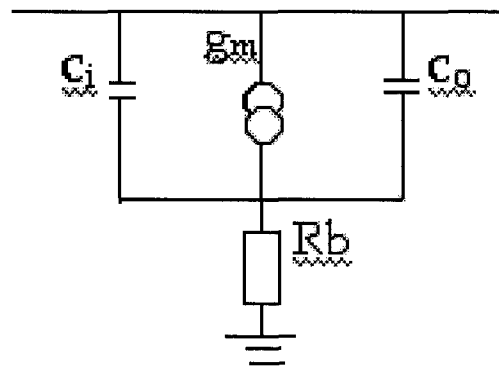


Fig. 2 The equivalent circuit of the InAs HVT as an analog device.

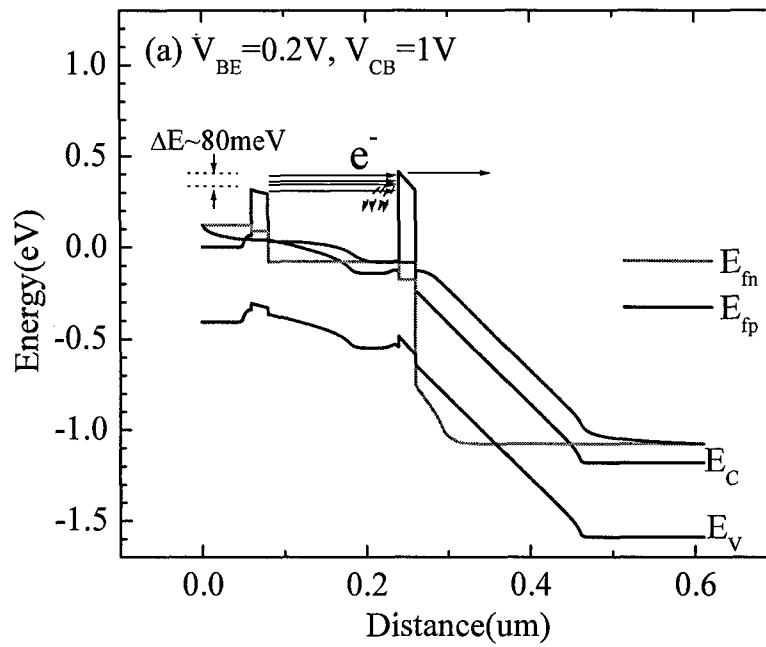


Fig. 3 Energy band diagram showing the InAs HVT operation.

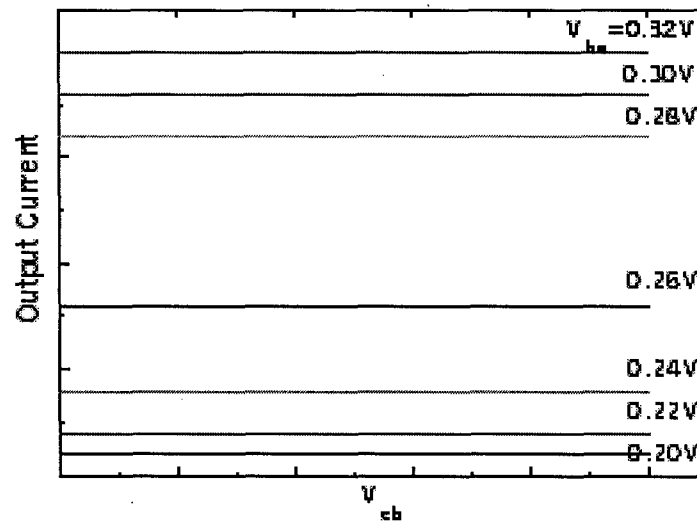


Fig. 4 Common-base output characteristics

Device performance of the InAs HVT

In Fig. 4 shown above, the output characteristics of an InAs HVT in the common-base configuration clearly shows the device advantage of the novel vertical transistor. As can be seen, the input differential resistance is very high because the bias current is determined by the emitter heterojunction barrier height. The actual value of low-frequency short-circuit current gain is determined by the resistance shunting C_i . The current in this shunt represents thermalized electrons in the base region. The actual value of low-frequency open-circuit voltage gain depends on the resistance shunting C_o . The current in this shunt represents direct electron emission over the collector-base barrier. At high frequency, the power gain of the HVT is very high because the input impedance is very high and the transconductance is also very high. Since the InAs HVT can be operated at very low current and power dissipation, its noise figure can be much better than that of any existing HEMT or HBT-based devices at extremely high frequencies.

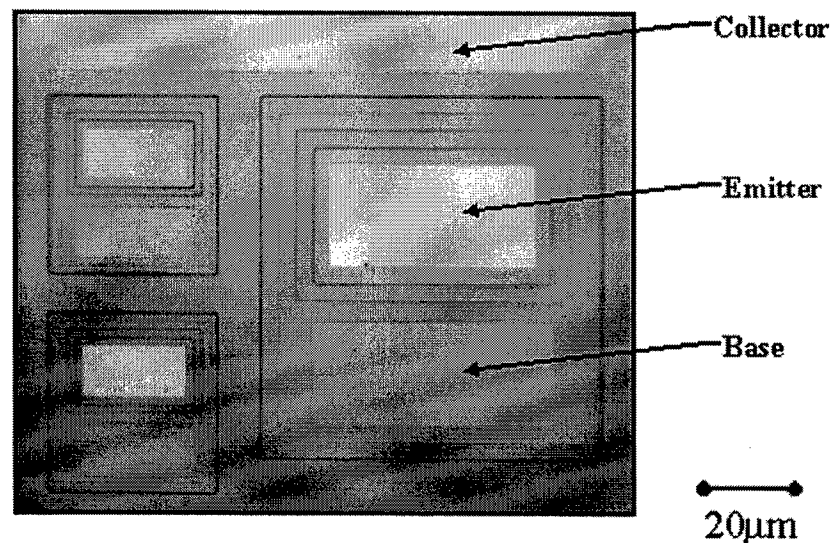


Fig. 5 The mask designed for the InAs HVT

The InAs HVT was grown by MBE and fabricated into a structure with four-level mesas. As shown in Fig. 5, two of which are passivation ledges. Standard photolithography and selective wet chemical etching techniques were employed. After the selective etching, the sample was immediately immersed into a freshly prepared, room-temperature $P_2S_5:(NH_4)_2S_x:H_2O$ passivation solution. The emitter, base, and collector were all contacted from the top using non-alloyed Ti/AuGe.

The transfer characteristics of the InAs HVT are shown in Fig. 6 and Fig. 7. The expected current-voltage characteristics have been achieved. The measured transconductance for a device with $7 \times 14 \mu m^2$ emitter size is as high as 1880 mS/mm at 80 K and 780 mS/mm at 300 K. These are the best device parameters reported so far either for HEMT or HBT-based device structures, thus confirming that the innovative device design of the InAs HVT has brought out the best device parameters of the InAs, i.e., high electron mobility and high electron velocity.

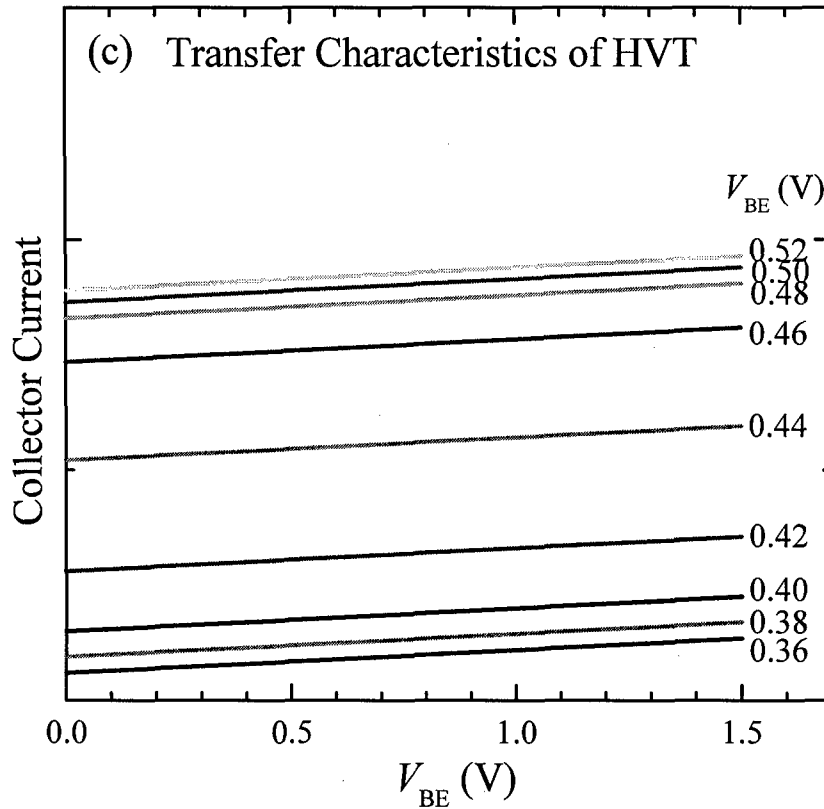


Fig. 6 The transfer characteristics of the InAs HVT at 300K

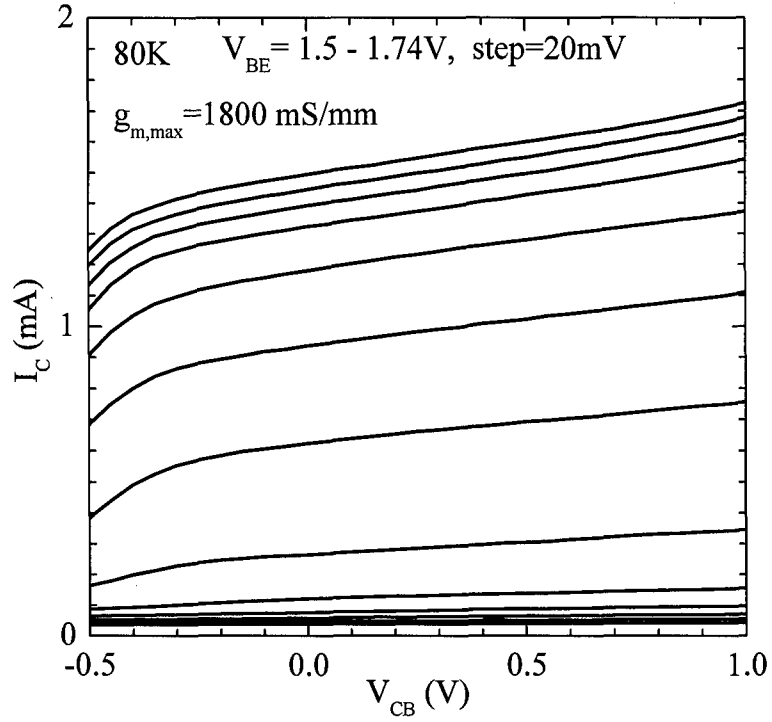


Fig. 7 The transfer characteristics of the InAs HVT at 80K

For analog circuit applications, the maximum frequency of oscillation may be estimated as

$$f_{\max} = \frac{1}{2\pi} \sqrt{\frac{g_m}{C_i C_o R_b}} \quad (1)$$

assuming a matched load impedance and a simple-pole roll-off of the current transfer ratio. In (1), R_b is the base resistance, which is reduced due to the high mobility in InAs and can be 2.5 ohms. With an operating current of 2.5 mA, the transconductance is 0.1 S and $f_{\max} = 3 \text{ THz}$.

For comparison, the performance of the best 0.1-um gate length InGaAs HEMT is

discussed here, using the same equivalent circuit and neglecting all parasitic parameters. The scaled-down 30- μm gate small-signal low-noise device works at $V_{DS} = 2\text{ V}$ and $I_{DS} = 9\text{ mA}$, with $g_m = 26.4\text{ mS}$, $R_S = 5.6\ \Omega$, $C_i = 36\text{ fF}$ and $C_o = 5\text{ fF}$. The calculated $f_{max} = 800\text{ GHz}$, which is consistent with the measured value of 600 GHz. As can be seen, the value of f_{max} for the InAs HVT is 3 times higher than that of the 0.1- μm gate-length HEMT.

3. Personnel supported:

Associated Research Scientist: Dr. S. Xin

Graduate Research Assistants: Y.C. Chen, Weiping Li, and Sheyum Syed

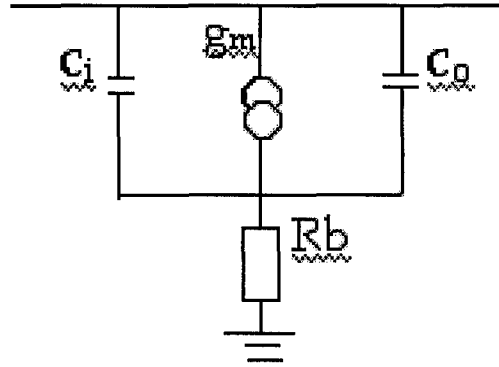


Fig. 13 The equivalent circuit of the InAs HVT as an analog device.

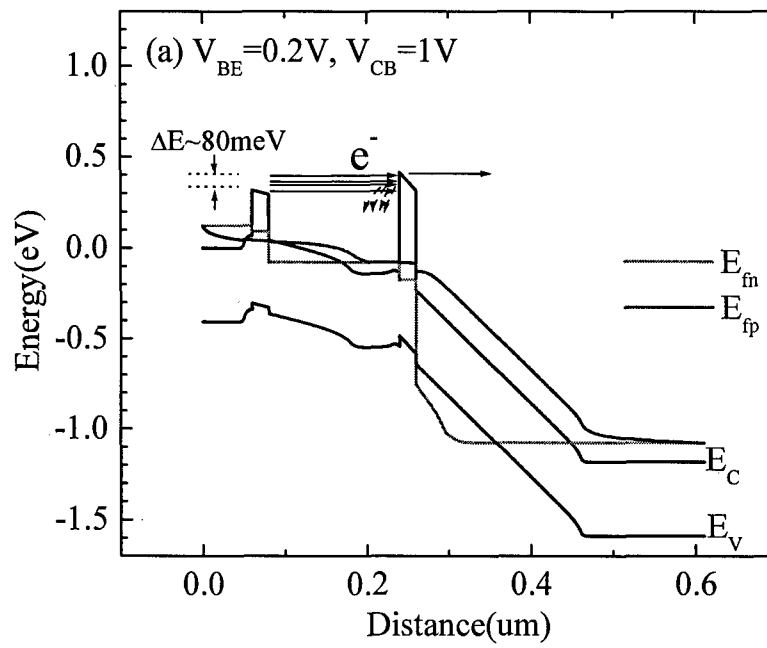


Fig. 14 Energy band diagram showing the InAs HVT operation.

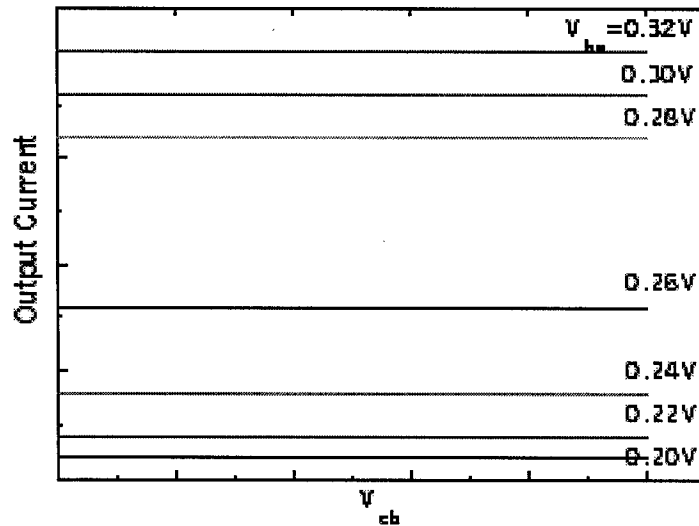


Fig. 15 Common-base output characteristics

Device performance of the InAs HVT

In Fig. 15 shown above, the output characteristics of an InAs HVT in the common-base configuration clearly shows the device advantage of the novel vertical transistor. As can be seen, the input differential resistance is very high because the bias current is determined by the emitter heterojunction barrier height. The actual value of low-frequency short-circuit current gain is determined by the resistance shunting C_i . The current in this shunt represents thermalized electrons in the base region. The actual value of low-frequency open-circuit voltage gain depends on the resistance shunting C_o . The current in this shunt represents direct electron emission over the collector-base barrier. At high frequency, the power gain of the HVT is very high because the input impedance is very high and the transconductance is also very high. Since the InAs HVT can be operated at very low current and power dissipation, its noise figure can be much better than that of any existing HEMT or HBT-based devices at extremely high frequencies.

The InAs HVT was grown by MBE and fabricated into a structure with four-level mesas. As shown in Fig. 11, two of which are passivation ledges. Standard photolithography and selective wet chemical etching techniques were employed. After the selective etching, the sample was immediately immersed into a freshly prepared, room-temperature $P_2S_5:(NH_4)_2S_x:H_2O$ passivation solution. The emitter, base, and collector were all contacted from the top using non-alloyed Ti/AuGe.

The transfer characteristics of the InAs HVT are shown in Fig. 16 and Fig. 17. The expected current-voltage characteristics have been achieved. The measured transconductance for a device with $7 \times 14 \mu m^2$ emitter size is as high as 1880 mS/mm at 80 K and 780 mS/mm at 300 K. These are the best device parameters reported so far either for HEMT or HBT-based device structures, thus confirming that the innovative device design of the InAs HVT has brought out the best device parameters of the InAs, i.e., high electron mobility and high electron velocity.

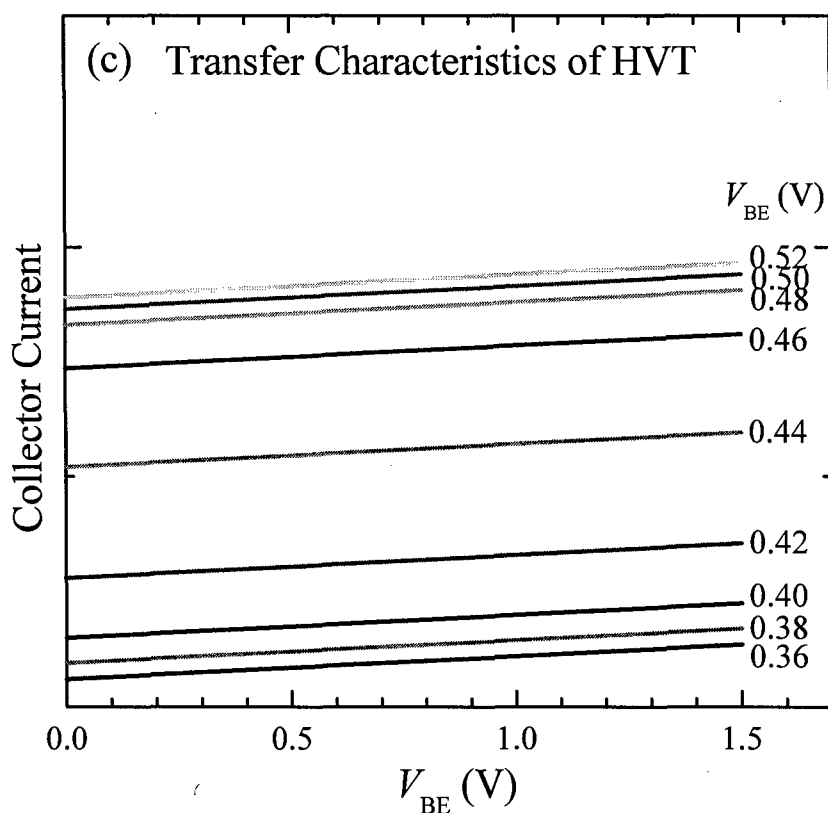


Fig. 16 The transfer characteristics of the InAs HVT at 300K

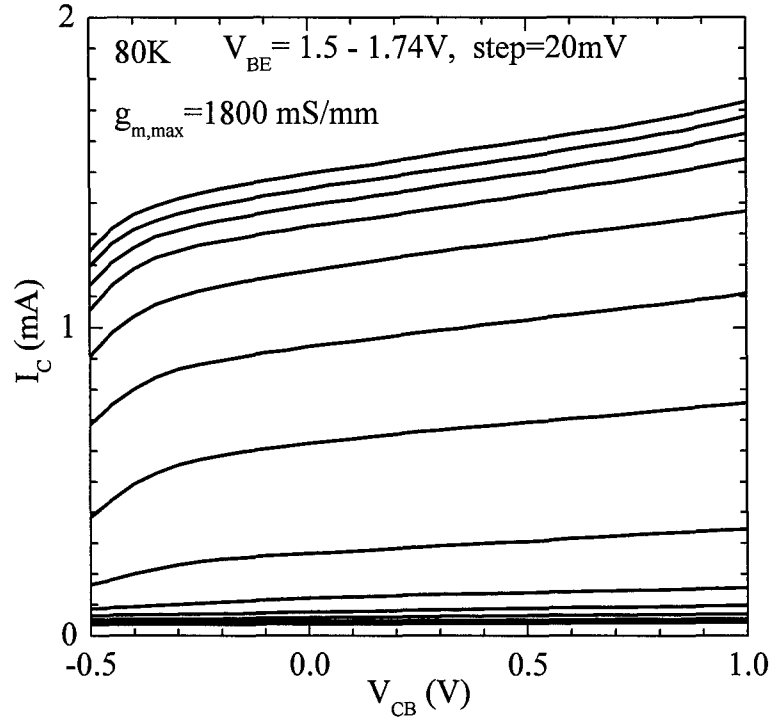


Fig. 17 The transfer characteristics of the InAs HVT at 80K

For analog circuit applications, the maximum frequency of oscillation may be estimated as

$$f_{max} = \frac{1}{2\pi} \sqrt{\frac{g_m}{C_i C_o R_b}} \quad (1)$$

assuming a matched load impedance and a simple-pole roll-off of the current transfer ratio. In (1), R_b is the base resistance, which is reduced due to the high mobility in InAs and can be 2.5 ohms. With an operating current of 2.5 mA, the transconductance is 0.1 S and $f_{max} = 3 \text{ THz}$.

For comparison, the performance of the best 0.1- μm gate length InGaAs HEMT is discussed here, using the same equivalent circuit and neglecting all parasitic parameters. The scaled-down 30- μm gate small-signal low-noise device works at $V_{DS} = 2\text{ V}$ and $I_{DS} = 9\text{ mA}$, with $g_m = 26.4\text{ mS}$, $R_S = 5.6\ \Omega$, $C_i = 36\text{ fF}$ and $C_o = 5\text{ fF}$. The calculated $f_{max} = 800\text{ GHz}$, which is consistent with the measured value of 600 GHz. As can be seen, the value of f_{max} for the InAs HVT is 3 times higher than that of the 0.1- μm gate-length HEMT.

3. Personnel supported:

Associated Research Scientist: Dr. S. Xin

Postdoctoral Scientist: Dr. Jean Heroux

Graduate Research Assistants: Y.C. Chen, Hui Shao, Julian Sweet, Steve Yang