REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	27 September 2005	Final Progress Report: 8/20/01 – 5/19/05

4. TITLE AND SUBTITLE
Three-Dimensional Nano-Lithography for Emerging Technologies

5. FUNDING NUMBERS
DAAD19-01-1-0727

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8. PERFORMING ORGANIZATION REPORT NUMBER
ELEG332134 - 092704

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U. S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
42872.1-PH-DRP

11. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.

12 a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)
Grayscale lithography has shown particular success in the pursuit of surface machining capabilities because of the flexibility and convenience it offers in the fabrication of arbitrary three-dimensional surfaces. Accordingly, grayscale lithography has been demonstrated for a wide range of applications, including refractive and diffractive optical elements for focusing and beam shaping, optical interconnects, and MEMS.

While our original motivation for this research area was the fabrication of three different micro-optical devices that would enable novel photonic devices, our efforts and results went considerably beyond that modest goal. Thus, in addition to demonstrating a gray-scale coupling device and tilted mirrors, we designed and realized other approaches to coupling light from an optical fiber, fabricated a retro-reflector for the holographic exposure of three-dimensional photonic crystals, designed and realized compound-angle micro-prisms for arbitrary beam steering to enable free-space optical interconnection on a chip scale, produced a large-area blazed grating on a convex lens for space-based spectrometer, and fabricated numerous diffractive optical elements, such as high-efficiency lenses, for a variety of applications. We also developed a novel concept of an optical die for high-density interface between optical-fiber cable and chip-scale photonic circuitry, and demonstrated its feasibility by fabricating a prototype.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Grayscale lithography, micro- and nano-fabrication, 3D micro-machining, nanolithography	10
	16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION ON THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	**UNCLASSIFIED**	**UNCLASSIFIED**	**UL**

NSN 7540-01-280-5500

Standard Form 298 (Rev.2-89)
Prescribed by ANSI Std. 239-18
298-102

Three-Dimensional Nano-Lithography for Emerging Technologies

Dennis W. Prather

Foreword

Micro-optics, in particular diffractive and meso-optics for optical system integration, and the burgeoning field of micro-electro-mechanical systems (MEMS), provide drive in the micro- and nano-machining fields. This is due in part to their offering reduction in fabrication costs, improvement in performance, and opening of new areas of application. A number of techniques exist and others are being developed for machining devices for these applications. The goal is to produce arbitrary material topographies that provide useful optical, electronic, and mechanical functionality. For example, computer generated holograms, lenses, photonic crystals, optical couplers, gears, motors, micro-fluidics, and other such devices are all enabled by micro-machining capabilities.

Grayscale lithography has shown particular success in this pursuit of surface machining capabilities because of the flexibility and convenience it offers in the fabrication of arbitrary three-dimensional surfaces, while borrowing tried-and-true fabrication techniques from the well-established silicon integrated circuit fabrication technology. The utility of grayscale lithography has been demonstrated for a wide range of applications, including refractive and diffractive optical elements for focusing and beam shaping, optical interconnects, and MEMS. Many applications would be difficult to conceive without the capabilities extended by grayscale lithography.

While our original motivation to enter this research area lay in the fabrication of three different micro-optical devices that would enable novel photonic devices, our efforts, and results, went considerably beyond that modest goal. Thus, in addition to demonstrating a gray-scale coupling device and tilted mirrors, we designed and realized other approaches to coupling light from an optical fiber, fabricated a retro-reflector for the holographic exposure of three-dimensional photonic crystals, designed and realized compound-angle micro-prisms for arbitrary beam steering to enable free-space optical interconnection on a chip scale, produced a large-area blazed grating on a convex lens for space-based spectrometer, and fabricated numerous diffractive optical elements, such as high-efficiency lenses, for a variety of applications. We also developed a novel concept of an optical die for high-density interface between optical-fiber cable and chip-scale photonic circuitry, and demonstrated its feasibility by fabricating a prototype.

This effort resulted in two masters' theses, numerous papers published in scientific literature, and presentations at conferences devoted to micro- and nano-fabrication and micro-optics. More importantly, we developed technology for fabricating arbitrary relief structures in both polymers and semiconductor materials with nano-scale fidelity. This propelled us to become an enabler of research efforts pursued at other research institutions focusing on the development of devices for both civilian and military applications, and allowed us to undertake other projects that required gray-scale patterning capability.

In all, the project was a resounding success in developing the technology and the expertise in a unique lithography method as required for the continuing progress in photonic interface and integration.

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PROBLEM STUDIED

The object of the work performed under this grant was twofold. First, it was to develop and refine gray-scale electron-beam lithography and associated processes to realize arbitrary three-dimensional surfaces. Second, it was to demonstrate the capabilities of the process by demonstrating devices for coupling light between an optical fiber and a chip-scale integrated photonic device, and devices for three-dimensional routing of optical signals on a chip scale. Thus, the ultimate goal is the demonstration of a viable technology capable of realizing devices vital for the optical communication in an integrated circuit, and between the circuit and outside world. The challenge lied in having control over the geometry of the surface profiles down to few tens of nanometers, which is essential for achieving operational characteristics compatible with the requirements of the envisioned applications.

SUMMARY OF MOST IMPORTANT RESULTS

Accordingly, the results can be divided into two classes: those dealing with the process development, and the demonstration of particular devices realized using the process.

Results in process development

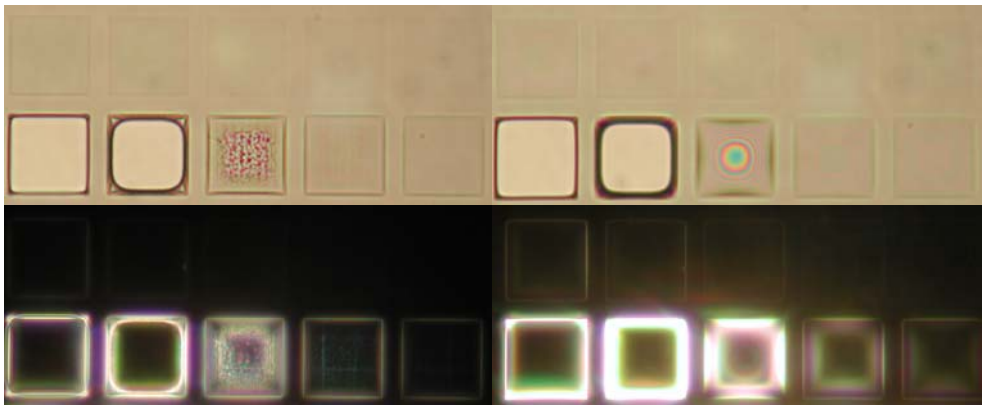

Figure 1. Comparison of gray scale lithography immediately after development with the same structures subjected to post-development bake.

In the early stages of the project, we realized that if the method were to be viable, we had to bring under control the surface roughness that results when the resist is essentially underexposed to achieve the desired three-dimensional topography. While the origin of the roughness is still a subject of a debate, we overcame the problem by suitable post processing. The results are shown in Fig. 1 where it is clear that post-development bake smoothes out the roughness visible after the development. At the same time, the bake does not compromise the resolution, so the small features exposed with the electron beam are preserved in the final structure. This can be seen in Fig. 2 where the small features look almost identical before and after the post-development bake.

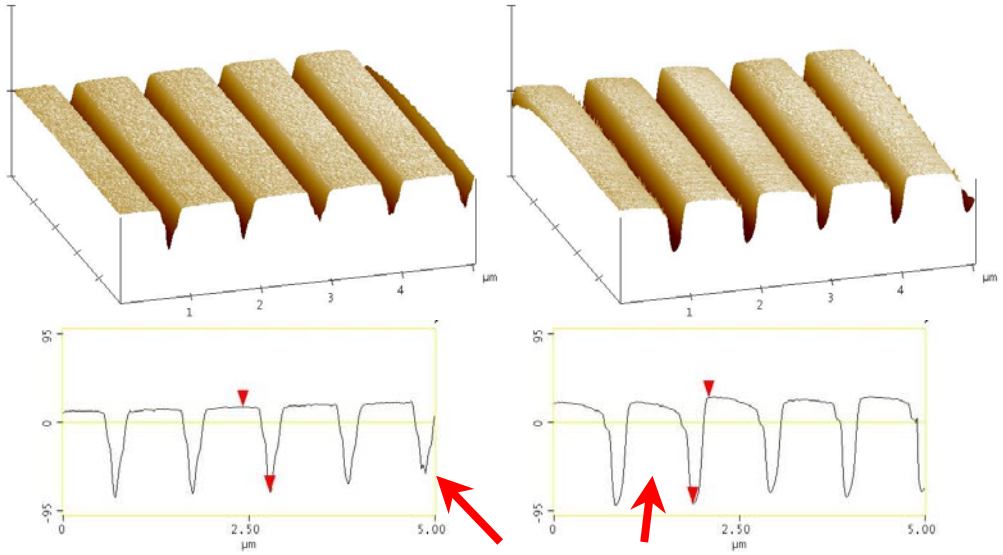

Figure 2. Small features exposed with electron beam are preserved during the post-development bake.

Further refinement of the process required considerable effort in understanding the processes taking place during the exposure, that is the interaction of the high-energy electrons penetrating the material with the molecules, as well as the dynamics of the development of the exposed resist. Figure 3 shows the distribution of energy deposited inside material by electron beam with accelerating potential of 30 kV. This energy distribution is equivalent to the local dose received by the e-beam sensitive material. The understanding of the involved physics enabled the tackling of the optimization of the process that would allow us to arrive at the desired surface profile. To this end, we developed a set of custom computer programs where the dose is calculated using realistic simulations of the electron interactions and the development dynamics to iteratively approach the designed topography.

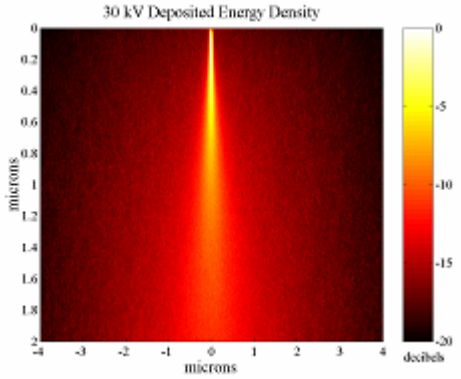

Figure 3. Energy deposited in material by a beam of electrons accelerated to the energy of 30 keV. The result was obtained by Monte Carlo simulation of individual electron trajectories.

Demonstrated devices

The realized devices included the following.

Tapered couplers

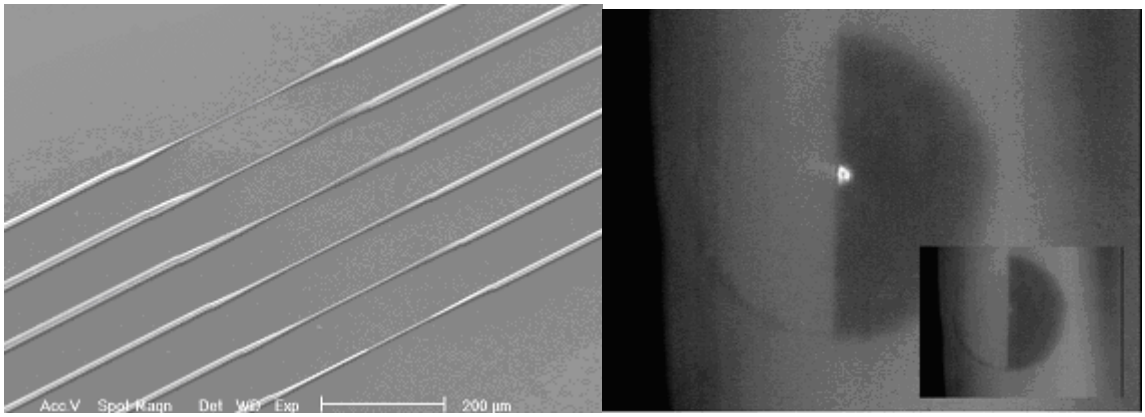

Figure 4. Tapered couplers and their performance. Left figure shows an SEM micrograph of the structure. Right figure shows light at the output of one of the tapers. They are used to couple light from an optical fiber to an integrated photonic device.

Compound-angle prisms

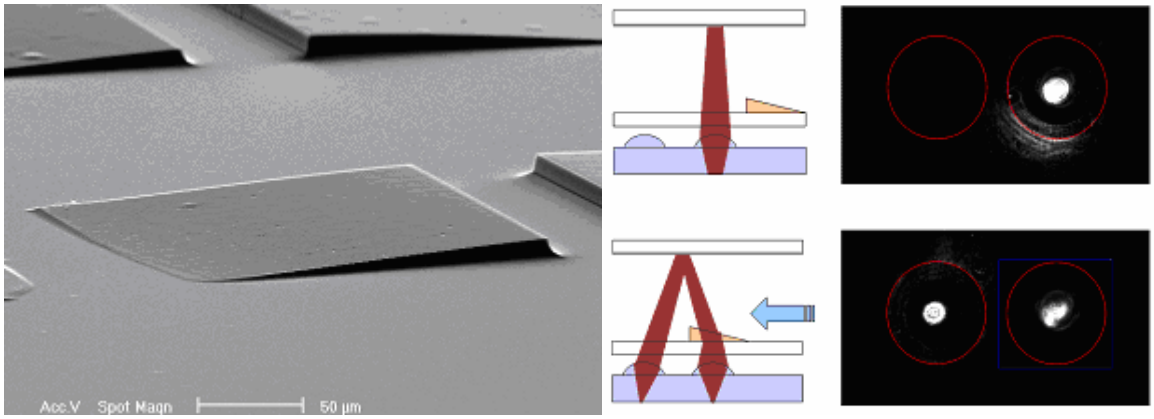

Figure 5. Compound-angle prisms. Used for redirecting beam in arbitrary directions for optical communication on a chip. Left picture shows a micrograph of the realized devices, the right figure shows a conceptual drawing of the operational principle, and the optical performance of the complete structures.

Vertical J-coupler

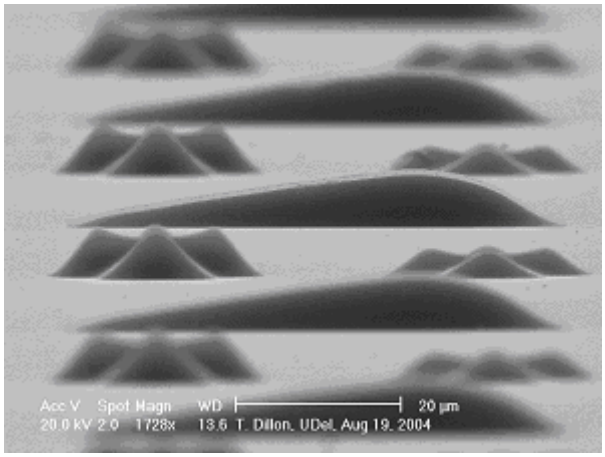

Figure 6. Vertical J-coupler. It is used to couple light from an optical fiber to a planar integrated photonic device. It converts the wide, 10-mm beam of a single-mode optical fiber into a few-hundred-nanometer wide mode of a single-mode slab waveguide. The input fiber is perpendicular to the surface of the photonic chip.

Optical die

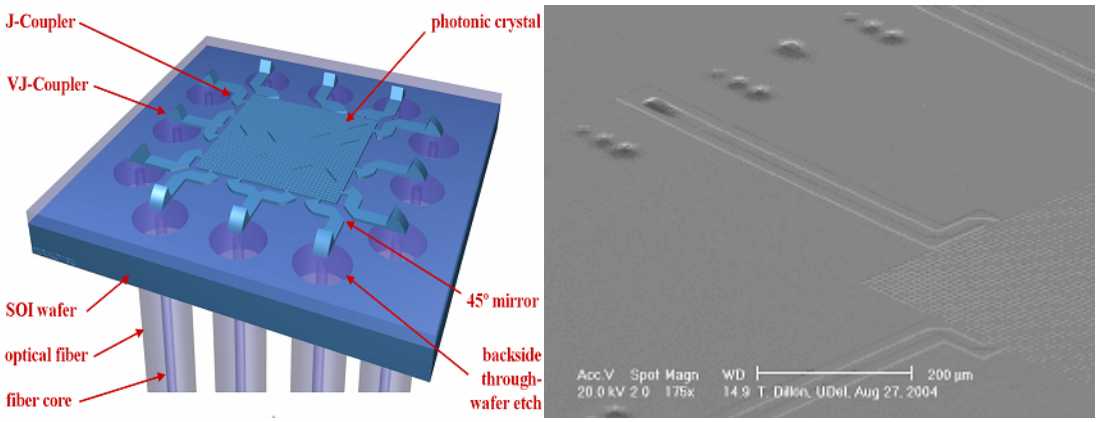

Figure 7. Conceptual drawing of an optical die (left) and its realization (right). Visible in the figure on the right is a vertical J-coupler, alignment marks, and a photonic circuit where wide waveguides are used to interface the vertical J-couplers with planar J-couplers that, in turn, couple light into the photonic circuitry.

Diffractive lenses

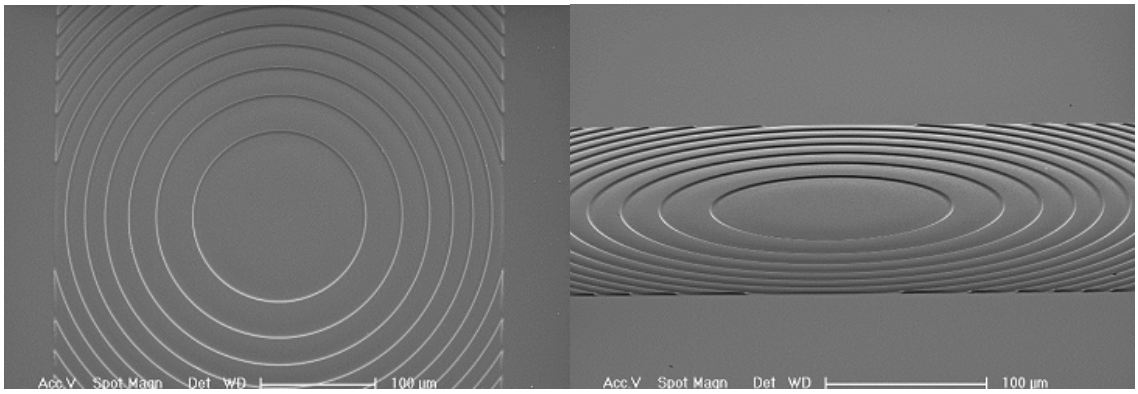

Figure 8. High-quality diffractive (zone) lenses realized with gray-scale lithography.

Retro-reflector

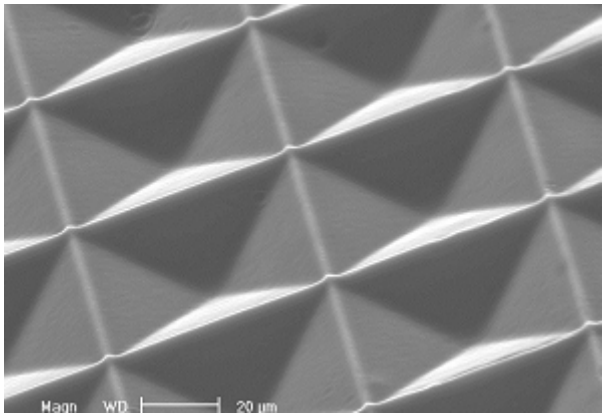

Figure 9. Inverted pyramid structures used as retroreflectors for the exposure of three-dimensional photonic crystals.

LIST OF PUBLICATIONS SUPPORTED BY THIS GRANT

Published in peer reviewed journals

"Fabrication and characterization of three-dimensional silicon tapers", Anita Sure, Thomas Dillon, Janusz Murakowski, Chunchen Lin, David Pustai and Dennis W. Prather, Optics Express, December, 2003.

"Continuous-Tone Grayscale Mask Fabrication using High-Energy-Beam-Sensitive (HEBS) Glass," Thomas Dillon, Anita Balcha, Janusz Murakowski, and Dennis Prather, Journal of Microlithography, Microfabrication, and Microsystems, October 2004.

"Optical Interconnects: A Potential Solution to the Intrachip Interconnect Problem?", Michael W. Haney, Michael J. McFadden, Muzammil Iqbal, Dennis W. Prather, and Thomas Dillon, IEEE LEOS Newsletter, June 2005, pp 15 -17.

Published in conference proceedings

"Novel Coupling Structures for Photonic Crystal Devices", Thomas Dillon and David Pustai, IPR 2002, Vancouver.

"Process development and application of grayscale lithography for efficient three-dimensionally profiled fiber-to-waveguide couplers", T. Dillon, A. Balcha, J. Murakowski, Dr. Prather, SPIE 48th Annual Meeting, San Diego, August 3, 2003.

"Three-Dimensionally Profiled Optical Couplers Fabricated by Grayscale Lithography", Thomas Dillon, Anita Sure, Janusz Murakowski and Dennis W. Prather, IPR 2003, Washington, DC.

"Vertical J-coupler for Optical Systems Integration", Thomas Dillon, Janusz Murakowski, Caihau Chen, Anita Balcha, and Dennis Prather, MOC'04, 10th Microoptics Conference, Jena Germany, September 1, 2004.

"Towards demonstrating multi-scale free-space optical interconnects for intrachip global communication", Proceedings of OSA 88th Annual Meeeting: Frontiers in Optics/Laser Science, Rochester, NY, October 2004.

Presented at meetings but not published in proceedings

”Grayscale Lithography with the Raith50 E-beam Lithography Tool”, Thomas Dillon, NANO2004, 10th Workshop on SEM-based E-beam Lithography, Dortmund, Germany, February 17, 2004.

Manuscripts submitted but not published

“10GBps, Three-Dimensional Parallel Optical Interconnects Using A Novel Conductive Polymer Flip-Chip Process”, S.K. Lohokare, C.A. Schuetz, Z. Lu, T. Dillon, A. Sure, and D.W. Prather, Optical Engineering, accepted for publication.

Technical reports

“Three Dimensional Nano-Lithograpy for Emerging Photonic Technologies”, Dennis Prather, Janusz Murakowski, Tom Dillon, Anita Sure, Hermann Raith, Advanced Lithography Program Review, Santa Fe, NM, May 7, 2003.

“Three Dimensional Nano-Lithography for Emerging Photonic Technologies”, Dennis Prather, Janusz Murakowski, Tom Dillon, Anita Sure, Hermann Raith, Advanced Lithography Program Review, Las Vegas, NV, February 3, 2004.

PERSONNEL AWARDED MASTER DEGREE UNDER THIS PROJECT

Thomas Dillon. Master Degree, University of Delaware, 2005.
Anita Sure. Master Degree, University of Delaware, 2004.