# HIGH-END CMOS ACTIVE PIXEL SENSORS FOR SPACE-BORNE IMAGING INSTRUMENTS

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**RÉSUMÉ :** Les capteurs optiques intégrés sont utilisés dans le domaine spatial dans un large éventail d'applications. Beaucoup d'entres elles reposent toujours sur la technologie CCD, alors que les capteurs CMOS à pixel actifs (APS) ont des nombreux avantages pour des applications embarquées. Cette publication présente des capteurs CMOS hautes performances d'aujourd'hui et met en lumière leurs avantages par rapport à leur équivalent CCD. Ces capteurs sont issus de réflexions et de développements menés par FillFactory sur la base de collaborations avec l'Agence Spatiale Européenne et d'actions en partenariat avec le CNES et Alcatel Space.

**ABSTRACT:** Solid-state optical sensors are used in the space environment for a wide range of applications. Many applications still rely on charge coupled device (CCD) technology, but CMOS active pixel sensors (APS) offer great promise for use in space-borne imaging instruments. This paper highlights present-day high-end CMOS APS sensors and sketches their advantages with respect to their CCD counterparts. These advantages are illustrated with Fillfactory analysis and ongoing developments resulting from collaborations with ESA and partnerships with CNES and Alcatel Space.

## 1 INTRODUCTION

Mainstream technology for space imaging application is still CCD. Optical requirements are stringent: high quantum efficiency and fill factor over a wide spectral range, low noise, low defects and high resolution. Despite a continuous effort in developing and optimizing CCD technology, it remains a specialized process and thus doesn't benefit of CMOS technology dynamism [1]. Because of that, CMOS APS becomes a viable alternative for more and more space applications.

Today, optical sensors are the core components in applications like earth and planetary (hyperspectral) imaging, lander and rover imaging, robotics, spacecraft optical guidance and navigation (attitude and orbit control systems (AOCS)), etc [2,3]. Some years ago, many developments were started to investigate how CMOS APS could replace CCDs in several low to medium end space imaging applications. These developments were driven by the idea that those applications could cash-in on CMOS APS's inherent advantages over CCDs:

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- Lower system cost: low power operation on a single power supply, on-chip integration of analog circuitry and digital functionality, lower direct processing cost, system dimensions and mass, etc.
- Faster technological progress: large area devices (yield) and higher speed.
- Compared to the charge transfer mechanism in CCDs:
    - Access to individual pixels or windows is greatly simplified and sped up. This is required in applications where simultaneous tracking of several objects at high frame rate is needed (e.g. star trackers, robotics).
    - Radiation tolerance and absence of CCD-like transfer losses.

# 2 CMOS APS POTENTIAL APPLICATIONS

For a long time, it was expected that high-quality scientific imaging would remain out of reach for CMOS sensors since they lacked the required performance in noise, non-uniformity and dark signal levels and hence could not compete with high-end scientific CCDs offering high quantum efficiency, large dynamic range and special operation modes as Time Delay Integration (TDI) and binning. However, CMOS imaging performs better than expected and gets into domains where CCDs are even not feasible. The following paragraphs describe several types or CMOS detector architectures, some of these being already in development, for different type of space applications:

- High resolution pushbroom imaging instrument
- Hyperspectral cameras
- Step and stare imaging instruments
- Cameras for AOCs and scientific missions

## 2.1 PUSHBROOM TDI CAPABILITY

Linear detectors operating in TDI mode is one of the key technology of high resolution imaging pushbroom instruments (Figure 2.1).

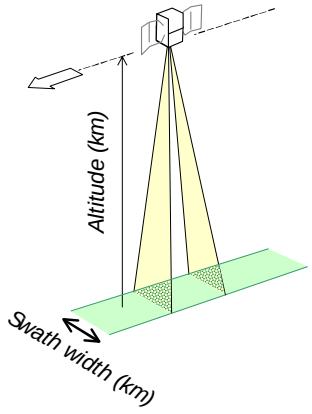


*Figure 2.1 - Pushbroom instrument principle.*

For such applications, the detector is usually a CCD sensor. Signal at the output of the sensor is the result of the accumulation, in charge domain, of many acquisition of the same scene via different pixels. This mode allows better radiometric performances when incoming light power is low and the scene not stable, as the shot noise grows with the square root of the signal

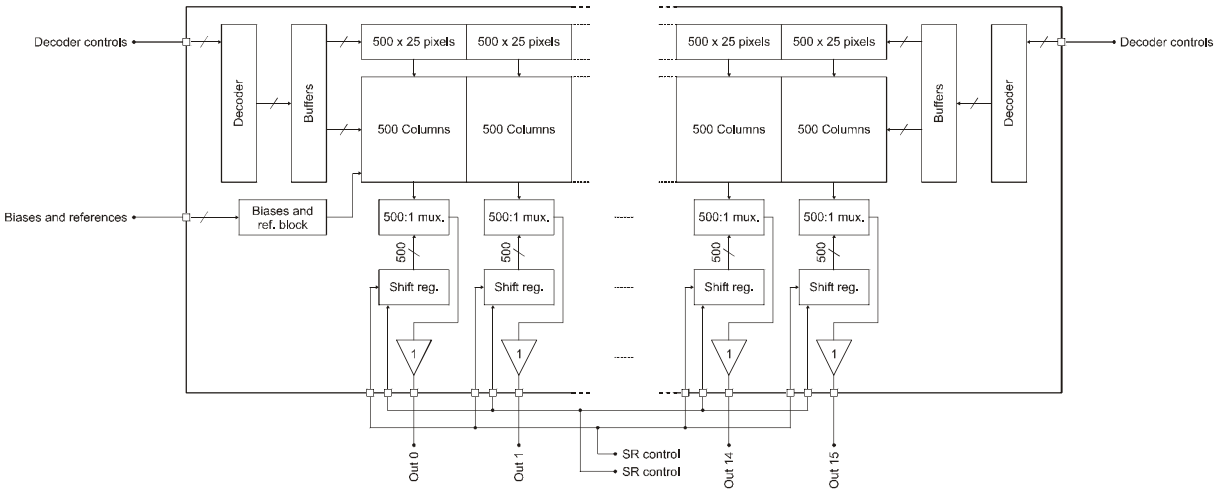


*Figure 2.2 - TDI APS floor plan.*

Such a detector concept could also be envisaged with CMOS technology. Unlike CCD's, signal summation should take place outside the pixel in the voltage domain. In order to keep the noise floor low, careful design of the column circuitry is mandatory. The sensor may be as large as 8000 pixels wide and up to 25 rows could be used in TDI mode (Figure 2.2). As the sensor is larger than the reticle size, stitching technique is necessary to process it.

Although implementation of the TDI summation is significantly more complex on a CMOS APS compared to CCD's, the cost should be dramatically reduced. Target technology is easily accessible and only low voltage sources are required, making the system design easier. Power consumption would be low (0.5 W compared to several watts), and the CMOS technology is inherently more resistant to radiation.

## 2.2 RADIOMETRIC PERFORMANCE ENHANCEMENT OF ACTIVE PIXEL SENSORS

In this paragraph, we present a development under ESA contract in collaboration with Imec, Belgium, for a high-end CMOS APS sensor optimized for hyperspectral imaging (Figure 2.3) in space [4].

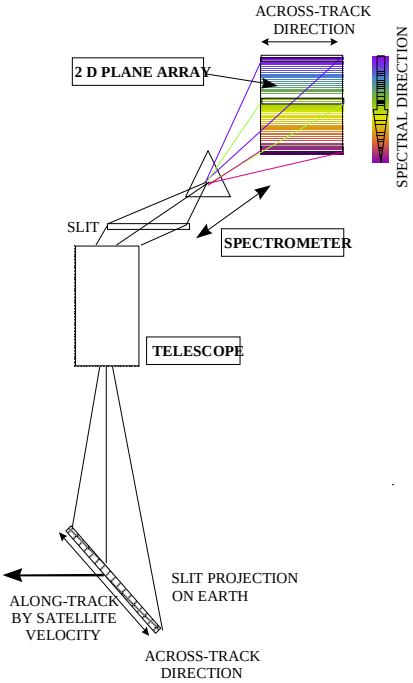


*Figure 2.3 – Principle of hyperspectral imaging.*

The CMOS sensor combines two main technology developments:

- Backside thinning and hybridization to achieve the highest possible quantum efficiency with optimization of several post-processing steps like anti-reflective coating for a broad wavelength range and techniques for cross talk reduction..
- On-chip in-pixel correlated double sampling for low noise operation, combined with synchronous shutter operation.

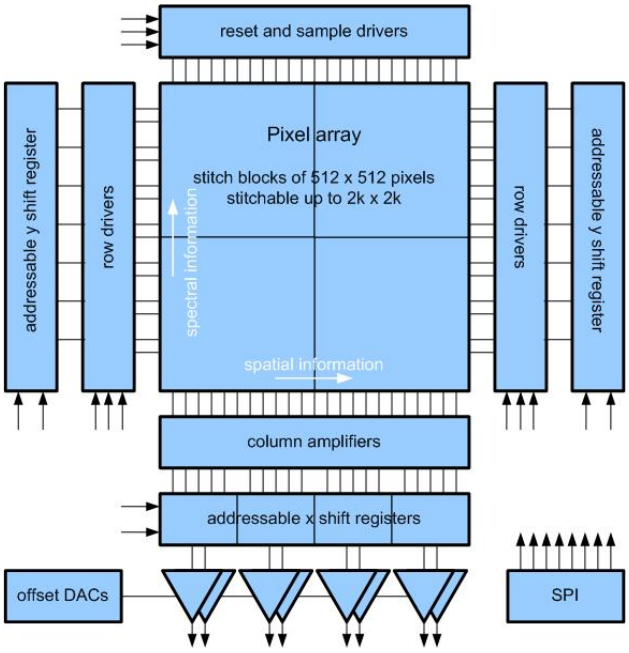


*Figure 2.4 - Sensor architecture.*

Figure 2.4 shows the architecture of the readout sensor. The pixel pitch is 22.5 µm in both X and Y direction. Since the size of the device is larger than the reticle size, the sensor also requires the stitching technique in which smaller blocks are repeated on the wafer. The pixel array consists of stitch blocks of 512 by 512 pixels and is stitchable up to 2048 by 2048 pixels. Hence, the resolution of the pixel array is not fixed. Columns are multiplexed in groups of 256 to a pseudo differential output (signal and reference output). Each output runs at a maximum readout frequency of 20 Mpixels/s. The whole sensor is designed using proprietary techniques to achieve high radiation tolerance.

The readout sensor as shown in Figure 2.4 is implemented for the use in a hybrid approach but has also the possibility to be used as a monolithic, backside thinned, backside illuminated image sensor on its own. In the hybrid approach, the readout circuit is combined with hybrid Si diodes processed on wafers that are afterwards thinned, diced and flip-chipped on the readout sensor using 10 µm Indium bump technology.

The pixel consists out of two stages: a light detecting stage and a sample and hold stage with three storage capacitors. This architecture, as shown in Figure 2.5, allows for a true pipelined synchronous shutter with on-chip correlated double sampling (CDS), i.e. all pixels start and stop integration at the same moment while the previous frame is still read out.

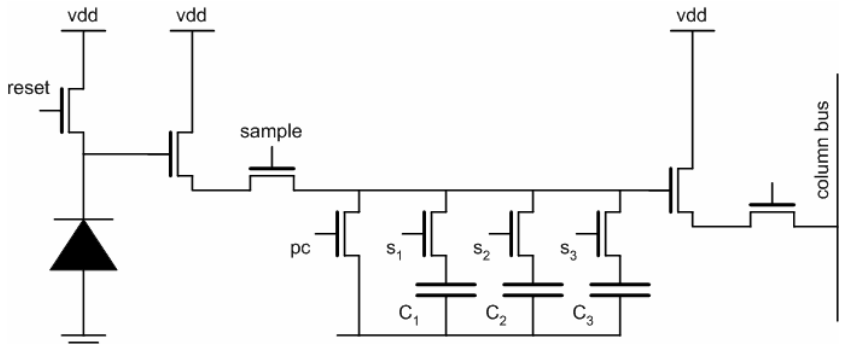


*Figure 2.5 - Snapshot shutter pixel with 3 storage capacitors.*

The pixel readout noise is determined by the size of the storage capacitors. The three capacitors, made by poly on diffusion, occupy about 70 % of the pixel area and equal each 350 fF. The photodiode capacitance is about 15 fF in case of the monolithic sensor and can vary from 25 fF to more than 1 pF in the hybrid approach. It allows for different operations of readout to cope with a large dynamic range, i.e. non-destructive readout, line-by-line variable integration time and in case of hybridization the possibility to optimize the pixel capacitance for each wavelength.

## 2.3 LOW PARASITIC LIGHT SENSITIVITY SYNCHRONOUS SHUTTER APS

CMOS technology is compatible with large size 2D detectors which are of particular interest for instrument operating in “stare” or “step & stare” mode (Figure 2.6). This type of instrument would be compatible with high resolution imaging systems, even in the case of microsatellite with low performance attitude and control orbit subsystem.

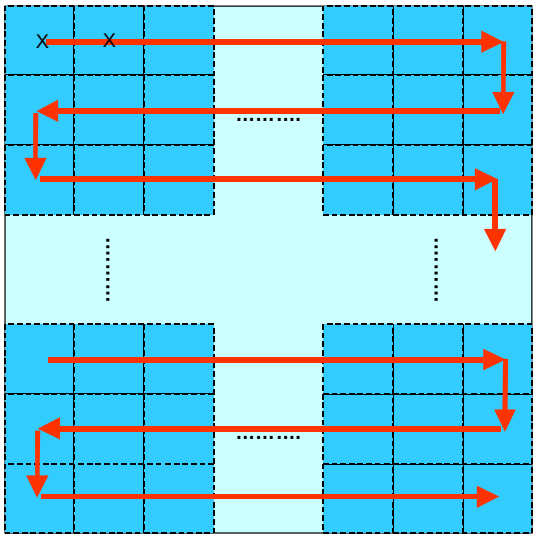

*Figure 2.6 – Step & stare scanning principle.*

As explained in paragraph 2.1, high resolution earth observation instruments use preferably CCD TDI devices in pushbroom mode. However, acquisition could also be done with 2D high resolution CCD arrays. Because a long read out time is needed to dump a full image, a mechanical shutter is required to stop integration during frame read out. This function could be implemented at the device level with CMOS APS, simplifying the system design and suppressing shutter failure risk.

FillFactory has already developed several snapshot detectors with such requirements. Because the sensor is much larger than the reticle, stitching technique is again essential. The pixel architecture is similar to what is described in the paragraph 2.2, but with a single capacitance on the memory node. Careful design of the pixel is needed to keep radiometric performances high (front side illumination) and thus making this sensor a competitive solution. It is achieved by combining solutions at the circuit and layout level. It is also possible to improve furthermore performances by optimizing the substrate doping profile [5,6].

The parasitic light sensitivity (PLS), or shutter efficiency, is a key performance parameter. It measures the ability of the sensor to stop integration while still being under illumination and to keep the information stored in the pixel during read out. It is defined as the ratio of the sensitivity when the shutter is on (signal stored on the memory node) and when the shutter is off (acquisition). With careful pixel design, low PLS (1:2000 or better) could be achieved. Together with high read out data rate (> 400Mpix/s), high resolution devices (4000 x 4000) exhibit a shutter performance suitable for space imaging.

## 2.4 SPECIFIC DEVELOPMENT FOR ATTITUDE AND ORBIT CONTROL SYSTEMS (AOCS): STAR TRACKER WITH ON-CHIP CONTROLLER AND MEMORY

CMOS detector present a strong interest for smaller cameras for scientific (exploration missions, robotics,…) or optical guidance and navigation cameras which will take full advantage of CMOS specific functional capabilities and power consumption reduction.

The LCMS device, developed by FillFactory for ESA [7], is the sensor for a low-cost low-mass radiation tolerant star tracker head. The die is integrating a 512 x 512, 25 µm pixel size focal plane array, a 12-bit ADC, and logic for image acquisition, processing, and interfacing, as shown in Figure 2.7.

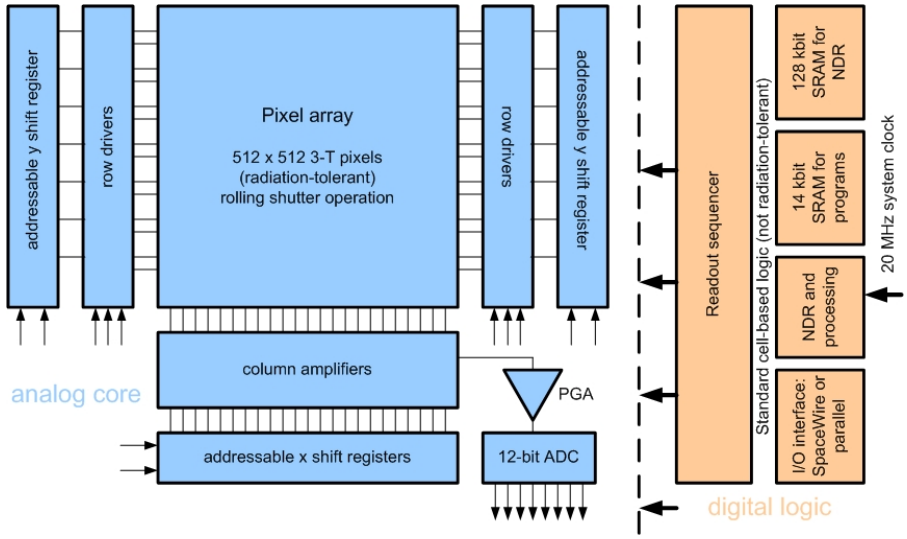


*Figure 2.7 - LCMS block diagram.*

The sensor supports basically two operation modes. In the acquisition phase, full frame images can be read at 5 frames/s. In tracking mode, up to 20 windows of 20 x 20 pixels with an update rate of 10Hz can be taken. The windows each can have individual exposure time and gain, and are read according to a user-programmed timeline stored in on-chip memory. The signal processing comprises of digital-domain correlated double sampling, using on-chip SRAM, background removal, and star signal thresholding. Communication to and from the device is with a 20 MHz SpaceWire interface or a parallel port. Electrical levels are CMOS or LVDS.

## 3 CONCLUSION

In this paper we presented advantages of some CMOS APS over their CCD counterparts for several type of space applications. While being cheaper, more accessible and offering new functions (random pixel access, windowing, synchronous shutter, etc.), CMOS APS exhibit radiometric performances comparable to CCD sensors. Although CCD sensors will certainly remain used in high end spatial imaging applications, it is expected that CMOS APS will be more and more present in this field of applications.

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