DEVELOPMENT OF A LARGE-FORMAT SCIENCE-GRADE CMOS ACTIVE PIXEL SENSOR FOR EXTREME ULTRA VIOLET SPECTROSCOPY AND IMAGING IN SPACE SCIENCE

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ABSTRACT

We describe our programme to develop a large-format science-grade CMOS active pixel sensor for future space science missions, and in particular an extreme ultra-violet spectrograph for solar physics studies on ESA's Solar Orbiter. Our route to EUV sensitivity relies on adapting the back-thinning and rear-illumination techniques first developed for CCD sensors. So far we have designed and tested a 4k x 3k 5µm pixel sensor fabricated on a 0.25 µm CMOS imager process. Wafer samples of these sensors have been thinned by e2v technologies with the aim of obtaining good sensitivity at EUV wavelengths. We present our results to date, and plans for a new sensor of 2k x 2k 10 µm pixels to be fabricated on a 0.35 µm CMOS process.

1 - INTRODUCTION

We are developing science-grade CMOS active pixel sensors for future space science missions. CMOS sensors promise significant advantages over today's CCD technology. Firstly, modern CMOS processing enables smaller pixels than current science-grade CCDs, enabling more compact and lower mass instruments. Secondly, on-chip integration of the readout electronics minimizes the size, mass and power requirements for ancillary control electronics and the associated problems of space-flight component procurement and radiation tolerance. Finally, deep sub-micron CMOS technology promises significantly higher radiation tolerance in the space environment compared to CCDs.

Our goal is the development of a large-format CMOS sensor with useful sensitivity in the extreme ultra-violet (EUV) for solar spectroscopy and imaging on ESA's Solar Orbiter. Our route to EUV sensitivity relies in adapting the back-thinning and rear-illumination techniques first developed for CCD sensors.

We have developed a 4k x 3k pixel sensor with 5µm pixels fabricated on a 0.25 µm CMOS imager process. Wafer samples of these sensors have been thinned by e2v technologies with the aim of obtaining good sensitivity at EUV wavelengths. We present our results to date from both front- and back-illuminated versions of the sensor.

We also present our plans to develop a new EUV-sensitive sensor of 2k x 2k 10 µm pixels for the Extreme Ultra-violet Spectrograph (EUS) on ESA's Solar Orbiter. In progress towards this goal, we have designed a test-structure consisting of six arrays of 512 x 512 10 µm pixels. Each of the arrays

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
13 JUL 2005	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Development Of A Large-Format Science-Grade Cmos Active Pixel Sensor For Extreme Ultra Violet Spectroscopy And Imaging In Space Science	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Rutherford Appleton Laboratory, Chilton, Didcot, Oxfordshire, UK, OX11 0QX**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM001791, Potentially Disruptive Technologies and Their Impact in Space Programs Held in Marseille, France on 4-6 July 2005., The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**UU**	**12**	

has been given a different pixel design to allow verification of our models, and our progress towards optimizing a design for minimal system readout noise and maximum dynamic range. These sensors will also be back-thinned for characterization at EUV wavelengths.

2 - THE 4K X 3K PIXEL CMOS ACTIVE PIXEL SENSOR

A block diagram of the sensor and a schematic of the pixel are shown in Figure 1.

Many CMOS sensors, including our earlier designs [1], employ a simple 3-transistor pixel. This consists of a Reset transistor for recharging the photodiode, a Source Follower for readout, and a Row Select transistor for connecting to the Column Read Lines. Apart from the fixed pattern noise due to processing variations in the diodes and transistors of each pixel, the drawback to this design is that the Reset transistor generates kTC noise when it is switched off, and this can be the dominant noise source in CMOS sensors. For our new sensor, we added a Transfer transistor to allow correlated double sampling of the reset charge and subsequently the integrated photon signal charge, the aim being to cancel the kTC noise.

The transistors inside the pixel are usually all NMOS type, but if an NMOS Transfer transistor is used, the reset voltage to the pixel must be lowered to allow the gate to operate. This not only limits the voltage swing and hence the dynamic range of the pixel, but it also shifts the operating voltage away from the positive power rail. This combines with the level shift imposed by the NMOS output Source-Follower to compress the maximum linear signal range. We therefore decided to implement a PMOS Transfer transistor instead. In this case, the Reset transistor should also be implemented in PMOS to allow the photodiode to be reset to the positive power supply rail. However, we were unable to accommodate this within our 5 µm x 5 µm pixel layout and thus had to compromise with the PMOS Transfer transistor and NMOS Reset transistor.

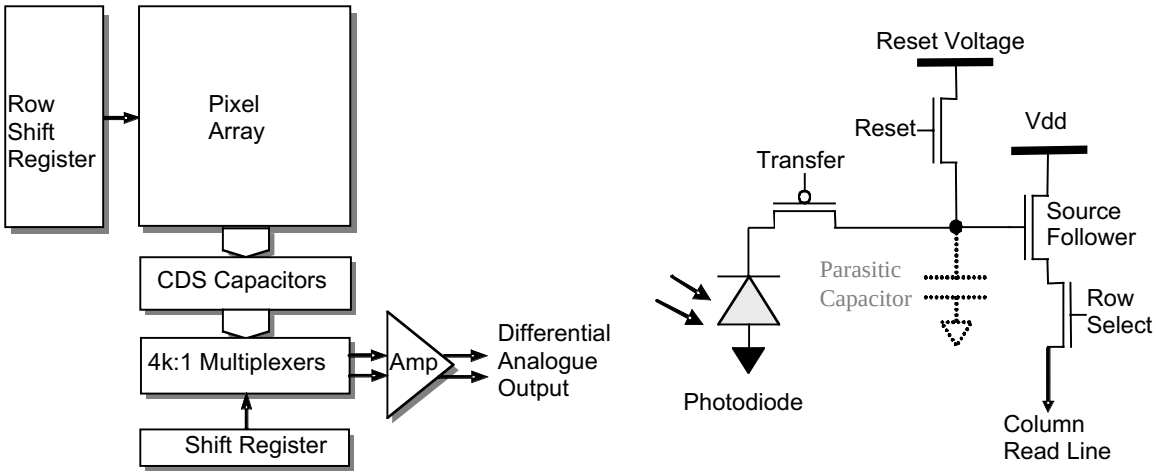

Figure 1 - 4k x 3k pixel sensor architecture and pixel design

The sensor consists of 2880 rows, each of 4096 pixels, and is read out row by row under the control of the Row Shift Register. Each pixel within a row is connected to a Column Read Line so that all pixels within a selected row are read in parallel. Each Column Read Line is connected to a pair of 1 pF correlated double sampling (CDS) capacitors at the bottom of the array which provide storage for samples of the pixel's reset charge and integrated photon charge. Two 4096:1 multiplexers addressed by a shift register route the sample pairs through to a differential switched-capacitor amplifier. This subtracts the two samples to generate a differential analogue output signal. The amplifier's gain can be programmed to be x1 or x2. We use a 14 bit differential-input analogue-to-digital converter to digitize the pixel signals at up to 1 Mpixels/s. The readout rate is limited because of the inherently large resistances and parasitic capacitances of the 4096:1 multiplexers prolonging signal settling time to ~ 1 µs for 12 bits precision. This makes the readout time for the whole sensor ~ 12 seconds, which means cooling is required to reduce the leakage current.

The sensor was fabricated on a 0.25 µm CMOS process intended for imaging chips, and featuring an 8 µm epitaxial layer. The foundry has developed an optimized version of the N-well/P-epi diode with a dark current of 28 mV/second for a 1.9 μm^2 photodiode. The thresholds for the Reset, Row Select and Source-Follower transistors have also been optimized individually. The pixel array and the analogue readout circuits are powered from 3.3 V, while the logic is powered from 2.5 V. All of the sensor's control clocks and digital interface signals are buffered with on-chip LVDS transmitters and receivers.

Each sensor is mounted on an invar block and wire-bonded to a small printed circuit board (PCB) that carries ceramic decoupling capacitors for the power and DC bias supplies, and termination resistors for the LVDS clock receivers. A 51-way micro-D connector soldered to the underside of the PCB provides the connections interface. A black-anodised aluminium cover provides protection for the bond wires and a small degree of optical shielding over the sensor's readout circuitry running along the long edge of the chip. Photographs of the sensor, PCB and bond-wire cover are reproduced in Figure 2.

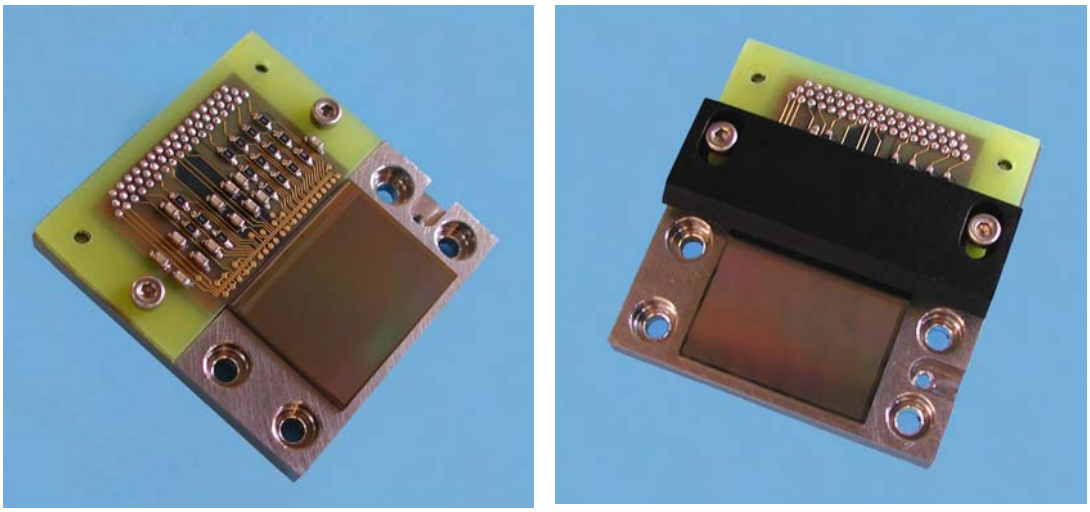

Figure 2 - Photograpghs of the 4k x 3k pixel sensor

3 - BACK-THINNING FOR EUV SENSITIVITY

Figure 3 shows the optical absorption coefficient in silicon over the EUV-Visible band. At EUV wavelengths the absorption depth is so shallow that the oxide layers on front-illuminated CMOS sensors absorb the photons before they reach the photodiodes. Our route to EUV sensitivity relies in adapting the back-thinning and rear-illumination techniques first developed for CCD sensors.

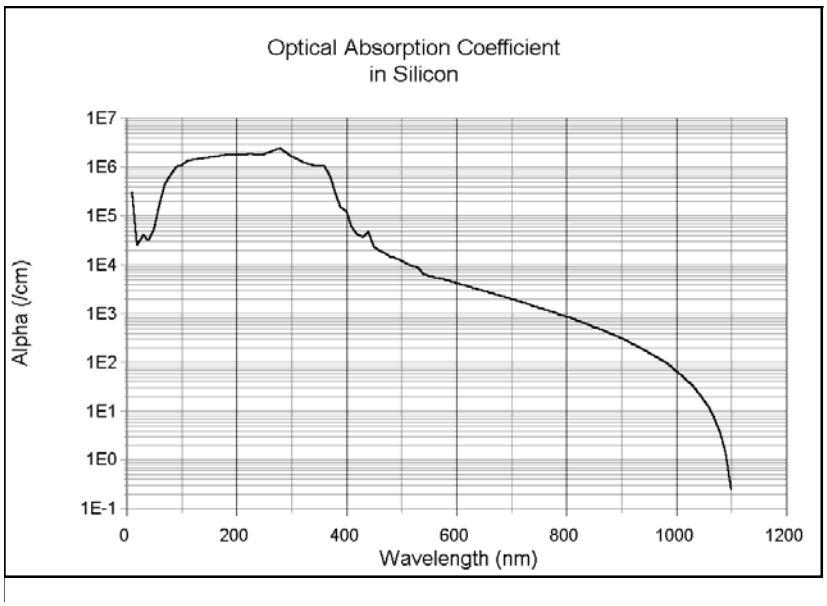

Figure 3 - Optical absorption coefficient in silicon

Figure 4 illustrates a cross-section through a typical front-illuminated CMOS sensor, and then after back-thinning. After first bonding the front side of the sensor to another substrate to provide mechanical support, the bulk silicon is removed by chemical etch. For CMOS sensors the thickness of the silicon wafer, and in particular the epitaxial layer vary between CMOS foundries. It is the thickness of the epitaxial layer that is critical for successful thinning and back-illumination.

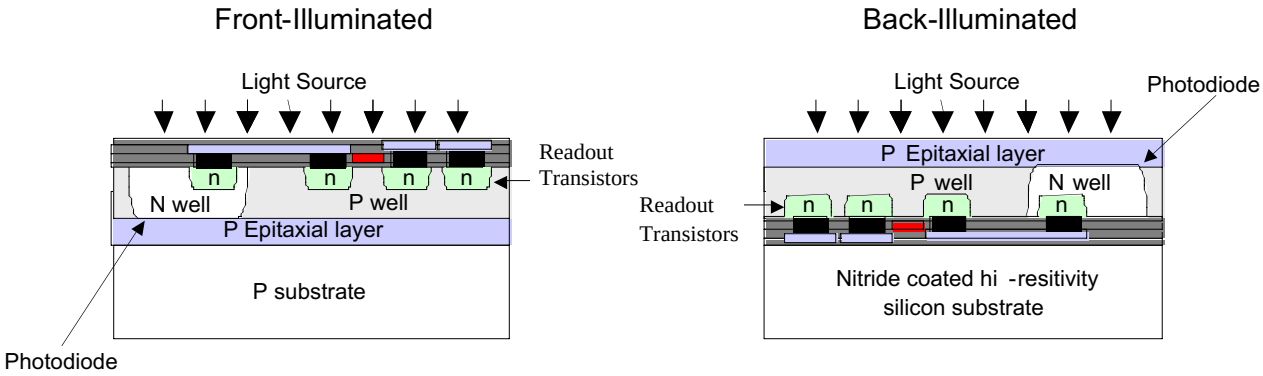

Figure 4 - Typical CMOS sensor cross-sections - front- and back-illuminated

If the epitaxial layer is too thin it will very likely be impossible to control the uniformity of the chemical etch sufficiently such that only epitaxial material remains. Over-etching will damage or destroy the sensor electronics while under-etching will leave unwanted bulk substrate which will compromise the sensitivity of the device at short wavelengths [1].

In contrast, if there is still a thick epitaxial layer remaining after back-thinning, it will compromise the MTF performance of the sensor at short wavelengths. Here the critical parameters are the pitch of the pixels and the depth of the field-free region within the remaining epitaxial layer. Electrons created close to the entry face will be free to diffuse latterally, and significant diffusion will compromise MTF performance.

Our sensor was fabricated on 8 µm epitaxial, 8-inch silicon wafers. Samples of the 8-inch wafers were first cut into smaller sections as e2v technologies thinning apparatus is designed for their standard 5-inch CCD wafers. Sectioning of the wafers was a prerequisit to identifying the precise location and profile of the epitaxial/bulk silicon boundary, and thinning to ≤ 6 µm was required.

Precise details of the thinning process and the repair of damage to the backside surface are propriotary to e2v technologies and thus not for disclosure. However, we can report two obvious challenges.

1. The fear that the subsequent repair of the backside surface after thinning to inside the epitaxial layer might damage the sensor electronics.
2. Developing a reliable technique for wire-bonding through to the sensors bond pads.

After thinning, e2v technologies mounted the sensors on invar blocks and wire-bonded to modified PCBs, mirror-imaged in the long dimension from those of the front-illuminated sensors. A photograph of a finished sensor is reproduced in Figure 5.

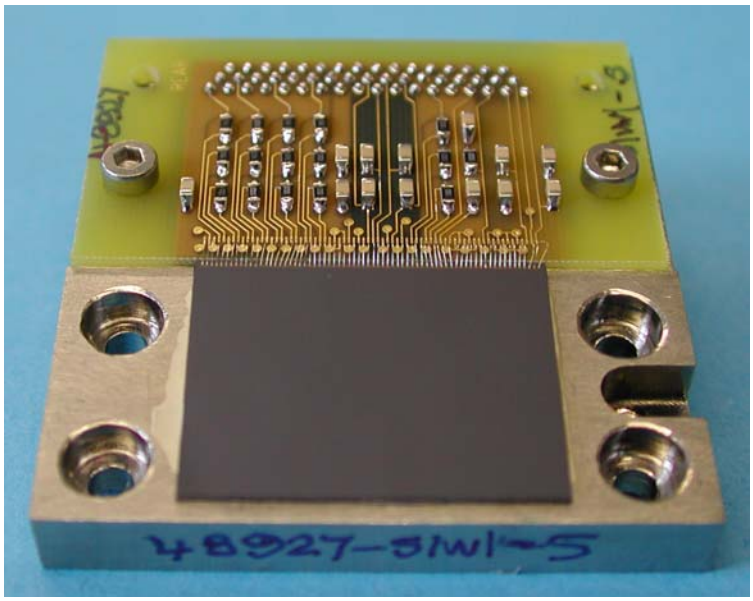

Figure 5 - Finished thinned, back-illuminated 4k x 3k pixel CMOS sesnor

4 - TEST RESULTS FROM FRONT- AND BACK-ILLUMINATED SENSORS

Initial results from a front-illuminated sensor have already been published [2]. Here, we present for comparison early test images obtained from both front- and back-illuminated versions of the sensor, and then a brief summary of the intrinsic pixel and readout electronics performance.

Test images obtained from both front- and back-illuminated sensors are reproduced in Figure 6. Both were obtained with sensors cooled to 273K. The front-illuminated image was taken in white light, whereas the back-illuminated image was obtained through a 50 nm wide narrow-band filter centered at 350 nm and an IR-blocking filter. It is important to note that the back-illuminated sensor would not be expected to work well at long wavelengths because photons penetrate sufficiently to create electrons within the readout electronics rather than in the substrate from where they are collected by the photodiode. We have yet to attempt detailed characterization of the MTF performance of the back-illuminated sensor, but we have determined that the resolution is not significantly degraded compared to the front-illuminated sensor.

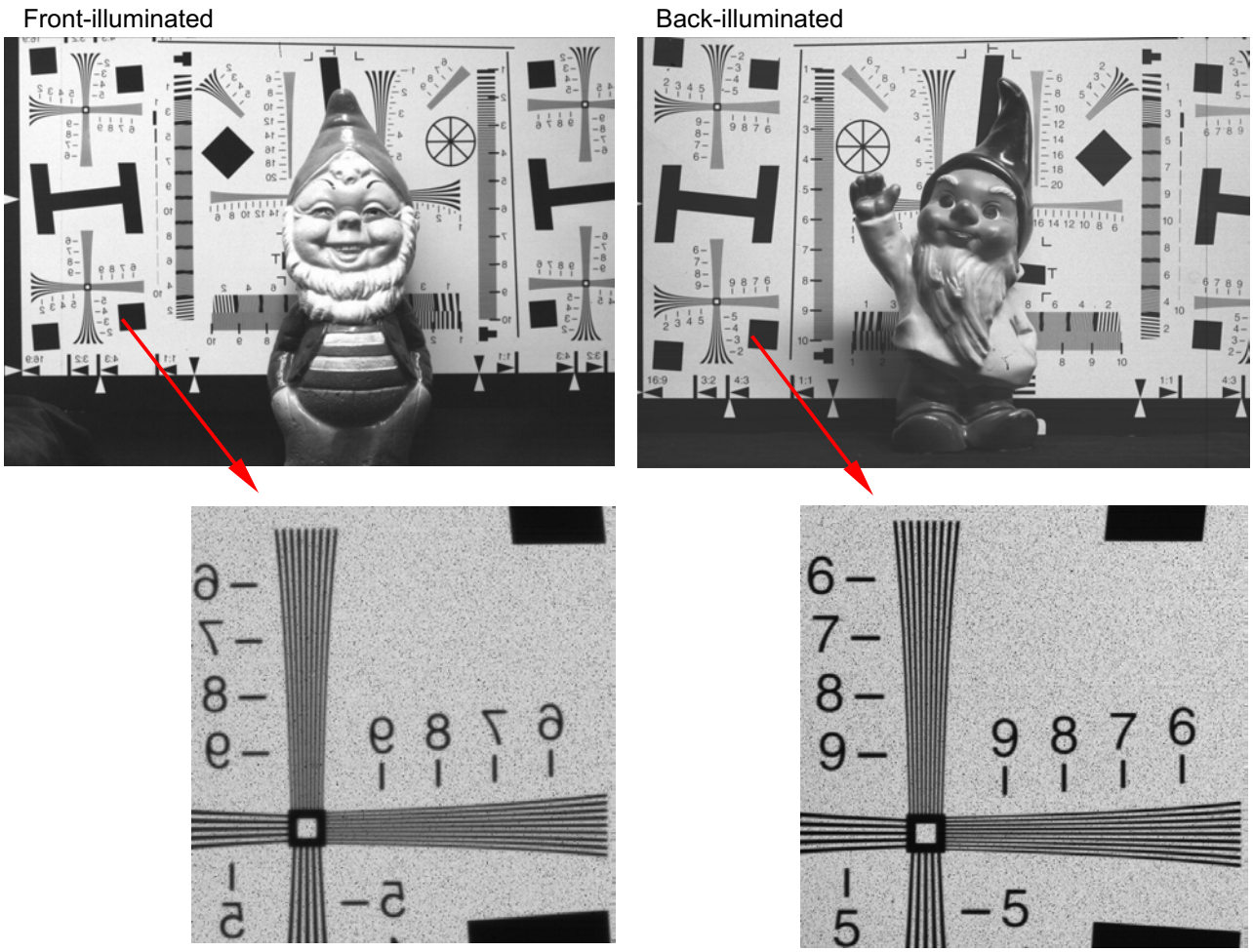

Figure 6 - Test images from front- and back-illuminated sensors

Photon transfer curves for the two sensors are shown in Figure 7 and indicate a system gain of 15 electrons per ADU, and a linear dynamic range ~ 18,000 electrons.

The readout noise of the sensor is ~ 41 electrons rms, which is far more than the 15 electrons rms we were hoping to achieve with CDS cancellation of the kTC noise. On investigation we found that holding the Transfer transistor off reduces the noise to ~ 17 electrons rms which is in much closer agreement with our model. Our belief is that the kTC noise is not cancelled, and in fact this is to be expected from the way we first thought to operate the pixel.

- Recharge the photodiode (and output node) prior to an exposure.
- After exposure, pulse the Reset transistor on to reset the output node, and then sample the reset level.
- Switch the Transfer transistor on and sample the photodiode signal.

After exposure and reset of the output node, the kTC noise charge is sensed as a noise voltage on the reset node capacitance (~ 4.5 fF). However, when the Transfer transistor is switched on to sense the integrated signal charge on the photodiode, the original kTC noise charge is shared between the capacitance of the photodiode (~ 5.5 fF) and the reset node. The kTC noise voltage therefore changes, and is not cancelled by CDS. To overcome this problem, it would be necessary to modify the way we operate the pixel as follows.

- Prior to an exposure, recharge the photodiode and output node as before.
- Switch the Reset transistor off and measure the kTC noise induced on the photodiode and output node. Then switch the Transfer transistor off and start the signal integration.
- After exposure, switch the Transfer transistor on and sample the photodiode signal.

This scheme should allow cancellation of the kTC noise arising from the Reset transistor. However, there arises the new problem that any light or leakage currents reaching the reset node during the signal integration will corrupt the fraction of kTC charge held upon it. A second problem is that when the Transfer transistor is switched off prior to the exposure, kTC noise from the Transfer transistor is induced on the photodiode capacitance which is also not cancelled by the subsequent CDS. Unfortunately, our design of the logic circuitry controlling the Reset and Transfer transistors precludes us from testing these ideas on our existing sensor.

Another consequence of the reset node and photodiode capacitances being roughly equal is that the signal charge is also shared between them. This means that the available dynamic range, or full well capacity to use CCD terminology, is also effectively halved. The dynamic range is further limited by having to operate the reset voltage at 2.5 V to ensure the photodiode is properly reset. Overall, it is now clear that our introduction of the Transfer transistor has not been beneficial.

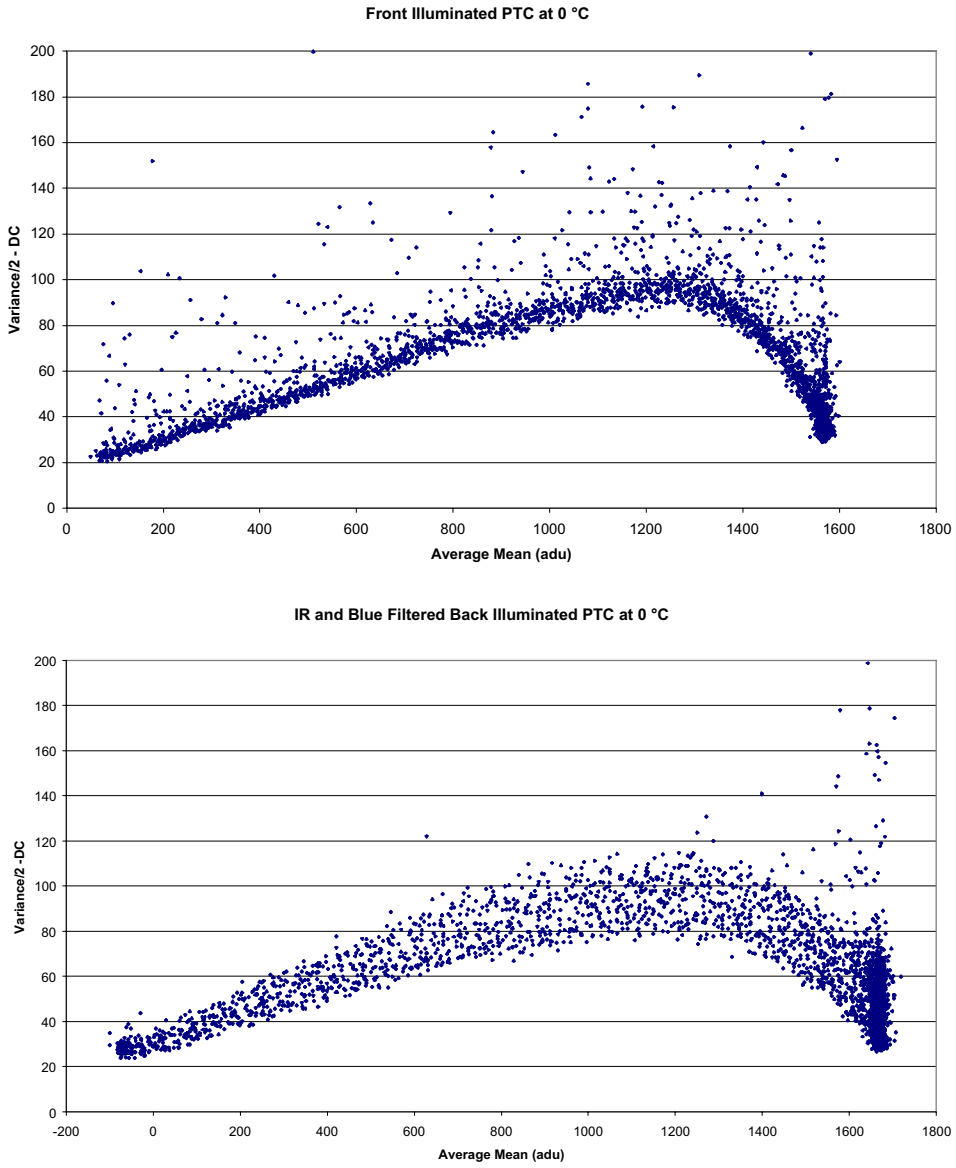

Figure 7 - Photon transfer curves from front- and back-illuminated sensors

Closer examination of the regions of interest from the test images presented in Figure 6 reveals that the general “background” scene appears “speckled” with darker pixels. On investigation the darker pixels are found to be less responsive than the normal pixels, and total ~ 2% of the whole array. We have no explanation of why there should be so many “black” pixels, but speculate that the N-well required for the PMOS Transfer transistor is too close to the photodiode and resistive paths are occurring between the two.

In conclusion, we now regret our choice of pixel design for this sensor. The dynamic range has been severely compromised and the CDS cancellation of kTC noise has not worked as we first hoped. On the other hand, we have shown that a large-format sensor can be thinned uniformly to inside of an 8 µm epitaxial layer. Further work is required to characterize the quantum efficiency and MTF performance, but the results to date have been encouraging. The next step in our development programme will be to address how to maximize the pixel dynamic range.

5 - PLANS FOR THE NEXT SENSOR

We are planning to develop a new EUV-sensitive sensor of 2k x 2k 10 µm pixels for the Extreme Ultra-violet Spectrograph (EUS) on ESA's Solar Orbiter. The original concept for the instrument called for a 4k x 4k pixel detector format, hence our design of a 4k x 3k pixel prototype. However, subsequent optimization of the instrument's conceptual design has seen this requirement relaxed to a 2k x 2k pixel format.
In progress towards this goal, we have designed a test-structure consisting of six arrays of 512 x 512 10 µm pixels. The larger pixel size allows us to use a 0.35 µm CMOS process, and we have selected one from austriamicrosystems (AMS) that is fabricated on a relatively thick epitaxial layer of at least 14 µm. Each of the arrays has been given a different pixel design to allow verification of our models, and our progress towards optimizing a design for minimal system readout noise and maximum dynamic range. These sensors will also be back-thinned for characterization at EUV wavelengths.
All the pixels are 3-transistor type and so the only possibility for kTC noise cancellation will be to read the chip twice, before and after the signal integration, and perform the CDS off-chip. However [3] has shown that kTC noise can be reduced by using a soft-reset with the expectation that the kTC noise contribution is closer to $\sqrt{kTC/2}$ rather than the normal $\sqrt{kTC}$. On its own, soft-reset will give rise to image lag with the result that one image is affected by the previous. However, [3] has shown that this can be overcome by first using a hard-reset to ensure that all photodiodes are equally reset, followed by a soft-reset to gain the advantage in reset noise. This reset strategy is referred to as a "flushed-reset", and we have implemented it on our new test-structure.

Figure 8 shows a schematic of the basic 3-transistor pixel with the additional circuitry required for the flushed-reset. Figure 9 simplifies the schematic to illustrate how the circuit operates during the hard- and soft-reset phases.

During hard-reset, the Flush line is asserted connecting the Reset Voltage Bus between Mb1 and Mb2' (via Mfb). Mb1 and Mb2' are biased so as to force the Reset Voltage Bus to some voltage lower than Vdd. When the Reset line is switched to Vdd, Mr will be overdriven and the pixel will be hard-reset to the voltage on the Reset Voltage Bus.

The soft-reset is applied after allowing sufficient time for the hard-reset. Flush is de-asserted such that Mb2' is no longer connected to the Reset Voltage Bus, and Mrf overrides Mb1, pulling the Reset Voltage Bus up to Vdd. Mr is no longer overdriven, and so the reset becomes soft.

A second advantage of the flushed-reset scheme is that the difference in the voltage on the Reset Voltage Bus between hard- and soft-reset is coupled onto the photodiode during the soft-reset phase and thus increases the dynamic range [3].

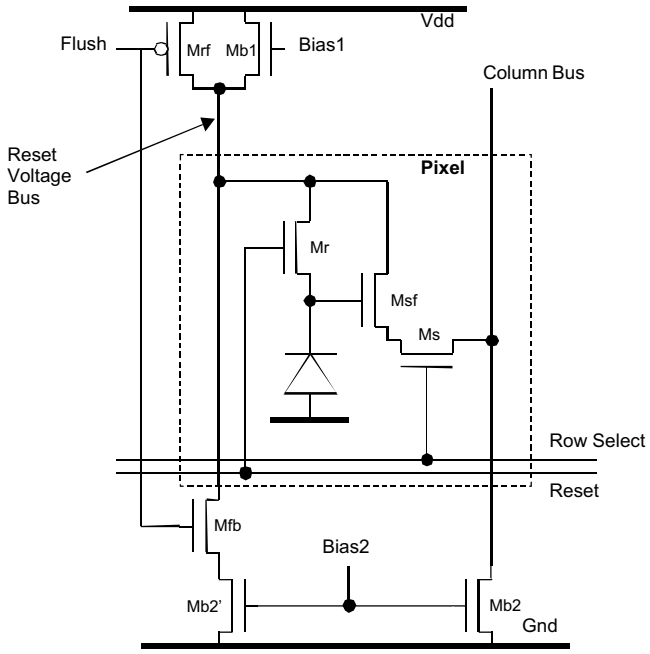

Figure 8 - Schematic of the flushed-reset 3-transistor pixel

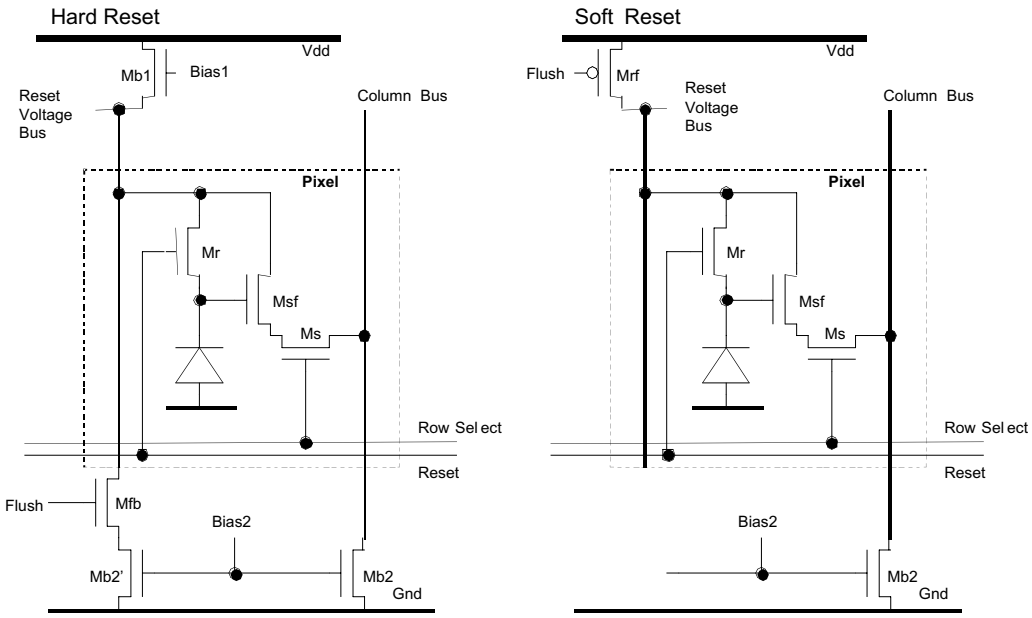

Figure 9 - Flushed-reset operation

A floor-plan of the test-structure sensor is shown in Figure 10, and the different pixel types are listed in Table 1. A prime objective is to explore the optimal pixel capacitance required for minimizing the total system noise and maximizing the dynamic range. Large capacitance is desirable to maximize the photodiode full well capacity, and hence the overall dynamic range. On the other hand, small capacitance is needed to minimize kTC noise. Flushed-reset is expected to minimize the kTC noise contribution, and off-chip CDS may reduce it still further. Figure 11 illustrates the full well capacity expected as a function of noise for varying capacitance.

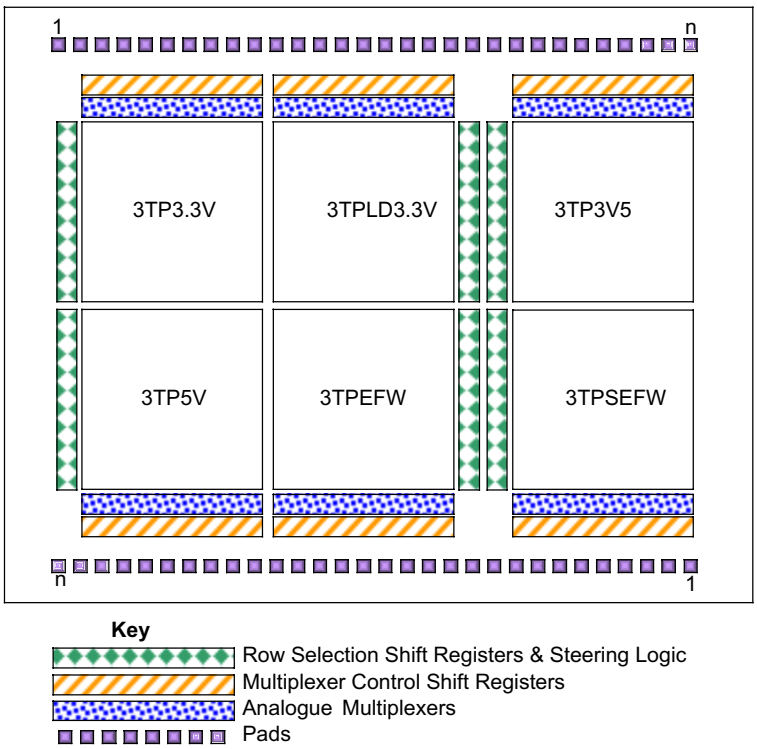

Figure 10 - Floor plan of of our new test-structure chip

Pixel Name	Photodiode capacitance	Main Features
3TP3.3V	5 fF	Simple 3-transistor pixel designed for minimal capacitance and thus minimum kTC noise.
3TPLD3.3V	10 fF	Same as 3TP3.3V but optimized with larger capacitance for greater well capacity.
3TP3V5	5 fF	3.3 V and 5 V mixed voltage version of 3TP3.3V
3TP5V	5 fF	All 5 V version of 3TP3.3V.
3TPEFW	20 fF	Enhanced full-well version of 3TP3.3V with an added capacitor to maximize well capacity.
3TPSEFW	7 - 24 fF	Switchable version of 3TPEFW to allow selectable photodiode capacitance and hence well capacity.

Table 1- Pixel types of the 6-part 512 x 512 pixel test-structure

We have designed the first pixel (3TP3.3V) with minimal capacitance (~ 5 fF) and the second (3TPLD3.3V) with larger capacitance (~ 10 fF). Both of these pixels employ the standard 3.3 V transistors for the AMS 0.35 µm CMOS process. The third and fourth pixel types are variants of the basic small-capacitance pixel; one with a mixture of 3.3 V and 5 V transistors (3TP3V5), and the other a full complement of 5 V transistors (3TP5V). These will be used to investigate whether 5 V biasing can be employed to increase the operating voltage range of the pixel, and hence the dynamic range. There are side-effects with the 5 V transistors which suggest that the pixel characteristic is not altogether straightforward to model. The fifth pixel (3TPEFW) has a capacitor added to the photodiode to increase the overall capacitance to ~ 20 fF. Here we are maximizing the full well capacity in the knowledge that we will suffer more kTC noise. In the final pixel (3TPSEFW), shown in Figure 12, we have added a fourth transistor (Range) which allows the extra node

capacitance to be switched in or out. The overall node capacitance will be switched between ~ 7 fF and ~ 24 fF, thus allowing the full well capacity and kTC noise to be selected depending on the signal range of interest. For weak signals, the lower range will be selected to minimize noise; whereas for strong signals, the full well capacity will be maximized as photon shot noise might be expected to dominate. This feature is of particular interest for the Extreme Ultra-violet Spectrograph on ESA's Solar Orbiter where imaging of both weak and strong lines can be anticipated.

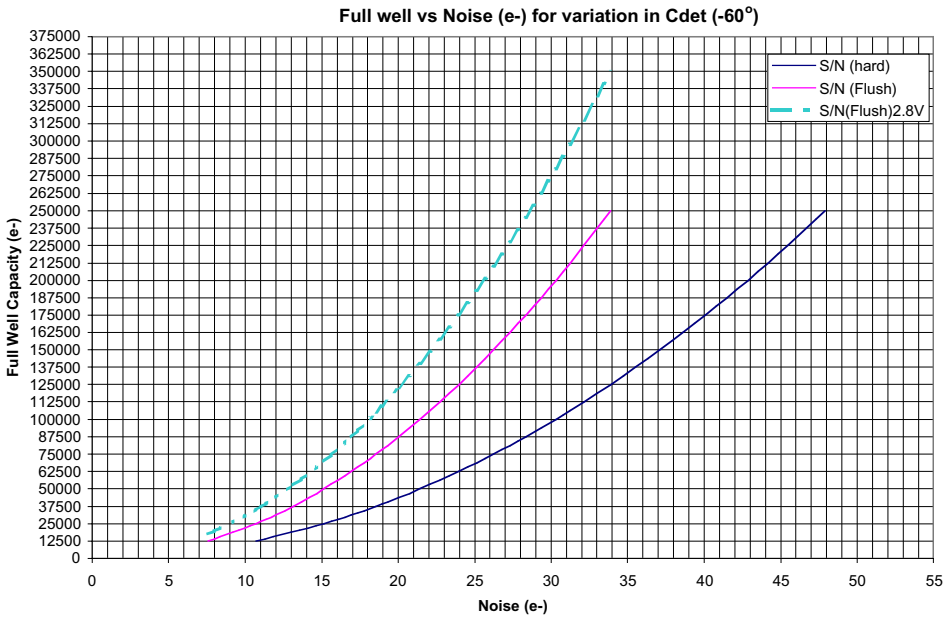

Figure 11 - Variation of pixel full well capacity with reset noise

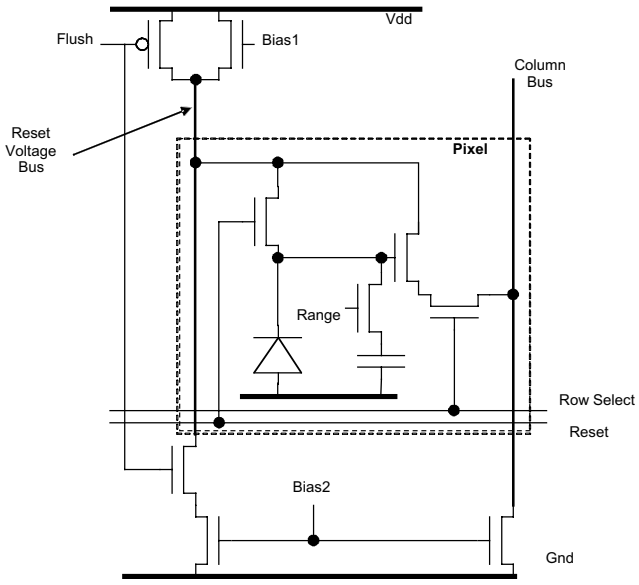

Figure 12 - Switched Extended Full Well pixel (3TPSEFW)

The six arrays are laid out such that the top three are operated from the top set of bond pads, and the bottom three from the bottom set of bond pads. The bond pad assignment has been mirrored such that one set of electronics can operate the chip from either top or bottom. The chip and a printed circuit board to carry local decoupling capacitors will be mounted on an invar block similar to that used for our 4k x 3k pixel sensor. Both front- and back-illuminated versions of the test-structure will be characterized.

6 - CONCLUSIONS

We have demonstrated a large-format 4k x 3k pixel CMOS sensor with 5 µm pixels and the feasibility of thinning for back-illumination. Further work is required to characterize the quantum efficiency and MTF performance of both the front- and back-illuminated sensors.

We have also presented our plans to develop a new EUV-sensitive sensor for the Extreme Ultra-violet Spectrograph on ESA's Solar Orbiter, and in this the design of a new test-structure consisting of six arrays of 512 x 512 10 µm pixels. Each of the arrays has been given a different pixel design to allow verification of our models and progress towards optimizing well capacity and readout noise. These sensors will also be back-thinned for characterization at EUV wavelengths.

ACKNOWLEDGMENTS

The development of our 4k x 3k pixel sensor, our new test-structure, and the back-thinning programme with e2v technologies has been funded through a PPARC Rolling Grant to the Space Science and Technology Department (SSTD) at the Rutherford Appleton Laboratory. A Marshall, M Clapp, J King, D Drummond and J Rainnie of SSTD are acknowledged for the design and commissioning of the data acquisition system.

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