Microgating carbon nanotube field emitters by *in situ* growth inside open aperture arrays

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Multiwalled carbon nanotubes were grown using chemical vapor deposition inside small apertures having a horizontal gate and a sidewall insulator spacer. Emission currents up to 140 nA per cell at 63 V have been obtained. These arrays have exhibited a gate current as low as 2.5% of the anode current throughout the entire gate voltage range, representing the lowest gate to anode current ratio of gated nanotube emitters reported to date. We attribute this feature to the emitter geometry and method of fabrication. The overall fabrication method required only a few and simple processing steps. [DOI: 10.1063/1.1472463]

One of the first applications of carbon nanotubes (cNTs) has been their use as field emitters on account of their natural material, structural, and electronic properties which satisfy many demanding requirements for field emission, including stability, robustness, low voltage, high current-carrying capacity, and mechanical strength. A key factor to their stability as field emitters is the lack of a nonvolatile surface oxide. Surface oxide formation (such as on metal or silicon emitters) increases the work function, impedes electron transport, and makes the effective work function variable during emission. Furthermore, surface oxides could be the main cause for field emitter array (FEA) catastrophic destruction by trapping charge which could lead to arcing.[1] Carbon nanotubes are also less likely to form nanoprotrusions as metal and silicon cathodes do, thus reducing the probability of current runaway.[2] Their small diameters (2–50 nm) and high aspect ratios enable the high electric field enhancement for low-voltage operation, despite the relatively high work function ($\sim$5.0 eV for graphite). They are resistant to blunting by residual back ion bombardment, especially when placed vertical to the substrate, since the nanotube diameter remains the same even when material has been removed from by sputtering.

The most commonly studied cNT emitters involved a diode configuration in which the cNTs, grown or placed as dense mats on substrates, were positioned at a known separation from an anode, to which a positive potential was applied to induce field emission from the cNTs. Although very low turn-on voltages (as low as 1–2 V per μm) were measured, the voltages used were still too high for most applications because the cNT–anode separations were usually large distances. In addition, many device applications, such as flat panel displays, require precise control of the array pixels, thus precluding a diode configuration. Hence, gating of the emission by the placement of a third electrode in close and precise proximity to a group of cNT emitters is necessary to lower the operating voltage as well as afford precise local control of emission. Gating is necessary to enable certain applications which include field emitter displays, high-frequency amplifiers, high-voltage switches, portable x-ray sources, multibeam electron-beam lithography, radiation and temperature-insensitive electronics, space craft propulsion, and electrostatic charge management.

Gating of cNT emitters has been undertaken only within the last two years. A common technique involved the use of a cNT paste (cNTs mixed in a binding matrix) in conjunction with screen print or lithographic technology and the fabrication of ''grid gates,''[3] ''under-gates,''[4,5] ''normal gates,''[6–8] and ''drilled gate holes.''[9] All the gate diameters used in these studies were quite large ($>30\ \mu$m). The operating voltages for these configurations range from low to high (threshold gate voltages from 20 V to over 70 V at high anode voltages). With the exception of the work of Ito and co-workers,[7] the gate currents were either quite high[8,9] (over 50%) or not reported. A cNT paste technology was also used by Wang and co-workers[10] in filling large gate apertures (30 μm) which had prefabricated sidewall insulator spacers. Relatively low-threshold voltages ($\sim$25 V) and significant gate current ($\sim$30% of anode current) were observed.

To date five articles on integral microgated, *in situ* grown cNT FEAs with demonstrated emission have been published: (1) Lee and co-workers[11] have grown cNTs inside 0.7-μm-diam open gated apertures and have reported a low threshold voltage and the anode current-gate voltage characteristics. The gate current was not reported. (2) Talin and co-workers'[12] large aperture structures produced low threshold voltages but high gate currents. (3) Perio and co-workers[13] reported very low-threshold voltages but did not report on the gate current for their 2-μm-diam integrally gated structures. (4) Ahn and co-workers have grown cNTs inside open trenches with a buried gate,[14] reported triode emission but did not show data plots. (5) Our group has grown cNTs on the tops of gated silicon posts as well as inside open gated apertures.[15,16–17] Our cNT-on-silicon post configuration[17] had a significant gate current ($\sim$30% of anode current). The open gate aperture configuration, which we describe in greater detail in this letter, has the lowest reported gate current of cNT FEAs to date. The scarcity of reports on the *in situ* growth approach is largely due to the difficulty of controlling the growth of cNTs (both in length

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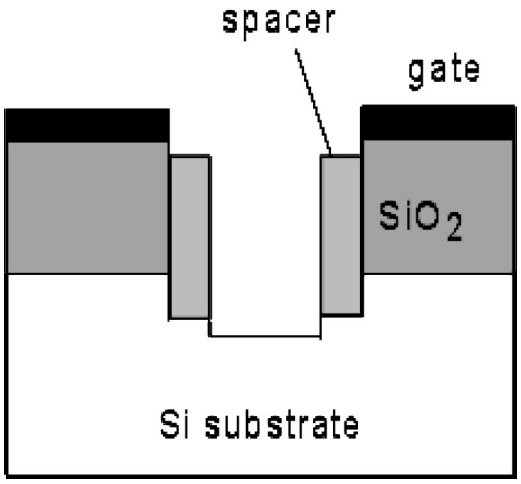

FIG. 1. Schematic drawing of a starting template cell structure showing oxide spacer lining vertical sidewall of gated aperture.

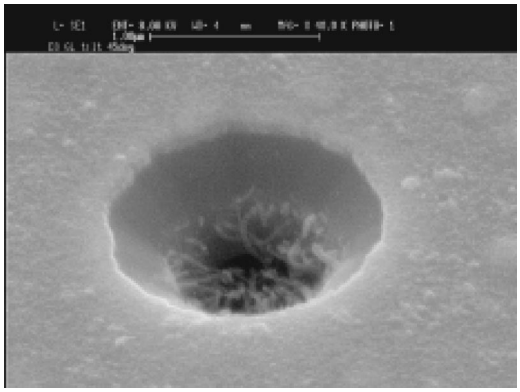

FIG. 2. Scanning electron micrograph of a cell at 45° tilt angle showing multiwalled nanotubes grown on the sidewall of the oxide spacer. The gate diameter and the oxide spacer thickness are 1.7 and 0.35 μm, respectively.

and direction) as well as maintaining gate material integrity at the high growth temperature.

Figure 1 shows schematically the starting template structure with a sidewall spacer. The general fabrication steps of arrays of these starting template structures were similar to those used in our previous work in fabricating gated vertical thin-film edge FEAs.[18,19] The same starting template structures were adapted in our fabrication of gated cNT FEAs.[20] The processing steps are as follows: (1) Gate insulator consisting of 0.5-μm-thick thermal silicon dioxide was grown on a silicon (100) wafer. (2) The gate is a 150-nm-thick boron-doped amorphous silicon layer deposited by low pressure chemical vapor deposition (CVD), followed by evaporative deposition of 50 nm of chrome. (3) Arrays of small holes in photoresist were patterned on the wafer using photolithography. (4) With the photoresist as mask, ion milling was used to remove the chrome from the exposed holes. (5) Reactive ion etching (RIE) was used to etch holes through the amorphous silicon and thermal silicon dioxide, and at least 100 nm into the silicon substrate. (6) Low pressure CVD was used to deposit a blanket (close to conformal) layer of silicon dioxide over the wafer. (7) Directional (RIE) was then used to remove the silicon dioxide layer from the top horizontal surface of the wafer while leaving the vertical sidewall portion intact. Some overetching ensured that the silicon dioxide at the bottom of the holes was removed. The resulting structure was a gated aperture narrowed in its diameter by a vertical sidewall silicon dioxide spacer. This spacer will ultimately serve as a part of the insulator between the nanotubes and the gate. Gated arrays, each consisting of small number of apertures (numbering 10–40) were isolated from each other by thermal oxide regions (i.e., after removing chrome and amorphous silicon from these regions).

The cNT growth process began with sputter deposition of a thin film of Fe ($<$20 nm) onto the starting substrate (cut into 1×1 cm samples). Because the sputtered Fe was not collimated, Fe would be deposited not only on the top surface of the sample and the bottoms of the apertures but also on the sidewalls in the apertures. The sample was sputtered using an Ar ion beam at a glancing angle of 15° with respect to the surface, in order to remove the Fe from the top surface without removing it from inside the apertures. The sample was then placed in a cold-walled hot filament-assisted CVD reactor for nanotube growth under same conditions as in Ref. 17 except that ethylene was used as the carbon precursor.

The top surface of the sample proved to be relatively free not only of cNTs but also of amorphous carbon, which was necessary to prevent shorting of neighboring arrays. Tests on witness oxide surfaces under similar growth conditions showed them to remain highly insulating. No cNT grew on the chrome gate because any remaining Fe apparently diffused into or alloyed with chrome at the high growth temperatures, thereby losing catalytic activity for cNT growth. No significant amorphous carbon on the catalyst-free top surface was found due to the excess ammonia (i.e., ammonia-derived radicals such as H, NH_2, and NH likely reacted with carbon). Using a scanning electron microscope (SEM) we observed multiwalled cNT growth (with 20–30 nm diameters) inside the apertures, both on the bottoms and on the sidewalls. TEM analysis of cNTs grown under same conditions showed a significant ''bamboo-like'' segment feature within the tubes.

Figure 2 shows a SEM photograph of a cell of a gated cNT FEA grown at 700 °C and 22.4 Torr total pressure for 2 min 45 s. The gate aperture diameter and the oxide spacer thickness were 1.7 and 0.35 μm, respectively. This particular array had 40 cells, and SEM examination showed that every cell had many cNTs extending from the bottoms and sidewalls. The cNTs were relatively short and the ones closest to the gate were attached to the upper portions of the sidewall of the oxide spacer. Field emission would more likely take place from these closest cNTs, since the sidewall should be in electrical contact with the underlying silicon substrate through a ''mat'' of cNTs, and through carbonaceous (from catalyzed growth) and residual catalyst deposits on the sidewall and the bottom surfaces. We also believe that growing relatively short cNTs affords better control in preventing cNT shorting to the gate, compared to growing long cNTs exclusively from the bottom of the aperture. As shown in Fig. 2, many of the nanotubes near the top of the aperture had a significant horizontal component (parallel to the top surface) and pointed toward the center part of the gate aperture. The side portions of the nanotubes might also contribute to emission by emitting from defects sites, according to observations of Chen and Shaw,[21] on field emission dependence on nanotube orientation.

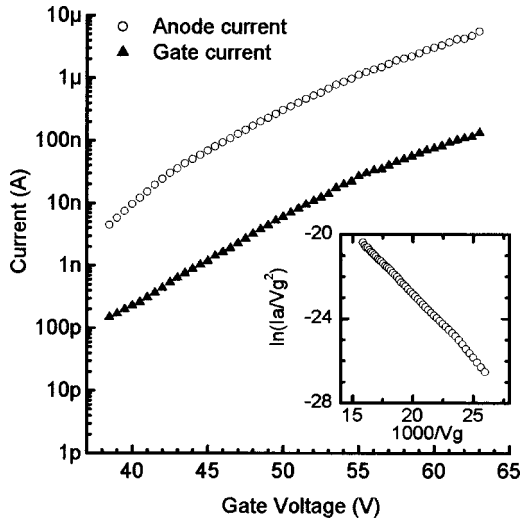

FIG. 3. Emission current–voltage characteristics from an array of 40 cells corresponding to Fig. 2. Inset shows a Fowler–Nordheim plot of the anode current.

Emission characterization was carried out in an ultra high vaccum chamber (base pressure 10^{-10} Torr) equipped with cathode, gate, and anode probes with computerized data collection for current–voltage, current–time, and electron energy distribution characteristics. The anode probe was placed about 1 mm from the arrays and an anode voltage of 200 V was used.

Figure 3 shows the current–gate voltage characteristics of the 40-cell array corresponding to Fig. 2. The threshold gate voltage was about 35 V (2 nA at 35 V), and a current of 5.6 μA was obtained at a gate voltage of 63 V. This current corresponded to about 140 nA per cell. The very low gate current (about 1/40 of the anode current) is distinctively different from all previous reports on gated cNT FEAs, which either had significant gate currents or reported only the anode currents. The inset displays a Fowler–Nordheim plot of the anode current, which suggests well-behaved field emission by its high linearity. Three of our other devices with similar template structures, with cNTs grown in three separate runs on separate days, also showed low threshold voltages V_t and low ratios of gate current to anode current I_g/I_a ($V_t=35$ V, 35 V, 45 V, and $I_g/I_a=0.04$, 0.02, and 0.06, respectively). Low gate currents are necessary for preventing gate burnout in applications that require high emission currents such as high-frequency amplifiers and high-voltage switches. For current gain ($\Delta I_a/\Delta I_g$) and power gain ($\Delta I_a \Delta V_a/\Delta I_g \Delta V_g$) devices (i.e., amplifiers), where ΔI_a, ΔI_g, ΔV_a, and ΔV_g are the changes in anode current, gate current, anode load voltage, and gate voltage, respectively, obviously a high ratio of anode current to gate current (I_a/I_g) (or a high ratio of $\Delta I_a/\Delta I_g$) is important. A high gate current can limit switching speed if the gate impedance is high so that heat generation in the gates begins to degrade the device. For field emission displays (FEDs), a significant gate to anode current ratio can be tolerated because the required emission current is low.

The single most important aspect of this letter is the combination of low gate current and low-threshold gate voltage with relatively low anode voltage (200 V at 1 mm anode–substrate separation), compared to all the other published works on gated cNT FEAs. It could possibly be attributed to the small gate diameter and a spacer thickness that was a significant fraction of the gate diameter so that any part of the gate edge could still exert significant field on all the emitting cNTs at low voltages.

In conclusion, we report the fabrication of a microgated cNT FEA, in which cNTs were grown in small diameter open apertures with insulator sidewall spacers. We believe that the most effective cNT emitters were grown on the upper portions of the spacer sidewall. We have demonstrated low-voltage and lowest gate current operation which we attributed to our unique emitter cell geometry and method of fabrication. Further emission characterization in regard to long-duration stability, effect of ambient gases, electron energy distributions, and nanotube–substrate interfaces are in progress. The manufacture of these FEAs should be very economical given the few simple processing steps.

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