REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing this collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number. **PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.**

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
15 Oct 04	Conference Paper POSTPRINT	2003-2004

4. TITLE AND SUBTITLE
Mobility and transverse electric field effects in channel conduction of wrap-around-gate nanowire MOSFETs

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
A.K. Sharma, *S.H. Zaidi, S. Lucero, †S.R.J. Brueck, ǂN.E. Islam

5d. PROJECT NUMBER
4846

5e. TASK NUMBER
RP

5f. WORK UNIT NUMBER
AA

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) AND ADDRESS(ES)
Air Force Research Laboratory
Space Vehicles
3550 Aberdeen Ave SE
Kirtland AFB, NM 87117-5776

*Gratings Inc.
2700B Broadbent Pkwy NE
Albuquerque, NM 87107-1610

8. PERFORMING ORGANIZATION REPORT NUMBER
AFRL-VS-PS-TP-2006-1006

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
Published in IEE Proceedings – Circuits, Devices and Systems, Vol: 151, Issue: 5, pp. 422-430, 15 Oct 04
Government Purpose Rights
†Dept of Physics and Astronomy, University of New Mexico, Albuquerque, NM 87106
ǂDept of Electrical and Computer Engineering, University of Missouri, Columbia, MO 65211

14. ABSTRACT
The current conduction process through a nanowire wrap-around-gate, ~50 nm channel diameter, silicon MOSFET has been investigated and compared with a ~2 μm wide slab, ~200 nm thick silicon (SOI) top-only-gate planar MOSFET with otherwise similar doping profiles, gate length and gate oxide thickness. The experimental characteristics of the nanowire and planar MOSFETs were compared with theoretical simulation results based on semi-empirical carrier mobility models. The SOI nanowire MOS devices were fabricated through interferometric lithography in combination with conventional I-line lithography. A significant increase (~3×) in current density was observed in the nanowire devices compared to the planar devices. A number of parameters such as carrier confinement, effects of parallel and transverse field-dependent mobilities, and carrier scattering due to Coulomb effects, acoustic phonons, impurity doping profile and surface roughness influences the transport process in the channel regions. The electron mobility in the nanochannel increases to ~1200 cm^2/V s compared to ~400 cm^2/V s for a wide slab planar device of similar channel length. Experiments also show that the application of the channel potential from three sides in the nanowire structure dramatically improves the subthreshold slope characteristics.

15. SUBJECT TERMS
Transverse electric field effects; Channel conduction; Conduction process; Doping profiles; gate length; gate oxide thickness; Interferometric lithography; Nanowire device

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			David R. Alexander
Unclassified	Unclassified	Unclassified	Unlimited	10	19b. TELEPHONE NUMBER *(include area code)* 505-846-4499

Mobility and transverse electric field effects in channel conduction of wrap-around-gate nanowire MOSFETs

A.K. Sharma, S.H. Zaidi, S. Lucero, S.R.J. Brueck and N.E. Islam

Abstract: The current conduction process through a nanowire wrap-around-gate, ~50 nm channel diameter, silicon MOSFET has been investigated and compared with a ~2 μm wide slab, ~200 nm thick silicon (SOI) top-only-gate planar MOSFET with otherwise similar doping profiles, gate length and gate oxide thickness. The experimental characteristics of the nanowire and planar MOSFETs were compared with theoretical simulation results based on semi-empirical carrier mobility models. The SOI nanowire MOS devices were fabricated through interferometric lithography in combination with conventional I-line lithography. A significant increase (~3×) in current density was observed in the nanowire devices compared to the planar devices. A number of parameters such as carrier confinement, effects of parallel and transverse field-dependent mobilities, and carrier scattering due to Coulomb effects, acoustic phonons, impurity doping profile and surface roughness influences the transport process in the channel regions. The electron mobility in the nanochannel increases to ~1200 $cm^2/V s$ compared to ~400 $cm^2/V s$ for a wide slab planar device of similar channel length. Experiments also show that the application of the channel potential from three sides in the nanowire structure dramatically improves the subthreshold slope characteristics.

1 Introduction

Scaling of semiconductor devices to the nanoscale regime can lead to device and performance parameter improvements including reduction in operating voltage, increased speed and greater packaging densities. As silicon is the material of choice for a large percentage of semiconductor devices, the fabrication, analysis and testing of scaled down versions of existing Si devices has been an active research subject [1, 2]. The scaling of device parameters of many structures is under consideration and theories for improved effective channel length for a fully depleted, surrounding-gate MOSFET and double-gate SOI MOSFET have been proposed [3, 4]. Dimension reduction for current technologies, however, has its limits set by optical lithography, and scaling of MOSFETs has complexities of short-channel-effects (SCEs). Scaling of double gate and silicon-on-insulator (SOI) Delta MOSFETs to the nanoscale regime shows promise but further scaling has been limited due to fabrication difficulties [5].

For MOS transistors, scaling studies have mainly focused on decreasing channel length to submicron dimensions while the width has remained several microns in size due to the necessity of maintaining the current driving capability (width-to-length ratio) of the transistor. True nanoscaling requires the reduction of the overall size of the transistor and not just the gate length. Such studies have recently attracted considerable research interest since the electrical, optical and thermodynamic properties of nanostructures can be significantly different from those of bulk material of the same composition [6]. MOSFETs with a nanowire channel wrap-around-gate (WAG) structure have been shown to have significantly improved carrier transport properties over conventional devices because of reduced scattering and better gate control. Additional study is necessary in order to fully determine the physical processes impacting the transport mechanisms [7].

In this paper we demonstrate that the current density is enhanced in nanowire channel WAG MOSFETs as a result of higher carrier mobilities. We discuss the physical processes contributing to the increased mobility, specifically quasi-1D transport at the channel centre of such devices. Equations for the mobility model and a physical interpretation are provided. For this study, we fabricated ~50 nm diameter nanowire, wrap-around-gate MOSFETs with single and multiple parallel channels and compared their characteristics with ~2 μm wide, 200 nm thick slab, top-only-gate MOSFETs that were identical in all aspects except for dimensionality of the channel region. In order to focus on the effects of scaling the channel width region, the nanowire channel length and the slab gate length were both made intentionally long (~2 μm) for this study so that short channel effects would be minimised. Simulations of carrier mobility for both nanowire WAG and slab gate devices are presented. The device conduction processes are explained in

© IEE, 2004

IEE Proceedings online no. 20040993

doi:10.1049/ip-cds:20040993

Paper first received 10th October 2003 and in revised form 5th April 2004

A.K. Sharma and S. Lucero are with the Air Force Research Laboratory, Space Vehicles Directorate, Kirtland AFB NM 87111, USA

S.H. Zaidi is with Gratings Inc., Albuquerque, NM 87109, USA

S.R.J. Brueck is with the Department of Physics and Astronomy, University of New Mexico, Albuquerque NM 87106, USA

N. E. Islam is with the Department of Electrical and Computer Engineering, University of Missouri, Columbia MO 65211, USA

A.K. Sharma and S.R.J. Brueck are also with the Centre for High Technology Materials, University of New Mexico, Albuquerque NM 87106, USA

terms of changes in the channel mobility, the influence of transverse and parallel components of the channel electric field, and the impurity distribution within the channel as a result of the fabrication process.

2 Nanowire fabrication

Interferometric lithography (IL) is a well-developed technique for inexpensive, large-area nanopatterning and was used in the nanowire fabrication process [8]. In its simplest version, IL is interference between two coherent waves resulting in a 1D periodic pattern with a pitch of $\lambda/2\sin\theta$ where λ is the optical wavelength and 2θ is the included angle between the interfering beams. A typical IL configuration consists of a collimated laser beam incident on a Fresnel mirror (FM) mounted on a rotation stage for period variation [9]. There is no depth dependence to an IL exposure pattern, for which the depth-of-field is limited only by the laser coherence length and beam overlaps. The 1D nanoscale patterns were first formed in photoresist followed by pattern transfer on to the underlying substrate using reactive-ion-etching (RIE) in a parallel plate reactor using CHF_3/O_2 plasma chemistry [10]. Figure 1 shows cross-sectional views of these structures after thermal oxidation. These nanowires form the channel region of a wrapped-around-gate nanochannel MOSFET as described in Section 3.

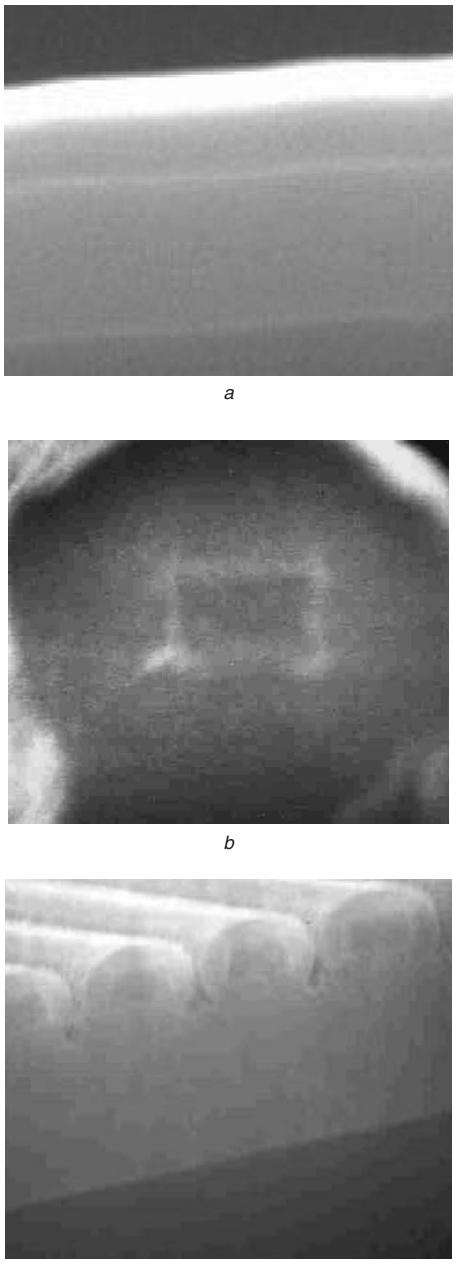

Fig. 1 *SEM micrographs showing results of thermal oxidation*
a SOI slab gate region
b single nanowire surrounded by thermally grown SiO_2
c multiple parallel nanowires surrounded by thermally grown SiO_2

3 Nanowire WAG channel and top-only-gate slab MOSFET fabrication

Nanowires were fabricated using the processes described in Section 2 in localised channel/gate areas of the MOSFET devices using IL, along with conventional I-line contact mask printing [11] for defining the device source and drain regions. For comparison, we also fabricated MOSFET devices with slab top-only-gate regions.

Figure 2 shows a process flow sequence. A 10–22 Ω-per-square bare silicon on insulator (SOI) wafer with a 200 nm thick active Si layer on top of a 400 nm thick buried oxide (BOX) isolation layer was spin coated with photoresist (PR) and exposed to an interference pattern as described above. A 30 nm thick blanket layer of Cr was then deposited by e-beam evaporation and a lift-off step was used to create an array of Cr lines that are an effective RIE etch mask. In order to localise the Cr lines to the regions where the wires would be produced, the wafer was again spin coated with a PR layer and a mask was then used to selectively pattern the PR to protect portions of the Cr lines from a chemical

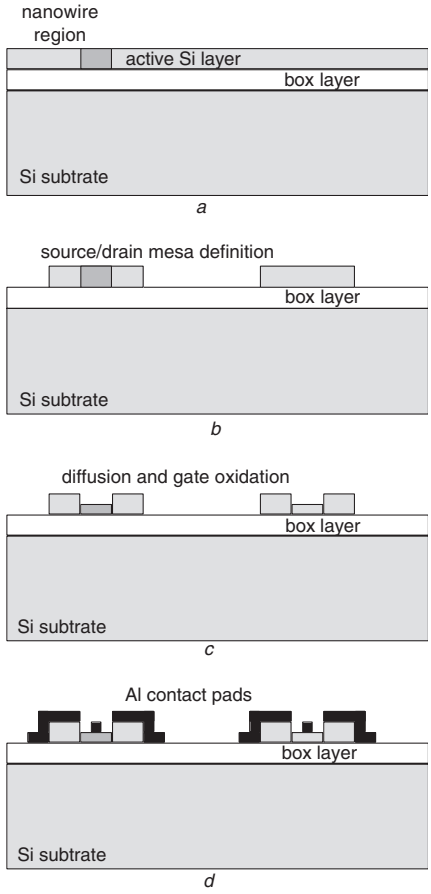

Fig. 2 *Process flow sequence for fabrication of nanowire wrap-around-gate MOSFET (left) and slab-top-only-gate MOSFET device (right)*

Cr-etch solution. Once the Cr was etched from the unwanted regions, the PR was removed. Once again a layer of PR was applied on to the sample to define the source and drain regions. The source and drain definition mask was aligned to the Cr lines (gate pattern). After the exposure and develop processes, the remaining structure had source and drain mesas masked by PR and Cr lines masking the gate region between the source and drain regions. The samples were then etched to the BOX layer by RIE, thus defining the channel and source/drain regions. Figure 3 shows SEM micrographs of a slab gate and nanowire gate structures before thermal oxidation. Basically at this point we have two mesa structures (source and drain regions) connected by a wide slab or by wires, respectively. After the RIE step the PR and the Cr etch mask lines were removed. There is considerable damage left by the RIE step. In order to remove some of this damage, two rapid thermal anneal (RTA) steps were performed. The first RTA was performed at 900°C for 5 min in a nitrogen environment to anneal the damaged surface [12] followed by a second RTA step for 3 min at 450°C in a hydrogen environment to passivate the Si surfaces. Next a thick ~0.5 μm thick silicon nitride layer was deposited on to the samples to be used as a diffusion mask. A layer of PR was spin coated on to the wafer and windows were opened in the nitride layer above the source and drain regions using buffered oxide etch (BOE) solution. PR was removed and a layer of phosphorous spin on glass (PSG) was coated on to the sample for the pre-deposition step that was performed at ~900°C for 5 min. Next the PSG and nitride layers were removed using BOE. The gate oxidation and dopant drive-in were performed in a single thermal step using an oxidation furnace at 1000°C. As a thermal oxide was grown around the wire structures it consumed the Si, thus decreasing the width of the wire. Careful characterisations were performed in order to optimise the thermal process in order to result in a Si nanowire region diameter of ~50 nm. This process grew a gate oxide that was ~60 nm thick around the nanowires. Similarly a ~60 nm gate oxide was grown on the slab gate devices in order to minimise any oxide capacitance (C_{ox}) effects in our final analysis. The time for the oxidation to yield ~50 nm diameter Si wires drove some of the dopant into the channel region. Figure 4*a* shows a process simulation of the predicted phosphorous impurity content in the wires. The resultant doping profile resulted in an $n^+n^-n^+$ structure as shown in the process simulation (Fig. 4*b*–4*c*), which shows the modelled impurity profiles before and after the oxidation/diffusion process. Next a layer of PR was deposited and patterned for metallisation. A 300 nm thick Al layer was e-beam deposited using multiple shadow evaporations and liftoff in order to achieve conformal gate coverage. The samples were cleaned and annealed at ~430°C in a rapid thermal anneal (RTA) to create ohmic contacts at the source and drain region. Completely fabricated single and multiple nanowire channel WAG MOSFETs and top-only-gate slab MOSFET are shown in Fig. 5.

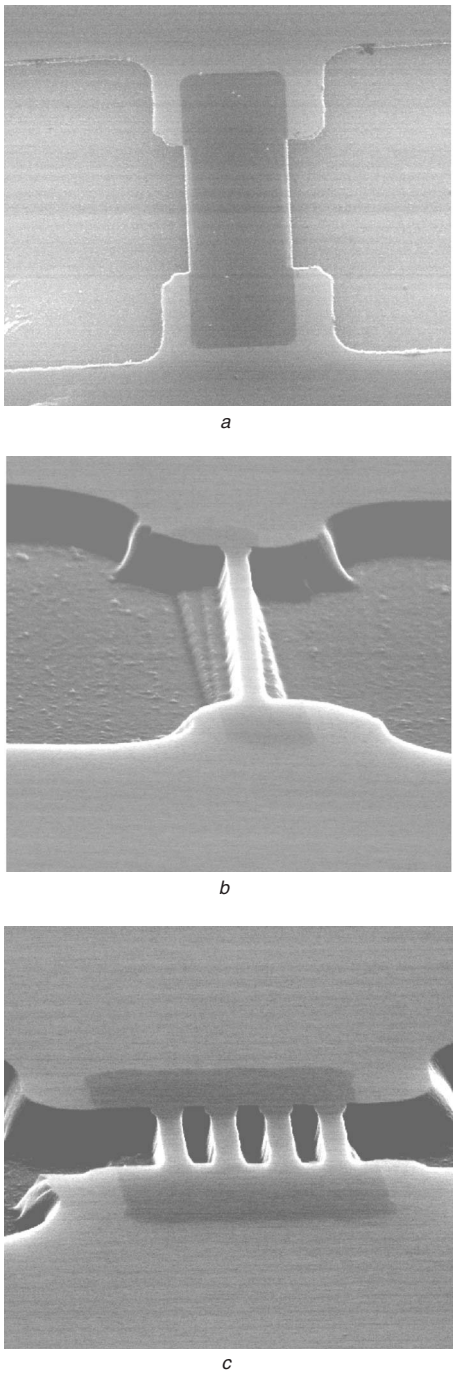

Fig. 3 *SEM micrographs of slab structure and precursors to single and multiple nanowire gate structures*
a Slab structure connecting top source mesa region and bottom drain mesa region
b Precursor to nanowire gate structure connecting source and drain mesa regions
c Precursor to multiple nanowire gate structure connecting source and drain mesa regions

4 Current–voltage measurements, modelling, and analysis

Experimental *I–V* plots for both the nanowire and slab devices are shown in Fig. 6. The drain current (I_d) as a function of drain-to-source voltage (V_{ds}) for various gate biases was measured using a digital curve tracer. As seen from the plots, for similar doping profiles, gate length and gate oxide thicknesses the current–voltage characteristics of the nanowire and slab MOSFET are considerably different. The drain current in the nanowire is rather flat in the saturation region ($V_{ds} > 1$ V) compared to the significant slope in the slab device. This is due to the geometry of the slab MOSFET, in which the fringing fields at the edges of the slab significantly impact the drain current. As the channel approaches pinch-off, the carrier charge drops at the drain end and the lateral fringing field increases at the edges of the slab. Further increasing V_{ds} causes the high-field region at the drain end to widen the channel enough to accommodate the additional potential drop, thus resulting in a further increase in the drain current. In contrast, when

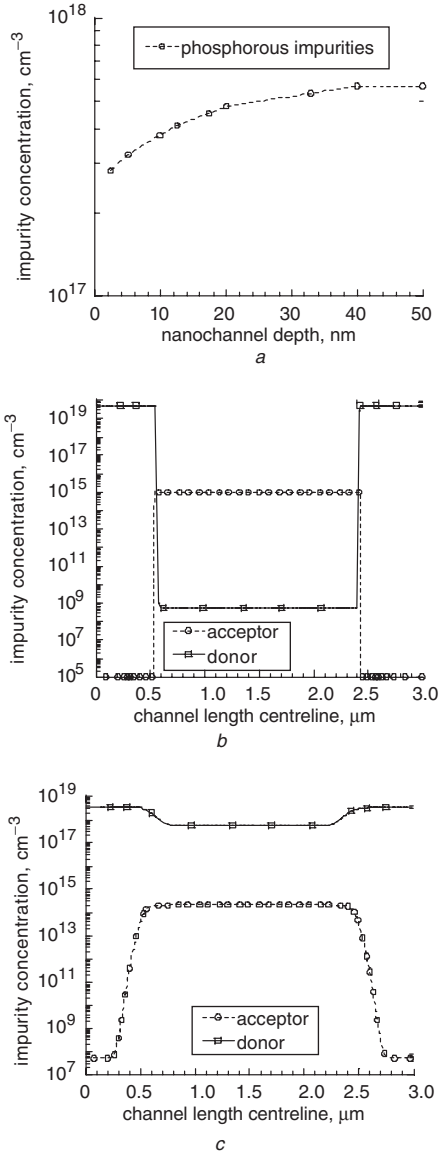

Fig. 4 *Simulation plots of impurity concentrations*
a Impurity concentration through the nanowire diameter width from the base of the nanowire ($x = 0$ nm) to the top surface ($x = 50$ nm)
b Pre-diffusion impurity concentration of acceptors (substrate doping) and donors (phosphorous doping) throughout the source–gate–drain regions
c Post-diffusion impurity concentration of both acceptors and donors throughout the source–gate–drain regions

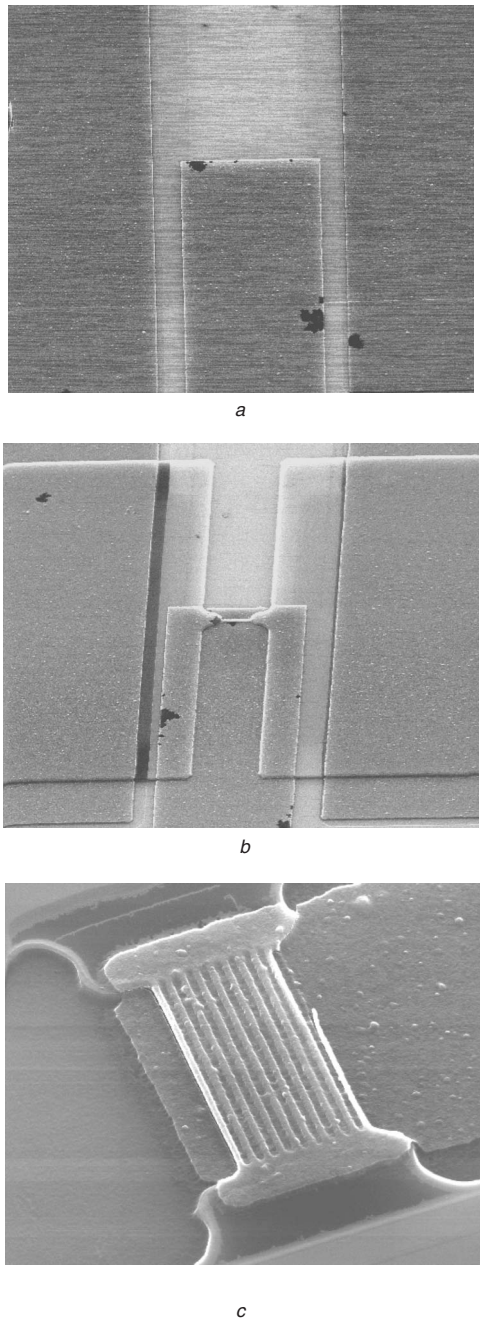

Fig. 5 *SEM micrographs of various MOSFET structures*
a Slab-MOSFET where the centre electrode is the gate surrounded by the source and drain electrodes
b Single nanowire-MOSFET
c Multiple nanowire-MOSFET

the nanowire device is biased in the saturation region, the effective channel length of the nanowire device is essentially unaffected since the depletion region at the drain terminal is physically restricted to ~ 50 nm. This effect, known as channel length modulation, is a well-known phenomenon in conventional transistor designs [13]. This phenomenon is more dominant in conventional short channel devices. Suppressing such effects in the $\sim 1 V_{ds}$ nanowire device (as is the case here) is of significant benefit, specifically in the development of low voltage circuit applications.

Figure 6 shows that in the nanowire MOSFET the current is an order of magnitude less than for the slab device. Scaling to the cross-sectional area shows that the nanowire device current density is three times higher than that of the planar slab device. From the experimental data the resultant conductivities for the slab and nanowire devices are $\sigma_{slab} \sim 9 \times 10^3$ A/V cm^2 and $\sigma_{wire} \sim 3 \times 10^4$ A/V cm^2. This means that we can obtain the same amount of total current driving capability in nanowire channel devices that have much smaller cross-sections by configuring several nanowires in parallel. In order to understand and improve the current characteristics of the nanodevice, we also modelled the current–voltage characteristics of the transistors. We are not aware of any reported standard nanowire channel wrap-around-gate MOSFET drain current-voltage (I_d–V_{ds}) relations and in order simulate the results we developed a very simple model based on the 2-D sketch of Fig. 7*a*.

Poisson's equation in cylindrical coordinates can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi}{\partial r}\right) = -\frac{\rho}{\varepsilon_s} \quad (1)$$

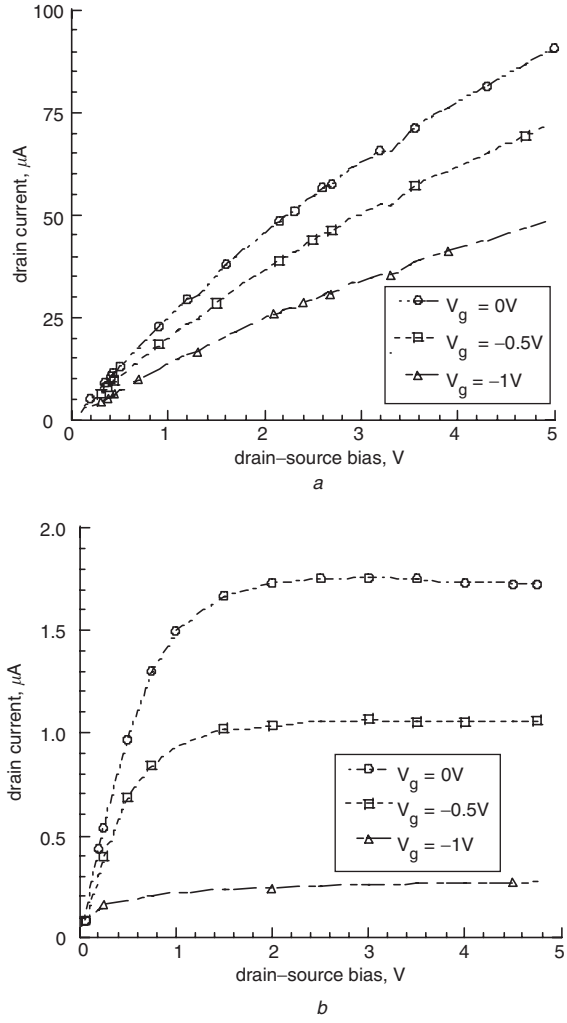

Fig. 6 *Experimental plots of drain current as a function of drain-to-source bias for various gate voltages*
a Slab-MOSFET
b Single nanowire-MOSFET

where ψ is the electron potential, r is the radius vector, ρ is the charge density per unit volume, and ε_s is the dielectric constant of silicon.

We assume that the average charge in the cylindrical channel is

$$Q_{\text{average}} \approx (Q_S + Q_D)/2 \tag{2}$$

where Q_S is the charge per unit area in the channel near the source and Q_D near the drain regions. The current density in the channel can be then approximated by

$$J_d \approx -Q_{\text{average}} v_{\text{drift}} \tag{3}$$

where v_{drift} is the channel region carrier drift velocity. The cylindrical nanowire oxide capacitance $C_{\text{r ox}}$ near the source and drain regions can be written as a function of the regional charge and applied source, drain and gate potentials as follows:

$$\begin{aligned} C_{\text{rox}} &= -(Q_s/V_{\text{gs}} - V_t) \\ &= -Q_D/(V_{\text{gd}} - V_t), \text{ where } V_{\text{gd}} = V_{\text{gs}} - V_{\text{ds}} \end{aligned} \tag{4}$$

where V_{gs} is the gate-to-source potential, V_{dg} is the drain-to-gate potential, and V_t is the threshold voltage.

Substituting Q_S and Q_D into the equation for J_d results in

$$J_d \approx C_{\text{rox}}[(2V_{\text{gs}} - Vt - V_{\text{ds}})/2]v_{\text{drift}} \tag{5}$$

Thus the current density J_d depends on the drift velocity, the drain and gate biases and the channel capacitance. Any

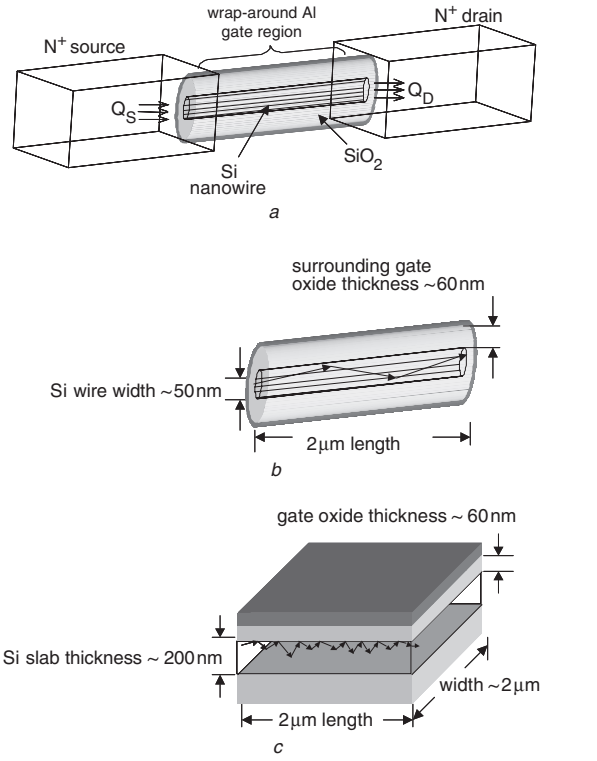

Fig. 7 *Schematic views of nanowire WAG MOSFET and carrier conduction*
a Schematic configuration of a nanowire WAG MOSFET
b Carrier conduction through a nanowire gate
c Carrier conduction through a slab gate

variation in these parameters will be reflected in the current density value. Since the channel capacitance per unit area (F/cm^2) is fixed for a given oxide thickness and because the oxide thickness is about the same (~60 nm) for both the nanowire and the bulk devices, the capacitance per unit area effect may not contribute significantly to the current density. Neglecting contributions from the terminal bias effects, the major contribution comes from the drift velocity component. The drift velocity is a function of carrier mobility while the mobility itself depends on the electric field in the channel. The electric field at any channel region is the vector sum of the parallel ($E_{\parallel}$) and transverse ($E_{\perp}$) component, where $E_{\parallel}$ is in the direction of the current flow. It may be noted that even without significant change in 'actual' mobility, changes in parallel and transverse electric field component can alter the mobility (carrier velocity) components (and hence the drain current) significantly. For example, the magnitude of the E-field at any point can be written as $|\vec{E}| = \sqrt{\vec{E}_{\perp}^2 + \vec{E}_{\parallel}^2}$ which can be satisfied by various values for $E_{\perp}$ and $E_{\parallel}$. (e.g. $|E| = \sqrt{50}\,\text{kV/m}$ is satisfied for $E_{\perp} = 5\,\text{kV/m}$ and $E_{\parallel} = 5\,\text{kV/m}$, or $E_{\perp} = 1\,\text{kV/m}$ and $E_{\parallel} = 7\,\text{kV/m}$). The increase in $E_{\parallel}$ (second case), results in an increase in the parallel drift velocity, thus increasing current flow. The hypothesis stated above was tested through incorporating mathematical models for mobility and electric fields in the channel regions of the devices. Most mobility models incorporate saturation at high parallel field of the form as suggested by Thornber [14],

$$\begin{aligned} v_{\text{drift}}(E_{\parallel}, E_{\perp}, N_I, T) = \mu(E_{\perp}, N_I, T).\{1 \\ + [\mu(E_{\perp}, N_I, T)E_{\parallel}/v_s(T)^{\beta}]^{1-\beta}\}.E_{\parallel} \end{aligned} \tag{6}$$

where N_I is the local impurity concentration, and T is the absolute temperature. The carrier saturation velocity, v_s in the channel region is assumed independent of normal electric field, impurity concentration, and direction of current flow with respect to the crystal orientation. The fitting parameter β has been well characterised with a value of 2 for both electrons and holes [15]. Besides the electric field dependence, other mechanisms such as acoustic phonon scattering, impurity scattering and surface scattering also contribute to the mobility. Thus the mobility can be approximated by the sum of the following terms, [16, 17]:

$$1/\mu = 1/\mu_{ac} + 1/\mu_b + 1/\mu_{sr} + 1/\mu_{Coulomb} \quad (7)$$

where $\mu_{ac,}$ is the mobility limited by scattering acoustic phonons and is given by [17]

$$\mu_{ac} = qh^3\rho\mu_I/(m^* m_\mu Z_A^2 k_B T) \quad (8)$$

where q is the elementary charge, h is Dirac constant, μ_I is the sound velocity, m^* and m_μ is the effective mass and mobility mass, respectively, Z_A is the deformation potential, k_B is the Boltzmann constant, T is the absolute temperature and ρ is the areal mass density of silicon.

The bulk mobility of silicon μ_b is given by [18]

$$\mu_b(N_I, T) = \mu_0 + (\mu_{max}(T) - \mu_0)/[1 + (N_I/C_r)^\alpha] - \mu_1/[1 + (C_s/N_I)^\beta] \quad (9)$$

where N_I is the local impurity concentration, μ_{max} is the ohmic (pure-lattice) electron mobility, C_r and C_s are fitting parameters and α, β, μ_1 are model parameters for electrons or holes where the values can be found in Masetii *et al.* [16] For example, $\mu_{max} = 1417\,cm^2/Vs$, $\mu_0 = 52.2$ and $44.9\,cm^2/Vs$ for electrons and holes respectively.

μ_{sr} is the mobility limited by surface roughness scattering and is given by [19]

$$\mu_{sr}(E_\perp) = \delta/E_\perp^2 \quad (10)$$

where $E_\perp$ is the transverse electric field and δ is a model parameter and is $5.82 \times 10^{14}\,V/s$ and $2.0546 \times 10^{14}\,V/s$ for electrons and holes respectively [20].

$\mu_{Coulomb}$ is due to the effect of Coulomb scattering, which is mainly due to oxide fixed charge and surface states charge and can be found from [20]

$$\mu_{Coulomb} \propto T/Q_f \quad (11)$$

where Q_f is the fixed oxide charge and T is the absolute temperature.

Details of mobility models and parameters for non-planar structures can be found in Lombardi *et al.* [21] and will not be discussed here. However, it is important to note that μ_{sr} is the main reason for the higher mobility in the nanowire devices, and that the values of μ_{ac}, μ_b, $\mu_{Coulomb}$, are comparable for both devices. The carrier transport is based on changes in the mobility components due to transverse and parallel electric fields, and is also due to the physics described in (8)–(11), which is reflected in the final mobility value and hence the drift velocity component. Any reduction in the transverse field (expected to be minimum near the centre of the nanowires) increases the μ_{sr} component (10) and the overall mobility value in the Mathiesen's summation (7). In the slab device, the transverse field is directed from the top towards the substrate, while in the wrap around gate structure, the transverse field is directed from all around and is minimum at the centre. Thus, due to the electric field configuration affecting the surface interactions the mobility is expected to increase at the centre of the nanowires. Figure 7*b*–7*c* shows an expected schematic model of the carrier transport mechanism for both nanochannel and slab devices. For reasons discussed above, the nanowire is expected to show 'enhanced forward' motion compared to the conventional MOSFET surface scattering model for the slab geometry.

Figures 8 and 9 show a 2D simulation plot of carrier parallel ($\mu_{||}$) and perpendicular ($\mu_\perp$) mobilities for both slab and nanochannel devices. In the slab device (Fig. 8*a*) the mobility is lower at the Si–SiO_2 interface due to surface interactions and the large transverse electric field. Further away from the interface in the perpendicular direction these effects decrease and the mobility increases and levels out to the bulk mobility value. The dip in $\mu_\perp$ is due to the location of the edge of the depletion region where the field-

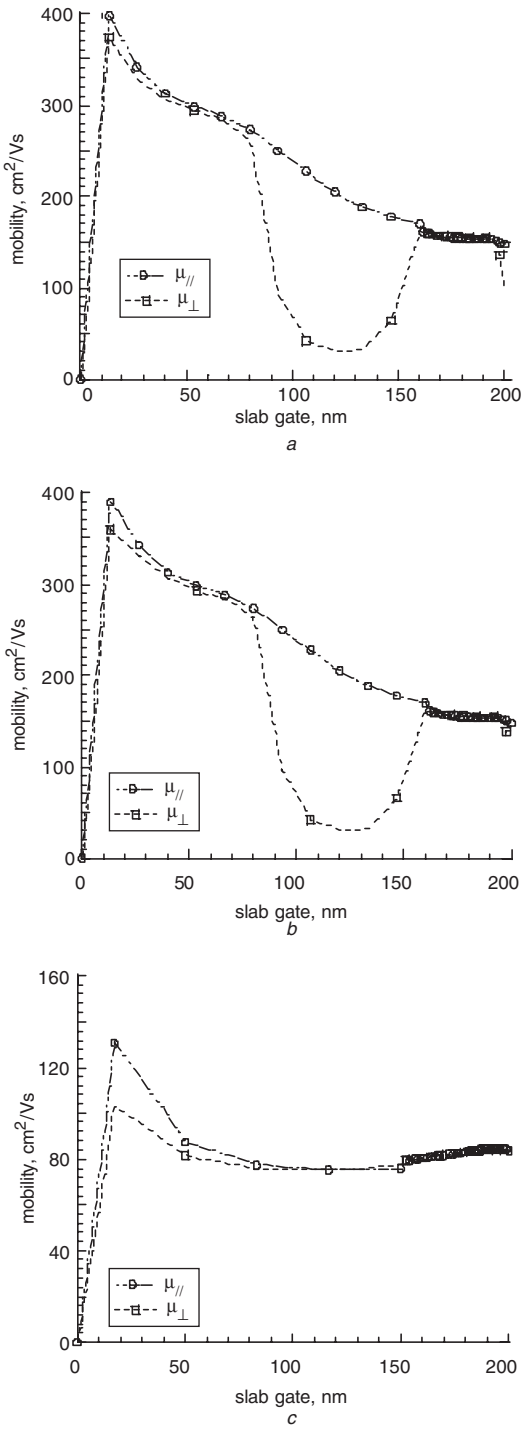

Fig. 8 *Simulation plots for slab channel carrier mobility in the parallel and transverse directions for various gate biases*
a $V_g = 0\,V$
b $V_g = -0.5\,V$
c $V_g = -1.0\,V$

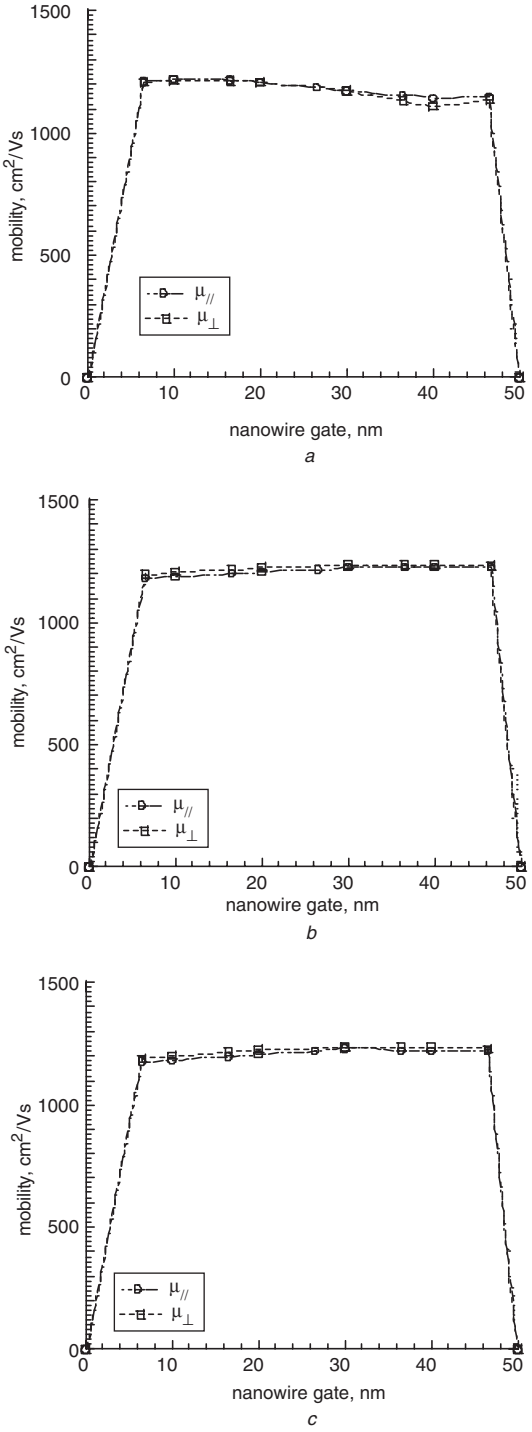

Fig. 9 *Simulation plots for nanowire channel carrier mobility in the parallel and y transverse directions for various gate biases*
a $V_g = 0\,V$
b $V_g = -0.5\,V$
c $V_g = -1.0\,V$

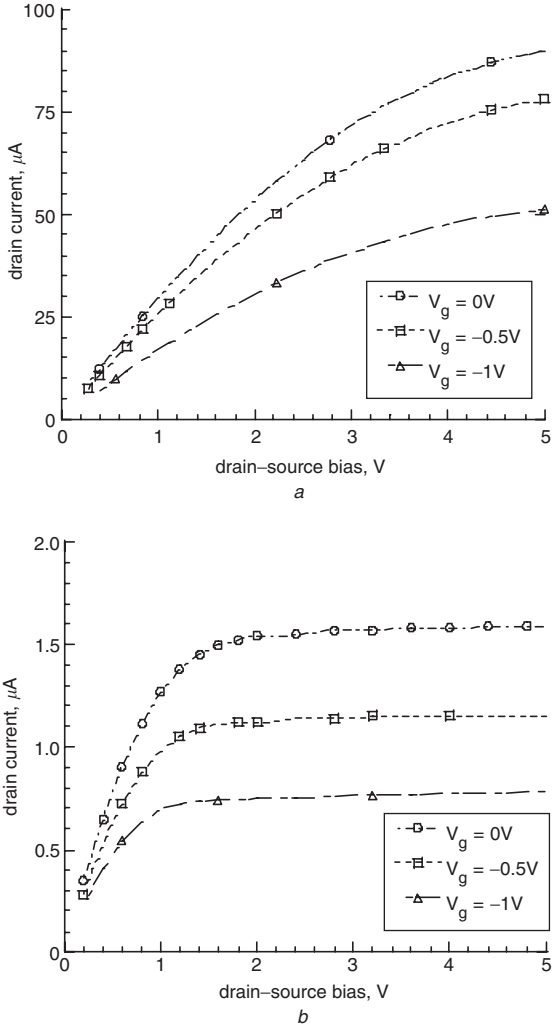

Fig. 10 *Simulation plots of drain current as a function of drain–source bias for various gate biases*
a Slab-MOSFET;
b Single-nanowire MOSFET

dependent component drops rapidly. The nanowire device (Fig. 9*a*) shows similar trends but the mobility at the channel centre is about three times larger than the slab devices. The enhanced mobility is due to the fact that the transverse field has an equipotential configuration in the channel instead of from the top only as in the slab case. This results in an improved parallel electric field distribution through the centre of the cross-sectional channel region, where the surface scattering and Coulomb effects are also minimal. Figures 8*b*–8*c* and 9*b*–9*c* show plots of the effects of applying gate bias (transverse electric field) on carrier mobility for both wire and slab devices. As can be seen from the plots the variations in transverse electric field are more pronounced in the slab gate devices compared to the nanowire channel devices. Figure 10 shows simulated *I–V* characteristics for the ~50 nm channel device at different gate biases. The results are in agreement with the measured *I–V* for the fabricated single channel device as shown in Fig. 6. The close match between the simulated and measured *I–V* plots is an indication of the validity of the model and material parameters chosen for the simulation.

The simulation also shows that the nanowire channel device has characteristics that are somewhat similar to a buried channel MOSFET [22]. Our simulations show that the *I–V* characteristic of the device is very sensitive to the doping profile of the narrow ~50 nm thick channels. The best fit is for the case where an n-type dopant is near the upper surface and decreases monotonically in the *y*-direction (Fig. 4). This profile is expected since during the fabrication process the source and drain were diffused at 1000°C with an n-type dopant with a peak concentration of $10^{18}\,cm^{-3}$. It is very likely that diffusion into the channel region also took place. The net effect is the creation of a device very similar to a normally-on n-buried channel MOSFET. The channel doping profile prior to and following the diffusion process is different as is evident from the process simulation in Fig. 4 [23]. As can be anticipated, during device operation the conducting channel is the n-region rather than an inversion layer at the $Si–SiO_2$

interface as would normally be the case if the p-type channel were the dominant dopant. Buried n-layer MOSFETs have been analysed and the physics of the device I–V characteristics for the linear and saturation regions are different from that for an inversion layer formed at the Si-SiO_2 interface [24].

5 Subthreshold currents

The subthreshold region performance is particularly important when evaluating the suitability of MOSFETs for low voltage, low power applications, such as when the MOSFET is used in high bit rate switching applications. The subthreshold currents as a function of gate bias are shown in Fig. 11 for a single WAG nanochannel and slab devices. As can be seen from the figure the current drops about three decades for a small ($\Delta V \sim 0.1$ V) variation in the gate bias. In contrast, the subthreshold current in the slab gate device did not drop one decade for a much larger variation in gate bias. Typical nanochannel devices characterised had ~ 50 nm width Si surrounded by ~ 60 nm oxide with an Al wrap-around-gate electrode and the slab devices had ~ 200 nm thick Si that was $\sim 2\,\mu$m wide with a ~ 60 nm thick oxide with top only Al gate. Both nanochannel and slab channels were $\sim 2\,\mu$m long. From Fig. 11 we can calculate the gate voltage swing S using the standard definition given by (12), which results in a subthreshold slope of ~ 100 mV/decade for the nanowire MOSFET.

$$S = \ln 10[dV_G/d(\ln I_D)] \tag{12}$$

Since the subthreshold current did not drop even one decade we extrapolated the subthreshold slope to be ~ 4 V/decade for the slab gate devices where the current cannot be effectively turned off. This is due to the fact that these devices do not have a typical n-channel MOSFET doping profile but are essentially buried channel devices with an $n^+n^-n^+$ doping profile in which there are sufficient carriers in the channel for conduction even at 0 V gate bias.

Considering we have a similar doping profile for the nanowire channel device that has a gate oxide thickness of ~ 60 nm, the subthreshold performance is truly remarkable. These results also demonstrate that narrow channels provide better control over the channel potential due to the enhanced gate control from all sides in contrast with only the front surface coverage in conventional planar transistors, even for these unconventional device-doping profiles.

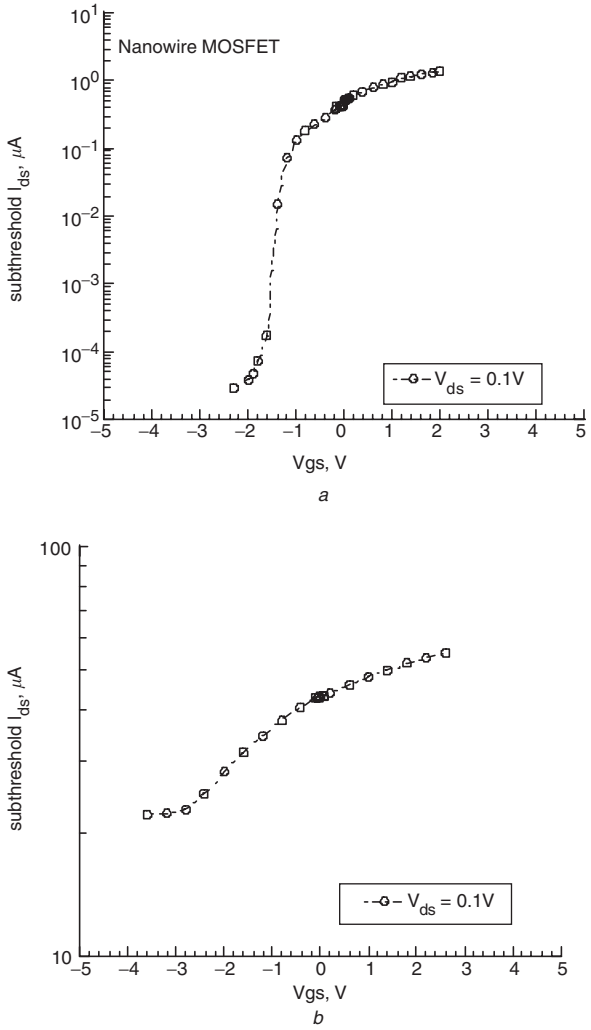

Fig. 11 *Measured subthreshold drain current plots as a function of gate bias*
a Nanowire WAG MOSFET
b Slab top only gate MOSFET

6 Analysis and conclusion

Through experiments and simulation, we have explained the carrier transport properties of Si nanowire channel wrap–around–gate MOSFET. Nanowire WAG MOSFET devices were fabricated along with slab top-only-gate MOSFETs for a comparative study. Interferometric lithography was used to define the nanowire in the channel region and conventional lithography was used to define the source and drain regions. Devices characterised had ~ 50 nm diameter wire channels and ~ 200 nm thick, $\sim 2\,\mu$m wide slab regions that were both $\sim 2\,\mu$m in length. In future studies we plan to investigate shorter devices to understand non-equilibrium effects as a function of lateral and transverse dimensions. A semi-empirical carrier mobility model for non-planar silicon structures was used to model the current–voltage characteristics. Simulation results show good agreement with experiment. Analysis showed that the current density is about ~ 3 time higher in the nanowire channel WAG devices as then in the slab devices. This is primarily due the average higher carrier mobilities in the nanowire channel devices as well as conformal uniform electric flux densities in the wire devices. Study also shows that MOSFET width scaling is possible while maintaining the current driving capability high by integrating multiple nanowires in parallel. The experimental results showed that the current was a linear function of the number of wires.

7 Acknowledgment

The authors would like to thank Mr Richard Marquardt for assisting in the experimental setup for the subthreshold response, Dr P. Varangis for assisting in the critical fabrication steps of the devices, and Mr George Jzeremes for setting up the computer simulations.

8 References

1 Wind, S.J., *et al.*: 'Lithography and fabrication processes for sub-100nm scale complementary metal-oxide-semiconductor', *J. Vac. Sci. Technol. B*, 1995, **13**, (6), pp. 2688–2695
2 Fritze, M., Astolfi, D., Liu, H., Chen, C.K., Suntharalingam, V., Preble, P., and Wyatt, D.W.: 'Sub-100 nm KrF lithography for complementary metal-oxide-semiconductor circuits', *J. Vac. Sci. Technol. B*, 1999, **17**, (2), p. 345–349
3 Auth, C.P., and Plummer, J.D.: 'Scaling theory for cylindrical, fully-depleted surrounding-gate MOSFET's', *IEEE Electron Device Lett.*, 1997, **18**, (2), p. 74–76

4 Suzuki, K., Tanaka, T., Tosaka, Y., Horie, H., and Arimoto, Y.: 'Scaling theory for double-gate SOI MOSFETs', *IEEE Trans. Electron Devices*, 1993, **40**, (12), p. 2326
5 Colinge, J.P., Gao, M.H., Rodriguez, A.R., and Claeys, C.: 'Silicon-on-insulator gate-all-around devices', *IEDM Tech. Dig.*, 1990, pp. 595–598
6 Persans, P. D., Lurio, L.B., Pant, J., Lian, G.D., and Hayes, T.M.: 'Zn incorporation in Cds nano particles in glass', *Phys. Rev.*, 2001, **63**, pp. 115320(1)–115320(8)
7 Leobandung, E., Gu Gian, Lingjie, G., and Chao, S.Y.: 'Wire-channel and wrap-around-gate metal-oxide semiconductor field-effect transistors with a significant reduction of short channel effects', *J. Vac. Sci. Technol., B*, 1997, **5**, (6), p. 2791
8 Chen, X., and Brueck, S.R.J.: 'Imaging interferometric lithography: a wavelength division multiplex approach to extending optical lithography', *J. Vac. Sci. Technol.*, 1998, **B16**, pp. 3392–3397
9 Zaidi, S.H., and Brueck, S.R.J.: 'Multiple exposure interferometric lithography', *J. Vac. Sci. Technol.*, 1993, **B11**, p. 653
10 Zaidi, S.H., and Brueck, S.R.J.: 'Si-texturing with sub-wavelength structures', *Proc. 26th IEEE Photovoltaic Specialists Conf. PVSC*, 1997, **26**, pp. 171–174
11 Zaidi, S.H., Brueck, S.R.J., Hill, T., and Shagam, R.N.: 'Mix and match interferometric and optical lithographies for nanoscale structuring', *Proc SPIE*, 1998, **3331**, p. 406–413
12 Wolf, S., and Tauber, R.N.: 'Silicon Processing for the VLSI Era' (Lattice Press, 1986), Vol. **1**, pp. 57–58
13 Gary, P.R., and Meyer, R.G.: 'Analysis and Design of Analog Integrated Circuits' (John Wiley & Sons, Inc., 1993, 3rd edn.), pp. 59–66
14 Thornber, K.K.: 'Relation of drift velocity to low-field mobility and high-field saturation velocity', *J. Appl. Phys.*, 1980, **51**, pp. 2127–2136
15 Masetti, G., Severi, M., and Solmi, S.: 'Modeling of carrier mobility against carrier concentration in arsenic-, phosphorous-, and boron-doped silicon', *IEEE Trans. Electron Devices*, 1983, **ED-30**, pp. 764–769
16 Sah, C.T., Ning, T.H., and Tschopp, L.L.: 'Scattering of electrons by surface oxide charges and by lattice vibrations at the silicon-silicon dioxide interface', *Surf. Sci.*, 1972, **32**, pp. 561–575
17 Deybe, P.P., and Conwell, E.M.: 'Electrical properties of n-type germanium', *Phys. Rev.*, 1954, **93**, pp. 693–706
18 Masetti, G., Severi, M., and Solmi, S.: 'Modeling of carrier mobility against concentration in arsenic-, phosphorous-, and boron-doped silicon', *IEEE Trans. Electron Devices*, 1983, **ED-30**, pp. 764–769
19 Fang, F.F., and Fowler, A.B.: 'Electron scattering in inverted silicon surfaces', *Phys. Rev. B*, 1968, **169**, (3), pp. 619–631
20 Goodnick, S.M., Gann, R.G., Ferry, D.K., Wilmsen, C.W., and Krivanek, O.L.: 'Surface roughness induced scattering and band tailing', *Surf. Sci.*, 1982, **113**, pp. 233–238
21 Lombardi, C., Manzini, S., Saporito, A., and Vanzi, M.: 'A physically based mobility model for numerical simulation of nonplanar devices', *IEEE Trans. Computo-Aided Design*, 1988, **7**, (11)
22 Sze, S.M.: 'Physics of Semiconductor Devices' (John Wiley and Sons, NY, 1981, 2nd edn.), Chap. 8
23 Process simulation software, Athena, Silvaco International Software, Users Manual, 2000
24 Merckel, G.: 'Ion Implanted MOS Transistors-Depletion Mode Devices', *in* Engle, F. and Jespers, W.L. (Eds.) 'Process and Device Modeling for IC Design' (Noordhoff, Leyden, 1977)