

TECHNICAL DOCUMENT 3196
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DC and RF Characterization of Laser Annealed Metal-Gate SOI CMOS Field-Effect Transistors

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DC and RF Characterization of Laser Annealed Metal-Gate SOI CMOS Field-Effect Transistors

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Jason Rowland, Stephen D. Russell*

Space and Naval Warfare Systems Center
San Diego

American Physical Society
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Abstract

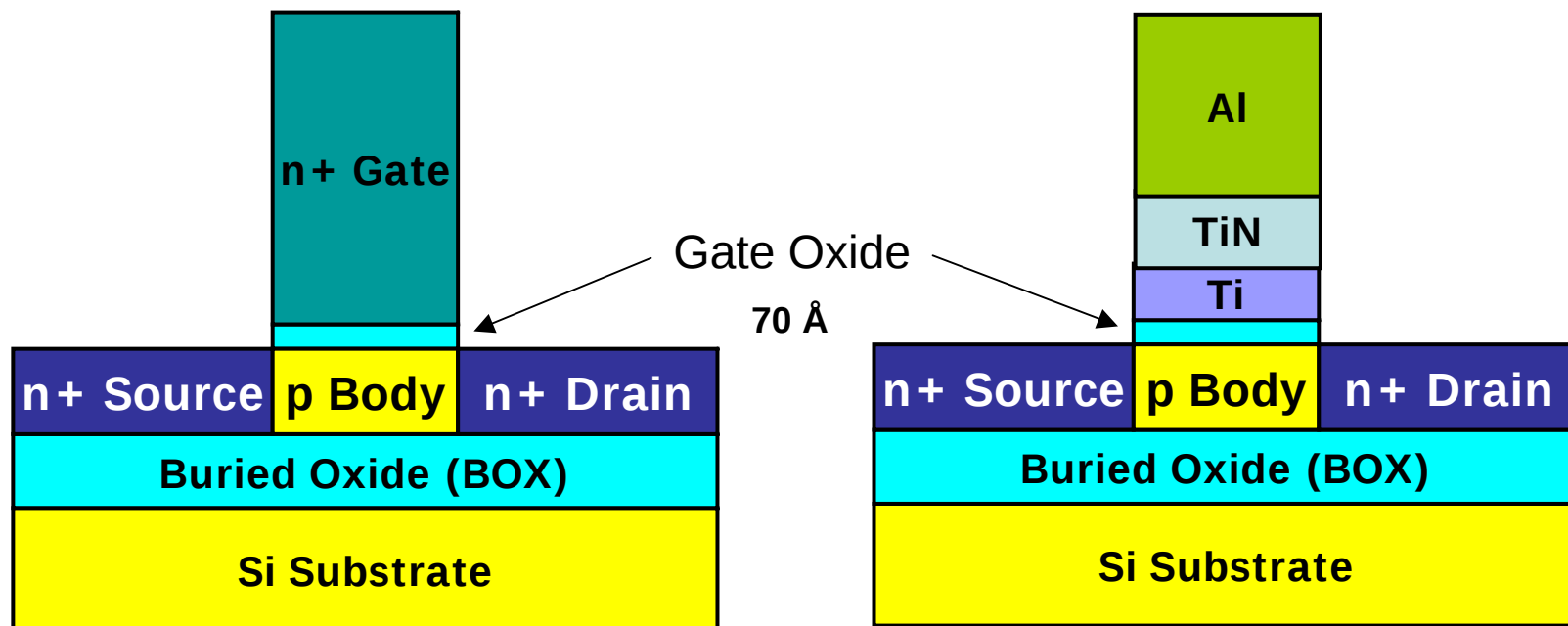
The conventional polysilicon gate in a MOSFET has been replaced by an aluminum metal gate which offers higher RF performance through the reduction of gate resistance. Pulsed excimer laser annealing of the source and drain was then used to avoid conventional furnace annealing that would melt the aluminum metal gate. CMOS field-effect transistors utilizing metal gates were fabricated in Silicon-on-Insulator (SOI) technology down to 0.25-micron gate lengths. The DC characteristics of devices with 10-micron gate lengths were consistently well-behaved. The 0.25-micron devices were found to be more sensitive to the laser energy that showed up in the DC measurements in threshold voltage variations and larger leakage currents in the subthreshold characteristics. At higher laser fluences, Technology Computer-Aided Design (TCAD) simulations show excessive lateral diffusion, explaining the observed effects. RF results of the drawn 0.25-micron metal-gate devices have an F_t and F_{max} of 25 GHz and 60 GHz, respectively. Similar devices with polysilicon gates were fabricated and characterized for comparison. RF results of the drawn 0.25-micron polysilicon-gate devices have an F_t and F_{max} of 34 GHz and 7 GHz, respectively. This device processing advance offers a deeply scalable technology for future “system-on-a-chip” applications.

Why use SOI?

As devices are scaled down in size, MOSFET performance suffers from short channel effects and the parasitic resistances and capacitances become more apparent in RF applications. These parasitics limits the potential to achieve a high cutoff frequency and power gain, F_t and F_{max} , respectively. Silicon-on-insulator technology reduces the short channel effects as well as parasitic junction capacitances for improved microwave frequency figures of merit.

Why use Metal Gates?

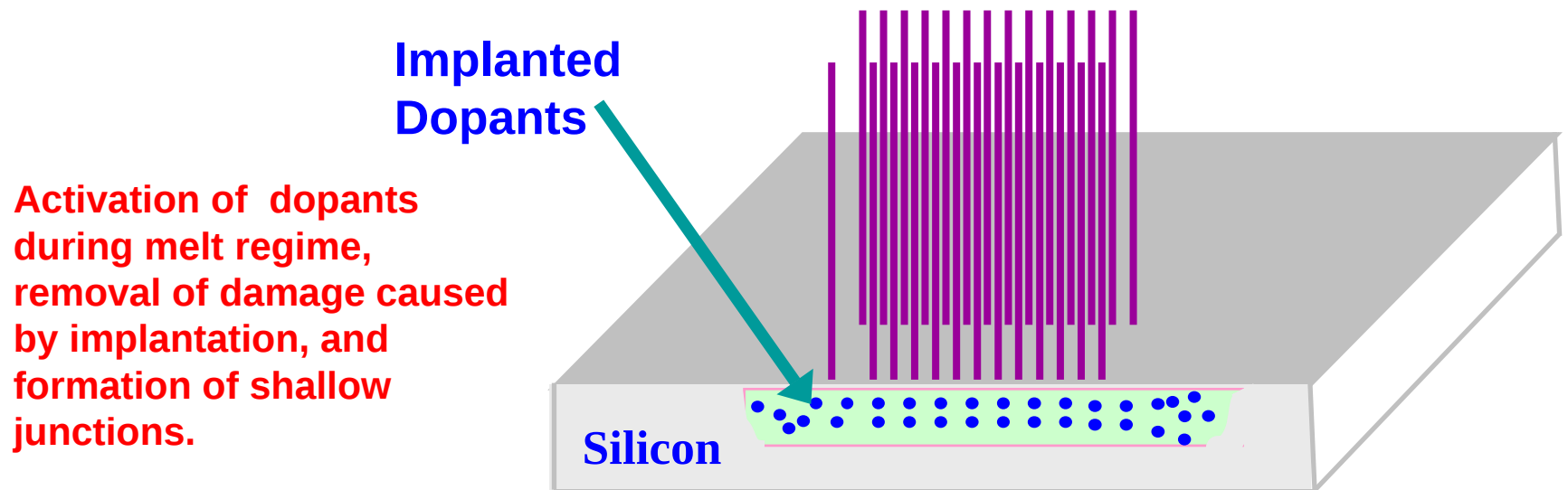
Using Al as the material for the metal gate creates a device that has at least an order of magnitude lower gate resistance than a silicide polygate. Reducing the gate resistance directly improves the RF performance of the device.



Why Use Laser Annealing?

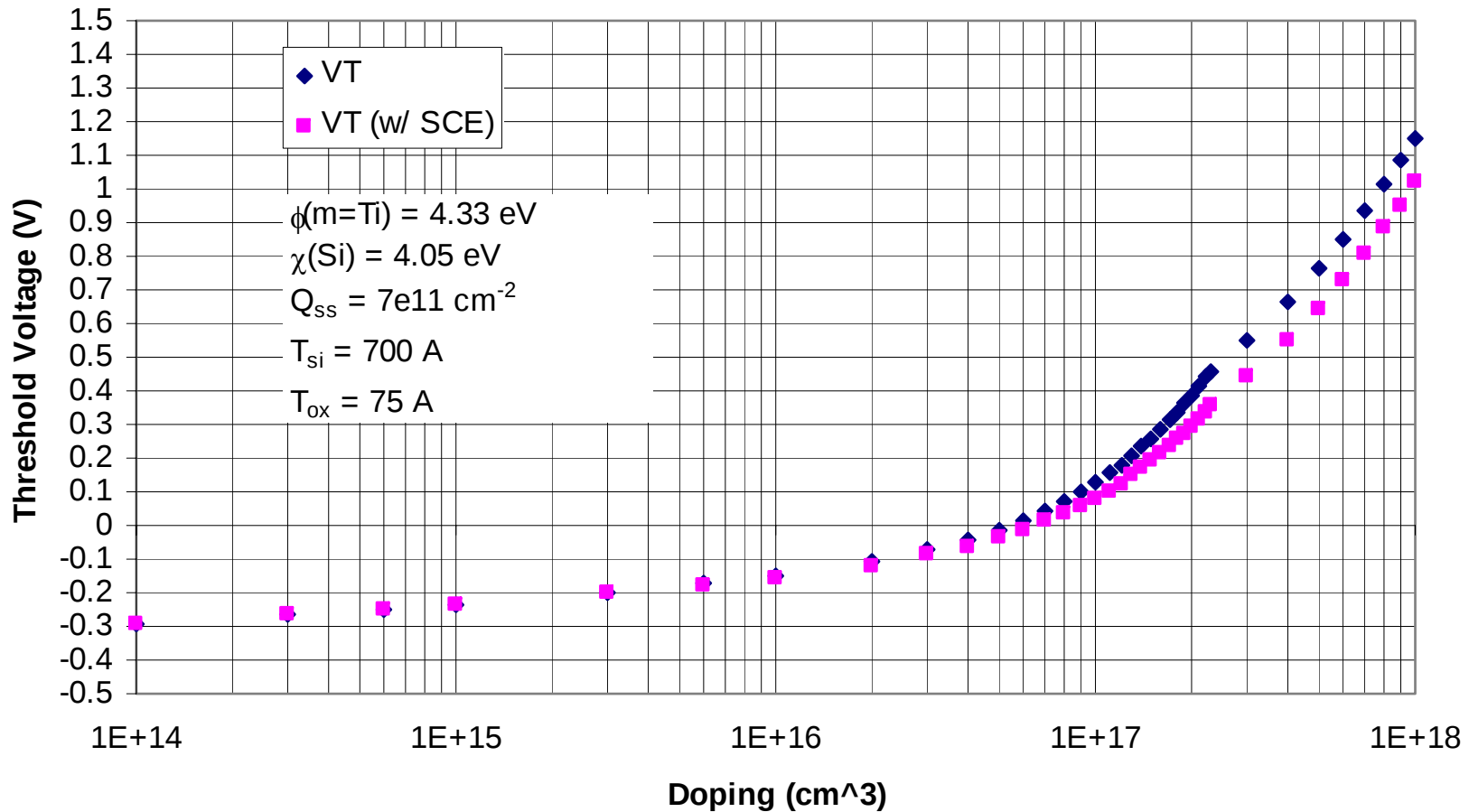
Activation of source/drain impurities via excimer laser annealing is necessary because the high temperatures used in conventional thermal annealing will melt the Al gate. The main disadvantage of laser annealing is the low throughput of wafers, which is an important consideration for manufacturability.

$\lambda = 308 \text{ nm}$ XeCl Excimer Laser



Threshold Voltage Calculation

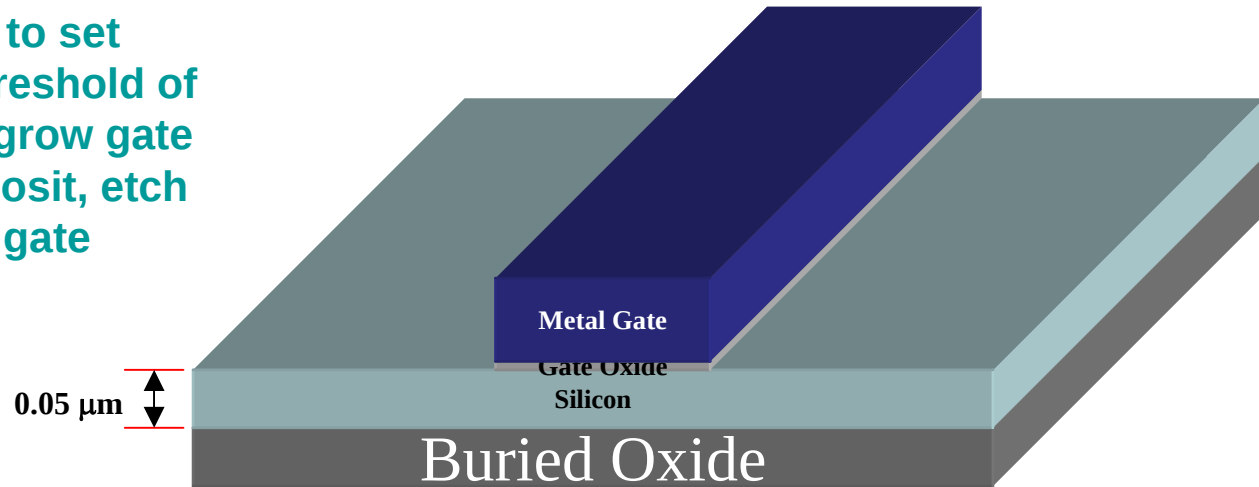
Threshold Voltage Calculations for nMOS with Short Channel Effects



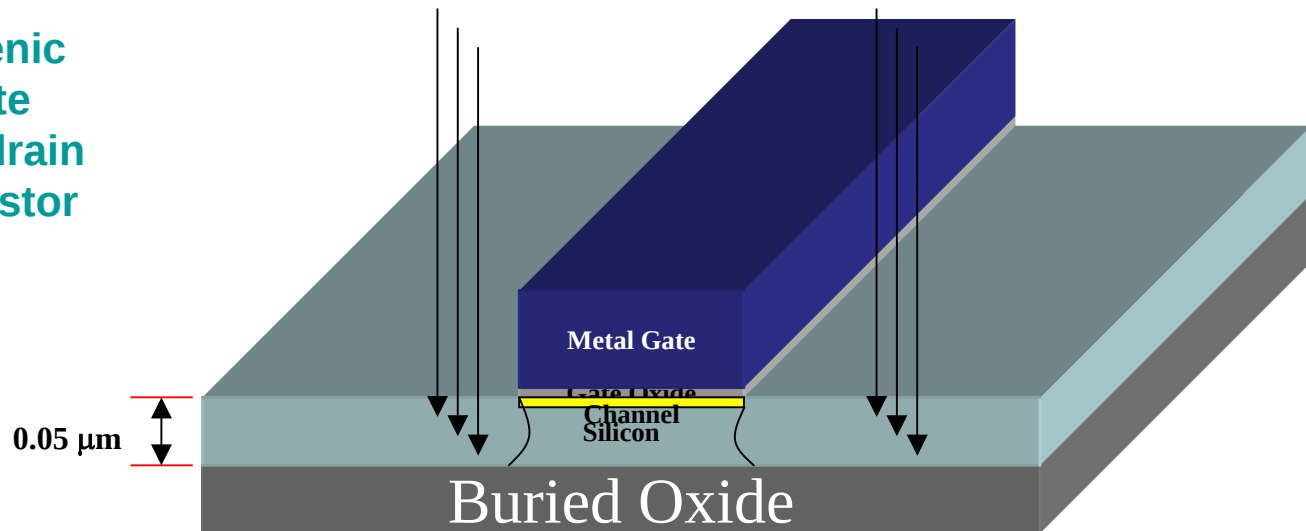
$$V_T = \Phi_{MS} - \frac{Q_{ss}}{C_{ox}} + 2\Phi_f + \frac{qN_a x_{dmax}}{C_{ox}}$$

MOSFET Fabrication Process

Implant Si to set
voltage threshold of
MOSFET, grow gate
oxide, deposit, etch
aluminum gate



Implant arsenic
ions to create
the source/drain
of the transistor





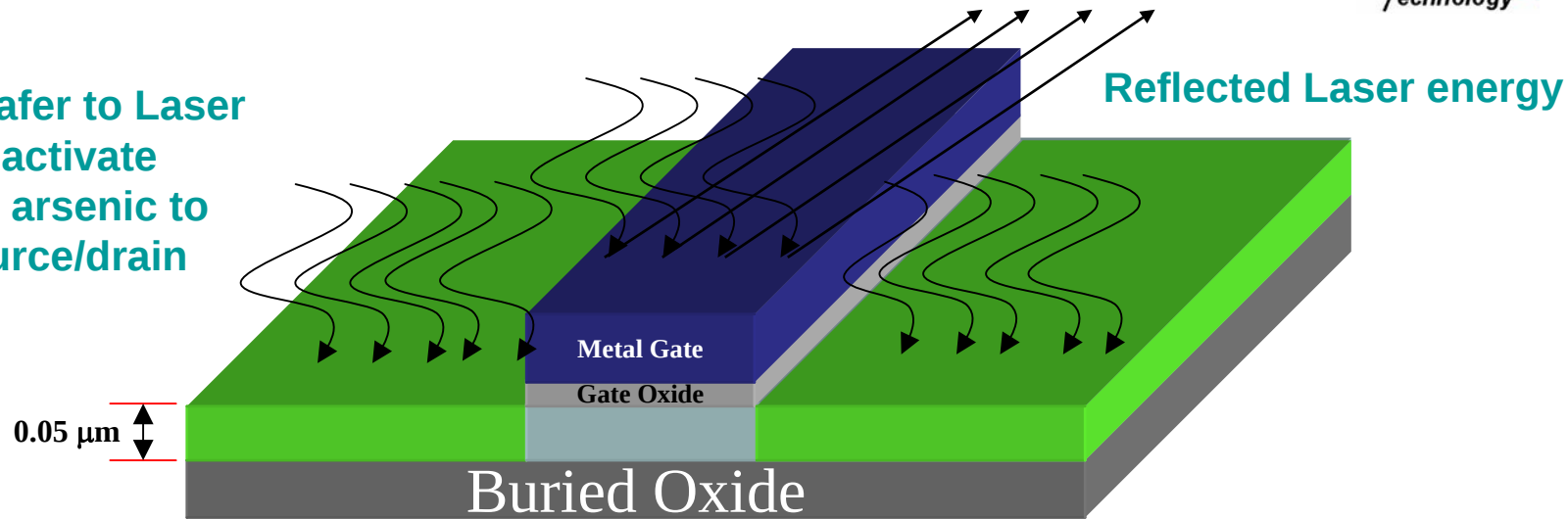
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Laser Annealing Process

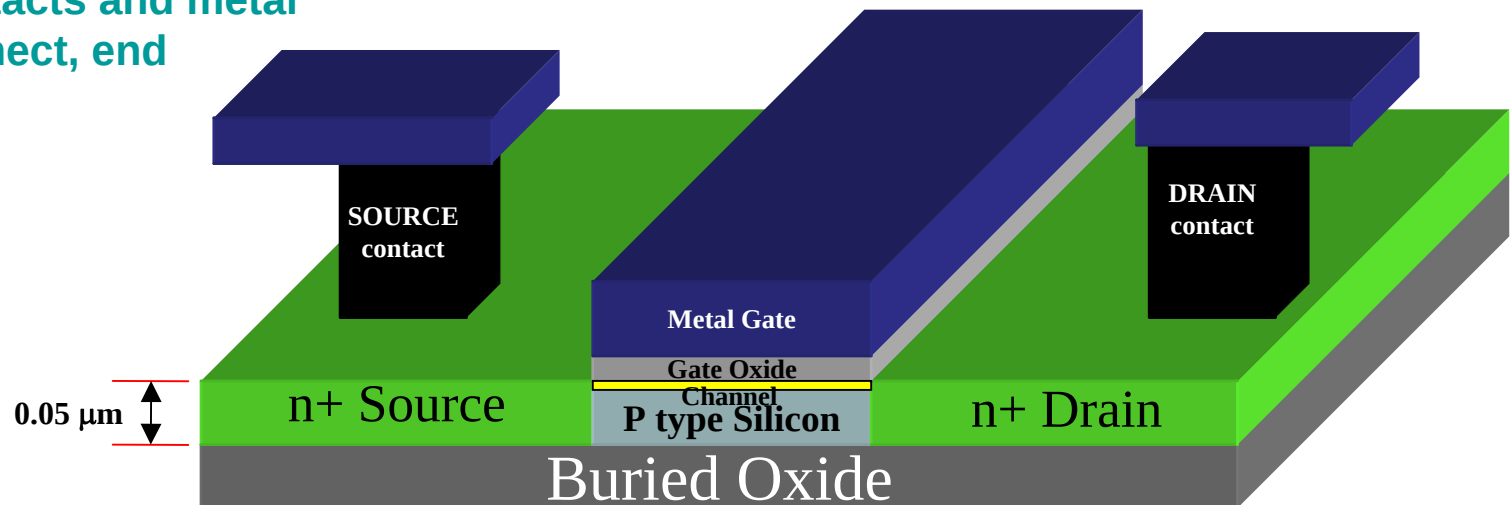
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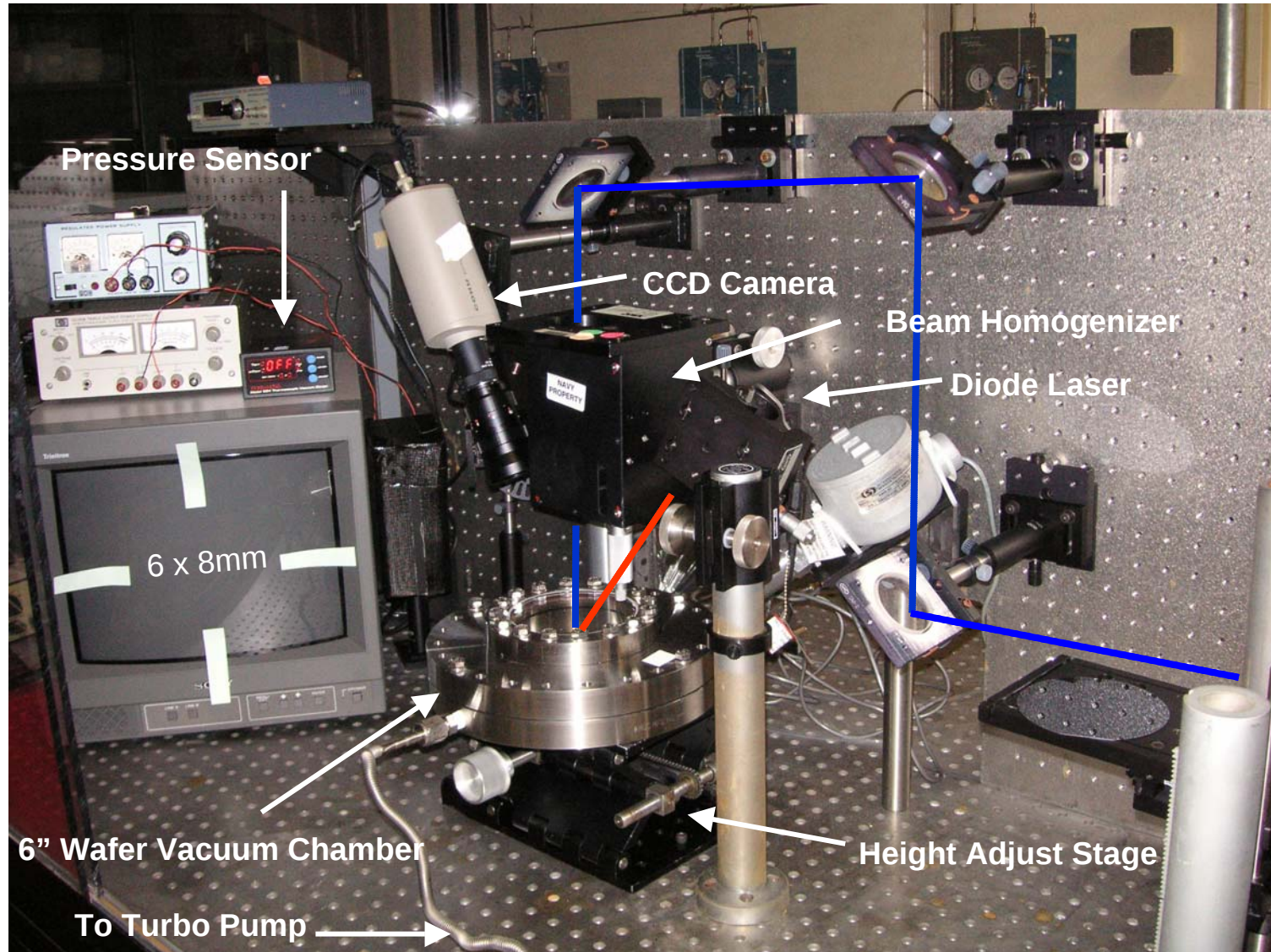
Expose wafer to Laser energy to activate implanted arsenic to define source/drain regions.



Deposit oxide, pattern, etch contacts and metal interconnect, end product.



Laser Annealing System





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Laser Parameters

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	SOI Wafers Characteristics	
Material	6-in SOI Wafer	Ion Implanted with As at a dose of $5 \times 10^{15}/\text{cm}^2$ @ 30 KeV SIMS Analysis Performed to determine carrier concentration
Orientation	<001>	
Si Thickness	700 Å	
SiO ₂ Thickness	on a 3800Å-layer of SiO ₂	
Laser	Excimer, 308 nm XeCl	
Pulse Energies	Up to 450 mJ	
Fluence	Ranged from 300 to 400 mJ/cm ²	
Pulse Rep. Rate	1 Hz, ~20 ns pulse length	
Pressure	200 mtorr (processing chamber)	



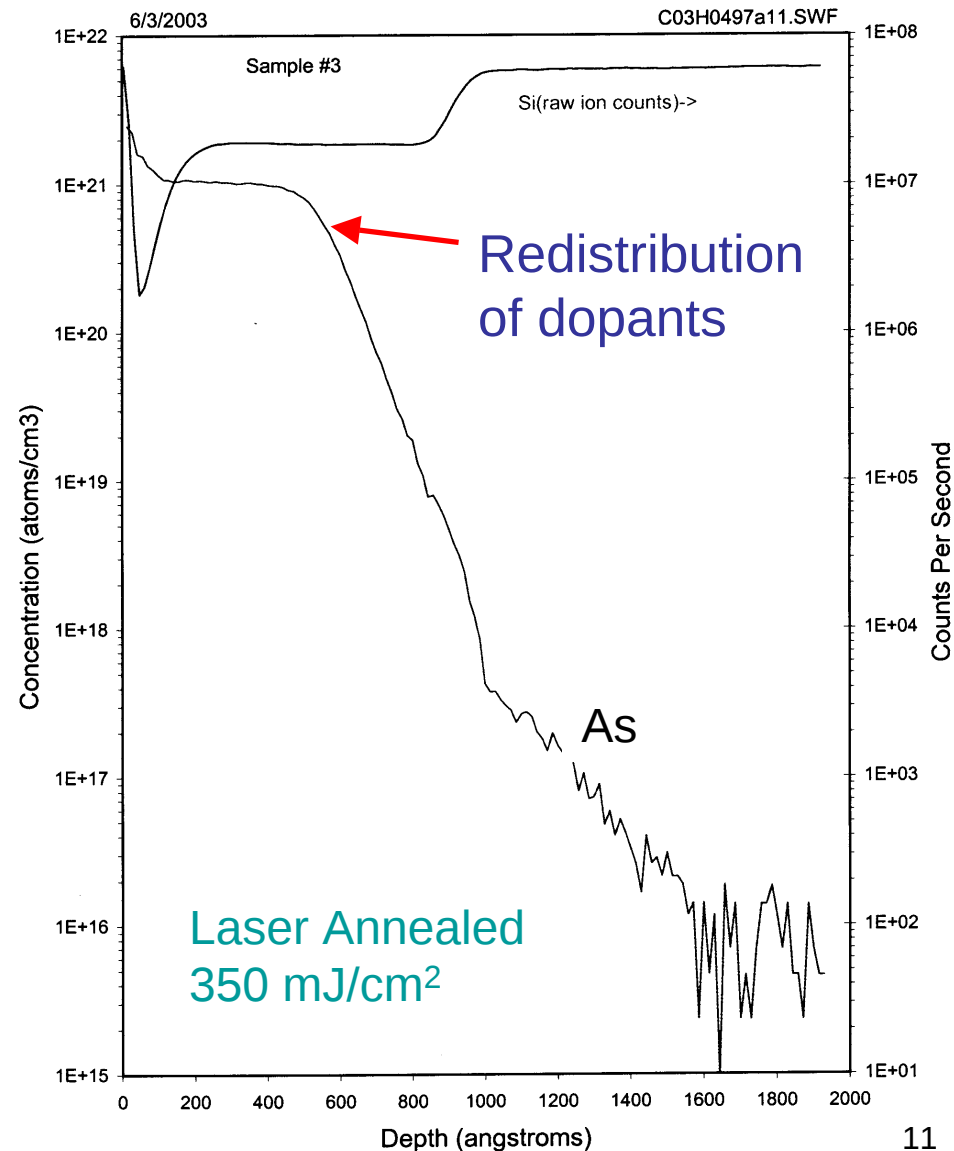
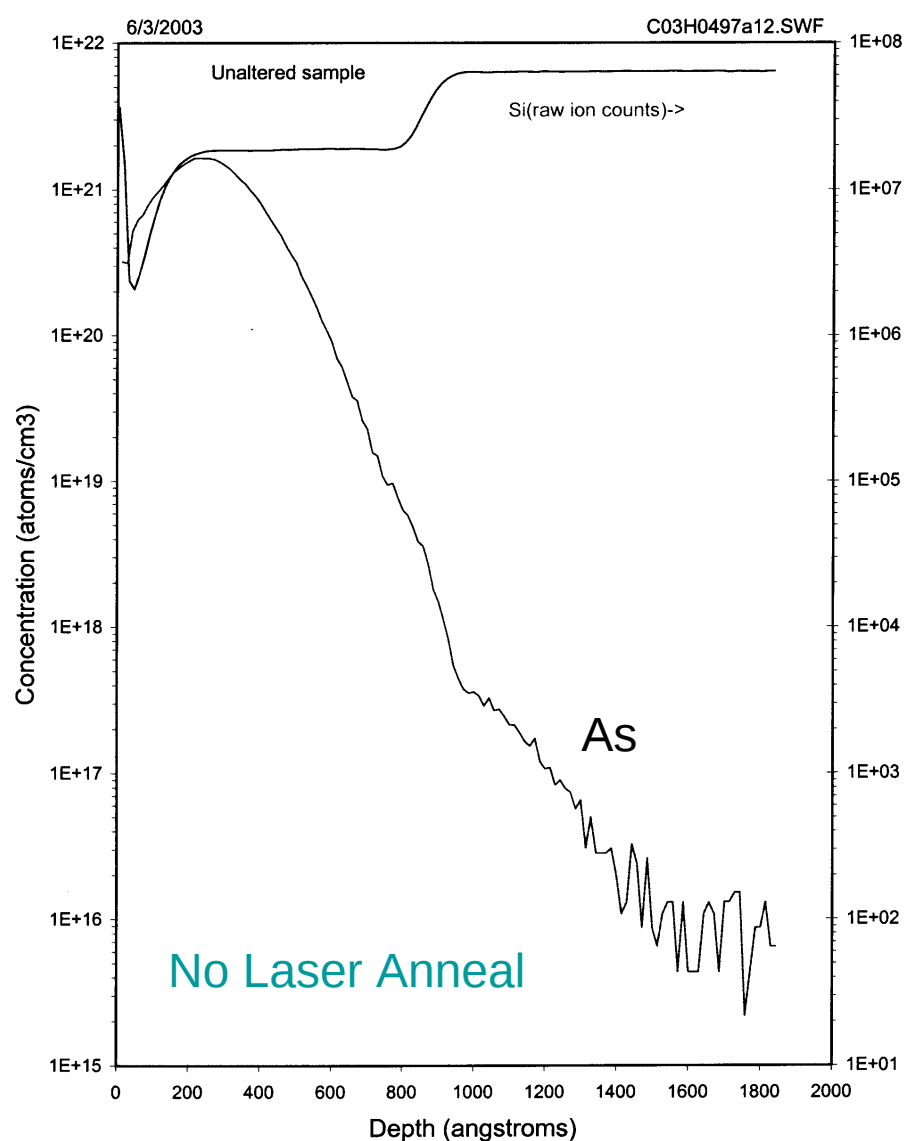


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SIMS Analysis

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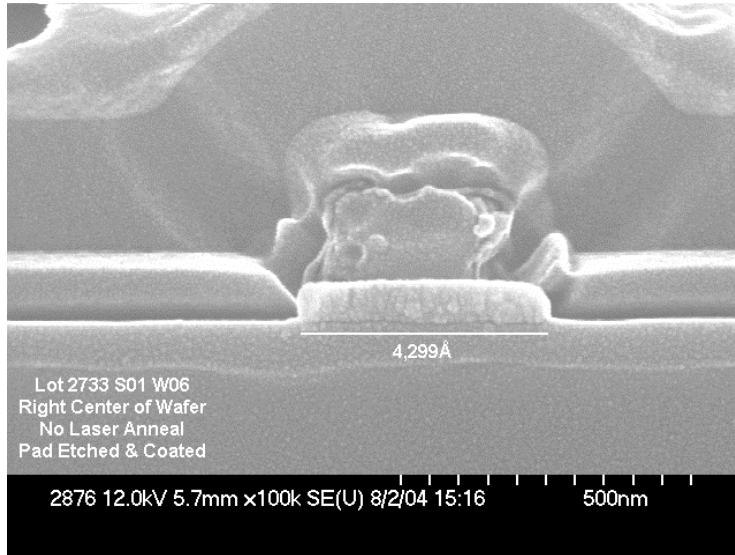


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SEM Images



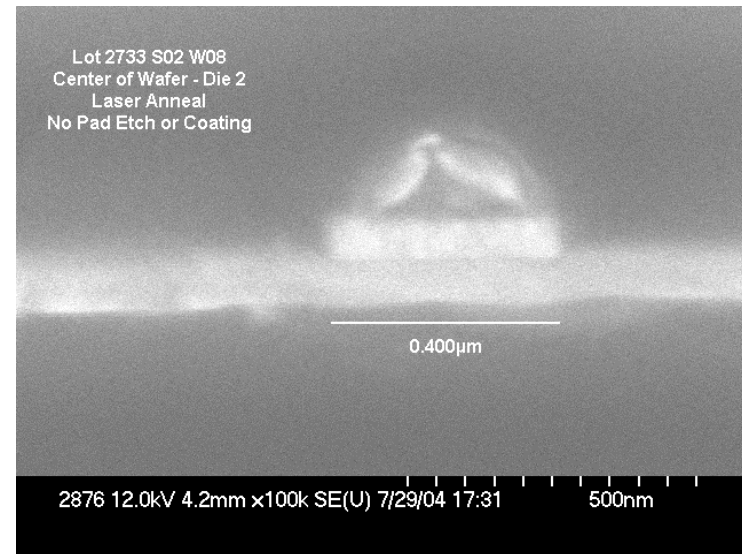
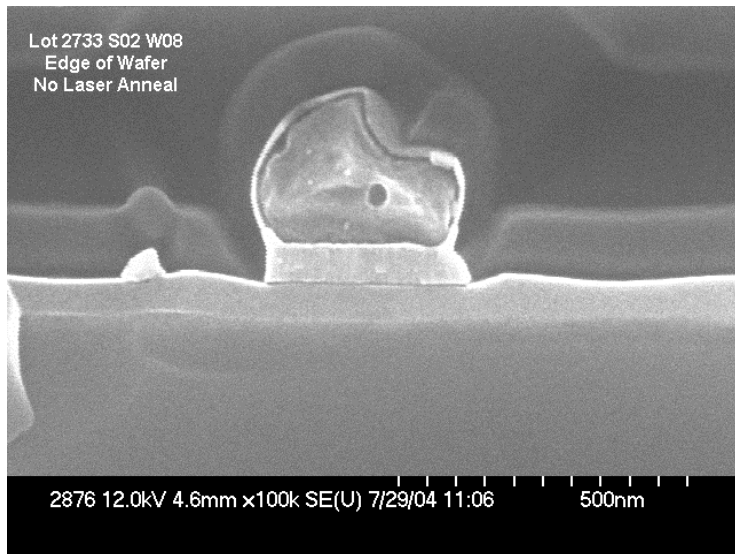
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0.25-micron drawn gate length.

0.40-micron actual gate length.

Lithography and PVD Gate metal etch process needs optimization.





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Summary of Device Transfer Characteristics

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Energy	Pulses	W (μm)	L(μm)	Vt (V)	SS (mV/dB)	Ion/Ioff	Comments
350	3	10	10	X	X		Shorted
		3	10	0.24	79.1	10 ⁶	
		3	0.8	X	X		
		10	0.25	0.19	101.7	10 ⁷	
		5	0.25	0.18	91.9	10 ^{6.5}	
		3	0.25	0.13	92.7	10 ^{6.5}	
350	5	10	10	0.24	85.2	10 ⁶	Shorted
		3	10	0.23	80.1	10 ⁶	
		3	0.8	0.17			
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.11			
375	3	10	10	0.21			Shorted
		3	10	0.19			
		3	0.8	0.19			
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.16			
375	5	10	10	0.22	78.4	10 ^{6.5}	
		3	10	0.22	79.4	10 ⁶	
		3	0.8	0.19	73.4	10 ⁷	
		10	0.25	X	X		
		5	0.25	0.19	95.2	10 ⁷	
		3	0.25	0.18	97.7	10 ^{6.5}	



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Summary of Device Transfer Characteristics

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Energy	Pulses	W (μm)	L(μm)	Vt (V)	SS (mV/dB)	Ion/Ioff	Comments
400	3	10	10	0.20	79.9	10 ^{6.5}	Shorted Shorted
		3	10	0.20	78.4	10 ⁶	
		3	0.8	0.18	71.7	10 ⁷	
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.16	111.1	10 ⁶	
400	5	10	10	0.18	81	10 ⁶	Shorted Shorted
		3	10	0.19	77.9	10 ⁶	
		3	0.8	0.20	87.2	10 ^{6.5}	
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.07	105.3	10 ^{6.5}	
450	3	10	10	0.18	77.6	10 ⁷	Shorted Shorted
		3	10	0.19	76.5	10 ⁶	
		3	0.8	0.25	74.4	10 ⁷	
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.19	104.5	10 ⁷	
450	5	10	10	0.21	77.4	10 ⁷	Shorted Shorted
		3	10	0.20	77.6	10 ⁶	
		3	0.8	0.18	70.7	10 ⁷	
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.16	103	10 ⁶	

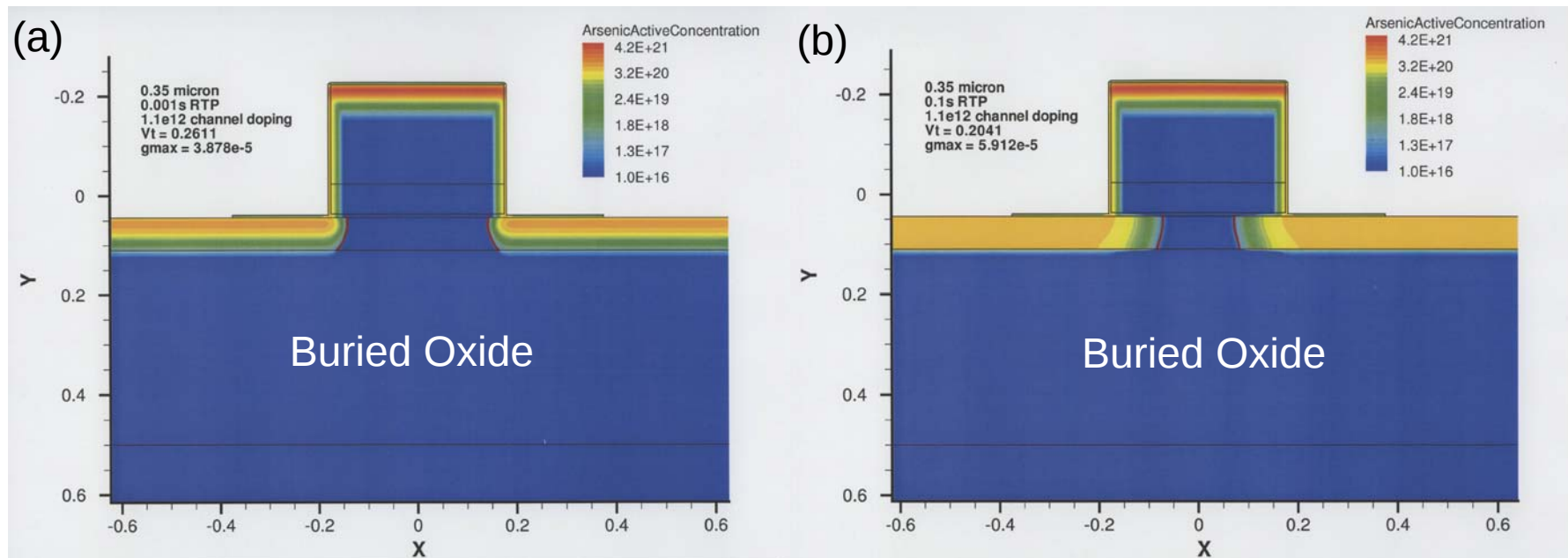


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Process Simulations

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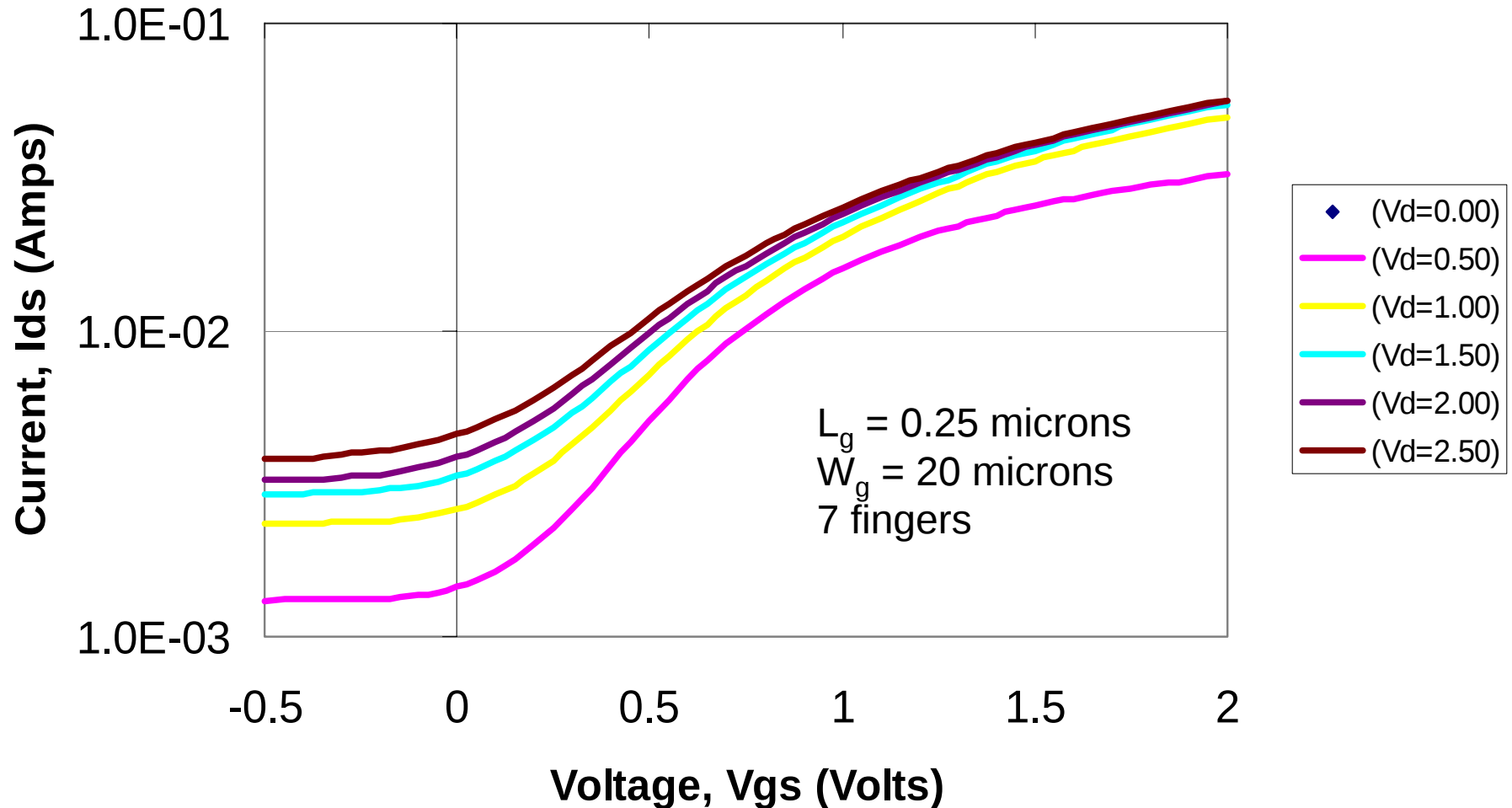
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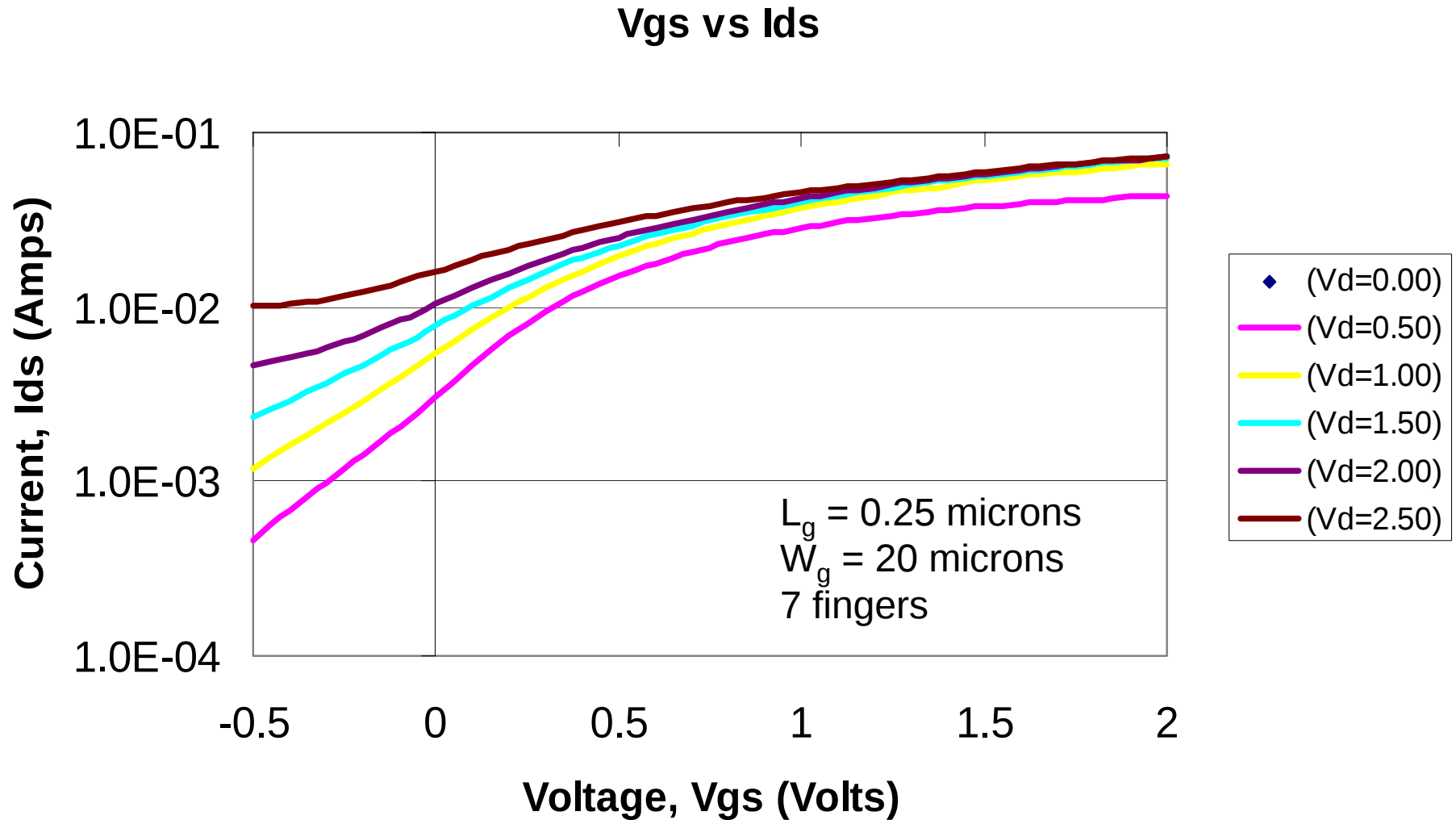
Previous studies found in the literature show junction temperatures reaching 1200 °C Kim et al., *IEEE Trans. Elec. Dev.*, 1748, 49 (2002).

Rapid Thermal Processing (RTP) simulation using integrated systems engineering (ISE) DIOS (a multidimensional process simulator for semiconductor devices) shows noticeable As dopant diffusion under the gate for a 0.1-sec RTP, which can explain shorting of submicron devices. However, laser pulse length are several magnitudes smaller (20 to 30 ns) where the source/drain profile is better represented by Figure (a).

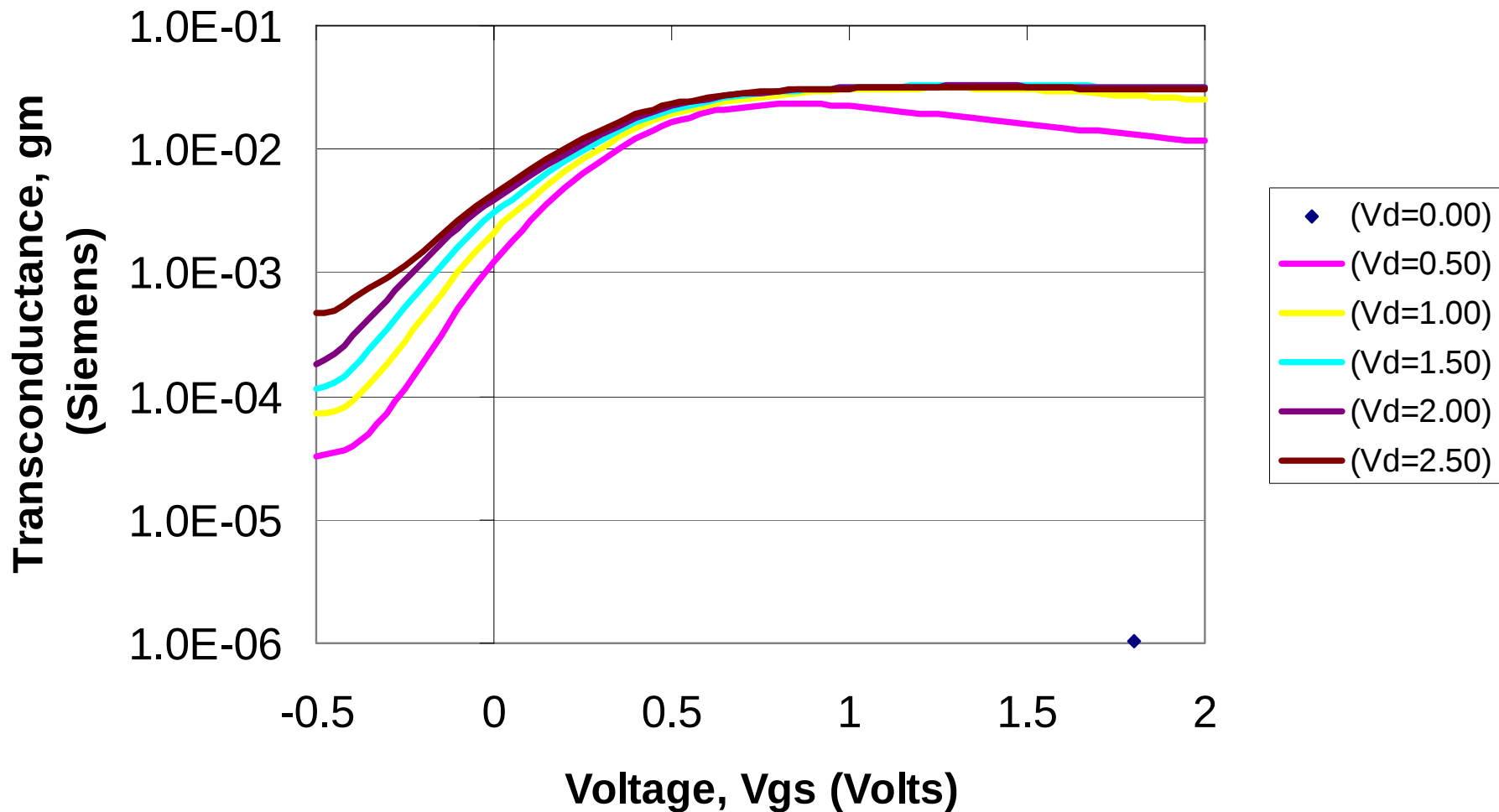
V_{gs} vs I_{ds}



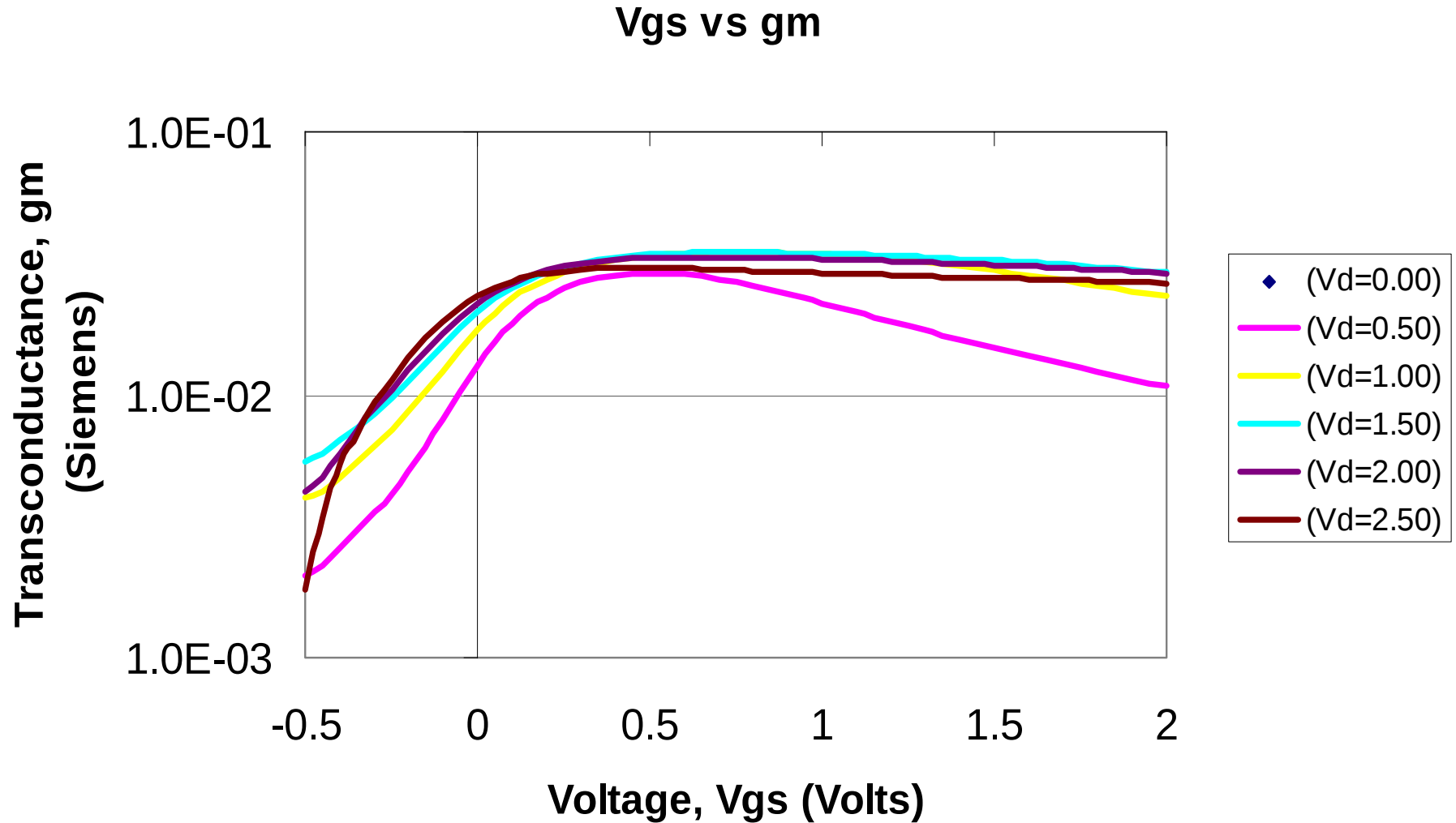
Polygate Device Transfer Characteristics



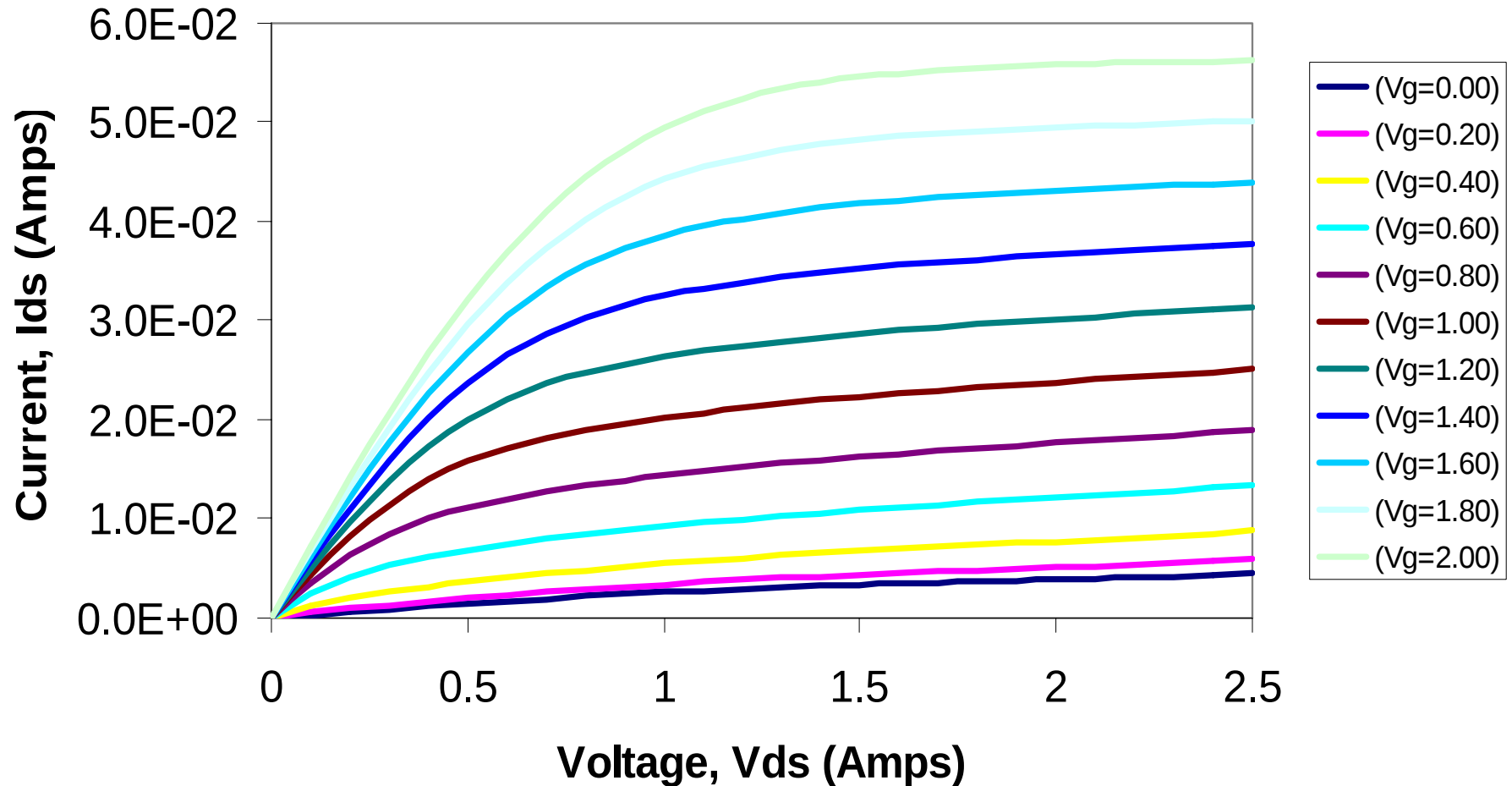
V_{gs} vs g_m



Polygate Device Transconductance

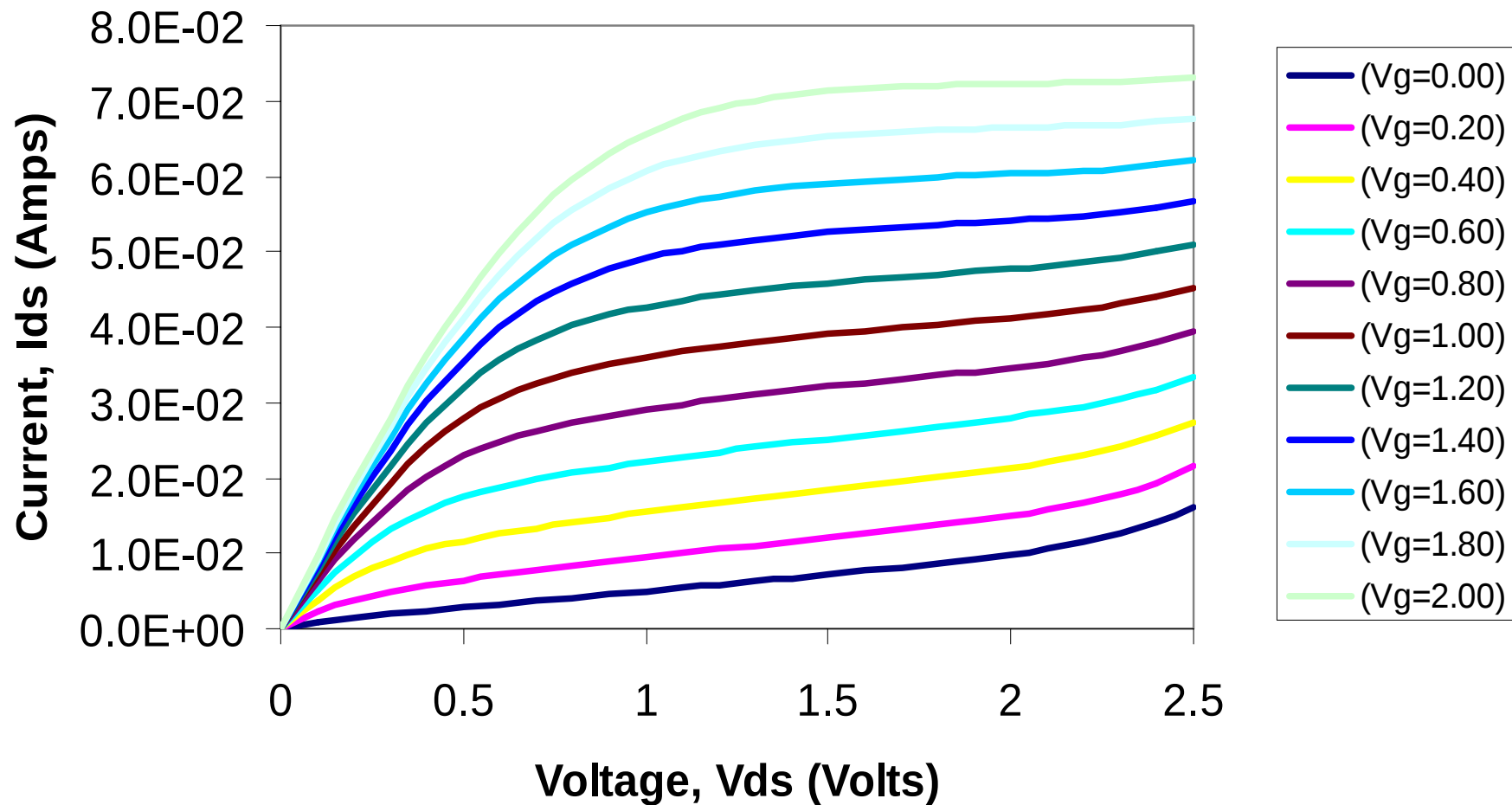


V_{ds} vs I_{ds}



Polygate Device Output Characteristics

Vds vs Ids



Unity Current Gain Frequency

$$f_t = \frac{g_m}{2\pi (C_{gs} + C_{gd} + C_{gb})}$$

Speed

Decrease $C'_s \longrightarrow$ Increase f_t

Unity Power Gain Frequency

$$f_{max} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + g_{ds} [R_g + R_s]}}$$

RF Gain

Decrease $R_g \longrightarrow$ Increase f_{max}

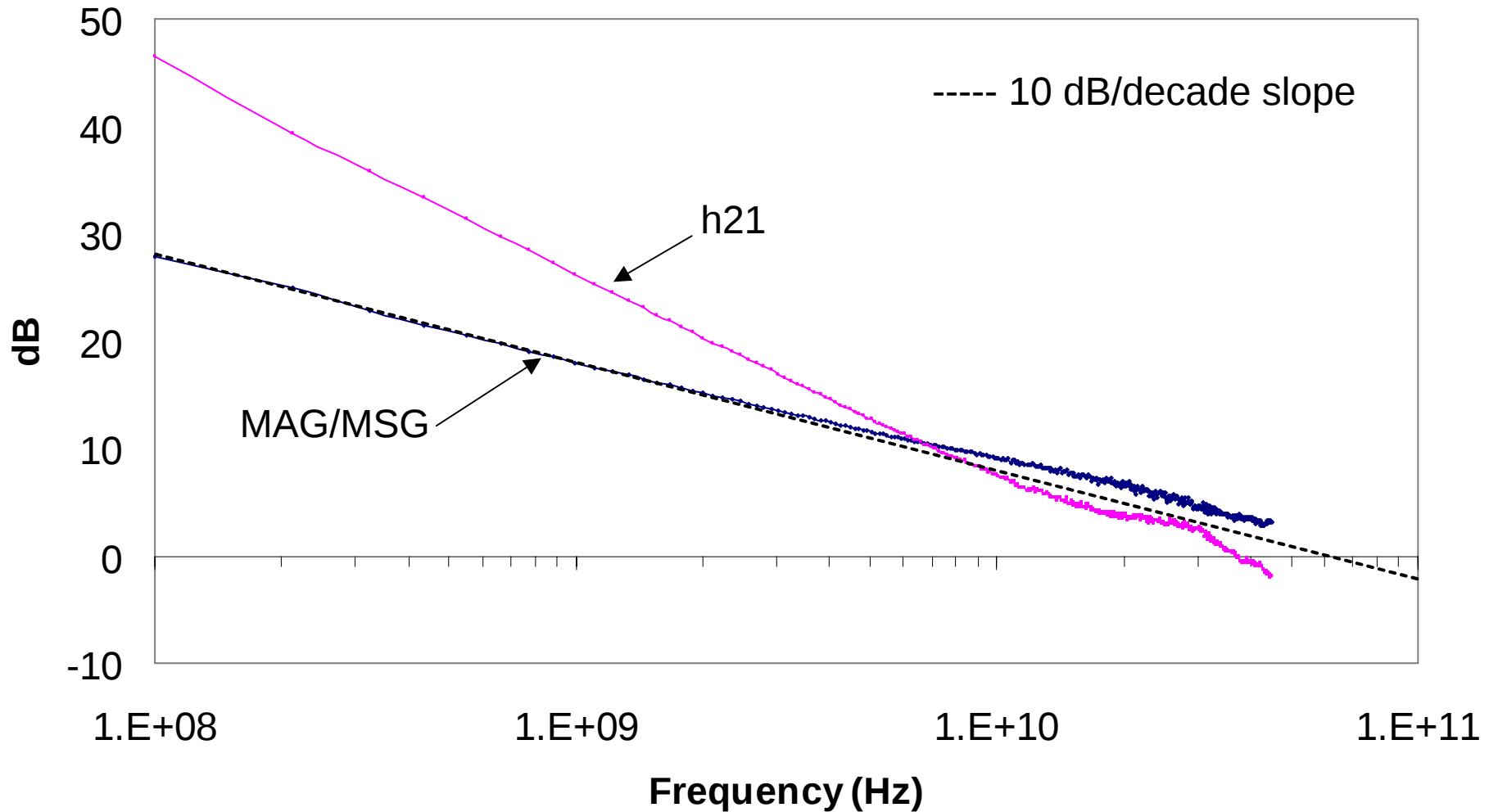
Minimum Noise

$$F_{min} = 1 + k \frac{f}{f_t} \sqrt{g_m [R_s + R_g]}$$

Microwave Noise

Decrease $R_g \longrightarrow$ Decrease F_{min}

RF Characterization of Metal-Gate Device



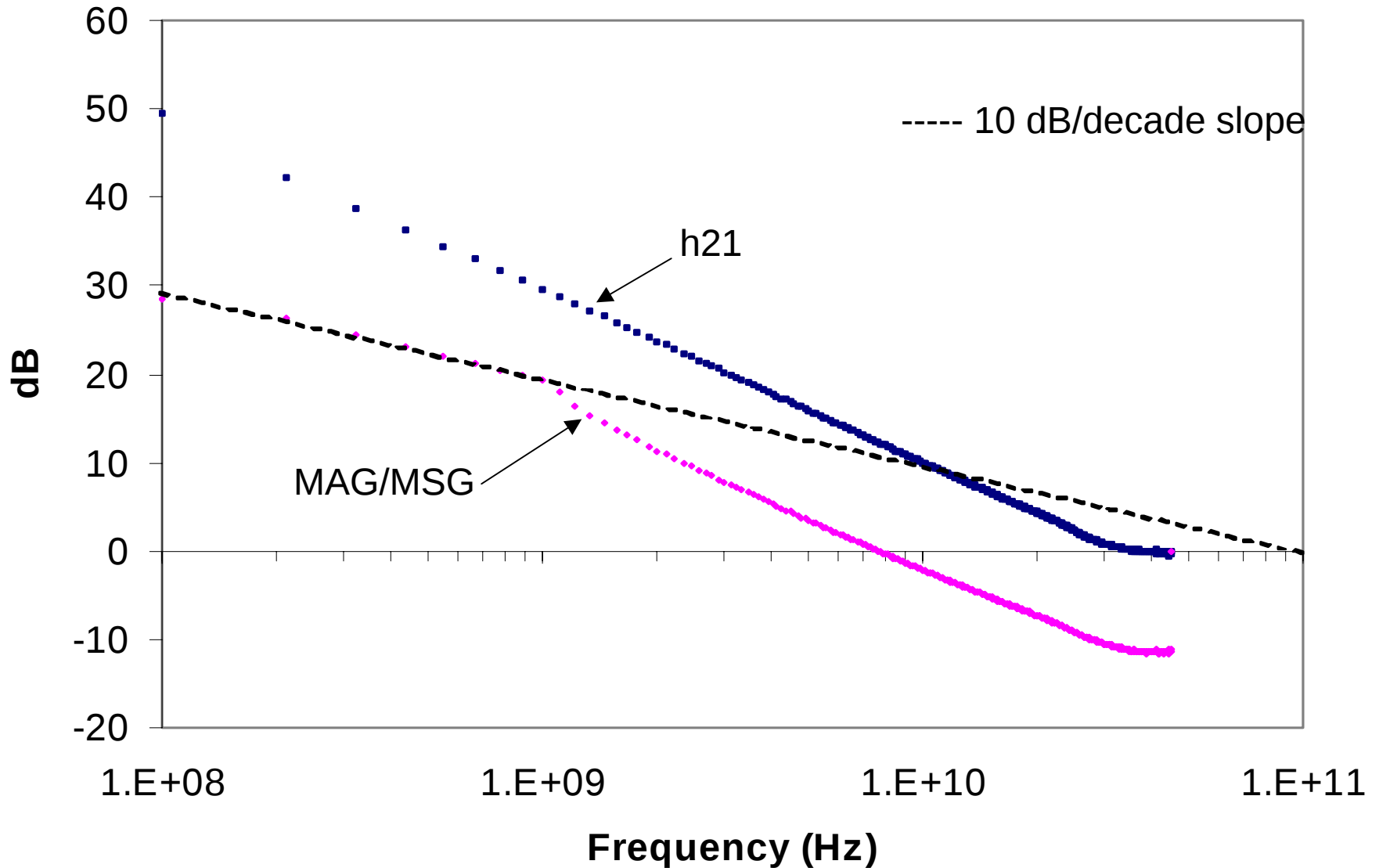


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RF Characterization of Polysilicon Gate Device



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Conclusions

1. Performed DC and RF characterization of laser annealed MOS SOI devices with Ti/TiN/Al gate.
2. DC device characteristics were found to be relatively independent of laser fluence.
3. Device shorting occurs for 0.25-micron drawn gate length devices.
4. ISE DIOS Process simulation indicates laser-induced Source/Drain shorting is not possible for 0.25-micron devices due to nanosecond laser pulses. Further studies need to be conducted to explain the low yield of submicron devices.
5. nMOS devices exhibit I_d values of over 50 mA, F_t values of over 25 GHz, and F_{max} values of 60 GHz.

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