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LOW VOLTAGE ELECTROLYTIC CAPACITOR PULSE FORMING INDUCTIVE NETWORK FOR ELECTRIC WEAPONS

by

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June 2006

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Electric weapons, such as the railgun, require a pulse power supply capable of providing reliable high-current, high-energy pulses of many megawatts. Pulsed alternators potentially have the same maintenance issues as other motor-generator sets, so a solid-state system would be desirable, but high voltage capacitor systems are not robust enough for the field. We propose here a Low Voltage Electrolytic Capacitor Pulse Forming Inductive Network (LVEC PFIN) which stores power in a relatively low voltage capacitor bank and provides weapon power pulses by first draining the capacitors into a power inductor and then interrupting the flow of current via a switch counterpulsing technique in order to achieve railgun-appropriate voltages. For this thesis, a 13 kJ LVEC PFIN was constructed, using solid-state semiconductor switches to redirect 25 kA of current into a 1 mΩ load, and the redirection of larger currents is clearly feasible. This technique may be a viable alternative once the energy densities and equivalent series resistances of low voltage capacitors and ultracapacitors reach the necessary levels.

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LOW VOLTAGE ELECTROLYTIC CAPACITOR PULSE FORMING INDUCTIVE NETWORK FOR ELECTRIC WEAPONS

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ABSTRACT

Electric weapons, such as the railgun, require a pulse power supply capable of providing reliable high-current, high-energy pulses of many megawatts. Pulsed alternators potentially have the same maintenance issues as other motor-generator sets, so a solid-state system would be desirable, but high voltage capacitor systems are not robust enough for the field. We propose here a Low Voltage Electrolytic Capacitor Pulse Forming Inductive Network (LVEC PFIN) which stores power in a relatively low voltage capacitor bank and provides weapon power pulses by first draining the capacitors into a power inductor and then interrupting the flow of current via a switch counterpulsing technique in order to achieve railgun-appropriate voltages. For this thesis, a 13 kJ LVEC PFIN was constructed, using solid-state semiconductor switches to redirect 25 kA of current into a 1 mΩ load, and the redirection of larger currents is clearly feasible. This technique may be a viable alternative once the energy densities and equivalent series resistances of low voltage capacitors and ultracapacitors reach the necessary levels.

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TABLE OF CONTENTS

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LIST OF FIGURES

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LIST OF TABLES

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I. BACKGROUND AND PROPOSAL

A. RAILGUNS AND ELECTRIC WEAPONS

For the last twenty years, the ability of surface ships to provide shore and land strike support has been seriously lacking. With the decommissioning of the battleships, the advent of precision strike missiles and bombs, and the focus on potential targets outside the 12 nautical mile range of the current generation of 5-inch guns, the utility of naval gunfire support has waned. The loss of this capability is a strategic vulnerability; thus, it has been a goal of researchers and force planners to find some way of revitalizing this critical mission area.

One of the most promising candidates for a new age of naval gunfire support is the railgun, an electrically powered weapon capable of launching a precision guided kinetic or explosive projectile a distance of 300 km at a high rate of fire, without the wasted space and vulnerability of powder charges or the massive expense of individual tactical cruise missiles. The railgun as a concept is over 100 years old [1], but the technological challenges imposed in fielding one have not yet been solved. Now, with advances in material science, energy storage, and power generation, as well as the recent focus on an all-electric ship, those challenges are being met. The naval railgun, the army railgun, coilguns, and other electric weapon systems such as Active Denial (the Army's less-than-lethal microwave crowd deterrent) and the Free Electron Laser are all on the horizon, and one need they share is for a reliable pulse power system capable of delivering megajoules of energy for shot after shot.

It has been the goal of the NPS Railgun group to explore innovative concepts in resolving the issues facing railguns as weapon systems, and in this thesis we seek to demonstrate and evaluate one particular alternative pulse power supply: the Low Voltage Electrolytic Capacitor Pulse Forming Inductive Network (LVEC PFIN).

B. COMMON PULSE POWER SUPPLIES

The two leading candidates for a railgun pulse power supply take vastly different approaches to achieving weapon-level voltages and currents. By weapon-level, it is implied that they are capable of firing a railgun projectile at a speed of around 2500

meters per second, far in excess of that achievable by an explosive propellant in a regular gun. The kinematics necessitate a muzzle energy of nearly 65 MJ, a breech energy of 250 MJ, and currents of 5 to 6 MA, all released in the span of 10 ms, for a power of more than 15 GW in a single pulse [2]. Though they arrive at the end state in different ways, the two pulse power supplies described below have either been proven through years of testing or are said to be on track to meet all their program objectives. However, they are not without their faults, and though the LVEC PFIN is not a proven technology, it shows great promise in resolving the outstanding issues and providing a third alternative for achieving weapon-level currents and voltages.

1. High Voltage Capacitor Pulse Forming Network

The most natural design for a railgun pulse power supply is to simply connect a bank of high voltage capacitors (on the order of 10's of kV) through a switching system directly to the railgun. By adding capacitors to the bank until the desired current and voltage level is reached, and then grouping banks together in a pulse forming network (PFN), successive triggering of banks will yield a nearly constant square current pulse capable of driving the railgun. The high voltage capacitor PFN is the basic pulse power supply used in every lab in the world and it was initially the intended supply for the proposed railgun weapon systems. However, high voltage capacitors have their disadvantages as well.

High voltage capacitor PFN's are very large and the capacitors themselves would be difficult to change out efficiently in an operational environment. Capacitors presently in use have a high power density, but a relatively low energy density, a limited lifetime at full voltage, and a relatively low number of discharge cycles in their lifetimes. Thus, while perfectly suitable for a laboratory environment in which they are charged and discharged rarely, they are less suitable for an operational military application where robust shelf and service lifetimes are necessities.

2. Compulsator (Rotating Flywheel) Pulse Forming Network

Compensated Pulsed Alternators, or Compulsators as they are called, are essentially large motor-generator sets capable of producing rapid high-power energy pulses for driving electric weapons and pulsed magnetic systems such as the Electromagnetic Aircraft Launching System (EMALS) with relatively low output

inductance. Also known as rotating flywheels, the energy for powering the railgun is stored mechanically as rotational kinetic energy rather than in the electric field of a capacitor. Mounted in counter-rotating pairs in order to offset the inertial effects of angular momentum, the compulsators planned for the Army railgun project carry enough energy for several successive shots at ≥ 10 MJ muzzle energy each without recharging [1]. Physically smaller than the high voltage capacitor systems, compulsators are based upon proven rotating machine technologies already in wide use aboard naval combatants. However, though they show great promise, there are some technical hurdles that have to be overcome. As with all rotating machines, there are increased maintenance concerns in terms of bearings, lubrication, cooling, vibration, and shock, which would be non-existent or mitigated in a solid-state system. Also, the compulsators being planned for the Army are already pushing the boundaries of material science with rotational tip speeds approaching the speed of sound and millimeter clearances between the rotor and stator, yet cannot provide the power levels required for Naval railgun applications by at least an order of magnitude.

C. THE PULSE FORMING INDUCTIVE NETWORK

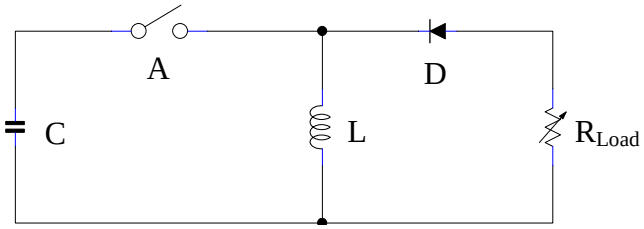

Figure 1. Simplified PFIN Schematic

The Pulse Forming Inductive Network (PFIN) (shown above in Figure 1) differs from usual PFN's in that energy is stored at a relatively low voltage (less than 1000 V) and is discharged via a power inductor which provides power appropriate for the weapon [2]. High voltage capacitor PFN's contain inductors as well as capacitors, but these inductors are used to either stretch out the current pulse or attenuate switching transients via saturable reactors. Instead, in the PFIN, the low voltage capacitor is allowed to discharge to zero, resulting in a high current state in the power inductor. At that point, the switch between the capacitor and the inductor is forced open, interrupting the flow of current and causing the inductor's voltage to reverse and increase in an attempt to

maintain current flow. The only remaining current path is in a diode-protected loop, which couples the high voltage and high current of the power inductor to the railgun load. This process will be explained in greater detail in section II.

The PFIN is not the first time an inductive pulse power supply has been proposed. Inductive supplies have long been desirable, but they have been hard to implement because of the difficulties inherent in interrupting the flow of current through the main switch. Previous inductive supplies, including the homopolar generator/inductor system used by the Center for Electromechanics (CEM) for their 90 mm railgun, interrupted the flow of current via heavy mechanical switches or explosively opened switches [3]. Pokryvailo developed a true PFIN, but his system for an electro-thermal gun was battery driven rather than capacitor-based and utilized either explosive opening switches or counterpulsed semiconductor switches[4], [5]. The use of explosively opened switches introduces needless dangers and maintenance issues and obviates their use aboard ship.

Our particular basic PFIN design to drive railguns was first conceptualized by Professor Bill Maier [2], and later refined by CDR Jerry Stokes [6] and ENS Michael Graham [7]. The current thesis is the third written concerning that basic schematic. Our design takes the counterpulsing technique proven in Graham's thesis and develops a medium power supply capable of firing one of the school's laboratory railguns. Built from low voltage electrolytic capacitors (LVEC's) and integrated gate commutated thyristors (IGCT's), this supply has many potential advantages over other supplies. The LVEC's have low energy densities, similar to that of high voltage capacitors, but with much longer lifetimes at full voltage, and they are capable of hundreds of thousands of discharges without failure. Their smaller size and longer service lives immediately make them more desirable to maintain than bulky high voltage capacitors. The system is also completely solid-state, with no moving parts, so maintenance and cooling issues become much easier to solve. And should the design prove viable, it could then be applied to other storage media, such as ultracapacitors whose energy densities are orders of magnitude better than LVEC's, and whose equivalent series resistances are rapidly improving. These properties would allow for much smaller, more efficient, and more reliable pulse power supplies and would be a notable improvement on the long road to fielding electric weapons.

II. RAILGUN AND PFIN THEORY

A. BASIC RAILGUN THEORY

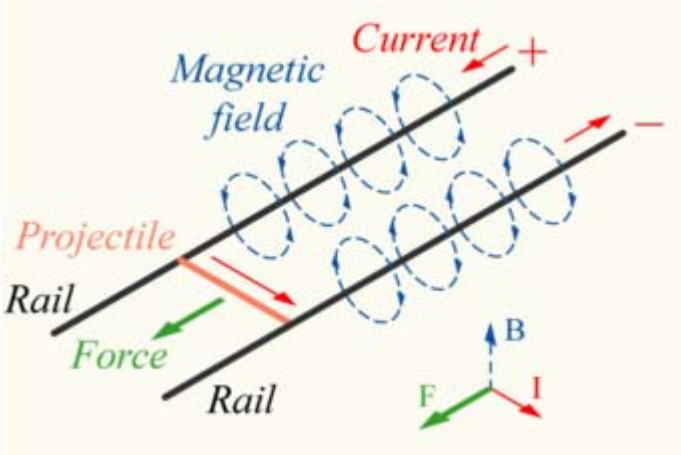

Figure 2. Basic Railgun Theory

Unlike regular guns, which propel rounds through the constrained expansion of gases from explosive propellant charges and are thus inherently limited in speed by the gas's speed of sound, railguns propel rounds via the interaction of high currents and magnetic fields. In a railgun, Figure 2, two parallel flat rails are constrained with respect to one another with insulating materials on the outside and a uniform gap between them. A sliding electrical contact (armature) is placed between, allowing a path for current flow. High voltage is applied to the rails, causing a large current to develop within the rails and through the sliding armature. The Lorentz force, given below, governs this interaction and there is no inherent limitation in the speeds and kinetic energies that can be obtained.

$$\vec{F} = \int I d\vec{l} \times \vec{B}$$

F is the force on the armature, *I* is the current, *dl* is the path length, and *B* is the strength of the magnetic field. In a railgun, the equation can be expressed in terms of current and the induction gradient, *L'*, leaving the following solution:

$$F = \tfrac{1}{2} L' I^2 = m\, dv/dt$$

Here, *m* is the mass of the rail and *dv/dt* is the acceleration down the rails [2].

Railguns are complex enough in their own right, and many papers have been written on their specific function. From the standpoint of the pulse power supply, however, it is important only to note their properties as an electrical load. In that sense, the rails represent a variable resistance and variable inductance, both of which increase from almost a dead short when the round is fired to an open and extinguishing plasma as the accelerated sliding block armature breaks contact with the rails. It should also be noted that the acceleration of the railgun round is due to the current applied, not the voltage. In order for a high voltage capacitor PFN to provide a constant current as desired, the voltage pulse from every bank in the PFN must each be greater than the last. In the PFIN, the current is constant for each bank pulse, while the power inductor provides whatever voltage is necessary to maintain current flow. Thus, the PFIN is potentially a more elegant solution to the whole railgun power problem than either the high voltage capacitor PFN or the compulsator system.

B. PFIN THEORY

As stated before, the Pulse Forming Inductive Network produces weapon-level current and voltage pulses from low voltage capacitive storage by means of an inductive boost. The voltage boost is essentially the same as "inductive kick", the arc produced by any circuit with a high inductance (such as an electric motor) when power is suddenly removed. In an effort to maintain the steady flow of current through a coil, the collapse of the coil's magnetic field produces a voltage opposite in polarity to that of the original circuit, changing it from a load to a source, in accordance with Lenz's Law. The instantaneous rise in voltage magnitude is determined by the rate of current change, given by the equation:

$$V = L\, dI/dt$$

In practical terms, the voltage depends only upon the dielectric strength of whatever was used to interrupt the flow of current, or in the case of the PFIN, upon the impedance of the railgun load. The resulting high voltage current decays exponentially as the magnetic field collapses. The amount of time it takes to decay depends upon the energy initially stored by the field and the rate of dissipation by the resistance of the load. At start up, the railgun is essentially a short circuit, a low impedance contact between the

metal rails and the stationary metal armature, and the first PFIN pulse would last for a relatively long time. As the armature moves down the rails, the length of the circuit and its associated impedance increases, therefore subsequent PFIN pulses would decay more quickly. As the armature nears the end of the rails, the resistance often becomes quite large as solid metal contact is lost and the round "transitions" or wears down so much that only a plasma contact is maintained for current flow, resulting in greater voltage drop.

In addition, it has been noted in the study of railguns that the power draw of the weapon is proportional to the product of armature force and armature velocity [2]. Therefore, as velocity increases, input power must increase to maintain a constant force on the round. Since force is proportional to the square of current, a constant current implies an ever increasing power draw. Therefore, because of the greater dissipative losses, the greater percentage of energy lost in building the magnetic field of the rails, and the velocity-dependent nature of power draw, both PFN's and PFIN's must supply more and more power as the round moves down the weapon, either by increasing the energy capacity of individual modules or firing the modules more rapidly.

1. PFIN Operational Sequence

To understand the operation of the PFIN, it is necessary to look at the circuit in stages. In Figure 3, the simplified PFIN schematic is shown in its initial condition: the capacitor bank is charged, the switch group is open, and current through the power inductor and the load are zero.

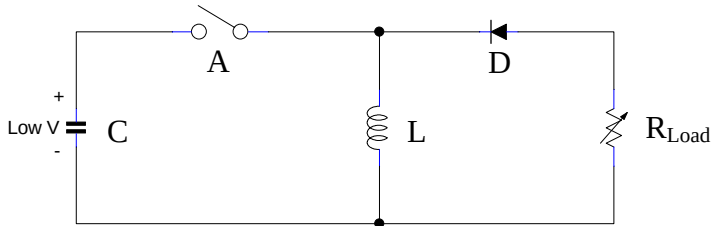

Figure 3. PFIN Initial Condition, Time t_0

At time t_0, the switch, A, is closed, and the full voltage of the capacitor bank C is placed across the inductor L (neglecting the voltage drop across the switch and the losses within wiring and components). Current begins to flow in the left half of the circuit, rising at a rate given by the resonance between the total capacitance and total inductance of the circuit. This same capacitor voltage reverse biases the diode D in the right half of

the circuit, so no current flows through the load R. At time t_1, shown in Figure 4, the current through the inductor L is at its peak and voltage on the capacitor bank C is low, but not zero.

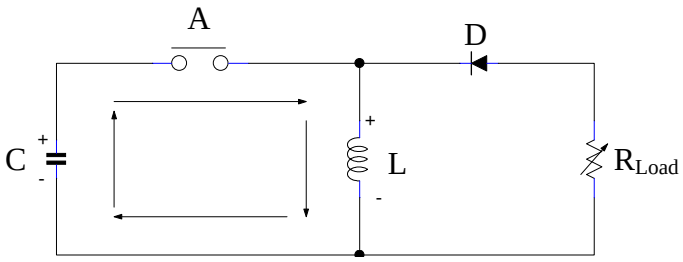

Figure 4. PFIN at Time t_1

At time t_2, the charge on the capacitor bank is zero and almost all of the energy originally stored in the electric field of the capacitors is now stored within the magnetic field of the inductor. The current has fallen slightly from its peak value, but it is still quite high. At this point, the switch A is opened and the current between the capacitor bank and the power inductor is interrupted. The voltage on the inductor L reverses and increases in order to maintain the flow of current through itself. The voltage would increase to the point of causing a dielectric breakdown between the poles of the switch, but long before that, the diode D in the load section becomes forward biased and conducts, allowing an alternate path for current flow through the inductor (Figure 5).

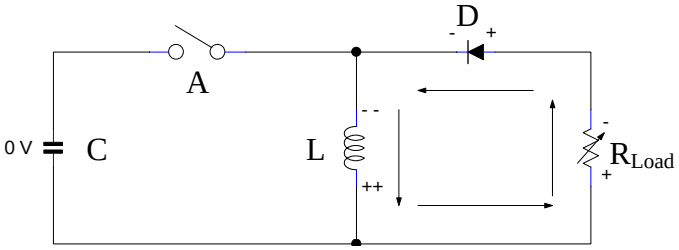

Figure 5. PFIN after Time t_2

Figure 6 shows a P-SPICE simulation of the PFIN, showing capacitor voltage V_C, switch current I_S, inductor current I_L, load current I_R, and inductor voltage V_L from time t_0, through t_1 and t_2, and to current dissipation.

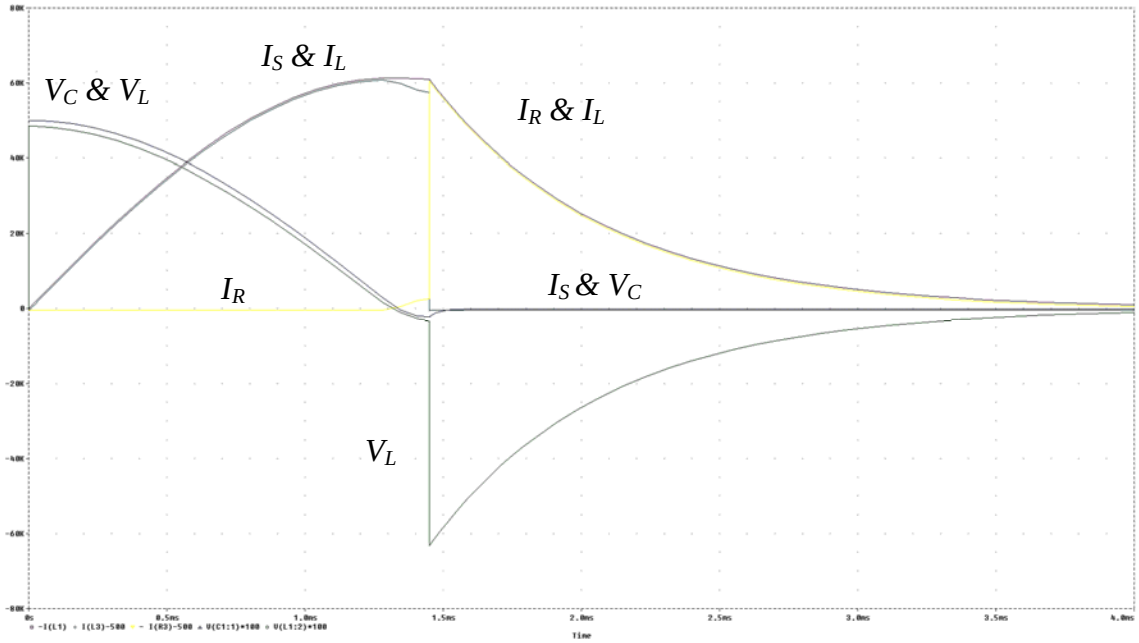

Figure 6. PFIN P-SPICE Simulation

2. Counterpulsing

Most of the energy in the circuit is delivered to the load, with only the losses due to circuit resistances and switch resistances affecting efficiency. The pulse or physical arc can be minimized by keeping the inductance in the rest of the circuit as low as possible. Even then, the current running through the capacitor bank and the switch group will tend to persist, causing a brief voltage pulse capable of physically damaging the switch, e.g. punching the solid state switch. For this reason, past inductive pulse power supplies have tended to use large mechanical switches or explosively opened switches, neither of which is desirable in an operational environment. Solid-state switches for the most part break down physically under the high voltages inherent in such a function. This high voltage pulse has been the major stumbling block to the use of a PFIN, but there are ways of reducing the voltage and current through the switch so that any tendency to arc is minimized or eliminated entirely.

One such technique is the counterpulse [4], [7]. As an alternative to a mechanical switch, counterpulsing enables the use of semiconductor devices by shunting away the high currents from the main switch for a brief moment, allowing the solid-state switch to shut off at a current and voltage well within its rated capabilities. This effect is accomplished (as shown in Figure 7) by placing a second semiconductor switch B and a

capacitor C2 in parallel to the main switch A. The counterpulse capacitor C2 probably should be selected to have a much smaller capacitance, but a much higher voltage rating than the main capacitor bank.

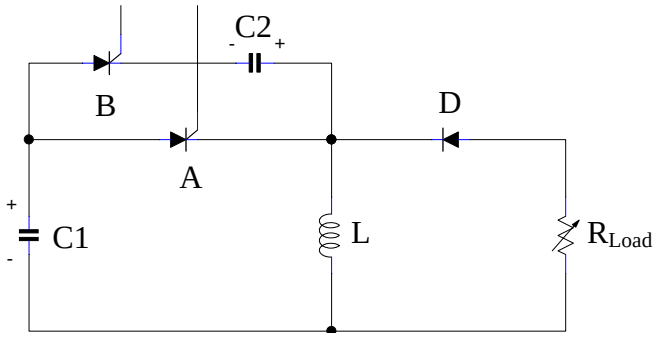

Figure 7. PFIN with Counterpulse Switching

When the main switch A is closed or turned on, current develops and capacitor voltage V_{C1} falls off as in the previous examples. At time t_2, however, rather than open or turn off the main switch, the counterpulse switch B (in Figure 7) is closed / turned on, placing the counterpulse capacitor C2 in parallel with the main switch. The charge on the counterpulse capacitor is configured such that the cathode of the main switch is placed at a higher potential than the anode, reverse biasing it for a moment and driving its current to either zero or a low value, depending upon the relative amount of charge. The current through the switch group is then diverted from the main switch A into the counterpulse switch B and the counterpulse capacitor C2, which then feeds the power inductor L so there is no interruption in current flow felt there. Once main switch current I_S falls near zero, it may be opened or turned off safely, without developing a reactive voltage spike. Once the charge on the counterpulse capacitor falls to zero, it is at the same potential as the main capacitor bank and there is no longer any potential difference to drive current flow. This process is transparent to the power inductor, which only sees the opening of the switch group and reacts as previously described.

The previous thesis, which proved the counterpulse concept when applied to a small PFIN, used thyristors as the main and counterpulse switches. The results were very timing dependent since the main thyristor would continue to conduct unless it was reverse biased long enough for all the charge carriers to drift out of the semiconductor junction [7]. The recommendation from that experiment was to utilize a different type of

switch which had an adequate turn-off capability so the current would only need to be decreased to some level vice turned off completely. In this thesis, the thyristors were replaced by Integrated Gate Commutated Thyristors (IGCT's), semiconductor opening switches which could each turn off 4000 amps, four times the current reached in the initial experiment [8]. With appropriate counterpulsing, this turn-off capability could be increased by an order of magnitude and would allow semiconductor switches to control weapon-level currents and voltages.

3. PFIN Equation Derivation

The theory behind the PFIN is essential to the design and operation of the LVEC PFIN. The schematic shown in Figure 7 shows the basic parts of the device, but neglects the true complexity found in any ordinary electrical circuit. The capacitor bank, switch group, power inductor, and load each have certain amounts of resistance, capacitance, and inductance, and each of these will affect the PFIN and alter its performance from the ideal. The components' resistance and inductance especially can negatively affect the efficiency of the circuit.

To begin, a differential equation is formulated from Kirchhoff's Voltage Law which takes into account the total capacitance, *C*, inductance, *L*, and resistance, *R*, of all the components combined.

$$V_C + V_R + V_L = \frac{q}{C} + RI + LI' = 0 = \frac{q}{LC} + \frac{Rq'}{L} + q''$$

V_C is essentially the voltage on the main capacitor bank C1, V_R is the voltage drop across all resistances in the left half of the PFIN, and V_L is the total voltage drop across the power inductor L and the inherent circuit inductance. When this differential equation for a classic LRC circuit is solved, one finds that maximum current occurs at time t_1 and zero capacitor charge occurs at time t_2 as follows [2]:

$$t_1 = \left(1/\omega\right) Arc\tan\left(\frac{2\omega L}{R}\right) = \left(1/\omega\right) Arc\cos\sqrt{\eta}$$

$$I_{L_{\max}}(t_1) = V_{C_o}\sqrt{\frac{C}{L}}e^{-\sqrt{\frac{\eta}{1-\eta}}Arc\cos\sqrt{\eta}}$$

$$t_2 = \left(1/\omega\right) Arc\tan\left(-\frac{2\omega L}{R}\right) = \left(1/\omega\right) Arc\cos(-\sqrt{\eta})$$

The intermediate terms η and ω are defined for ease of solution:

$$\eta = \frac{CR^2}{4L}$$

$$\omega = \sqrt{\frac{1-\eta}{LC}}$$

Once the maximum current of the circuit is known for a given capacitance, inductance, and resistance, design of the LVEC PFIN becomes possible. Knowing the theoretical maximum current I_{max} at t_1, time t_1, and time t_2 allows comparison to the experimental values from preliminary trials, providing indirect measurement of the circuit's true electrical properties. Examining the quantity η also permits us to estimate the efficiency of the PFIN in transferring energy from the capacitor bank to the power inductor, called "charging". As inductance rises and resistance falls, η also falls, which indicates greater efficiency according to the formula below.

$$efficiency_{\text{charging}} = \frac{W_{t_2}}{W_{C_o}} = \frac{\frac{1}{2}LI_{t_2}^2}{\frac{1}{2}CV_o^2} = e^{-2\sqrt{\frac{\eta}{1-\eta}}Arc\cos(-\sqrt{\eta})}$$

W is the energy in the circuit at the specified time. The efficiency of the circuit in providing power to the load is based on the relative amounts of inductance between the power inductor and the inductance of the railgun. This "discharging" can be estimated from the equation below, which gives the best possible energy transfer, assuming all purely dissipative processes are negligible.

$$efficiency_{\text{discharging}} = \frac{W_{load}(t)}{W_{t_2}} \le \frac{L'x(t)}{L_{power} + L'x(t)}$$

L_{power} is the inductance of the power inductor. The equation is dependent upon the length of the inductor in the railgun (the position of the armature along the rails is a function of time, $x(t)$), so efficiency would seem to improve as the shot progresses. However, this neglects the increasing dissipative losses from coil resistance and the armature

transitioning to more resistive modes of conduction as velocity increases. What is to be gleaned from this relationship, though, is that a great deal of energy stored in the inductance of the power supply is not transferred to the kinetic energy of the projectile, and is thus lost to dissipative processes after the shot is fired or during projectile acceleration. Therefore, while charging efficiency is relatively improved by a higher value of L_{power}, peak current is reduced, dissipative losses in charging the power inductor may be higher, and muzzle efficiency is lost as the size of the power inductor increases. For a fully operational weapon system the efficiency equations must be equated and solved to find an acceptable value for L_{power}, as inductor optimization is critical in creating the most efficient weapon possible. In previous theses, inductor optimization was not a factor, as the relative size of the network or the final pulse shape were of more interest. Here, our primary concern is in maximizing weapon/load current while staying within the rated action of the IGCT's used. This decision process is described more fully in the following section.

For a counterpulsed PFIN, an accurate estimate of the required size of the counterpulse must be known prior to testing if the counterpulse is to protect the main switch adequately. The estimate of counterpulse voltage can be made by considering the relative amounts of energy represented by the current through the switch and main capacitor bank and the electric field in the counterpulse capacitor, or by considering the relative amounts of charge in each. An assumption for both approaches is that the charge on the main capacitor bank is close to zero and does not affect the action of the counterpulse. If the level of reverse bias voltage applied by the counterpulse on the main IGCT be less than the voltage of the main capacitor bank at that time, the counterpulse will not be effective, but if the counterpulse is imposed at the zero voltage crossing of the capacitor bank, residual bank charge should be small enough.

The counterpulse capacitor should have as low a capacitance and as a high a voltage rating as possible, in order to minimize the time of current falloff in the main switch, and thus maximize the efficiency of the switching process. The counterpulse capacitor should also be able to be reverse charged, as the high negative voltage spike from the power inductor may well impose an opposite potential on the capacitor prior to

the counterpulse IGCT ceasing to conduct. Looking at the counterpulse as a process of energy exchange, the following relationship is developed.

$$\tfrac{1}{2} C_{C2} V_{C2}^{\,2} = \tfrac{1}{2} (L_{\text{switch group}} + L_{C1}) I_{t_2}^2$$

$$V_{C2} = I_{t_2} \sqrt{\frac{L_{\text{switch group}} + L_{C1}}{C_{C2}}}$$

C_{C2} is the capacitance of the counterpulse capacitor C2, V_{C2} is the charging voltage of C2, $L_{\text{switch group}}$ is the inductance of the switch group, and L_{C1} is the inductance of the main capacitor bank.

Choosing a voltage in this manner should momentarily drive current in the main switch to zero. Choosing a lesser value will allow some current to continue to flow in the switch, but as long as current is less than the turn-off capability of the IGCT, the main switch should safely open. It is also apparent from this equation and the equation for discharge efficiency (if applied to the left half of the PFIN rather than the load portion) that it is advantageous to limit the inductance of the main capacitor bank.

Approaching the counterpulse problem as a matter of relative amounts of moving or static charge rather than one of energy requires detailed knowledge of the time it takes to turn off the IGCT. The only defined parameter for the IGCT relating to this is the time it takes from ordering the change in state, to receiving feedback that the change has happened, and this is on the order of 5 μs [8]. If this value is used as the time for closure, another relationship can be found.

$$I_{t_2} \Delta t_{closure} = C_{C2} V_{C2}$$

$$V_{C2} = I_{t_2} \frac{\Delta t_{closure}}{C_{C2}}$$

However, there is no way to determine what the actual closure time is, or even if the closure time stays reasonably constant, therefore all estimates for initial counterpulse voltage were made using the energy relationship. The voltages V_{C2} from both equations are not equivalent, but when worked out using the experimental component values, the V_{C2} found using the energy relationship invariably resulted in a higher value. As this was

the most conservative value, and it had the least unknown quantities, the energy relationship was used to select for V_{C2}. In practice, the arrangement of components and the presence of additional components not shown here became an issue, and will be covered later, but they had no appreciable affect upon the PFIN theory as presented.

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III. LVEC PFIN DESIGN AND CONSTRUCTION

A. CAPACITOR BANK

Design and construction of the LVEC PFIN necessarily begins with the capacitor bank, because its design will affect the construction of the remaining components. Given the desired parameters of high capacitance, low voltage rating, efficient and effective charge storage and discharge capability, and low equivalent series resistance, there are still a myriad of electrolytic capacitors to choose from. When construction of the PFIN was first proposed at NPS, a large number of Cornell-Dubilier 2500 μF, 360 VDC capacitors were procured, enough for 250 kJ of PFIN modules. From these a 60 capacitor, 9.72 kJ module was assembled; however this unit proved too fragile and assembly was too time consuming to attempt to duplicate. The 2500 μF capacitors were designed with solder posts rather than screw posts, and they proved to be too difficult to work with in our experimental environment. Though they may prove useful in a later experiment as greater power levels are attempted, these first capacitors and their constructed bank were rejected for my thesis.

Instead, 50 Cornell-Dubilier capacitors (Model PF212V500BF2B) were used. These were 2100 μF, 500 VDC photoflash electrolytic capacitors with screw terminals and an individual equivalent series resistance (ESR) of ≈ 95 mΩ [9]. Mounted in parallel in order to maximize capacitance and minimize ESR and inductance, the resulting capacitor bank would have a capacitance of 0.105 Farads, an ESR of 1.9 mΩ, a rated voltage of 500 VDC, a total energy of 13.125 kJ. Each capacitor was individually brought to a 500 VDC charge to verify they would not fail, and then discharged for assembly.

The arrangement of capacitors was modeled with the computer-aided design (CAD) program Rhino and then placed in a square array. The copper bar stock available allowed us to place eight capacitors side by side; therefore, the bank was designed to have eight rows of capacitors, with 64 capacitors in parallel, arranged in a single layer, and feeding both a negative and positive bus (see Figure 8). Should more capacitors be procured, a single 64 capacitor bank would have a total capacitance of 0.1344 Farads, an

ESR of 1.5 mΩ, and energy of 16.8 kJ. The single layer configuration easily lends itself to adding another layer on top, doubling the possible energy storage capability.

The inductance of the bank C1 was measured by connecting it in series with a much smaller capacitor (thus lowering the overall capacitance to a value just under that of the small capacitor) in a tank circuit. The circuit was then driven with a function generator and its resonant frequency found, which then allowed the resulting inductance of the bank to be calculated using the following formula.

$$L_{C1} \approx (4\pi^2 f^2 C_{equivalent})^{-1}$$

With this method, the inductance was $L_{C1} \approx 0.24$ nH for the bank. This low amount of inductance will likely be overshadowed by the inductance of the switch group's bus, as the size of the switches necessitate three, approximately 0.75-m runs of copper bar stock.

Electrolytic capacitors will not tolerate reverse charging; therefore diode protection must be installed. An array of three ABB pressure mounted diodes (Model Nr. 5SDA24F2003 [8]), D1, were mounted over the capacitor bank, in parallel, and configured such that any reverse voltage applied to the bank would forward bias the diodes and short out the bank entirely.

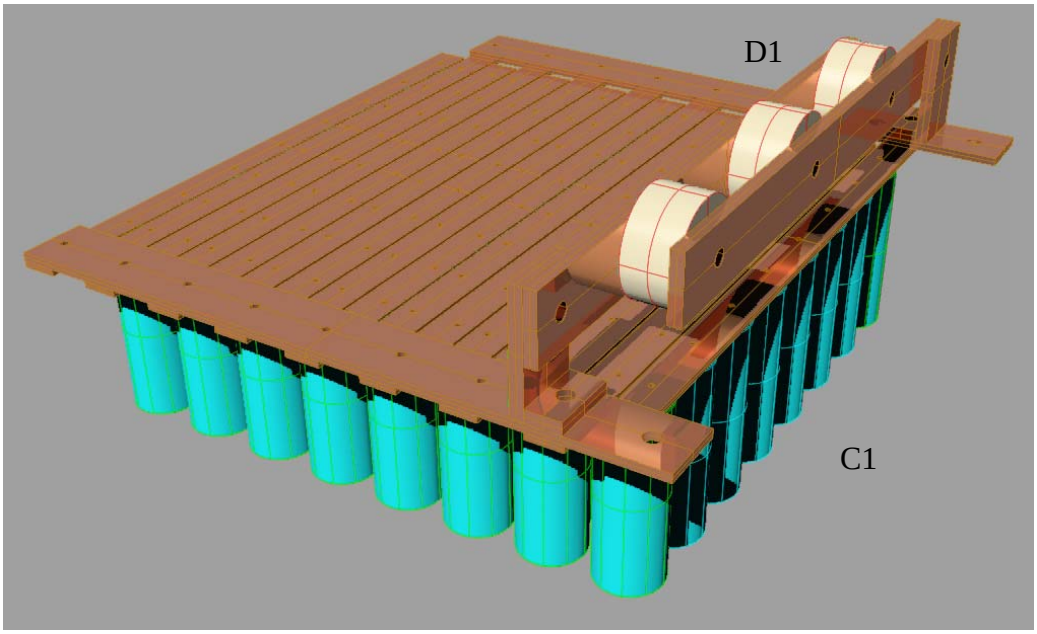

Figure 8. LVEC Bank Design

B. SWITCH GROUP

To handle the main current (which is projected to approach 50 kA) a fast semiconductor switch with adequate turn-off capability is needed. Four ABB IGCT's (Model Nr. 5SHY35L4512 [8]) were procured, rated at 4500 V hold-off, 35 kA surge current (in 10 ms), and a 4000 amp turn-off capability. Though the intended pulse length is much shorter than 10 ms, implying each IGCT could perhaps handle a full 50 kA, we decided it would be safest to install two IGCT's in parallel (A1 and A2) to act as the main switch.

The IGCT's are pressure mounted, ceramic disk devices, with the gate driver and switch protective networks (snubber) mounted on an attached circuit board. The dimensions of the IGCT, including those of the 40 kN mounting brackets, were drawn in Rhino and bus work was designed to tie the main switches to the positive side of the capacitor bank (see Figure 9).

A third IGCT, B, was designed to fit below the parallel main switches, with bus work designed to place the switch in parallel with the primary IGCT's and in series with the counterpulse capacitor, C2. The counterpulse capacitor itself was designed to connect via cables rather than rigid copper bars. Since it was not clear at this point how much capacitance would be needed in the counterpulse circuit, we anticipated trying a variety of capacitors in that position. To provide enough energy to reduce a 50 kA peak current down to an acceptable 8 kA stopping current, and assuming $L_{\text{switch group}} \approx 1$ μH inductance, the counterpulse capacitor C2 would have to provide 882 J through some combination of high voltage and capacitance. Since the true residual inductance was not known at that time, and since the balance between higher voltages or higher capacitances had not been decided, flexible cable connections to the counterpulse capacitor seemed the best idea.

Each of the IGCT's could be driven by AC or DC power, requiring a fiber optic light pulse to operate. A 28 V DC power supply was connected to each of the gate units, and an LED pulse box and delay generator were hooked up to provide control. The gate units themselves provided status feedback on their condition through a set of LED indicators on the IGCT. The heavy bar stock, rigid connections, and substantial weight

of all the components and copper obviated the need for tie-downs to secure the PFIN from any movement during a current surge, but wooden support blocks were measured and cut to prevent undue stress from damaging the bus bars. The initial switch design is given in the figure below. Switches are beige in color, and the counterpulse capacitor is shown in blue.

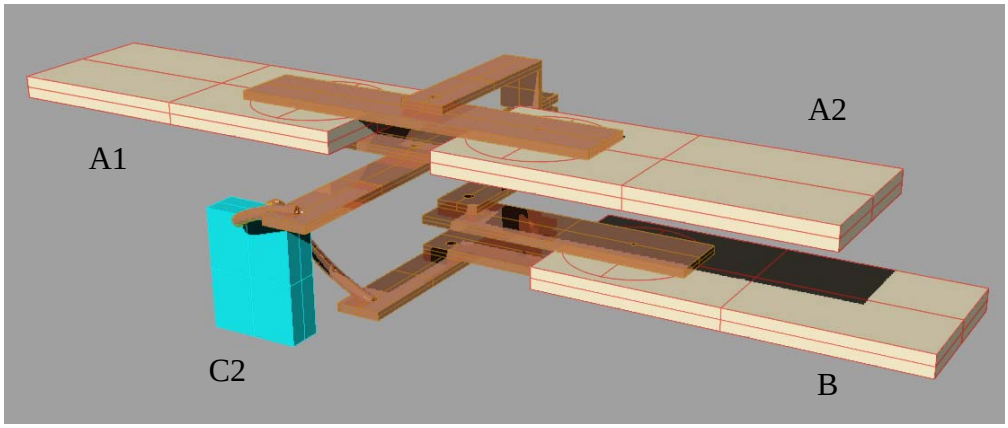

Figure 9. Switch Group Design

C. POWER INDUCTOR

The inductor assembly includes both the large power inductor, L1, and the load diode, D2, which prevents current from entering the load while the capacitor bank C1 is discharging. The load diode is a pressure mounted ceramic disc, ABB diode (Model Nr. 5SDD50N5500 [8]) rated at 5500 V, 73 kA, and mounted with a 90 kN bracket.

As stated before, it is desirable to have as low an inductance *L* and resistance *R* in the power inductor as possible, while keeping the peak current within the rated capacities of the switch group. A low value for *R* delivers a low η and thus a high efficiency from the capacitor to the power inductor. If the design current is 50 kA, and if resistance is negligible ($\eta \approx 0$), then the desired inductor size is 10.5 μH. In reality, the resistance of such an inductor is not negligible and would lower current below the 50 kA goal. In order to predict the inductance, resistance, and final shape of the air-core coil inductor to be assembled, the following empirical equations were used [10].

$$L_{L1} = \frac{0.001N^2r^2}{228r + 254l}$$

$$R_{L1} = 0.1608 \cdot (2\pi rN + 0.5)$$

N is the number of turns in the coil, r is the radius of the coil (in meters), and l is the length of the coil turns. Using 4/0 copper welding cable, extra cable insulation, and a 12.5 inch diameter PVC pipe as a form for the coil, it was found that a four turn coil wound inside the pipe would provide an inductance of L_{L1} = 5.7 μH and a resistance of R_{L1} = 0.63 mΩ. The measured values for inductance and resistance after construction were $L \approx 6.2$ μH and $R \approx 0.7$ mΩ. The coil was wound within the interior of the PVC pipe in order to restrain the inductor from its natural tendency to expand radially and shrink axially during high current transients.

The calculated value for η from the values above is 0.0295, which gives a projected inductor charging efficiency of 54.4 %, places t_1 at 1.10 ms and t_2 at 1.37 ms, and gives a peak current of 53 kA for an initial capacitor bank voltage of 500 VDC. The process can be made more efficient by using better conductors, conducting paste, or parallel coil windings. Cutting resistance in half would result in $\eta \approx 0.007$, a charging efficiency of 76 %, and a peak current of 59 kA. However, while not yet optimized for performance or size, the values calculated from the given configuration (see Figure 10) are acceptable for the goals of this experiment.

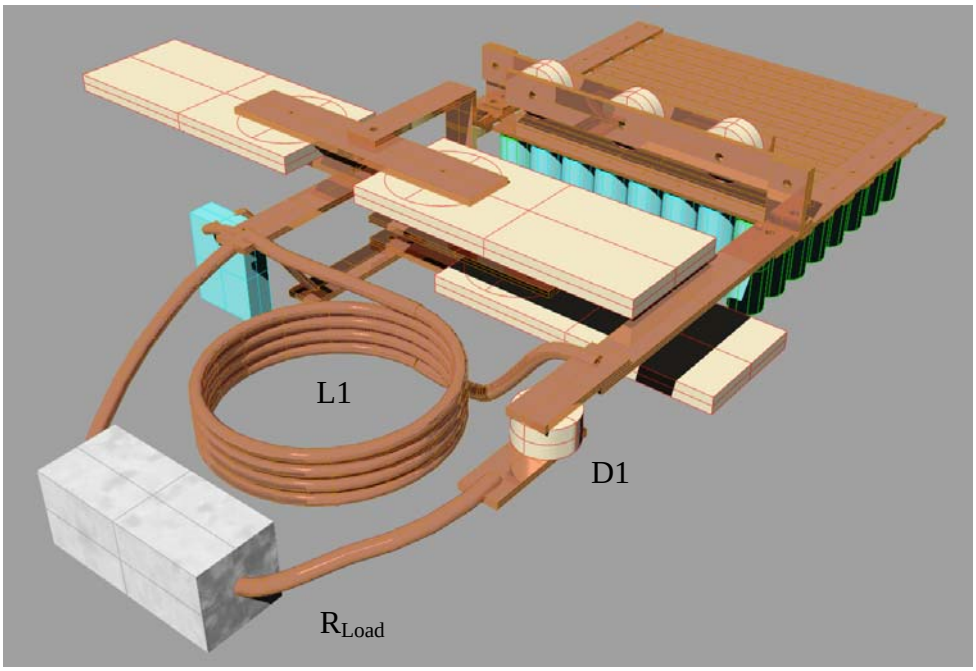

Figure 10. Complete LVEC PFIN Design, Power Inductor and Load View

D. CONSTRUCTION AND ASSEMBLY

The Rhino design plans required little alteration from drawing to reality and the copper was cut, bent, and assembled over the course of weeks. The entire unit was mounted on a sheet of plywood atop a portable table and placed near power connections for charging the capacitors. Two high voltage power supplies were connected in parallel to the two sets of capacitors and the LVEC PFIN was ready for preliminary testing. Figure 11 shows the initial schematic, as constructed.

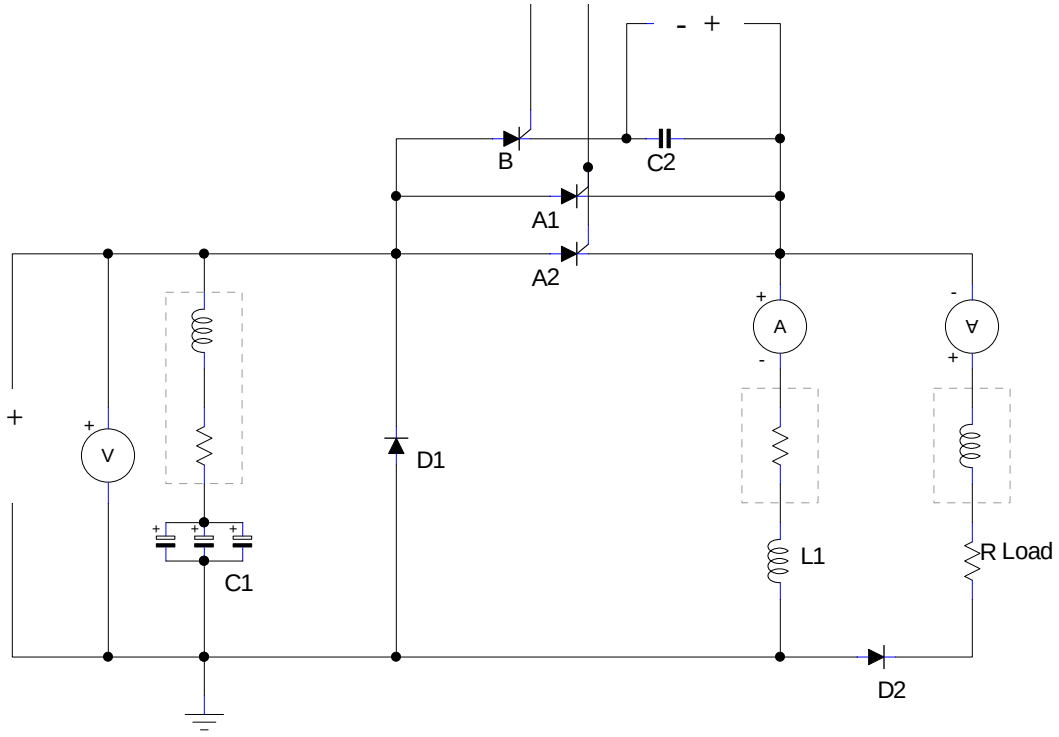

Figure 11. LVEC PFIN, Initial Schematic, Before Testing Changes

In this schematic, the negative side of the main capacitor bank C1 is grounded. The counterpulse capacitor C2 power supply was configured to float, with L1 equivalent to ground when no current was flowing through the circuit, thus providing a negative voltage with respect to ground to the cathode side of the counterpulse IGCT B. The switch group is comprised of main switches A1 and A2, as well as the counterpulse switch B. Current monitors were added to read inductor current I_{L1} and load current I_R, the difference between them being switch current I_S. Voltage dividers were added to monitor main capacitor bank voltage V_{C1} and power inductor voltage V_{L1}, their difference

being the switch voltage V_S. Surrounded by boxes in the schematic are the inherent resistances and inductances within the components, bus work, and cabling, all of which had to be simulated as separate components in the P-SPICE model of the circuit [8], [9].

C1 Voltage Rating	500 VDC
C1 Capacitance	2100 µF · 50 = 0.105 F
C1 ESR	0.095 Ω / 50 = 1.9 mΩ (rated) 0.036 Ω / 50 = 0.72 mΩ (meas)
C1 Inductance	0.235 nH (meas)
C1 Energy	262.5 J · 50 = 13.125 kJ
D1 Voltage Rating	2000 VDC
D1 Surge Current	29 kA · 3 = 87 kA
D1 Bias Voltage	1.35 V dropped
A1, A2 & B Voltage Holdoff	4500 VDC
A1, A2 Surge Current	35 kA · 2 = 70 kA (10 ms pulse)
A1, A2 Shut-off Current	4 kA · 2 = 8 kA
A1, A2 & B Max dI / dt rise	200 A / µs
A1, A2, & B r_T	0.21 mΩ
A1, A2, & B Reverse Voltage	17 VDC
C2 Voltage Rating	+/- 1600 VDC
C2 Capacitance	100 µF
L1 Inductance	5.67 µF (calc), 6.2 µF (meas)
L1 Resistance	0.63 mΩ (calc), 0.7 mΩ (meas)
D2 Voltage Rating	5500 VDC
D2 Surge Current	73 kA

Table 1. Overview of Major LVEC PFIN Components

The initial version of the LVEC PFIN is shown in Figure 12, prior to changes made during preliminary testing. The power and control leads were not yet attached, but all components were in place.

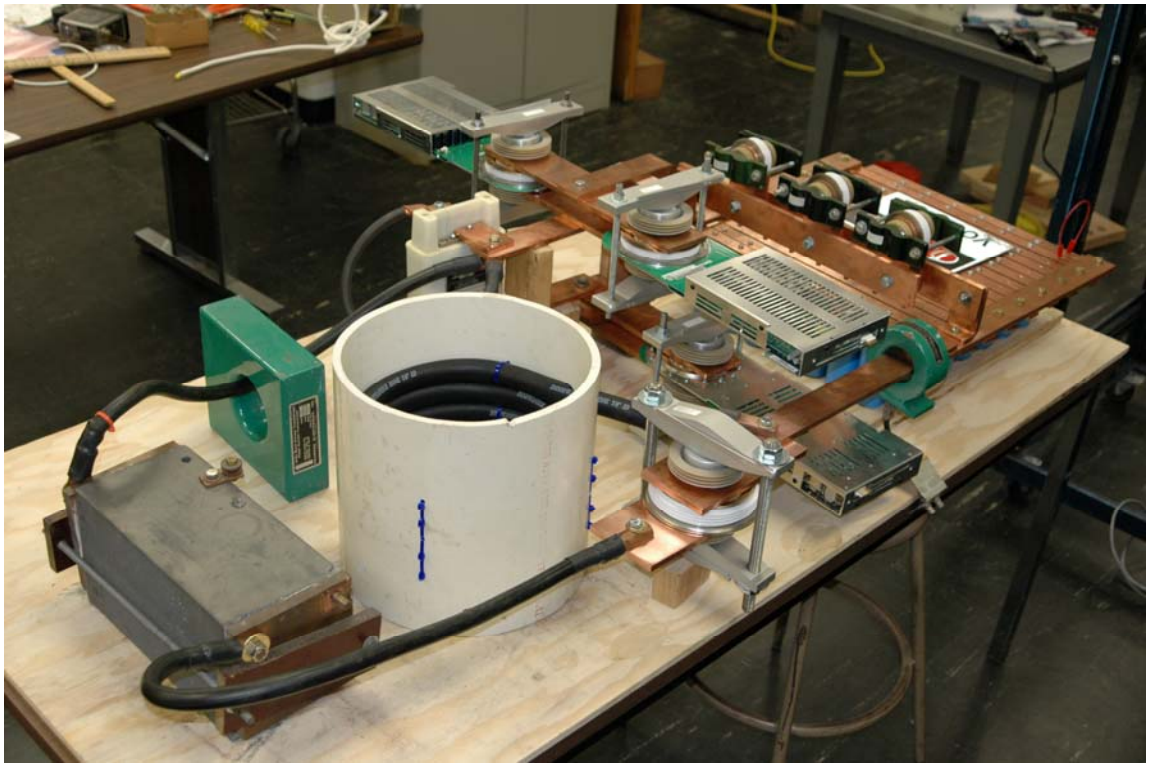

Figure 12. LVEC PFIN, Initial Version

IV. LVEC PFIN TESTING

A. TESTS OF SWITCH CAPABILITIES

The first priority was to verify proper operation of the IGCT's in their assigned roles, so initial testing of counterpulsed switch opening was done at 10 VDC - 50 VDC, which corresponds to a peak current $I_S = I_L \leq 8$ kA. If the switches performed to specifications, this current would still be below the safe current shut-off rating of the IGCT's, rendering the counterpulse superfluous. This initial testing also allowed us to evaluate our data-recording equipment and procedures, as well as the validity of the theory and the P-SPICE model of the LVEC PFIN.

The first tests were run at 10 - 150 VDC, with no attempt to close the counterpulse switch B and no attempt to open main switches A1 or A2. For these tests the current was allowed to decay exponentially in the current path back through the capacitor/diode bank (C1 and D1) as well as through the load (R_{Load}). The power supplies for C1 and C2 were disconnected after charging their respective capacitors for each of these tests. Data are shown in Figure 13, where V_{C1} is shown in yellow (trace 1), I_L is green (trace 2), and I_R is purple (trace 3). Note that the load current I_R does not begin to rise until bank voltage V_{C1} drops to zero and the induced voltage in the power inductor compensates in order to maintain current, thus forward biasing D2.

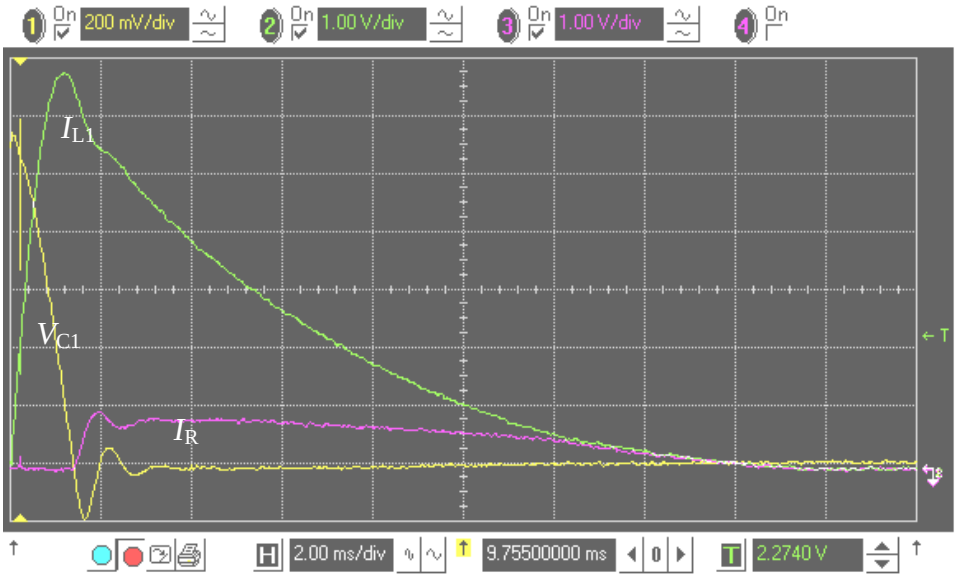

Figure 13. Preliminary Testing, No Opening, No Counterpulse

For each of these tests, either A1 or A2 was used independently, with no attempt at parallel operation and with the unused switch's gate unit powered down. These first tests performed much as expected, but gave no real data on the performance of the circuit, other than the fact that the switches held off the bank voltage until commanded on, closed properly. Each switch could individually handle currents of up to 20 kA. One problem that did occur was that when the capacitor bank passed through its zero voltage point, the diodes D1 did not seem to conduct adequately, allowing the bank to momentarily charge to a negative voltage equal to approximately 20% of the initial bank voltage. Since the diode bank was verified to be working properly, the fault seemed to present either a problem with the voltage monitors or something else was allowing the bank to build to a negative voltage. It was theorized that the multiple current pathways present atop the capacitor bank might allow some inductive "cross talk" between capacitors once the circuit currents began to fall and the bus work between capacitors acted as individual inductors, reversing voltage to maintain current flow. These circulating currents would normally be cancelled out by the conduction of the diodes D1, but since the diodes were physically attached to only one point around the bank, cross talk might still occur. Though it might be deemed excessive protection, two more diodes were added atop the capacitors, one tied into the center of C1 and one tied to the end opposite the original diode bank. Unlike the smaller ABB 5SDA24F2003 diodes originally used for D1, two of the larger ABB 5SDD50N5500 "pucks" were added [8]. The 5 diodes paralleled to the main capacitor bank and physically attached at different points seemed to resolve the cross talk issue. Subsequent tests showed the diodes conducting properly, preventing any large negative build up of voltage. These first tests also confirmed the peak values of I_L at t_1, as well as the approximate timing of t_1 and the zero crossing of the bank voltage at time t_2. These confirmations validated both the P-SPICE model of the circuit and the theory laid out earlier in this thesis.

The next tests were confined to main bank capacitor voltages of 10 - 25 VDC ($I_S \leq 4$ kA) and A1 and A2 were tested independently with the offline switch powered down. During these tests, the switches were opened (commanded off) at time t_2, just after the current peak in the power inductor when the bank voltage was zero. As the current was approximately 3400 Amps, no counterpulse was used or needed. Two problems were

immediately apparent. First, the current monitors appeared to show markedly different readings of currents which should be almost identical. Second, the IGCT's would open/turn off when commanded, 1.3 to 1.5 ms after being closed/turned on at time t_0, but only momentarily, for a period on the order of microseconds. After current began its sudden jump to the load (I_R) at time t_2, conduction through the switch group would recommence and would then decay through both current paths, as it had in the first set of non-opening preliminary tests.

The different switch current readings were determined to be due to the current monitors themselves. When both identical Pearson 1330 inductive current monitors were positioned to measure I_L at the same time, they each showed different readings, with a variance of nearly 20% between them. Since neither unit agreed exactly with the P-SPICE simulation value for I_L (nor were the final values of total resistance and inductance known to make a more accurate simulation), and since there was not a third 1330 monitor available, nor a procedure for calibrating a particular unit, this difference was accepted. Both units were then put back in place in order to give a qualitative, rather than quantitative, measurement of current rise and fall.

The erratic IGCT behavior confounded the railgun group and the IGCT manufacturers as well. The aborted interruption of current at levels below the rated capability of the semiconductor switches was unprecedented. Each switch, A1, A2, and even B was tried individually but without success, the exact same problem occurring on each IGCT. Some unknown factor was causing the switches to turn on and conduct after they had been commanded off/opened. Eventually, we tried operating both A1 and A2 simultaneously, in parallel as the design had originally intended, with power to the gate units of all three IGCT's. Surprisingly, the LVEC PFIN worked as it was supposed to, successfully shutting off currents of 3400 - 7000 Amps. Whether this is a fault or whether it is by design is not entirely understood, but the un-powered, un-commanded IGCT's would conduct whenever the power inductor reacted to the opening of the tested switch by reversing voltage. However, since the circuit worked when operated according to design, the condition was not investigated further. In Figure 14 below, a typical set of data from this series of tests is shown for a V_{C1} = 25 VDC shot, where V_{C1} is yellow trace 1, I_{L1} is green trace 2, and I_R is purple trace 3. Note the sharp current spike and jagged

oscillation of both I_L and I_R, as well as the fact that the purple and green current traces do not match up exactly, though they read the same amount of current after A1 and A2 are opened. This is due to differences in the actual sensitivity of each current monitor.

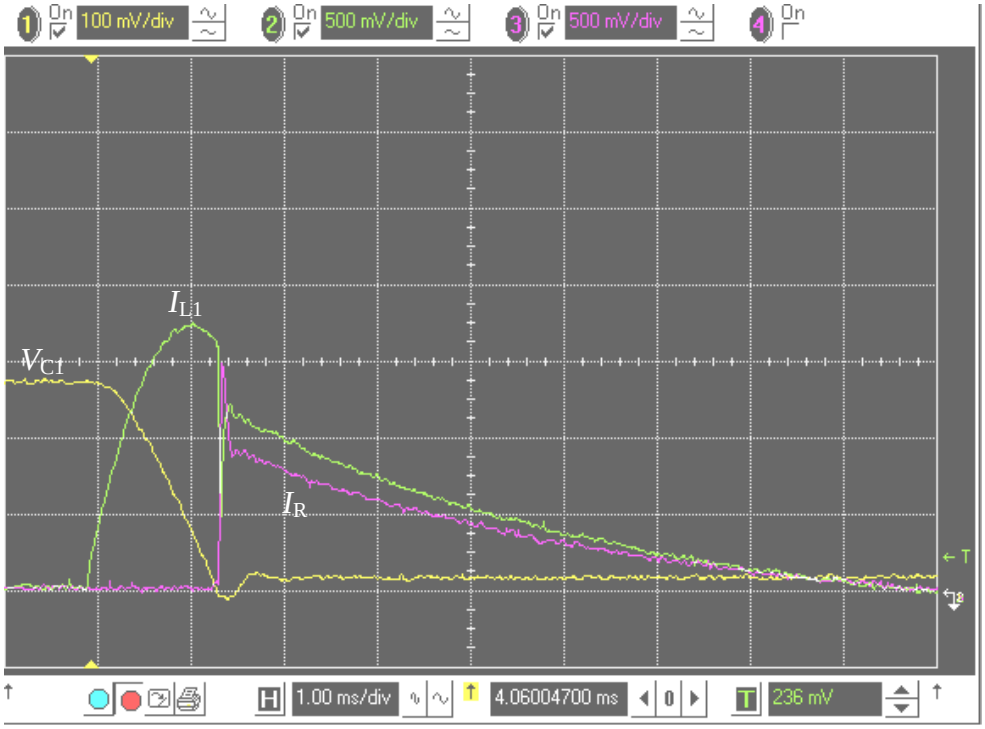

Figure 14. Preliminary Testing, Opening With No Counterpulse

Once the IGCT's were confirmed to open effectively, tests were begun to see how the circuit would react to a counterpulse. Initially, the counterpulse capacitor could not be charged. When its voltage supply was turned on to apply a negative voltage, charge current would go to maximum but the voltage across C2 would remain zero. There was evidence that the negative voltage was being grounded out, but no ground was immediately apparent. It was discovered through ground isolation that capacitor C2 would only hold a negative charge when power was removed from the counterpulse IGCT B's gate control unit. The manufacturer later confirmed that the cathode of the IGCT was connected to ground through the gate driver, a path not indicated on the switch's specification sheet. The grounding characteristic required a rearrangement of components, placing C2 on the anode side of B, such that C2 was in series with C1. This new arrangement is electrically identical to the previous one, except that now a positive voltage could be applied to C2 in order to reverse bias A1 and A2.

Counterpulsing should produce a momentary drop in current through the main switch, or should show as a momentary rise in current through the load. Since the main switches are still commanded on/closed, current should again flow fully through both paths once the charge on the counterpulse capacitor is dissipated. This brief shift of current was borne out by observations of the circuit through multiple tests at both V_{C1} = 25 VDC and 50 VDC with a counterpulse capacitance C2 of 100 µF, and counterpulse voltages V_{C2} = 100 VDC - 300 VDC. When monitoring the change in load current, the counterpulse was very hard to detect, the change being so short in duration that little current was forced onto the alternate path through the load. When the current monitor was moved to monitor switch current, however, the counterpulse effect was very evident. It was noted that the counterpulse lowered current most effectively when the voltage on the capacitor bank was zero, about 1.4 ms after the main switches were closed/turned on, very close to t_2, with $t_1 \approx 1.1$ ms, in close agreement to both theory and the P-SPICE model. Figure 15 shows an example of this series of tests, specifically a shot in which V_{C1} = 25 VDC and where V_{C1} was yellow trace 1, I_L was green trace 2, I_R was purple trace 3, and I_S was red trace 4 (measured with a Pearson 1432 current monitor, equivalent to I_L before t_2).

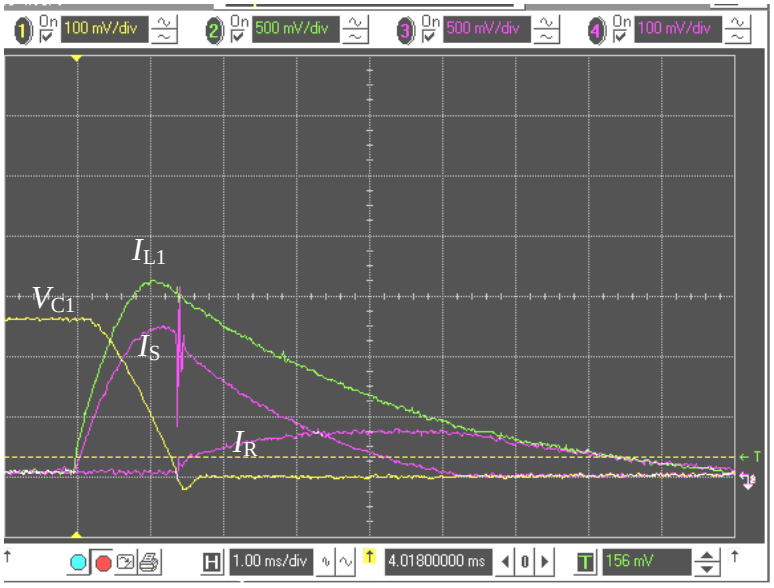

Figure 15. Preliminary Testing, Counterpulsing With No Opening

When monitoring I_S during a counterpulse, a great deal of sharp oscillation was present. This oscillation indicated a possible circulation of currents and could have lead to a reverse current condition through the main switches or the counterpulse IGCT. Two things were done to minimize this oscillation and to reduce the corresponding sharp oscillations in switch voltage: the addition of a snubber capacitor C3 = 100 μF and a snubber resistor R1 = 50 kΩ in parallel to IGCT's A1 and A2, similar to protecting a regular thyristor; and an input diode D3 to the counterpulse capacitor, which provided a one-way isolation between C1 and C2 as well as removing almost all oscillations during both a counterpulse and an opening. D3 was only a small, parallel diode string, rated at 1000 volts hold-off, but at the time, it was all that was available and it was well outside the voltage we were testing on the counterpulse circuit. Aside from removing most of the sharp oscillations present during a counterpulse or the opening of the main switches, D3 also allowed a negative charge to be built up and retained on C2 from the momentary voltage reversal of the power inductor. This voltage was simply bled off by triggering the uncharged LVEC PFIN a second time after data was taken for the charged run.

The final preliminary test was to operate the LVEC PFIN as a pulse power supply, from discharge, to counterpulse, to opening, and to monitor its operation at a low, safe voltage and current. For these tests C1 was charged to either 25 or 50 VDC, C2 to several values from 160 VDC to 400 VDC, and the circuit was operated at several different values of $t_2 = t_{\text{counterpulse}}$ = 1.4 or 1.45 ms, and t_{opening} of 1.4163 or 1.472 ms respectively (which corresponded to the time at which switch current was lowest following the counterpulse). This series of tests showed adequate counterpulsing, with curves and times similar to that of the P-SPICE simulations, with one exception. Though most of the oscillations and odd current behavior of the IGCT's had been resolved by the addition of the snubber and the input diode D3, a reverse current spike was observed for I_S upon every opening of A1 and A2 preceded by a counterpulse. Figure 16 shows a typical test at V_{C1} = 50 VDC, where V_{C1} was yellow trace 1, I_{L1} was green trace 2, I_R was purple trace 3, and I_S was red trace 4. Note the sharp reverse current spike in I_S after t_{opening}.

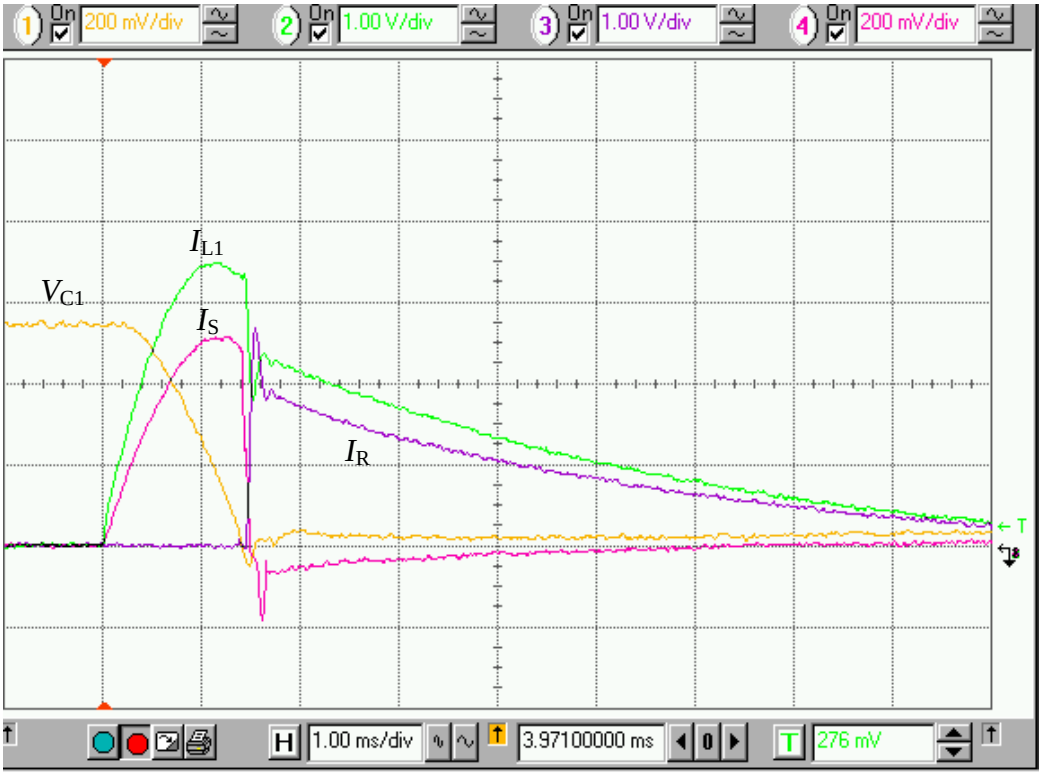

Figure 16. Preliminary Testing, With Counterpulse, With Opening

A reverse current condition was not believed to be possible in a thyristor device like the IGCT due to the arrangement of semiconductor junctions. Since reverse current implies a negative voltage and a corresponding reverse bias, current should be stopped by A1 and A2 before going negative, just as it would in a diode. The IGCT's did not react adversely to passing the brief reverse current, and it was not known if the lack of response was an undocumented characteristic of the IGCT or if it implied an impending fault. Left with no explanations and a rigorous testing schedule, we made the decision to continue testing at higher voltages and currents, since the overall design of the LVEC PFIN was working. It was not until later in testing that we decided to add another diode, D4, between the switch group and the power inductor in order to solve the problem (see Figure 17).

B. DESIGN ALTERATIONS AND CIRCUIT ADDITIONS

By the time true testing began, the LVEC PFIN schematic from Figure 11 was no longer valid. Changes included the addition of two large diodes to the diode bank D1 to reduce circulating currents and voltage spikes in the main capacitor bank; the reversal of

B and C2's positions in the counterpulse branch of the circuit to allow charging of C2; the addition of the counterpulse input diode D3 and the snubber circuit R1 and C3 in order to reduce the sharp current and voltage oscillations associated with operation of the switch group; the addition of a third current monitor, a Pearson 1432, to monitor I_S; and finally the addition of another ABB 5SDD50N5500 diode D4 in order to keep the large negative voltage spike from the power inductor from affecting the switch group, thus normalizing currents to the P-SPICE ideal [8]. These changes are all reflected in Figure 17 below.

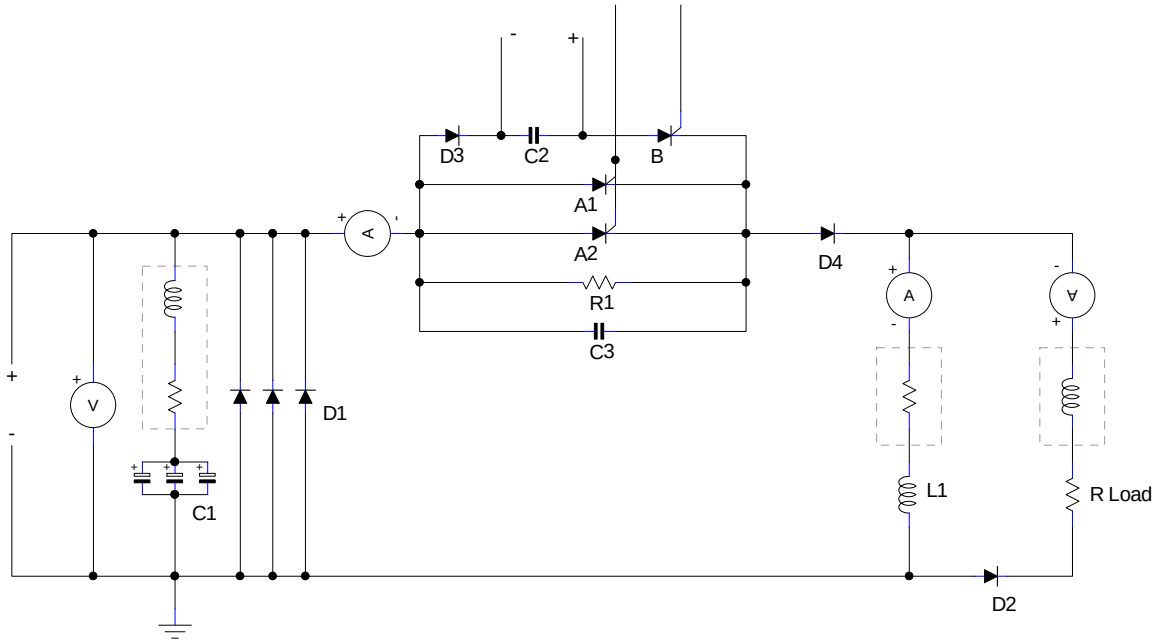

Figure 17. LVEC PFIN, Revised Schematic

Not indicated here are the specifics of the various types of voltage meters and differential amplifiers used to measure switch group voltage. Measuring the voltage across the IGCT's proved to be very difficult and no satisfactory direct measurement was ever achieved. Instead, the only reliable measurement came from measuring the voltage difference between the main capacitor bank C1 and the power inductor L1.

C. HIGH POWER TESTING

Once preliminary tests were completed and we had a fairly good understanding of the circuit (as represented in Figure 17, with the exception of D4), testing above the rated IGCT capabilities could proceed toward the 500 VDC, 50 kA goal. The testing procedure was the same at every voltage step. First the system was discharged without

counterpulsing or switch opening to establish a baseline for the current traces at that V_{C1}. Then, the system was counterpulsed at t_2, but not opened, so both the fall time and current drop from the counterpulse could be verified. The counterpulse was designed to lower total current I_S through A1 and A2 to less than 8 kA. Finally, once the optimal time for opening was verified, several tests were done, counterpulsing the switch at t_2, then IGCT's A1 and A2 were opened at the point of least current.

1. 50 VDC to 125 VDC

The first sets of tests were done with the LVEC PFIN in the configuration seen in Figure 17, except for the inclusion of diode D4. Also, due to the limitations of our counterpulse power supply and a recognized need for more energy in the counterpulse to offset the higher currents for these tests, a larger high voltage power supply was put across C2 and three other capacitors were added in parallel to the counterpulse capacitor, bringing C2's parameters to 1600 VDC max and 270 µF. This change placed the optimal t_1 at 1.1 ms, t_2 at 1.4 ms, and $t_{opening}$ at 1.447 ms, though other times were also tried for individual tests in order to see how the PFIN responded. The current and voltage traces appeared much as they had in Figure 16, except for variations in oscilloscope scale.

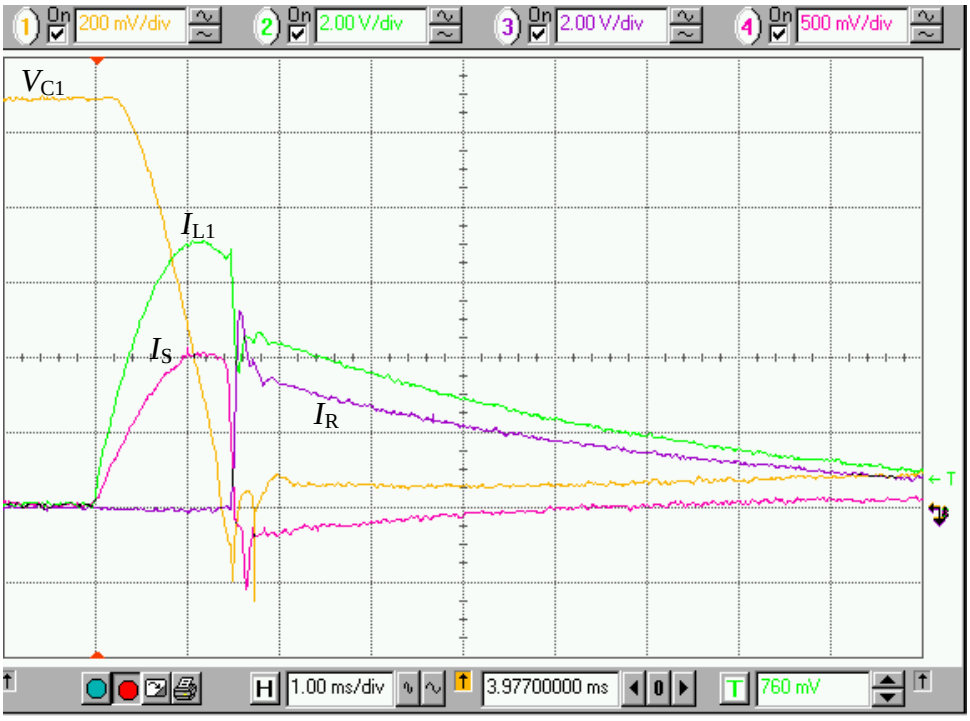

Figure 18. LVEC PFIN at V_{C1} = 100 VDC, Before Addition of D4

Testing according to our procedure went quickly and well, validating the operational concept and design of the LVEC PFIN. Tests were conducted at V_{C1} = 50 VDC, 75 VDC, and 100 VDC, achieving a maximum switch current I_S of 9.6 kA (calculated) or 10.4 kA (measured, with simultaneous measurement of I_L = 14.26 kA and I_R = 0.0 kA). The counterpulse capacitor was charged to various voltages from 300 VDC to 800 VDC, with the empirical result that every 100 volts put on C2 resulted in approximately 1 kA reduction in switch current. This relationship is rough due to the inconsistent current sensitivities of the three Pearson current monitors, which should have all been in complete agreement.

After conducting several shots at V_{C1} = 100 VDC and V_{C2} = 800 VDC, a fault condition was shown on the counterpulse switch, IGCT B, and the counterpulse capacitor would no longer hold a charge. The fault indications and the inability to charge C2 pointed to a short to ground through the sensitive gate circuitry which incidentally shared a ground with the cathode of the IGCT. The maximum reverse voltage on the IGCT was supposed to be 17 volts, according to the specification sheet, but it had not yet presented a problem even in the early tests when inductor voltage consistently exceeded that value many times over. Current however should not have flowed in the reverse direction through B because of D3, however, so this fault was seen as a singular failure rather than a design flaw. As was understood later, D3 would prevent a reverse current from cathode to anode, but due to the sensitive internal connection between the gate and the cathode, a negative voltage at the cathode would not be deterred by a diode on the anode. In the hope that this failure was due to damage done when the IGCT and the counterpulse capacitor were in their initial configurations, or was due to a momentary surge, the IGCT was removed and replaced with the one remaining spare.

There were many things not understood about the operation of the IGCT's when this thesis began, their extreme sensitivity to reverse voltage and their ability to conduct in the reverse direction for a short time being chief among them. Now that these issues were apparent, however, it became prudent to protect the IGCT's from these damaging voltages and currents. At this point, a fourth diode, D4, was added at the common cathode of the switch group, leading into the power inductor L1. The ABB 5SDD50N5500 had a high enough rating to protect all three IGCT's from a negative

voltage on the cathodes and should protect the gate drivers. It would also eliminate the reverse current spike in I_S after counterpulsing and opening.

Testing with the new switch and diode was begun at V_{C1} = 50 VDC and V_{C2} = 300 VDC and continued through V_{C1} = 125 VDC and V_{C2} = 1000 VDC according to the established procedure. These tests showed the smoothest current traces and switch transitions yet, as close as possible to the P-SPICE ideal, thus proving that diode D4 was necessary for the proper operation of the LVEC PFIN. At V_{C1} = 125 VDC, peak current was I_S = 11.998 kA (calculated) or 12.64 kA (measured, with a simultaneous measurement of I_L = 17.5 kA and I_R = 0.0 kA). Figures 19 and 20 show these values, with V_{C1} as yellow trace 1, I_L as green trace 2, I_R as purple trace 3, and I_S as red trace 4.

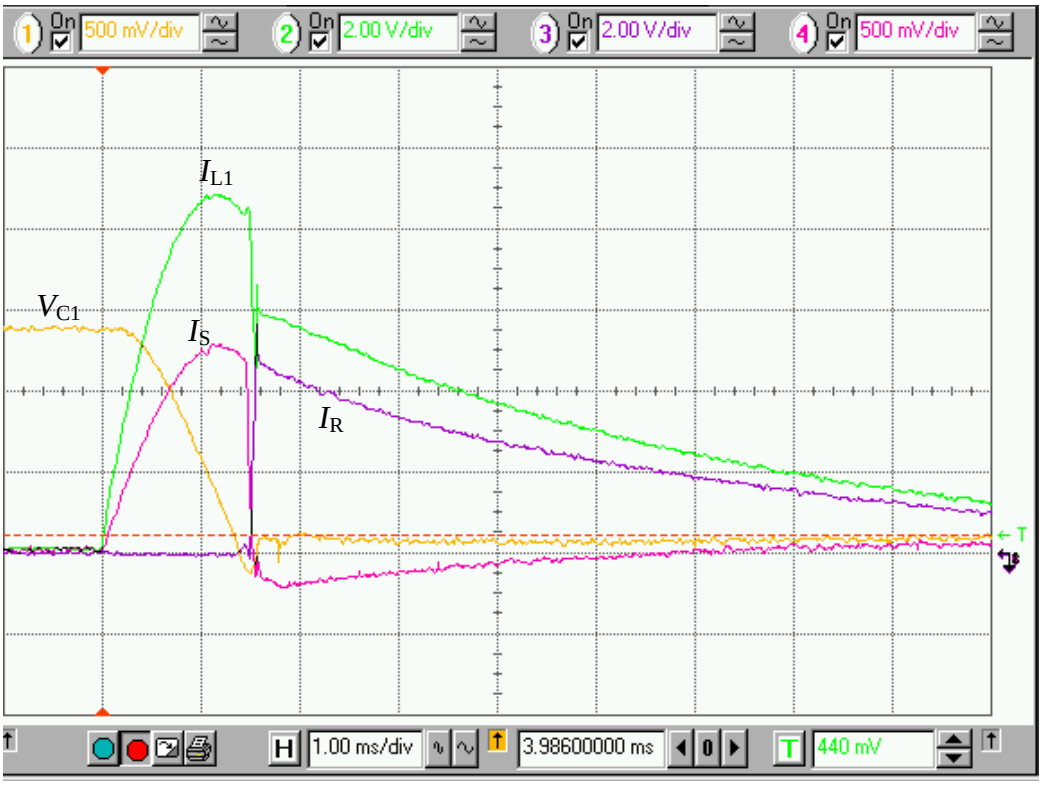

Figure 19. LVEC PFIN at V_{C1} = 125 VDC, After Addition of D4

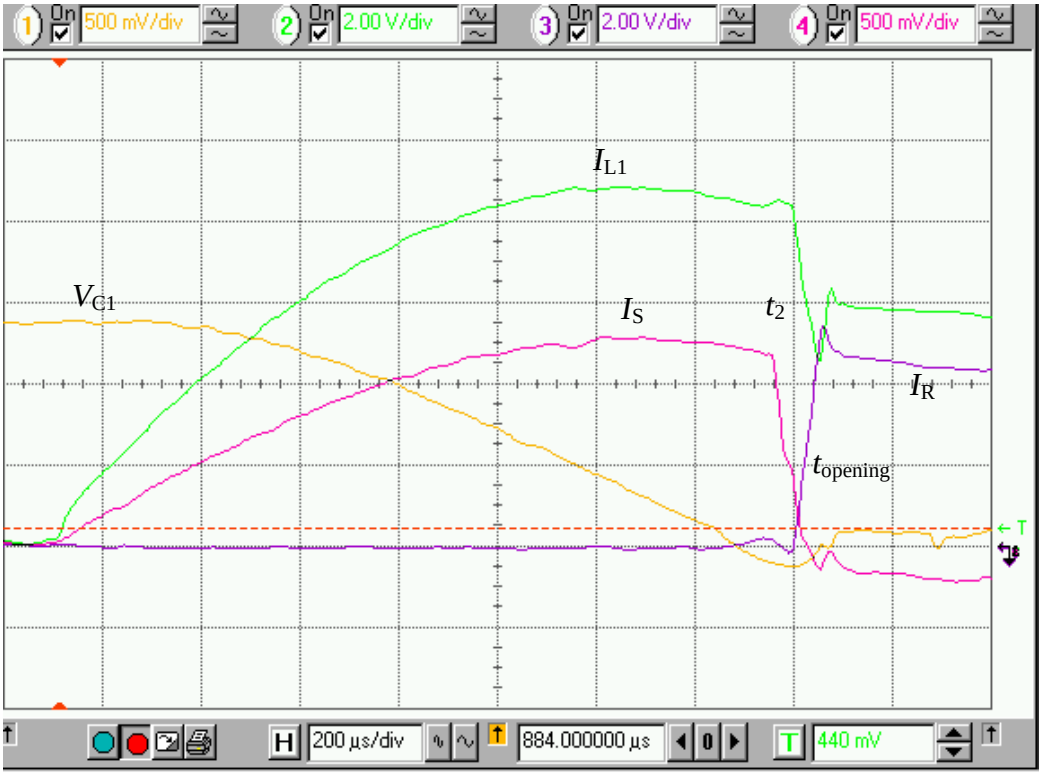

Figure 20. LVEC PFIN at V_{C1} = 125 VDC, Expanded

Unfortunately, as preparations were made for an additional test at V_{C1} = 125 VDC before resetting and beginning the test procedure for 150 VDC, diode D3 failed, shorting out during the charging of C2 to 1000 VDC. It was surmised in later analysis that the diode failure allowed the floating ground of C2's power supply to present -1000 VDC to the switch group's common anode. The voltage divider formed by the snubber circuit resistor and the cathode-to-gate current path of the counterpulse switch allowed more than 17 volts reverse voltage to be placed upon IGCT B, causing it to short out through the gate unit. Though the counterpulse switch was originally thought to be the least important and least stressed of the three IGCT's, it had proved to be the weak point in the circuit several times.

It is important to understand that the difficulties imposed by the counterpulse IGCT have less to do with the PFIN or counterpulse concepts than they do with the choice of semiconductor switches in that position. An IGCT was used for switch B because it was the highest rated semiconductor device on hand when construction began. Since the characteristic ability of the IGCT - the ability to turn off large amounts of

current - was not required for the counterpulse switch, any high power thyristor would work. In fact, the sensitive gate-cathode connection was a significant liability given the amounts of current being shifted and the floating nature of the high potential stored on C2. Even with the unanticipated failings of the IGCT in this role, the reason for the failure of the switch this last time has to be attributed somewhat to human error. The failure of D3 at its rated voltage of 1000 VDC should have been anticipated, and the diode should have been replaced with a higher voltage diode. Had that occurred, the subsequent failure of IGCT B probably would not have occurred and the goal currents and voltages may have been reached.

2. 150 VDC to 200 VDC

After the failure of the second IGCT for switch B, further testing was necessarily halted while the manufacturer, ABB, was consulted. The ABB technical representatives agreed that large negative voltage transients exposed to the cathode likely led to the failures of both gate drivers, as they were only designed to hold off a reverse voltage of 17 VDC. The representatives accepted the two failed IGCT's for analysis and refurbishment and graciously lent NPS a high power thyristor more suited for the role of switch B. Once the thyristor was installed with the appropriate gate driver, snubber, and larger counterpulse capacitor (850 μF), testing was able to continue at higher voltages.

For safety's sake, the test program was re-initiated at V_{C1} = 25 VDC and V_{C2} = 100 VDC, and conducted in the same fashion as before, increasing V_{C1} in 25 V increments and V_{C2} in 100 V steps. Testing with the new counterpulse thyristor and counterpulse capacitor appeared almost identical to the testing done with the previous circuit configuration. The tests at new main capacitor bank voltages of 150 VDC, 175 VDC, and 200 VDC, were very similar to the traces shown at lower voltages, but one can see an increased amount of reverse current through I_S after $t_{opening}$, shown in Figure 21, with V_{C1} as yellow trace 1, I_L as green trace 2, I_R as purple trace 3, and I_S as red trace 4. The change in the relative heights of I_S and I_L is due to a 2X filter being placed in line with I_L, allowing it to be read on the oscilloscope.

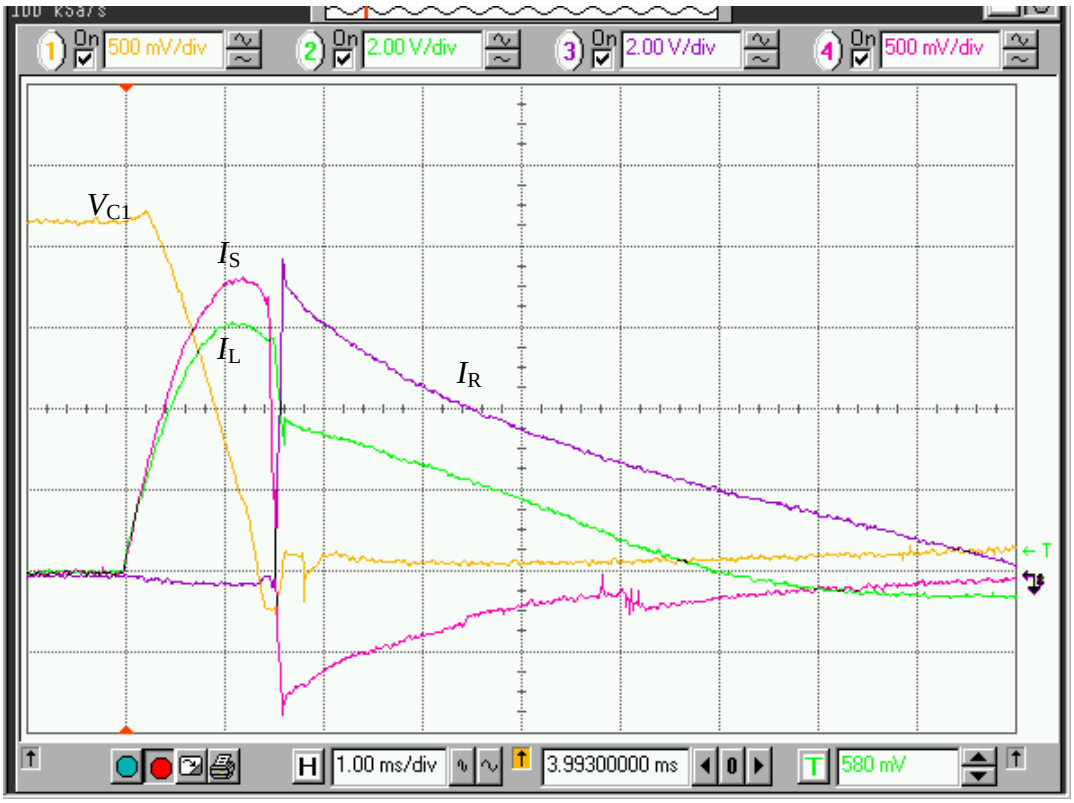

Figure 21. LVEC PFIN at V_{C1} = 200 VDC, After Change of B and C2

After reaching a measured current I_L of 24.6 kA, there was a third casualty to the system, causing the failure of switch A2's gate driver. The large amount of smoke and the fact that it emerged from the gate driver rather than the semiconductor puck of the IGCT seems to indicate that the delicate gate control circuitry was again responsible for the switch's failure. This event also indicates that diode D4 did not solve all the problems we were having with back EMF from L1. For tests to continue, either a new, more robust IGCT would have to be found, or some other method of blocking the large reverse voltage encountered by the cathode to gate path within the switches.

The last series of tests are reproduced in graph form in Figure 22, showing their correlation to both theoretical data and an ideal circuit with no resistance, i.e. with $\eta = 0$. In the plot, IL is the same as the inductor current I_L through L1, and IS is the switch group current I_S through A1, A2, and B..

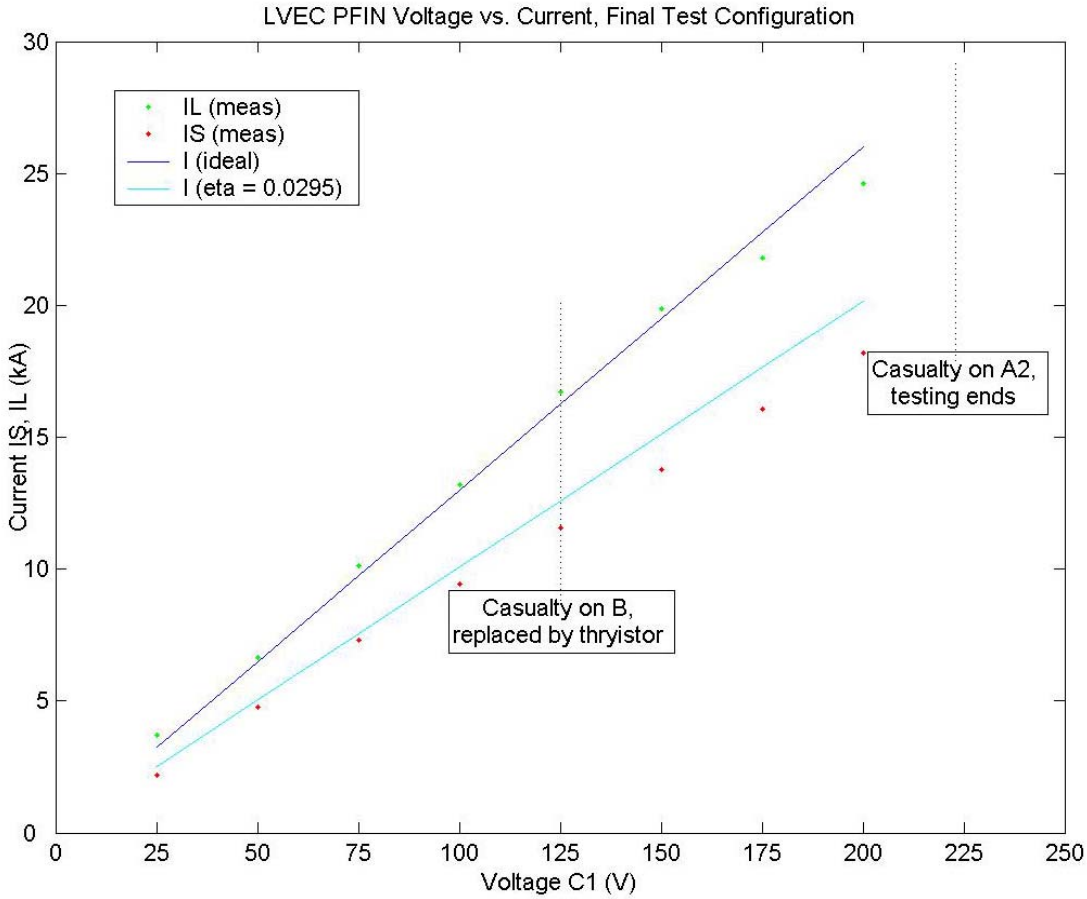

Figure 22. High Power Test Data

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V. EVALUATION AND CONCLUSIONS

Despite the switch failures that occurred, preventing the thesis from reaching its original goals, the LVEC PFIN was demonstrated successfully, allowing two paralleled semiconductor switches to shut off a measured current of 24.6 kA, well above their combined current shut-off rating. In addition, it was shown that a PFIN could supply high voltage and current pulses to a resistive-inductive load from an efficient low voltage source. In those terms, this project was successful and should be continued as a potentially viable alternative to the accepted electric weapon pulse power supplies.

Several issues with the design became apparent during research that will require further study, however. First, obviously, the choice of semiconductor switches must be reconsidered. The thyristor now installed as the counterpulse switch would appear to be perfect for its job, and though the IGCT's have performed well as main switches A1 and A2, the oversensitivity of their gate-cathode connection and of the gate driver itself must still be considered as a potential failure mode. If another turn-off switch can be found that has a more robust floating gate circuit and reverse voltage hold-off capability, it would be more desirable than this model of IGCT.

Also, the counterpulse circuit requires a large amount of energy in order to adequately damp the current through the main switches prior to opening or turning them off. Effective counterpulsing requires a substantially high voltage, capacitance, or some combination of the two, all of which leads to increased volume and mass which do not contribute to the final output of the PFIN. The needs of the circuit reached the point that we were using a standard high voltage capacitor (usually used to drive railguns) to provide the counterpulse, as it had the highest voltage rating of the capacitors available in the lab (though its capacitance and voltage were much higher than necessary to successfully counterpulse the LVEC PFIN, even at full power). The counterpulse capacitor will therefore require optimization as well.

Finally, this was a laboratory setup and was therefore not optimized for energy efficiency, size, or portability. The snubber circuit that we used across the IGCTs was not optimized and may have significantly degraded performance. The layout of

components and the choice of materials all would need to be rethought prior to moving to an operational system. The low voltage electrolytic capacitors had about the same energy density as the large high voltage capacitors, and when the size and weight of the counterpulse circuit and power inductor are added in, there seems to be no major benefit to using a LVEC PFIN rather than another pulse power supply. It is only when other low voltage storage media are considered that the PFIN concept truly shines and its importance to continued research becomes clear. With an appropriately sized high voltage counterpulse capacitor, and a main capacitor bank comprised of efficient ultracapacitors or supercapacitors with 10 to 100 times the energy density of available high voltage capacitors or low voltage electrolytic capacitors, and a design which emphasizes compactness and portability, then an electric weapon pulse power supply capable of servicing the Army or Navy railguns becomes feasible. The only impediment to this design is not the applicability of the PFIN concept, but the equivalent series resistance and availability of these special capacitors. Industry experts indicate that adequately low ESR's at the discussed energy densities should become commercially available in five to ten years. When that time has come, the concept of the PFIN proven here should finally be developed enough to incorporate them into a fielded weapon system.

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