ABSTRACT

BOLLAPRAGADA, RAJESH. An Integrated Tool for High Speed Circuit Design Including Substrate Effects. (Under the direction of Professor Dr. Michael B. Steer).

An integrated environment for layout-oriented design of high speed circuits is the main target of this study. The simulation environment would include a full-wave electromagnetic simulator and a circuit simulator(fREEDA, with a front engine), which is the major emphasis in this document. fREEDA implements local reference node instead of a global ground and this is crucial for distributed circuits. The models are implemented in object-oriented fashion and uses automatic differentiation. The same model can be used for DC, transient and harmonic balance analysis.

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An Integrated Tool for High Speed Circuit Design Including Substrate Effects

by

Rajesh Bollapragada

A thesis submitted to the Graduate Faculty of
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requirements for the Degree of
Master of Science

Electrical Engineering

Raleigh

2003

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I dedicate this to my parents

Biography

Rajesh Bollapragada was born April 2, 1980 in Chennai, TamilNadu, India. He received his elementary and secondary education in Chennai, India, graduating from Chinmaya Vidhyalaya . He received the Bachelor of Science degree with a major in Electronics and Communication Engineering from the University of Madras-Government College of Engineering, Salem in 2001. In August 2001 he was admitted to North Carolina State University to begin studying for the Master of Science in Computer Engineering. While pursuing the MS degree he held a Research Assistantship with the Electronics Research Laboratory in the department of Electrical and Computer Engineering. His interests include 3D CAD Layout tool development and Analog Circuit design for Wireless Applications.

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Contents

List of Figures **vii**

1 Introduction **1**
1.1 Motivation for and Objective of this Study 2
1.2 Thesis Overview 3

2 Literature Review **4**
2.1 Background 4
2.2 Modeling of Quasi-Optical System 5
2.3 Local Reference Terminal 7
2.4 Technology file 8

3 Java Philosophy **11**
3.1 Introduction 11
3.2 Event Delegation Model 13
3.3 Class Structure 13
3.4 Summary 14

4 Tool Flow **15**
4.1 Introduction 15
4.2 Local Reference 17
4.3 Tool Flow 19
4.3.1 Simulating High Speed Circuits 19
4.3.2 Schematic Capture Flow 22
4.4 EMPDK 24
4.4.1 Introduction 24
4.4.2 Creating a technology file 25
4.5 Electric 26
4.5.1 Introduction 26
4.5.2 Identifying the Local Reference 27

4.5.3 Creating Exports in a Schematic . . . 27
4.5.4 Schematic Capture . . . 30
4.6 Integrating Electric and EMPDK . . . 31
4.7 fREEDA . . . 31
4.7.1 Introduction. . . . 31
4.7.2 Simulating structures . . . 32

5 Case Study **34**
5.1 Quasi Grid Amplifier . . . 34
5.1.1 Introduction . . . 34
5.1.2 Unit Cell . . . 34
5.1.3 5x5 Grid . . . 35
5.2 Microwave Stub-filter . . . 36
5.2.1 Introduction . . . 36
5.2.2 Simulation Results . . . 37
5.2.3 Performance Measures . . . 42
5.3 Summary . . . 42

6 Conclusion **43**

7 Future Research **44**

8 Appendix **46**
8.1 **Appendix A** . . . 46
8.1.1 CIF file format . . . 46
8.2 **Appendix B** . . . 48
8.2.1 EMPDK User Guide . . . 48
8.2.2 Introduction . . . 48
8.2.3 Creating a new technology file . . . 48
8.2.4 Editing an existing technology file . . . 48
8.3 **Appendix C** . . . 50
8.3.1 Technology File Structure . . . 50

Bibliography **52**

List of Figures

2.1 Planar Grid System. 5
2.2 Unit cell with gate bias lines. 6
2.3 Equivalent circuit model. 6
2.4 A two port micro-strip line. 8
2.5 A sample process parameters. 9
2.6 Sample technology file. 10

3.1 Model-View-Controller architecture. 12

4.1 Typical Grid Amplifier System. 16
4.2 Division of system in fields and circuits. 16
4.3 Unit cell with port voltages and local reference terminals identified. . 17
4.4 Local Reference Groups shown on a 4x4 grid amplifier. 18
4.5 Block Diagram of Tool Flow. 19
4.6 Preparation of Layout for EM Simulation - Flowchart. 21
4.7 Schematic Extraction - Flowchart. 23
4.8 EMPDK v1.0 24
4.9 Sample technology file 25
4.10 Local Reference Terminal. 28
4.11 Creating Export. 29
4.12 Creating spice netlist. 30
4.13 Integrating Electric and EMPDK. 31
4.14 Simulation of distributed structures under fREEDA. 33

5.1 Unit Cell Dimensions. 35
5.2 Unit Cell S21. 36
5.3 Microwave stub filter. 37
5.4 Stub filter block. 38
5.5 Microwave Stubfilter extracted netlist. 39
5.6 S11 - Stub filter. 40

5.7 S21 - Stub filter. 41

8.1 Sample technology file 50

Chapter 1

Introduction

The IC market is characterized by an ever increasing level of integration complexity. Today complete systems that previously occupied one or more boards, are integrated on a few chips or even on one single multi–million transistor chip – a so called System– on– Chip (SoC).

Research interest is moving in the direction of system synthesis where an object–oriented system level specification is translated into a hardware–software co-architecture with high level specification for both the hardware, the software and the interfaces. In addition, reuse and platform based design methodologies are being developed to further reduce the design effort for complex systems.

Millimeter-wave circuits are becoming ever more commercially and militarily viable and, coupled with large scale production, design practices must evolve to be more sophisticated in order to handle more complex relationship between constituent elements. Also, as the frequency of radio frequency (RF) circuits extends beyond a gigahertz to tens and hundreds of gigahertz, wavelengths become large with respect to device and circuit dimension and the three-dimensional EM environment becomes more significant.

Microwave and millimeter-wave systems have generally been developed from a circuit perspective with the effect of the electromagnetic (EM) environment modelled

using lumped elements or N-port scattering parameters. The recent development of the local reference terminal concept coupled with steady-state and transient analysis using state variables allows the incorporation of unrestrained EM modelling of microwave structures in a circuit simulator. A strategy implementing global modelling of electrically large microwave systems using the circuit abstraction is presented.

1.1 Motivation for and Objective of this Study

One fundamental issue that arises in modelling electrically large systems in a circuit representation is the assignment of system ground. Currently, circuit simulators use a nodal approach in which voltages are assigned to terminals and each of these voltages is referred to a common reference point, which is commonly called 'ground'. In a spatially distributed system, a common reference point cannot always be defined as the (electrically significant) spatial separation of a node and its reference point cannot be tolerated. If the separation is an appreciable fraction of a wavelength, it is not possible to uniquely define voltage.

Transmission line effects frequently lead to problems like overshoot, undershoot and ringing. Board interconnects limit performance by introducing delay into the timing path. Crosstalk and EMI are beginning to present formidable problems in what traditionally have been considered acceptable board designs.

EM models, relying on the global reference terminal concept cannot accurately treat large multi-port structures. This thesis presents a tool flow for model development based on a new concept of local reference nodes (LRN's). The LRN concept enables the conversion of a port – based model to a terminal- based model, which can be used in a general purpose circuit simulator after modifications to the way the nodal admittance matrix is treated.

There is a lot of research being carried out for the simulation of quasi-optical grid amplifier structures. A Method of Moment simulator was created by Nuteson [9] which generates a multi-port impedance model of the passive section of a grid structure. Summers [8] describes a tool flow for linking the passive structures and

the active devices in a non-linear circuit solver. Since the system consists of spatially distributed components, we need a system which can identify the local reference terminals.

This thesis will outline the creation of a tool set with the capability to simulate spatial power combining systems. This thesis documents the development of a tool flow for integrated steady state nonlinear circuit analysis and electromagnetic analysis of a quasi-optical grid amplifier system. The analysis incorporates surface modes, nonuniform excitation, and full nonlinear effects. The work is verified using measurement of a 5x5 grid amplifier.

1.2 Thesis Overview

This thesis describes the integration of a circuit and field simulator, which will ultimately be used to simulate a grid amplifier.

Chapter 2 is a review of literature relevant to the grid amplifier systems. The review includes modeling of quasi-optical arrays, local reference terminal concept for simulating spatially distributed circuits and the need for a technology file to describe the process in a multilayered system.

Chapter 3 is an overview of the Java philosophy and explains the programming interface.

Chapter 3 is an overview of the program flow required to complete the simulation. The overview includes a discussion about each program used and a detailed description of the interfaces between the programs are presented.

Chapter 4 is a case study on modeling a grid amplifier. A detailed description of the model development process as well as results from the completed model are presented

Chapter 5 presents conclusions derived from this project and areas that need further exploration in the future.

Chapter 2

Literature Review

2.1 Background

Quasi-optical power combining techniques are a means of combing the power output of numerous solid state devices generally in a free space environment. In [6] a review of the various techniques and systems is presented. Mink [3] conducted a theoretical investigation of an array of filamentary current sources radiating into a plano-concave open resonator. Mink [3] discuses the possibility of obtaining high combining efficiency for systems several wavelengths in dimension. The field was further advanced by the construction of a grid oscillator [4] and grid amplifier [5]. A diagram of the general system is shown in Fig.2.1 The systems represented a proof of concept.

The number of spatial power combining systems has increased greatly over the years, but the design of the systems has largely been empirical or through the use of simplified models. The task of characterizing the structures has proved to be difficult because the systems are usually several wavelengths in dimension. Some significant work has been done in the area of planar grid structures. Early models assumed the grid was infinitely large, but recent developments [9], have removed this assumption

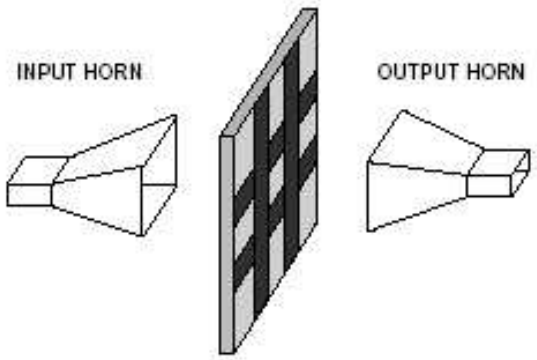


Figure 2.1: Planar Grid System.

from the model. The literature review discusses modeling techniques for quasi-optical grid amplifiers and oscillators.

The power combining system is a way of efficiently coupling the energy via free space instead of using transmission lines. If you use transmission lines, there is an inherent upper limit on the number of elements that can be combined. It finds application in X-band (8 Ghz) and Ka - band (34Ghz) combiners.

2.2 Modeling of Quasi-Optical System

The grid oscillator presented in [4] was one of the early demonstrations of quasi-optical power combining. The system was designed using a unit cell model that is presented in [9]. In [5] Kim presents a grid amplifier.The equivalent circuit and unit cell layout are shown in Fig.2.2 and Fig. 2.3.

In [9] the unit cell model was extended to improve its performance. The surface current distribution was approximated using the method of moments technique and the EMF method was used to calculate the impedance of the grid leads. The substrates and free space regions in the systems are represented by transmission lines. The polarizers are modeled by reactive elements.

Research at North Carolina State University led to the development of a Method

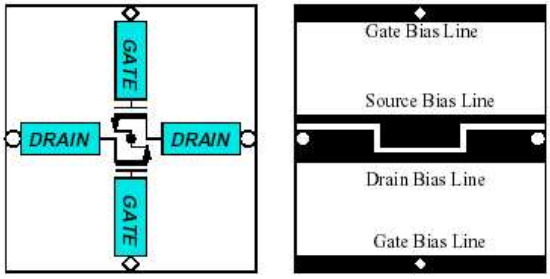


Figure 2.2: Unit cell with gate bias lines.

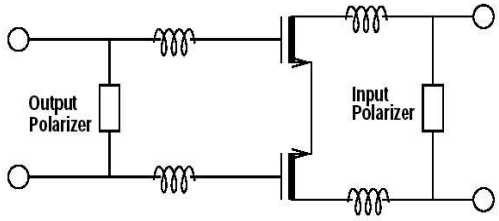


Figure 2.3: Equivalent circuit model.

of Moments simulator [9] which no longer relied on the unit cell approximation in characterizing planar grid structures. The significance of this work is that surface waves, nonuniform excitation, and gain and phase variations of the unit amplifiers can be considered. Finite grids can now be rigorously specified, with the effects of mutual coupling between cells and variations in magnitude and phase of the feed sources included. The simulator also included the effects of quasi-optical components far away from the grid, such as lenses. The simulator computed an impedance matrix for the grid structure, which can be used in a microwave circuit simulator. An implementation is presented in [10]. The gain of an amplifier grid and an analysis of frequency and phase synchronization in oscillator arrays are presented.

2.3 Local Reference Terminal

Circuit theory has evolved to include a common reference terminal to which all voltages in a circuit are referred. However, it is generally not feasible to define voltages or a single reference point in a spatially distributed system. In [1] , Steer describes a framework to simulate distributed strucutres. Microstrip networks are examples of distributed structures for which reasonable approximations have been made so that they can be treated as elements in conventional circuit simulators. A micro-strip transmission-line segment is shown in Fig. 2.2 with the conventionally accepted definition shown for the node voltages at the ends of the line. In the common approach, the voltages V_1 and V_2 are determined as the integral of the electric field from the strip to the ground plane using the shortest path - defined with vertical arrows. However, an absurd 'value' for V_2 would be obtained if the integral were to be performed along the dashed line. Thus, the common approach treats the ground plane itself as a global reference point even though this implies and requires that charges can instantaneously redistributed on the ground plane. While this has proven to be a successful modelling approach for microwave microstrip circuits that are generally arranged as cascaded stages, limitations are becoming evident in the modelling of strip-like distribution networks in high speed digital systems.

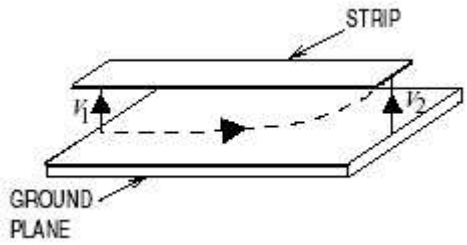


Figure 2.4: A two port micro-strip line.

2.4 Technology file

In multi-layered structures, we need to define the layers that are used in the system. The technology file contains process specific parameters such as layer thicknesses and the sheet resistance of the various layers. In addition to this it also provides the mesher tool with information regarding the ordering of layers. A generic CMOS process is shown in Figure 2.5. In Figure 2.6 a sample technology file for the given process is shown.

In conventional layout tools, the technology file contains information pertaining to lambda–based design rules. They do not store the material properties (dielectric constant), (loss tangent), (sheet resistivity), (conductivity), which are essential in characterizing multi-layered structures. The main advantage to having this information external is that, we can change our process parameters without having to redo our layout.

In addition to this, the information pertaining to the order of layers is also embedded in the file. This helps us render a two-dimensional layout to a three-dimensional layout.

The output of the program is a text file, which is human readable. The information available in the file can be parsed to generate inputs for other layout tools like Cadence, LinkCad, L-Edit etc.

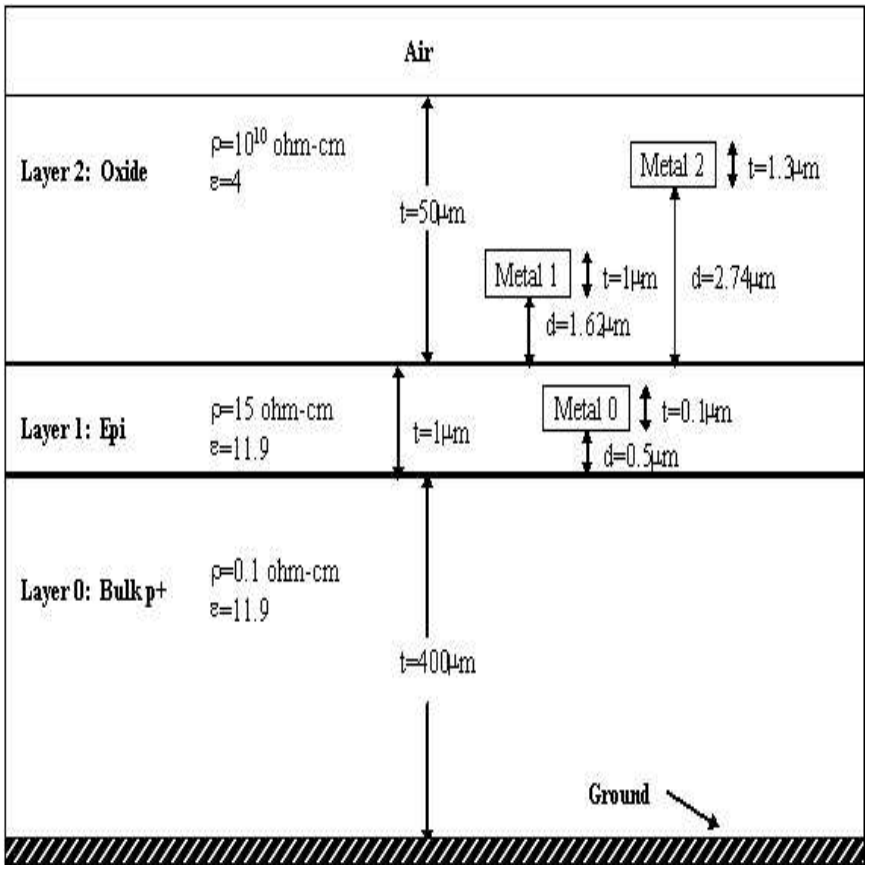


Figure 2.5: A sample process parameters.

```
// TECHNOLOGY FILE

// METAL LAYERS : 2
// DIELECTRIC LAYERS: 1

technology cmos
  UNITS microns
  metal
     //name        zmin   thickness  resistivity(ohms.cm)  desc
     layer 0        0.00   0.35       0.2                  // G substrate
     layer 1     0.7  0.2          1.56E-4                 // M
   endmetal

   dielectric
     //name        zmin   thickness  dielectric constant
     layer 2     0.35       0.35       3.9
   enddielectric
endtechnology
```

Figure 2.6: Sample technology file.

Chapter 3

Java Philosophy

3.1 Introduction

Java is a system-independent object oriented programming language. The program architecture is based on the MVC (Model–View –Controller architecture). The goal of the MVC design pattern shown in Figure 3.1 is to separate the application object (model) from the way it is represented to the user (view) from the way in which the user controls it (controller).

The model object knows about all the data that need to be displayed. It also knows about all the operations that can be applied to transform that object. However, it knows nothing whatever about the GUI, the manner in which the data are to be displayed, nor the GUI actions that are used to manipulate the data. The data are accessed and manipulated through methods that are independent of the GUI. A simple example of a model would be a clock object. It has intrinsic behaviour whereby it keeps track of time by updating an internal record of the time ever second. The object would provide methods which allow view objects to query the current time. It would also provide methods to allow a controller object to set the current time.

The view object refers to the model. It uses the query methods of the model to

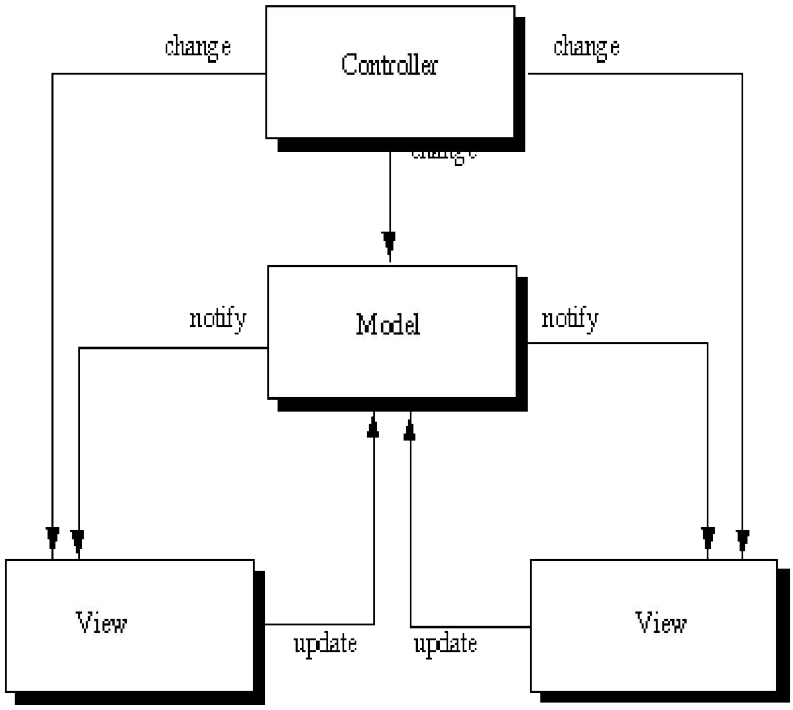


Figure 3.1: Model-View-Controller architecture.

obtain data from the model and then displays the information. The display can take any form, in the clock example, one view object could display the time as an analogue clock, another could show it as a digital clock. The different displays would have no bearing whatsoever on the intrinsic behavior of the clock.

The controller object knows about the physical means by which users manipulate data within the model. In a GUI for example, the controller object would receive mouse clicks or keyboard input which it would translate into the manipulator method which the model understands. For example, the clock could be reset directly by typing the current time into the digital clock display. The controller object associated with the view would know that a new time had been entered and would call the relevant 'SetTime' method for the model object.

3.2 Event Delegation Model

The delegation event model supports a clean separation between the core program and its use interface. The delegation pattern allows robust event handling that is less error prone due to strong compile- time checking.

The delegation model consists of three separate objects to deal with event handling: event sources, events, and listeners. Event sources are any of the user interface components such as buttons, text fields. Event sources generate and fire events, and the events propagate until they are finally attended to by their listeners.

3.3 Class Structure

Model Class The model class is CIF file parser and the Technology file generator.

View Class The view class is composed of the different panels (ex. metalPanel, dielectricPanel, viaPanel, mainMenu)

Controller Class The controller class is embedded in the view class. Each individual component has its own listener and adapter class.

3.4 Summary

We have chosen Java as the programming language as it simplifies the programming effort by providing a single file which can run on different platforms. Since Java is based on the event-delegation model, this allows us to separately handle the events generated by individual objects in the program.

Chapter 4

Tool Flow

4.1 Introduction

Figure 4.1 is a typical spatial power combining system. The system contains horns for input and output and components which are spread over several wavelengths. The active surface contains numerous nonlinear devices connected to input and output radiators.

The system presents some very challenging problems: components are spatially distributed, power is radiated through the system, and nonlinear devices are present in the system. The first two problems dictate that electromagnetic models be used, however the nonlinear devices are naturally handled in a circuit simulator. The solution is to divide the two problems up as shown in Figure 4.2 .

The spatially distributed elements are handled through electromagnetic simulation, and the nonlinear devices are handled by common circuit simulation techniques. The interfaces between the two worlds must be clearly defined. The circuit simulator requires the impedance network seen by the active devices. The simulator also requires any excitation currents or voltages generated by input fields. The excitation should be normalized to limit the amount of electromagnetic simulations required.

The electromagnetic simulator will require the voltages at the ports of the active devices to calculate the current distribution and radiated fields.

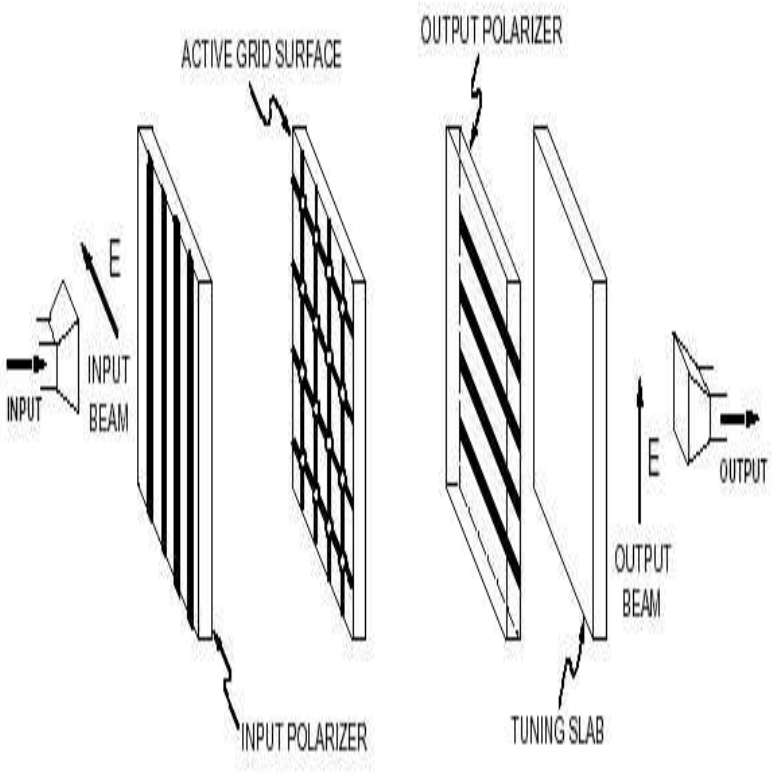


Figure 4.1: Typical Grid Amplifier System.

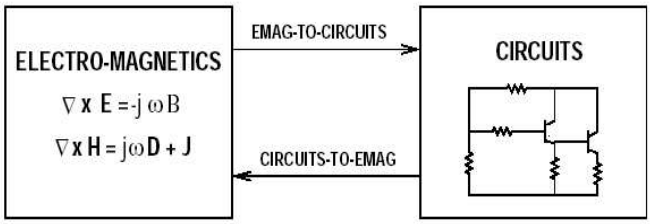


Figure 4.2: Division of system in fields and circuits.

4.2 Local Reference

Once the division of the system is done, we need to identify the local reference terminals and the local reference groups. The port–based admittance matrix is nodal in nature as illustrated in Figure 4.3. The local reference terminals are marked as there is no global ground. The implementation of the local reference terminal is discussed in more detail in [2].

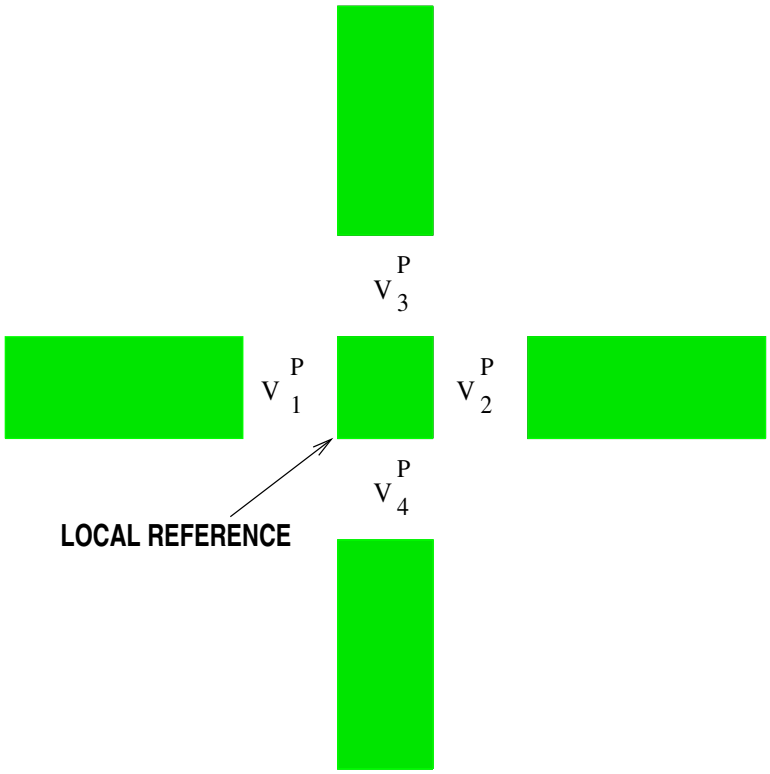


Figure 4.3: Unit cell with port voltages and local reference terminals identified.

In our simulation we assume each unit cell with the active device to form the local reference group as shown in Figure 4.4.

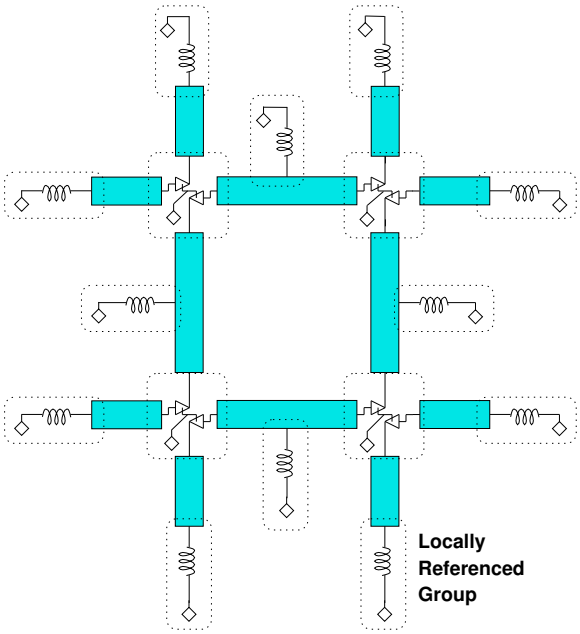


Figure 4.4: Local Reference Groups shown on a 4x4 grid amplifier.

4.3 Tool Flow

Figure 4.5 shows the complete block diagram of the simulation environment which is capable of handling the distributed effects in high speed circuits. Off the shelf tools were taken and modified to capture the distributed effects. The main contribution to the tool flow was adding support to capture the geometrical and electrical properties of a layout and handling the interface between the programs.

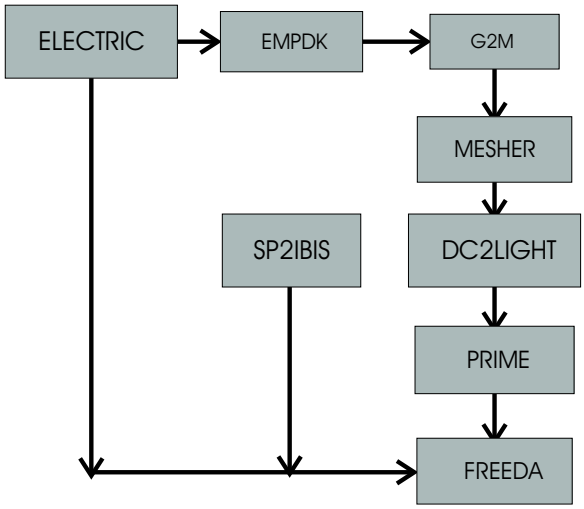


Figure 4.5: Block Diagram of Tool Flow.

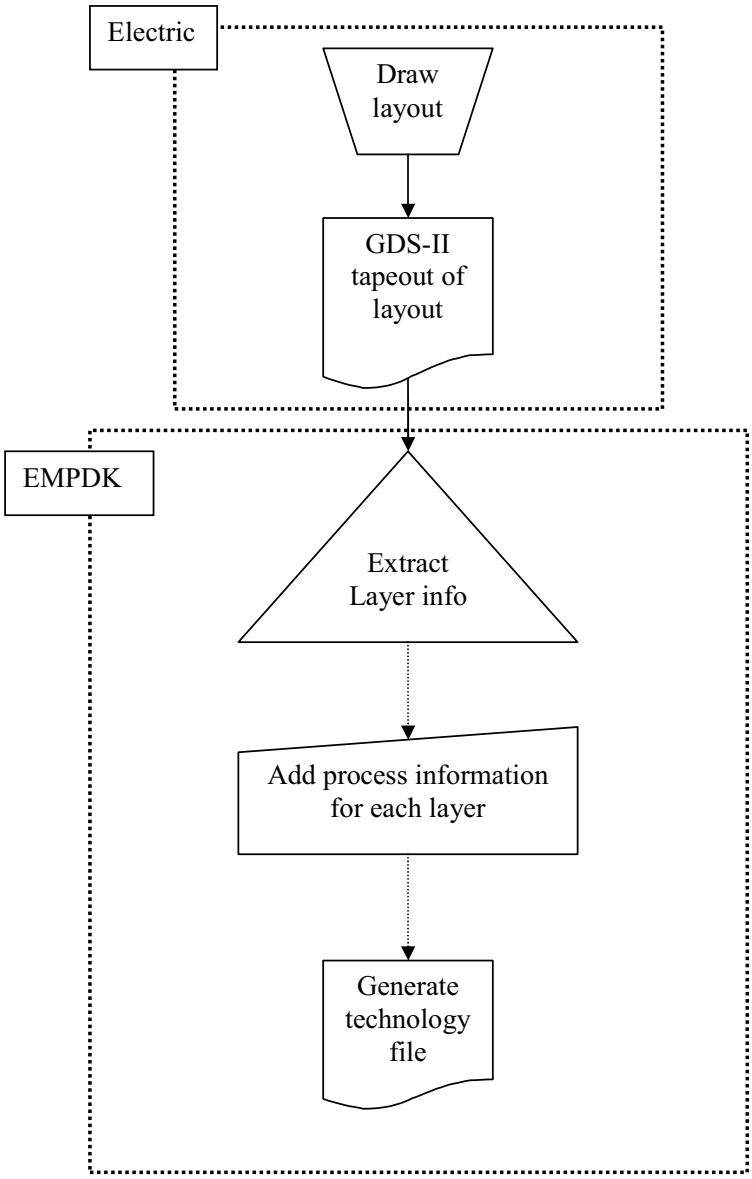
4.3.1 Simulating High Speed Circuits

Figure 4.6 shows the steps involved in preparing a generic layout for EM simulation. The system under observation is drawn using Electric. The geometrical information is automatically taped out as a GDS-II file. The additional information included in the GDS-II file is the local reference terminals that are manually identified by the user.

The primary input to EMPDK is the circuit layout description in CIF or GDS-II format. This file is parsed and the user is presented with the layers in the drawing. The user can then manually select the layers of interest and provide the electrical

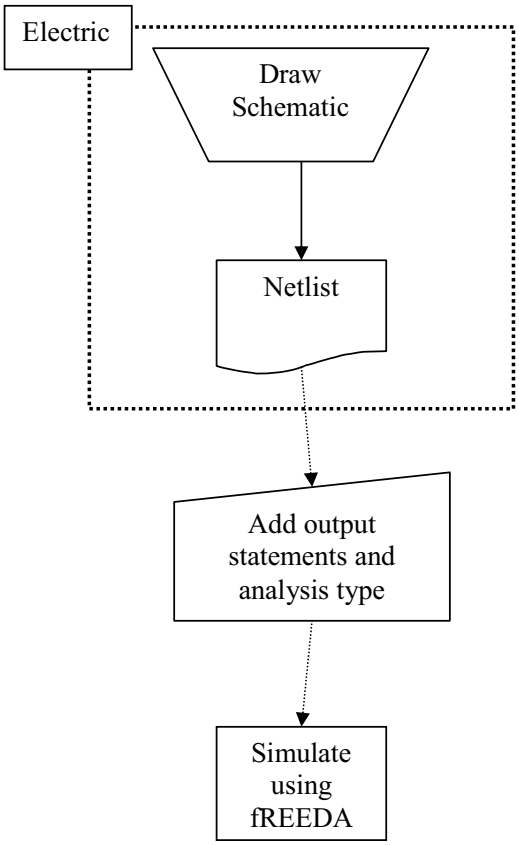
parameters required for EM - simulation. This stage prepares the layout file for EM - simulation.

The output files generated by Electric and EMPDK completely describe a distributed structure. This information is then fed to the field solver which provides us with the port-based parameters. The port-based parameters characterize the distribute structure and this information is used to simulate circuits with active devices.


Electric
Draw layout
GDS-II tapeout of layout
EMPDK
Extract Layer info
Add process information for each layer
Generate technology file

4.3.2 Schematic Capture Flow

The tool flow presented in Figure 4.5 can also be used to study simple circuits with microwave elements directly from their schematic. fREEDA has a good set of microwave elements. But it is a circuit netlist interpreter. To make the simulation environment more user friendly, we need a graphical user interface. This allows the user to draw the schematic and automatically generate the netlist for simulation. At this stage, the user has to manually enter the output statements and the analysis type required in the simulation. The flow is explained in Figure 4.7.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Netlist
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4.4 EMPDK

4.4.1 Introduction

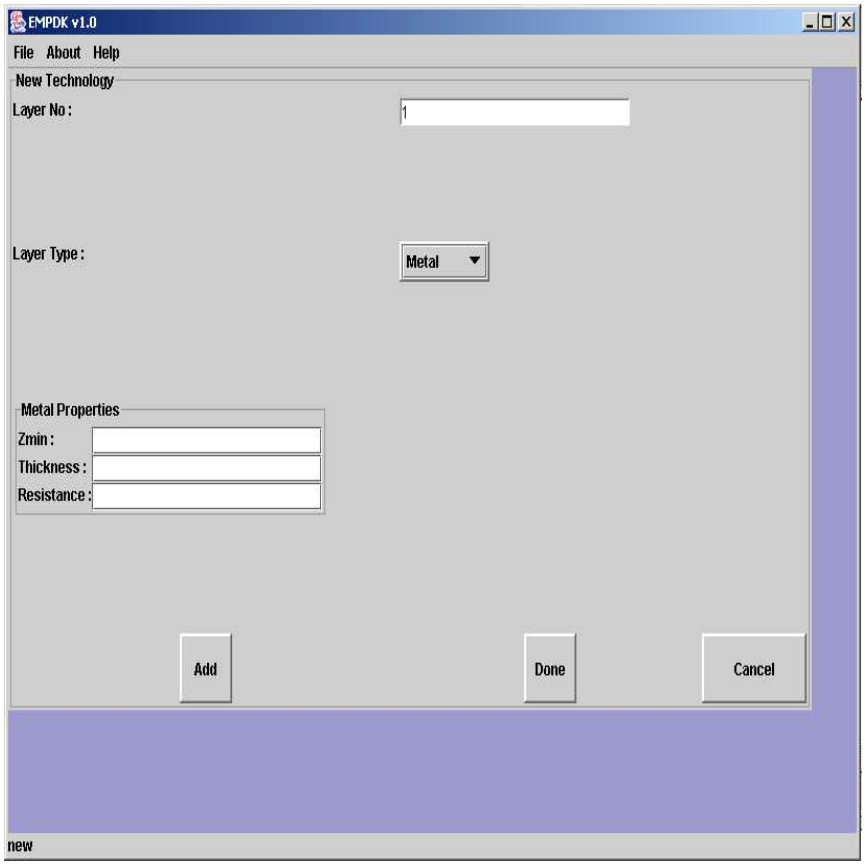

Figure 4.8: EMPDK v1.0

EM-Physical Design Kit is a Java program which takes generic GDS-II or CIF file as its input and produces an output CIF file and an associated technology file. This progam was developed as part of the work for this thesis. It provides an interface between the layout tool and full-wave electromagetics simulator.

The technology file gives us information regarding

- the material properties of the layers in the process

- the ordering of the layers, which helps us render the layout to a three–dimensional view.
- provides thickness information of each layer.

The geometrical information of the on-chip placement is obtained from the CIF file. The technology file gives the mapping between the different layers in the CIF file and the generic layers that any layout tool can interpret. The output of EMPDK is a human readable text file.

4.4.2 Creating a technology file

```
// TECHNOLOGY FILE

// METAL LAYERS : 2
// DIELECTRIC LAYERS: 1

technology cmos
  UNITS microns
  metal
     //name       zmin   thickness  resistivity(ohms.cm)  desc
     layer 0       0.00   0.35       0.2                 // G substrate
     layer 1     0.7  0.2          1.56E-4               // M
   endmetal

   dielectric
     //name       zmin   thickness  dielectric constant
     layer 2     0.35      0.35       3.9
   enddielectric
endtechnology
```

Figure 4.9: Sample technology file

A sample technology file is shown is Fig 4.9.The 'layer' statements define the various dielectric and substrate layers. A conducting substrate layer is specified by

stating its resistivity in ohm-cm. A dielectric layer can be modeled as an equivalent resistivity according to the dielectric loss tangent. The thickness is specified in microns. The relative permitivity is unitless. Notice that the substrate layers are defined from bottom up. In other words, the order is important. Thus the bulk layer is listed first, followed by the epi, and finally followed by the oxide layer.

The conducting metal layers are defined in the 'metal' sections. Each metal layer belongs to a specific layer specified with the layer identification. Most metal layers will be defined in non-conducting oxide layers. The sheet resistance of the metal layers is specified in milli-Ohms/Square along with the metal thickness. The z-coordinate of the bottom of the metal layer is specified under zmin where zmin is the distance in microns from the bottom of the substrate layer to the bottom of the metal layer.

You can also define optional vias to make connections from metal layer to metal layer. Note that vias are totally optional and usually play a minor role in determining the characteristics of a device. On the other hand, one can create multi-layer devices, or symmetric center-tapped inductors, with many via connections in series with the device. In these situations the inclusion of vias is necessary. Via layers are added in the 'via' sections. The top and bottom sections define the metal connectivity of the via. Note that the numbers correspond to the numbers used in the 'metal' sections.

4.5 Electric

4.5.1 Introduction

The Electric VLSI Design System is a highly flexible and powerful system that can handle many different types of circuit design (MOS, Bipolar, schematics, printed circuitry, hardware description languages, etc.) It handles geometry at any angle (not just Manhattan) and can even handle curves.

Layout is done by placing and wiring electrical components. Although this is standard practice for schematics, it is unusual for chip layout. However, because of this style of design, Electric understands chip layout at a more sophisticated level, and

can aid in design to an unprecedented degree. Electric maintains circuit information based on connectivity. This feature was made us to incorporate the idea of local reference terminal in Electric.

Electric has many analysis tools, including design-rule checking, simulation, and network comparison. Electric has many synthesis tools, including routing, compaction, silicon compilation, PLA generation, and compensation,

The user interface is quite sophisticated and runs on all popular workstations (Windows, Macintosh, and UNIX). It also provides interpretive languages (Lisp, TCL, and Java) for advanced users.

The most interesting feature of the system is its global enforcement of connectivity which provides top-down design capability and ease of post-design modifications. The features provided by Electric is described in the progammers reference manual [7].

In the next few sections we will see how a layout is prepared for either EM simulation or in general the process for going from layout to circuit netlist simulation.

4.5.2 Identifying the Local Reference

A facet as shown in Figure 4.10 can represents a local reference group or a system of local reference groups. Electric is based on the connectivity approach, it stores terminal information for the given schematic. This information is used to identify the reference terminals on a facet.

The tool was modified to automatically identify the local reference terminal. This information is available to the user as a extension to the CIF file of the layout.

4.5.3 Creating Exports in a Schematic

The user can explicitly name the exports or terminals on a facet. This gives the user the advantage to identify local reference terminals in a system of local reference groups. This allows the naming of nodes at points of connection between schematic and layout as shown in Figure 4.11.

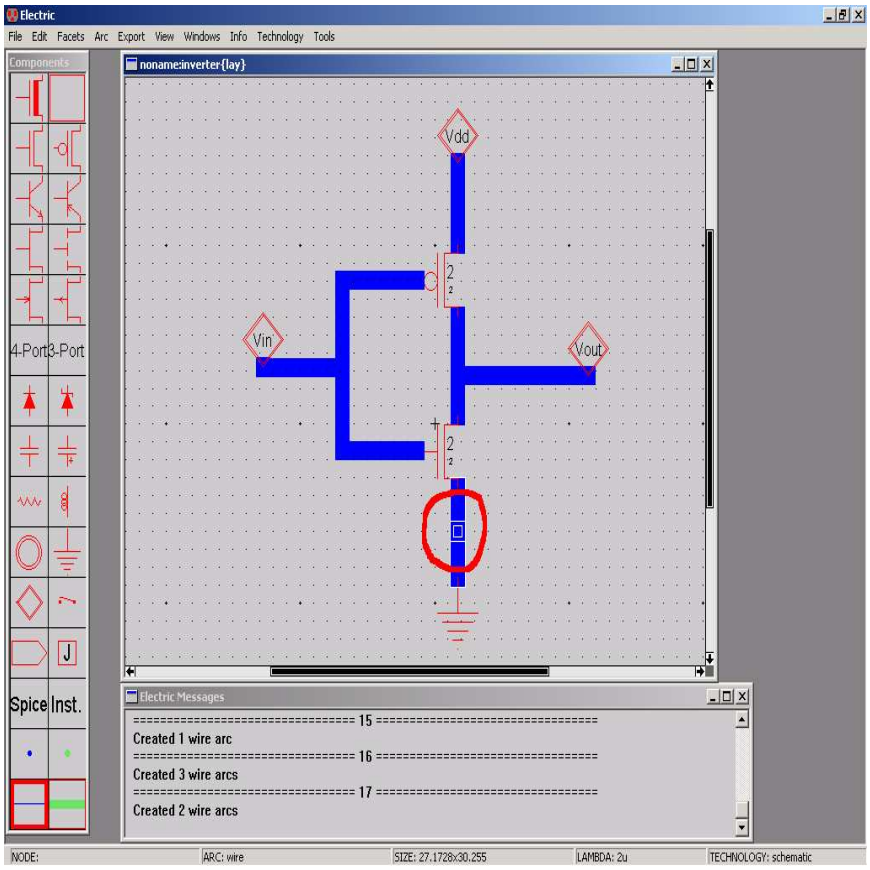

Figure 4.10: Local Reference Terminal.

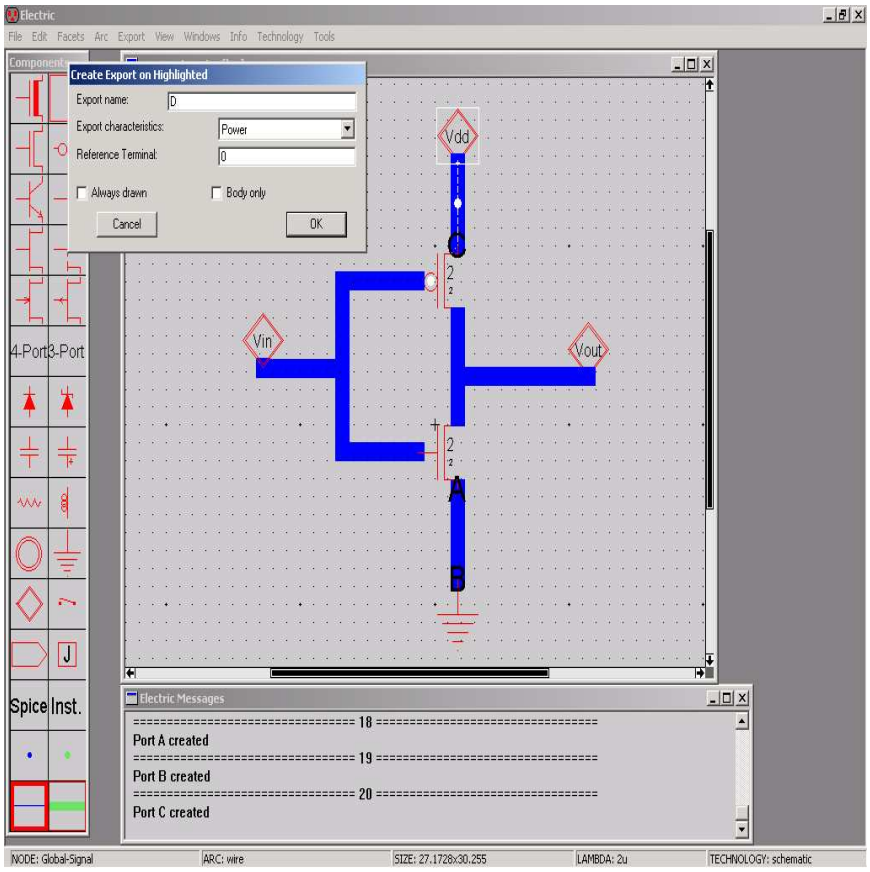

Figure 4.11: Creating Export.

With the facility to name ports, the user can mark the internal and external ports required for EM simulation within the layout tool itself.

4.5.4 Schematic Capture

Up to this stage, we have represented the circuit description of the power combining system and identified the local reference terminals on the circuit. Based on this data, we can generate a netlist describing the electrical circuit as shown in Figure 4.12.

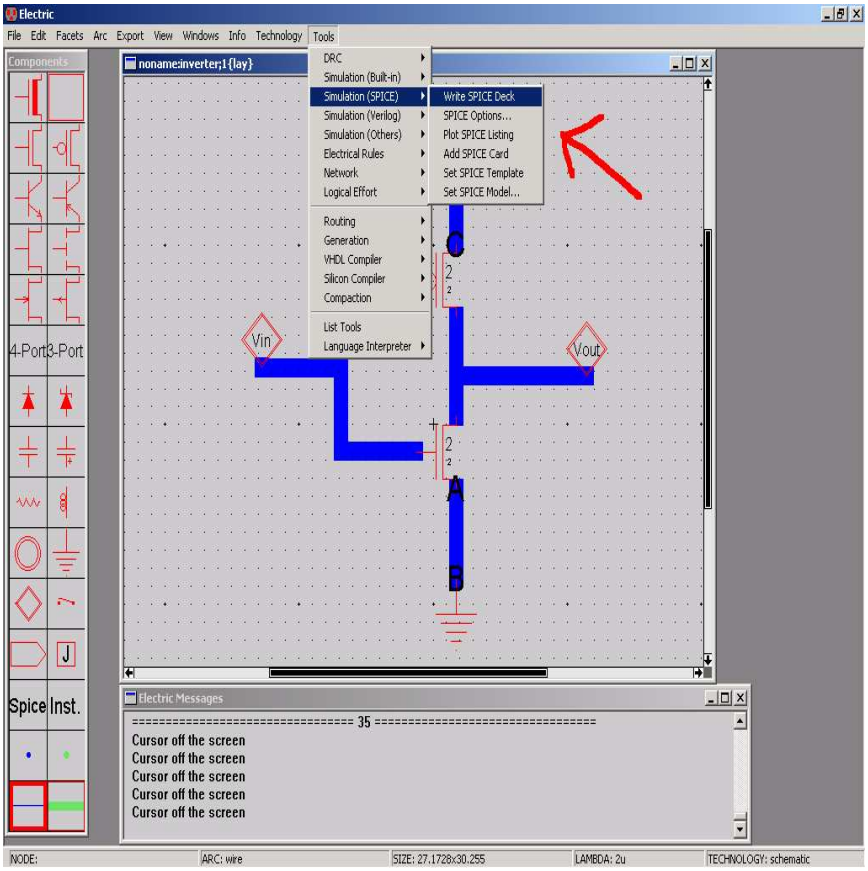

Figure 4.12: Creating spice netlist.

4.6 Integrating Electric and EMPDK

In addition to the netlist we also output two files, which make the system an EM-Aware system. These files describe the geometry of the distributed structures in the layout and also provide process parameters of the layers used to layout the circuit.

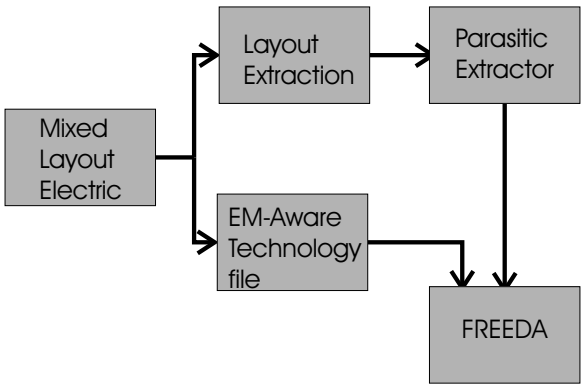

Figure 4.13: Integrating Electric and EMPDK.

The integration of Electric and EMPDK is shown in Figure 4.13.The above information is given as input to fREEDA to extract the port voltages in the circuit.

4.7 fREEDA

4.7.1 Introduction.

fREEDA(TM) is a multi-physics circuit simulator under development by a user community from universities, communities and laboratories.

It uses state variables, local reference group concepts, automatic differentiation and hence captures multo-physics and makes model development straightforward.

The simulation approach realizes the first new approach since SPICE-like analyses were developed. The approach allows the modeling of virtually any physical model and the generic model evaluation mechanism, in which the primitive model equations are wrapped in analysis specific generic functions, reduces the time required not only for computation but also development.

fREEDA(TM) implements several types of analyses, all of them state variable based, including a DC analysis, time marching transient analysis (different integration methods available), harmonic balance analysis and a unique wavelet transient analysis.

It also implements various linear devices from resistors to Foster's canonical port representation and non-linear devices from diodes to three and four terminal transistors.

4.7.2 Simulating structures

. Up to this stage, we have complete description of the layout under inspection. To complete the suite, we required the netlist to be in a format that could be read into fREEDA. Since Electric provides us with a SPICE netlist, we had to develop a script to automate the process of conversion. The netlist description is given as input to fREEDA, to generate the port voltages.The simulation process is shown in Figure 4.14.

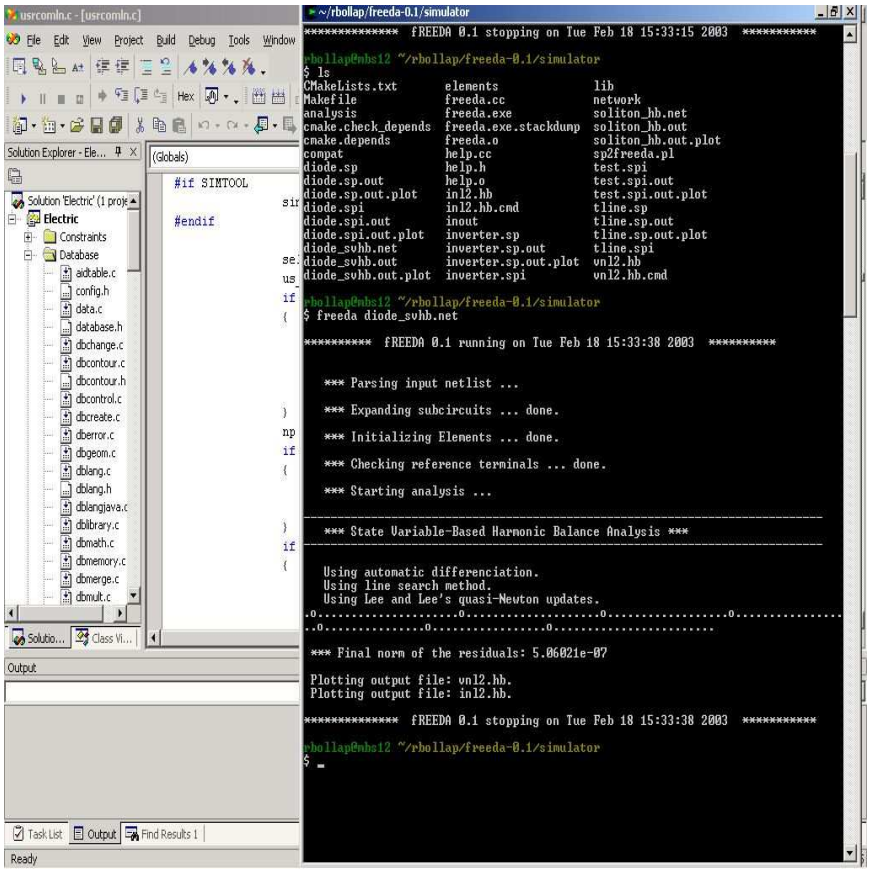

Figure 4.14: Simulation of distributed structures under fREEDA.

Chapter 5

Case Study

5.1 Quasi Grid Amplifier

5.1.1 Introduction

The earlier chapters described the approach towards an integrated design environment for design of spatial power combining systems. In this chapter various results are presented. The achievement is that the same results are obtained with the current design environment compared to previous results in [10].

In this section various size grids are analyzed and the intermediate CIF data is compared with that in [10]. The principle achievement is that the CIF output generated automatically by this work is exactly same to that handgenerated by user in [10]. This indicates that the CIF output precisely captures the geometry.

5.1.2 Unit Cell

The CIF output provided in [Appendix A] is for a unit cell shown in Fig. 5.1. Its magnitude and phase are plotted versus frequency in Fig. 5.2. The solid line shows

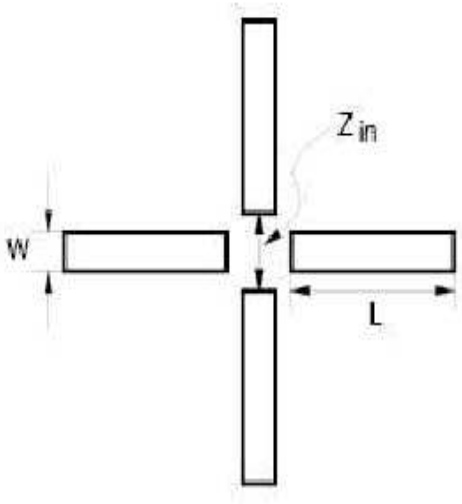

Figure 5.1: Unit Cell Dimensions.

results obtained by simulation and the dashed line is for the measurements taken. In Fig. 5.1 , the geometry for a unit cell of dimension 93.8 mm x 93.8 mm with a gap spacing of 9.8 mm and a line width of 6.35 mm is shown.

5.1.3 5x5 Grid

The data (CIF) generated for this grid was compared and found to match with the data in [10]. In [10], the design and simulation were performed for the 5x5 grid array placed in the lens system at z = 0 on a dielectric substrate with er = 2.56 and thickness 9.5 mm. It may be noted that the significant improvement over [10] is the ability to automatically generate CIF information with local reference nodes.

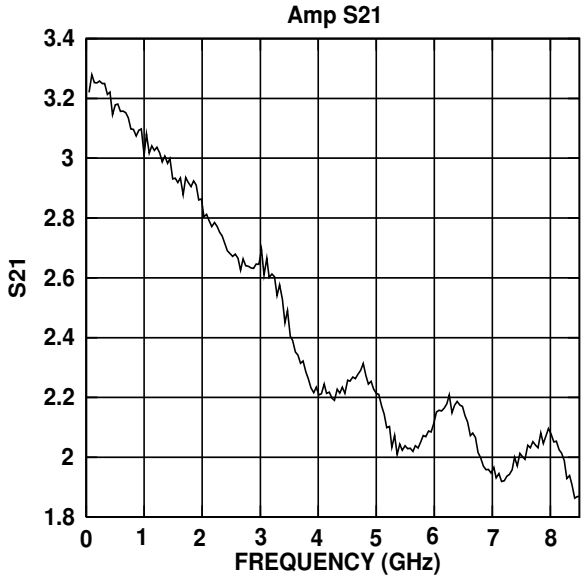

Figure 5.2: Unit Cell S21.

5.2 Microwave Stub-filter

5.2.1 Introduction

Figure 5.2 is a microwave stub filter. A microwave filter is a two port network used to control the frequency response at a certain point in a microwave system by providing transmission at frequencies within the passband of the filter and attenuation in the stopband of the filter. Typical frequency response include low-pass, high-pass, band-pass and band-reject characteristics. Applications can be found in virtually any type of microwave communication, radar, or test and measurement system.

There are two methods to design microwave filters as described by Pozar [12]. One is the image parameter method, which consist of a cascade of simpler two-port filter sections to provide the desired cutoff frequencies and attenuation characteristics, but do no allow the specification of a frequency response over the complete operating range. The second is the insertion loss method, which uses network synthesis techniques to design filters with a completely specified frequency response.

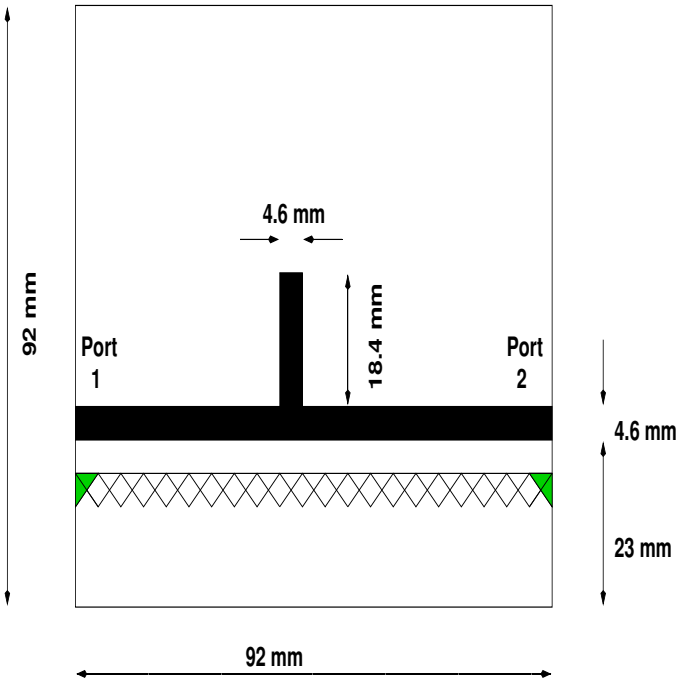

Figure 5.3: Microwave stub filter.

Both these methods provide lumped element circuits. For microwave applications, such designs usually must be modified to use distributed elements consisting of transmission line sections. The Richard's transformation and the Kuroda identities provide this step.

Figure 5.3 describes the process or the layers that makeup the stub filter.

5.2.2 Simulation Results

In this particular case–study, we were able to successfully identify distributed structures in a layout as opposed to considering then as simple wires. The individual components in the netlist we correctly identified. The user had to manually enter the analysis type required. Figure 5.4 shows the extracted netlist of the microwave stubfilter under inspection.

The extracted netlist were checked for errors and simulated using fREEDA. The

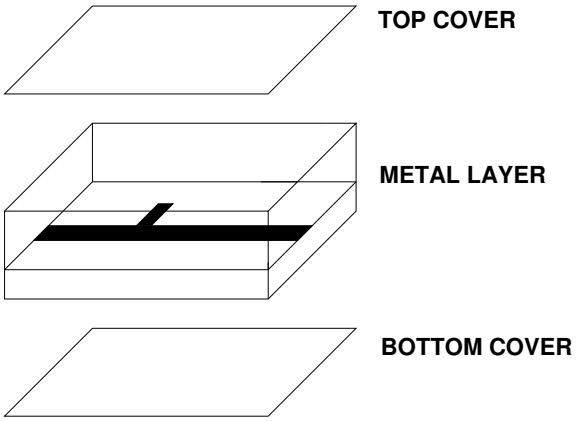

Figure 5.4: Stub filter block.

waveforms show the return loss and the insertion loss of the filter.

```
*transim netlist

vsource:v1 1 0 vac = 1
.ref 5

tlinp4:t1  21 0 2 0
+ z0mag=75.00 length=5e-3 k=7 tand=.01 fscale=1.e10
alpha=1.
+ nsect = 20 fopt=35e9

tlinp4:t2  2 3 4 5
+ z0mag=38.53 length=18e-3 k=7 tand=.01 fscale=1.e10
alpha=1.
+ nsect = 20 fopt=35e9

tlinp4:t3  3 0 6 0
+ z0mag=75.00 length=10e-3 k=7 tand=.01 fscale=1.e10
alpha=1.
+ nsect = 20 fopt=35e9

res:rl 6 32 r=75
vsource:v2 32 0
res:r2 1 21 r=75
res:ropen 4 5 r=10K


.ac start = 4.5e9 stop = 8e9 n_freqs = 100

.out plot element "vsource:v2" 0 if mag db in "atten.out"
.out plot element "vsource:v1" 0 if in "input.out"
.end
```

Figure 5.5: Microwave Stubfilter extracted netlist.

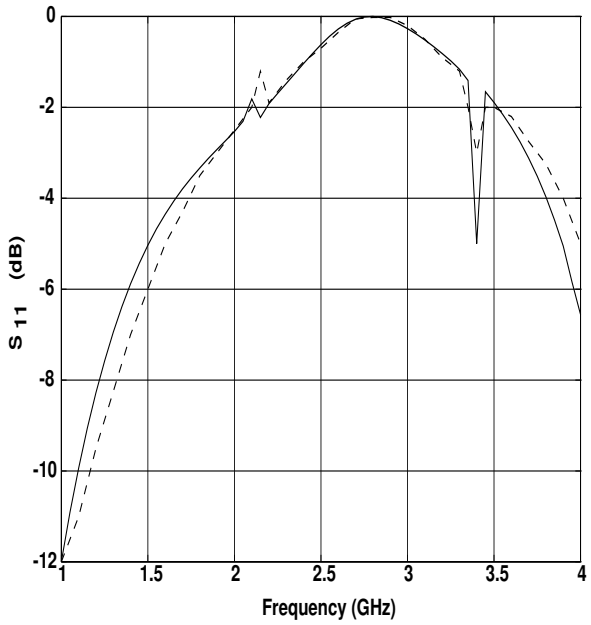

Figure 5.6: S11 - Stub filter.

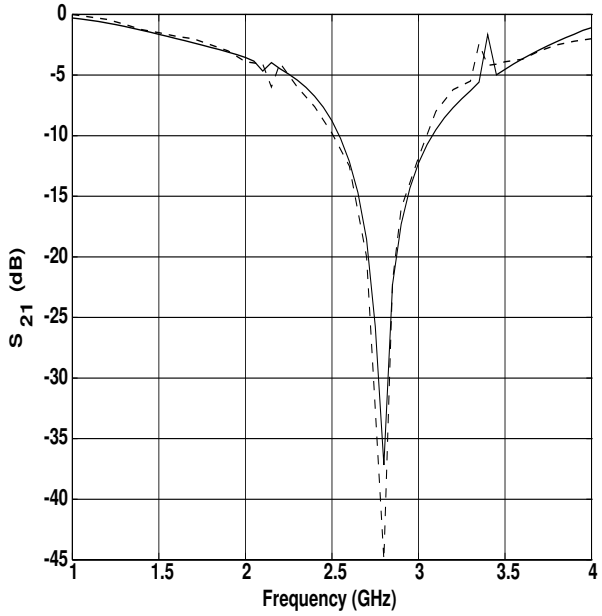

Figure 5.7: S21 - Stub filter.

The above s–parameters obtained from simulation were in agreement with measured data obtained from experiments conducted in the lab.

5.2.3 Performance Measures

Advantages of the presented tool-flow

- Since all the tools are GPL licensed software, allows programmability/customizability and seamless integration.
- Can be used with additional libraries like MPI(parallel algorithm) to improve efficiency

Accuracy of the simulated results

It has been shown that the automatically generated CIF file matches with the hand generated, published by Patwardhan[10]. With the incorporation of the local reference groups, we make sure that effects like time delay, substrate coupling are simulated accurately. The current distribution values and the s-parameters extracted from the full-wave simulator for simple structures were in agreement with the measured data.

5.3 Summary

The above mentioned case studies tested the validity of the individual tools in the framework. The CIF output generated in the first case–study was in agreement with the hand generated CIF file. The simulated results for the structure were in agreement with the measured data. In the second case–study, the tool was tested for its accuracy in capturing distributed structures. The tool was able to identify most of the structures that were laid out.

Chapter 6

Conclusion

An integrated electromagnetic and circuit simulation environment capable of simulating high speed circuits has been implemented. The analysis incorporates surface modes and full nonlinear effects. A 4 cell grid amplifier was used to validate the simulation tools with measurements. The package consists of a method of moments full-wave electro-magnetic simulator, along with a general nonlinear circuit simulation program. The programs and the interfaces between have been defined and documented. The simulation environment allows grid amplifier structures to examined from a wholistic point of view. The effect of edge effects, mutual coupling, and device variations can now be considered. Given a generic layout file, we can attach it with any process. The simulation environment will allow what-if studies to be conducted, limiting the amount of empirical design required Inherent problems in the grid design such as edge elements can now be considered. The effects of device variations can also be examined. Design ideas can now be implemented on the computer first, increasing the overall chance of success

Chapter 7

Future Research

There are many areas that could be pursued further with regard to this simulation environment. The programs in the hybrid co-simulation environment need to be combined together in a more coherent fashion. There is a lot of scope to implement to EM analysis using FDTD techniques. Support for alternate incident field distributions should also be added. Currently only uniformly distributed fields are considered. Other field distributions, such as gaussian distributions should also be implemented. Oscillator and stability analysis also need to be included in the tool set. This would require the inclusion of an oscillator analysis in the circuit simulator. The oscillation analysis should also include a means to test the stability of a grid amplifier system. Another improvement in the circuit simulator is the ability to use subcircuits. Subcircuits are currently supported for passive elements. This needs to be extended to include nonlinear elements also. The use of subcircuits becomes very important as the size of the structures examined increases. The chances of errors in the netlists is greatly reduced and the speed of making changes is greatly increased. Along with improvements in the circuit simulator, the active device models also need to be improved. A strategy for developing nonlinear behavior models is essential. The results from the circuit simulator will in most cases be limited by the accuracy of the active device model. This is especially true under large signal operation. Stability

analysis will require an active device model which is accurate over a large frequency range. The same requirements will hold for designing high efficiency power amplifier systems where harmonic loading is important.

Chapter 8

Appendix

8.1 Appendix A

8.1.1 CIF file format

Caltech Intermediate Format (CIF) is a recent form for the description of integrated circuits. Created by the university community, CIF has provided a common database structure for the integration of many research tools. CIF provides a limited set of graphics primitives that are useful for describing the two-dimensional shapes on the different layers of a chip. The format allows hierarchical description, which makes the representation concise. In addition, it is a terse but human-readable text format. CIF is therefore a concise and powerful descriptive form for VLSI geometry.

Each statement in CIF consists of a keyword or letter followed by parameters and terminated with a semicolon. Spaces must separate the parameters but there are no restrictions on the number of statements per line or of the particular columns of any field. Comments can be inserted anywhere by enclosing them in parenthesis.

There are only a few CIF statements and they fall into one of two categories: geometry or control. The geometry statements are: LAYER to switch mask layers,

BOX to draw a rectangle, WIRE to draw a path, ROUNDFLASH to draw a circle, POLYGON to draw an arbitrary figure, and CALL to draw a subroutine of other geometry statements. The control statements are DS to start the definition of a subroutine, DF to finish the definition of a subroutine, DD to delete the definition of subroutines, 0 through 9 to include additional user-specified information, and END to terminate a CIF file. All of these keywords are usually abbreviated to one or two letters that are unique.

Label Command

94 Input 10,20 Type"Input" Reference="Ground";

This command is another common extension and is used to mark points with a name. The parameters are the name of the label, and the x and y coordinates of the point.

Extensions to CIF can be done with the numeric statements 0 through 9. Although not officially part of CIF, certain conventions have evolved for the use of these extensions

Sample CIF File

This is a sample CIF file modeling a dipole antenna. The units are in millimeters. The name of the layout is 'dipole'. It consists of two boxes on a metal1 type layer.

The centers of two cells are located at the coordinates **(-100; 0)** and **(100; 0)**, and both cell sizes are 200 mm x 200 mm (square boxes). A circuit port (See chapter 3 for port description) is specified at the coordinate (0; 0).

```
DS 1 1 1;
9 Dipole;
L metal1;
B 200 200 -100,0;
B 200 200 100,0;
94 Ground 0,0 Type="Ground";
DF;
C 1;
E
```

8.2 Appendix B

8.2.1 EMPDK User Guide

8.2.2 Introduction

EMPDK prepares a layout file for EM simulation. Some of the basic requirements are the material properties of the layers in the layout. The output of EMPDK is in a human–readable form. This file can be imported to other layout tools like Cadence, LinkCad etc.

8.2.3 Creating a new technology file

The user must have information regarding the process and the layers that go into the layout. To create a new file, the user has to select the option 'New' from the 'File' Menu.

After providing the 'filename' the user will be prompted for information regarding the layers in the process. This information has be entered starting with the substrate layer working your way upwards.

Once the user is done entering the information for each of the layers in the process, he/she can select the 'Done' button in the dialog box. This will automatically generate the file for the user.

More information regarding the layer types supported and how to specify dimensions are given in Appendix C.

8.2.4 Editing an existing technology file

To edit an existing file, the user must select the option 'Open' from the 'File' Menu. Once the user provides the tool with the layout filename, the tool displays a dialog box with the layers used for the layout.

The user must have process information regarding the layers generated by the layout tool. This information can be entered in the dialog box. Once the user is done, the process can be completed by pressing the 'Done' button in the dialog box.

8.3 Appendix C

8.3.1 Technology File Structure

```
// TECHNOLOGY FILE

// METAL LAYERS : 2
// DIELECTRIC LAYERS: 1

technology cmos
  UNITS microns
  metal
     //name        zmin   thickness  resistivity(ohms.cm)  desc
     layer 0        0.00   0.35       0.2                 // G substrate
     layer 1      0.7  0.2          1.56E-4               // M
   endmetal

   dielectric
     //name        zmin   thickness  dielectric constant
     layer 2      0.35       0.35       3.9
   enddielectric
endtechnology
```

Figure 8.1: Sample technology file

The technology file allows the user to specify the process related parameters. The characteristic information obtained from the technology is used

- to specify the thickness of the layers
- obtain the ordering of the layers
- to obtain the electrical parameters like resistivity, dielectric constant, etc.

The structure of the file is very simple and human readable. The first line is a comment line which gives us the version number of the technology file. The next two

lines tell the simulator the number of metal and dielectric layers in this particular process. The description of the process starts with the process name specified by the 'technology' tag. Then we provide the simulator with the units in which the related distance information is provided. By default it is microns. Then we specify the metal layers between the tags 'metal' and 'endmetal'. The information is specified in the bottom-up fashion, i.e, we provide the substrate and then the layer closest to it and work our way upwards. In the similar fashion we provide information of other layers like 'dielectric' and 'via'. The end of the file is denoted by the 'endtechnology' marker.

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