AFRL-PR-WP-TR-2007-2004

DEVELOPMENT OF HIGH-TEMPERATURE, HIGH-POWER, HIGH-EFFICIENCY, HIGH-VOLTAGE CONVERTERS USING SILICON CARBIDE (SIC)

Delivery Order 0003: SiC High Voltage Converters, N-Type Ohmic Contract Development for SiC Power Devices

Lin Cheng, Ph.D.
Michael S. Mazzola, Ph.D.

Mississippi State University
Mississippi Center for Advanced Semiconductor Prototyping
Department of Electrical and Computer Engineering
Box 9571
Mississippi State University, MS 39765-9571

DECEMBER 2006

Final Report for 09 December 2003 – 23 March 2004

Approved for public release; distribution is unlimited.

STINFO COPY

PROPULSION DIRECTORATE
AIR FORCE MATERIEL COMMAND
AIR FORCE RESEARCH LABORATORY
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7251

NOTICE AND SIGNATURE PAGE

Using Government drawings, specifications, or other data included in this document for any purpose other than Government procurement does not in any way obligate the U.S. Government. The fact that the Government formulated or supplied the drawings, specifications, or other data does not license the holder or any other person or corporation; or convey any rights or permission to manufacture, use, or sell any patented invention that may relate to them.

This report was cleared for public release by the Air Force Research Laboratory Wright Site (AFRL/WS) Public Affairs Office and is available to the general public, including foreign nationals. Copies may be obtained from the Defense Technical Information Center (DTIC) (http://www.dtic.mil).

AFRL-PR-WP-TR-2007-2004 HAS BEEN REVIEWED AND IS APPROVED FOR PUBLICATION IN ACCORDANCE WITH ASSIGNED DISTRIBUTION STATEMENT.

*//Signature//

JAMES D. SCOFIELD, Ph.D.
Project Engineer
Electrical Technology and Plasma Physics Branch

//Signature//

JOSEPH A. WEIMER
Chief
Electrical Technology and Plasma Physics Branch

//Signature//

KIRK L. YERKES, Ph.D.
Deputy for Science
Power Division

This report is published in the interest of scientific and technical information exchange, and its publication does not constitute the Government's approval or disapproval of its ideas or findings.

*Disseminated copies will show "//Signature//" stamped or typed above the signature blocks.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number. **PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS**.

1. REPORT DATE *(DD-MM-YY)*
December 2006

2. REPORT TYPE
Final

3. DATES COVERED *(From - To)*
12/09/2003 – 03/23/2004

4. TITLE AND SUBTITLE
DEVELOPMENT OF HIGH-TEMPERATURE, HIGH-POWER, HIGH-EFFICIENCY, HIGH-VOLTAGE CONVERTERS USING SILICON CARBIDE (SiC)
Delivery Order 0003: SiC High Voltage Converters, N-Type Ohmic Contract Development for SiC Power Devices

5a. CONTRACT NUMBER
F33615-01-D-2103-0003

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
62173C

6. AUTHOR(S)
Lin Cheng, Ph.D.
Michael S. Mazzola, Ph.D.

5d. PROJECT NUMBER
1660

5e. TASK NUMBER
PO

5f. WORK UNIT NUMBER
C1

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Mississippi State University
Mississippi Center for Advanced Semiconductor Prototyping
Department of Electrical and Computer Engineering
Box 9571
Mississippi State University, MS 39765-9571

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Propulsion Directorate
Air Force Research Laboratory
Air Force Materiel Command
Wright-Patterson AFB, OH 45433-7251

10. SPONSORING/MONITORING AGENCY ACRONYM(S)
AFRL-PR-WP

11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S)
AFRL-PR-WP-TR-2007-2004

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
PAO case number: AFRL/WS 07-0127; Date cleared: 17 Jan 2007. This report contains color.

14. ABSTRACT
The durability and reliability of metal-semiconductor contacts are two of the main factors limiting the operational high-temperature limits of SiC electronic devices. To date, nickel (Ni) has been the most widely used metal for ohmic contacts to n-type SiC. The way to make smooth Ni-silicide – SiC interfaces and silicide top surfaces is important for producing uniformly low contact resistances to achieve device operation at high-current levels without hot spot formation and contact degradation. For as-deposited single Ni thin layers, agglomeration of Ni-silicide after annealing can happen depending on the conditions of deposition and thermal annealing processes. This is mainly due to the residual stress on the Ni films after deposition on SiC with a significantly lower coefficient of thermal expansion. Typically, an additional stress reduction layer, such as titanium, is deposition on top of the Ni thin contact film to prevent silicide agglomeration. The objective of this Delivery Order Task was to study and develop a process to produce robust, smooth ohmic contact, with low contact resistivity, to n-type SiC for high power, high temperature, and harsh radiation environments.

15. SUBJECT TERMS
silicon carbide, power devices, VJFET, pilot production, salicide, plasma etching, ohmic contacts

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT:	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON (Monitor)
a. REPORT	b. ABSTRACT	c. THIS PAGE			James D. Scofield
Unclassified	Unclassified	Unclassified	SAR	16	19b. TELEPHONE NUMBER *(Include Area Code)* N/A

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std. Z39-18

Title: Self-Aligned Salicide Process Development

Funding: F33615-01-D-2103-0003 (delivery order #3)

Time period: December 09, 2003 – March 23, 2004

I. Background and Purpose:

All useful semiconductor electronics require conductive signal paths in and out of each device. Although SiC itself is theoretically capable of high-performance operation under extreme conditions, such functionality is useless without contacts that are also capable of operation under the same conditions to enable SiC-based electronic devices functionality. The durability and reliability of metal-semiconductor contacts are two of the main factors limiting the operational high-temperature limits of SiC electronics. To date, nickel (Ni) has been the most widely used metal for ohmic contacts to n-type SiC. The way to make smooth Ni-silicide – SiC interface and silicide top surface is important for producing uniformly low contact resistance to achieve device operation at high-current level without "hot-spot". For as-deposited single Ni thin layers, agglomeration of Ni-silicide after annealing could happen depending on conditions of deposition and thermal annealing process. This is mainly due to the built-in stress in Ni film during deposition. An additional metal layer, such as Ti, deposited on top of Ni is then applied to prevent the silicide from agglomeration. The goal of D.O. 3 is to research and develop a robust, smooth ohmic contact with low contact resistance to n-type SiC for high-power, high temperature, and radiation-hardened applications.

II. Material Description:

Substrate					Thickness, concentration of MSU epilayers (center area)			
Wafer #	Vendor	Polytype	Off °	N_{sub}	N^{+}_{buffer}	$N^{-}_{blocking}$	$N_{channel}$	N^{+}_{source}
AG0854-04	Cree	4H	8	7.20E+18	0.34μm, 7.9E+17	4.45μm	N/A	0.43μm, 2.7E+19
CB0440-04	Cree	4H	8	6.60E+18	0.31μm, 2.2E+18	7.9μm	2.1μm	0.29μm, 1.6E+19
998-08	II-VI	6H	3.5	N/A	0.39μm	8.6μm	N/A	0.48μm, 3.4E+19
998-09	II-VI	6H	3.5	N/A	0.18μm, 3.9E+18	8.4μm	1.8μm	0.46μm, 1.7E+19
998-10	II-VI	6H	3.5	N/A	0.15μm	8.9μm	1.9μm	0.56μm, 1.15E+19

III. Process Description:

The carbon-mask fingers used as the implant stop layer on all lot 3 wafers were consumed during the first Plasmatherm PECVD oxide deposition (Fig. 1). Without carbon-mask fingers, the n^+ SiC source fingers would have been implanted during the p^+ gate implantation, eliminating the possibility of working devices from this lot if we had finished the entire process described in the traveler. Although we lose the n^+ SiC source region, the original n^+ layer should still remain n-type after p^+ implantation. The resulting p^+-n junction can be still used to test for electrical shorting after the salicide process. Based on these considerations, the SemiSouth/MSU team decided to send all lot 3 wafers

out for implantation and finish the SA salicide process according to the traveler but then stop there. Details on procedures and results during the process development are described as follows:

1. Survival of C finger and adhesion of oxide spacer to the C finger (as implantation mask) sidewall for ion-implantation

# of Attempts (Date)	Brief Description of Process	Results / Comments
1 (01/05/2004)	5 KÅ oxide deposition using recipe "Oxide 3" • Chemistries: SiH_4 /N_2O/N_2 • Dep. temp.: 250 °C • Power: 25 W • Pressure: 900 mTorr • Dep. Rate: ~ 140 Å/min.	1) C mask fingers were consumed during the oxide deposition: Consumed C fingers SiC source fingers (Lot 3 wafer) Fig. 1 after stripped off the deposited oxide. 2) The above result was further confirmed by the same process on a Si test wafer: Fig. 2 Before oxide dep (left); after oxide dep (mid); after stripped off the deposited oxide.
2	5 KÅ oxide deposition on Si test wafers using recipe "Oxide 1A" • Chemistries: SiH_4 /N_2O • Dep. temp.: 250 °C • Power: 25 W • Pressure: 900 mTorr • Dep. Rate: ~ 400 Å/min.	1) C fingers/Si were not consumed. 2) no oxide peeled has been found. Fig. 3 Before oxide dep (left); before/after BOE etch (mid); after stripped off the deposited oxide.

3	1) Repeat “attempt 2” on a quarter of one SiC test wafer (B1056-14). 2) Etch back oxide	No oxide and C finger peeled: Fig. 4 After oxide deposition and etch back.
4	Following “attempt 3”, Simulate the ion-implantation condition by anneal the sample in vacuum at 650 °C for 10 minutes.	Oxide spacer stick well to the C finger sidewall after vacuum anneal: Fig. 5 After vacuum anneal at 650 C for 10 min.
Conclusion	• The oxide deposition process for forming oxide implant spacer has been examined. • “Attempt 2” was demonstrated to avoid the consumption of C finger during the oxide deposition and any oxide peel afterwards.	

2. High yield, good morphology / low surface roughness of self-aligned silicide formed on both n^+ source finger and p^+ gate areas with no electrical short

No. of Attempts (Date)	Brief Description of Process	Results / Comments
1 (Jan. 21-30, 04)	<u>Blanket metal deposition:</u> Oxide spacer →Blanket metal deposition using old sputtered Ni/Ti/TiN recipe → RTA at 950 °C for 2 min → strip off the un-reacted metals.	1) After RTA and strip-off metal, smooth salicide and SiC-salicide interface were obtained. 2) 30 of 33 tested structures on 998-09 pc1 shows No electrical short.

		Fig. 6 self-aligned silicide formed on S & G on 998-09-pc01 (top) and pc02 (bottom) after RTA at 950 °C for 2 min and striped off un-reacted metals.
2 (Feb. 02-10, 04)	<u>Lift-off metal stack by photo-resist:</u> Oxide spacer → Pattern with VJFET04B Salicide mask using LOR3A/AZ1805 → deposit old Ni/Ti/TiN → PR lift-off with help of ultrasonic bath → RTA at 950 °C for 2 min.	1) Experiencing difficulty to lift off metal, while introducing stress into the structure due mainly to the use of ultrasonic bath → not recommended. 2) Rough salicide surface, but no discontinuity.
3a (Feb. 02-10, 04)	<u>Process for sputtered metal dep and lift-off:</u> Same process as "Attempt 2" on wafer 998-08, but use new sputtered TiN recipe in the Ni/Ti/TiN stack to lower the resistivity of TiN while reduce the TiN roughness after RTA.	1) Still rough salicide surface after RTA. 2) Sputtered Ni/Ti/TiN metal stack made the lift-off process difficult → Need to develop new process for metal deposition to make the metal lift-off easier. 3) The resistivity of new sputtered TiN was around 300 mΩ·cm.
3b	<u>Process for evaporated metal dep and lift-off:</u> Same process as "Attempt 2", but use evaporated Ni(700Å)/Ti(200Å)/TiN(500Å) on	1) Metal lift off for the evaporated Ni/Ti/TiN was much easier than that for the sputtered metal stack in "Attempt 3a". 2) The capability to do Ar ion-mill

	Si test wafer first then on SiC pc with surface pre-clean by Ar ion-mill at 750V at ~ 10^{-5} mTorr.	before metal dep in the e-beam evaporator can make/keep clean surface/contact area for metal contact formation. 3) The resistivity of TiN evaporated on the glass sheet/wafer varied from 92, 160, and 201 mΩ·cm.
4 (Feb. 24-26, 04)	<u>Test on un-reaction of oxide at field and SF sidewall to metal during RTA:</u> Quarter wafer 998-10 into A, B, C, D → 1) On quarter A, directly apply ohmic metal on S & G by lift-off process. 2) Instead of metal lift off, use oxide to pattern the areas that do not required silicide (field and SF sidewall), then blanket dep ohmic metal as follows: Blanket oxide 1A (~ 6K Å) deposition on B → pattern with VJFET04B salicide mask using resist 1805 → etch through the oxide and leave the oxide on the field area and SF sidewall → remove the resist → blanket metal (new Ni/Ti/TiN) deposition → RTA at 950 °C for 2 min. → wet etch unreacted metal (Ti/TiN) away from top of the oxide and leave silicide formed on S & G area → electrical test. 3) Repeat B on C and D	1) Quarter A was failed with lift-off process. Metal was already rough after incomplete lift-off. 2) Quarter B has Smooth salicide on both gate and source region (Fig. 7 left), and has no electrical short tested before and after strip-off oxide spacer. Oxide began peeling from the mesa edge after anneal (Fig. 7 right). 3) The results from quarter B can not be repeated on quarter C and D using the same process. Oxide peeled from after deposition. Oxide was redeposited. The oxide etching process varied un-intentionally due to uncertainty on the system/equipment conditions. For example, the oxide etch rate were much slower on C and D than B using same recipe. Evidence of polymer formation during the oxide etch. Electrical short everywhere on C and D. 4) Problem to completely remove metal from top of the oxide after RTA, possibly due to the reaction of Ni or Ti with oxide during RTA. 5) On two Si test wafers, Oxide 1A was not stable and gave relatively large non-uniformity (up to 1K A difference) across the 2" wafer. 6) Optimization of the oxide deposition is necessary for a robust salicide process.

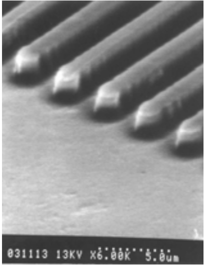
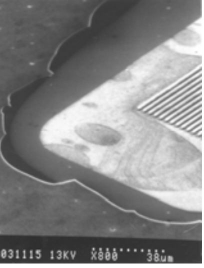
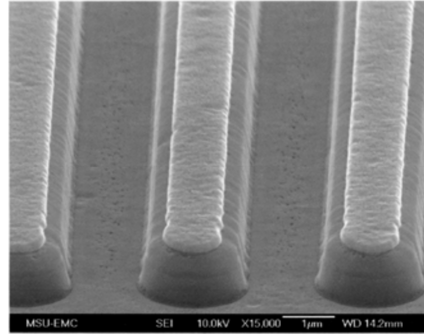
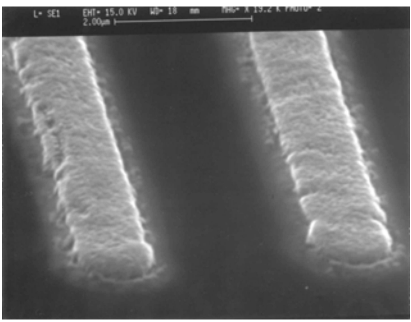
<table>
<tr>
<td></td>
<td> 

Fig. 7 Left: self-aligned silicide formed on S & G on 998-10-B after RTA at 950 °C for 2 min and striped off un-reacted metals. Right: 998-10-B after RTA showed the oxide peeled.</td>
<td></td>
</tr>
<tr>
<td>5
(Mar. 01-04, 04)</td>
<td><u>Test of more oxides as insulator which should not react with metal during the RTA:</u>
Seven oxides (~ 4K to 6.7K A) have been formed on 7 good Si test wafers:
• Oxide 1A with 25 W,
• Oxide 1B with 50 W,
• Oxide 1C with 100 W,
• Oxide 1 with 250 W,
• Oxide 1den with 250 W and densification in dry O_2 at 900 °C for 1 hr,
• Oxide 4 = oxide 3 but using 250 W,
• Oxide 4den with 250 W and densification in dry O_2 at 900 °C for 1 hr.
Then → pattern with VJFET04B guard ring mask using resist Omnicoat/AZ1805 → etch through the oxide and leave the oxide on the field area and source finger sidewall → remove the resist → blanket metal (new Ni/Ti/TiN) deposition → RTA at 950 C for 2 min. → strip off the un-react of metals → electrical test.</td>
<td>After stripping off the rest of metal:
1) Most field area (>90%) of Oxide 1A is clean (reddish pink) and smooth, electrical short is only tested in the area with dense devices, while all other oxides show rough or partially rough oxide surface with metal left which contribute to the electrical short between S-G.

2) The leakage current of oxides measured at 50V on all samples showed that:
I_{leak}(oxide1A)=160 μA
I_{leak}(oxide1B)=0
I_{leak}(oxide1C)=30 μA
I_{leak}(oxide1)=13 μA
I_{leak}(oxide1_{den})=0 μA
I_{leak}(oxide4)=0 μA
I_{leak}(oxide4_{den})=0 μA

3) The elements analysis by EDAX on all oxides at the field area showed the existence of small amount of Ti in the oxides after RTA.

<u>Comments:</u> Oxide densification on 1_{den} and 4_{den} made the oxides cleaner, smoother and less electrical leakage than those before densification.</td>
</tr>
</table>

6 (Mar. 02-23, 04)	Finalize salicide process by adding or modifying the following process, according to the results from previous attempts: • Etch SiC mesa before ohmic metal deposition • Do sacrificial oxidation after mesa etch, not after implantation. • Densification of oxide spacer and oxide left in the field area. Densified oxide should not react with ohmic metal during RTA. • Pattern the oxide with "salicide mask" leaving the oxide on SF side-wall and field area, followed by metal deposition using sputtering system. Then un-reacted metal on the oxide and source-gate region will be wet-etched away. More detailed process: Cut wafer AG0854-04 in halves → 1) pattern A-B half with VJFET04B guard ring mask using Omnicoat/6000 P (w/o filter, 120 mJ/cm^2) → SiC mesa etch on A-B half (~ 0.7 µm using #34, NF_3) → remove resist → 2) cut A-B (after mesa etch) and C-D (no mesa etch) halves into four quarters A, B, C and D → 3) sacrificial oxide (wet, 1100 °C for 45 min.) on B → wet etch B in BOE to remove oxide → deposit 6K Å oxide (Oxide1 or Oxide4) on A and B → pattern A and B with "VJFET04B salicide" mask using omnicoat/AZ1805 → etch oxide till clear → remove PR → densification in dry O_2 at 900 °C for 1 hr → Ar etch (15s-20s) → metal deposition → RTA at 950 °C for 2 min. → wet etch off any un-reacted metals → Gap fill → etch back to open ohmic window on both SF top and gate pad for final metal deposition (Ti/Al) → … finish … → test breakdown	 Fig. 8 self-aligned silicide formed on S & G on AG0854-04-pcA after RTA at 950 °C for 2 min and striped off un-reacted metals.  Fig. 9 AG0854-04-B after etch back of gapfill. On top of the SF: silicide. Purposes to change process as follows: 1) etch 0.7 µm SiC mesa before deposit ohmic metal stack to improve G-D breakdown voltage. 2) Do sacrificial oxidation after SiC mesa etch to remove the damages from both ion-implantation and mesa etch. Previously, the sac oxidation was done before SiC mesa etch. In that case, there is no way to do the sac oxidation after mesa etch due to the existence of metal/ silicide formed before mesa etch. • Repeating B on C and D failed because of the bad pattern.

	4) Repeat B on C and D.	
Conclusion	• Process for SA silicide formation has been developed and finalized as it described in "Attempt 6". • The developed salicide process can provide smooth, clean and self-aligned silicide formed on top of SF and gate area. • According to Fig. 9, the etching process for final metal contact can roughen the formed silicide surface, which might affect the device performance, but not known.	

3. Optimization of RTA process for good ohmic contact formed on self-aligned n^+ source finger and p^+ gate areas

The process set for previous Lot 2 has been used (i.e., 2 min. in UHP N_2 at 950 °C in RTA). No changes have been made to this process.

4. Ohmic contact characteristics at both RT and elevated temperatures

Two quarter pieces of one 4H-SiC lot 3 wafer (AG0854-04-A & B) have been tested for breakdown voltage at temperatures from RT to 300 °C, as shown below. Regarding the difference between the processes applied to A and B, B received sacrificial oxidation and oxide strip in order to remove damage induced during mesa etch on the side wall and surface, while A didn't receive the sacrificial oxidation after mesa etch. Moreover, the etched mesa depth of A and B are slightly different due to the unintentional variation of etch parameters for different runs. From the data shown below (Fig. 10), the breakdown voltage of the PN diode on B is about twice that of A. This indicates that the surface damage introduced during mesa etch negatively affects the device performance. Performing the sacrificial oxidation after mesa-etch rather than after ion-implantation can help to improve the breakdown behavior at both room temperature and elevated temperature.

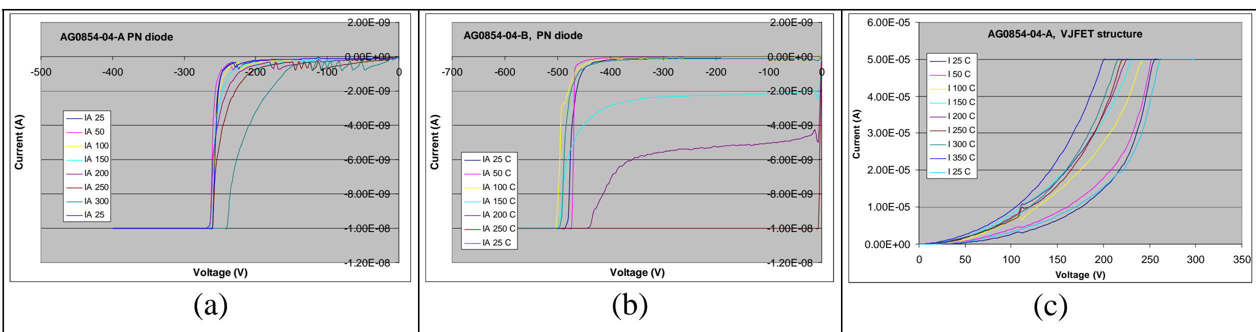


Fig. 10 Breakdown voltage of a PN diode on (a) AG0854-04-A and (b) AG0854-04-B measured from 25 to 300 °C; (c) Breakdown voltage of a VJFET on AG0854-04-A measured from 25 to 300 °C.

IV. Results and Summary:

- Due to the unexpected consumption of the carbon fingers during the Plasmatherm PECVD oxide deposition used to form the oxide spacer before ion implantation, there was no possibility of obtaining working devices from this lot. However, the original n^+ source layer remained n-type after p^+ implantation and activation. This allowed the lot to continue for the alternative purpose of developing a self-aligned salicide process with no source-to-gate electrical shorting.
- Survival of carbon-finger and adhesion of oxide spacer to the carbon-finger sidewall for ion-implantation was then examined. Two attempts preceded, as described on page 2. "Attempt 2" in Sec. III-1 was first tried on a quartered 2" Si test wafer then repeated on a quarter of one 2" SiC test wafer, followed by simulating the actual ion-implantation temperature condition by annealing the sample in vacuum ($\sim 10^{-5}$ Torr) at 650 °C for 10 minutes. Therefore, "Attempt 2" in Sec. III-1 was demonstrated to be qualified for no consumption of C finger during the oxide deposition with no oxide peeling after annealing at "implant-temperature."
- As shown in Sec. III-2, six splits were executed to develop a "clean, smooth and not electrically shorted" self-aligned salicide process. Because of its natural tendency not to react with silicide metals at the anneal temperature (at least 950 °C ± 100 °C), oxide was chosen as the electrical and chemical isolation layer during the silicide metal deposition and anneal. Several Plasmatherm PECVD oxides layers were then tested for such purpose, as shown in the "Attempts 4 & 5" on pages 5-7. By "Attempt 6", a self-aligned but clean, smooth metal silicide was formed on top of the source fingers and at the gate areas on the trench bottom. The technical approach taken for each of the six attempts is as follows:

  Attempt 1: Blanket metal deposition as a reference for comparison of silicide formed by lift off and non-lift off process.
  Attempt 2: Lift-off metal stack by photo-resist.
  Attempt 3: Comparison of lifting off sputtered and e-beam evaporated ohmic metal stack. Evaporated metal stack gave smoother metal and silicide after lift-off.
  Attempt 4: Test on un-reaction of oxide at field and SF sidewall to metal during RTA process.
  Attempt 5: Test of more oxides as insulator which should not react with ohmic metal during the RTA process.
  Attempt 6: Finalize salicide process.

  In the meantime, the process used in "Attempt 6" was further modified to improve the device performance as well as production yield as follows:

  1. etch ~ 0.7 μm SiC mesa before deposit ohmic metal stack to improve G-D breakdown voltage.
  2. Do sacrificial oxidation after SiC mesa etch to remove the damage from both ion-implantation and mesa etch. Previously, the sacrificial oxidation was done before SiC mesa etch. In that case, there is no way to do the sacrificial oxidation after mesa etch due to the presence of metal/ silicide formed before mesa etch.
  3. Densified the oxide spacer and oxide left in the field area to improve the quality of the oxide stoichiometry, and to reduce pin holes if any. Also the

densified oxide was expected to have better dielectric properties (less leakage current and higher dielectric strength) than the un-densified oxide. However, no test was performed to verify this assumption.

Moreover, according to Fig. 9 in "Attempt 6", the etching process for final metal contact can roughen the formed silicide surface, which might affect the device performance.

- The breakdown behavior of the samples having the sacrificial oxidation before and after mesa etch have been compared between AG0854-04-A & B. The breakdown voltage of PN diodes on B is about twice that on A. This indicates that the surface damage introduced during mesa etch can negatively affect the device performance. Performing the sacrificial oxidation after mesa-etch rather than after ion-implantation can help to improve the breakdown behavior at both room temperature and elevated temperature.