

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
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1. REPORT DATE (DD-MM-YYYY) 02-27-2007		2. REPORT TYPE Technical Report		3. DATES COVERED (From-To) 12-01-2006 to 02-28-2007
4. TITLE AND SUBTITLE Q5 Known Goods Substrates Technical Report		5a. CONTRACT NUMBER N00014-05-C-0324		
		5b. GRANT NUMBER		
		5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S) Loboda, Mark; Carlson, Eric; Chung, Gilyong; Russell, Brian		5d. PROJECT NUMBER		
		5e. TASK NUMBER		
		5f. WORK UNIT NUMBER		
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		11. SPONSOR/MONITOR'S REPORT NUMBER(S)		
12. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified/Unlimited				
13. SUPPLEMENTARY NOTES				
14. ABSTRACT: The Known Good Substrates (KGS) program is on track technically and financially with program tasks. A no cost time extension was processed from February to March 31, 2007. The remaining Q3 and Q4 wafers were delivered after a delay due to equipment down time. Q4 wafer metrology and characterization was completed. Results are reported from first device fabrication lots. Many subcontractors are ramping down activities as their work nears completion.				
15. SUBJECT TERMS SiC wafer, SiC epi, SiC material metrology				
16. SECURITY CLASSIFICATION OF: U		17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES 9	19a. NAME OF RESPONSIBLE PERSON Mark Loboda
a. REPORT U	b. ABSTRACT U			c. THIS PAGE U

Q5 Known Good Substrates Technical Report
 CONTRACT/PR NO. N00014-05-C-0324 Dow Corning Corporation
 Quarterly Technical Report
 Reporting Period: 1 December 2006 – 28 February 2007

Executive Summary

The following tables summarize progress against key milestones and metric goals after 15 months of work. The color coding shows red as incomplete milestone or below metric target, yellow as behind schedule or close to metric and green as a completed milestone or achieved metric.

Thrust	Quarter	Milestone
Task 1: SiC Wafer Products	1	50% sliced wafer increase for 76 mm diameter crystals
	2	Complete model of 100 mm PVT growth*
	3	80% sliced wafer increase for 76 mm diameter crystals
	4	Deliver first generation 4H n+ 100mm wafers - DELAYED
Task 2: Materials Applied Research	1	Complete model of Generation1 bulk gas growth
	1	Qualify Batch Epitaxy processes for program
	2	Demonstration of CVT growth*
	4	Deliver first 76mm CVT wafers
Task 3: Metrology for Wafer Specifications	2	Implement LLS inspection with particles, pits, and scratches delineated.
	3	Start routine microwave loss inspection of 4H SI wafers
	2	u-PCD tool installed and lifetime measurements implemented for epitaxy layers and SI wafers
Task 4: Device Technology Maturation	1	Publish Rev-0 roadmap for wafer and epi goals
	2	Complete disposition strategy for n+ epiwafers
	4	Publish revised roadmap to reflect power and RF device progress

Executive Summary

Work in the fifth quarter has focused on the following areas:

- **Catch up of wafer generation backlog from Q3-Q4 due to polisher failure.** This has been completed and 35 wafers were delivered to ONR under the program. In addition the final group of epiwafers will start process March 1 and be delivered to the subcontractors.
- **Suppression of ancillary deposition in CVT.** Novel redesign of the gas injection scheme and the crystal growth reaction zone has been completed. Test results of the new gas injector are extremely promising as no clogging has been observed in several consecutive tests. A new intermediate design of the reaction chamber also shows that the method developed has high probability to eliminate downstream deposits as well. The newly machined reaction cells with the full new design are due for delivery week of Feb 26 and will be tested in March.
- **First results of SIT device testing at NGES have been delivered.** In the first lot which contained 6 DCCSS epiwafers (from Q1 and Q2) and 2 from a qualified external supplier,

the results showed that the DCCSS wafers provided the same device functional yields as the legacy wafers, and also the CSS wafers showed the same functional yield as the historical data. Mis-targeting of the dopant concentration of one of the epilayers fabricated by DCCSS pushed the device operating point outside the target limits. This has been corrected in later deliverables from DCCSS. Small numbers of DCCSS wafers processed in other NGES lots also demonstrated high functional yields.

Most all metrics have been achieved in the program. Current data in Q5 shows that by the end of Feb 2006 the quarterly MPD median has dropped to 20/cm², exceeding the metric value goal for program. It is most likely that the first CVT wafers will not be available until sometime in the first half of 2007. With the NGES device performance, DCCSS will complete the defect reduction roadmap and publish it in the KGS year 1 final report.

Technical Progress

The following table documents the key program thrusts, milestones by quarter and progress for the activity in the quarter documented by this report. New text, associated with Q4 progress is shown in black.

Thrust	Complete by Quarter	Milestone	Progress
Task 1: SiC Wafer Products	1	50% sliced wafer increase for 76 mm diameter crystals	Since Jan 2005 (the anticipated start of the KGS program, about which the goal was projected) the slice wafer yield has increased by 2x.
	2	Complete model of 100 mm PVT growth	Thorough modeling of 76mm was extended one month to insure agreement with all experimental results. 100 mm modeling is underway at both subcontractor and in house. Initial modeling of the heat losses has helped to drive PVT process alterations which resulted in a 3x reduction of growth rate variability in 100 mm PVT processes.
	3	80% sliced wafer increase for 76 mm diameter crystals	Since Jan 2005 (the anticipated start of the KGS program, about which the goal was projected) the slice wafer yield has increased by 2x.
	4	Deliver first generation 4H n+ 100mm wafers	Work on 100mm crystal growth has succeeded to produce crystals of diameter 100mm and length exceeding 25 mm, but crystal stress grain boundary density is undesirable. Recent PVT process development for 76mm diameter crystal growth has yielded new methods to reduce stress and micropipes. DCCSS feels that to achieve the desired quality for 100mm diameter crystals, it is pertinent to go stall the 100mm effort and repeat the crystal expansion work using these new techniques. Three polished wafers will be delivered to ONR to baseline the progress so far in the program.
Task 2: Materials Applied Research	1	Complete model of Generation 1 bulk gas growth	Due to delay in release of funds for KGS, Dow Corning funds were used to initiate the modeling project in the second half of 2005. A Gen-1 model has been completed based on one chlorosilane precursor and one set of process conditions. The results show that growth rate and deposition uniformity comparable to PVT processes can be expected over the

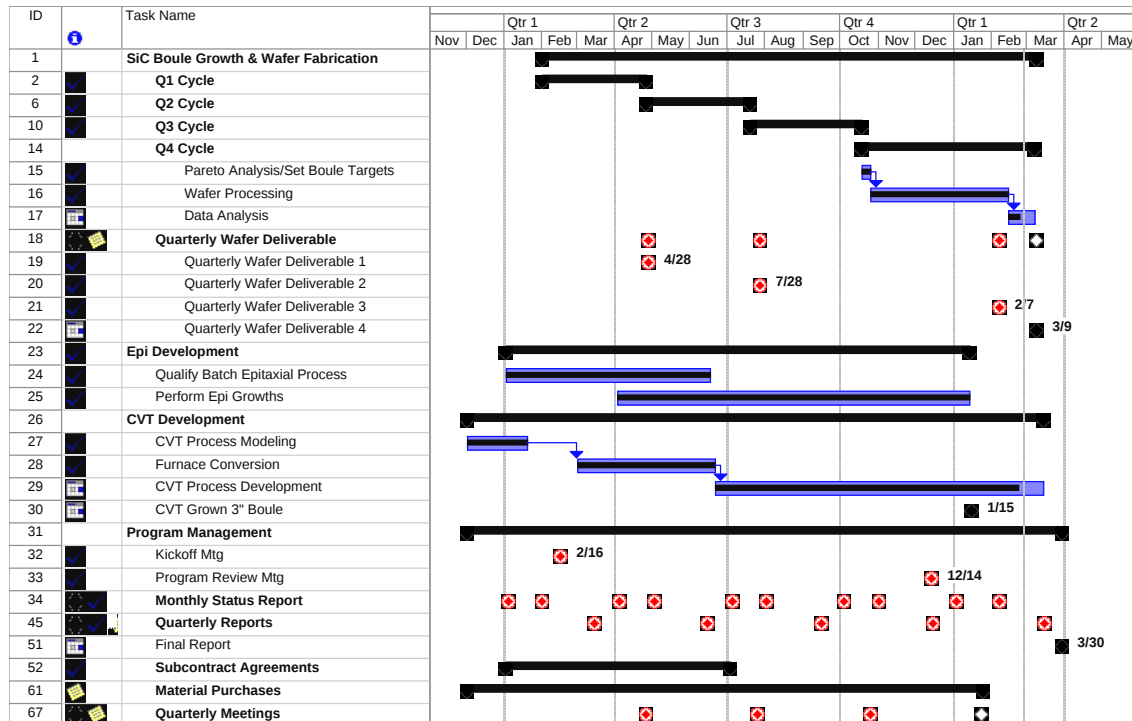
			temperature range 1900-2100 C. At this point it is believed largest source of error in the model is the formation of deposits on ancillary surfaces of the crucible. Additional modeling work was performed to better understand the mechanism for observed ancillary deposition of silicon in the gas injector. The temperature distribution near the region of deposit is the critical issue. A new injector design is being developed.
	1	Qualify Batch Epitaxy processes for program	Recent epitaxy work focused to develop processes for the Northrup Grumman device subcontract. Developmental work in the multiwafer reactor produced mid doped ($1E15$-$1E16/cm^3$) epi layers with thickness uniformity (standard deviation/mean) of less than 4 % and doping uniformity of less than 8%. By the end of Q2 24 epiwafers will be processed and delivered to Northrup for device fabrication. Limited work was performed to assess low doped drift layer epitaxy. In these cases it was demonstrated that levels of $5E14/cm^3$ could be produced in the multiwafer reactor. Epiwafer deliverables were shipped to NRL with full characterization data. Samples exhibit carrier lifetimes in the 5-10 usec range. For the remainder of the first year of the KGS program, the minimum doping target for drift layer epitaxy will stay in the 1-$3E15/cm^3$ range to afford better assessment of carrier lifetime by microwave photoconductive decay measurement. NGES has provided wafer probe data from first fabrication lots of SIT devices. Fabrication lots include both DCCSS epiwafers (~80%) and epiwafers purchased from NGES qualified legacy vendor (~20%). Functional yields of devices on the DCCSS wafers was equivalent to that of the wafers from the legacy vendor and to the historical device process capability. A doping concentration target offset was observed in the DCCSS wafers, this resulted in a threshold voltage shift outside the device target limit. This offset is not a process capability error, but is just a result of DCCSS/NGES learning how to tune the process so both sites read the same doping targets. NGES has an additional lot of CSS epiwafers that have been tested and meet the desired doping concentration targets. NGES is very pleased with the results and will continue to assess the quality of the material for future use in their device fabrication work.
	2	Demonstration of CVT growth	CVT (gas phase) depositions start week of 6/12/06. System is in house and facilitated.
	4	Deliver first 76mm CVT wafers	After several developmental growth experiments a major issue evolved with silicon deposition upstream of the seed in the injector. Modeling has been used to define the effect very accurately. New injector designs are being developed. A 5 mm thick crystal was grown in the CVT system in 5 successive growth experiments. The injector was changed each time. The growth rate was very consistent throughout the crystal growth at nominally 250 um/hr. Step formation was

			apparent over the majority of the crystal. The resulting crystal was primarily 4H, with some sections of 6H polytype. Small (<1 mm) inclusions of 3C-SiC were clustered in the center, and this is likely the result of gas induced cooling of the growth front. The system will now be rebuilt with a different crucible design and modified exhaust system to suppress downstream reactant condensation. This quarter has focused to reduce the formation of deposits in the gas injectors and in the system exhaust. Redesign of the gas injection to the reaction zone has eliminated the formation of deposits in the injectors as best as can be tested. The deposition of ancillary SiC at the exhaust of the reaction zone has also been reduced, and a new design is in fabrication which is believed to achieve the same performance as on the inlet injectors. Downstream deposits in the exhaust system have been eliminated by redesign of the valves. The improvements will allow the CVT process to be capable of extended crystal growth (>25 hrs), and this will be tested in March 2007.
Task 3: Metrology for Wafer Specs	2	Implement LLS inspection with particles, pits, and scratches delineated.	Wafers were shipped to ONR and NRL with LLS topography maps. First generation work to segregate defect types is nearly complete and data will be provided in June. Algorithms and mapping used for pit detection and fine scratch identification are in use. The results show a clear reduction of pits and scratches has been achieved between Q1 and Q2. Pit and scratch levels on polished wafers are now at program goal.
	3	Start routine microwave loss inspection of 4H SI wafers	Loss measurement calibration and test is progressing well. Full wafer global loss testing in cavities has been performed at 4 GHz and compared to SI GaAs as a benchmark. Several 6H SI wafers with resistivity $1E5$-$1E7$ ohm cm show microwave loss equal to SI GaAs. There is no obvious correlation between loss and resistivity, as expected in these materials. Mapping tests show many regions with loss less than SI GaAs. Next focus is on extending the measurements to X-band. In Q3 a method for measurements of microwave loss on SiC wafers has been developed. Trends closely mimic the observations at L-Band. In general, the results show that SiC is a lower loss material than both GaAs and alumina. In Q4 additional capability was developed to make measurements to 13 GHz. Similar trends between SiC, GaAs and sapphire were observed from 2-13 GHz. A capability to perform loss maps on wafers over this frequency range is now established.
	2	u-PCD tool installed and lifetime measurements implemented for epitaxy layers and SI wafers	u-PCD testing of carrier lifetime is fully operational. Key results show that chlorosilane-based SiC epi has very high lifetime. Samples were delivered to NRL for conformational analysis. Photoluminescence decay tests at NRL confirm long recombination lifetime values in chlorosilane-based epitaxial

			layers grown and tested at Dow Corning. The samples generated to date in the KGS program represent the longest lifetime values reported in the literature. Efforts at ASU to measure generation lifetime in MOS structures grown on chlorosilane-based epitaxial layers also show large values consistent with PL and μ-PCD testing. A provisional patent has been filed by Dow Corning regarding gas phase processes to produce long lifetimes in SiC semiconductors. μ-PCD testing on PiN structures was performed. It was found the presence of the p^+ layer does not inhibit the measurement of the carrier lifetime, but it does result in a lower measured lifetime compared to the same structure with the p^+ layer removed. This could be the result of interfacial or surface recombination effects. The μ-PCD maps will be compared to PiN device yields when the devices complete fabrication in year two of the program.
Task 4: Device Technology Maturation	1	Publish Rev-0 roadmap for wafer and epi goals	See Appendix 2
	2	Complete disposition strategy for n^+ epiwafers	See Appendix 3.
	4	Publish revised roadmap to reflect power and RF device progress	

Schedule

A detailed description of achievements and progress against milestones and deliverables was provided in the table above. The project schedule is provided below as an overview of the progress against the high level tasks on the program. Progress is on track with exception of the gas phase (CVT) task, which is 1.5 months behind due to delays in receiving the tool from the vendor (the schedule has been updated accordingly) and the 100mm wafer task (described in the technical section above).



Program Management

Monthly e-mail status updates were submitted to the Program Officer, Dr. Colin Wood. A not cost time extension was granted from February to March 31, 2007. Most subcontractors have completed their work and have a small amount of budget (reference % spending table below) left to wrap up analysis and reporting for the program. A couple of the universities are continuing to complete efforts under the no cost time extension with goals of finishing over the next couple of months.

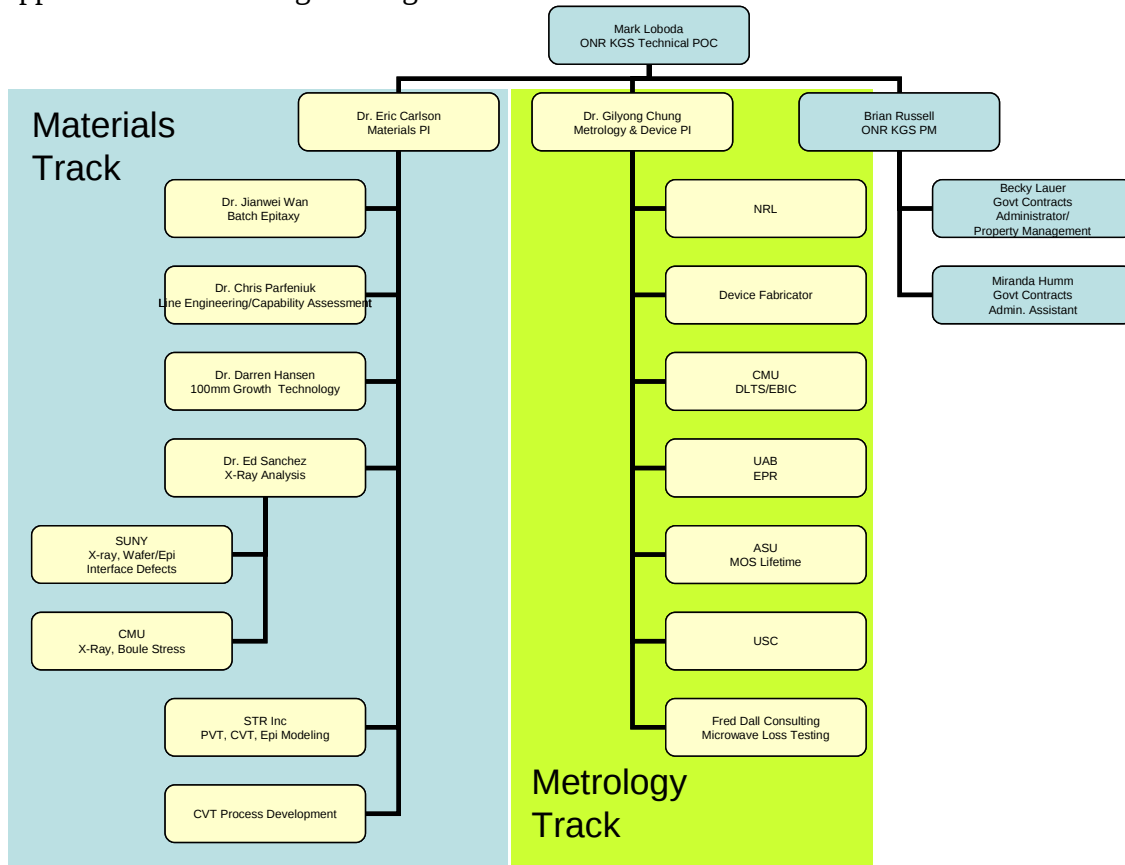
	ASU	CMU	SUNY	UAB	USC	STR	NG	Fred Dall
% Spent	71%	94%	98%	31%	97%	91%	81%	100%

Appendix 3 contains the updated distribution of program wafers. It is important to note that the original plan had to be modified to meet various needs and opportunities for the work on the program – see Appendix 3 for details.

Cost Status

Cost status updates are provided to Dr. Colin Wood in the monthly e-mail updates.

Appendix 1 – KGS Program Organization



Appendix 2 – KGS Rev-0 Roadmap for Wafer and Epi Goals

Proposed Goals:	Top 30%	Top 50%
Timing for 76 mm diameter	Q1/06	
Timing for 100 mm diameter	Q1/07	
MPD and inclusions (cm ⁻²)	<10	<30
Scratches (total length)	<50% diameter	<75% diameter
Areal density surface particles and pits in epiwafers, diameter >0.5 um	<5 cm ⁻²	<10 cm ⁻²
Bulk Metals Contamination B, Al, Ti, V, Fe (atoms/cm ³)	<1E15	<5E15
Stable Epi drift layer carrier concentration (atoms/cm ³)	<1E14	<5E14
Epi thickness uniformity	<8%	<10%
Epi Doping Uniformity	<10%	<15%

Appendix 3 – KGS Wafer Disposition Plan

Wafers Produced for Program

75mm n+
75mm SI
100mm n+
100mm SI
Total

Q1	Q2	Q3	Q4	Total Wafers
0	43	21	56	120
0	0	6	0	6
0	0	3	0	3
0	0	0	0	0
0	43	30	56	129

Distribution

NRL (Lifetime Measurements)
CMU (Deep Level, XRT)
Alabama (Deep Level Measurements)
ASU (Lifetime Measurements)
USC (Diodes)
NGES
ONR

Epi	No Epi	Epi	No Epi	Epi	No Epi	Epi	No Epi	
	5		2	2	4		0	13
			2	2	2		0	6
				2			0	2
			2		2			4
	2		1		1			4
	28		14		14			56
	2	6		3	0	33		44
								129

	Mixed Lots
	n+
	SI

The plan has been altered again as compared to the original proposal and the Q3 modification. No cost changes result. The number of wafers increases. Changes are primarily a result of the Northrup Grumman subcontract which required more n+ wafers than originally proposed and new direction from the ONR program manager requiring substrates for ONR use (see details below). To accommodate these changes, less semi-insulating material and less 100mm material will be produced. DCCS has already started to send in deliverables shown for Q3 with some Q4 deliverables planned for early January delivery. Additional wafers were sent to University of Alabama, Arizona State and CMU at no cost to the program.

November 2006 – per request of ONR, Q4 deliverables will be adjusted. 35 pcs. 4H n+ 76 mm on axis polished wafers will be delivered.