

Negative differential resistance of InGaAs dual channel transistors

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Abstract. We demonstrate a new type of velocity modulation transistor (VMT) with an InGaAs dual channel structure fabricated on an InP (001) substrate. The dual channel structure consists of a high mobility 10 nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ quantum well, a 2 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer, and a low mobility 1 nm $\text{In}_{0.26}\text{Ga}_{0.74}\text{As}$ quantum well. The VMTs have a negative differential resistance (NDR) effect with a low source-drain voltage of 0.38 V. The NDR characteristics can be clearly seen in the temperature range of 50 to 220 K with a gate voltage of 5 V. The NDR mechanism is thought to be the carrier transfer from the high mobility to the low mobility channels. Three-terminal VMTs are favorable for applications to high-frequency, high-speed, and low-power consumption devices.

1. Introduction

Negative differential resistance (NDR) effects in semiconductor heterostructures have attracted much interest in relation to high frequency oscillators and high speed memories, since the invention of the resonant tunneling diodes (RTDs) and real space transfer (RST) transistors [1-10]. However, RTDs are two terminal devices and it has been necessary to combine it with passive elements, field effect transistors, or hetero-bipolar transistors [4-6]. In contrast, a three terminal NDR device such as a RST transistor effectively simplify the device structure and reduce the circuit complexity [7-10]. In a conventional RST device, the NDR effect is based on the carrier transfer from the high mobility quantum well region to the low mobility barrier region. Because the carriers have to obtain high energy to transfer to the barrier region, the NDR onset voltage (V_{NDR}) is large. Velocity modulation transistors (VMTs) with dual channel structures are alternative candidates for realizing gate voltage controlled NDR effects [11,12]. However, the peak-to-valley current ratio (PVR) of the VMTs is poor because a significant portion of electrons remains in a high electron mobility channel.

Recently, we fabricated a trench-type InGaAs/InAlAs quantum wire (QWR) structure on an InP (311)A V-groove substrate, which was produced by selective epitaxial growth using molecular beam epitaxy (MBE) with atomic hydrogen and a dimer arsenic source [13,14]. A field-effect transistor (FET) with a trench-type QWR channel has pronounced NDR effects with a highest PVR of 13.3 and a V_{NDR} as low as 0.16 V at 24 K [15,16]. However, the operating current of the QWR-FET was low, and the fabrication process was complex because of the need for selective growth on an InP (311)A substrate. In this work, we demonstrate a new type of VMT with an InGaAs dual channel structure fabricated on a flat InP (001) substrate. This VMT exhibits pronounced NDR effects with a low source-drain voltage. The

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NDR characteristics can be observed even at 220 K. The operating current of the VMT is one order of magnitude larger than that of a trench-type QWR-FET.

2. Experiment

VMTs with InGaAs dual channel structures were fabricated on semi-insulating (001) InP substrates. The substrate was loaded into an MBE chamber and cleaned with atomic hydrogen at 430°C for 5 min, after which a 400-nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer was grown at a growth rate of 1 $\mu\text{m}/\text{h}$. A high-mobility 10 nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ quantum well, a 2 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer, and a low-mobility 1 nm $\text{In}_{0.26}\text{Ga}_{0.74}\text{As}$ quantum well, which formed a dual channel structure, were grown on the buffer layer. To fabricate the VMT, a 10 nm spacer of undoped InAlAs was grown on top of the dual channel, followed by a Si δ -doped layer, a Schottky layer, and a non-alloy ohmic layer. The epitaxial layers were grown at a substrate temperature of 490 °C, with a substrate rotation of 5 rpm. During the growth of the lattice-matched layers to InP substrate, the flux intensities of As_2 , In, Ga and Al were 6.6×10^{-4} , 4.5×10^{-5} , 1.6×10^{-5} , and 1.3×10^{-5} Pa, respectively. The layer structure is shown in the Fig. 1(a). After growth of the layer structure, the VMTs were prepared by optical lithography and wet chemical etching. The etched surface was passivated by depositing a 100 nm SiO_2 film, into which windows were opened and Ti/Au films deposited to form non-alloyed ohmic contacts. As a final processing step, a 300 nm-long Pt/Ti/Au Schottky-gate was deposited between the source and the drain by using electron beam lithography and recess etching. Figure 1(b) shows a plan view SEM image of the 300 nm gate-length VMT. The channel width and lateral separation between the source and drain contacts were 1.0 and 4 μm , respectively.

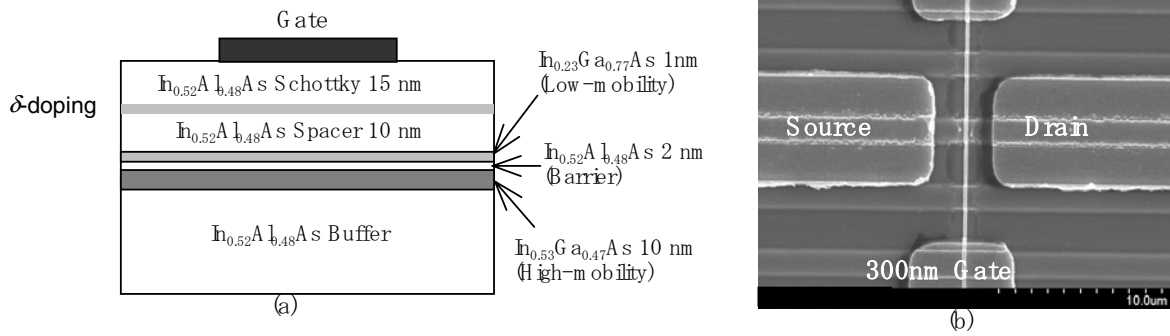


Figure 1. (a) Schematic structure of cross-sectional VMT, (b) SEM plan-view image of the VMT with the gate-length of 300 nm.

3. Results and discussion

The I_d - V_{ds} characteristics of the VMT at 150 K are shown in Fig. 2(a). The gate voltage was varied from 2 to 5 V in 1 V steps. Pronounced NDR effects were observed with an onset voltage of 0.38 V and a PVR of 2.3. The enhanced NDR effects were clearly observed with increasing gate voltage. The operating current of the VMT is about one order of magnitude larger than that of the QWR-FET [15,16]. The temperature dependence of the I_d - V_{ds} characteristic of the VMT is shown in Fig. 2(b). NDR spectra can be clearly seen in the 50 to 220 K temperature range with a gate voltage of 5 V. These results indicate that our new type of VMT with an InGaAs dual channel structure was successfully fabricated on a (001) InP substrate. The VMTs are simple in the device structure and the fabrication processes.

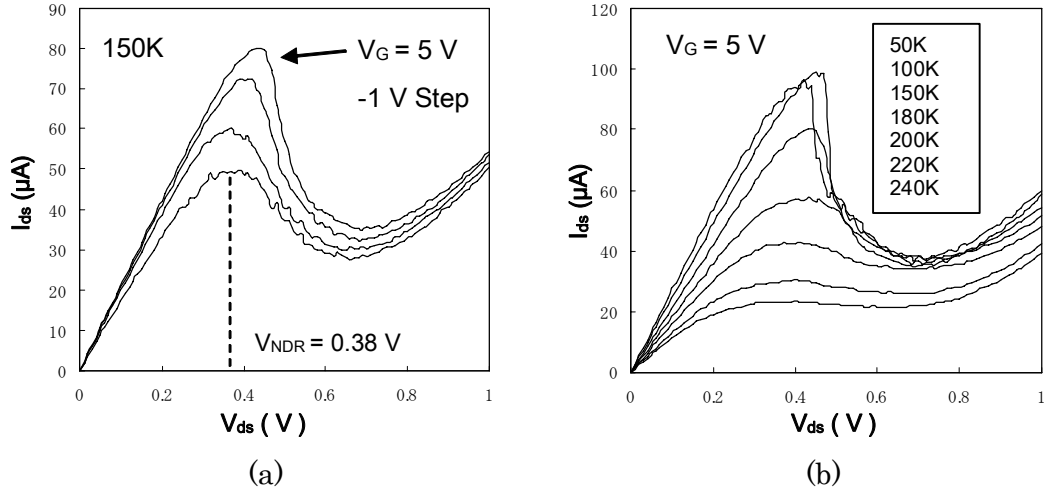


Figure 2. (a) NDR characteristics of a VMT with a gate length of 300 nm at 150 K ($V_{NDR} = 0.38$ V, $PVR = 2.3$), (b) Temperature dependence of the NDR effects for the VMT. The NDR characteristic is clear until 220 K.

The NDR mechanism is thought to be the carrier transfer from the high mobility to the low mobility channels. The mobility of a 1 nm $In_{0.26}Ga_{0.74}As$ channel is extremely low, because of the thinner channel and the lower In content. Figure 3 indicates the schematic diagram of the conduction-band energy of the dual channel structure. The calculated energy separation between the fundamental levels of the high mobility and low mobility channels is about 0.37 eV. The accelerated electrons caused by the drain voltage can be tunnel and transfer from the high mobility to the low mobility channels, because the 2 nm barrier layer is sufficiently thin to tunnel. A V_{NDR} of 0.38 V is consistent with the energy separation in the dual channel structure.

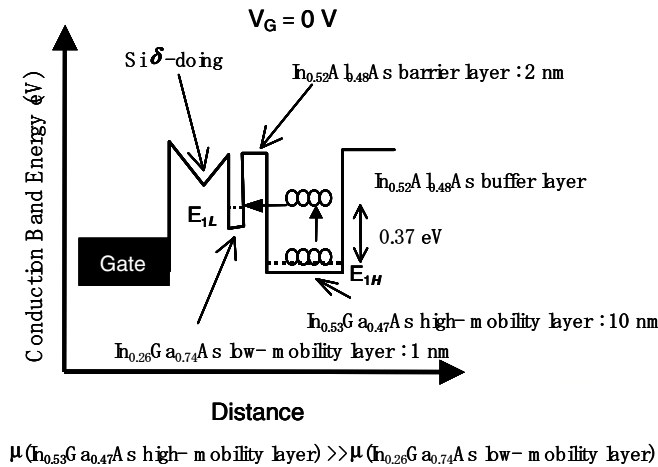


Figure 3. The schematic diagram of the conduction-band energy of the dual channel structure at thermal equilibrium ($V_G = 0$ V).

Another possible mechanism for the NDR is a RST of the carriers to the InAlAs space layer. Conventional RST devices have a large V_{NDR} of 1- 2 V because of the large conduction band offset between the high mobility channel and the barrier layer [9,10], namely, it is larger than the V_{NDR} of our device. This confirms that the mechanism for our NDR device is the carrier transfer from the high mobility channels to the low mobility channels. The dual channel structure in our device is effective in reduction the V_{NDR} .

4. Conclusion

In conclusion, we demonstrated a new type of VMTs with InGaAs dual channel structures on (001) InP substrates. The VMTs are found to exhibit NDR characteristics with an onset voltage of 0.38 V. The NDR effect can be observed even at 220 K, and the operating current of the VMT is one order of magnitude larger than that of a trench-type QWR-FET. Because the VMTs are simple in the device structure and controllable with the gate bias in a three-terminal configuration, they are favorable for applications to high-frequency, high-speed, and low-power consumption devices with reduced circuit complexity.

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