AFRL-PR-WP-TP-2007-207

1.8 kV, 10 mΩ-cm^2 4H-SiC JFETs (PREPRINT)

James Scofield, Sei-Hyung Ryu, Sumi Krishnaswami, Husna Fatima, and Anant K. Agarwal

JANUARY 2006

Approved for public release; distribution is unlimited.

STINFO COPY

PROPULSION DIRECTORATE
AIR FORCE MATERIEL COMMAND
AIR FORCE RESEARCH LABORATORY
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7251

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
January 2006	Conference Paper Preprint	09/30/2005 – 01/30/2006

4. TITLE AND SUBTITLE
1.8 kV, 10 mΩ-cm^2 4H-SiC JFETs (PREPRINT)

5a. CONTRACT NUMBER
FA8650-04-2-2410

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
62203F

6. AUTHOR(S)
James Scofield (AFRL/PRPE)
Sei-Hyung Ryu, Sumi Krishnaswami, Husna Fatima, and Anant K. Agarwal (Cree, Inc.)

5d. PROJECT NUMBER
3145

5e. TASK NUMBER
13

5f. WORK UNIT NUMBER
OM

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Electrical Technology and Plasma Physics Branch (AFRL/PRPE)
Power Division
Propulsion Directorate
Air Force Research Laboratory, Air Force Materiel Command
Wright-Patterson Air Force Base, OH 45433-7251

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Propulsion Directorate
Air Force Research Laboratory
Air Force Materiel Command
Wright-Patterson AFB, OH 45433-7251

10. SPONSORING/MONITORING AGENCY ACRONYM(S)
AFRL-PR-WP

11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S)
AFRL-PR-WP-TP-2007-207

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
Conference paper submitted to the 2006 Proceedings of the European Conference on Silicon Carbide and Related Materials (ECSCRM 06).

The U.S. Government is joint author of the work and has the right to use, modify, reproduce, release, perform, display, or disclose the work. PAO Case Number: AFRL/WS 06-1794; Date cleared: 27 Jul 2006. Paper contains color.

14. ABSTRACT
Fabrication and characteristics of high voltage, normally-on JFETs in 4H-SiC are presented. The devices were built on 5x10^{15} cm^{-3} doped, 12 μm thick n-type epilayer grown on a n$^+$ 4H-SiC substrate. A specific on-resistance of 10 mΩ-cm^2 and a blocking voltage of 1.8 kV were measured. Device characteristics were measured for temperatures up to 300ºC. An increase of specific on-resistance by a factor of 5 and a decrease in transconductance were observed at 300ºC, when compared to the value at room temperature. This is due to a decrease in bulk electron mobility at elevated temperature. A slight negative shift in pinch-off voltage was also observed at 300ºC. The devices demonstrated robust DC characteristics for temperatures up to 300ºC, and stable high temperature inverter operation in a power DC-DC converter application, using these devices, is reported in this paper.

15. SUBJECT TERMS
Silicon Carbide, power, JFET, dynamic characteristics

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT:	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON (Monitor)
a. REPORT	b. ABSTRACT	c. THIS PAGE			James D. Scofield
Unclassified	Unclassified	Unclassified	SAR	12	19b. TELEPHONE NUMBER *(Include Area Code)* N/A

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std. Z39-18

1.8 kV, 10 mΩ-cm^2 4H-SiC JFETs

James Scofield[1], Sei-Hyung Ryu[2], Sumi Krishnaswami[2], Husna Fatima[2], and Anant K. Agarwal[2]

[1]Air Force Research Laboratory, Wright-Patterson Air Force Base, OH 45433
[2]Cree, Inc., 4600 Silicon Drive, Durham, NC 27703

ABSTRACT

Fabrication and characteristics of high voltage, normally-on JFETs in 4H-SiC are presented. The devices were built on 5x10^{15} cm^{-3} doped, 12 μm thick n-type epilayer grown on a n$^+$ 4H-SiC substrate. A specific on-resistance of 10 mΩ-cm^2 and a blocking voltage of 1.8 kV were measured. Device characteristics were measured for temperatures up to 300^{o}C. An increase of specific on-resistance by a factor of 5 and a decrease in transconductance were observed at 300^{o}C, when compared to the value at room temperature. This is due to a decrease in bulk electron mobility at elevated temperature. A slight negative shift in pinch-off voltage was also observed at 300^{o}C. The devices demonstrated robust DC characteristics for temperatures up to 300^{o}C, and stable high temperature inverter operation in a power DC-DC converter application, using these devices, is reported in this paper.

INTRODUCTION

4H-silicon carbide (4H-SiC) is a material of choice for high performance power switching devices because it offers a very high critical field and a high thermal conductivity. In addition, 4H-SiC has negligible intrinsic carrier generation at temperatures up to 300^{o}C, due to its' large bandgap. This results in very small leakage currents in reverse biased junctions, and enables 4H-SiC devices to operate at much higher temperatures compared to devices in conventional semiconductor materials. Several types of 4H-SiC power devices have been demonstrated [1-3] and characterized at elevated temperatures. Power MOSFETs in 4H-SiC are very attractive devices. However, the operating temperature of a 4H-SiC MOSFET is limited to 200^{o}C due to poor reliability of the gate oxide at elevated temperatures. Bipolar Junction Transistors, BJTs, in 4H-SiC can operate at higher temperatures (300^{o}C) because their operation does not depend on the gate dielectric, but requires a static base current, necessitating a more complex drive circuit. 4H-SiC Junction FETs, JFETs, are viable high temperature alternatives because they are voltage controlled devices without critical gate dielectric functionality. In this paper, we present our latest results in high voltage 4H-SiC JFET development.

DEVICE STRUCTURE AND FABRICATION

Figure 1 shows a simplified cross-sectional view of a JFET cell. Electrons flow from the source contact into the n$^+$ source regions, then flow laterally through the JFET channel. The electrons then flow through vertical JFET regions, which are formed by two adjacent p-well regions, through the lightly doped drift layer, and then finally, to the drain contact. The

thickness of the lateral JFET channel is defined by the thickness of the n-epilayer and the widths of depletion regions formed by the n-channel and p-well (bottom), and the n-channel and top p^+ gate (top). At turn-on, the top gate is shorted to source, and the width of the depletion region is at its' minimum. To turn the device off, a negative voltage is applied to the top gate (with respect to the source) and the depletion expands. The device is completely off when the top depletion region converges with the bottom depletion, pinching-off the n-channel layer.

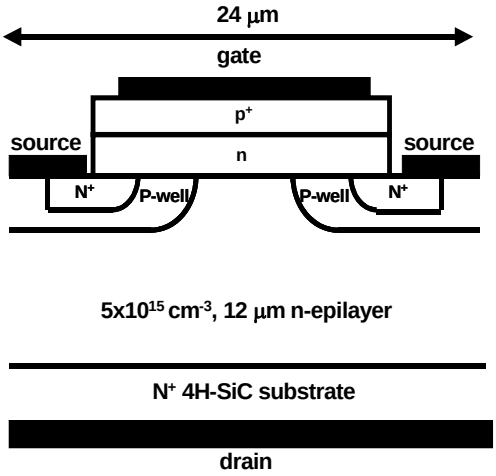

Fig. 1. Simplified cross-sectional view of a 4H-SiC JFET cell.

Devices were fabricated using a 12 μm thick, 5 x 10^{15} cm^{-3} doped n-type epilayer grown on an n^+, 4H-SiC substrate. P-wells and floating guard ring edge termination were formed by Al^+ implantation, and n^+ source regions were then formed by heavy-dose N^+ implantations. The channel length, defined by the distance from the edge of the n^+ source implant to the edge of the p-well implant, was 1 μm. The implants were activated at 1600 ^oC in a silicon-rich ambient. A 0.8 μm thick n-type epilayer with a doping concentration of 1.4 x 10^{17} cm^{-3} was grown as the lateral channel layer, and an Al^+ implantation was done to form top p^+ gate layer and annealed at 1600^oC. The top p+ gate layer concentration was 1 x 10^{19} cm^{-3} and 0.3 μm deep. The p^+ implanted layer and n-channel epilayers were then patterned using a dry etching technique down to n^+ source and p-well implants. A 0.6 μm thick PECVD field oxide layer was then deposited and densified in dry O_2. After opening vias, Al/Ni ohmic contacts were formed on the n^+ source, the p-wells, and the p^+ gates regions, while Ni was used to form backside ohmics. The ohmic contacts were then covered with $TaSi_2$/Pt or Ta-Ru diffusion barrier layers to prevent deterioration of ohmic behavior at elevated temperatures. A 2 μm thick Ti/Pt/Au layer was evaporated and lifted-off to form the metal overlayer. Finally, a 0.3 μm thick Si_3N_4 layer was deposited and patterned for passivation and contact metal oxidation protection.

DEVICE CHARACTERISTICS

Figure 2 shows the on-wafer I-V characteristics of a 4H-SiC JFET, with an active area of 4.65E-2 cm^2, measured at room temperature. Fig. 2(a) shows the pulsed on-state IV characteristics measured using a Tektronix 371A curve tracer. With a V_{GS}=0 V, an $R_{DS,ON}$=0.21 Ω, which corresponds to a specific on-resistance ($R_{on,sp}$) of 10 mΩ-cm^2, was measured. As seen in the figure an I_D=10 A (=215 A/cm^2) was measured at V_{DS}=2.25 V. Although the device appears to be off in Fig. 2(a) when a V_{GS} = –25 V was applied, it needed a gate bias of -30 V for complete shut-off. Fig. 2(b) shows the blocking capability of the device. To prevent arcing in air, the device was immersed in Fluorinert. The device was able to block 1.8 kV with V_{GS} = –33 V, yielding a theoretical E-field in the drift layer of 2.1 MV/cm.

The devices were brazed to TO-258 packages using Au-Ge eutectic preforms. Fig. 3 shows the on-state IV characteristics of a 4H-SiC JFET at 300 ^oC. V_{DS} measured at I_D=5 A (107 A/cm^2) was approximately 5.7 V. $R_{DS,ON}$ measured at a V_{DS}=0.2 V and V_{GS}=0V, increased to 1.07 Ω ($R_{on,sp}$ = 50 mΩ-cm^2), primarily due to a decrease in bulk electron mobility at elevated

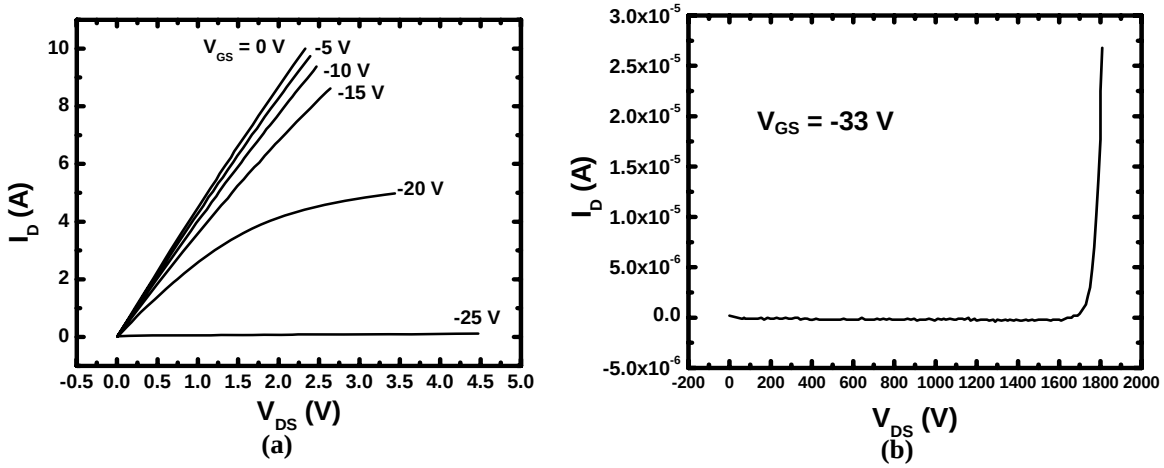

Fig. 2. (a) On-state, and (b) Off-state I-V characteristics of the 4H-SiC JFET. The measurements were done on wafer at room temperature.

temperatures. $R_{DS,ON}$ was measured at temperatures ranging from room temperature to 300 ^{o}C, and is shown as a function of temperature in Fig. 4. $R_{DS,ON}(T)$ was compared to calculated values of $1/\mu_n$ [4]. It can be seen that the on-resistance trend with temperature follows the predicted mobility trend very closely, verifying that the increasing $R_{DS,ON}$ is due to increased drift layer scattering with temperature.

Pinch-off voltage (V_P) and transconductance (g_m) were also measured as functions of temperature. V_P was defined as the V_{GS} required to reducing the drain current to <1 μA at V_{DS}=10 V. At room temperature, a V_P = –26.7 V was measured, which increased to –28.9 V at 300 ^{o}C. This negative shift in V_P is due to an increase in intrinsic carrier concentration (n_i) with temperature. Increased n_i reduces the built-in potential of the pn junction, which results in a reduction in the width of the depletion region and thus, increasing the amount of charge in the channel. To deplete the additional charge, a more negative bias is required on the gate, translating to a larger magnitude pinch-off voltage. The measurements for g_m were done at a V_{DS} = 10 V, and V_{GS} = (V_P + 2V), to ensure that the device is in saturation mode. g_m is a direct function of the electron mobility in the lateral channel ($\mu_{n,channel}$). As expected, the value of g_m decreases as the temperature increases. It should be noted that at 300 ^{o}C, Ron,sp, which is a

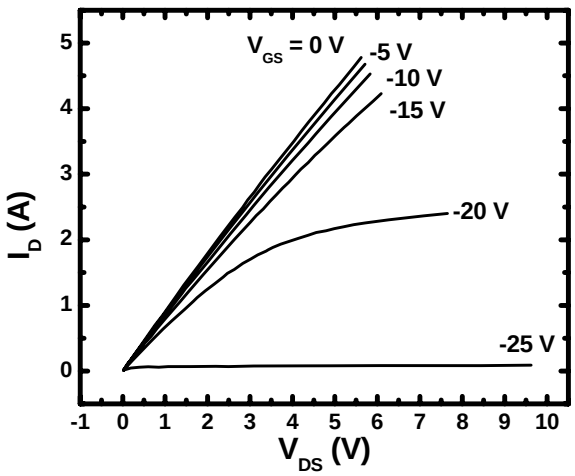

Fig. 3. On-state I-V characteristics of a 4H-SiC JFET at 300 ^{o}C.

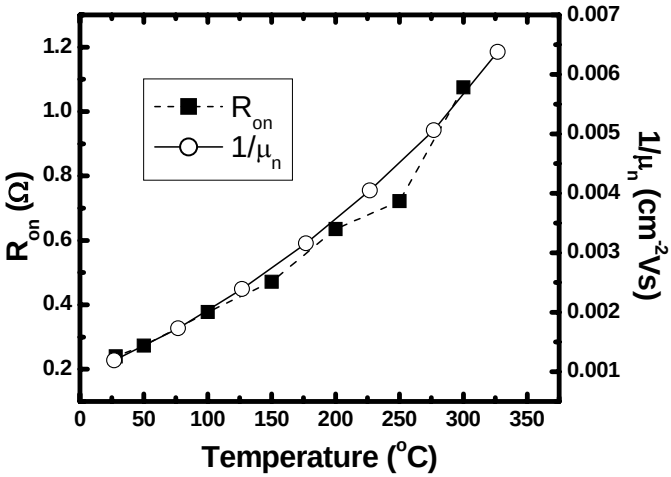

Fig. 4. On-resistance is plotted as a function of temperature. $1/\mu_n$ is also plotted for comparison.

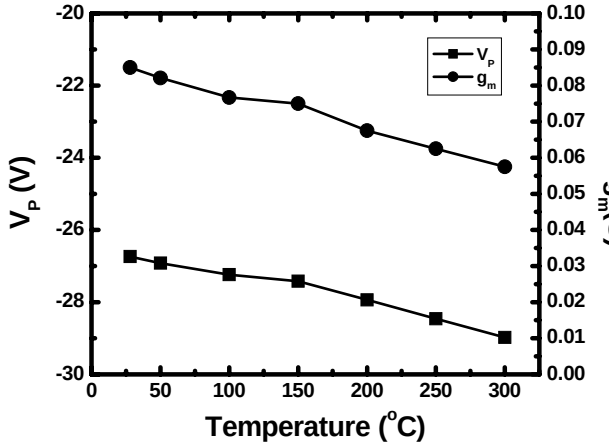

Fig. 5. Pinch off voltage and transconductance plotted as functions of temperature

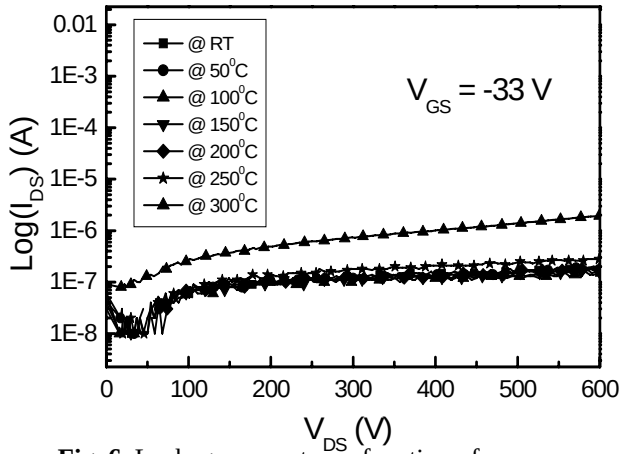

Fig. 6. Leakage current as a function of temperature. A maximum drain bias of 600 V was used, and a V_{GS} of –33 V was used.

function of electron mobility ($\mu_{n,drift}$) in the drift layer, increased by a factor of 5, which means that the value of $\mu_{n,drift}$ was reduced by factor of 5 compared to the value at room temperature. However, g_m was reduced by only a factor of two over the same temperature range, which suggests that the temperature dependence of $\mu_{n,channel}$ is different from that of $\mu_{n,drift}$.

Figure 6 shows the leakage current in the off-state at a V_{GS} of –33 V for temperatures ranging from room temperature to 300 °C. Since the cavity of the package was not filled with an appropriate potting material, the drain voltage was limited to 600 V to prevent arcing. For temperatures up to 250 °C, the leakage current at 600 V remained at around 0.1 μA, which increased to approximately 1.5 μA at 300 °C. Subsequent measurements of package leakage over the same temperature range eliminated the package as a source of the increase in leakage at 300°C. Even with this sudden jump in the leakage current, the leakage current density remains low 32 μA/cm^2. This suggests that the device can be operated at temperatures up to 300 °C.

HIGH TEMPERATURE DC-DC CONVERTER APPLICATION

Subsequent to discrete device characterization, devices were selected for insertion into a 2 kW, 270 – 28 V, DC-DC converter designed for 200°C operation. A simple phase-shifted H-bridge topology is utilized and was built using polyimide 10 oz Cu circuit boards, high temperature powdered-ferrite transformer cores, polyimide wire insulation, and PbSnSb high temperature solder. The rectifier section was built using 300 V, commercially available CREE Schottky diodes, and a custom gate drive circuit was modified for 0 to -36 V operation. Four, 4H-SiC JFETs, described above,

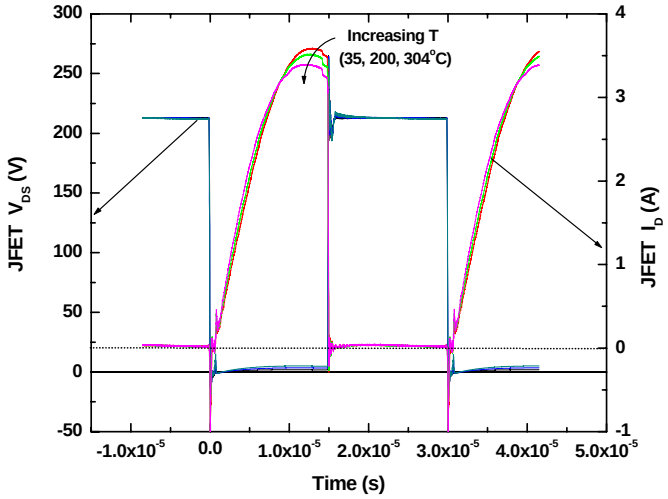

Fig. 7. Current and voltage waveforms for one of the 4H-SiC JFET low-side switches in the converter H-bridge, at 35, 200, and 304°C.

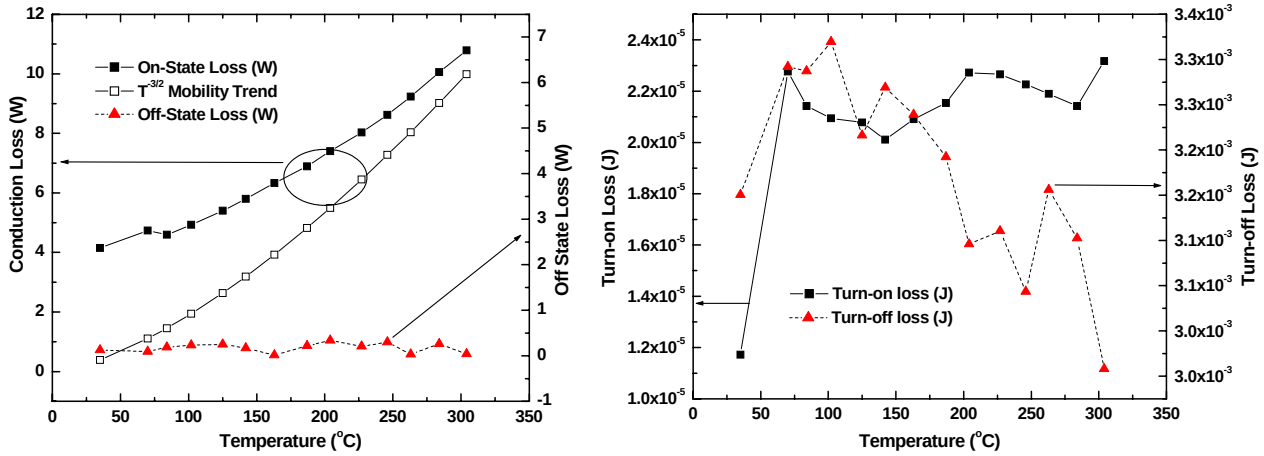

Fig. 8. (a) on-state and blocking conduction losses as f(T), including decreasing mobility trend due to acoustic phonon scattering mechanism, and (b) dynamic loss data as f(T) for JFET turn-on and turn-off.

were used to populate one of the three H-bridge inverter phases for high temperature characterization. This inverter phase was thermally isolated from the remaining 200°C circuit components for testing to 300°C, using a dedicated heat source. Fig. 7 shows the current and voltage waveforms for one of the low-side switches of the SiC JFET H-bridge. The I-V waveforms shown are exciting the transformer primary at 33 kHz switching frequency, 532 W input power, and at 35, 200, and 304°C case temperatures. The converter output is dissipated into a cooled 1Ω wire wound resistor load bank. V_{DS} increases from 1.89 V at 35°C to 5.03 V at 304 °C, owing to the increase in $R_{DS,ON}$ with increasing temperature. The reduction in inverter current from 3.6 A to 3.39 A over the same temperature range is attributable to a decrease in the watt-loss characteristic of the magnetic material used for transformer fabrication and thus, an increase in transformer efficiency. Fig 8a and 8b illustrate the calculation of static and dynamic loss components for the instrumented switch, as a function of temperature, from the measured waveform data. Consistent with the 2.66X increase in V_{DS} over the temperature range of measurement, is the increase in conduction loss from 2 to 11 W. This is in relative agreement with increasing drift layer carrier scattering, due to acoustic phonons, represented by the $T^{-3/2}$

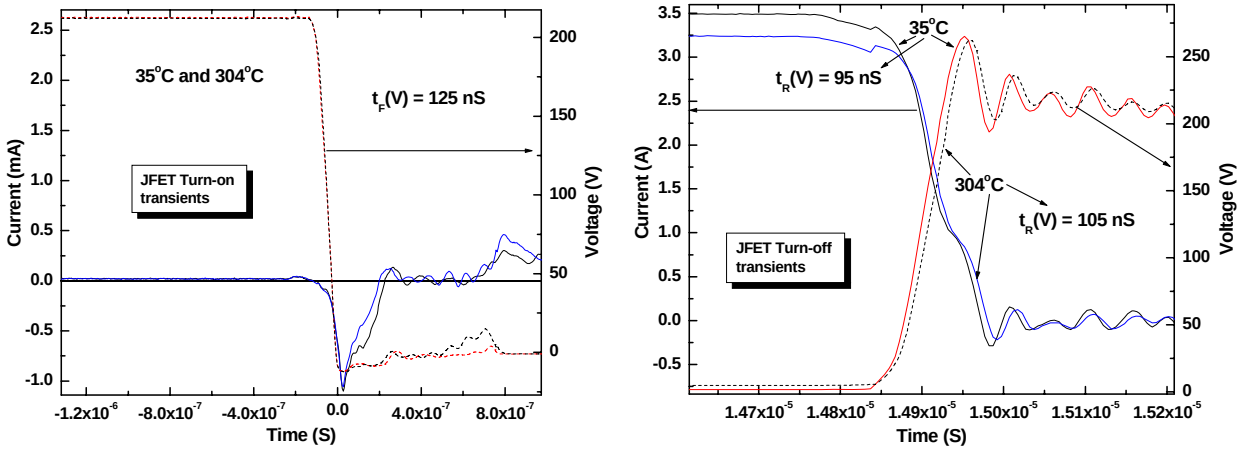

Fig. 9. Turn-on and turn-off waveforms of the SiC JFET H-bridge low-side switch 35 and 304°C

mobility trend impact to drift layer resistance and thus conduction loss, also shown in Fig. 8a. The off-state power dissipation is seen to be invariant with temperature, consistent with the data of Fig. 6, and represents a negligible fraction of the total loss even at 300^{o}C.

Fig. 8(b) illustrates the benefit of the JFETs high speed switching characteristics for both the turn-on and turn-off transients. The dominance of the turn-off energy loss characteristic is due to the inductive transformer load being commutated, resulting in a slow build-up of current during the turn-on transient and throughout the on-state. Fig. 9 is a graphical representation of the turn-on and turn-off dynamic waveforms at 35 and 304^{o}C. As readily seen from the figure, the JFET dynamic characteristics are virtually invariant with temperature and voltage rise and fall times are on the order of 100 and 125 ns, respectively, driving an inductive element.

SUMMARY

1.8 kV, 10 mΩ-cm^2, normally on 4H-SiC JFETs are reported in this paper. Characterization of the devices was performed for temperatures ranging from room temperature to 300 ^{o}C. The specific on-resistance increased from 10 mΩ-cm^2 at room temperature to 50 mΩ-cm^2 at 300 ^{o}C, which agrees with temperature coefficient of bulk electron mobility. However, the transconductance decreased by only a factor of two for the same temperature range, suggesting that the electron mobility in the lateral channel has a different temperature coefficient of that in the drift layer. With –33 V applied to the gate, the device was able to block 600 V with a leakage current density less than 32 μA/cm^2 for all temperatures. Initial characterization of SiC JFET performance in a power converter designed for high temperature operation illustrates the significant performance potential of these devices and SiC in general. These results indicate that SiC-based devices are capable of robust performance in high temperature power applications.

ACKNOWLEDGMENTS

This work is supported by AFRL contract # F33615-01-C-2188, monitored by Dr. J. Scofield.

REFERENCES

[1] S. Ryu, A. Agarwal, J. Richmond, J. Palmour, N. Saks, and J. Williams, " 10 A, 2.4 kV Power DiMOSFETs in 4H-SiC," *IEEE Electron Device Letters*, Vol. 23, No. 6, June 2002. pp. 321-323.

[2] S. Krishnaswami, A. Agarwal, C. Capell, J. Richmond, S. Ryu, J. Palmour, S. Balachandran, T. P. Chow, S. Bayne, B. Geil, K. A. Jones, and C. Scozzie, "1000 V, 30 A SiC bipolar Junction Transistors and Integrated Darlington Pairs," *Materials Science Forum Vols. 483-485*, pp. 879-900.

[3] P. Friedrichs, R. Elpelt, R. Schorner, H. Mitlehner, and D. Stephani, "Optimization of Vertical Silicon Carbide Field Effect Transistors towards a Cost Attractive SiC Power Switch," *Materials Science Forum Vols. 457-460*, pp. 1201-1204.

[4] W. J. Schaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, "Conductivity Anistropy In Epitaxial 6H and 4H SiC," *Mat. Res. Soc. Symp. Proc. Vol. 339 (1994*), pp. 595 – 600.