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Despite a substantial effort in both institutions, we have so not yet reached the initial goal of this project, the demonstration of crested layered barriers suitable for NOVORAM. However, in the course of the work, we have obtained two very encouraging results:

1. We have demonstrated that the developed HfON/Si3N4 and AlOx layers with better tunneling characteristics than the Si02 used in industry for floating-gate (e.g., flash) memories. These materials may enable both better (lower-voltage) flash memories and new scalable floating-gate random access memories with a 10-ns-scale time, over-1-s retention time, and the number of cycles in excess of 1010. We believe that (possibly, after some process improvement) the latter memories may replace DRAM at the 32-nm ITRS technology node and beyond. We are going to pursue this opportunity aggressively.

2. The observed bistability ("memory") effects in double-layer AIOx barriers may be used in prospective nonvolatile "resistive" (or "crossbar") memories with an ultimately small cell footprint. (These observations still need additional confirmation and fabrication technology optimization.)

We believe that these results alone (even leaving aside the important fundamental results on electron transport through nanoscale films) more than justify the human and financial resources invested into this project.

Hw

Final Report

Crested Tunnel Barriers for Fast, Scalable, Nonvolatile Semiconductor Memories

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1. Introduction

The main objective of this project was the experimental demonstration of the theoretically predicted enhanced quantum- mechanical tunneling through layered ("crested") barriers. If demonstrated in silicon-compatible materials with sufficient endurance under electric stress, this effect may enable high-density, high-speed nonvolatile memories that may potentially replace DRAM as the main random access memories of semiconductor electronics. With that objective, we have combined the expertise at Stony Brook University in crested barrier theory (Prof. Konstantin Likharev) and aluminum oxide layer growth (Prof. James Lukens, Dr. Vijay Patel) with that of Yale University (Prof. T.P. Ma, Dr. X. Wang) in jet vapor deposition of silicon nitride and silicon dioxide films, as well as in nonvolatile memory technology. The main results of our effort are listed below.

2. Basic Results

(i) Work at Yale

During the first year of this research project, we demonstrated successful deposition of SiO_2 and Si_3N_4 films by the JVD method, and Al_2O_3 films by thermal oxidation of deposited Al. We measured the electrical properties of these films, and obtained very promising results. However, we encountered a major problem in *I-V* characteristics of our synthesized Si_3N_4 and Al_2O_3 films; i.e., an area factor of many orders of magnitude was required in the theory to quantitatively fit the experimental data. Alternatively, the *I-V* data could be fit perfectly with a theoretical model, which required insertion of a thin but high barrier in between the electrode and the synthesized dielectric film. This mysterious phenomenon had existed and puzzled us for a long time until recently. Because the mismatch between the experimental data and the theory was later found to exist not only for MOS structures with synthesized dielectric films but also for those with thermal SiO_2 (although the degree of mismatch was less), it is likely that the problem may have arisen from several process steps besides film deposition, including, for example, possible formation of a thin layer of aluminum oxide during thermal evaporation of Al electrode. Study along this line has resulted in improved curve fitting of experimental data with theory, both on single-dielectric MOS structures such as $Al/Si_3N_4/Si$, and on one-side crested barrier structure consisting of $Al/(Si_3N_4/SiO_2)/Si$.

In the middle of this research, the JVD machine, which we used to deposit the aforementioned gate dielectrics, became unavailable to us because its owner (which loaned us the machine) decided to take it back. Therefore, we decided to design and construct our own deposition machine. After a year of diligent work, we had completed our own deposition machine, named the "MAD" (Molecular and Atomic Deposition) machine, and started to reproduce the gate dielectrics that we were able to get with the old JVD machine. At the present time, the quality of our MAD silicon nitride is even superior to our high-quality JVD nitride. In addition, with the MAD machine we can also produce HfO_2 with the quality comparable to, or even better than, the state-of-the-art ALD HfO_2.

To make a fair evaluation of our Al/ $HfON/Si_3N_4$ /p^+-Si crested barrier (Fig. 1), we took theoretical *I-V* curve for SiO_2 as the reference to compare with the experimental *I-V* characteristics of such a stack. We found that such a single-side crested barrier already exhibited substantially higher current injection efficiency than what the theory predicted for SiO_2. We then tested this tunnel stack in a simple MONOS type structure and observed faster programming and longer retention as compared to a similar structure where the tunnel barrier was a single layer SiO_2 with similar EOT [19].

In Fig. 2, the solid symbols represent the typical *I-V* characteristics of an $Al/(HfON\text{-}Si_3N_4)/Si$ structure. The black curve (with open symbols) is a simulated *I-V* curve for theoretical SiO_2 with the same EOT. It can be seen clearly that it takes only 3 volts for the crested barrier to achieve 8-orders increase in the current density but 4.2 volts for the SiO_2. The steep JV curve obtained on the $HfON/Si_3N_4$ stack can be attributed to (1) barrier height lowering in the high fields; (2) the high quality of the stack components. As shown in the inset of Fig. 2, this *I-V* curve fits the Fowler-Nordheim tunneling model over 7 orders of magnitude, indicating a nearly trap-free feature of our $HfON/Si_3N_4$ stack. This feature is further evidenced by the temperature independence of the *I-V* curve as shown in Figure 3.

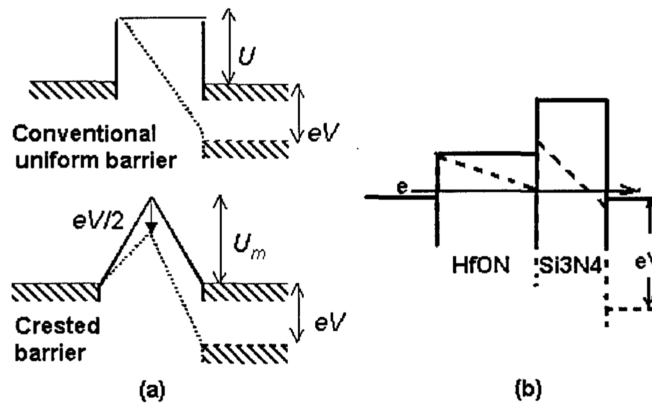

Fig.1 (a) The crested barrier concept, and (b) the conduction band-edge diagram of a $HfON/Si_3N_4$ single-side crested barrier.

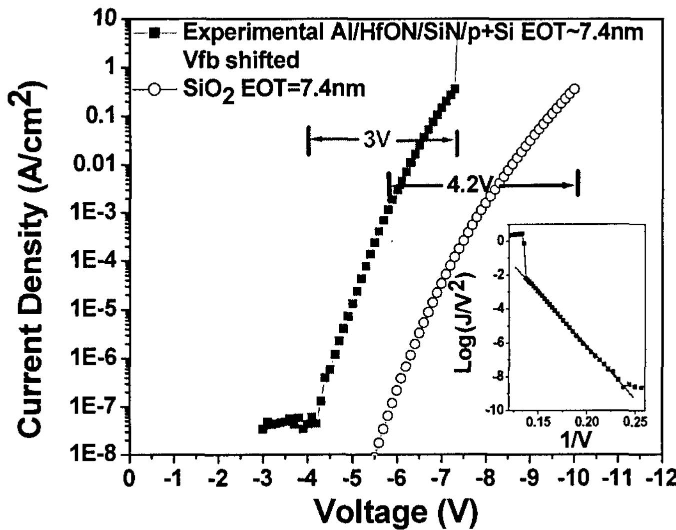

Fig. 2. *I-V* curves of $Al/HfON/Si_3N_4/P^+$-Si stack and theoretical SiO_2. Inset shows the Fowler-Nordheim fitting of the *I-V* curve of the crested barrier.

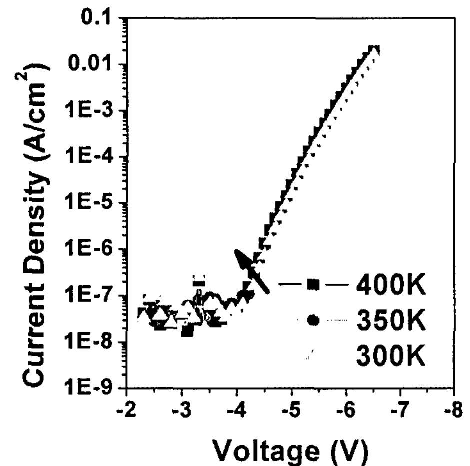

Fig. 3 Temperature dependence of *I-V* curves of the $Al/HfON/Si_3N_4/p^+$-Si stack.

In order to test whether such a steep *I-V* characteristic would lead to a faster programming, we have constructed a demo MONOS-like structure. As depicted in Fig. 4a, $HfON/Si_3N_4$ stack is used as the tunneling dielectric in the test samples while in the control samples (Fig. 4b) a single layer SiO_2 made by the MAD technique is used as the tunnel oxide. Our data (not shown here) indicate that the MAD SiO_2 is in an excellent quality comparable to, or even better than the standard thermal SiO_2. Figure 5 compares the programming speed, while Fig. 6 compares the retention time of the two tunnel dielectrics, where flat-band voltage shifts of the MONOS capacitors were measured to determine the memory window. As expected, the MONOS test cells exhibit faster programming speed, and longer retention than the control cells. The latter is attributed to the thicker physical thickness of the high-k stack than the single SiO_2 with similar EOT. (The apparent high programming voltage in Fig. 5 for both test and control cells should not be a concern as it is solely due to the non-standard structure used in this study.)

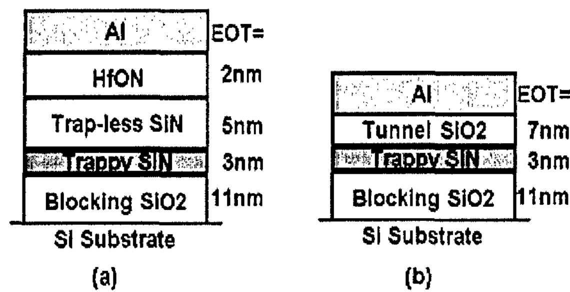

Fig. 4 Structure of MONOS stacks. (a) HfON/Si_3N_4 crested barrier as the tunnel dielectric; (b) SiO_2 as the tunnel dielectric.

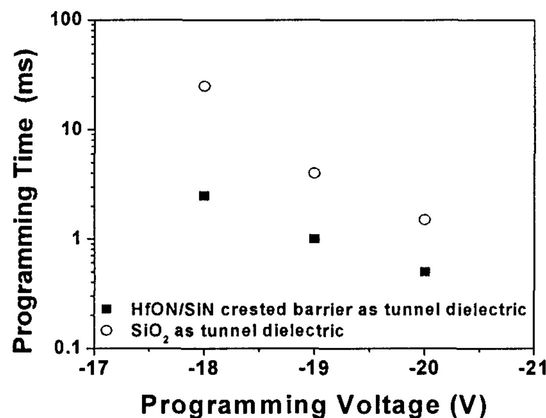

Fig. 5 Programming times of HfON/SiN stack and SiO_2 at different voltages for the same flat-band voltage shift

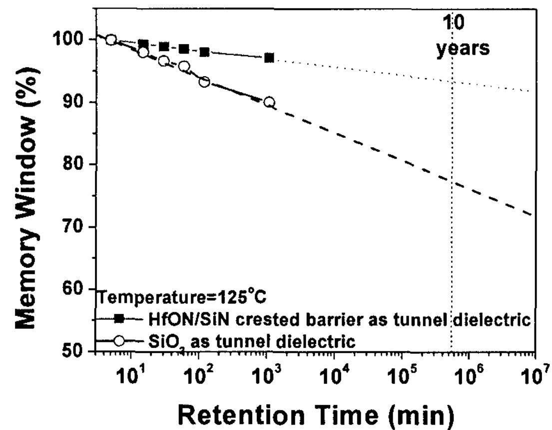

Fig. 6 Retention characterization of MONOS structure with HfON/Si_3N_4 stack or SiO_2 as tunnel dielectric.

During the last year of the project, we also initiated the process development of Al oxide by MAD. Al oxide is known to have higher dielectric constant than SiO_2 and it is considered as a major candidate for the implementation of crested tunnel barriers for nonvolatile memories [6, 7]. The objective of making MAD Al_2O_3 is to make it trap-free so as to maximize the tunneling current in the high fields and minimize the leakage current in low fields. Some preliminary results are shown in Figs. 7 – 10, which represent high quality AlOx / Si interface and very low density of bulk traps. Process optimization and precise physical and electrical characterizations are underway. We are confident that the MAD Al_2O_3 will be soon available to the NOVORAM applications.

(ii) Work at Stony Brook

The main goal of the Stony Brook effort was to evaluate aluminum oxidation techniques as a possible way to obtain high-quality Al_2O_3 layers for crested barriers. We have fabricated and tested several batches of aluminum oxide barrier samples, in order to evaluate parameters of such barriers grown in various oxidation modes. The barriers were parts of Nb-trilayer (Nb/Al/AlO_x/Nb) structures deposited on Si wafers.

For fabrication, a 150 nm Nb film was deposited by dc magnetron sputtering in a cryopumped system with the base pressure of 2×10^{-7} torr. This base electrode was covered by a similarly sputtered Al layer, 8 nm to 10 nm thick. This layer was then oxidized at room temperature in a static dry oxygen atmosphere in the pressure range from 1 to 100 torr for a time interval from 25 minutes to 40 hours to achieve the desired barrier transparency. After pumping down the chamber to the base pressure, a 150

nm Nb counter electrode was sputtered. Wafers were patterned by optical lithography with PMMA resist and reactive ion etching in SF_6 plasma. Each 5×5 mm^2 chip had 18 tunnel junctions with sizes ranging from 3×3 μm^2 to 300×300 μm^2. After the junction etch, the PMMA etch mask was used as a mask to lift off a 150 nm SiO_2 dielectric layer insulating the base electrode from the wiring layer (the so-called self aligned lift-off process). Finally, a 300 nm Nb wiring layer was deposited and patterned using lift-off, with wiring configured to enable four-point measurements.

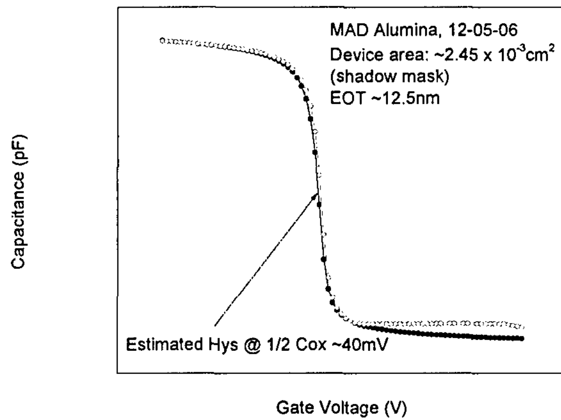

Fig. 7 *C-V* characteristics of an $Al/AlO_x/Si$ capacitor show very small hysteresis window, indicative of very low density of border traps.

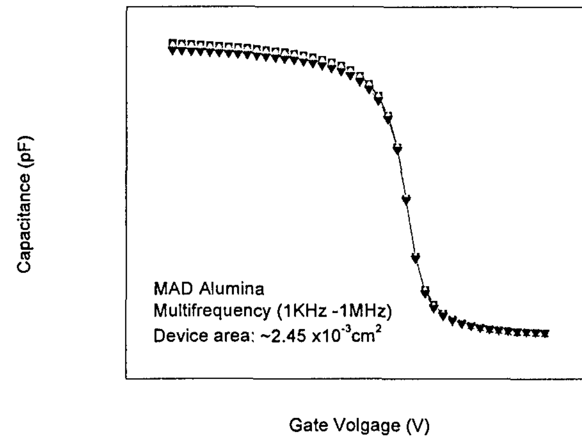

Fig. 8, Multi-frequency *C-V* characteristics of an $Al/AlO_x/Si$ capacitor. The lack of frequency dispersion indicates high quality interface.

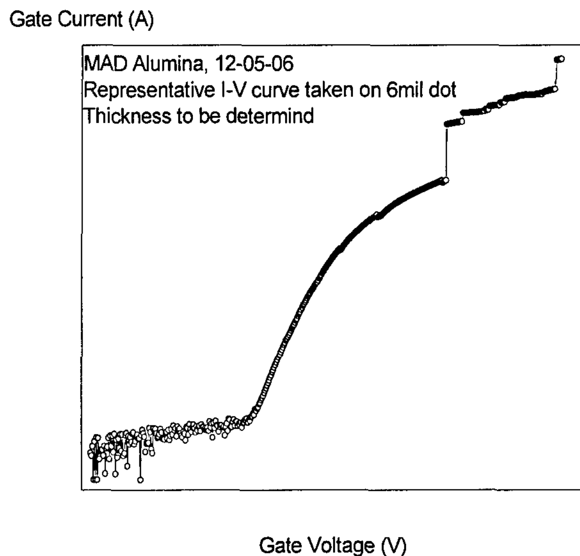

Fig. 9. An example of *I-V* characteristics of an $Al/AlO_x/Si$ capacitor.

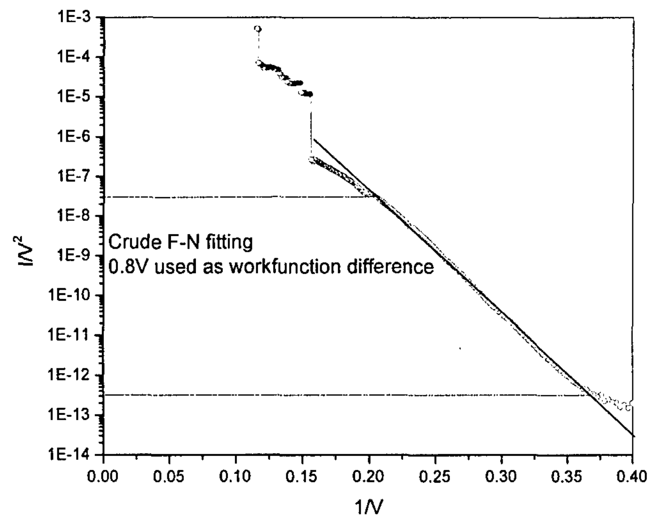

Fig. 10. Fowler-Nordheim fitting of the *I-V* curve shown in Figure 9.

Transport measurements were done using the a specially designed automated system which allowed to measure currents in a large dynamic range (from ~10^{-13} A to 10^{-2} A) at arbitrary temperatures from 4.2 K to 300 K.

Table 1 shows the full list of fabricated wafers, listing the fabrication conditions and experiment purpose, while Table 2 briefly summarizes their transport properties.

Table 1

Wafer	Oxide Type	Base Electrode		Al interlayer nm	Oxidation			Purpose
		Metal	Thickness nm		Pressure mTorr	Time min	Power W	
CB1	Plasma	Nb	125	6	15	10	50*	PO
CB2	Plasma	Nb	125	6	15	10	50*	PO
CB3	Plasma	Nb	100	6	75	10	50*	PO
CB4	Thermal	Nb	50	3	100000	50	-	TO
CB6	Plasma	Nb	50	6	15	3	50*	PO
CB7	Plasma	Nb	50	5	15	30	50*	PO
CB11	Thermal Plasma	Al	50	- 3	100000 15	50 10	- 50*	Bilayer TO+PO
CB12	Plasma	Al	50		15	10	50*	Calibration
CB13A	Plasma	Al	50		15	10	50	Calibration
CB13B	Plasma	Al	50		15	10	50	Calibration
CB14	Plasma	Nb	50	6	15	10	50	Calibration
CB15	Thermal Plasma	Al	50	~3.8	100000 15	40 10	- 50	Bilayer TO+PO
CB16	Plasma Thermal	Al	50	~1.5	15 100000	10 40	50 -	Bilayer PO+TO
CB17	Plasma	Al	50		15	10	10	Power dep.
CB18	Plasma	Al	50		15	10	100	Power dep.
CB19A	Plasma Thermal	Al	50	~3.0	15 100000	10 40	50 -	PO+TO w/ thick Al

*Fabricated using an old power system. All other samples were fabricated in a new system with an automated rf power control.

Table 2

Wafer	Breakdown @ 300 K (V)	Breakdown @ 4.2K (V)	G_0 @ 300 K (S/m^2)	G_0 @ 4.2K (S/m^2)
CB1	--	4.09 ±0.13	0.71	0.34
CB2	--	3.93±0.13	0.19	0.13
CB6	2.48±0.11	4.05±0.24	0.63	0.26
CB7	2.7	4.18	0.25	0.013
CB12	2.7	3.93	0.3	0.1
CB13A	3.76	4.27±0.06		0.003
CB13B	3.41±0.05	4.1±0.3	0.004	0.003
CB13B RTA 400C 30s	3.0	4.5	0.008	0.0026
CB14	2.5	4.42±0.06	0.0053	0.0023
CB16	3.0	4.0	0.018	0.0009
CB16 RTA 400C 30s	3.0+	4.5	0.0015	0.0009
CB15	2.7	4.11	6.45E-3	1.43E-3
CB17	-	-	1000.7	804.2
CB18	3.19	4.5	2.47E-2	8.4E-4
CB19A		4.0		1.16E-3

1. Uniform AlO_x barriers

Most uniform barriers, fabricated by either thermal or plasma oxidation, after appropriate RTA processing, have shown extremely high quality, as characterized by:

- high (~8 orders of magnitude) change of effective conductance by applied electric field,
- high (>10 MV/cm) breakdown field, and
- weak (below one order of magnitude) change of conductance between 4.2 K and 300 K.

The rapid thermal annealing decreases the conductance of thermally-oxidized junctions rather substantially, while that of plasma-oxidized junctions changes much less. Fitting of the *I-V*-curves by theoretical curves calculated from the microscopic theory of direct quantum-mechanical tunneling has allowed to identify this conductance suppression with the growth of the tunnel barrier height (Fig. 11), most probably by the formation of the γ-Al_2O_3 phase.

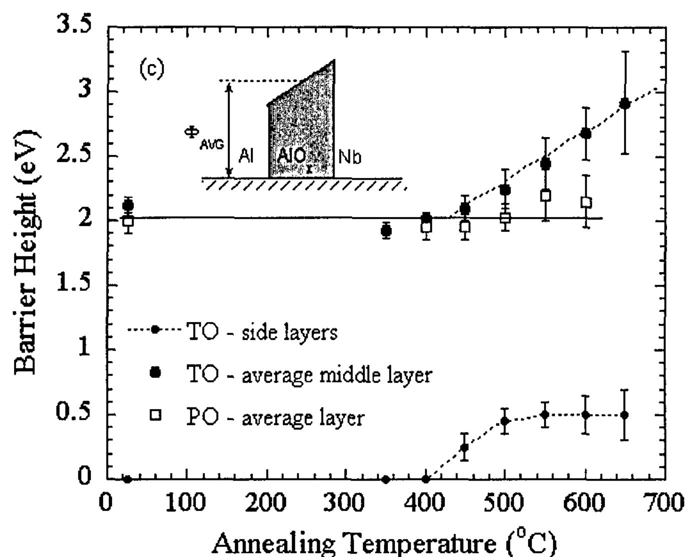

Fig. 11. Change of the barrier height of the thermally grown (TO) and plasma-grown (PO) aluminum oxide layers.

Despite the faster growth of the barrier in thermally-oxidized layers, their conductance remains too low for the advanced memory applications, so that our Phase II effort has been focused mostly on plasma-oxidized junctions whose conductance may be substantially suppressed by the increase of rf discharge power. For example, junctions on wafer CB18 have (at room temperature) the low-voltage specific conductance G_0 of the order of 3×10^{-2} S/m^2. At the same time, specific capacitance C_0 of such junctions is close to 1×10^{-2} F/m^2 [7]. This means that if such junctions are used to insulate a floating gate in a typical flash-like memory cell [1, 2], its retention time $\tau_R \cong C_0/G_0$ will be above 1 sec, quite sufficient for a periodic refresh similar to used in present-day DRAM. On the other hand, at high voltages ~3 V (but still below the breakdown – see Table 2), the effective specific conductance of such junctions is close to 10^5 S/m^2, enabling the floating gate recharging as fast as in ~10 ns. Such speed is sufficient to challenge the current DRAM technology.

The feature critical for this potential application is the junction endurance under high electric stress. It is usually characterized by the so-called charge-to-breakdown *CBD*, defined as the product $I_W t$ (where t is the time before a junction, carrying high current I_W, suffers an irreversible change of transparency), or alternatively by the potential number of write-erase cycles, $N = CBD/C_0V_W$, where V_W is the applied (high) voltage. We have carried out extensive measurements of these parameters; the results are summarized in Figs. 12 and 13.

Figure 12 shows that for the best of our samples the charge-to-breakdown may be as high as 10^6 Coulomb per cm^2, the which compares very favorably with ~10^1 C/cm^2 typical for SiO_2 layers used in flash memories. Figure 13 shows that these barriers may combine >10^{11} write/erase cycles with 10-ns-scale

write time. We are confident that these results may be further improved by the optimization of the plasma and RTA parameters. In particular, our resources have been insufficient to optimize the RTA time.

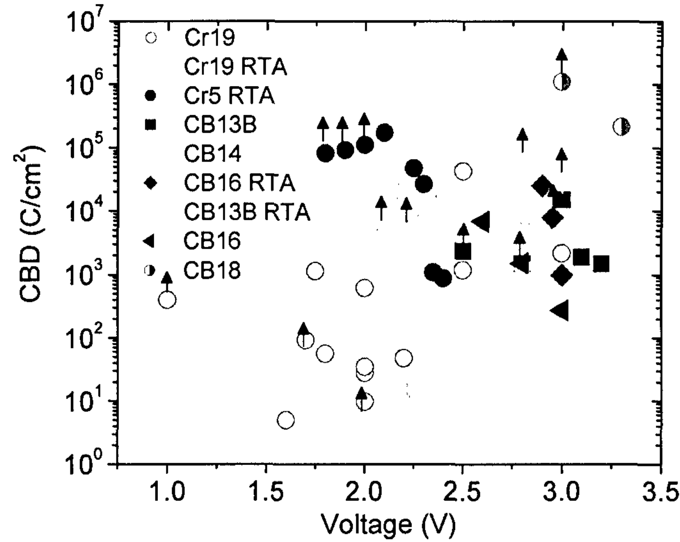

Fig. 12. Charge to breakdown (per unit area) as a function of applied voltage, for several samples fabricated at different conditions (see Table 1). Arrows mean the lower bound points.

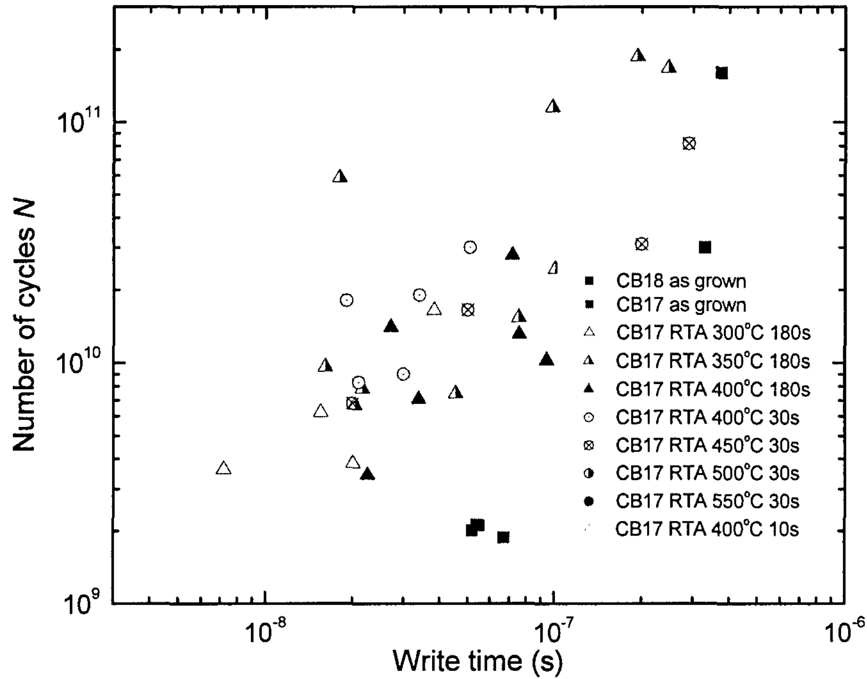

Fig. 13. The maximum number of write-erase cycles, defined by Eq. (1), as a function of the write time scale $\tau_W \equiv C_0 V_W / I_W$, for several junctions from wafers CB17 and CB18, with various RTA time and temperatures.

2. Layered AlO_x barriers

Our attempts to implement the basic idea of crested barriers [1, 2] by deposition have been generally less successful. For example, Fig. 14 shows the $G(V)$ curves of a typical sample from Wafer

CV15 on which the formation of a thermal oxide layer was followed by the deposition of ~4nm of new aluminum and its plasma oxidation. The plots show that transport properties of the junctions are virtually identical to those of the similar plasma oxide layer alone (Wafer CB13A). We interpret these data as a result of dissolving of the thermal oxide by energetic oxygen atoms of the plasma discharge.

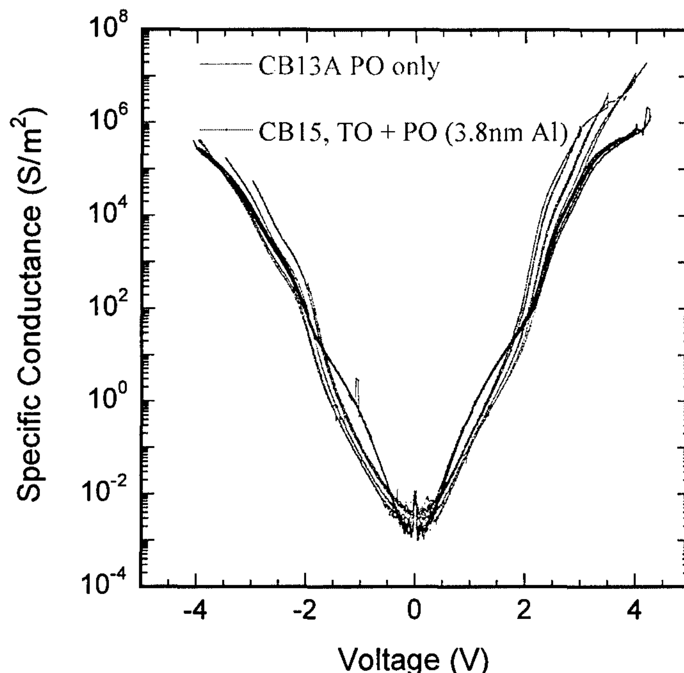

Fig. 14. $G(V)$ for a typical sample of Wafer CB15 (thermal oxide followed by plasma oxide), compared with Wafer CB13 (plasma oxide alone).

An alternative way toward layered barriers is to form the plasma oxide layer first, and then form a TO layer by thermal oxidation of a very thin (~1.5 nm) additional layer of aluminum. Figure 15 shows results from Wafer 16 fabricated in this way (for fabrication parameters, see Table 1). One can see that the transport is again similar to that through the plasma oxide alone, and the conductance is much higher than that expected from theory (blue curve) in assumption that the two oxides layers were just superposed on each other.

Most probably, these results may explained by the granular character of the second (ultra-thin) aluminum layer. (Unfortunately, the layer cannot be made thicker because of rapid saturation of the thermal oxidation process.) If these grains are well separated, the transport should be dominated by the area between them, and thus be close that in through the plasma oxide layer alone.

This interpretation has found an indirect confirmation in the experiment with one of a few good wafers (#388) from HYPRES, with a similar PO/TO structure – see Fig. 16. Junctions from this wafer (before the RTA) has shown strong bistability ("memory") effects, similar to those observed recently by other groups in metal-oxide layers [8-15]. The physical mechanism of this bistability s not yet clear, but for the currently most reproducible metal-oxide devices it is probably due to electron trapping in localized states [16].

This effect has the key importance for the implementation of the so-called "resistive" (or "crossbar") memories which may have the smallest cell footprint (at fixed design rules) [17]. Recently we have shown [18] that the hybrid (CMOS/nano) version of the resistive memories, using the "CMOL" interface suggested in our group, may enable circuit integration scales approaching 1 Tbit/cm^2, at sub-100-ns access time and large (>10%) defect tolerance.

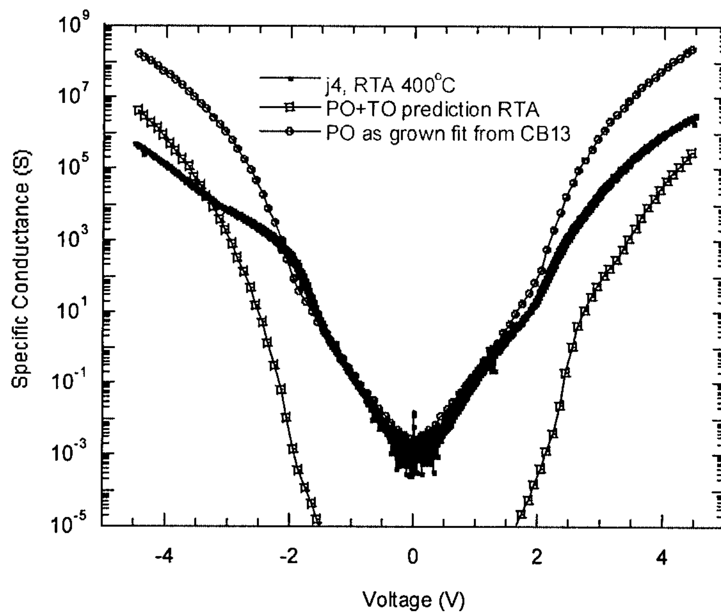

Fig. 15. $G(V)$ curve for a typical sample of Wafer CB16 (plasma oxide followed by thermal oxide), compared with Wafer CB13 (plasma oxide alone).

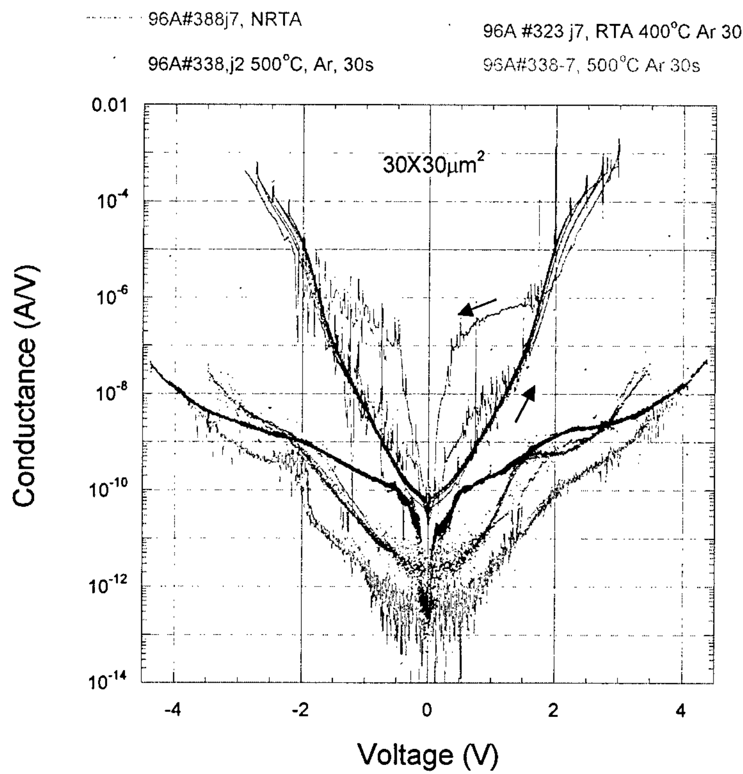

Fig. 16. $G(V)$ curves of the virgin (red lines) and annealed samples from HYPRES Wafer 388. Arrows show the direction of the voltage sweep.

(iii) Conclusion

Despite a substantial effort in both institutions, we have so not yet reached the initial goal of this project, the demonstration of crested layered barriers suitable for NOVORAM. However, in the course of the work, we have obtained two very encouraging results:

1. We have demonstrated that the developed HfON/Si_3N_4 and AlO_x layers with better tunneling characteristics than the SiO_2 used in industry for floating-gate (e.g., flash) memories. These materials may enable both better (lower-voltage) flash memories and new scalable floating-gate random access memories with a 10-ns-scale time, over-1-s retention time, and the number of cycles in excess of 10^{10}. We believe that (possibly, after some process improvement) the latter memories may replace DRAM at the 32-nm ITRS technology node and beyond. We are going to pursue this opportunity aggressively.

2. The observed bistability ("memory") effects in double-layer AlO_x barriers may be used in prospective nonvolatile "resistive" (or "crossbar") memories with an ultimately small cell footprint. (These observations still need additional confirmation and fabrication technology optimization.)

We believe that these results alone (even leaving aside the important fundamental results on electron transport through nanoscale films) more than justify the human and financial resources invested into this project.

4. References

[1] K. K. Likharev, "Layered tunnel barriers for nonvolatile memory devices". *Appl. Phys. Lett.*, vol. 73, pp. 2137-2139, May 1998.

[2] K. K. Likharev, "NOVORAM: A new concept for fast, bit-addressable nonvolatile memory based on crested barriers". *IEEE Circuits and Devices*, vol. 16, pp. 16-21, Apr. 2000.

[3] S. J. Baik , S. Choi, U-I. Chung, and J. T. Moon, "Engineering on tunnel barrier and dot surface in Si nanocrystal memories", *Solid-State Electronics*, vol. 48, pp. 1475–1481, Sep. 2004.

[4] S. H. Hong, J. H. Jang, T. J. Park, D. S. Jeong, M. Kim, C. S. Hwang, and J. Y. Won, "Improvement of the current-voltage characteristics of a tunneling dielectric by adopting a Si_3N_4 /SiO_2/Si_3N_4 multilayer for flash memory application", *Appl. Phys. Lett.,* vol. 87, pp. 152106 1-3, Oct. 2005.

[5] B. Govoreanu, P. Blomme, J. Van Houdt, and K. De Meyer, "Enhanced tunneling current effect for nonvolatile memory applications", *Jpn. J. Appl. Phys.*, Part 1, vol. 42, pp. 2020–2024, Apr. 2003.

[6] S. K. Tolpygo, E. Cimpoiasu, X. Liu, Yu. A. Polyakov, J. E. Lukens, and K. K. Likharev, "Tunneling Properties of Barriers in Nb/Al/AlO_x/Nb Junctions" *IEEE Trans. on Appl. Supercond,*vol..13, pp. 99-102, Jun. 2003.

[7] E. Cimpoiasu , S. K. Tolpygo, X. Liu, Yu. A. Polyakov, J. E. Lukens, and K. K. Likharev, "Aluminum Oxide Layers as Possible Components for Layered Tunnel Barriers", *J. Appl. Phys*, vol. 96, pp. 1088-1093, Jul. 2004.

[8] For the review of early results, see, e.g., G. Dearnaley, A. M. Stoneham, and D. V. Morgan, *Rep. Prog. Phys.*, "Electrical phenomena in amorphous oxide films", vol. 33, pp. 1129-1200, 1970. References 9-15 below are to the most recent work.

[9] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D.-S. Suh, Y. S. Young, I. K. Yoo, I. R. Hwang, S. H. Kim, I. S. Byun, J.-S. Kim, J. S. Choi, and B. H. Park, "Reproducible resistance switching in polycrystalline NiO films", *Appl. Phys. Lett.*, vol. 85, pp. 5655-5657, Dec. 2004.

[10] I. G. Baek, D. C. Kim, M. J. Lee, H.-J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O. Park, H. S. Kim, I. K. Yoo, U-In Chung, J. T. Moon and B. I. Ryu, "Multi-layer cross-pint binary oxide resistive memory (OxRRAM) for post-NAND storage applications", *IEDM'05 Tech. Digest*, 31.4, 2005.

[11] D. C. Kim, S. Seo, S. E. Ahn, D.-S. Suh, M. J. Lee, B.-H. Park, I. K. Yoo, I. G. Baek, H.-J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U-I. Chung, J. T. Moon, and B. I. Ryu, "Electric observations of filamentary conductions for the resistive memory switching in NiO films", *Appl. Phys. Lett.*, vol. 88, pp. 202102 1-3, May 2006.

[12] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Wasser, B. Reichenberg, and S. Tiedke, "Resistive switching mechanism of TiO_2 thin films grown by atomic-layer deposition", *J. Appl. Phys.*, vol. 98, pp. 033715 1-8, Aug. 2005.
[13] D. Lee, H. Choi, H. Sim, D. Choi, H. Hwang, M.-J. Lee, S.-A. Seo, and I. K. Yoo, "Resistance switching of the non-stoichiometric zirconium oxide for nonvolatile memory applications", *IEEE Electron Device Lett.*, vol. 26, pp. 719-721, Oct. 2005.
[14] H. Sim, D. Choi, D. Lee, M. Hasan, C. B. Samantray, and H. Hwang, "Reproducible resistance switching characteristics of pulsed laser-deposited polycrystalline Nb_2O_5", *Microelectron. Eng.*, vol. 80, pp. 260-263, Jun. 2005.
[15] A. Chen, S. Haddad, Y.-C. Wu, T.-N. Fang, Z. Lan, S. Avanzino, S. Pangrle, M. Buynoski, M. Rathor, W. Cai, N. Tripsas, C. Bill, M. VanBuskirk, and M. Taguchi, "Non-volatile resistive switching for advanced memory applications", *IEDM'05 Tech. Digest*, 31.3, 2005.
[16] J. G. Simmons and R. R. Verderber, "New conduction and reversible memory phenomena in thin insulating films", *Proc. Roy. Soc. A*, vol. 301, pp. 77-102, 1967.
[17] J. C. Scott, "Is there an immortal memory?", Science, vol. 304, pp. 62-63, Apr. 2004.
[18] D. B. Strukov and K. K. Likharev, "Architectures for defect-tolerant nanoelectronic crossbar memories", *J. of Nanoscience and Nanotechnology*, vol. 7, pp. 151-167, Jan. 2007.
[19] Y. Liu, S. I. Shim, F. C. Yeh, X. W. Wang, and T.P. Ma, "Barrier Engineering for Non-Volatile Memory Application", to be published (2007).