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An 18-GHz, 10.9-dBm Fully-Integrated Power Amplifier with 23.5% PAE in 130-nm CMOS

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Abstract:

An 18-GHz fully integrated class-E power amplifier with 10.9-dBm saturated output power, and 23.5-% maximum PAE is fabricated in the UMC 130-nm digital CMOS process. At the saturated output, the required input power level is -5dBm and PA consumes 35mA from V_{DD}=1.5V. The amplifier is single-ended and includes a 2-stage pre-amplifier and a driver stage. A mode-locking technique exploiting the instability of driver amplifier is used to improve the drive for the gate of output stage. The mode-locking improves PAE by ~3% and reduces the required input power level by ~6dB to get same output level.

1. Introduction

Commensurate with the proliferation of wireless communication networks, there is constantly increasing demand for compact, low-cost and low-power portable devices. This has motivated the research of single-chip transceivers realized in low-cost CMOS technology (μNode) [1]. For the frequency bands around or above 10GHz, research efforts have mainly focused on receivers. Especially, high efficiency MOS power amplifiers (PA's) operating at frequencies around or above 10-GHz have received little attention, and still remain as a challenging RF block [3][4].

The power consumption of PA is the dominant component of total transmitter power consumption, making the PA efficiency crucial. Compared with linear power amplifiers, which are optimized for maximum gain and linearity, a switching class-E power amplifier provides much higher efficiency. Class-E PA's are particularly well suited for modern communication systems using constant envelope modulation schemes, such as the Zigbee wireless personal area networks (WPAN'S) and GSM cellular networks. This work describes an 18-GHz CMOS PA with 10.9-dBm saturated output power, which achieves maximum power added efficiency (PAE) of 23.5%. The input driving requirement of the large output stage in the PA is relaxed by using the mode-locking technique [6],[7]. The inherent instability of the driver circuit is exploited to eliminate the need for an addition of intentional positive feedback. The 10.9-dBm saturated output power is sufficient for the 1-5 m range applications proposed for the single chip transceiver [1],[2].

2. Circuit Design

Figure 1 shows the circuit schematic of power amplifier. It consists of a two-stage cascode amplifier, a common source driver, and a output stage. Due to the limited voltage headroom, common-source amplifiers are used in the last two stages. The cascode amplifiers are used to provide sufficient gain, good input matching and isolation from the last two stages which potentially could oscillate.

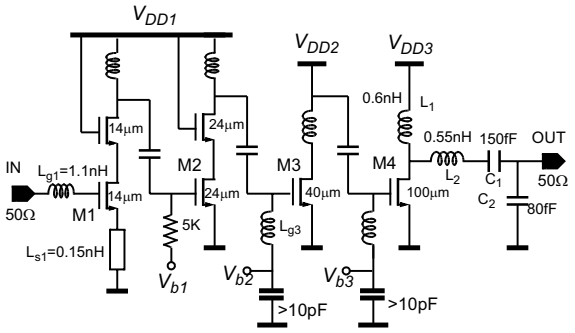

Figure 1. A schematic of the fully-integrated CMOS PA

2.1 Extended Transistor Model

Near 20GHz, the impact of series resistance and parasitic capacitance from the metal lines for making connections to transistors becomes more significant [5]. Figure 2 shows the extended NMOS transistor model used to design the PA's. It includes a foundry BSIM3v3 model and the elements to model the parasitics associated with the metal lines and substrate. The series inductive elements of transistors are smaller than that from metal interconnects and are included in the interconnect models in the design. The layout details have major impact on the parasitic elements, so models are extracted for fixed layouts. For the PA transistor, the gate finger width is 1μm and the finger is contacted on two ends. Since the source is grounded, the source length is increased from the 0.4-μm minimum to 0.56μm. This increases the separation between drain and source metal interconnects and that between the source metal interconnect and polysilicon

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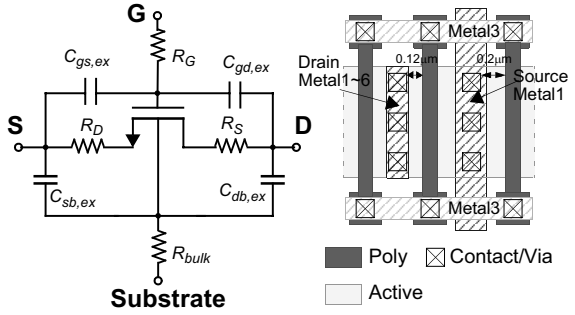

Figure 2. A transistor layout and an extended NMOS transistor model including additional parasitic elements

gate, which reduce the parasitic capacitances. The extracted values from the measured S-parameters of a 14-μm wide transistor show an effective substrate resistance of 42Ω. The C_{db} and C_{sb} were 70% larger than that due to the transistor core and while the C_{gd} and C_{gs} was nearly 50% higher. To take these into account, external parasitic capacitors are added to the transistor model as shown in Figure 2.

2.2 Class-E Output Stage

Normally, a class-E amplifier is treated as a switch, so that current and voltage are never appreciable at the same time. To achieve this, the matching network component (L_1, L_2, C_1, C_2) values have to be properly selected as described in [7],[8]. To lower the matching network loss, the inductors L_1 and L_2 are formed with the top two copper layers, which results an effective thickness of 1.6μm. The metal traces are 3.6-μm wide and 4-μm above the polysilicon patterned ground shield. The effective series resistance of two inductors is about 5Ω, which is the main source of loss for the matching network. A shunt inductor (L_g) is placed at the gate of output transistor to tune out the gate capacitance, which reduces the loss through the coupling capacitor, but as will be discussed below, also makes the circuit more potentially unstable.

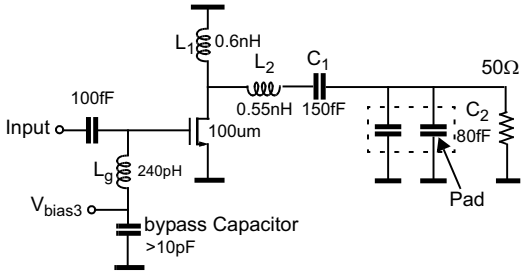

Figure 3. output matching network.

2.3 Stability and Mode Locking Technique

Near 20GHz, the common-source driver stage is unstable due to the feedback through C_{gd}, which is one of the reasons for the wide use of cascode amplifiers. Figure 4 shows the simplified small signal model of the common-source amplifier, which includes a transconductor and two resonant networks connected by C_{gd}.

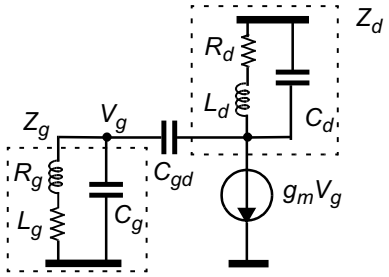

Figure 4. small signal model of common source amplifier

Due to C_{gd}, the output of the amplifier is fed back to the input. The open loop gain of this circuit is,

$$T(s) = \left(-g_m\left(Z_d \| \left(Z_g + \frac{1}{sC_{gd}}\right)\right)\right) \bullet \left(\frac{Z_g}{Z_g + 1/(sC_{gd})}\right) \qquad (1)$$

This expression consists of two parts: the gain from the gate to drain and voltage divider for the feedback path. To start oscillation, the loop gain should be larger than 1 and the phase change must be 360 degree. For the network at the gate node, below its resonant frequency, the network is inductive with an equivalent inductor $L_{g,equ}$ and a series resistor $R_{g,equ}$. The transfer function of the voltage divider between C_{gd} and the network is

$$\frac{j\omega L_{g,equ} + R_{g,equ}}{j\omega L_{g,equ} + R_{g,equ} + 1/(j\omega C_{gd})} = \frac{-\omega^2 L_{g,equ} C_{gd} + j\omega C_{gd} R_{g,equ}}{1 - \omega^2 L_{g,equ} C_{gd} + j\omega C_{gd} R_{g,equ}} \qquad (2)$$

When $\omega L_{g,equ} >> R_{g,equ}$ or Q is high, at frequencies below $1/\sqrt{L_{g,equ} C_{gd}}$, this voltage divider provides a phase shift close to 180 degree. Meanwhile, when $\omega L_{g,equ} << R_{g,equ,}$ it gives a phase shift of 0 to 90 degree. To satisfy the oscillation condition, the first term in Eq. (1) needs to provide 180 degree phase shift or the tank at drain node must resonate at the oscillation frequency, and the second term must provide another 180 degree phase shift. Therefore, the resonant frequency of $L_{g,equ}$-C_{gd} circuit is set higher than the oscillation frequency and the high Q inductive load at the gate node is used.

The output stage is designed to drive 50-Ω load, so the voltage gain is not high. On the other hand, the driver stage is designed to achieve high voltage gain. Because of this, it is easier to make the driver stage oscillate. To provide good input matching, two stage cascode amplifiers are used at the input. The gates of the common-gate transistors are connected to a bypass capacitor right beside the transistors to make the cascode stage stable [3].

The instability is generally undesired in power amplifiers. However, if the self-oscillation can be locked by the input, the instability actually increases the gain of the circuit and reduces the drive requirement for switching the output transistor. This is called mode-locking (also known as injection-locking) and has been previously utilized in power amplifiers [6],[7]. Usually, cross-coupled transistors are used to provide the positive feedback (or negative resistance). Since the driver in this work is

unstable, additional positive feedback is not included. To study the benefits of mode-locking, a power amplifier without mode-locking is also implemented. This is accomplished by removing the gate inductor of the driver stage (L_{g3} in Figure 1). In addition, a 3-kΩ resistor is added for dc biasing.

3. Measurement Results

The power amplifier was fabricated in the UMC 130-nm logic CMOS process with eight copper layers and a substrate resistivity of 20Ω·cm. The two power amplifiers are fabricated side by side for comparison. Figure 5 shows the die photograph of the two single-ended power amplifiers. The two amplifiers together occupy an area of 0.92mm x 0.85mm including bond pads.

The large signal measurements were performed using the setup shown in Figure 6. The output is connected to a power meter with an HP8495A 50MHz-26.5GHz power sensor. The losses of measurement setup are de-embedded using a thru-measurement. The loss at the output end (from the probe and short SMA cable) of ~0.7dB at 18 GHz was measured with a network analyzer. An Agilent E4448A 3Hz-50GHz spectrum analyzer is also used to monitor the output spectrum of power amplifier.

With 1.5-V supply voltage and proper gate bias (0.5~0.7V), the power amplifier shows self-oscillation with ~1-dBm peak power near 17.4GHz. As the input signal level is increased, the self-oscillation becomes weaker until finally the circuit is forced to oscillate at the same frequency as the input. Figure 7 shows the output spectrum with 17.6 GHz input. With -42-dBm input power level, the self-oscillation cannot be locked, and the self-oscillation peak and inter-modulation products are shown beside the main peak. At -36-dBm input power, the circuit locks to the input signal. Figure 7(b) shows that the output power is more than 10dBm when input power is -10dBm. When the input frequency is farther away from the self-oscillation frequency, the circuit becomes more difficult to be locked. At -10-dBm input power level, the circuit can be locked from 15.5GHz to 21.4GHz. In addition, when a 20-GHz -10-dBm FM signal with 16-MHz maximum frequency deviation and 1kbps to 1Mbps data rate is used as input, the PA locked to the input, while preserving the shape of spectrum [6],[7]. A drawback of the circuit is that the minimum output power level is above 2dBm when the PA is locked. If an output level below this is desired, the bias voltage can be lowered, making the oscillator easier to lock or stop the oscillation. The self-oscillation disappears when the gate bias of the driver stage is below 0.45V.

At 18 GHz, with -5-dBm input power, a single-ended output power of +10.9dBm is obtained while drawing 35mA from a 1.5-V supply. The maximum power added efficiency including all the amplifiers and driver is 23.5%. The last stage consumes 22mA. At 1.2V supply, the PA provides 7.5-dBm saturated output power and 18.6% maximum PAE, while drawing 24.5mA current. The results for the PA without mode-locking is also shown in Figure 8. This PA achieves 10.2dBm peak output power and 20.5% maximum PAE at 20GHz. Because the gain is lower, it requires ~6dB higher input power to get output of 9dBm. The use of mode-locking technique leads to slightly larger saturated output power and effi-

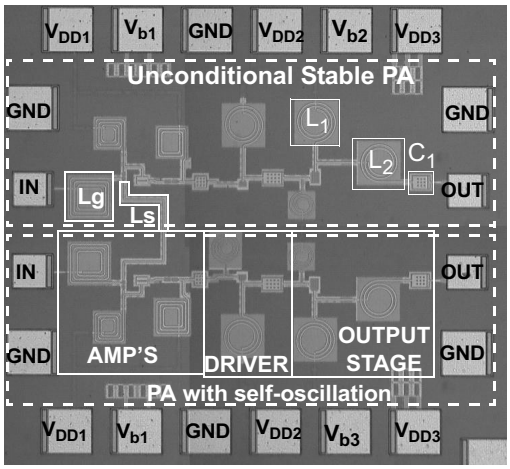

Figure 5: Die micrograph of the two single-ended power amplifiers. Chip size: 0.92mm x 0.85mm

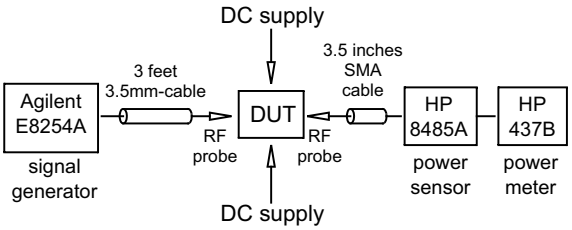

Figure 6. PA measurement setup

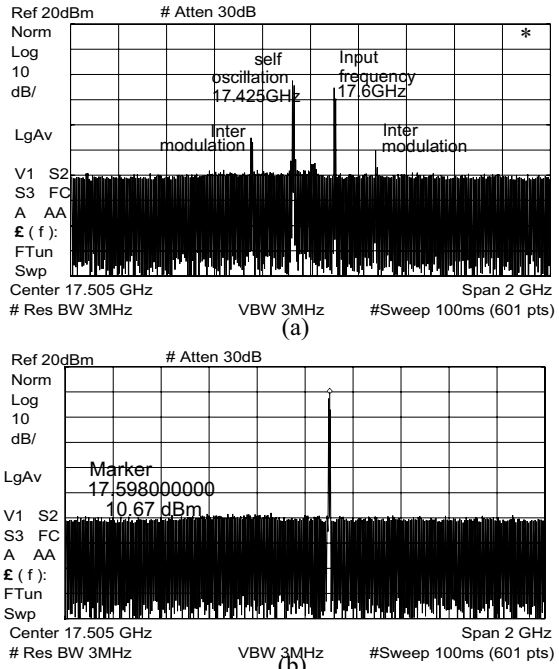

Figure 7: Output spectrum (a) unlocked, input:-42dBm (b) locked, input: -10dBm. (losses from the cable and connector have been de-embedded in these plots)

ciency. More importantly, it reduces the input power requirement of class-E amplifier. Figure 9 shows the saturated output power and PAE from 15.5GHz to 23GHz at 1.5V supply. The PA with mode-locking provides more than 8-dBm saturated output power over a 5-GHz band.

To evaluate the reliability, the power amplifier is stressed for 3 hours at 0-dBm 18-GHz input power (corresponding to the saturated output power with 50-Ω termination) and V_{DD}=1.5V, while the output is terminated with open. The PA survived this testing without any performance degradation. This ability to survive large voltage stress maybe due to the fact that the voltage across gate oxide is clamped to ~2.4V or 0.4V below the gate oxide breakdown voltage by the V_{DS} breakdown of transistors. These suggest that the PA could reliabily operate even when the output is mismatched, however, more studies are needed.

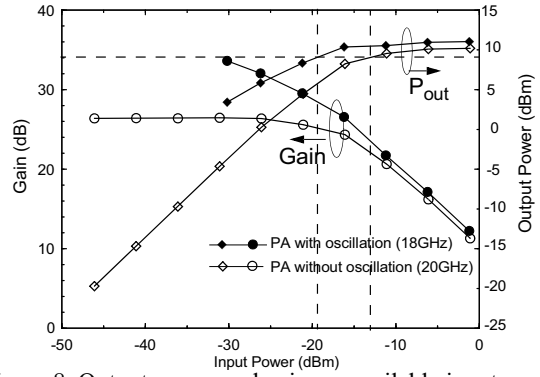

Figure 8. Output power and gain vs. available input power at V_{DD}=1.5V.

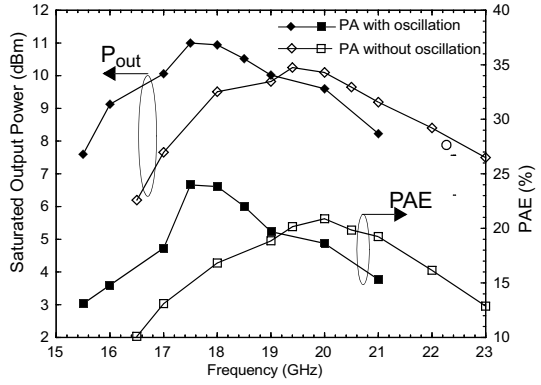

Figure 9. Saturated output power and PAE vs. frequency at V_{DD}=1.5V

4. Conclusions

An 18-GHz 10.9-dBm class-E power amplifier with 23.5% maximum PAE is demonstrated in the UMC 130-nm CMOS technology. The mode-locking technique is used to force the oscillating driver to follow the input signal. The performance of power amplifier in this work is compared to that of the previously reported power amplifiers operating near 20GHz in Table 1. The PA presented in this paper shows significantly higher efficiency and lower input requirement than that for the previously reported CMOS PA operating near 20GHz. This work suggests CMOS technology is a viable candidate for building fully-integrated transmitter near 20GHz.

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Ref	Freq.	Technology	Classification	V_{dd}	Small Signal Gain	P_{out}	Output	PAE
This work	18GHz	0.13µm CMOS	Class-E	1.5V	>30dB	10.9dBm	single-ended	23.5%
This work	20GHz	0.13µm CMOS	Class-E	1.5V	26dB	10.2dBm	single-ended	20.5%
[2]	24GHz	0.18µm CMOS	N/A	2.8V	7dB	14.5dBm	single-ended	5~6%
[8]	24GHz	0.13µm GaAs pHEMPT	Class-E	N/A	N/A	18dBm	Differential	26%

Table 1. Comparisons of power amplifiers operating near 20GHz