AFRL-ML-WP-TP-2007-419

PERFORMANCE AND RF RELIABILITY OF GaN-ON-SiC HEMTs USING DUAL-GATE ARCHITECTURES (PREPRINT)

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JULY 2006

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MATERIALS AND MANUFACTURING DIRECTORATE
AIR FORCE RESEARCH LABORATORY
AIR FORCE MATERIEL COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7750

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
July 2006	Conference Paper Preprint	07/12/2006 – 07/12/2006

4. TITLE AND SUBTITLE
PERFORMANCE AND RF RELIABILITY OF GaN-ON-SiC HEMTs USING DUAL-GATE ARCHITECTURES (PREPRINT)

5a. CONTRACT NUMBER
FA8650-05-C-5411

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
62102F

6. AUTHOR(S)
R. Vetury, J.B. Shealy, D.S. Green, J. McKenna, J.D. Brown, K. Leverich, P.M. Garber, and M.J. Poulton

5d. PROJECT NUMBER
4348

5e. TASK NUMBER
71

5f. WORK UNIT NUMBER
71100300

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
RFMD Infrastructure Product Group, Inc.
10420 Harris Oaks Blvd., Suite A
Charlotte, NC 28269-7513

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Materials and Manufacturing Directorate
Air Force Research Laboratory
Air Force Materiel Command
Wright-Patterson AFB, OH 45433-7750

10. SPONSORING/MONITORING AGENCY ACRONYM(S)
AFRL-ML-WP

11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S)
AFRL-ML-WP-TP-2007-419

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES
Conference paper submitted to the Proceedings of the 2006 International Microelectronics Symposium.
This work was funded in whole or in part by Department of the Air Force contract FA8650-05-C-5411.
PAO Case Number: AFRL/WS 06-0307, 06 Feb 2006.

14. ABSTRACT
AlGaN/GaN HEMTs on SiC have been fabricated with dual and single gate device geometries. Sub-threshold characteristics and drain bias dependence of large signal parameters were compared to identify differences in electric field. Degradation under RF stress reveals the relative impact of temperature and electric field. The results illustrate the beneficial effects of the dual gate geometry for performance and reliability.

15. SUBJECT TERMS
GaN, SiC, HEMT, Dual Gate, Cascode

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT:	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON (Monitor)
a. REPORT	b. ABSTRACT	c. THIS PAGE			John D. Blevins
Unclassified	Unclassified	Unclassified	SAR	10	19b. TELEPHONE NUMBER *(Include Area Code)* N/A

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std. Z39-18

Performance and RF Reliability of GaN-on-SiC HEMTs using Dual-Gate Architectures

R. Vetury, J.B. Shealy, D. S. Green, J. McKenna, J. D. Brown, K. Leverich, P. M. Garber, M.J. Poulton

***Abstract* — AlGaN/GaN HEMTs on SiC have been fabricated with dual and single gate device geometries. Subthreshold characteristics and drain bias dependence of large signal parameters were compared to identify differences in electric field. Degradation under RF stress reveals the relative impact of temperature and electric field. The results illustrate the beneficial effects of the dual gate geometry for performance and reliability.**

***Index Terms* — GaN, SiC, HEMT, Dual Gate, Cascode**

I. Introduction

Recently, AlGaN/GaN-based HEMT technology has emerged as a promising candidate for high efficiency, high power applications such as wireless base stations [1-3]. The competitive advantages of GaN HEMTs result from the material properties of the GaN/AlGaN material system and advantages afforded by various heterostructures possible in this material system [4-6].

Circuit parameters such as high bandwidth, low output capacitance and lower thermal resistance (due to SiC substrate) have contributed to the attractiveness of GaN-on-SiC HEMT technology for infrastructure power amplifiers [7]. Despite these advantages over incumbent Si-LDMOS or GaAs technology, control of the electric field profile by design of appropriate device structures still plays a critical role in determining the influence of traps as well as the reliability performance of GaN HEMTs [8].

Previously, dual-gate GaN HEMTs on sapphire have been reported for use as broadband amplifiers [9,10]. Further, cascode-connected GaN HEMTs have been shown to exhibit higher linear gain compared to a common source device [11].

In this paper, we present a comparison of the dc and RF characteristics of single gate and dual gate devices. We explore the sub-threshold characteristics of the device as a means to identify differences in electric field profile between the structures. The impact of the differences in electric field profile on CW output power at 2.14GHz is investigated by comparing CW loadpull measurements taken at drain voltages up to 60V. The degradation under RF stress under varying conditions of temperature and drain bias was investigated.

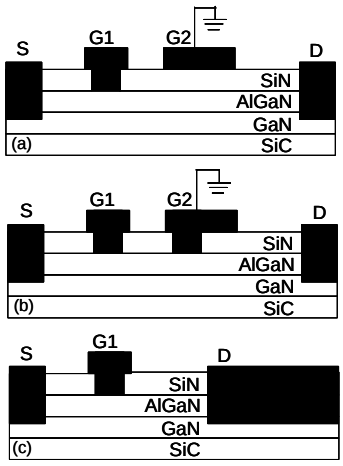

Figure 1. Cross Section of AlGaN/GaN devices investigated: (a) dual-gate HEMT with single-recess (DG-SR), (b) dual-gate HEMT with double recess (DG-DR) , (c) single-gate (SG) HEMT (control device).

II. Dual Gate HEMT Design and DC Characteristics

Figure 1 shows a schematic cross section of the device structures studied in this work. Three different gate structures were designed, namely, standard single gate control devices, dual gate devices with the second gate (G2) being either a Schottky gate structure on GaN surface (DG-DR) or a MIS gate structure on top of SiN dielectric (DG-SR). The second gate (G2) is dc and RF connected to source. All device structures were fabricated in the same process flow on the same epitaxial material structure.

Figure 2 presents a comparison of the transfer characteristics of the three device structures obtained at 10V V_{ds}. As can be seen, the threshold voltage is similar for all three device structures, while for positive gate biases, they exhibit different saturated drain current values. As expected, the DG-DR structure exhibits different saturation behaviors at Vg=0V, due to the presence of the second Schottky gate, which is tied to the ground potential, while the DG-SR structure has a slightly lower value of saturated drain current compared to the control SG structure, due to existence of SiN dielectric under G2 for DG-SR structure.

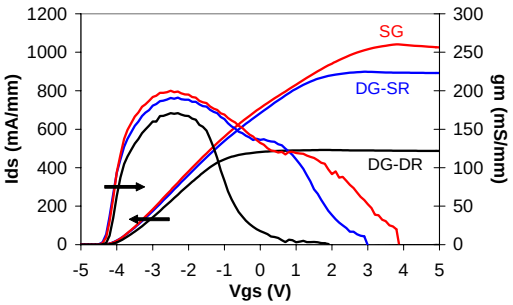

Figure 2. I_d and g_m versus V_{gs} (V_{ds}=10V) for (a) DG-SR HEMT, (b) DG-DR HEMT, (c) SR HEMT (control device).

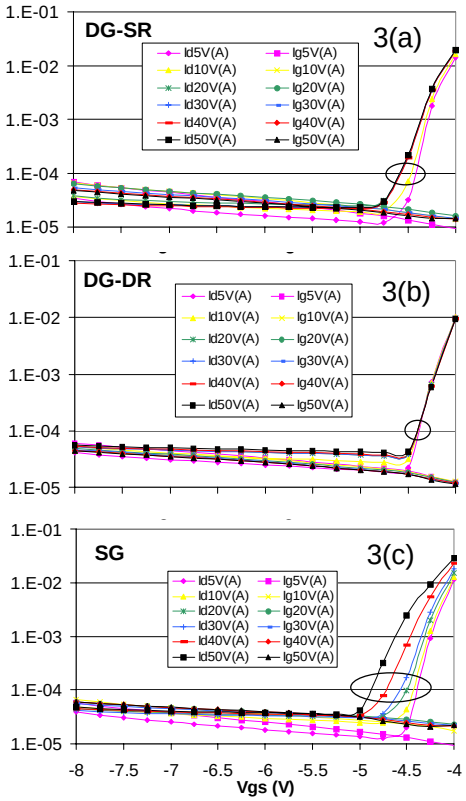

Figure 3. Sub-threshold currents versus V_{ds} from V_{ds}=5V to 50V for (a) dual-gate HEMT with single-recess, (b) dual-gate HEMT with double recess, (c) single-gate recessed HEMT (control device).

For each device structure, the subthreshold characteristic was measured at different V_{ds} (5V to 50V). The increase of I_d with V_{ds} in the subthreshold regime (defined here as: I_d within 0.1mA/mm to 1mA/mm) is directly related to the increase of electric field at the source due to current continuity. Therefore, the spread in V_{gs} for a fixed I_d as a function of increasing V_{ds} indicates the extent of penetration of the drain induced electric field into the source region. This behavior is quantified by measuring the shift in V_{gs} (ΔV_{gs}) to maintain I_d at 0.1mA/mm as V_{ds} is increased from 5V to 50V (as explained in Fig 4(a)). This metric, ΔV_{gs}, is shown for different device structures as measured on several samples in Figure 4(b).

This result indicates that the extension of the electric field to the source in reduced by the DG-SR structure and is further reduced by the DG-DR structure. This is consistent with a model that proposes that the second gate shapes the electric field, and that the magnitude of this effect is related to the proximity of the second gate to the channel.

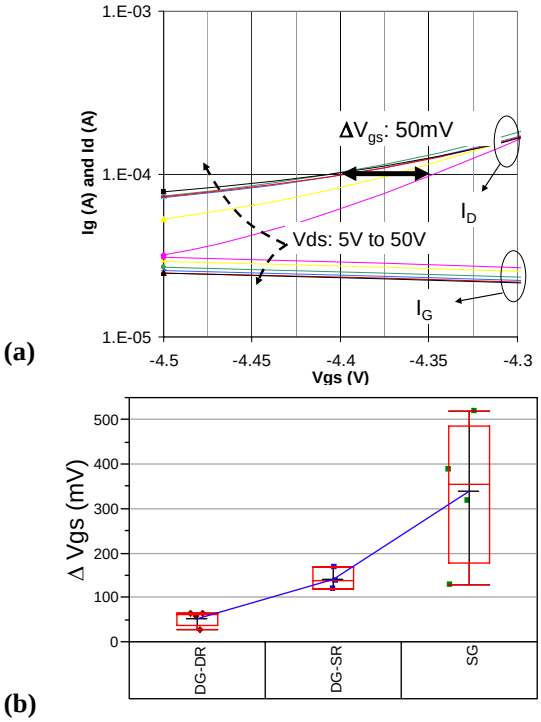

Figure 4. Comparison of spread in gate voltage (ΔV_{gs}) required to achieve 1e-4 A of sub-threshold drain current for three gate structures. Each data point represents a device, with data from several devices of each structure type across a wafer being shown in the graph above.

III. Large Signal Characteristics and Comparison

CW load-pull measurements at 2.14GHz were conducted for drain bias voltages of 28V, 48V, and 60V. Representative large signal characteristics are shown in Fig 5. The data shown in Fig 5 is obtained at drain bias of 48V and quiescent drain current of 0.1A/mm. Table 1 summarizes the key performance parameters for the three structures. The DG-DR and DG-SR structures have ~3dB higher small signal gain, as expected due to the decreased input capacitance and enhanced output conductance of these structures versus a single gate structure. The DG-DR structure has the highest PAE at V_{ds}=28V, however, the P_{sat} (defined as the Pout at maximum PAE) is approximately half the P_{sat} of the DG-SR and SG devices structures. This reduction in P_{sat} for the DG-DR structure is consistent with

the decreased value of $I_{d,max}$. The P_{sat} and PAE are plotted as a function of V_{ds} in Fig. 6. For all three gate structures, P_{sat} increases for increasing V_{ds} from 28V to 60V. However, the P_{sat} is seen to increase linearly with V_{ds} for the DG-SR structure, while the increase is sub-linear for both the SR and DG-DR structures. The PAE increases across the drain voltage range for the DG-SR structure while the PAE decreases for the SR and the DG-DR structures.

The observed behavior of the output power and efficiency can be explained by the relationship between the gate geometry and the resulting injection of electrons from the drain edge of the gate. The SG device suffers from the high peak field at the edge of the gate. The DG-DR device has the benefit of reduced field at G1, but has high peak electric field at the edge of G2. The DG-SR geometry has the advantage of field shaping, but without the degrading effect of charge injection from the edge of G2. The improvement in field profile without the charge injection from G2 is the reason for the advantageous relationship between PAE and drain voltage for the DG-SR device.

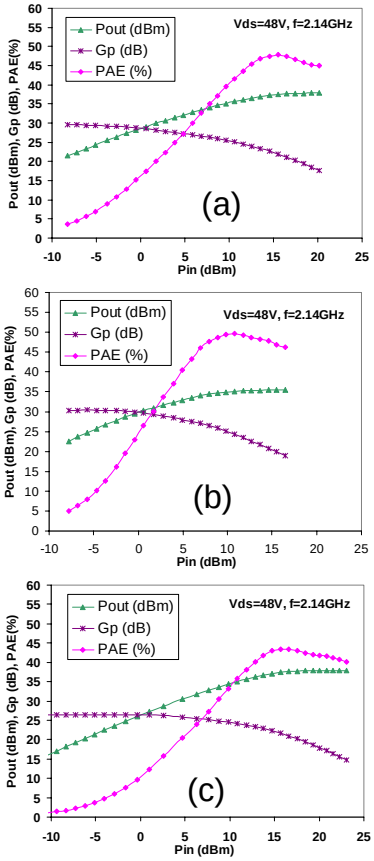

Figure 5. Large signal loadpull results at V_{ds}=48V for (a) dual-gate HEMT with single-recess, (b) dual-gate HEMT with double recess, (c) single-gate recessed HEMT (control device).

Table 1. Large Signal Power Summary

Vds (V)	Gt (dB)	Peak PAE (%)	Psat (W/mm)	Structure Type
28	24.9	46.8	4.0	SG
48	22.0	43.5	6.9	
60	24.5	45.6	7.2	
28	30.3	53.4	2.7	DG-DR
48	29.5	49.7	4.0	
60	30.0	46.2	4.2	
28	27.6	44.7	4.1	DG-SR
48	28.4	47.9	7.0	
60	29.7	50.0	8.7	

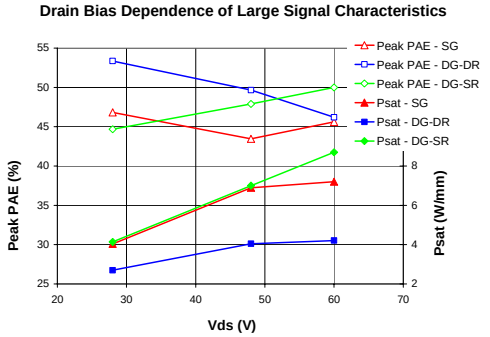

Figure 6. Drain bias dependence of key large signal parameters versus V_{ds}.

IV. Reliability under RF Stress

RF stress measurements were performed using a manually tuned load pull system with microwave probes on singulated die mounted to a substrate. The devices were biased to a specified V_{ds} and a quiescent drain current of 0.1 A/mm. The RF input power was subsequently increased to achieve an output power density of 2.5 W/mm. The gate current, drain current, and output power were then measured as a function of time for a fixed input power. The SR and DG-SR devices were measured for V_{ds}=28V at room temperature and the results can be seen in Fig. 7. After an initial burn-in period of ~1 hour, the devices were both seen to be stable with an output power drop less than 0.2 dB over 15 hours. Due to the performance advantages of the DG-SR device as a function of V_{ds}, and the expected reduction of the peak electric field, this structure was further studied for more stringent stress conditions.

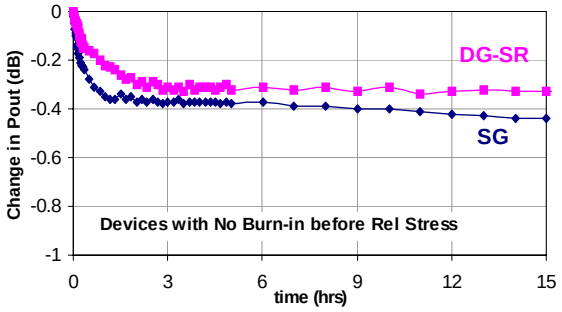

Figure 7. Change in Pout at 60V RF stress at room temperature for dual-gate HEMT with single-recess, and single-gate recessed HEMT (control device).

The impact of increasing electric field as compared to increasing operating temperature was compared for two typical devices with the DG-SR structure. The first device was subject to a stepped RF stress where V_{ds} was stepped up to 60V over a period of 24 hours. Subsequently, the output power was monitored over 250 hours at room temperature. The second device was biased at V_{ds}=30V but the base plate temperature was increased to 200°C and subjected to the same RF stress conditions over 250 hours. The graphs of output power and gain versus time can be seen in Fig. 8. From this comparison, the increase of operating temperature is clearly seen to have a stronger reliability impact as the degradation at higher field and room temperature.

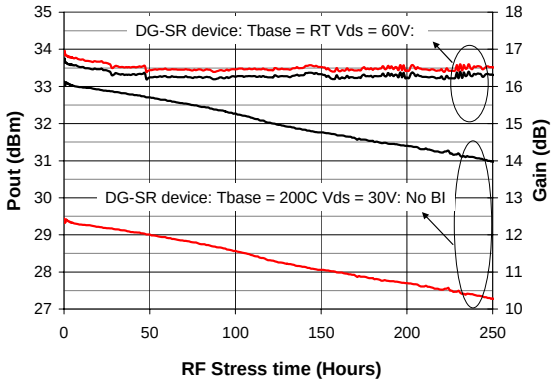

Figure 8. RF stress on the DG-SR structure for Vds=60V at room temperature and Vds=30V at baseplate temperature of 200°C.

The final parameter studied was the impact of a burn-in procedure on the RF output power stability over time. A DG-SR device was put through a thermal and electrical burn-in procedure and then subjected to RF stress at V_{ds}=30V and a base plate temperature of 175°C. The comparison of the device stressed without burn-in at 200°C and the device stressed with burn-in at 175°C can be found in Fig. 9. From this data, the burned-in device appeared to have significantly better output power stability over time. The exact mechanism for this stabilization is under study.

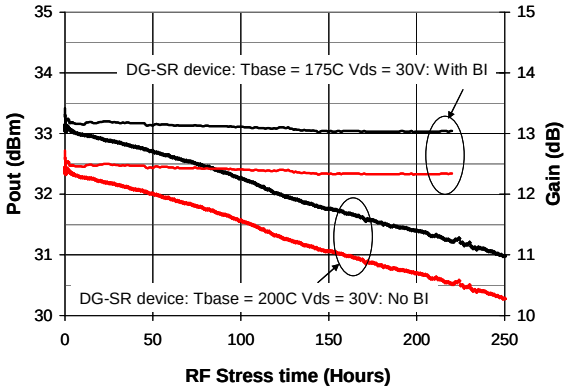

Figure 9. Impact of burn-in on elevated temperature RF stress degradation characteristic of dual gate-single recess device (DG-SR) structures:

VII. Conclusion

AlGaN/GaN HEMT device structures with field modifying gate geometries have been fabricated, characterized, and RF stressed. The results of this work support the hypothesis that both device performance and device degradation under stress are strongly affected by the strength of the peak electric field in the gate-drain region of the HEMT. The performance improvement is illustrated by the scaling of PAE with V_{ds} for the DG-SR geometry. This further advantage of this geometry is seen in the limited degradation displayed under RF stress conditions.

VIII. ACKNOWLEDGEMENTS

RFMD acknowledges support for GaN technology development from Harry Dietrich and Paul Maki at ONR.

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