STANDARD-CELL, OPEN-ARCHITECTURE POWER CONVERSION SYSTEMS

—Final Report—

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EXECUTIVE SUMMARY

This Final Report compiles all the work carried out at the Center for Power Electronics Systems (CPES), corresponding to the "Standard-Cell, Open-Architecture Power Conversion Systems" project sponsored by the Office of Naval Research (ONR). This project was purposefully aimed to develop a standardized hierarchical design and analysis methodology for modular power electronics conversion systems using as basis the ISO/OSI seven layer reference model. The foundational ideas of this engineering vision came from the Power Electronics Building Block (PEBB), seeking to expand the usage of this concept while exploiting the numerous advantages offered by it, namely modularity, scalability, reconfiguration and reduced design cycles. The mean to the end chosen was the actual embracing of the hierarchical nature of PEBB-based converters by applying it to the modeling approach, control software, and energy processing characterization of power electronics systems. The resultant two-dimensional hierarchical reference model pursues the complete analysis and design of power electronics systems, covering not only the electromagnetic, thermal and mechanical interactions from semiconductors up to complete power systems, but also their associated controls, modeling and communications at every hierarchy level. In order to achieve these objectives several tasks were identified and undertaken in this project. Specifically, several studies were conducted in order to fully characterize the energy processing functions observed in shipboard power systems, individually addressing the PEBB, power converter and power system levels. The PEBB level—using a CPES built 33 kW PEBB—was subjected to a complete study describing it across all defined hierarchies, i.e., energy processing, controls and modeling. Further, the complete design and evaluation of its digital controller (Hardware Manager) is also presented, thus fully characterizing the controls hierarchy at this level. The PESNet communications protocol developed in this project is also presented and described in details complementing the controls hierarchy analysis. Additionally, in an effort to explore the feasibility of applying the proposed reference model to different marine-like applications, the usage of PEBB-based distributed generation converters and the design and evaluation of protection systems for power electronics systems is also included. Regarding the modeling hierarchy of the proposed reference model, an in-depth revision of hierarchical modeling techniques for power converter systems is presented, focusing on the modeling of PEBB's and more involved PEBB-based power converter structures. Finally, a thorough coverage of the control software hierarchy is presented by assessing the advantages of employing dataflow-based programming techniques for the development of modular controls for power electronics systems. In all, the results obtained in this project have successfully verified the capabilities and great flexibility of the proposed power electronics standard-cell reference model for the analysis of PEBB-based systems. Its absolute validation would be accomplished by performing the complete electromagneto-mechano-thermal design and evaluation—from concept to simulations and emulations—of prospective architectures for marine power electronics conversion systems.

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Chapter 1 STANDARD-CELL, OPEN-ARCHITECTURE POWER CONVERSION SYSTEMS

I. Introduction

Adhering to the apparent success of the Power Electronics Building Block (PEBB) concept envisioned by the Office of Naval Research (ONR), this project has sought the consolidation of modular power electronics conversion systems by developing a standard-cell open-architecture reference model providing the required standardization and abstraction needed to enable the electromagnetic thermal design of power converter units; from semiconductor devices to converter structures, from PWM modulators to supervisory control loops, and from detailed switching to small-signal models. This threefold hierarchical approach following the seven layer ISO/OSI reference model has essentially furthered as well as benefited from the PEBB idea, incorporating and applying its intrinsic features to the electromagnetic thermal design of PEBB-based converters, to the development of modular control software, and to the development of hierarchical mathematical models for simulation studies.

The fundamental focus of this project has therefore been the study and analysis of the so-called standard-cells in order to determine and define the hierarchical layers of the proposed reference frame as well as characterizing the interfaces of the controls, models and power stage cells or blocks. While on system hardware blocks—actual components such as semiconductors, PEBB's, power converters, etc.—physics-based characterization of materials and energy were used for this purpose, information distribution and data flow analysis were used for the characterization of control software modules and simulation models. Although the methodology developed in this project is appropriate for all hierarchies of power conversion systems, the work performed has primarily focused on the PEBB and its subsequent level the power converter, taking advantage in this way of the 100 kW three-phase PEBB-based power converter built in the previous CPES-ONR project "Plug and Play Power Conversion Systems." Results obtained from these studies and analyses have been fruitful to say the least, and have provided the means to approach the design of power converters in a more structured systematic way leading the power electronics practitioner into simpler, orderly, and overall faster design cycles.

The contributions of this project towards the realization of advanced modular power electronics conversion systems are plentiful, and have been consequently organized throughout this report in order to provide the reader with a clear view and understanding of the main accomplishments. For the sake of completeness and ease of reading each chapter is organized as an independent self-contained document, hence avoiding unnecessary references among different chapters. What follows then is a brief description of each of the report chapters, providing the key points addressed and main results obtained.

II. Organization of Chapters

Chapter 2 presents a detailed study on the partitioning and energy flow characterization of a more electric ship power system. Based on a complete description of a reduced power system section comprising propulsion and system loads, a functional analysis is performed leading to a better comprehension of the system operation and thus to its intrinsic modular nature. This study is supported by the analysis of the ship power system using different instantaneous power theories enabling the characterization, evaluation and partitioning of the system in accordance to the governing laws of physics. From these studies, a sound understanding and characterization of ship power systems was obtained.

Chapter 3 presents an elaborate study and interface characterization of PEBB-based converters combining functional hierarchical analysis with three-phase and single-phase instantaneous power theories. This combined approach enables the complete description of the energy flow throughout the power converter structure and each of its components, PEBB's included The results presented take into consideration fundamental and harmonic frequencies, hence laying the foundations for PEBB design encompassing active semiconductor devices and passive reactive storage components.

Chapter 4 goes further down the proposed reference model hierarchy analyzing in great detail the interface and partitioning schemes for the 33 kW PEBB developed in CPES as part of the previous "Plug and Play Power Conversion Systems" ONR-sponsored project. This work employs detailed physics-based modeling exploiting the Poynting vector electromagnetic analysis tool, which enables the qualitative exploration and characterization of the energy flow throughout the PEBB module structure. These studies are performed on simplified simulation models and on detailed switching models with direct comparison with the hardware unit for verification purposes. The results obtained provide valuable insight into the partitioning choices of the PEBB module, and the grounds for further studies and designs explored by means of the thermal design of a busbars for PEBB-based converters.

Chapter 5 devotes completely to the PEBB-level reference model hierarchical layer, characterizing its terminals and interactions through and across the different hierarchies, i.e., controls, modeling and power processing. This work results in the complete description of the PEBB as a power processor, providing all necessary information for the synthesis of power systems based on such module as building block. The analyses presented comprised electromagnetic, thermal and mechanical characterization, associated detailed and behavioral simulation models, and corresponding modular control software.

Chapter 6 presents the complete design, testing and evaluation of the Hardware Manager, the digital control brains of the PEBB that enable its interaction with peers and establishes the communication link for control purposes with equal or higher level hierarchy levels. The Hardware Manager is critical since it represents the intelligent entity of the PEBB, which per definition is an intelligent power module capable of interacting with its peers while performing different power electronics tasks. As it is known, the Hardware Manager was conceived in the previous CPES-ONR project "Plug and Play Power Conversion Systems," but went through a complete revision and upgrading phase in this project finalizing with the manufacture of several new boards. This Chapter covers the complete hardware and software design—VHDL programming of its FPGA—of the Hardware Manager, focusing on the key components as the PWM modulator, sensors and fiber optic communications interface.

Chapter 7 presents an in-depth description and verification of the PESNet communications protocol developed to enable the communications of distributed digital control architectures based on PEBB modules. The PESNet protocol is built over the lowest four layers in the ISO/OSI reference model, namely the physical layer protocol (PLP), link layer protocol (LLP), network layer protocol (NLP) and application layer (AP). PLP specification defines the characteristics of the transmission medium, such as fiber-optic links, optical connectors and other components, frequency, power levels, and bit level encoding/decoding mechanisms. The LLP specification defines how to access the medium and make upper layer protocols independent of the physical layer, such as data frame format, addressing, error detection and correction, media configuration, node initialization, insertion and removal, and fault isolation and recovery. The NLP specification defines communication between a pair of a source and a destination, such as packet format, and routing methods. And the AL relates to the application layer controls. This chapter covers in great detail each and every component of the protocol as well as its functional description, discussing application related issues as synchronization and communications delay which affect the operation and performance of PEBB-based power converters.

Chapter 8 presents a brief survey and study on the applicability of the Standard Cell Open Architecture concept to the protection of shipboard power distribution systems. The intrinsic hierarchical nature of

protection devices is explored while analyzing several functional and time domain aspects of their operation. Through these studies their direct correspondence and mapping into the proposed reference model is established, setting the paths for possible future works on this field and the design of protection schemes for modular power electronics conversion systems.

In an effort to expand and prove the versatility of the proposed reference model for standardized open architecture power conversion systems, Chapter 9 explores the applicability of these and the PEBB concept itself into alternative marine-like applications. Specifically, it presents the study and analysis of PEBB-based power converters for distributed generation, which clearly resembles the operational characteristics of marine applications. It was found that the ideas promoted by these modular power electronics systems perfectly match and apply those of distributed generation, where at a higher hierarchy level these distributed power systems may be analyzed as a single entity comprised of converters built in turn with PEBB modules. The results obtained were promising and several control and operating modes are presented and discussed in details throughout this chapter regarding the usage of PEBB-based converters to connect and disconnect these systems to the utility grid under faulty or any other desired conditions.

Chapter 10 presents a comprehensive review of modeling and simulation techniques for power electronics systems, describing the main features and advantages of different modeling approaches across the complete modeling hierarchy, from semiconductor physics-based models to behavioral and small-signal models. The chapter focuses on practical issues such as mathematical complexity and needed processing power for the different methods described, as well as defining the minimum set of requirements needed to capture different electromagnetic phenomena, i.e., power flow, harmonics and EMI. Finally, the need for a unifying modeling approach is identified setting forth feasible guidelines to accomplish this.

Chapter 11 devotes entirely to the modeling of the 33 KW PEBB module developed at CPES as part of the previous ONR-sponsored project "Plug and Play Power Conversion Systems." The chapter presents a detailed electromagnetic modeling of the PEBB module under question, developing physics-based, switching, and behavioral models both in Saber and VTB. In an effort to support the Electric Ship Research and Development Consortium (ESRDC) further modeling and testing in VTB was performed, building a new series of PEBB and PEBB-based converter modules generated as part of a PEBB library made available to the University of South Carolina, Florida State University and Mississippi State University. These PEBB models presented throughout the chapter are complemented by the inclusion of a Universal Controller model, having all necessary low level and high level application controls required to implement many different shipboard three-phase power electronics applications.

Finally, Chapter 12 presents the control software related work realized in this project. Specifically, it focuses on the evaluation of the open control architecture implemented by means of the dataflow approach. This programming approach presents a reduced complexity, flexible, reconfigurable and reusable control software implementation that perfectly blends into the standard-cell open architecture work frame, providing the same modularity and advantages attained for hardware with PEBB modules but for software constructions. The chapter presents a complete description of this approach as well as thorough evaluation in terms of processing times and a final experimental verification where the clear advantages of this modular hierarchical control software development technique are clearly established.

Chapter 2 SHIP POWER SYSTEM PARTITION AND ENERGY FLOW CHARACTERIZATION

I. Introduction

A ship power system presents a wide diversity of components and equipment intended to provide the energy requirements for all different onboard applications. Therefore, the electric equipment throughout the ship is rather different in power capacity and functionality; nevertheless, when analyzing the functions at the different hierarchy levels there exists certain commonality. The idea is to find these similarities in order to identify the common components providing these common functions. These components are the power electronics building blocks, PEBB. The final goal of this work is to find precise partitioning protocols that can be used as design guidelines for PEBB-based power electronic systems.

A good power stage partitioning requires proper knowledge of the energy propagation in power converters. This knowledge provides information about the various trade-offs affecting the functional, spatial and temporal distributions of the different energy processes. In addition, the theoretical paradigms used to study the energy flow should be in agreement and be unified into the proposed hierarchy in order to characterize the power conversion system. Consequently, proper tools need to be identified and tested under different converter configurations and different applications.

The concepts presented in this chapter are applied to a ship power system, hereinafter described.

II. Ship power system description

The ship power system presents a variety of equipment in a wide power range making its partitioning into functional blocks a challenging process. The complete system can be divided into two main sections according to their respective purpose, namely propulsion and auxiliary systems. The propulsion system consumes the vast majority of the energy in the ship. The energy sources are synchronous generators driven by gas turbines. In the case of the ship under study the propulsion motors are induction machines with two sets of stator windings each. The energy to these windings is provided from a motor drive based on a voltage source inverter (VSI). An active rectifier that regulates the DC voltage level connects the VSI to the DC bus. Each VSI feeds a three-phase winding of the system. The auxiliary systems are primarily classified into AC and DC systems. The energy supply for the AC subsystem is taken from the same buses that feed the propulsion system. The single line diagram of the AC system is shown in Fig. 2-1.

The auxiliary DC subsystems are fed from the same buses feeding the AC system. Usually there are different services connected to the DC bus, specially those services that require a higher degree of reliability regarding energy availability. The DC bus system is composed of a double set of buses that can feed any of the consumers. A schematic of the DC system adopted for this study is shown in Fig. 2-2. The architecture of this system was previously presented in [15]-[17]. Although the configuration of the system follows the one in the ship, for this study we are considering only a selected set of components that generally cover the different types of equipment that are present in the ship power system. The DC system has a zonal configuration with the two sets of buses fed by three-phase boost rectifiers. Each piece

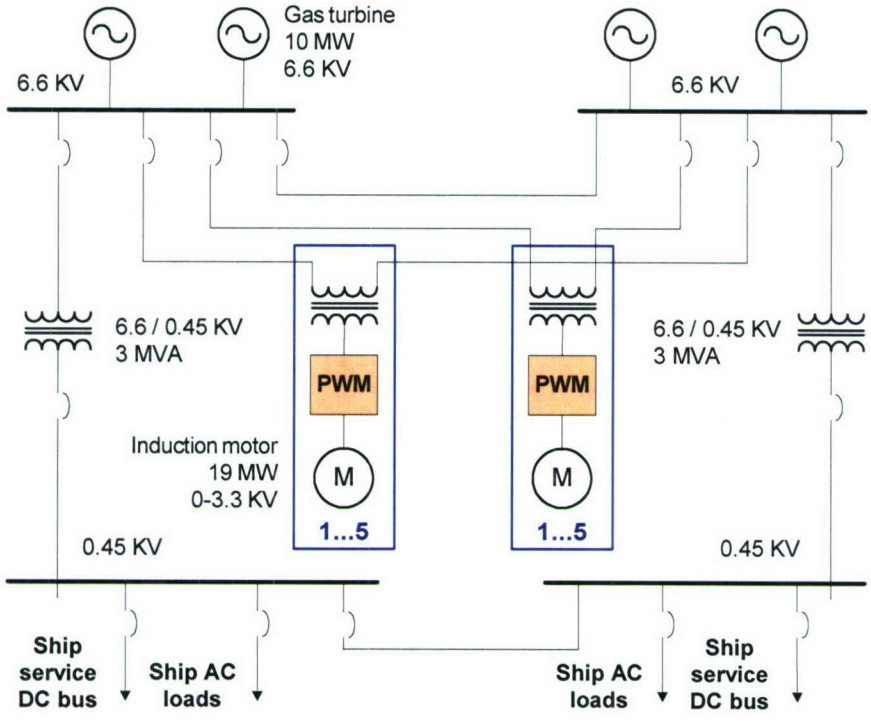


Fig. 2-1 AC portion of the ship power system

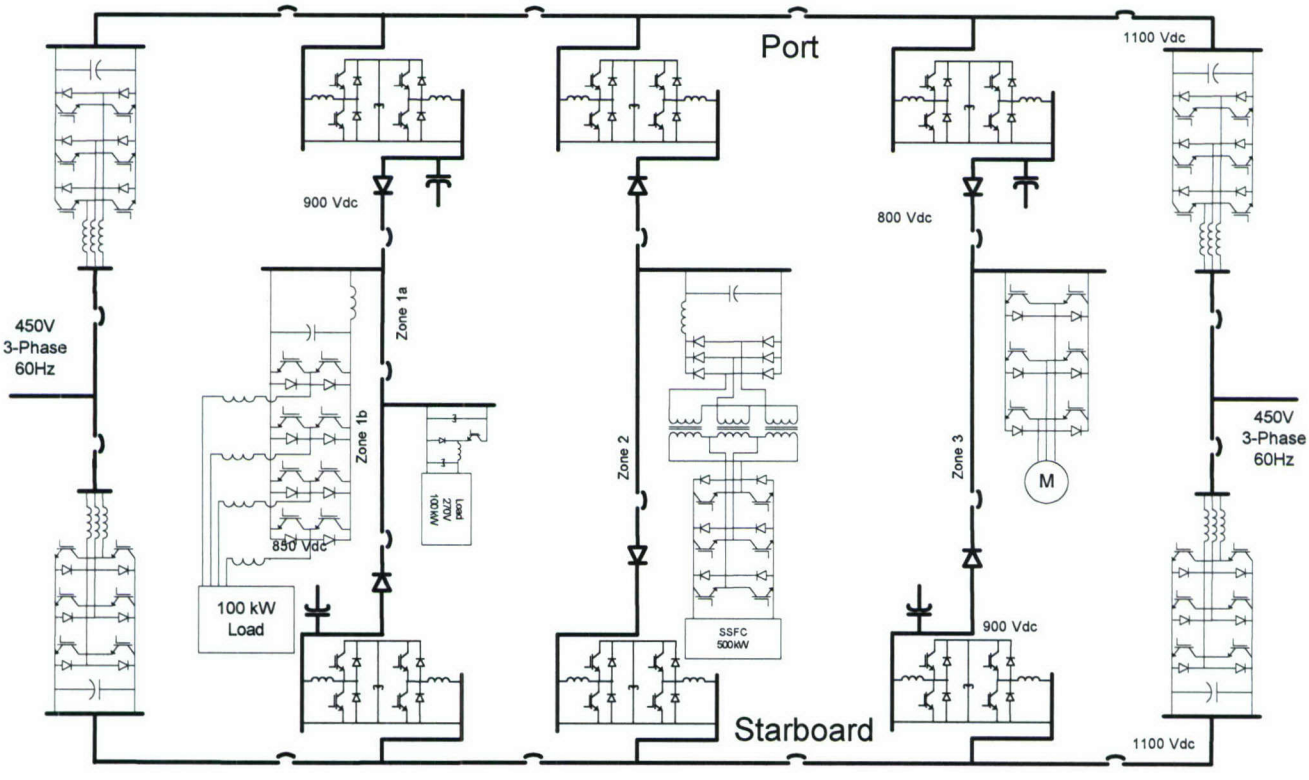


Fig. 2-2 DC zonal ship power system

of equipment can be connected to either one or the other DC bus. In case of failure in the energy distribution of one of the buses the equipment under consideration would be immediately connected to the other. Five zones are considered in our study, of which two provide the interconnection from and to the three-phase system. Three internal zones are considered that connect different types of loads and

generators. Two DC-DC converters are used in each zone to adapt the DC voltage levels. The second zone in Fig. 2-2 is composed by a three-phase four-leg converter and a single phase DC-DC buck converter. The third zone connects a fuel-cell generator, where a VSI is connected to the fuel-cell and a transformer plus diode rectifier used to adapt the voltage levels. In the fourth zone there is a motor drive supplying an induction machine.

II.1. Functional analysis

The first step of the partition methodology is to do the functional analysis of the components in our system. Therefore, the equipment in the ship power system was analyzed not only from the electrical point of view but also from mechanical and thermal perspectives. The details of the different functions are shown in Table 2-2. The functional analysis suggests a partition and PEBB configuration. The PEBB arises at certain level when the functions become repetitive throughout all the applications analyzed. In our case this happens at the third hierarchical layer or level (from bottom to top).

On the other side, when the mechanical and thermal functions are analyzed among the converters in the system a much higher repetitiveness is observed at all levels. This means that the requirements for these additional functions are considerably more common at all levels than the electrical functions. This can be explained by the requirements on each converter. Specifically, all converters are built with a certain purpose, defined by the electric functional requirements. On the other hand, these additional mechanical and thermal functions are complementary and significantly more standardized in equipment built using similar technologies, i.e., materials and general design criteria. The degree of repetitiveness in per unit is shown in Fig. 2-3. In the figure it is observed the change of the curve shape when moving across the different layers. For layers high in the hierarchy the curve tends to show low values of repetitiveness (in the vertical axes) and a large number of functions (in the horizontal axes). On the other side, for layers low in the hierarchy the curves show a large number of repetitiveness and a reduced number of functions. A formal mathematical conceptualization of the PEBB concept may be possible by extending the analysis to a large amount of equipment and the usage of statistical tools. This type of analysis will not be done here since our focus is concentrated in the partitioning and characterization of the energy interfaces. The partition obtained up to this point can be considered preliminary. The process of finding an optimal partition requires finding appropriate tools, which will be discussed in the next section.

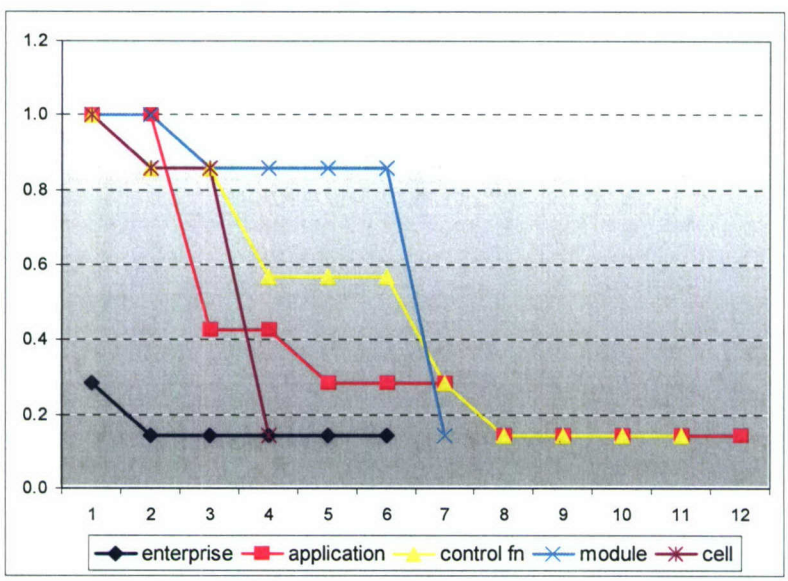


Fig. 2-3 Repetitiveness of power converter functions

Layer	Function	# app	app / tot
6- Enterprise	Transfer electric energy between 2 DC systems	2	0.286
	Provide electric energy to the motor	1	0.143
	Provide electric energy to a 3-phase unbalanced, non-linear load	1	0.143
	Energy delivery from a DC source (DC to 3-phase AC conv.)	1	0.143
	Energy conversion from 3-phase to DC system regulated	1	0.143
	Energy conversion from 3-phase to DC system non-regulated	1	0.143
5- Application	Proteccion of the equipment	7	1.000
	EMI limit requirements	7	1.000
	Vdc voltage regulation	3	0.429
	Low ripple on the DC side	3	0.429
	Vac voltage regulation	2	0.286
	Harmonic cancellation	2	0.286
	Zero sequence Vac voltage regulation (Vo)	2	0.286
	Torque control	1	0.143
	Speed (position)/flux control	1	0.143
	Machine rotor position detection	1	0.143
	Input power factor control (P,Q)	1	0.143
	AV magnitudes compatible with motor isolation	1	0.143
4- Control function	Processing of measurements	7	1.000
	Duty cycle calculation	6	0.857
	DC filter for voltage ripple	6	0.857
	Line synchronization (PLL)	4	0.571
	Current control (id,iq)	4	0.571
	AC ripple filtering	4	0.571
	Current control DC	2	0.286
	Frequency control	1	0.143
	Zero sequence current control (io)	1	0.143
	Three-phase balance in transf winding to prevent staircase core saturation	1	0.143
	Fixed voltage regulation tied to input voltage	1	0.143
3- Module	Primary protection of devices	7	1.000
	Power magnitudes sensing and conditioning	7	1.000
	Switching control (modulation)	6	0.857
	Pulse gating	6	0.857
	Safe commutation enabling (dv/dt, di/dt)	6	0.857
	Energy storage in the DC side	6	0.857
	Uncontrolled switching V-I characteristic	1	0.143
2- Power cell	Proper connection of I/V equivalent source terminals	7	1.000
	Bi-directional current conduction	6	0.857
	One-directional voltage blocking	6	0.857
	One-directional current conduction	1	0.143

Fig. 2-4 Functional evaluation summary for the ship power system

Table 2-1 Functional Analysis of drive propulsion system and relevant electromagnetic phenomena

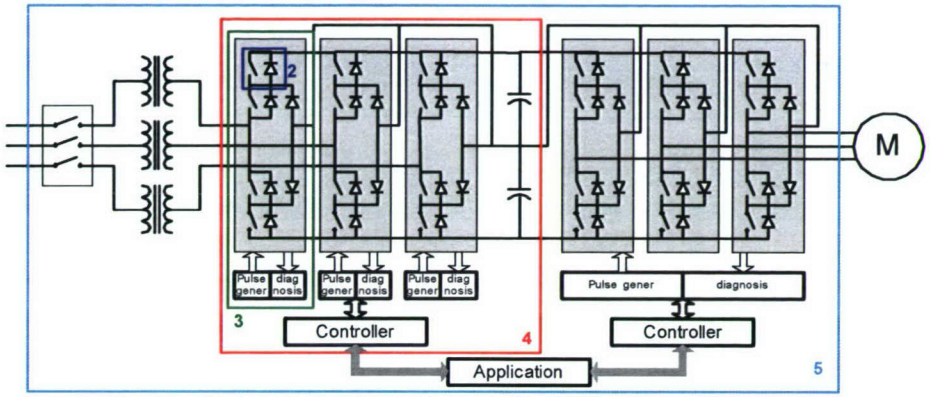
	Active Rectifier	Inverter	Phenomena	Time resolution
Simplified one-line diagram				
6- Enterprise (distribution)	1- Provide electric energy for driving the induction machine 2- Do not disturb the distribution network (power quality)		Conducted low-freq - Power frequency variations - Sags, swells and interruptions - Voltage unbalance - Harmonics, interharmonics - Non-useful current components (reactive)	 30 cycles – 3 sec 0.5 sec – 1min steady state 0-100th 0-6kHz steady state steady state
5- Application (station)	1- Vdc Voltage regulation 2- Input power factor control (P, Q)	1- Speed (position)/flux control 2- Torque control 3- Machine position detection	Conducted low-freq - Voltage unbalance - Zero-sequence current (I unbalance) - Harmonics, interharmonics - Non-useful current components (reactive) - Induced DC or low-freq voltages	 Steady-state Steady state 0-100th 0-6kHz steady state steady state steady state
4-Control function (converter)	1- Line synchronization (PLL) 2- Line current control (id, iq) 3- Duty cycle calculation	1- Frequency control 2- Current control (id, iq) 3- Voltage and current measurement 4- Duty cycle calculation	Conducted low-freq - Zero sequence current (I unbalance) - Power frequency variations - Harmonics, interharmonics - Induced DC or low-freq voltages	 Steady state 30 cycles – 3 sec 0-100th 0-6kHz steady state steady state
3- Power Conversion (module)	1- Switching control (modulation control) 2- Pulse gating 3- Safe commutation enabling (limiting dv/dt, di/dt, etc) 4- Primary protection of devices 5- Power magnitudes sensing and conditioning		Conducted high-freq - Unidirectional transients (low-freq) - Oscillatory transients (low-freq) Radiated low-freq - Electric, magnetic fields	 >1 msec 5 kHz (fsw) 5 kHz (fsw)
2- Power cell (device)	1- Bi-directional current conduction 2- One-directional voltage blocking 3- Proper connection of I / V equivalent source terminals		Conducted high-freq - Unidirectional transients (low & med freq) - Oscillatory transients (low & med freq) Radiated high-freq - Electric, magnetic, electromagnetic fields	 1msec – 50 nsec 5 – 500 kHz 5 kHz – 5 MHz

ABB ACS 6000 Motor drive family

Table 2-2 Functional Analysis of different ship electric components

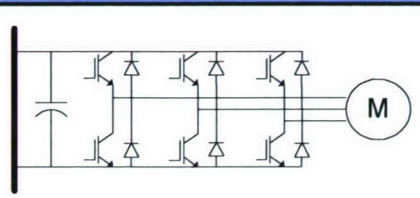
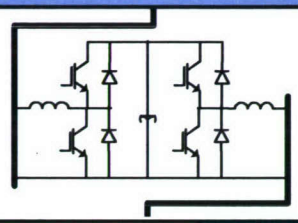
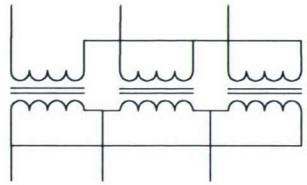
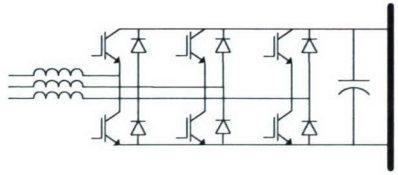
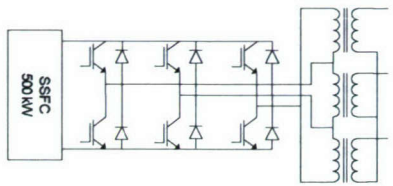
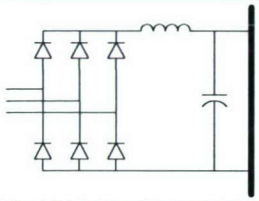
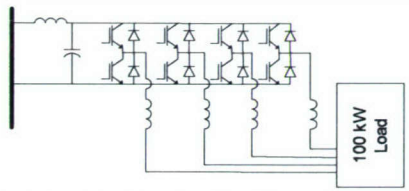
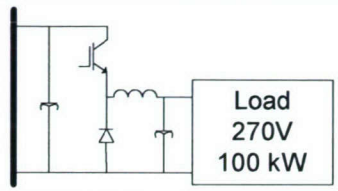
	Voltage source inverter for motor drive		DC-DC H-bridge converter		Single-phase power transformer		Power supply three-phase boost rectifier	
Simplified one-line diagram								
6- Enterprise	1- Provide electric energy to the motor	1- No damage to the rest of the system / people	1- Electric energy transfer between two DC systems at different Voltage	1- No damage to the rest of the system / people	1- Electric energy transfer between two isolated electric circuits	1- No damage to the rest of the system / people	1- Energy conversion from 3-phase to the DC distribution system	1- No damage to the rest of the system / people
5- Application	1- Speed (position)/flux control 2- Torque control 3- Machine position detection 4- Protection of equipment 5- Low disturbance in the connection bus 6- EMI limit requirements 7- AC V and I compatible with motor integrity	1- Achieve high efficiency 2- Electrical connection to the circuit 3- Appropriate size and weight	1- Vdc Voltage regulation 2- Protection of equipment 3- Low disturbance in the connection bus	1- Achieve high efficiency 2- Electrical connection to the circuit 3- Appropriate size and weight	1- Voltage level transformation for the two connected circuits 2- Balance among the phases 3- Current magnitude transformation 4- Isolation between the electric and magnetic circuits 5- Equipment protection 6- Additional Volt change (taps)	1- Connection to the electric grid 2- Achieve high efficiency 3- Dissipation of heat generated by losses 4- Appropriate size and weight	1- Vdc Voltage regulation 2- Input power factor control (P, Q) 3- Low harmonic content on AC side 4- Low ripple on DC side	1- Achieve high efficiency 2- Electrical connection to the circuit 3- Appropriate size and weight
4- Control function	1- Frequency control 2- Current control (id, iq) 3- Duty cycle calculation 4- DC filter for voltage ripple 5- AC ripple filtering in V, I 6- Processing of measurements	1- Paths to allow heat dissipation (air/water flow) 2-Mechanical structure and dimension 3- Electrical distances and geometry	2- DC Current control 3- Duty cycle calculation 4- DC voltage ripple limitation 5- AC current ripple limitation 6- Processing of measurements	1- Paths to allow heat dissipation (air/water flow) 2- Mechanical structure and dimension 3- Electrical distances and geometry	1- Energy conversion electric-magnetic-electric 2- Magnetic field guidance 3- Voltage regulation characteristic 4- Leakage impedance value (short-circuit, regulation) 5- Inrush current limitation and proper transient behavior 6- Equal charac in the 3-phase	1- Structural mechanical strength 2- Paths for fluid circulation for heat dissipation (oil/air) 3- Electrical distances and geometry	1- Line synchronization (PLL) 2- Line current control (id, iq) 3- Duty cycle calculation 4- DC bus low-pass filter 5- AC three-phase low-pass filter 6- Processing of measurements	1- Paths to allow heat dissipation (air/water flow) 2- Mechanical structure and dimension 3- Electrical distances and geometry
3- Power Conversion	1- Switching control (modulation) 2- Pulse gating 3- Safe commutation enabling (limiting dv/dt, di/dt, etc) 4- Primary protection of devices 5- Power magnitudes sensing and conditioning 6- Energy storage at DC side	1- Heat dissipation from devices 2- Voltage isolation 3- Low parasitic values	1- Switching control 2- Pulse gating 3- Safe commutation enabling (limiting dv/dt, di/dt, etc) 4- Primary protection of devices 5- Power magnitudes sensing and conditioning 6- Intermediate energy storage in DC capacitor	1- Heat dissipation from devices 2- Voltage isolation 3- Low parasitic values	Coil packets 1- Current conduction 2- Limit to the magnetic (iron) losses: eddy currents, hysteresis 3- Limit to the conduction losses: resistive, skin, proximity effect	1- Heat transmission for dissipation 2- Voltage isolation 3- Low parasitic values 4- Geometric disposition low proximity effect	1- Switching control (modulation) 2- Pulse gating 3- Safe commutation enabling (limiting dv/dt, di/dt, etc) 4- Primary protection of devices 5- Power magnitudes sensing and conditioning 6- Energy storage at DC side	1- Heat dissipation from devices 2- Voltage isolation 3- Low parasitic values
2- Power cell	1- Bi-directional current conduction 2- One-directional voltage blocking 3- Proper connection of I / V equivalent source terminals	1- Low commutation and conduction losses 2- Heat transmission for dissipation 3- Mechanical strength	1- Bi-directional current conduction 2- One-directional voltage blocking 3- Proper connection of I / V equivalent source terminals	1- Low commutation and conduction losses 2- Heat transmission for dissipation 3- Mechanical strength	Coil 1- Induced emf due to flux linkage 2- Current conduction 3- Voltage isolation	1- Low conduction losses 2- Heat transmission for dissipation 3- Mechanical strength	1- Bi-directional current conduction 2- One-directional voltage blocking 3- Proper connection of I / V equivalent source terminals	1- Low commutation and conduction losses 2- Heat transmission for dissipation 3- Mechanical strength

Table 2-2 cont.

	Three-phase inverter for fuel-cell		Three-phase diode rectifier		3-phase 4-leg voltage source inverter		Buck converter for single-phase load	
Simplified one-line diagram								
6- Enterprise	1- Deliver the energy from the power DC source	1- No damage to the rest of the system / people	1- Transfer the energy from the three-phase to DC circuit	1- No damage to the rest of the system / people	1- Provide electric energy to a three-phase unbalanced, non-linear load	1- No damage to the rest of the system / people	1- Provide electric energy to an AC single-phase load	
5- Application	1- DC to three-phase AC conversion 2- Vac voltage regulation Vd, Vq 3- Achieve good efficiency in the conversion	1- Achieve high efficiency 2- Electrical connection to the circuit 3- Appropriate size and weight	1- Six-phase, three-phase rectification 2- Low output voltage and current ripple 3- Achieve good efficiency in the conversion process	1- Achieve high efficiency 2- Electrical connection to the circuit 3- Appropriate size and weight	1- Vload voltage regulation Vld,Vlq, Vlo 2- Load unbalance compensation 3- Harmonic cancellation 4- Keep EMI under control	1- Achieve high efficiency 2- Electrical connection to the circuit 3- Appropriate size and weight	1- Vload voltage regulation	
4- Control function	1- Line synchronization (PLL) 2- Line current control (id, iq) 3- Duty cycle calculation 5- Primary winding balance to prevent staircase core saturation	1- Paths to allow heat dissipation (air/water flow) 2- Mechanical structure and dimension 3- Electrical distances and geometry	1- Voltage regulation characteristic (input + load magnitude) 2- Output voltage harmonic and ripple reduction (low-pass filter)	1- Paths to allow heat dissipation (air/water flow) 2- Mechanical structure and dimension 3- Electrical distances and geometry	2- Synchronization (PLL) for Park transformation 1- Current control (id, iq, io) 3- Duty cycle calculation 4- Processing of the measurements (anti-aliasing)	1- Paths to allow heat dissipation (air/water flow) 2- Mechanical structure and dimension 3- Electrical distances and geometry	1- Current control 2- Duty cycle calculation 3- Processing of the measurements (anti-aliasing)	
3- Power Conversion	1- Switching control (modulation) 2- Pulse gating 3- Safe commutation enabling (limiting dv/dt, di/dt, etc) 4- Primary protection of devices 5- Magnitudes sensing and condition 6- Transformer low leakage inductance	1- Heat dissipation from devices 2- Voltage isolation 3- Low parasitic values	1- Current conduction/blocking 2- Primary protection of devices 3- Power magnitudes sensing and conditioning 4- Heat dissipation	1- Heat dissipation from devices 2- Voltage isolation 3- Low parasitic values	1- Switching control (modulation control) 2- Pulse gating 3- Safe commutation enabling (limiting dv/dt, di/dt, etc) 4- Primary protection of devices 5- Power magnitudes sensing and conditioning (A/D convert)	1- Heat dissipation from devices 2- Voltage isolation 3- Low parasitic values	1- Switching control (modulation control) 2- Pulse gating 3- Safe commutation enabling (limiting dv/dt, di/dt, etc) 4- Primary protection of devices 5- Power magnitudes sensing and conditioning	
2- Power cell	1- Bi-directional current conduction 2- One-directional voltage blocking 3- Proper connection of I / V equivalent source terminals	1- Low commutation and conduction losses 2- Heat transmission for dissipation 3- Mechanical strength	1- One-direction current conduction 2- One-direction voltage blocking	1- Low commutation and conduction losses 2- Heat transmission for dissipation 3- Mechanical strength	1- Bi-directional current conduction 2- One-directional voltage blocking 3- Proper connection of I / V equivalent source terminals	1- Low commutation and conduction losses 2- Heat transmission for dissipation 3- Mechanical strength	1- Bi-directional current conduction through switch and diode 2- Voltage blocking at the switch	

III. Power Stage Partitioning

The process of power system modularization involves two main aspects. The first one is the partitioning of the system itself in order to achieve modularity. Once the system is partitioned into modules, it can be seen as a set of interacting sub-systems. Therefore, how the modules will be integrated in the system and how will they interact needs to be studied as part of the modularization process. Fig. 2-5 shows schematically the process of system partitioning, which is the transition from system to modules.

Fig. 2-5 The process of system modularization

The objectives in partitioning the system are to facilitate manufacturing and achieve volume. At this phase, the system functional and spatial distribution has more relevance than the temporal one. On the other side, in the process of integration, the physical –temporal and spatial– distributions characteristics are more relevant than the functions. For this process of partition/integration, the energy interactions and the information required for controlling the system are required to be carefully studied. Non-desired interactions are non-desired, non-useful, energy exchanges among system components. In addition, a good design of the control system must be in accordance to the characteristics of the information handling requirements by the control of the energy process.

Previous studies proposed the partitioning of the power converter control system [3], [4]. This proposition was based on the characteristics of the information flow in the different hierarchical levels of the control system, where the partitioning protocol was quantified through the information capacity in Mbit/sec. The measurement of this quantity provided a figure of merit and the basis for partitioning the control system [2]. In the case of power stage partitioning we intend to use a similar methodology. The flowchart of the proposed methodology is shown in Fig. 2-6. That methodology started with a functional analysis of the power converter, where the knowledge of the different functions led to the proposition of a preliminary partition that allowed for an evaluation of the amount of information exchanged through the interfaces between the different portions in which the system was partitioned. The quantification of the amount of information was then used to refine the partition based on more accurate criteria.

In the case of the power stage partitioning it is also necessary to find the tool that provides a quantified criterion for partitioning. The search for such a tool is related to the hierarchy proposed as a basis for the studies in this project because the basic idea in proposing this hierarchy is that there are analytic tools appropriate for describing the phenomena at each hierarchical layer. The goal is to be able to measure the energy exchange at the interfaces between the system parts. An overview of different ways of studying the energy flow in a power system was done. The different energy analytic tools were then related to a hierarchical level. The result of the overview is presented in Fig. 2-7 where different analytic tools describing electromagnetic phenomena are tied with the layers in the reference hierarchy.

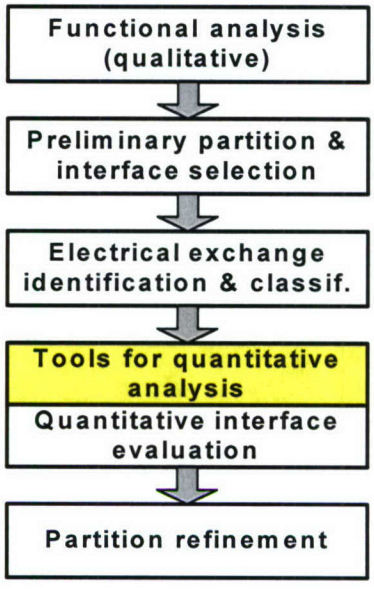


Fig. 2-6 Flowchart of the methodology used for power system partition

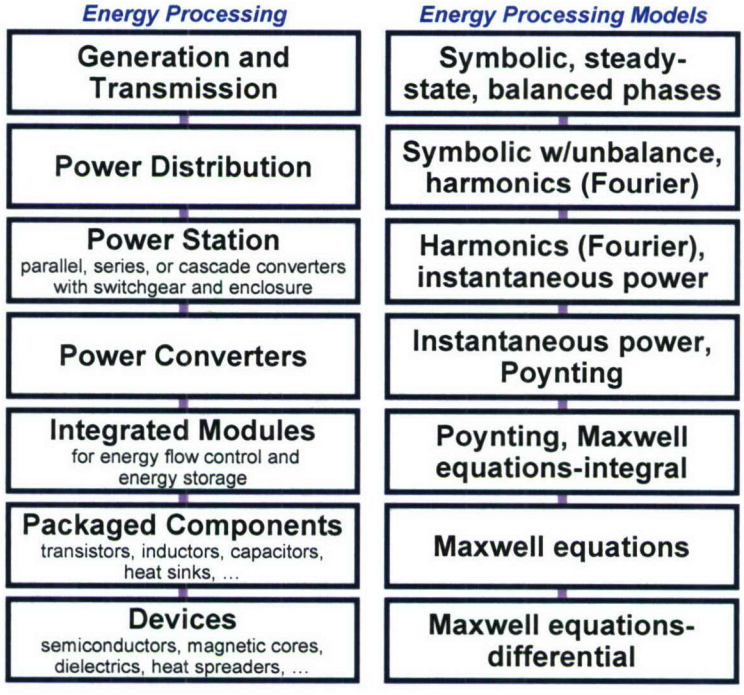


Fig. 2-7 Hierarchical layers and tools for characterization of the electromagnetic phenomena

The classification in Fig. 2-7 is preliminary and it is used as a basis for the energy flow characterization study. The characteristics of the phenomena most relevant at each layer set the general requirements for the tools that will be used to characterize the phenomena at them. From the steady-state operation of a power system to transient commutation of the power semiconductor device there is a wide range in the time-electromagnetic phenomena to be described. An appropriate tool needs to be well balanced between accuracy and mathematical effort in order for not requiring an excessive amount of calculation. The study described in the next section is then the search for that tool required providing a quantitative basis for the power stage partition.

IV. Tools for Characterization of the Energy Interfaces

In order to characterize the interfaces in the proposed system partition proper analytic tools are needed. Based on our previous knowledge of the characteristics of the system we are characterizing, and on different theories that used for electromagnetic analysis a correspondence was found between the levels in our hierarchy and the mentioned theories. This was presented in Fig. 2-7.

The tools and theories for evaluation of the energy processing in power conversion systems must be able to describe the electromagnetic phenomena at each of the layers of the hierarchy presented in Fig. 2-7. One of the characteristics of the hierarchy layers is the time constant of the electromagnetic phenomena most relevant at that layer. Therefore, how the tools handle the time frame is of prime importance. The general objectives of these tools, which can be called power theories, can be summarized as:

- Explanation of the relevant physical phenomena, especially that causing an increase in the apparent power, S, and therefore in the currents.
- Quantification of the energy flow between the different parts of a power system.
- Provide data needed for selecting the power ratings of power system equipment.
- Provide fundamentals for compensation of useless components of the apparent power, and improvement of the power factor.

The evaluation of the proposed analytic tools needs to be focused on the characteristics of the electromagnetic phenomena that are more relevant in our study. This is related to the levels in the proposed hierarchy. Analyzing those levels there are phenomena that are more relevant at a certain layer. Therefore, the proposed tool needs to able to describe those relevant phenomena with accuracy. To explain this with more detail lets concentrate on the four top layers.
In order to check the appropriateness of our approach the analytic tools have to be evaluated.

At the top layer there is the high power high voltage transmission network interconnecting the power plants with the consumer centers. Analysis of this type of electrical system is the subject of the power system studies. Some of the phenomena relevant to study are load flow, transient stability, voltage stability, and voltage regulation profiles. And several algorithm and analytical tools have been proposed to study these phenomena. Among these analyses there is a common set of hypotheses that include steady state operation, or neglecting the electrical time constants considering only the electromechanical ones. In the second layer, the distribution network, some of the phenomena interesting to study are short circuit, load flow, voltage distribution profile, unbalanced loads, harmonic propagation and others. Some of the assumptions are similar to the case of transmission systems, but the degree of detail required in the models is higher. The basic concept is that the characteristics of the phenomena being studied change with the layer level in the hierarchy. Therefore, the requirements on the model used to study those phenomena also need to change. Attached to the change in the degree of detail in the model, there is a change in the size, amount of equipment considered, that is possible to study simultaneously. Models with higher degree of detail are necessarily reduced in the amount of equipment that can be included together into the system model.

V. Modeling the Energy Flow

This section discusses the tools for evaluating energy processing along the system under study. Several formulations of the so-called instantaneous power theories were tested in simulation using different circuit operation conditions in order to evaluate the correctness of the theoretic formulations. Additionally, the energy flow description at different points of the power system provided by those formulations was obtained.

V.1. Instantaneous Power Theories in Circuit Analysis

Instantaneous power theories were originally proposed for studying the problem of load compensation without requiring energy storage in the compensator, for a basic system configuration like the scheme in Fig. 2-8. That is not the case of the study being developed here, but if the proposed theory is based on good understanding of the electric energy exchange, then such theory provides a good picture of the energy flow. Therefore, they may be suitable to understand the energy exchanges among the electrical equipment. This portion of the report analyzes some of the instantaneous power theories propositions and its applicability to our problem of characterizing the energy flow. The proposed instantaneous power tools can be grouped in four categories.

- Type 1: Fryze, Buchholz, Depenbrock (FBD) method
  This formulation was the first one proposed and it is the one more closely derived from the classical power theory
- Type 2: Akagi, with further developments by Peng, Ferrero, Willems, & others
  In this group we include the first proposed instantaneous power theory for the problem of load compensation using active filters and some additional further developments pursuing a mathematical basis for the calculation methodology
- Type 3: Tenti, Rossetto, Salmeron, Montaño
  It formulates the compensation problem as a transmission capacity optimization problem. The optimization is based on the Lagrange multiplier method
- Type 4: Czarnecki
  This approach considers the circuit load as fed by an ideal voltage source and analyze the current evolution by decomposition in components. It seeks for the physical meaning of the different current components. The current components by the voltage give the power components, with a physical meaning.

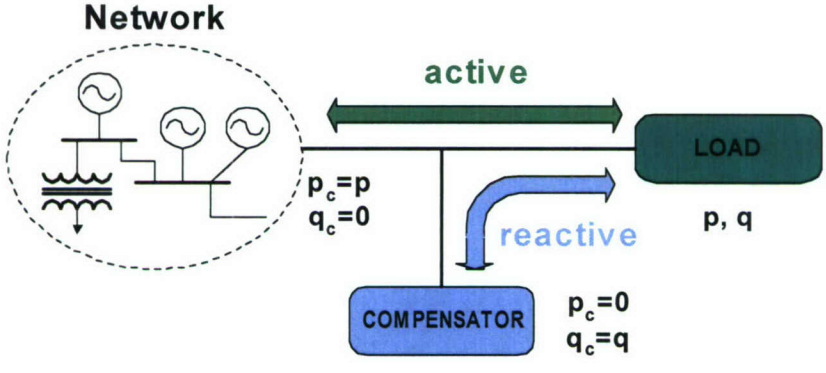


Fig. 2-8 The goal of compensation is to eliminate the non-useful power requirements from the system source

A. Type 1

The first power theory we will analyze was proposed by Depenbrock in the so-called FBD (Fryze, Buchholz and Depenbrock) method [19], [20]. The proposition is very general and attempts covering the general case of any multi-phase, multi-winding circuit. This formulation also presents a basic differentiation between the magnitudes that are defined as instantaneous and the average over one period of the line frequency. The collective current, voltage and instantaneous power for an undetermined set of conductors are defined as:

$$i_{\Sigma}^{2}(t) = i(t) \cdot i(t)$$

$$u_{\Sigma}^{2}(t) = u(t) \cdot u(t)$$

$$p_{\Sigma}(t) = u(t) \cdot i(t)$$

Under periodic conditions, the rms value can be calculated, the magnitudes becoming:

$$I_{\Sigma}^2(t) = \frac{1}{T}\int_0^T i_{\Sigma}^2(\tau)d\tau = \overline{i(t) \cdot i(t)} \tag{1}$$

$$P_{\Sigma}(t) = \frac{1}{T}\int_0^T p_{\Sigma}(\tau)d\tau = \overline{u(t) \cdot i(t)} \tag{2}$$

This collective current and power are defined as the one-period average. The current compensation can be based in any of the two sets of definitions. The instantaneous compensation defines the power component of the current as:

$$i_p(t) = G_p(t) \cdot u(t) \tag{3}$$

With the instantaneous conductance being

$$G_p(t) = \frac{u(t) \cdot i(t)}{u(t) \cdot u(t)} = \frac{p_{\Sigma}}{u_{\Sigma}^2} \tag{4}$$

And the powerless current, i_z, is defined as the component that does not involve power.

$$i_z(t) = i(t) - i_p(t) \tag{5}$$

The corresponding one-period average magnitudes is the active current

$$i_a(t) = G_a(t) \cdot u(t) \tag{6}$$

$$G_a(t) = \frac{\overline{u(t) \cdot i(t)}}{\overline{u(t) \cdot u(t)}} = \frac{P_{\Sigma}}{U_{\Sigma}^2} \tag{7}$$

The non-active current, and the variation current are respectively defined as:

$$i_n(t) = i(t) - i_a(t) \tag{8}$$

$$i_v(t) = i_n(t) - i_z(t) \tag{9}$$

Compensation without requiring energy storage in the compensator is strictly achieved when the compensation is instantaneous. If the one-period average is used, then the exchange between the system and the energy storage may be zero over one-period average, but not instantaneously. In other words certain energy storage is still required.

B. Type 2

A different approach, valid for three-phase circuit analysis was proposed in [18] and later refined by other authors [21]-[26]. This formulation uses the Clarke transformation matrix to transform the *a-b-c* magnitudes to the α-β-*o* coordinate system. The transformation is represented by the matrix *T*.

$$T = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} \end{bmatrix} \tag{10}$$

If the system is three-phase and has only three-wires, only two magnitudes are independent being possible to obtain the third one form the other two. Therefore, the third component in the α-β-*o* system does not give any useful information and can be disregarded. In the resultant α-β system, the instantaneous active and reactive power components are defined from the following matrix:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_{\alpha} & v_{\beta} \\ -v_{\beta} & v_{\alpha} \end{bmatrix}\begin{bmatrix} i_{\alpha} \\ i_{\beta} \end{bmatrix} \tag{11}$$

Additionally, defining the voltage and current vectors in the α-β reference system,

$$i_{\alpha\beta} = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \qquad v_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix},$$

The instantaneous active and reactive powers are the dot and cross products of voltage and current vectors:

$$p = v_{\alpha\beta} \bullet i_{\alpha\beta} \tag{12}$$

$$q = v_{\alpha\beta} \times i_{\alpha\beta} \tag{13}$$

These two equations define a plane for the instantaneous active power and an imaginary axis for the instantaneous reactive power, which are represented schematically in Fig. 2-9. Additionally, by manipulating the matrix equation (5-11) it is possible to obtain the active i_p and reactive i_q current components in the α-β system, those currents are expressed as:

$$i_{\alpha p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} p$$

$$i_{\alpha q} = \frac{-v_\beta}{v_\alpha^2 + v_\beta^2} q$$

$$i_{\beta p} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2} p$$

$$i_{\beta p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} q$$

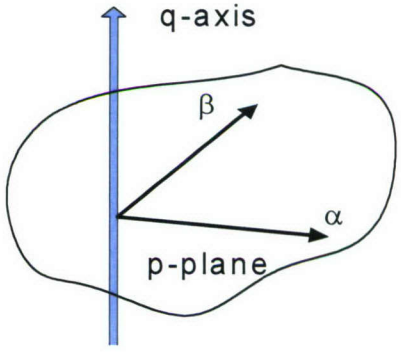


Fig. 2-9 α-β system and the p-plane and q-axis

The idea then is to cancel the instantaneous reactive power flow in the line supplying the load, Fig. 2-8, by compensating the instantaneous reactive current components. If the compensation is achieved instantaneously, no energy storage is required in the compensator generating the reactive current components. This compensation principle works appropriately in a three-phase, three-wire system. When a four-wire system must be analyzed, the o-axis cannot be disregarded and the formulation in [18] proposes the following matrix for the instantaneous powers definitions,

$$\begin{bmatrix} p_o \\ p \\ q \end{bmatrix} = \begin{bmatrix} v_o & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_o \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{14}$$

Where the o-axis instantaneous power p_o is introduced. Nevertheless, as it will be shown later with greater detail, in the four-wire system the formulation losses generality and the original proposition expressed in the previous paragraph is no longer met. Further developments by Peng, Ferrero, Willems, and other authors tried to overcome this problem and generalized the formulation for four-wire systems. After some development that valid generalization was achieved by using a four-dimensional space vector transformation [24]. This point will be discussed separately.

C. Type 3

Other authors [27],[28] formulated the compensation of non-useful current components as an optimization problem. The optimal line current is achieved when the non-useful current components are eliminated. This approach uses the Lagrange multiplier method for the calculation of the active current component. If a multi-phase load is fed by the voltage vector u, the instantaneous active current is defined as the "minimum theoretical" current that will deliver the same power to the load. The minimum is defined according to the instantaneous norm:

$$\left\| i_p \right\| = \left(i_p^T \cdot i_p \right)^{1/2}$$

Using the Lagrange multipliers method, the active current component is found in [27] to be,

$$i_p = u\frac{p}{\|u\|^2},$$

where p is the instantaneous active power, defined as $p = u^T \cdot i$. On the other side, the instantaneous reactive power is the "remaining current". Therefore, defined as,

$$i_q = i - i_p = i - u\frac{p}{\|u\|^2}$$

The reactive power is also equal to $q = u_q{}^T i$, and the two current components i_p and i_q result orthogonal,

$$i_q^2 = i^2 - i_p^2$$

In case the magnitudes are periodical, the instantaneous norm becomes the average norm, (or the rms value in electric circuits). And the instantaneous active current becomes just the active current and is obtained using the rms value,

$$U = \left[\frac{1}{T}\int_0^T u^2 dt\right]^{1/2}$$

$$i_a = u\frac{P}{U^2}$$

Where P is the average power dissipated by the circuit load, which is the one that is being compensated. The compensation principle derived from this technique in a circuit with periodic magnitudes will leave on the circuit portion just this last active current i_a.

D. Type 4

All the analytic tools discussed so far attempt to provide understanding for the meaning of the current components in the circuit, but only from an analytical point of view. There is no relationship between the current components and the physical elements in the circuit, as it is for example the correspondence between resistance to active current, and reactance (inductance, capacitance) to reactive current in a circuit where the current magnitudes are sinusoidal. Differently the approach by Czarnecki [29], [30] attempts to provide a basis for giving physical meaning to the current components. The approach assumes a sinusoidal or quasi-sinusoidal voltage in an AC circuit provided by a voltage source and the distortions are manifested in the currents. In the case of linear, time invariant load, the load current can be expressed as a sum of three components,

$$i = i_a + i_s + i_r$$

Where i_a is the active current component, i_s the scattered, and i_r the reactive current component. In a similar way than previous approaches, the active current component is obtained from the equivalent conductance,

$$G_e = \frac{P}{U^2}$$

Additionally, if the load has an admittance that depends on the harmonic frequency, which is generally the case since a simple capacitor or inductor change with frequency.

$$Y_n = G_n + jB_n = Y_n e^{-j\varphi_n} \qquad n = 0, 1, 2\ldots$$

According to [29] the two current components i_s and i_r are calculated by the following expressions,

$$i_s = (G_o - G_e)U_o + \mathrm{Re}\sum_n (G_n - G_e)U_n e^{jn\omega_1 t}$$

$$i_r = \mathrm{Re}\sum_n jB_n U_n e^{jn\omega_1 t}$$

As in the previous decomposition, all this current components are orthogonal. The first component i_a represents the active current according to the definition previously presented. The second component i_s represents the current increase produced by the change of the load conductance with the frequency. Moreover, the reactive current i_r represents the current increment due to the reactive components of the load.

In case the load is non-linear or time-variant, the load current form will be different form the linear case under the same conditions. The additional harmonic components of orders not present in the voltage can be identified as another current component, i_g

$$i = i_a + i_s + i_r + i_g$$

Where,

$$i_g = \mathrm{Re}\sum_{n\in K} I_n e^{jn\omega_1 t}$$

And K is the subset of current harmonic orders not present in the voltage. The four current components are still orthogonal, and the current component i_g is called in [29] the "generated harmonic current". In case of three-phase circuit, the current decomposition goes one step further identifying a component that is due to the load unbalance, i_u. The current composition is then:

$$i = i_a + i_s + i_r + i_g + i_u$$

Where the i_u harmonic components I_{un} can be calculated from the voltage harmonic components U_n and the load unbalance admittance A_n

$$I_{un} = A_n U_n$$

So far the method has identified different source of current distortion that will produce different power components and the physical reasons for the existence of these components. According to the last current decomposition and under the assumed voltage conditions the apparent power in the circuit can be decomposed in

$$S^2 = P^2 + D_s^2 + Q^2 + D_g^2 + D_u^2$$

Where P and Q are the power active and reactive components and the origin of the three distortion powers, D_s, D_g and D_u has been identified. Nevertheless, this physical interpretation of the current components is valid under more restrictive hypotheses with the voltage allowed to have a certain degree of distortion and a matrix A_n that can become of difficult calculation.

V.2. Evaluation of the Instantaneous Power Theories

To start studying the characteristics of the power theories formulation under general circuit conditions a three-phase, four-wire circuit with unbalanced load and non-symmetrical voltage source was used. The circuit is presented in Fig. 2-10. A current compensator that will behave according to the theory under analysis is included in the circuit. In this way the appropriateness of the different formulations can be tested.

The circuit in Fig. 2-10 was simulated in a circuit simulator. The study evaluated some of the phenomena relevant at certain layers in the reference model presented in Fig. 2-7 by mean of calculating the different power components that appear in the circuit. The evaluation included: compensation of non-active current components and its relation to the energy storage capacity required for compensation, line losses, transmission efficiency, and harmonic components. All different formulations work appropriately for the case of three-phase, three-wire systems without significant differences. The situation change when the four-wire is present in the system, but this case is analyzed with detail in the next paragraph. Considering an a-b-c representation of the three-phase components the current and voltage are written as:

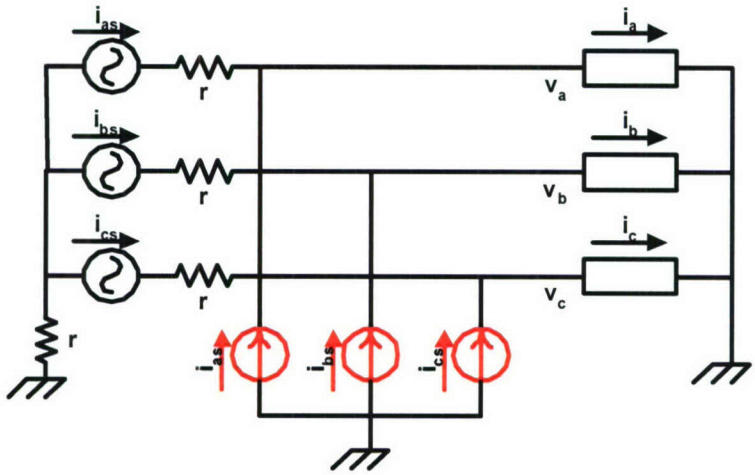


Fig. 2-10 Three-phase four wire circuit with non-symmetrical source and unbalanced load for testing the instantaneous power theories

$$i(t)=\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \qquad v(t)=\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix}$$

It was found that a good and compact representation of the instantaneous active and reactive powers is given by the dot product and cross products of the phase magnitudes respectively. This products can be calculated using the *i(t)* and *v(t)* representation in αβ like the original formulation in [18] or abc coordinates like in [21].

$$p(t)=v(t)\bullet i(t)$$
$$q(t)=v(t)\times i(t)$$

Optimal compensation is defined when the losses in the transmission line are minimal. The losses are proportional to $\|i(t)\|^2$, or to p^2+q^2. This is achieved when all the power is active and the reactive power is zero. According to the previous definitions it can be interpreted that the voltage and current vectors must be aligned, whatever the coordinate system. Additionally, the total power injected by the compensator must be zero. Errors in meeting these requirements would indicate that the interpretation of the electric phenomena in the circuit is not correct.

A. Four-wire System Analysis

Differently from the three-wire system, when it comes to four wire systems unbalanced conditions and magnitude of neutral currents must also be considered. In this case the mathematical interpretation is not as simple as in the case of three-phase, three-wire systems because the cross product is not defined in the four-dimensional case and the same definitions cannot be extended. The solution comes by means of a space vector transformation (SVT) [23]. Looking at the three-phase case, the instantaneous power definitions can be reduced to only two dimensions (α and β) after the Clarke SVT. The advantage of applying that SVT, or the Park transformation, is the reduction of three linearly dependent magnitudes to two linearly independent ones that provide a full description of the system. Therefore, if a proper SVT is applied for the four-dimensional case, it must be possible to reduce the coordinates to three linearly independent magnitudes and use the cross and dot product definitions of the instantaneous active and reactive power in a three-dimensional system. This has already been proposed making possible to use the instantaneous power theory postulates for the four-wire circuit [24]. The equivalent to the Clarke transformation for the four-wire system is given by the following matrix:

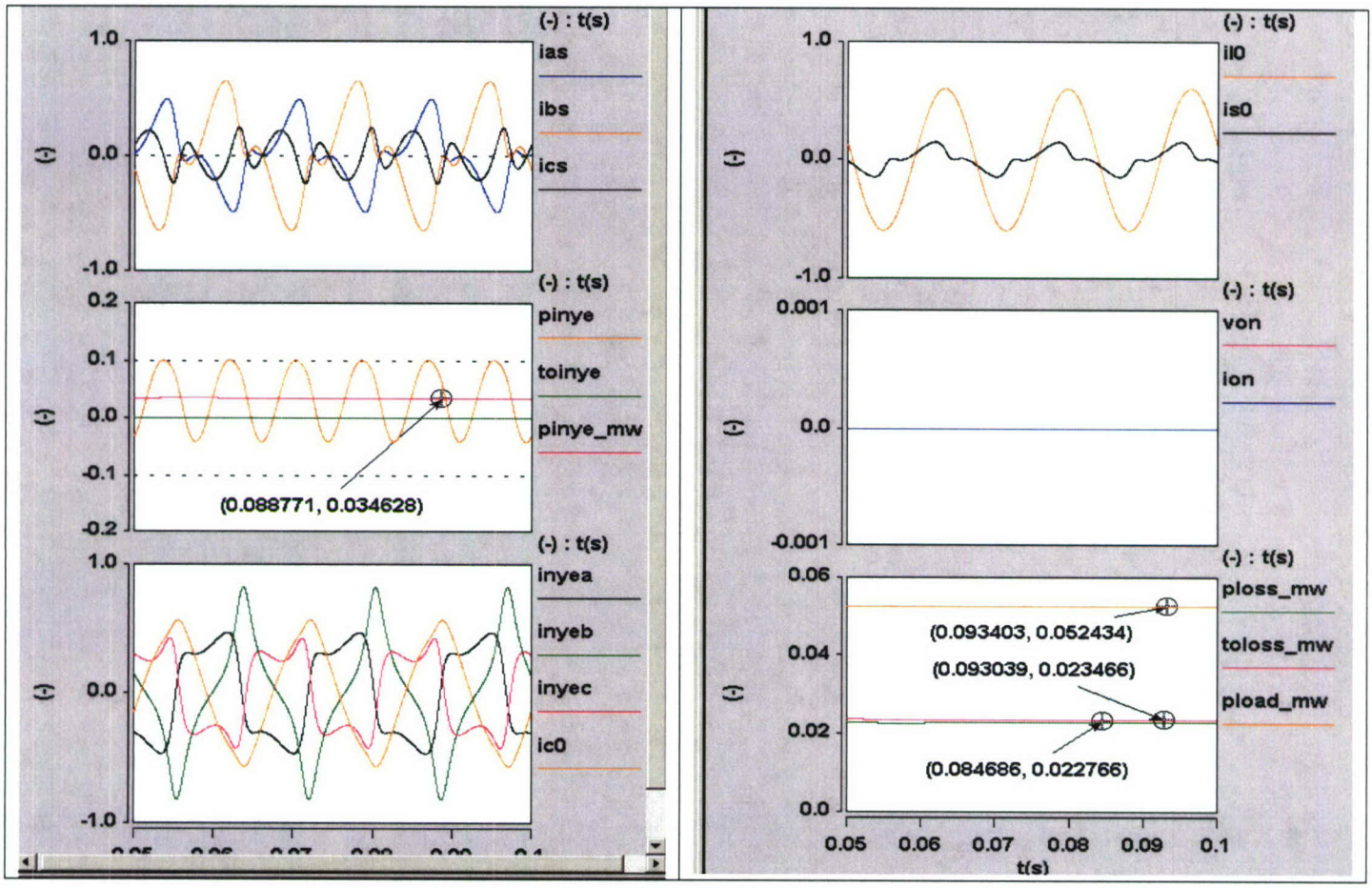


Fig. 2-11 Voltage and current waveforms in a four-wire circuit where the compensation based on power definitions in the 4-dimensional SVT

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}$$

The circuit in Fig. 2-10 was simulated in the unbalanced asymmetrical case and the results are presented in Fig. 2-11. That Figure shows the compensated and injected phase currents i_{abcs} and $i_{inyeabc}$ respectively, as well as the neutral current in the load, i_{lo} and the compensated source neutral current i_{so}. The total power injected by the compensator is toinye, which is instantaneously equal to zero.

In a different way, the type 3 formulation approaches the four-wire case by adding an extra term in the optimization model, which produces an additional compensating current i_o. Therefore, the instantaneous current is now given by the expression below, which can be represented by three orthogonal components like in Fig. 2-12.

$$i = i_p + i_q = \frac{p}{\|u\|^2} u + i_o + \frac{q}{\|u_q\|^2} u_q$$

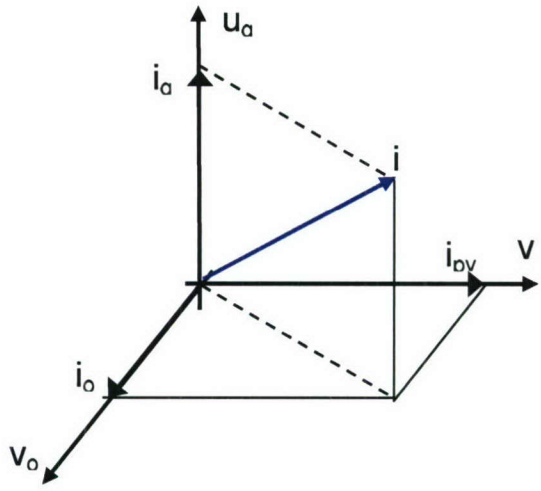
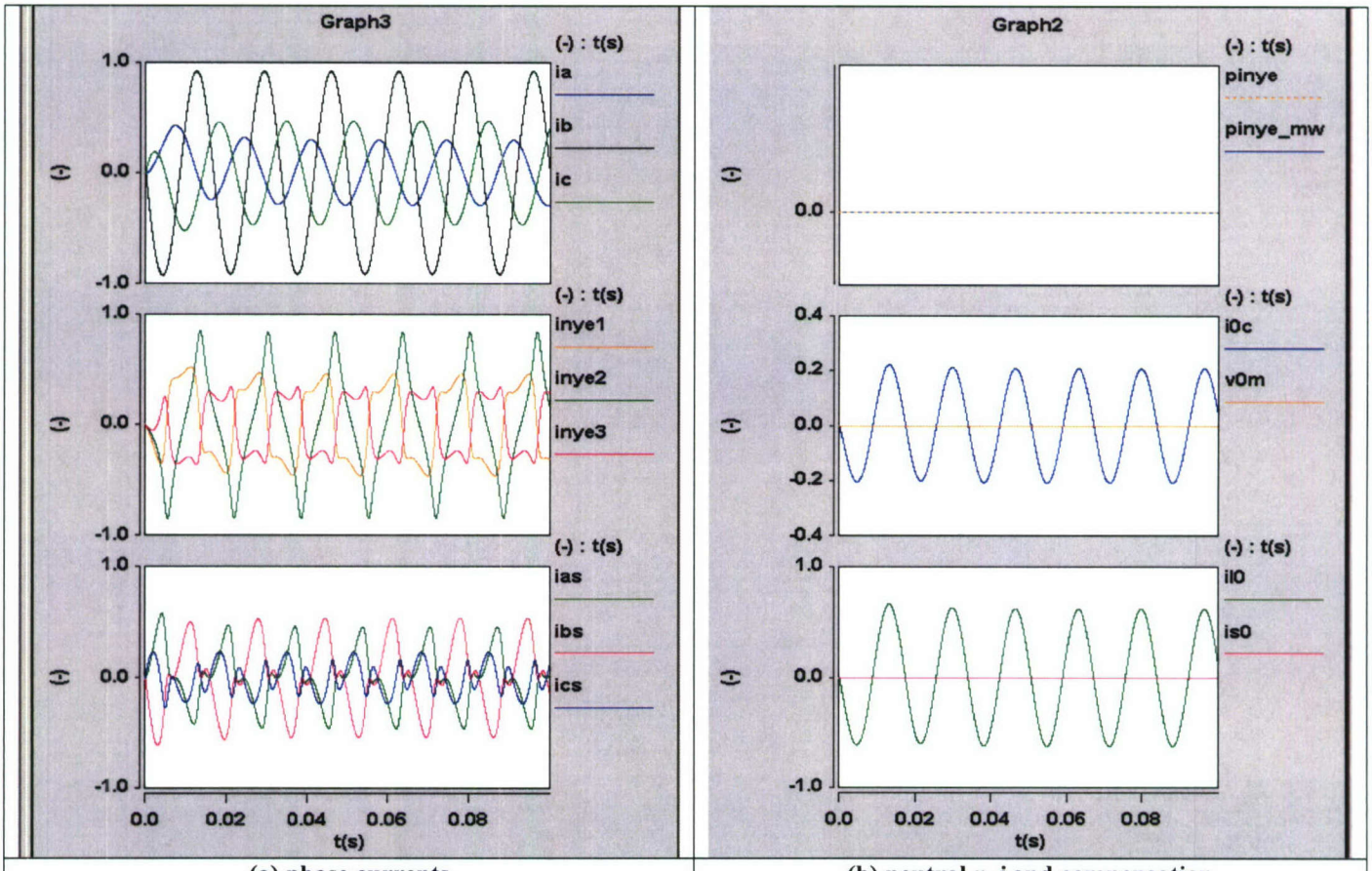


Fig. 2-12 Current decomposition for the four wire case according to the type 3 method

The instantaneous power corresponding to the previous current is given by:

$$u \cdot i_p = \frac{p}{\|v\|^2} u^T v + u^T i_o = p + p_o$$

With the original component p and the additional term p_o given by i_o. The circuit compensation according to this approach produces the results shown in Fig. 2-13.



(a) phase currents

(b) neutral v, i and compensation

Fig. 2-13 Compensation according to the type 3 approach, (a) three-phase magnitudes, (b) injected power and neutral magnitudes

The compensation currents are $i_{inye123}$ and the source compensated currents are i_{abcs}. The load neutral current is i_{lo} and the compensated current is i_{so}. A conceptual difference is observed in the neutral compensated current when comparing to the results presented in Fig. 2-11. It is also important to note that similar than Fig. 2-11, the compensated current in this last Figure are not free of harmonics. In this aspect the instantaneous compensation introduces harmonics in the system (energy source).

B. Evaluation of the simulation results

In order to evaluate the different types of instantaneous power theory formulations the circuit in Fig. 2-10 was simulated at different unbalance conditions. The FBD method produced different results according to its two versions, instantaneous and one-line period average. The time frame of each equation is different, and this fact is related to the electric phenomena considered. The test results for the four-wire system are summarized in Table 2-3. The most relevant and general result establishes that minimizing the instantaneous transmission losses does not mean being free of harmonic content; and in order to achieve harmonic compensation it is necessary to use one period averaging. In this way, the two possible definitions for the active current component are valid in its respective context. These two definitions are expressed in the FBD method as,

$$i_a(t) = \frac{p(t)}{\|u(t)\|^2} u(t)$$

$$i_a(t) = G \cdot u(t), \text{with } G = \frac{\frac{1}{T}\int_0^T ui\, dt}{\frac{1}{T}\int_0^T u^2\, dt}$$

Table 2-3 Results of the instantaneous power theory analysis

	P source (kW)	P load (kW)	Line loss (kW)	P injected (kW)	I neutro (A_{pk})
Akagi's matrix 4-wire	0.691	0.545	0.066	0.079	0
Peng's "generalized"	0.566	0.538	0.027	0	0.5
Lagrange multipliers	0.498	0.552	0.017	0.071	0
4-dimensional SVT	0.569	0.546	0.023	0	0.148
FBD instantaneous	0.569	0.546	0.023	0	0.148
FBD period average	0.559	0.546	0.0125	0	0.0703

The results that are obtained by applying the described SVT to the voltages and currents in the four-wire system are the same as the ones produced by the FBD method in its instantaneous version. An additional conclusion for four-wire systems establishes that overall optimal conditions do not mean that the current in the fourth conductor must be zero.

The results in the Table 2-3 correspond to the case of unbalanced load, asymmetrical source. The only methods that achieve the goal of not requiring energy storage are the FBD, the one based on the four-

dimensional SVT, and Peng's generalization. However, this last method does not present a good performance because the neutral current becomes very large. In addition, even when the active power injected is zero, the operation of the circuit is far away from optimal. The compensation based on the four-dimensional SVT and the FBD instantaneous definitions produce exactly the same results. And represent the optimal circuit operation without (theoretically) any energy storage. According to the losses criteria, the compensation based on the FBD average method improves the circuit performance over the instantaneous case. But strictly speaking this method does require certain energy storage. The total energy exchange over one-line period may be zero, but the instantaneous exchange is not zero, Fig. 2-1.

Other criteria for analyzing the compensation may also be required. The use of the strict instantaneous values introduces harmonic distortion in the line currents. This may not be desirable in most of the cases. On the other side, if one-period average compensation is used, no harmonic distortion is introduced as it is shown in Fig. 2-2; but then, some amount of energy storage is required, as it was mentioned. The presence of energy storage may also introduce non-desirable issues like some degree of instability according to the characteristics of the power system.

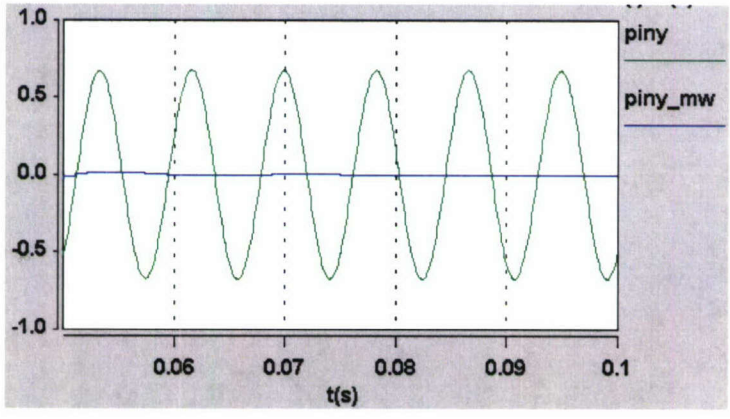


Fig. 2-1 Power exchanged between system and energy storage

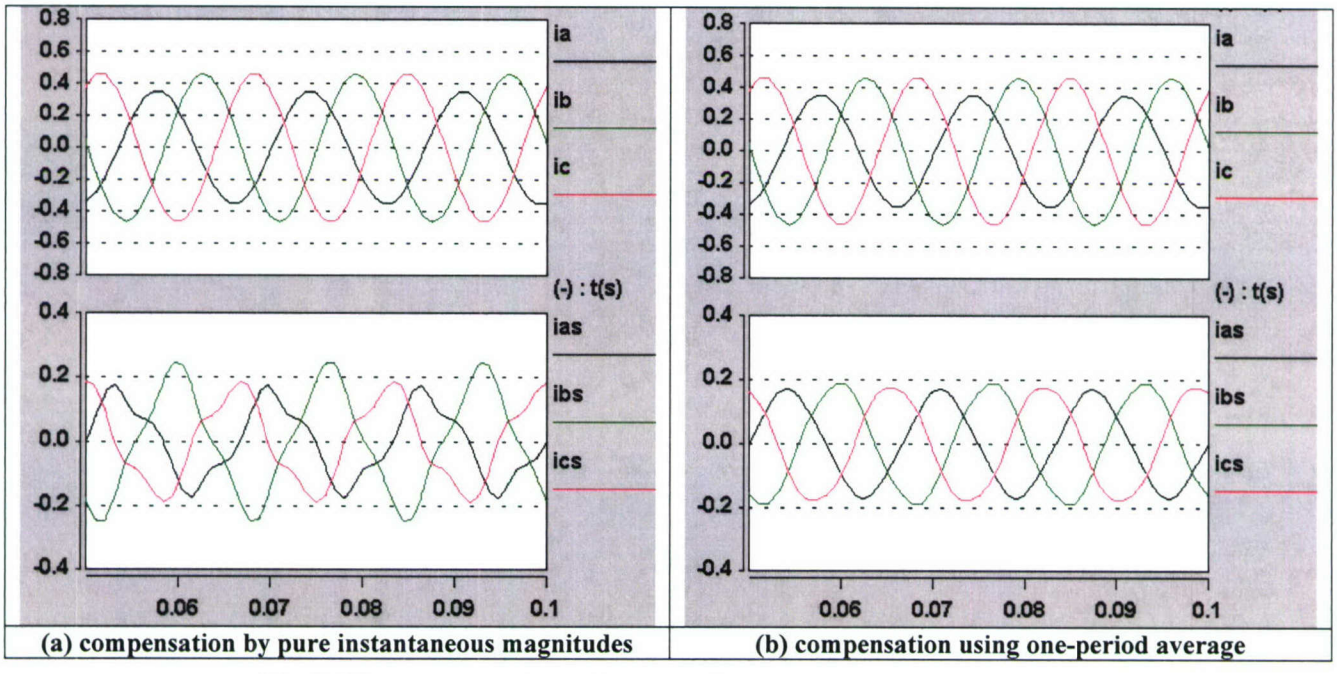


Fig. 2-2 Instantaneous (a) and average (b) compensation methodologies

V.3. Power theories for single phase circuits

The previously analyzed formulations are defined for the multi-phase systems. These original theories extract information on the energy process based on the inter-relation among the different phase components. Those kinds of relations are not present in the single-phase case. Nevertheless, the instantaneous power in single-phase circuits has been object of previous investigations. Because our analysis goes inside the power converter and phase by phase, a formulation valid for single-phase is required. This is done in the next paragraphs.

Some instantaneous power formulas applicable for single-phase circuits have been proposed [31]-[35]. From those, the equations in [31] propose to obtain a fictitious voltage and current in quadrate with the original ones by de-phasing them. If *u(t)* and *i(t)* in the circuit are:

$$u(t) = U \cdot \cos(\omega t)$$

$$i(t) = I \cdot \cos(\omega t - \varphi)$$

The same *u(t)* and *i(t)* de-phased ninety degrees are called the "imaginary" components.

$$u_{im}(t) = U \cdot \sin(\omega t) = U \cdot \cos\left(\omega t - \frac{\pi}{2}\right)$$

$$i_{im}(t) = I \cdot \sin(\omega t - \varphi) = I \cdot \cos\left(\omega t - \frac{\pi}{2}\right)$$

The original and this last imaginary components can be seen as U and I components in an α-β system. Then the active and reactive instantaneous powers, p-q are calculated by using the same formula in a similar way than in a three-phase circuit; *p* is the dot product and *q* the cross-product of *u(t)* and *i(t)* respectively.

$$p = u \cdot i = u_\alpha i_\alpha + u_\beta i_\beta$$

$$q = u \times i = u_\alpha i_\beta + u_\alpha i_\beta$$

Using these definitions of p and q it is also possible to calculate the equivalent of the current components presented in the previous section. This equivalence between the three-phase (FBD method) and single-phase formulation is summarized in Table 2-4.

Table 2-4 Equivalence between FBD method and the single phase current components

FBD method	Single-phase	Calculation
Power	Instantaneous active	$i_p = \frac{u}{u^2 + u_{im}^2} \cdot p$
Powerless	Instantaneous reactive	$i_z = -\frac{u_{im}}{u^2 + u_{im}^2} \cdot q$
Active	Average power	$i_n = -\frac{u_{im}}{u^2 + u_{im}^2} \cdot Q_{AV}$
Non-active	Average reactive	$i_a = \frac{u}{u^2 + u_{im}^2} \cdot P_{AV}$
Variation		$i_v = -\frac{u_{im}}{u^2 + u_{im}^2} \cdot (q - Q_{AV})$

The single-phase formulation presented in [31] and discussed here differs from the three-phase case in the necessity of creating the fictitious components u_{im} and i_{im}. This fact requires that the original magnitudes *u(t)* and *i(t)* have four-side symmetry, meaning that the time evolution is symmetric to the quarter period.

If this condition is met, the single phase calculation provides accurate results; otherwise they depart from accurate values. This last case exists when the electric magnitudes have harmonic components that do not meet with the one quarter period symmetry. How much the results are inaccurate depend on how large are those harmonic components.

VI. Characteristics of the Energy Flow

Several formulations of the so-called instantaneous power theories were tested in simulation using different circuit topologies in order to describe the energy flow at the points of the system represented in Fig. 2-14.

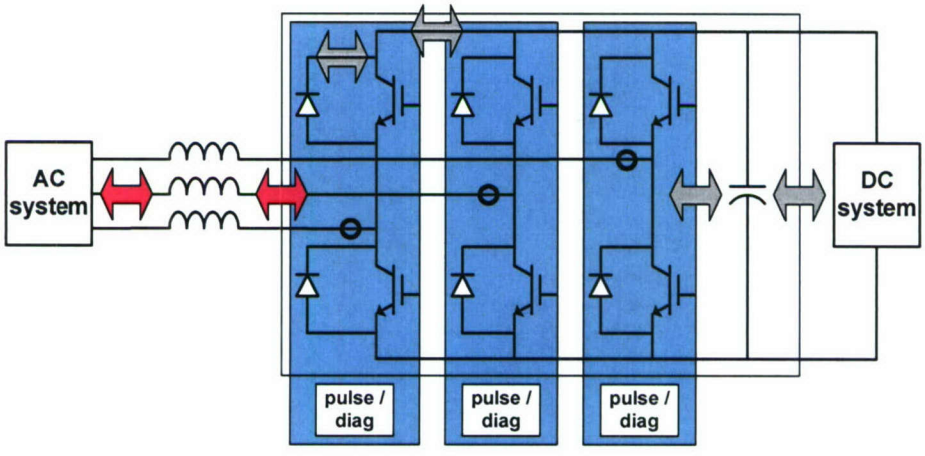


Fig. 2-14 Generic power electronic converter

In the same way than the three-phase case. The primary classification of the instantaneous power definitions is by the time frame using in their definition. In this way, the two possible definitions for the active current component according to [32]:

$$p(t) = u(t) \cdot i(t) = u_\alpha i_\alpha + u_\beta i_\beta$$

$$P_{av}(t) = \frac{1}{T} \int_0^T p(t)\, dt\,,$$

The fact that the time frame of each equation is different is related to the phenomena they can be used to analyze. Particularly, in the single-phase circuit analysis, if the *v(t)* and *i(t)* waveforms have four-side symmetry; the calculation period can be reduced to one quarter of the line cycle, *T/4* [32]. The difference between the two power definitions presented gives the oscillating component of the instantaneous power active and reactive components.

$$p(t) = P_{av}(t) + \tilde{p}(t)$$

$$q(t) = Q_{av}(t) + \tilde{q}(t)$$

The variation components of the power are related with the variation components of the currents. The variation reactive current component was already shown in Table 2-4 and is given by,

$$i_v = -\frac{u_{im}}{u^2 + u_{im}^{\ 2}} \cdot (q - Q_{AV})$$

VII. Conclusion

Having previously characterized the power converters in its information/control dimension [2], it is also important to know the characteristics in the energy-processing dimension. For this purpose it is necessary

to find appropriate analytical tools and models. Following the idea obtained form the control system analysis, a hierarchical reference model of the energy processing characteristics is useful in establishing the proper domain of application of the different analytical tools. In this way, a multi-layer hierarchical reference model is an appropriate architecture that can facilitate the analysis, design, and construction of power electronics systems using the PEBB concept. Although there may be variations in the control functions depending on the purpose of the system, the analysis shows that different applications present in the ship power system share a common set of functions. The idea and methodology originally developed for modularizing the controllers of power electronic converters were found to be applicable in a wider range. Therefore, that same methodology was followed for the power stage case. The functional analysis is the first step in the method and it provides the basic system partition. A consequence of that partition is the preliminary identification of the PEBB as the portion of the converter that has a common set of functions.

In addition of the PEBB identification, the functional analysis identifies each layer of the hierarchy with a characteristic set of functions. This set also relates to the electromagnetic phenomena that are more relevant at each layer. Some of that relevant phenomena have been presented together with the time characteristics and resolution required to represent them. This required time resolution, necessary for describing the phenomena, is also a basic characteristic that the analytic tools describing that phenomena must have. In order to proceed with a more accurate power stage partitioning a better tool for analysis is required. Fig. 2-3 presents a summary of the analysis of candidate tools for analyzing the energy flow. Some of those analytic tools candidates at the converter level have been studied and described in this chapter.

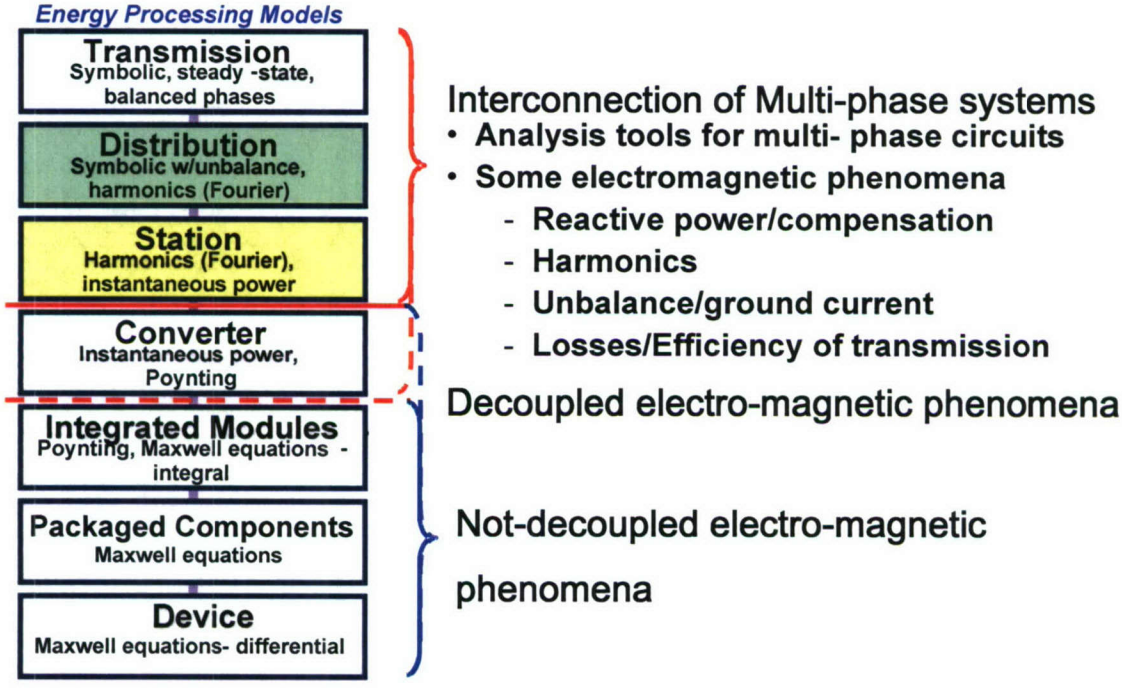


Fig. 2-3 Hierarchical reference model of power analytic tools and some of the electromagnetic phenomena under consideration

The actual PEBB modules may be of different topologies and ratings, but the way to use the PEBB modules can be standardized based on common control architecture and interface characteristics. Moreover, good insight on how the energy is processed will increase the understanding of the behavior of

systems, sub-systems, components, and interactions between them, providing good guidelines to the process of modularization of power electronic systems. Future research directions will focus on developing methodology and rationale that can lead to open system architecture for power conversion systems.

In order to complete the steps in the partition method the phenomena at the interfaces must be quantified. This task is done in the next chapter, which presents the analysis of the interface characteristics using the tools analyzed in the present chapter.

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Chapter 3 POWER INTERFACE CHARACTERIZATION

I. Introduction

On modular Power Electronics Building Block (PEBB) based electrical power systems, [1] presented the design of a distributed digital control architecture using as basis the analysis of the information processing required to control each individual power converter. Later, further analysis of the control requirements and the information flow in converters, together with the search for meaningful ways to partition these systems, led to the proposition of a hierarchical reference model for characterizing power electronic conversion systems [2]-[3]. Analysis of the information flow in some power converter applications is shown in Fig. 3-1. The chart in that Figure provides a figure of merit of the information managed by the control system. On the contrary to previous information flow analysis, the energy flow in power converters was thoroughly considered and analyzed in this case. Other outcomes from a sound energy flow description are the refinement of the partitioning approach used to identify modules within power systems, as well as the ability to characterize the interfaces between these same modules. Key results obtained from this study are presented in this Chapter, contributing to and extending the hierarchical reference model presented in [2][3]. The analysis presented is performed using suitable analytic tools studied in [3], namely the power theories in [4-5].

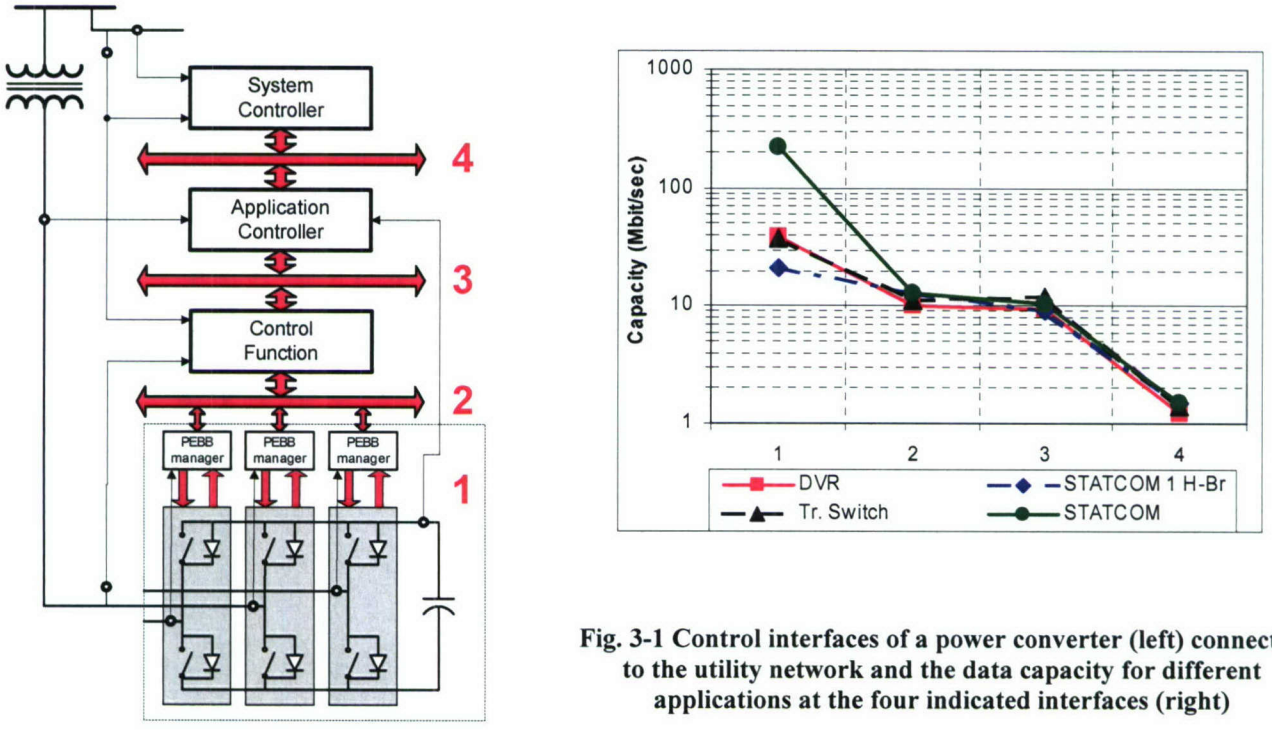

Fig. 3-1 Control interfaces of a power converter (left) connected to the utility network and the data capacity for different applications at the four indicated interfaces (right)

II. Power Flow and Interface Characteristics

The power flow in a power electronic system should be studied using analytic tools that provide a good balance between accuracy and simplicity. Additionally they must be able to describe the energy process

within the subsection of the system under study with good enough resolution. In a previous paper of the authors, different formulations of the generally called instantaneous power theories were analyzed [3]. That work showed that only some of the proposed formulations produce meaningful results for generic conditions, while on the contrary many of them are valid only under very particular conditions. Additionally, regarding power analysis tools, the characteristics of energy flow in the power system at a certain hierarchy levels needs to be described in terms of the corresponding time resolution and energy interaction components (like active, reactive, variation or other power components.)

Most of the instantaneous power theories have been proposed for three-phase circuits. In this Chapter, in addition to three-phase analysis, single-phase power theory formulations are used in order to analyze the power flow and energy components at different sections or points within converters [6]. On their analysis, the magnitude and evolution of each power component provide a description of how the different parts of the system handle the electric energy. This information may be conveniently displayed graphically, in which case it may be analyzed to discuss different issues relating the power system modularization, specifically partitioning and interactions. For instance, subsections of systems having large power component interactions may be candidates to be grouped into a single module, while low power interaction may indicate a proper place for drawing a boundary and hence partition the system.

In this Chapter the energy components and the respective values they reach at different points of the system are calculated for a three-phase circuit topology using computer simulation. The models and results of that study are later used for characterization of the interfaces that exist among the modules in a feasible proposed partition of a power electronics conversion system. In this way, the proposed analysis tool enables this proposed partition to be modified and or refined presenting a step-wise design and analysis tool.

II.1. Interface Characterization

In a modularized power electronics conversion system the characteristics of the modules at points of connection are of major relevance since they define the conditions and rules for their own interconnection. In accordance to the concept of hierarchical knowledge, only some of the characteristics of the components of a power electronic module are required to describe its interface at every hierarchy layer. This is represented schematically in Fig. 3-2, where the final goal is to obtain interface descriptions according to the proposed hierarchy.

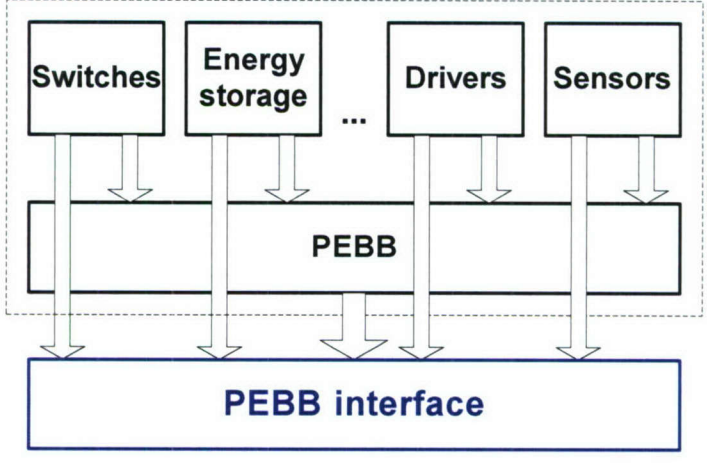

Fig. 3-2 Concept of interface characterization; while a comprehensive description of the subsystem might be considerably extensive, only some of that information is relevant for the interconnection aspects

The module interface description starts from its connection points. From the electric energy point of view, those connection points are the terminals. In a phase leg like in Fig. 3-3 the electric characteristics seen from the connecting AC and DC terminals give the desired description. At the DC interface, not only the amount of DC power handled is relevant, but also harmonic components that may be present, and voltage and current average and peak magnitudes. It is also important to know the combination of voltage and current that does not carries power producing non-active power components.

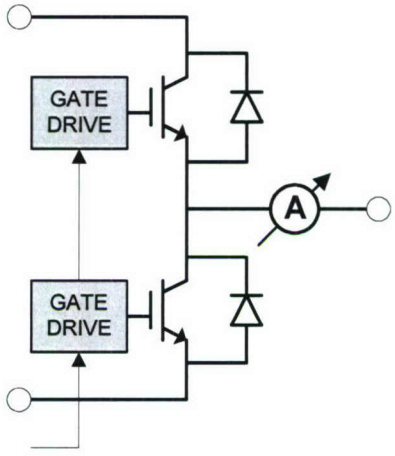

Fig. 3-3 Phase leg or single-pole double-throw switch with AC and DC connection terminals

On the AC side, the identification and quantification of the non-active power components acquires even more significance. Additionally, the active and reactive power and their relation with the voltage and current ranges (average, peak, rms) is part of the description.

A. Interfaces in a Power Converter

A partitioned power converter presents several points where it is important to know the energy flow. Fig. 3-4 shows a three-phase converter with PEBB modules given by each phase-leg and several of the points where it is important to know the energy flow. Further analysis in this Chapter will provide data on the energy exchange through the points represented in Fig. 3-4.

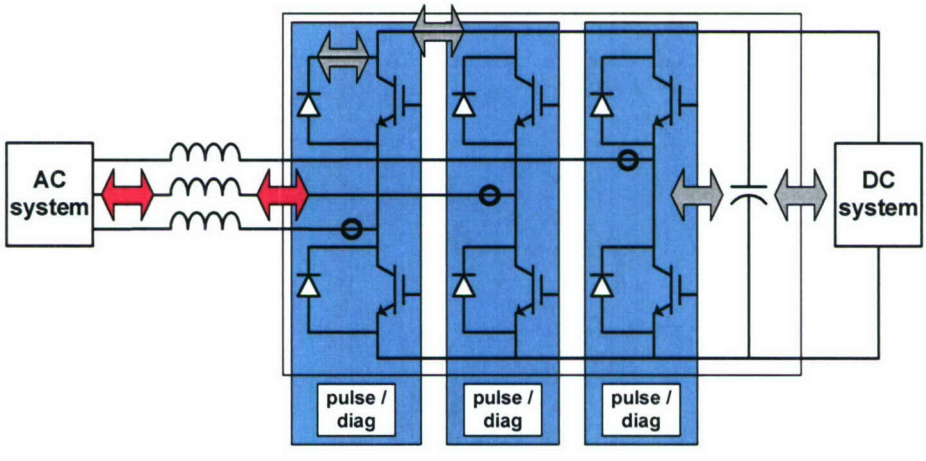

Fig. 3-4 Three phase power converter partition and points of description of the energy flow

B. Evaluation of Power and Current Components

The evaluation of the converter interfaces will be done by using the power theories discussed in the previous chapter. For the three-phase evaluation the FBD method is preferred, for the single phase evaluation the formulation presented in [7] is used for the analysis. The instantaneous active and reactive power are given by:

$$p = u \cdot i = u_\alpha i_\alpha + u_\beta i_\beta$$

$$q = u \times i = u_\alpha i_\beta + u_\alpha i_\beta$$

As it was discussed in the previous chapter, one of the most important ways to classify the power definitions is by the time frame they are defined. In case the magnitudes are periodic; their average over that period gives also a relevant value.

$$P_{av}(t) = \frac{1}{T}\int_0^T p(t)\,dt$$

$$Q_{av}(t) = \frac{1}{T}\int_0^T q(t)\,dt$$

Given the two previous power definitions, the power components can be decomposed in two portions. One of them is the average value; the other is the variation or also called distortion value, which gives the oscillation of the instantaneous value around the mean value.

$$p(t) = P_{av}(t) + \tilde{p}(t)$$

$$q(t) = Q_{av}(t) + \tilde{q}(t)$$

The compensation of a single-phase load can be based on this decomposition [7]. And the compensator can respond to the any of the three components Q_{av}, $\tilde{p}$ or $\tilde{q}$ separately or combined. If a total compensation is required, all the three magnitudes must be compensated; but, this may not be always compensation goal. In any case, the capacity requirements in the compensator are different and related to the desired compensation ability.

III. Evaluation of the Energy Flow in a Converter

This section presents the evaluation of the energy flow in a three-phase power converter by making use of the previously discussed formulas. Since our goal is to contribute to the interface characterization from an energetic point of view, the boundaries between modules are specially considered. Fig. 3-5 shows a three-phase boost rectifier with the different points where the power components are evaluated. The magnitudes used and the way the calculation was done is summarized in Table 3-1. In all the points the instantaneous, average and variation components were obtained form the simulation.

When a switched converter operates in the circuit, in addition to the system frequency, it is important to consider the switching frequency. The converter operation creates components at the switching frequency, f_{sw}, which propagates from the connection terminals. In the case of the boost rectifier, this harmonics will propagate at both the AC and DC systems. Therefore, when calculating the average and variation components two periods were considered for the calculation, one corresponding to the system frequency, the other to the line frequency. The way of calculating the power flowing in a circuit with more than one measurement point is in accordance to Blondell's theorem for the power measurement in multi-wire circuits.

Table 3-1 Points of evaluation of the instantaneous power flow in the three-phase boost rectifier

Point of measurement	Active power	Reactive power
Three-phase system	$p(u_a, i_a) = u_a \bullet i_a = u_a i_a + u_{ai} i_{ai}$	$q(u_a, i_a) = u_a \times i_a = u_a i_{ai} - u_{ai} i_a$
Converter terminals	$p(u_{as}, i_{as})$	$q(u_{as}, i_{as})$
Phase-leg	$p(u_{dc+}, i_{leg}) - p(u_{dc-}, i_{legb})$	$q(u_{dc+}, i_{leg}) - q(u_{dc-}, i_{legb})$
PEBB	$p(u_{dc+}, i_{peb}) - p(u_{dc-}, i_{pebb})$	$q(u_{dc+}, i_{peb}) - q(u_{dc-}, i_{pebb})$
Switch	$p(u_{dc+}, i_{leg})$	$q(u_{dc+}, i_{leg})$
DC	$p(u_{dc+}, i_{dc})$	$q(u_{dc+}, i_{dc})$

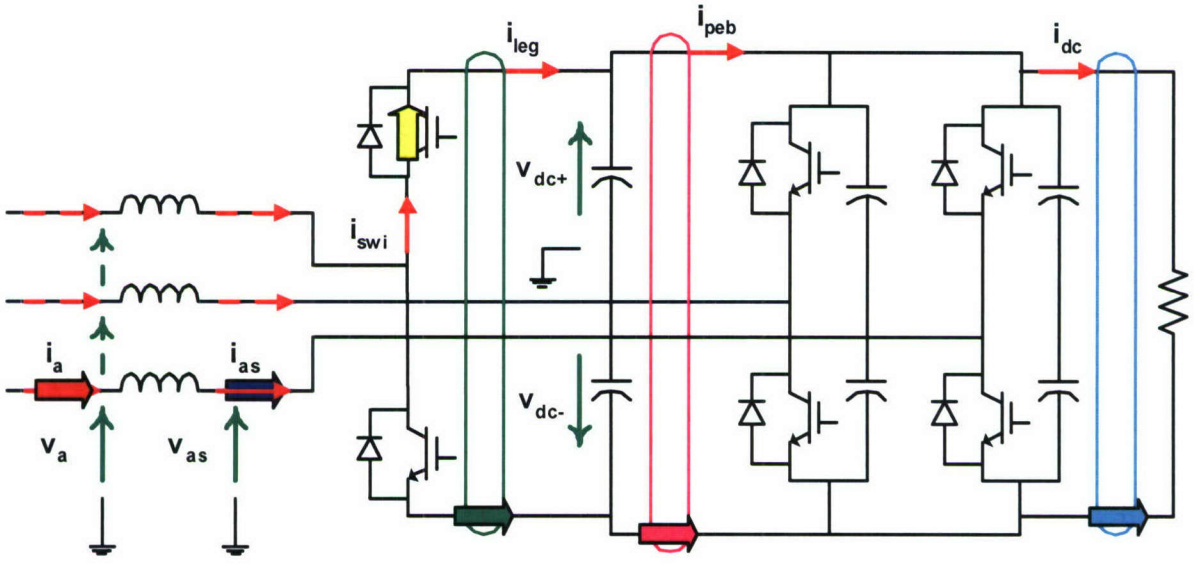

Fig. 3-5 Boost rectifier circuit schematic and different points where the instantaneous active and reactive power were evaluated

Fig. 3-6 shows the simulation results at the PEBB point of measurement calculated with the previously used formulas. It is possible to observe that the large magnitude of the variation component in both p and q. This variation component has the frequency of the switches operation. It is also possible to observe that the average value of the reactive power is null corresponding to a DC circuit.

The results obtained form the simulations show the evolution of the various power components along the converter and the connected power system. In a different way than the active power that only changes due to the conversion to another type of energy, or losses, the evolution of the non-active power components exhibit a more complex evolution throughout the system. The characteristics of this evolution provide an interesting picture of the behavior of the system that gives support for system partition and the concept of building blocks. Furthermore, it can possibly be used in later studies for optimizing the modularization of the system.

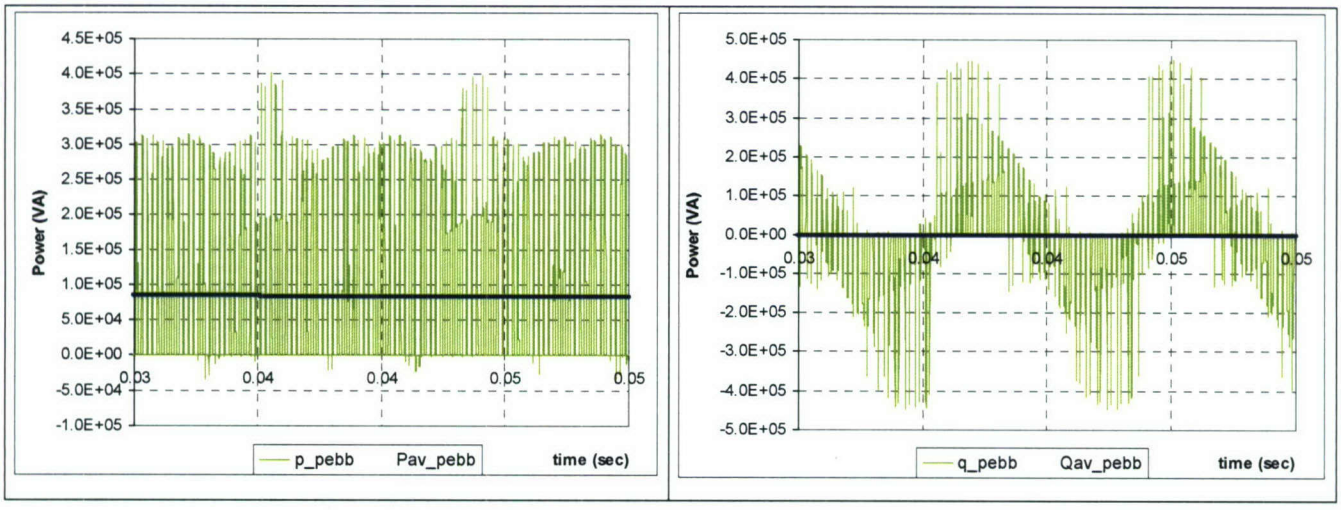

Fig. 3-6 Simulation results for the instant power evaluation at the PEBB. Left: active power; right: reactive power.

A quantitative evaluation of the energy flow and the evolution of the power components, can be observed in Fig. 3-7 through Fig. 3-9. Fig. 3-7 shows the magnitude of the instantaneous active and reactive component for the boost rectifier (Fig. 3-5) when the capacitance is not distributed in each phase-leg being combined at the DC load side. Fig. 3-8 shows the same results including the magnitudes at the switch (the chart is organized in a different way). Fig. 3-9 shows the same magnitudes than Fig. 3-8 but for the case where the capacitance has been distributed in each phase-leg as it is shown in Fig. 3-5. It can be observed that the placement of the DC capacitor in each phase leg, contributes to confine the flow of the different power components in each of the phase-legs. The evaluation of the power components presented in this section is part of the interface description from an electric power point of view. The information shown is based in a pre-determined partition and must be complemented with the evolution of other electrical magnitudes at the boundaries of any proposed partition.

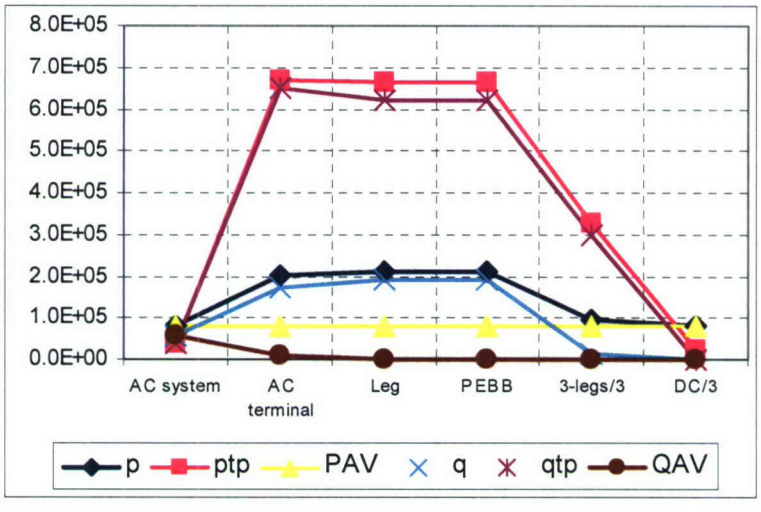

Fig. 3-7 Evolution of the different power components form the AC terminals to DC

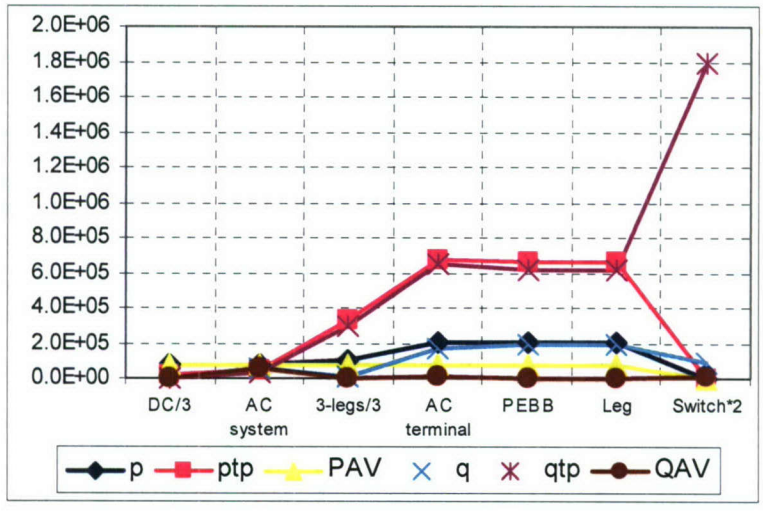

Fig. 3-8 Value of the different power components at the different points of measurement

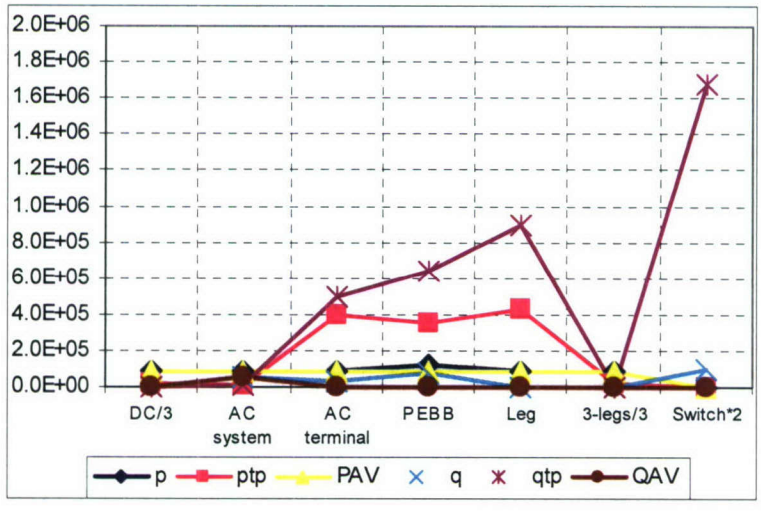

Fig. 3-9 Evolution of power components in a PEBB including capacitor at each phase-leg

IV. Analysis of Energy Processing by a PEBB

In the previous section, using instantaneous power formulations it has been possible to analyze the power flow and identify some of its components (active, reactive, distortion, variation). The combination of the multi-phase and single-phase tools allow for analyzing the power flow in circuits with power converters from the module level. Taking a closer look at the PEBB it can be seen as a power conversion unit from two systems of different frequencies, line frequency (60Hz for example) to DC. This frequency conversion is done by the switching action of the semiconductors in the PEBB. The switching action introduces then other components of the electric magnitudes at the systems at both sides of the PEBB with a frequency that is different form the original one. Therefore, it is necessary to study how the switching action is reflected in the power flow at each of the frequencies involved. Fig. 3-10 shows a PEBB composed of a phase-leg with a power flow direction from the AC to the DC circuit and the most relevant frequency components at each side. Harmonics of the frequencies shown also appear due to the action of the switches. The magnitudes in section III are based on certain periods for the average calculations. Fig. 3-11 shows the evolution of P_{av} and Q_{av} calculated using the average at the switching frequency. It is

possible to see in the figure that P_{av} presents a component at 120 Hz (two times the line frequency). This agrees wit the frequency of the power in a single-phase circuit working at 60 Hz.

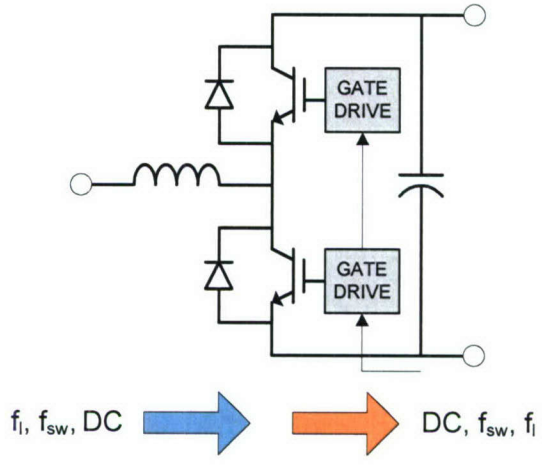

Fig. 3-10 A phase-leg with the power processed and the most relevant frequency components at each side

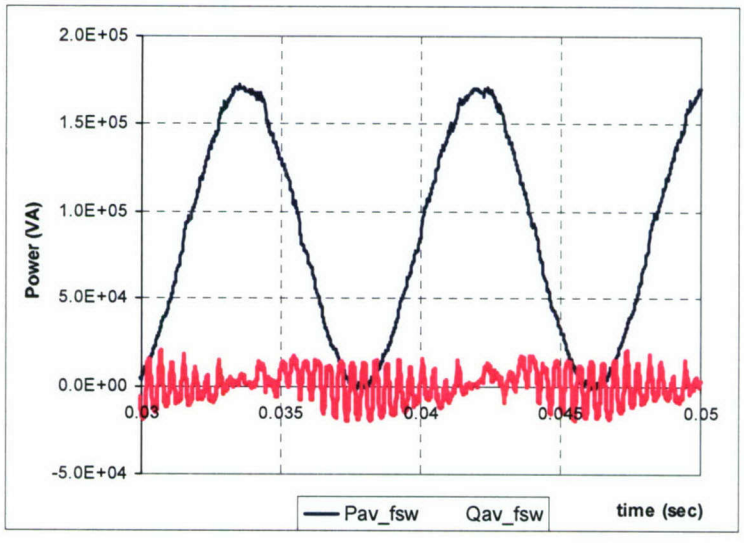

Fig. 3-11 P_{av} and Q_{av} components at the switching frequency on the converter DC side

V. Other Characteristics of the Interfaces and the Instantaneous Power Analysis

The analysis of the power flow in a three-phase circuit is also a good case to analyze and compare the results produced by the three-phase and single-phase formulations of the instantaneous power theories. An analytical comparison was already presented in the previous chapter when describing the instantaneous power theory formulation for single-phase circuits. However, that equivalence was valid in the case the magnitudes have the mentioned four-side symmetry. Having that symmetry mean that certain harmonic orders like even components, cannot be present in the waveform. In such cases the single-phase definitions are only approximated. Therefore, an evaluation of the results produced by single and three-phase was done in order to evaluate the accuracy of the single-phase formulas. Fig. 3-12 shows the boost rectifier schematic with the points of measurement. The comparison was done by means of the compensation currents directly related to the active and reactive power components (see previous chapter,

section V.3). Fig. 3-13 shows the waveforms of the currents calculated using the FBD method [5], while Fig. 3-14 shows the waveforms of the equivalent currents calculated using the single-phase formulation.

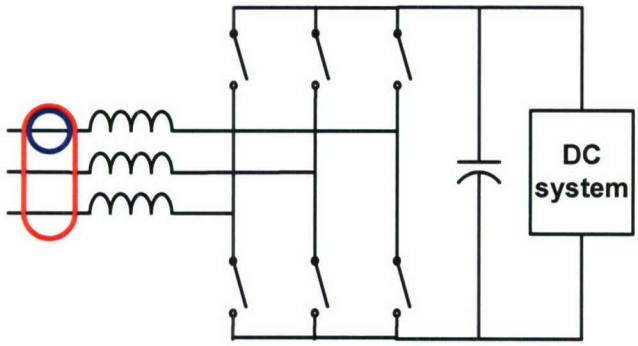

Fig. 3-12 Points of evaluation of the three (red) and single-phase (blue) instantaneous power formulas

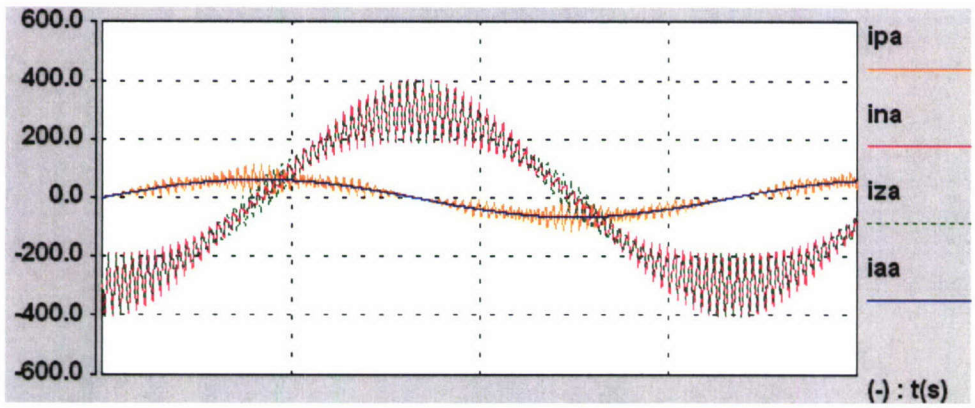

Fig. 3-13 Current compensation components calculated using the three-phase formulation, FBD method

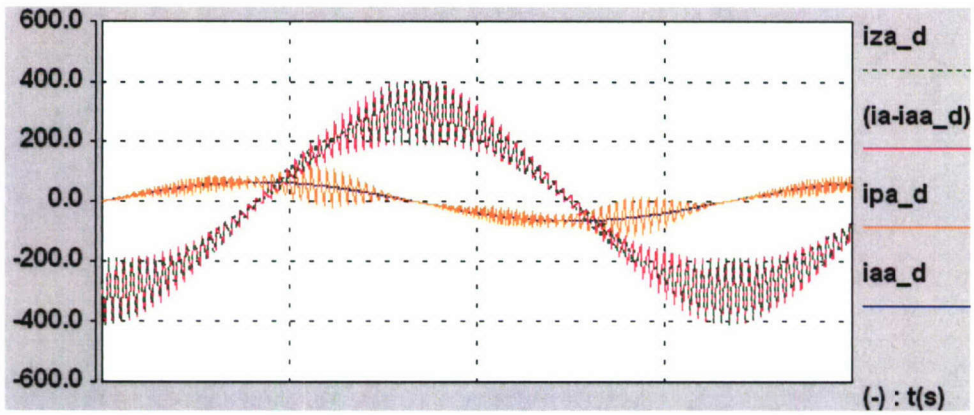

Fig. 3-14 Current compensation components calculated using the single-phase formulation

Comparing the two previous pictures it is possible to see that while the components look similar they are not the same; nevertheless, the differences are not large. This is related with the fact that a converter properly working in steady-state will produce waveforms that are close to the condition of four side symmetry.

The harmonic spectrum of the compensation currents was also evaluated. Previous works already refer to the harmonic components of the instantaneous power [12]. Fig. 3-15 shows the components of the power current at two points in the boost-rectifier circuit. It is possible to observe how the energy conversion produces a shift of the harmonic orders.

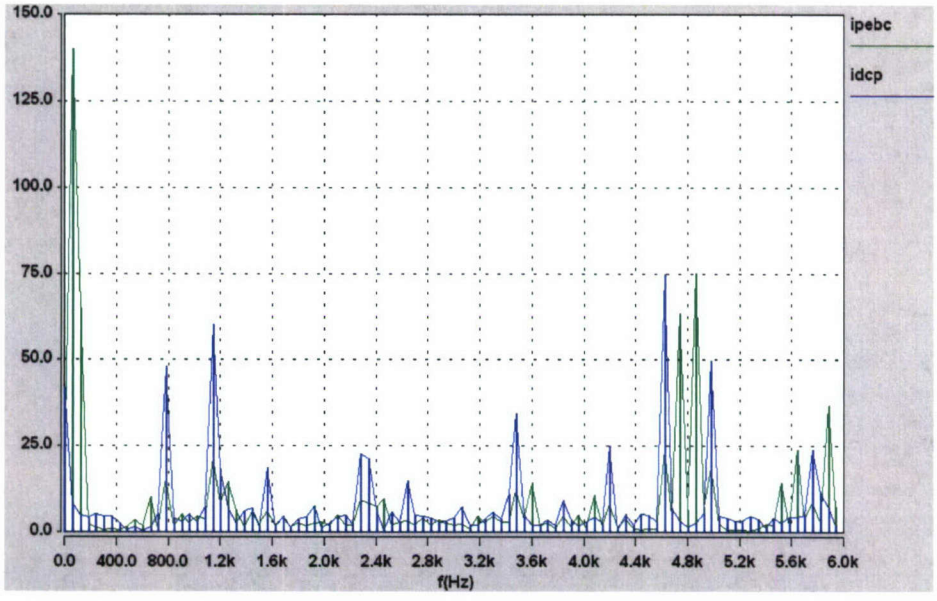

Fig. 3-15 Harmonic spectrum of the instantaneous power component at two different points of measurement

VI. Summary and Conclusions

Some previously proposed power theories have been applied to study the energy flow in a power converter. The analysis shows results of different energy components (active and non-active powers) at a three-phase rectifier obtained from simulation. Modules of the power conversion system can be seen as a portion of the system whose limits confine the non-useful power components that are involved in the energy conversion process. Therefore, finding the boundaries where the amount of power exchange is reduced can help in the process of partitioning and modularization. It can also help in defining better configurations for power converters and modules and to evaluate the usefulness of integrating passive components in a building block, like for example, the DC capacitor or the AC inductor in a phase-leg of a voltage source configuration.

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Chapter 4 HIERARCHICAL PARTITION VALIDATION THROUGH PHYSICS BASED MODELING

I. Defining the Objective

This Chapter presents the energy flow studies through physics-based modeling in order to validate the standard cell hierarchy shown in Fig. 4-1(a); however, in order to validate the depicted one dimensional hierarchy, a three dimensional (3-D) partition as the one shown in Fig. 4-1(b) is used as an overview map. This cube map provides an overview of how different aspects of the system are intertwined and linked with the other aspects of the system providing a more in-depth partition to the standard-cell hierarchy.

Physics-based analysis derived from Maxwell's Equations allows engineers a complete assumption-free view of the electromagnetic behavior exhibited by a circuit. However, most of modern day circuit studies are conducted through lumped parameter analysis with variables such as voltage and current due to the inability of physics based models to analyze complex circuit topologies in a simpler manner. Then, in order to use lumped parameter circuit analysis, some assumptions have to be made as is the utilization of boundary sets. The one major assumption being that all components exist at one point in space so that the travel time from one point of the circuit to another is non-existent. This Chapter presents and discusses the main assumptions used nowadays and required as described to perform lumped-type circuit analysis.

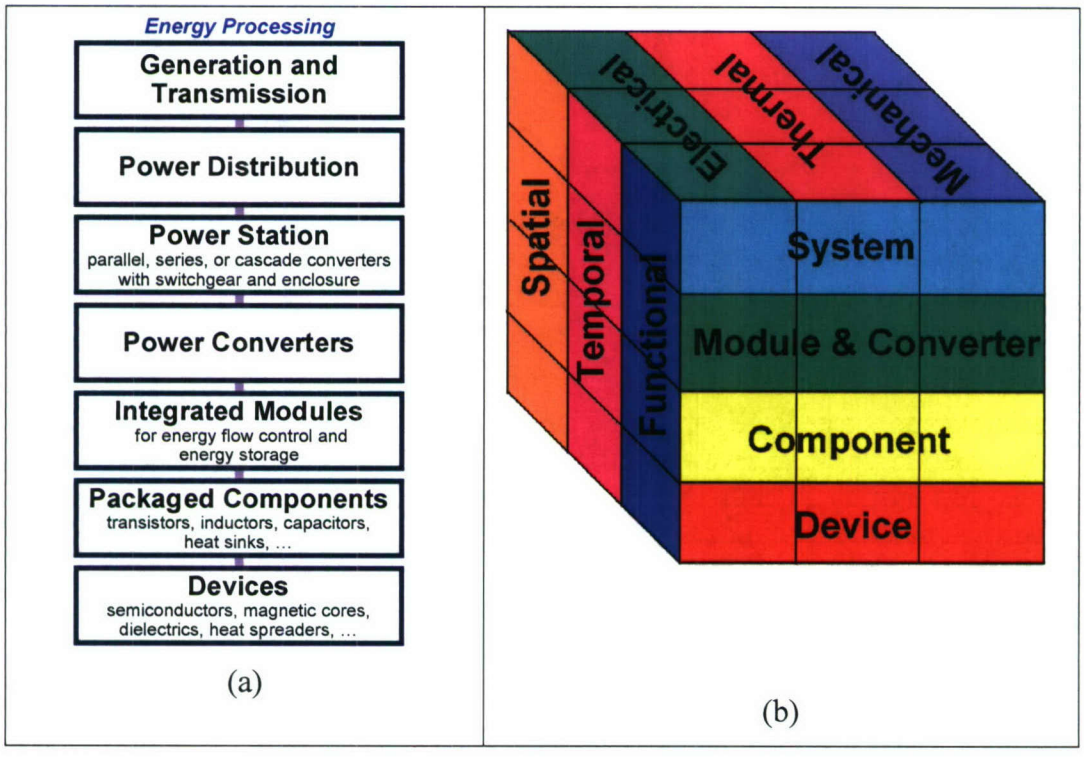


Fig. 4-1 a) Standard cell hierarchy, and b) arubis cube system partition.

Specifically, the physics-based energy flow study will be conducted by means of the Poynting vector. This tool derived from Maxwell's Equations, provides a unique view of how energy flows through a

physical structure. It establishes a link between electrical, thermal and mechanical energy and has proven to be a valuable tool in the design of components and equipment where two or all three types of energies are present. Understanding how energy distributes itself over a system and where points of high power density occur, something that is out of the scope of lumped parameter circuit analysis, will lead to better thermal-based design of a system from the very beginning of its design process. So with the ability to map 3-D energy flux in a system, proper partitions can be realized leading to modularization that may maximize such parameters as efficiency and reliability. The Poynting analysis as a basis for physical modeling will be the main focus of this Chapter [2].

II. Lumped Parameter Circuit Criteria

Different lumped parameter circuit criteria are studied in order to understand the partition that is made in order to facilitate the understanding of how similar partitions can be made using the standard-cell hierarchy. The whole concept of lumped parameter circuit relies on the fact that the entire circuit exists at one point in space so dimensions of the components are not important. Thus the voltages and current change instantaneously at all points in the circuit as there is no concept of travel time from one point of the circuit to another [3]. Applicability of lumped circuit formulations are heuristically based on three different but related views. The three views are 'rise time v. travel time', 'period v. travel time', and 'component size v. wavelength' [3].

II.1. Rise Time v. Travel Time

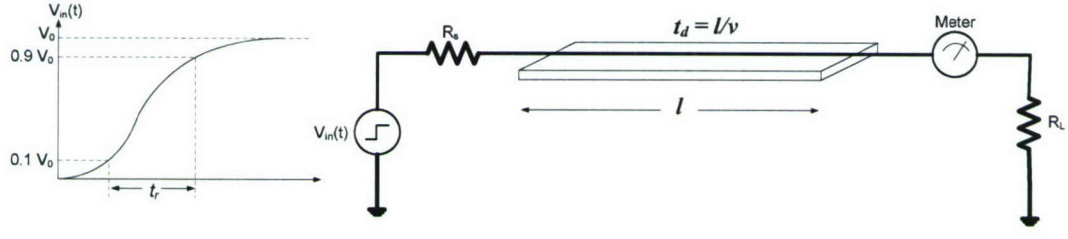


Fig. 4-2 Signal propagating through a medium.

Fig. 4-2 demonstrates the source signal (on the left) and the path through which the signal propagates (on the right). The time it takes the signal to go from 10% of its full voltage to 90% of its full voltage is defined as the rise time, t_r. The signal propagates through a medium of finite length, l, with a velocity, v. So the signal is delayed by the time $t_d = l/v$ before it reaches the load. So in order for the medium, through which the signal propagates, to be considered a lumped element, it must satisfy (1).

$$\left(\frac{t_r}{t_d}\right) > 6 \tag{1}$$

Lumped element would not be appropriate for,

$$\left(\frac{t_r}{t_d}\right) < 2.5 \tag{2}$$

and the appropriateness of lumped analysis would depend on the application in hand and the required accuracy for the range specified by (3).

$$2.5 < \left(\frac{t_r}{t_d}\right) < 6 \tag{3}$$

For example, the rise time of a GaAs technologies is $t_r = 0.1$ns. The speed of propagation of a signal through the material of SiO_2 is $v = 0.51c$, where c is the speed of light. The typical length of on-chip interconnections are $l = 1cm$. These values results in a delay time of $t_d = 65.36ps$. The ratio of rise time over delay time is given in (4) and it can be observed that lumped circuit is not appropriate for this case [3].

$$\left(\frac{t_r}{t_d}\right) = 1.53 \tag{4}$$

II.2. Period v. Travel Time

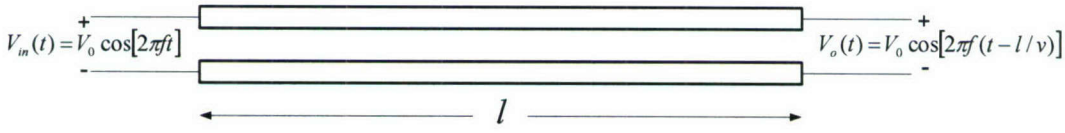


Fig. 4-3. Phase delay of a signal through a medium.

The input and corresponding output voltage through a medium is shown in Fig. 4-3. The output voltage is rewritten in another form in (5).

$$V_o(t) = V_0 \cos[2\pi f(t - l/v)] = V_0 \cos\left[2\pi ft - 2\pi \frac{t_d}{T}\right] \tag{5}$$

It can be observed from (5) that if $t_d << T$, then output voltage equals the input voltage. So a rule of thumb to consider the medium as a lumped element is given by (6).

$$t_d < 0.01T \tag{6}$$

For example, transmission line operating at a frequency of 60Hz has a period of 16.7ms. Dividing that number by 100, $t_d = 0.167$ms is obtained. So for a signal propagating at the speed of light, the length has to be $l = 50km$. Thus a lumped analysis is only valid for a transmission line less than 50km at 60Hz frequency [3].

II.3. Component Size v. Wavelength

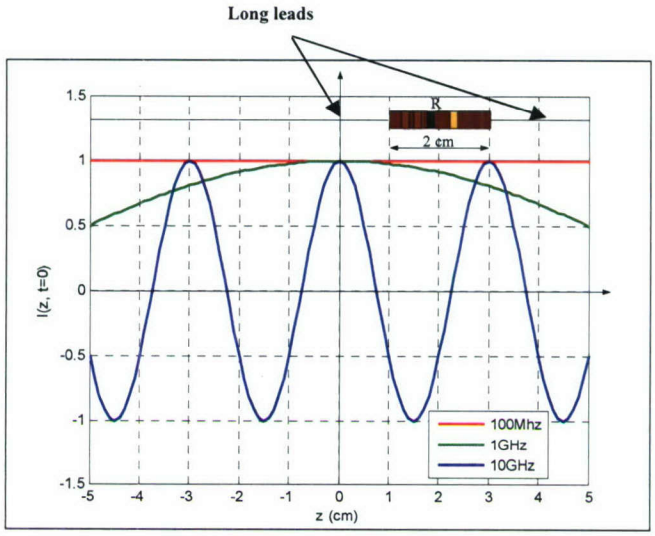


Fig. 4-4. Comparison of signal wavelength to component size.

Electromagnetic quantities are assumed to vary as given by (7).

$$I(z,t) = A\cos\left[(2\pi f)t - \left(\frac{2\pi}{\lambda}\right)z\right]$$

where

$A \equiv$ amplitude
$f \equiv$ frequency
$\lambda \equiv$ wavelength $= \dfrac{c}{f}$ } constants

(7)

At fixed point in time (i.e. t = 0), (7) is rewritten as (8).

$$I(z,t=0) = A\cos\left[-\left(\frac{2\pi}{\lambda}\right)z\right]$$

(8)

Observing (8), it can be seen that the polarity of the signal changes every $\dfrac{\lambda}{2}$ change in position. So in order for a component, such as the resistor with long leads shown in Fig. 4-4 to be considered as a lumped element, it must satisfy:

$l < 0.01\lambda$

$l \equiv$ length of propagation path

This requirement is quite clear by observing Fig. 4-4. The 1GHz and 10GHz signal undergo drastic changes in magnitude and/or polarity over the length of the resistor with its long leads [3].

III. The Poynting Vector

The Poynting Vector is defined as the cross product of the electric and magnetic field vectors, **E** and **H**. Thus,

$$\vec{S} = \vec{E} \times \vec{H} \ (\mathrm{W/m^2})(9)$$

where,

S = Poynting Vector = power density, $\mathrm{W/m^2}$

E = electric field vector, V/m

H = magnetic field vector, A/m

The Poynting Vector can be used to map 3-D flux. From the Ampere's Law and Faraday's Law, the point form of Poynting Theorem is derived as:

$$-\nabla \cdot \vec{S} = \vec{E} \cdot \vec{J} + \vec{E} \cdot \frac{\partial \vec{D}}{\partial t} + \vec{H} \cdot \frac{\partial \vec{B}}{\partial t} \ (\mathrm{W/m^3})(10)$$

The point form of Poynting Theorem states the net inward flux of the Poynting Vector per unit volume is the sum of the power dissipated and the rate change of energy stored per unit volume.

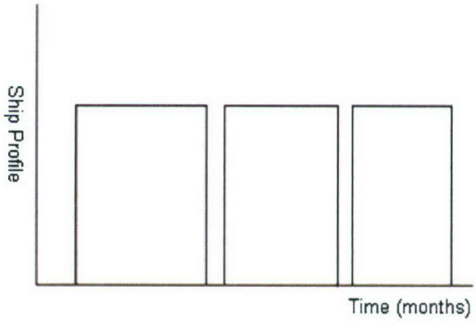
The integral form of Poynting Theorem is:

$$-\oint \vec{S} \cdot ds = \iiint \left(\vec{E} \cdot \vec{J} + \vec{E} \cdot \frac{\partial \vec{D}}{\partial t} + \vec{H} \cdot \frac{\partial \vec{B}}{\partial t} \right) dv$$

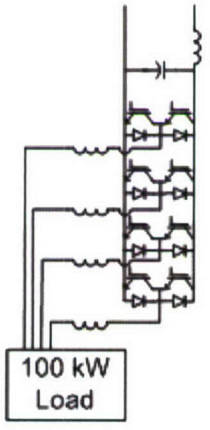
$$= \iiint \left(\vec{E} \cdot \vec{J} + \frac{\partial \left(\frac{\varepsilon \vec{E}^2}{2} + \frac{\mu \vec{H}^2}{2} \right)}{\partial t} \right) dv \quad (\mathrm{W})(11)$$

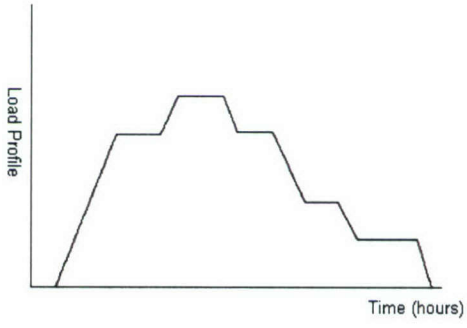
The integral form of Poynting Theorem states the net inward flux of the Poynting Vector through some closed surface is the sum of the power dissipated in the volume enclosed by the surface and the rate change of energy stored in the volume enclosed by the surface [2].

Unlike other energy analysis methods, the Poynting Vector relates to the components' physical structure, providing not only the electrical characteristics of the components, but also the thermal and mechanical characteristics at the same time. However, the Poynting vector itself provides information that may not be very different from one layer of the hierarchy to the next, but pointing vector coupled with energy time constants associated with the system under study provides a strong distinguishing partition. For example, Fig. 4-5(a) shows an aircraft carrier with its associated mission profile whose units are in months. Fig. 4-5(b) shows a 4-Leg 3-Phase VSI with its associated load profile with units in hours. While Fig. 4-5(c) depicts an IGBT switch with its associated switching profile with units in milliseconds. So mapping out the Poynting vector and its other forms such as the one given by (10) and (11) coupled with the associated time constant of the system under study provides a valuable tool towards realizing the final partition.

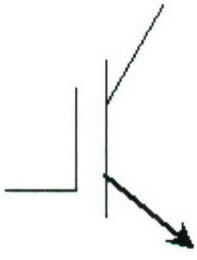


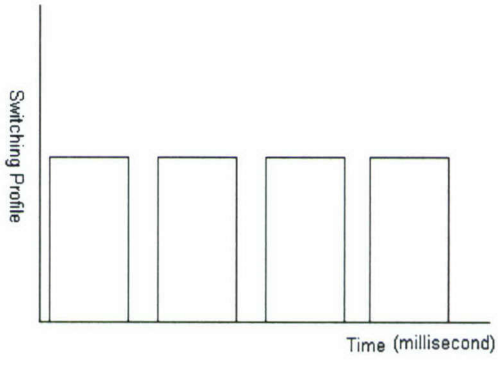
(a) Aircraft Carrier





(b) 4-Leg 3-Phase VSI





(c) IGBT

Fig. 4-5. Systems with their associated time profiles.

The next section will show the results of Poynting analysis on various electrical components.

IV. Poynting Analysis of Components

IV.1. Poynting Vector for a Resistor

The Poynting Vector for a cylindrical conductor is studied. The dimension of the conductor is shown in Fig. 4-6(a), with conductivity σ, and current density **J**.

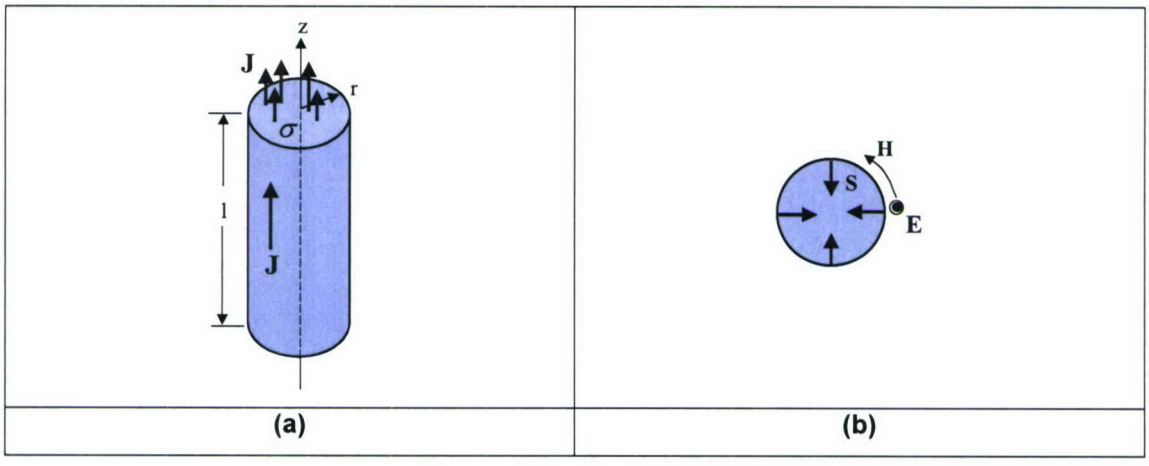


Fig. 4-6. Poynting vector for a conductor:(a) dimensions of the conductor, (b) Poynting vector of the conductor.

From the Ampere's Law and Ohm's Law, the induced magnetic field vector and the electric field vector are shown in Fig. 4-6(b) with their amplitude calculated in (12) and (13). The corresponding Poynting vector is shown in Fig. 4-6(b) perpendicular to the surface area of the side of the conductor. The direction of the Poynting vector indicates that the conductor absorbs the energy. Equation (14) is the spatial integration of the derived Poynting vector on the cylindrical conductor. The equation shows that the integration of the Poynting vector is the total power dissipated on the conductor through heat.

$$|H| = \frac{I}{2\pi r} \tag{12}$$

$$|E| = \frac{I}{\sigma A_{Cu}} \tag{13}$$

$$\oint_s \vec{S} \cdot d\vec{s} = \oint \frac{I^2}{\sigma A_{Cu} 2\pi r} \cdot d\vec{s} = \frac{I^2}{\sigma A_{Cu} 2\pi r} 2\pi r l = \frac{I^2 l}{\sigma A_{Cu}} \tag{14}$$

In this case, the Poynting vector gives the energy dissipated on the conductor. It provides the link between the electrical characteristics and the thermal characteristics [4].

IV.2. Poynting Vector for an Inductor

The structure of the inductor is shown in Fig. 4-7. The energy is mostly stored in the air gap, so only the energy variation in the air gap is considered. If a current flows in the winding as Fig. 4-7 shows, there will be a magnetic field inside the core. From the Faraday's Law, when this applied current changes, there will be an induced electric field, as expressed in (15). There are two possible conditions, one is the current

increase, the other is the current decrease, and the induced electric filed has different direction in these two cases, as shown in Fig. 4-8.

Applying the definition of the Poynting vector, the Poynting vector of these cases is shown in Fig. 4-9. When the current decreases, the inductor releases the energy. When the current increases, the inductor stores the energy.

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \tag{15}$$

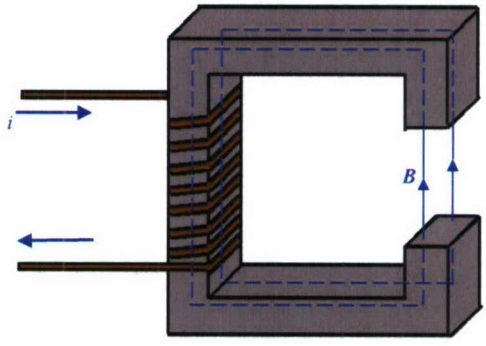
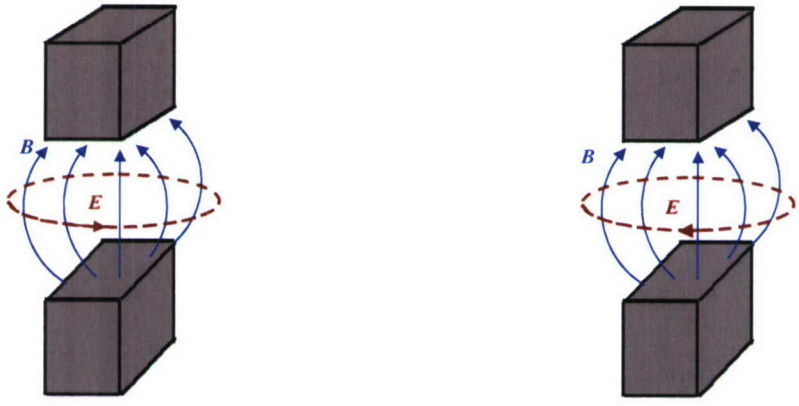


Fig. 4-7. Structure of the inductor.



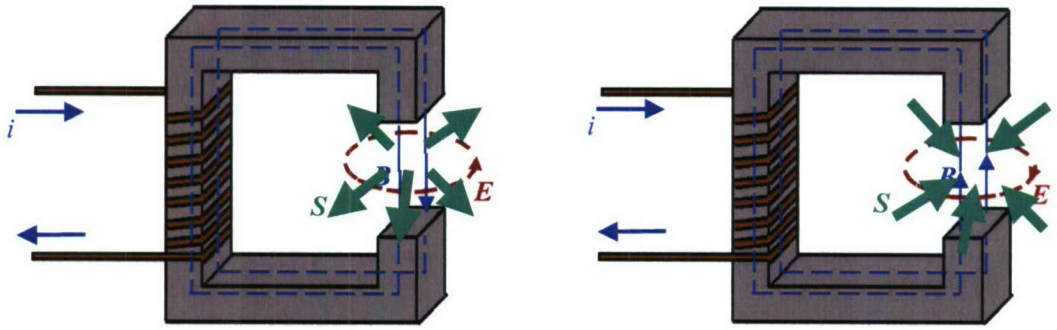
(a) **(b)**

Fig. 4-8. Magnetic field vector and electric field vector: (a) i decreases, (b) i increases.

The energy per volume stored in the induction is given as:

$$w_m = \frac{1}{2}\mu H^2 \tag{16}$$

The Poynting vector here provides a link between magnetic field energy and electric energy [4].



(a) (b)

Fig. 4-9. Poynting Vector for a inductor: (a) i decreases, (b) i increases.

IV.3. Poynting Vector for a Capacitor

The structure of a capacitor is shown in Fig. 4-10. There is an accumulation of positive and negative charges on the two plates and the associated electric field is shown. Similar to the inductor case, there are two possible scenarios: capacitor is storing energy, or the capacitor is releasing energy. From the Ampere's Law, there is an induced magnetic field with the change in the electric field, as expressed by (17). Applying the definition, the Poynting vector for a capacitor is obtained, as shown in Fig. 4-11.

$$\nabla \times \vec{H} = \frac{\partial \vec{D}}{\partial t} \tag{17}$$

The energy per volume stored in the capacitor is

$$w_e = \frac{1}{2}\varepsilon E^2 \tag{18}$$

Here, the Poynting vector provides a link between electric field energy and electrical energy. The thickness of the dielectric material between two plates can be calculated by the applied voltage and the material characteristics. Thus, the Poynting Vector also evinces the relationship between the electromagnetic configuration and the spatial configuration [4].

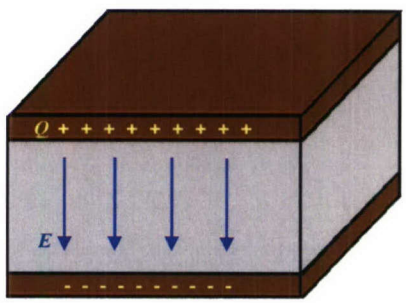
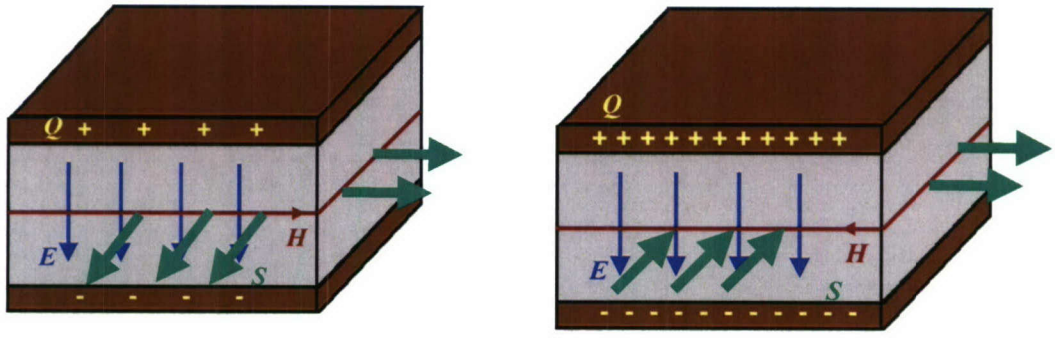


Fig. 4-10. Structure of the capacitor.

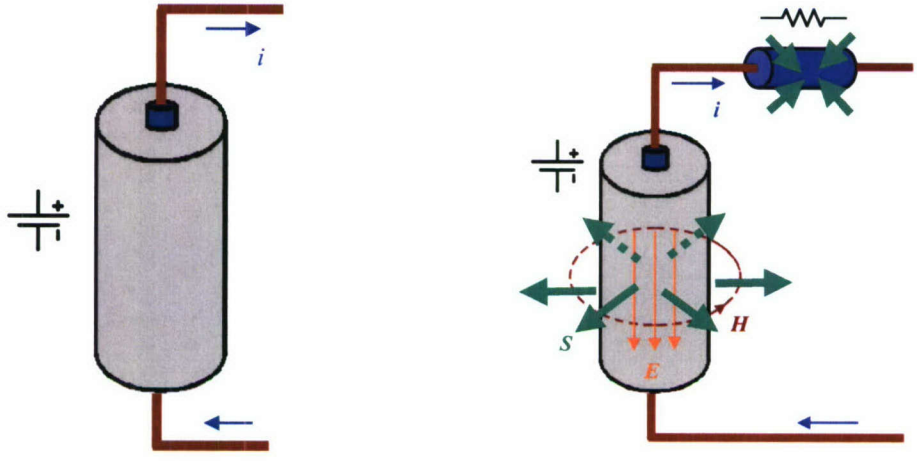


(a) (b)

Fig. 4-11. Poynting Vector for a capacitor: (a) Discharging, (b) Charging.

IV.4. Poynting Vector for a DC Voltage Source

Fig. 4-12(a) is the structure of the DC voltage source supplying energy to a circuit. The Poynting Vector of a DC voltage source with an intrinsic resistance can be obtained as shown in Fig. 4-12(b). The Poynting Vector depicts the energy flowing out of the voltage source [4].



(a) (b)

Fig. 4-12. Poynting Vector for a DC voltage source: (a) Structure, (b) Poynting Vector.

IV.5. Poynting Vector for the PEBB Phase Leg

Before Poynting analysis can be undertaken for the PEBB Phase Leg, the non-linear switching voltage and current signals of a IGBT are studied and simplified to a linear switching signal, and an electrical simplified model of the IGBT is attained. Fig. 4-13 shows both the simplified electrical IGBT model used in the Poynting analysis and the associated linear switching signal.

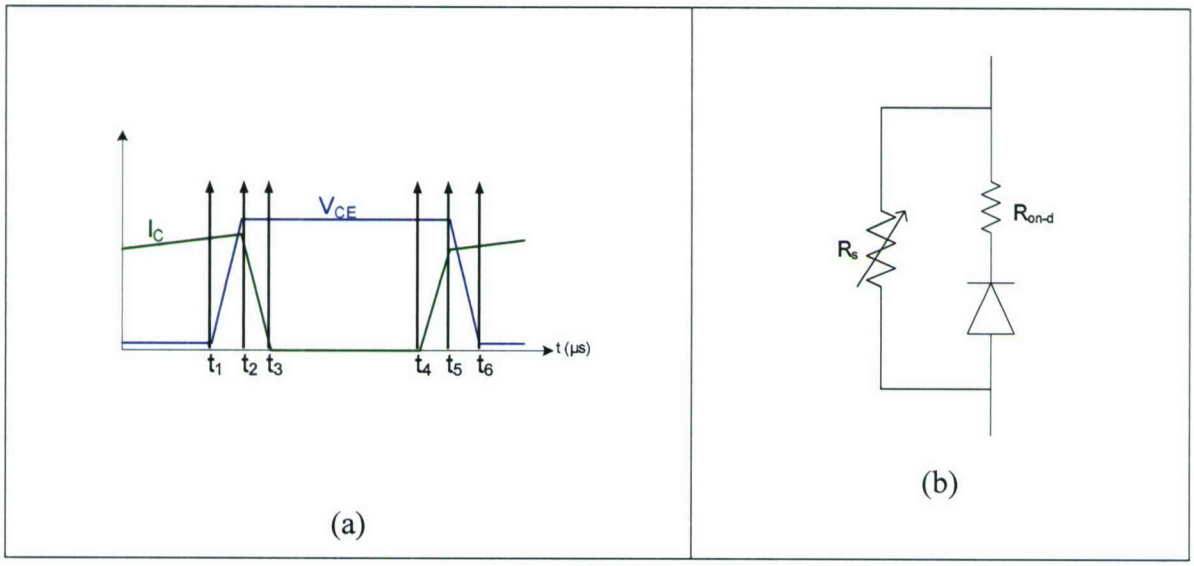


Fig. 4-13. IGBT a) simplified voltage and current signals, b) simplified model.

The voltage and the current of the switch do not change simultaneously. The turn off and turn on procedure each consists of two time intervals. Time t_1 to t_3 is the turn off procedure. In the time interval t_1 to t_2, the current stays relatively constant and the voltage increases linearly similar to the charging of a capacitor. In the time interval t_2 to t_3, the voltage stays constant and the current decreases linearly similar to the discharging of an inductor. At turn off, the induced voltage is added to the externally applied voltage and the chip voltage becomes larger; the displacement current adds to the externally applied current. From t_4 to t_6 is the turn on procedure. In the time interval t_4 to t_5, the voltage stays constant and the current increases linearly similar to the charging of an inductor. In the time interval t_5 to t_6, the voltage decreases linearly and the current stays relatively constant similar to the discharging of a capacitor. At turn on, the induced voltage is subtracted from the externally applied voltage and the chip voltage becomes smaller; the displacement current subtracts from the externally applied current. In order to undertake more complicated analysis of a module, a Poynting vector legend is created to represent various characteristic behavior of the energy. Fig. 4-14 depicts the legend used to perform the Poynting analysis.

The PEBB phase leg is studied in a Buck converter topology in the PEBB cabinet as roughly shown in Fig. 4-15(a). The corresponding geometric PEBB model that will be analyzed is shown in Fig. Fig. 4-15(b) [5]. For each of the six switching phase of the waveform shown in Fig. 4-13(a), the PEBB is analyzed in a Buck converter topology. Fig. 4-16 through Fig. 4-21 show the Poynting vector analysis on the PEBB phase leg. The right portion of each of the figure show pertinent information such as the point in time of the switching waveform of the top switch, associated time constants, and flow of the current in the buck converter at that point in time. The buck converter is operated at 15kHz switching frequency with the component values listed in the circuit depicted in (b) of each figure.

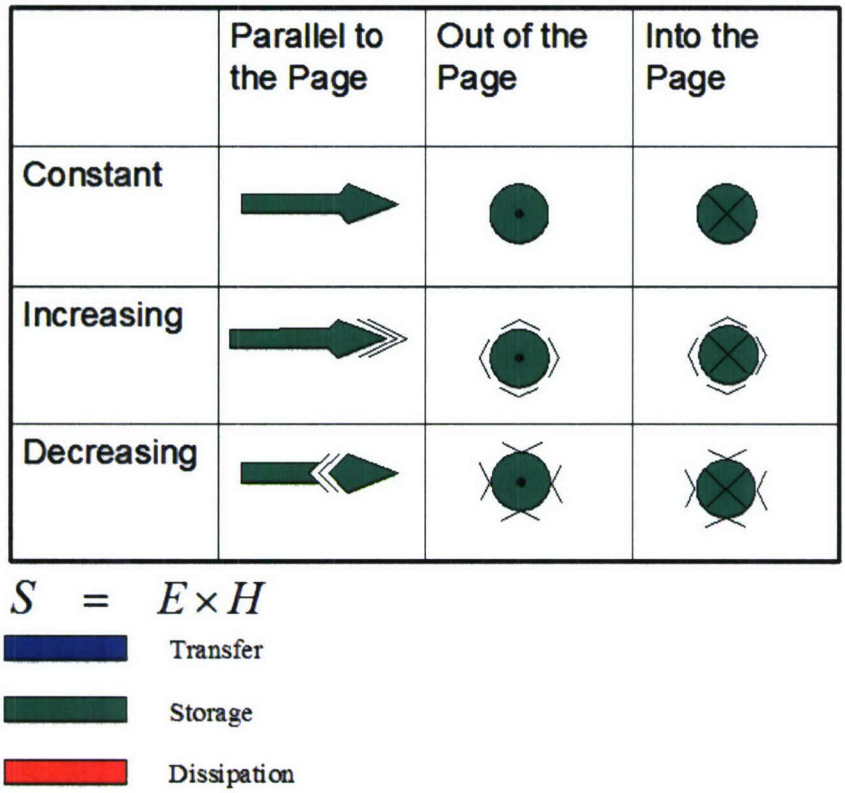


Fig. 4-14. Two-Dimensional Poynting Vector Legend.

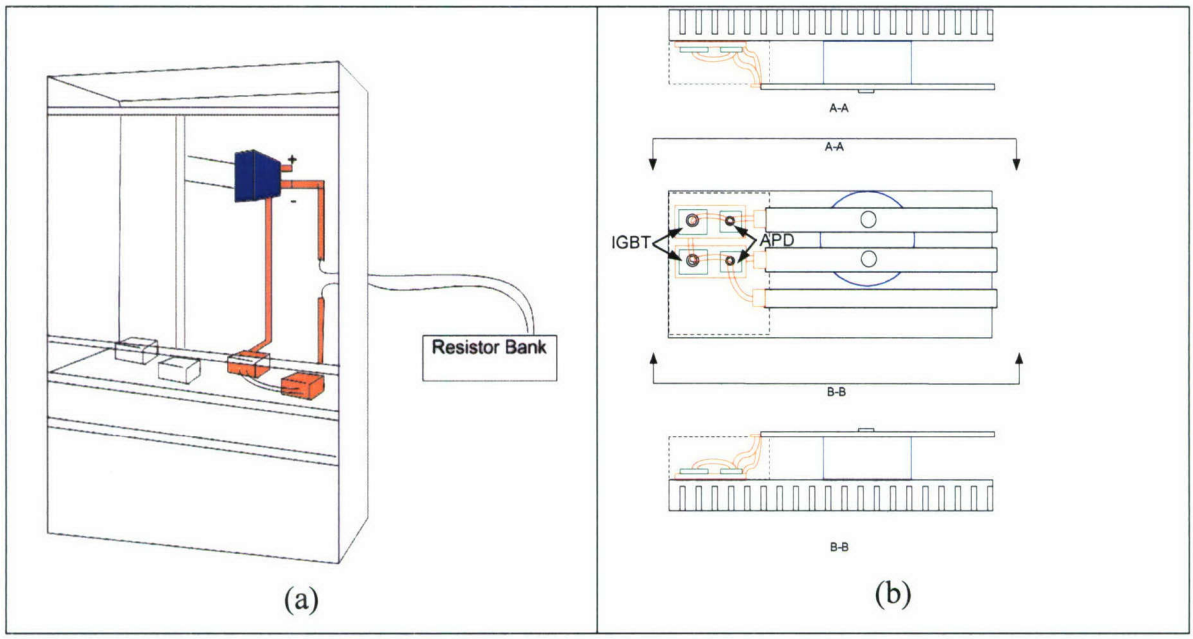


Fig. 4-15. a) Rough sketch of PEBB Cabinet, and b) simplified PEBB Phase Leg.

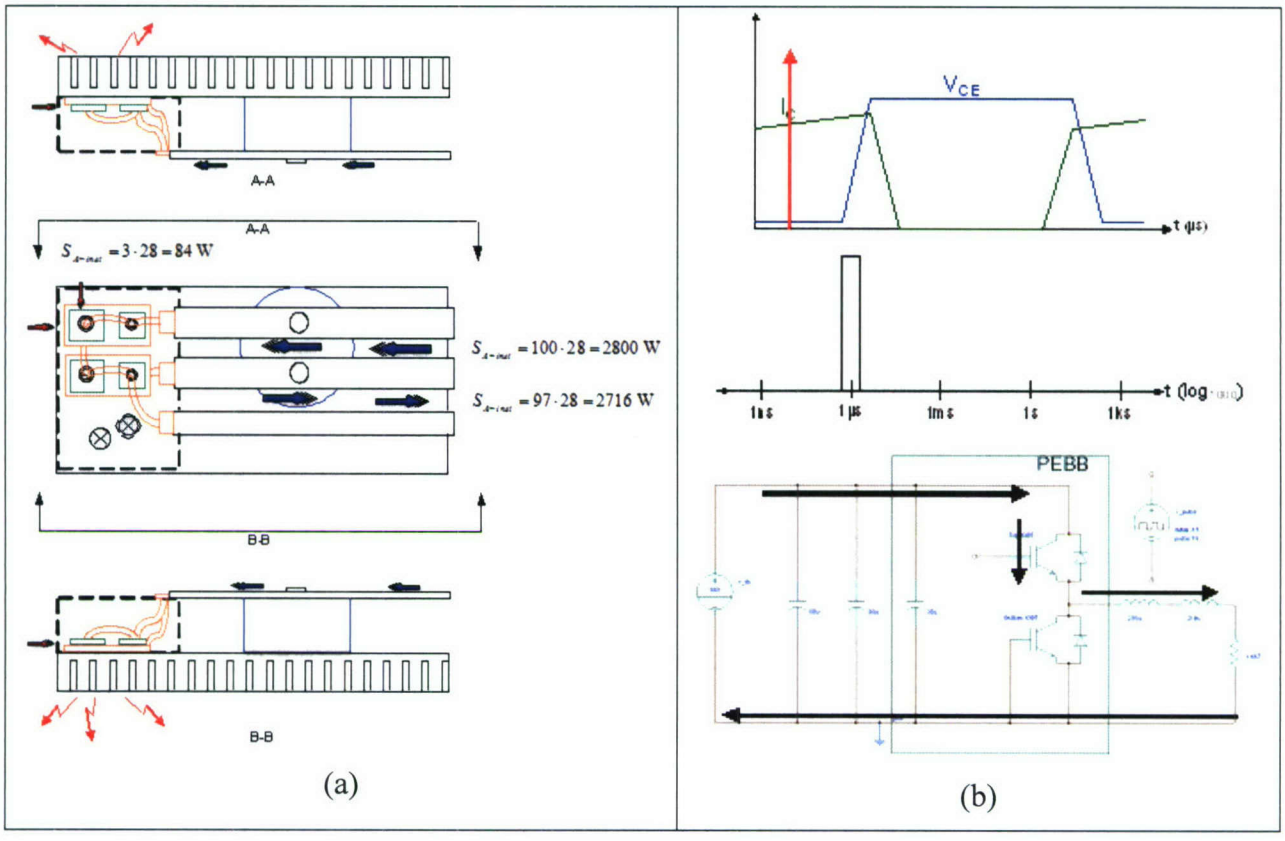


Fig. 4-16. The Poynting analysis on the a) PEBB Phase Leg, with b) Time and Flow.

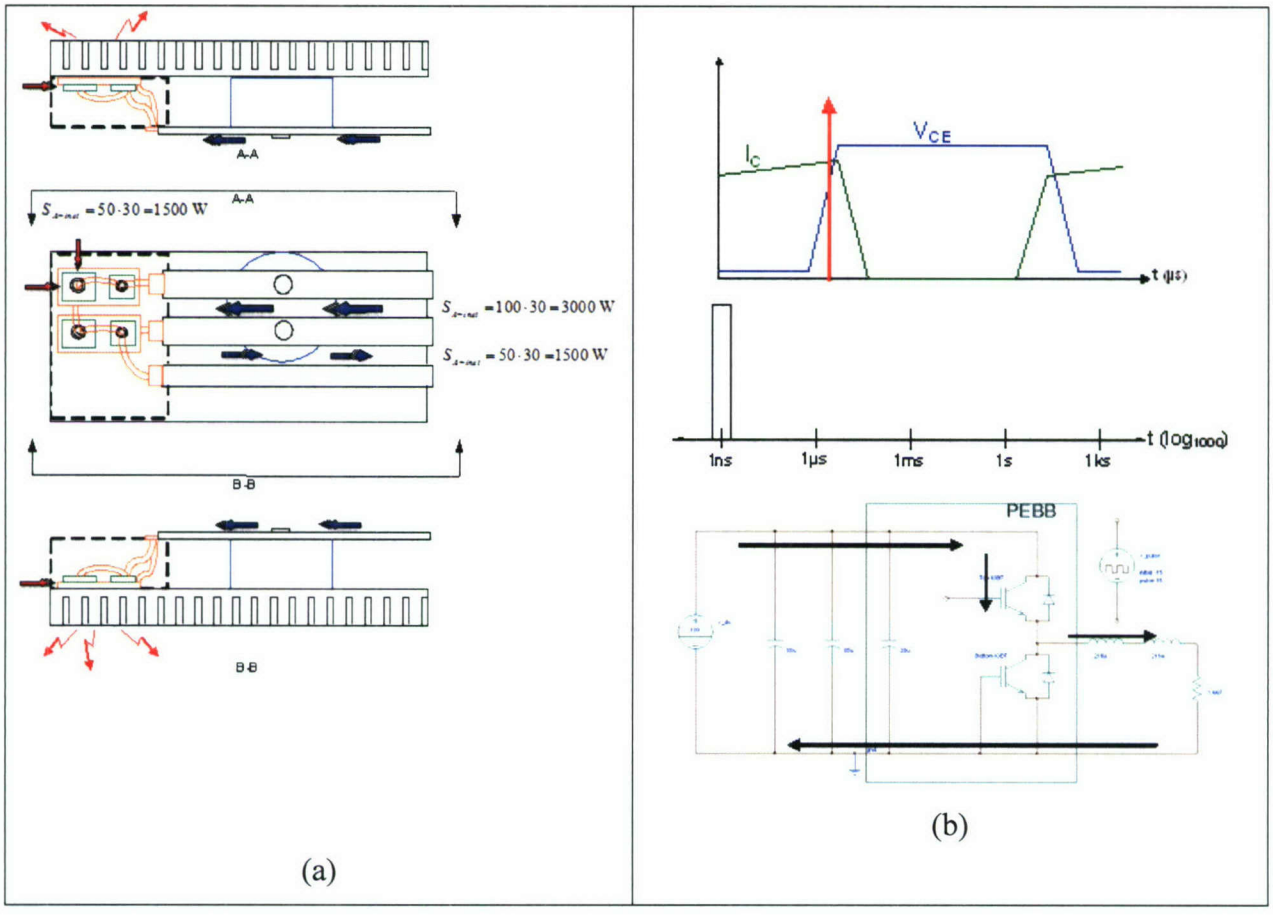


Fig. 4-17. The Poynting analysis on the a) PEBB Phase Leg, with b) Time and Flow.

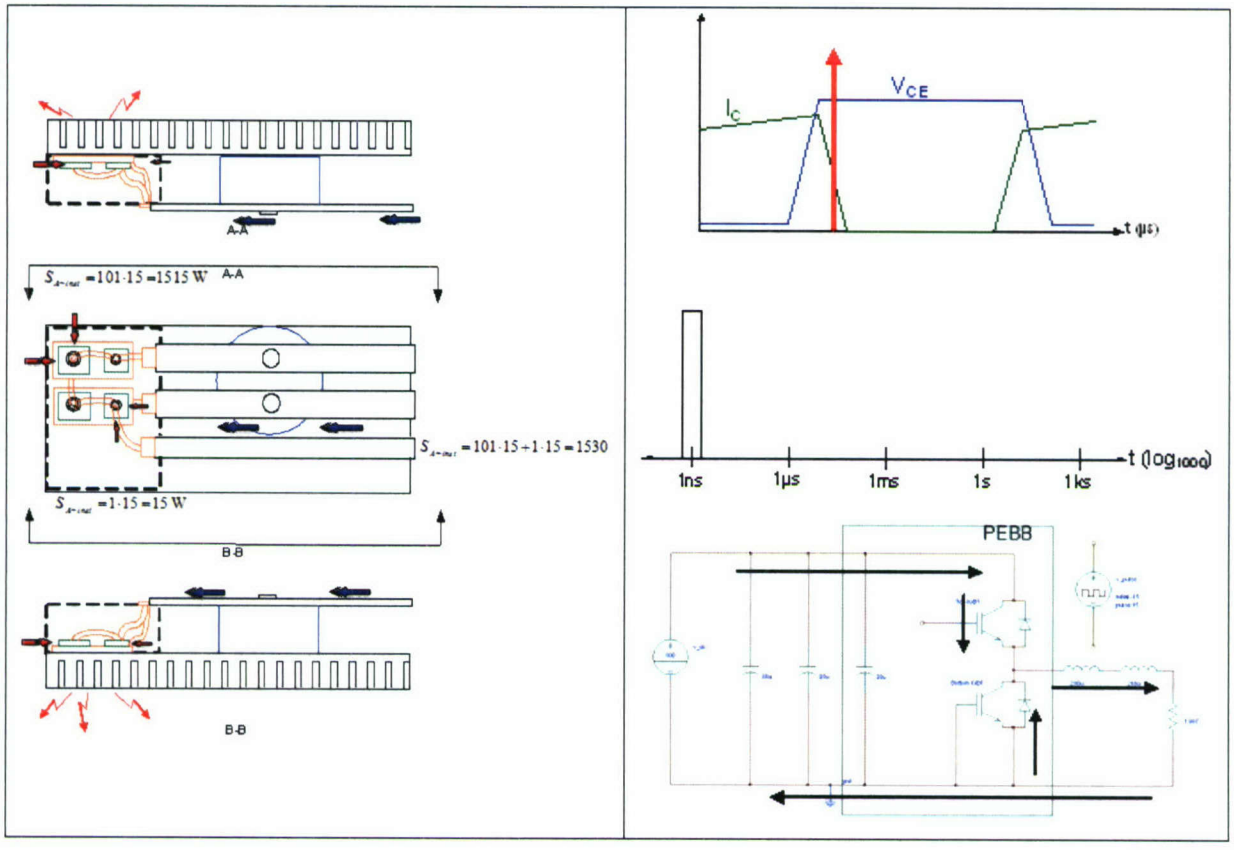
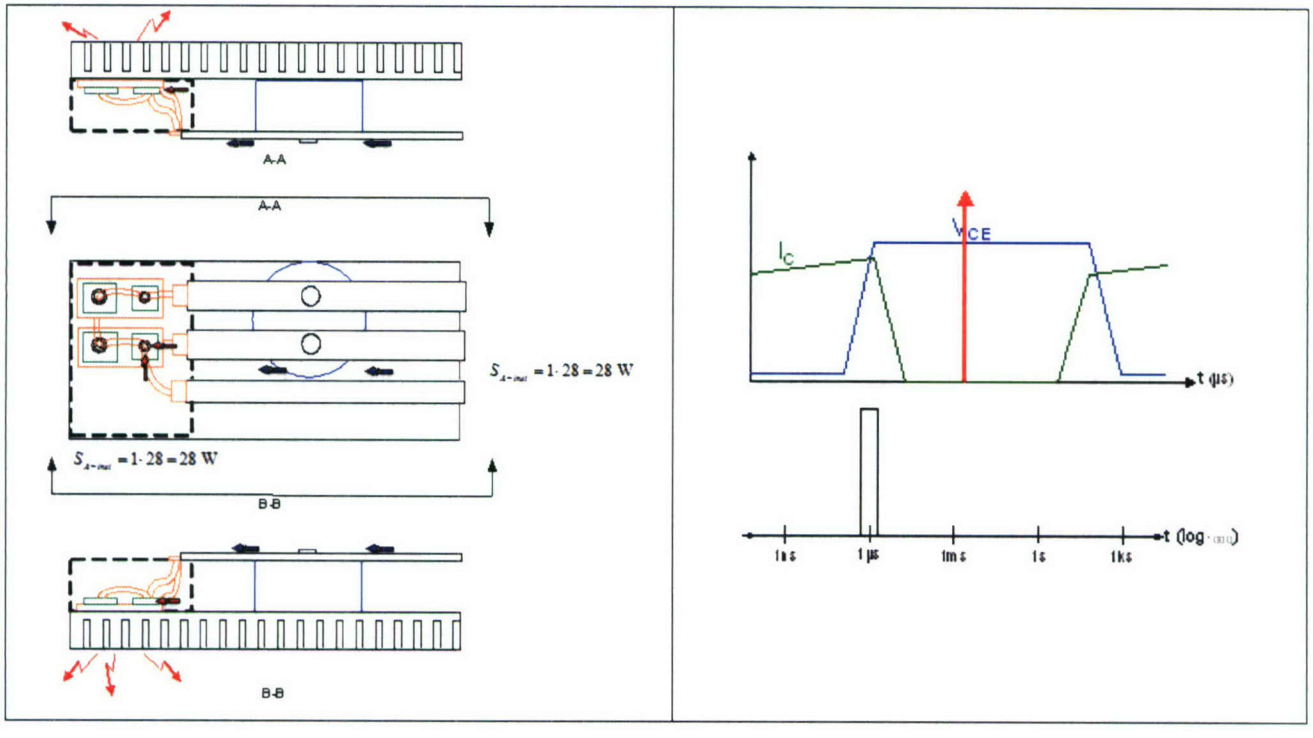


Fig. 4-18. The Poynting analysis on the a) PEBB Phase Leg, with b) Time and Flow.



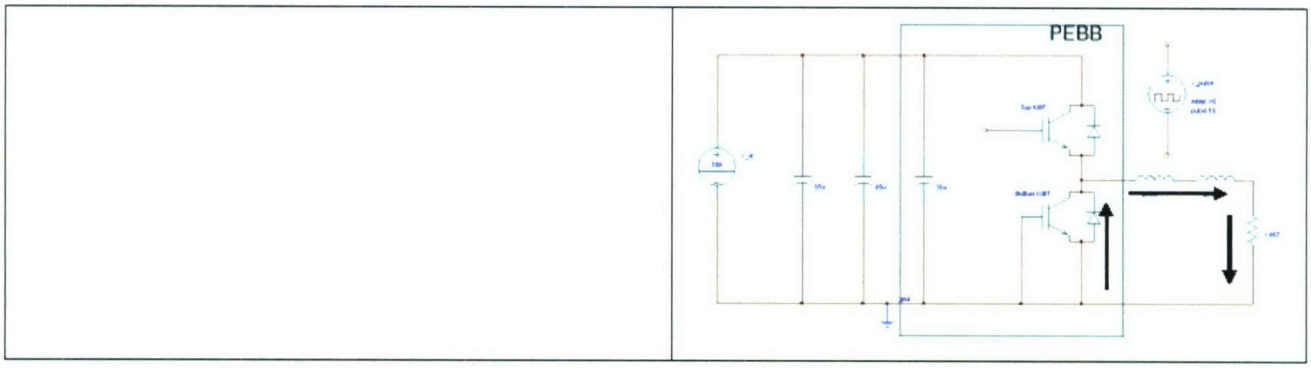


Fig. 4-19. The Poynting analysis on the a) PEBB Phase Leg, with b) Time and Flow.

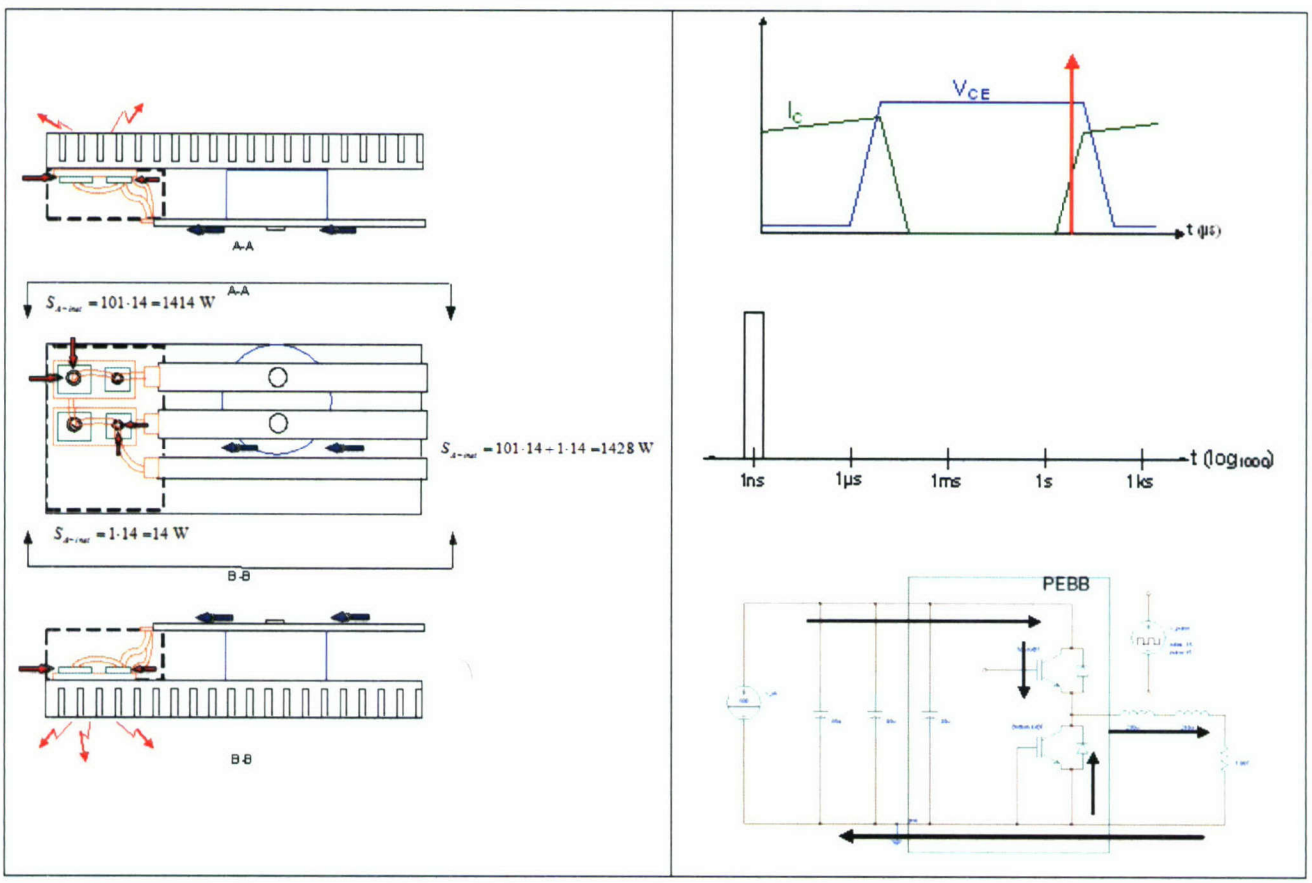


Fig. 4-20. The Poynting analysis on the a) PEBB Phase Leg, with b) Time and Flow.

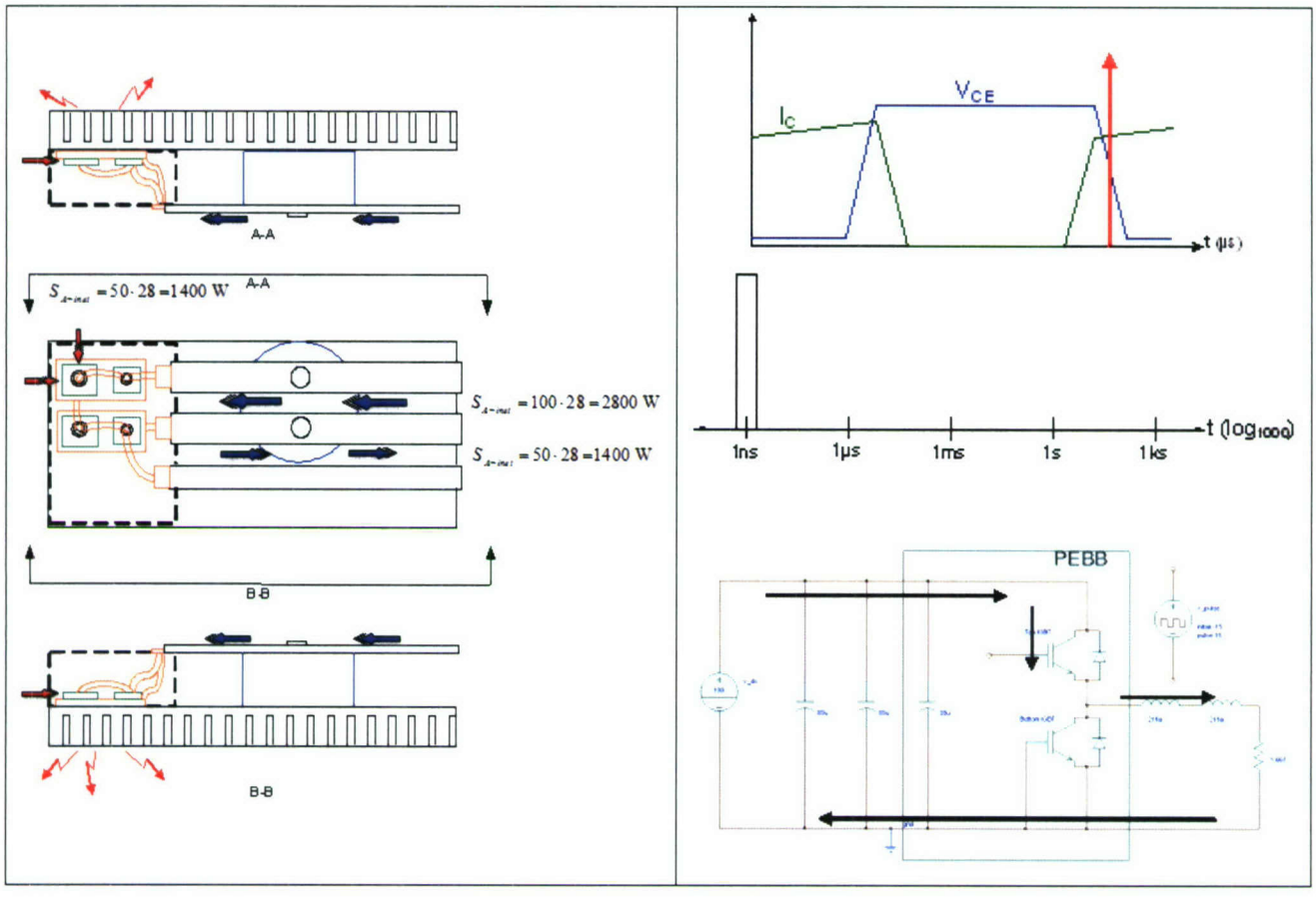


Fig. 4-21. The Poynting analysis on the a) PEBB Phase Leg, with b) Time and Flow.

IV.6. Poynting Vector for the 3-Phase VSI of the PEBB Cabinet

Before Poynting analysis can be performed on the 3-Phase VSI topology in the PEBB Cabinet, the actual physical structure of the inductors used in the cabinet are analyzed using Poynting vectors. The inductor's structure is analyzed using Poynting vectors in Fig. 4-22 and Fig. 4-23. The associated current and voltage curves across the inductor are also shown for each point in time under analysis. The 3-Phase VSI topology is depicted in Fig. 4-24 with the switching frequency of 10kHz and output inductor of 216µH and load of 1Ω. The output waveform is modulated using space-vector modulation to 60Hz. Due to the fact that there is such a big difference in switching and output frequency, it is not sensible to analyze the circuit at the same resolution of time. So, one PEBB Phase Leg is analyzed at the switching frequency resolution under the assumption that the output waveforms are basically DC. Due to the fact that all PEBB's undergo the same set of transitions with 120 degrees offset, only one phase leg is analyzed. The waveform under analysis is depicted in Fig. 4-25 with the points in time to be analyzed marked with vertical arrowheads. The corresponding Poynting vector analysis that one PEBB phase leg undergoes is shown in Fig. 4-26 for the four points in time. On the output side of the 3-Phase VSI where the waveforms are sinusoidal at a frequency of 60Hz, Fig. 4-27 depict the inductor current and output voltage waveforms and the points in time that the PEBB cabinet will be analyzed. For each of the four time markers, Fig. 4-28 through Fig. 4-31 show the Poynting vector analysis for the 3-Phase VSI in the PEBB Cabinet.

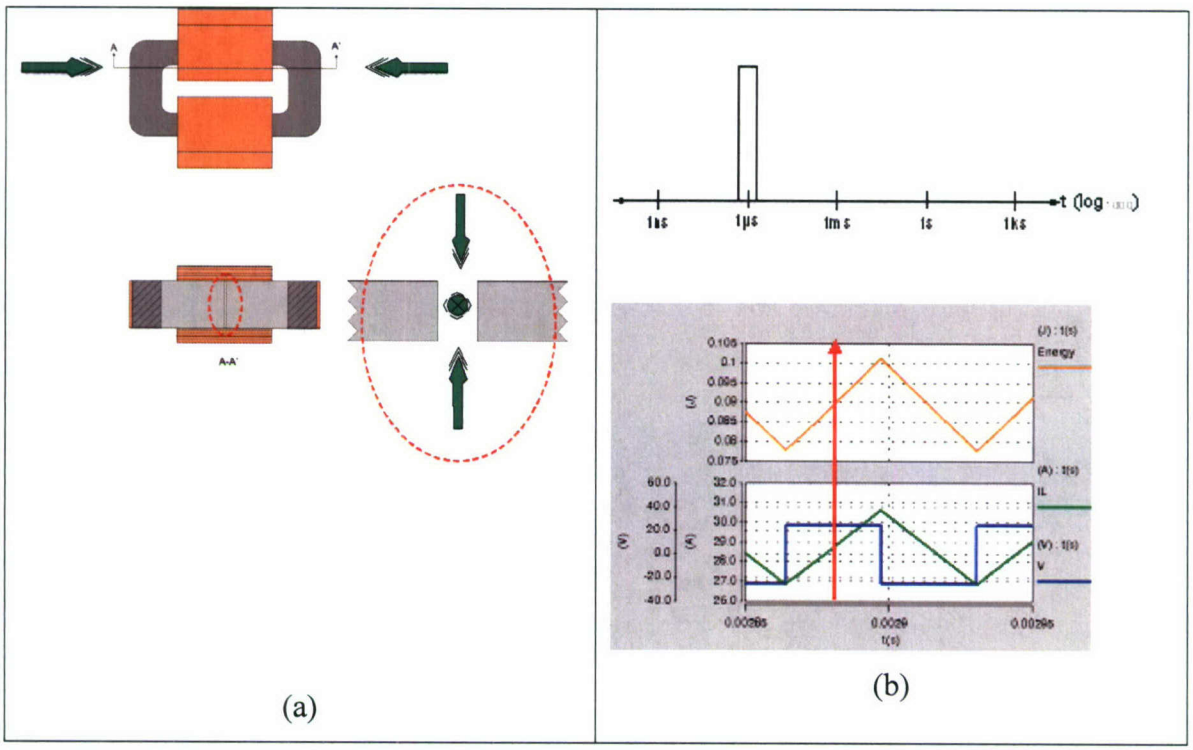


Fig. 4-22. Poynting Vector Analysis for a Charging Inductor.

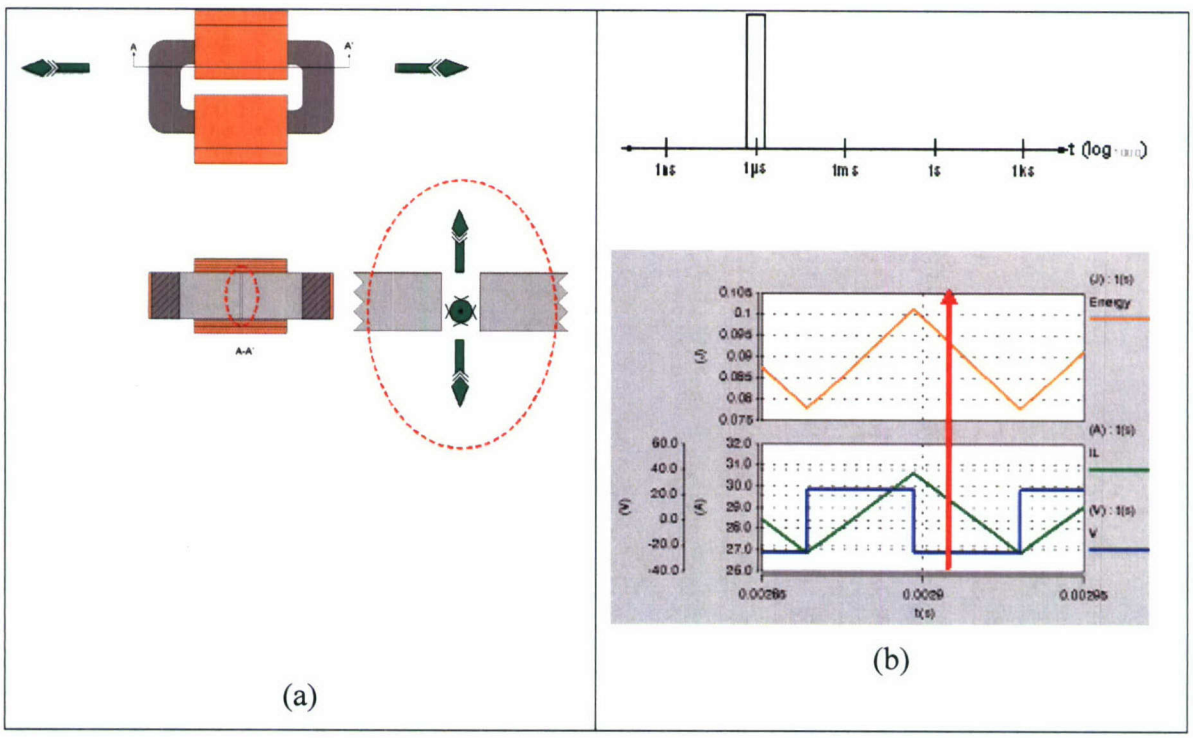


Fig. 4-23. Poynting Vector Analysis for a Discharging Inductor.

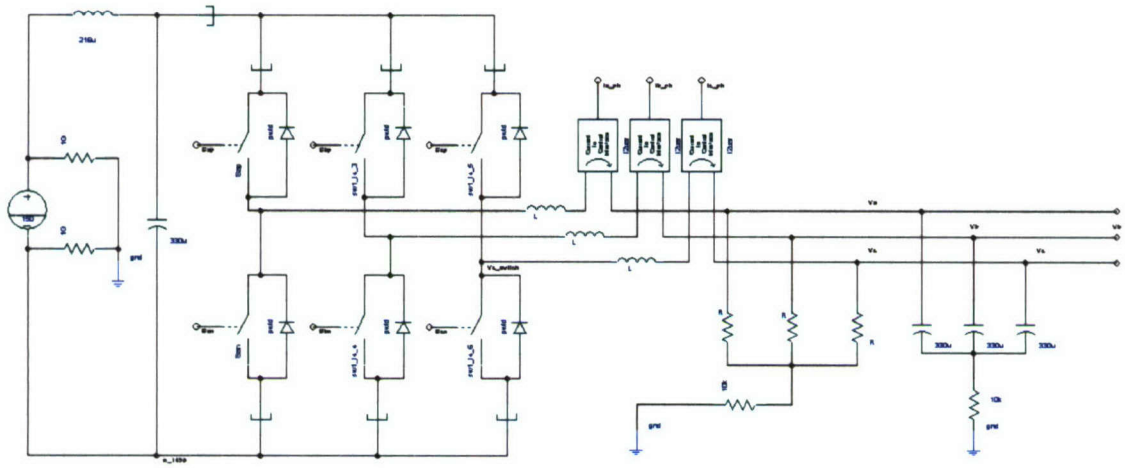


Fig. 4-24. Three phase VSI circuit under analysis.

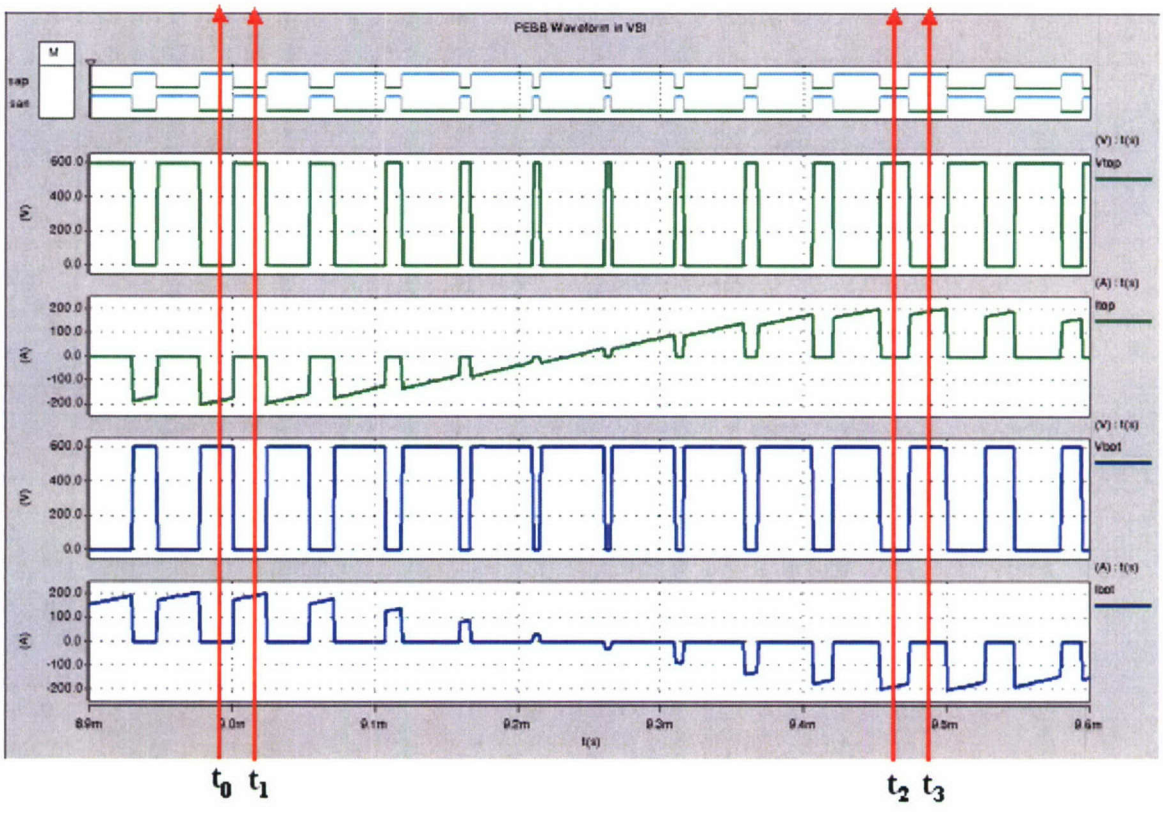


Fig. 4-25. The voltage and current waveforms of the top switch (green) and bottom switch (blue) in the phase leg.

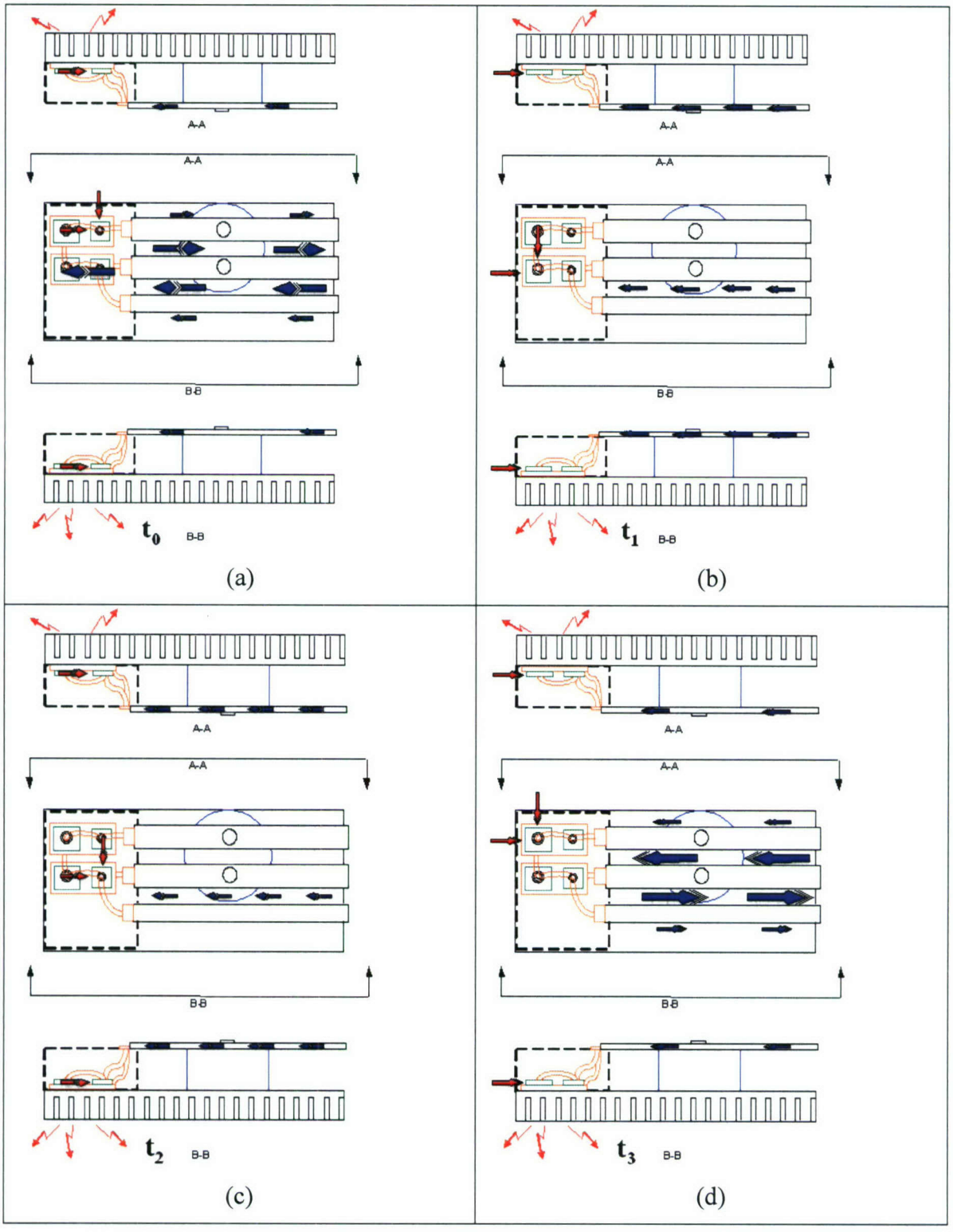


Fig. 4-26. The Poynting Vector analysis for the PEBB Phase Leg under 3-Phase VSI Topology for a) t0, b) t1, c) t2, and d) t3 time markers.

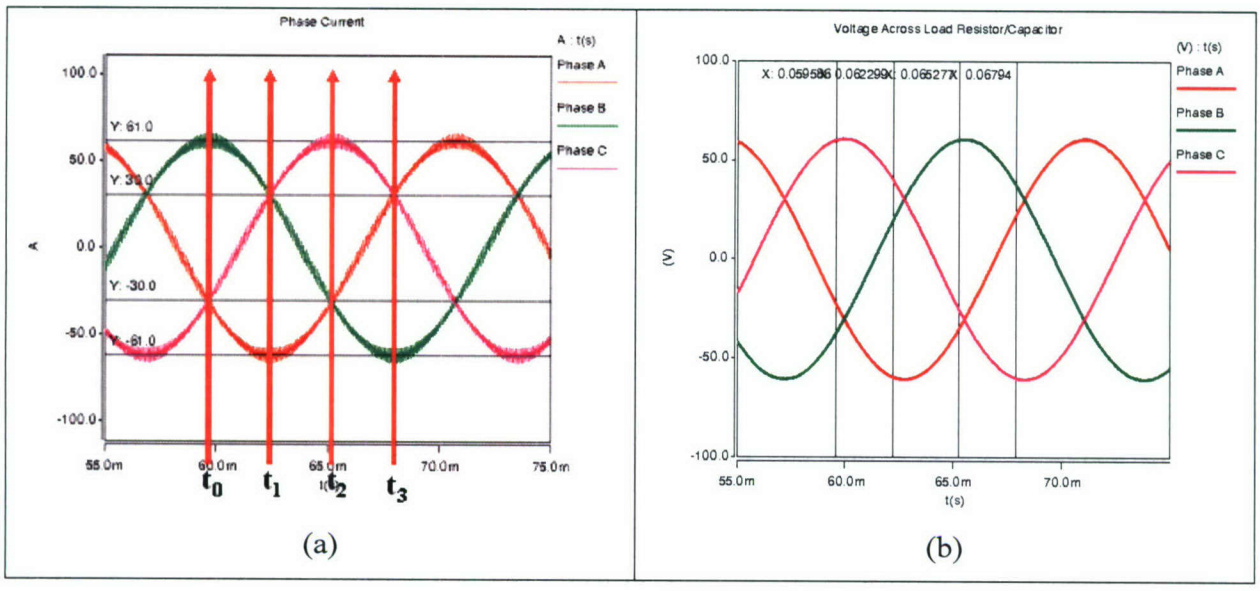


Fig. 4-27. Output waveforms of the 3-Phase VSI circuit with a) Inductor currents, and b) Output Voltage.

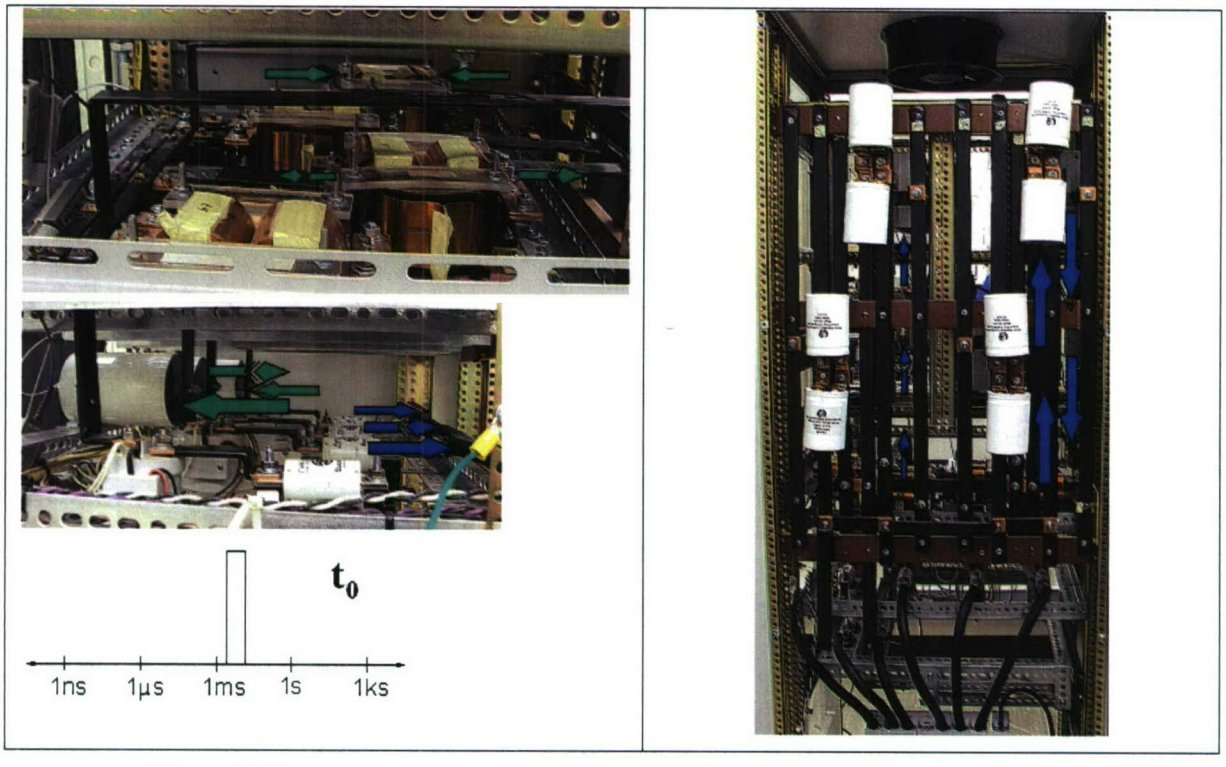


Fig. 4-28. Poynting Vector Analysis of the 3-Phase VSI PEBB Cabinet at time t0.

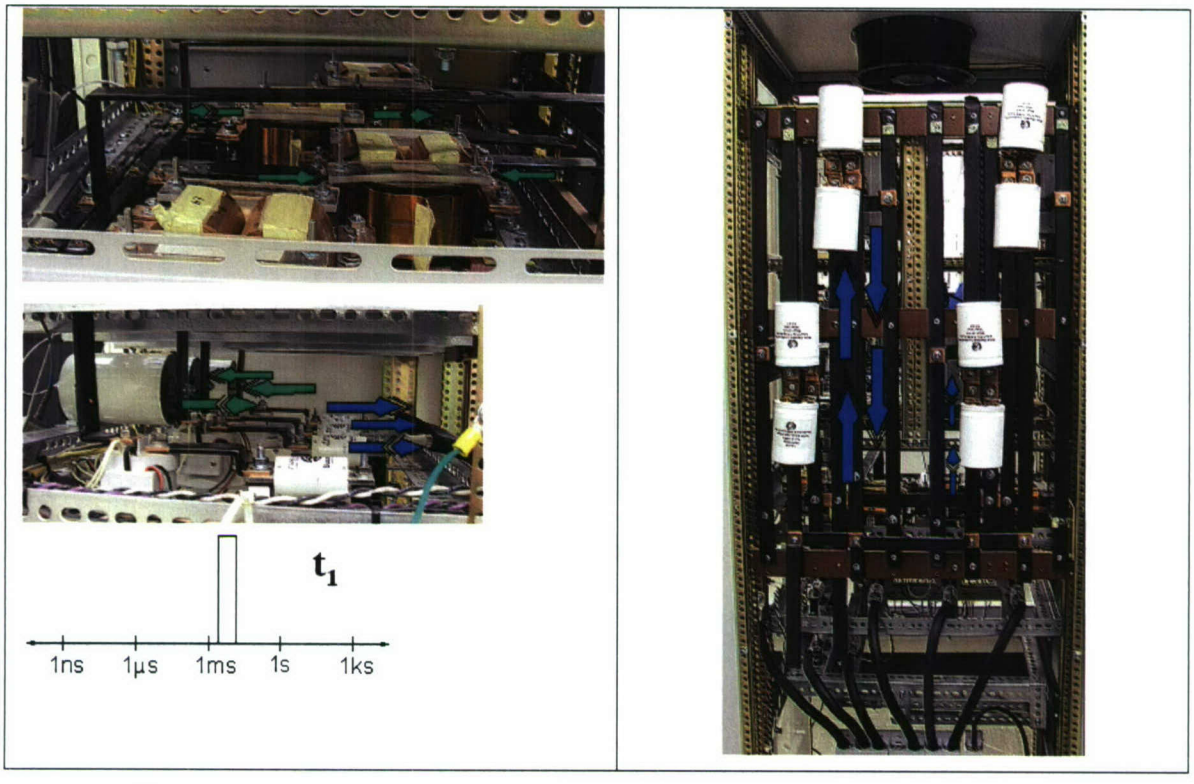


Fig. 4-29. Poynting Vector Analysis of the 3-Phase VSI PEBB Cabinet at time t1.

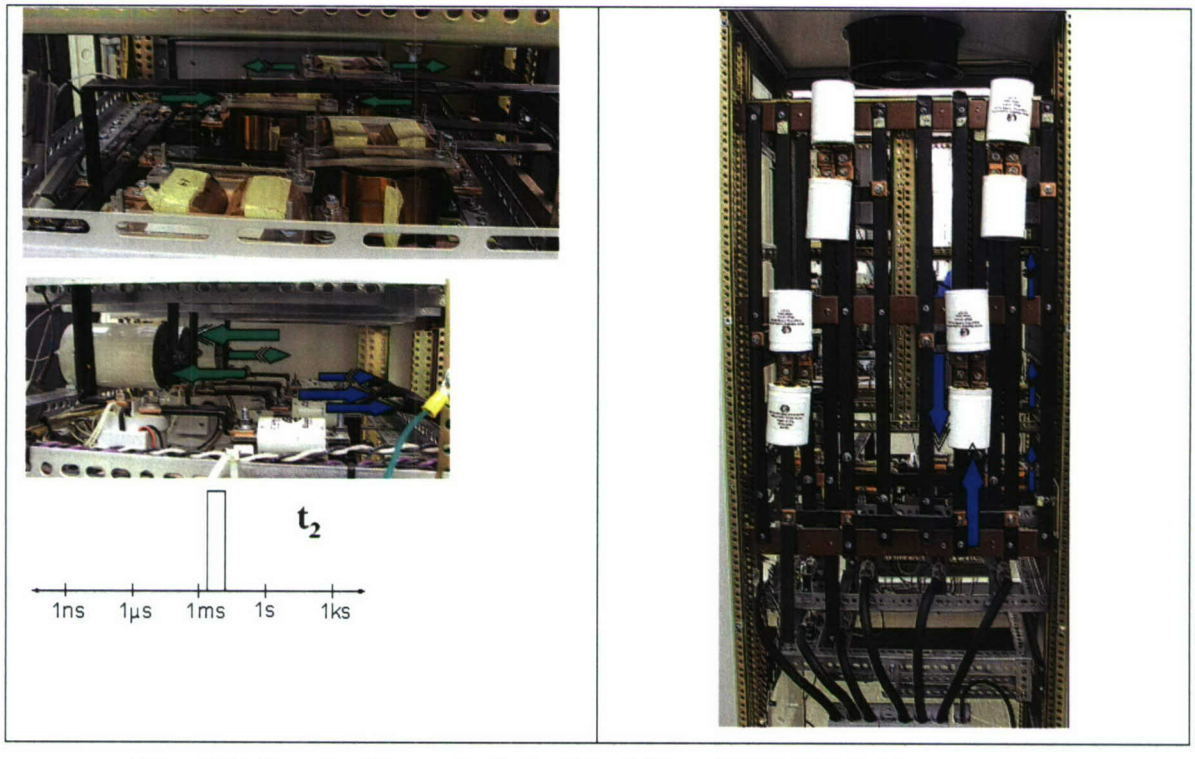


Fig. 4-30. Poynting Vector Analysis of the 3-Phase VSI PEBB Cabinet at time t2.

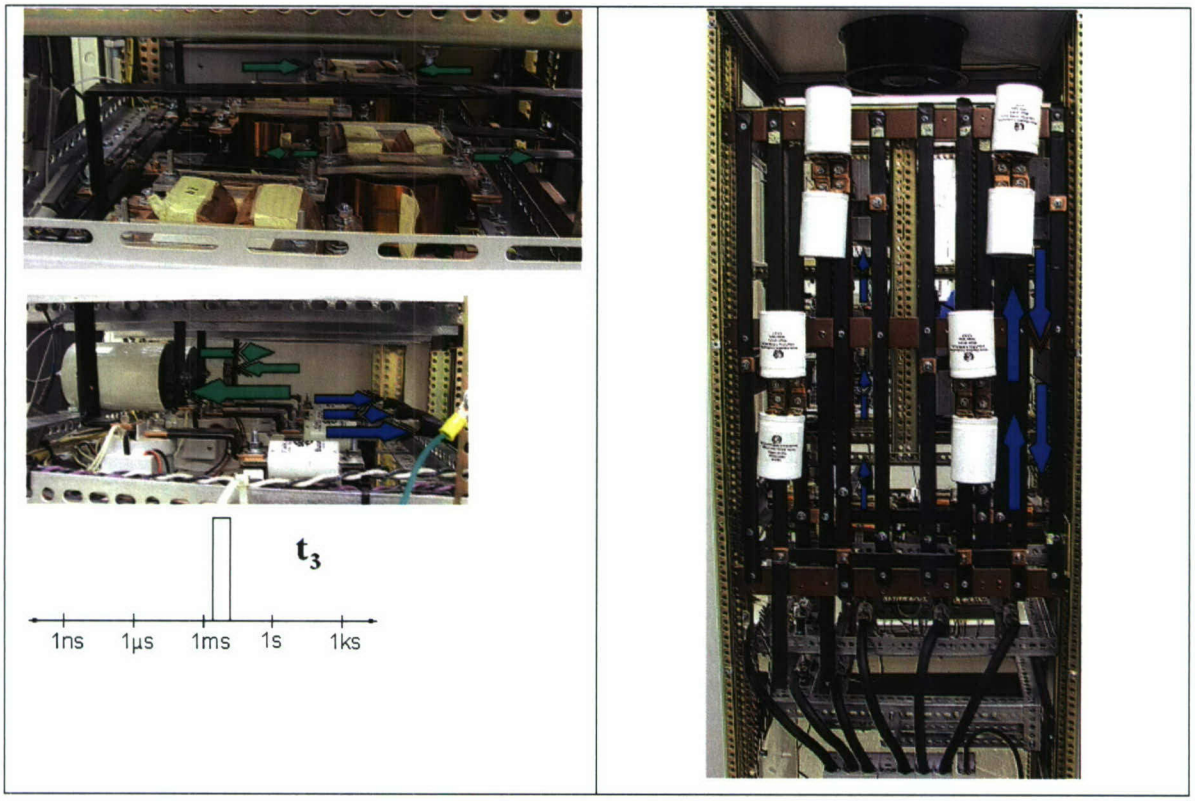


Fig. 4-31. Poynting Vector Analysis of the 3-Phase VSI PEBB Cabinet at time t3.

V. Alternate Method of Partitioning

The standard cell energy processing hierarchy was derived in terms of functionality of the various layers, so it is reasonable to validate the layers by how the processors in each layer handles energy. In order to do this, the standard cell hierarchy must be broken into sub-partitions that group common energy handling devices [6]. With such a method, the interfacing between layers and the partition of each layer becomes even better defined. Fig. 4-32 depicts such a sub-partition as described. The color codes for the vectors are the same one as defined in the legend in Fig. 4-14.

The horizontal partition in Fig. 4-32 is in terms of the energy handling behavior, being transfer and control of energy, storage, or thermal management. The vertical partition can be made in terms of functionality as already observable from the standard cell hierarchy. However, vertical partition is not just limited to functionality, but can encompass such issues as inter-module parasitics versus inter-component parasitics. The partition in Fig. 4-32 is not a solution but a step towards a proper solution. It was felt that creation of a horizontal partition would simplify validation of the vertical partition.

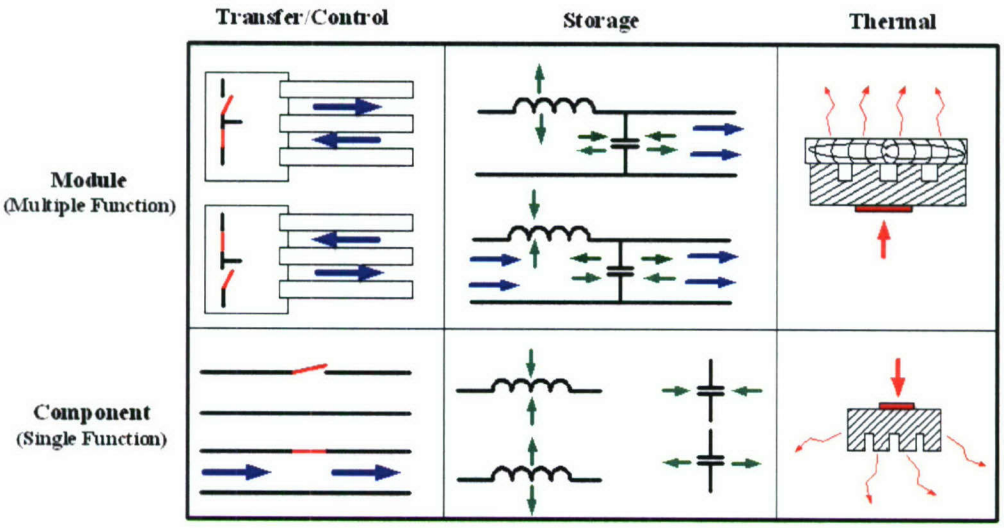


Fig. 4-32. The inter-layer partition created to group common energy handling devices together for a better defined vertical interfacing and partitioning.

VI. Busbar Design

VI.1. Thermal Criteria for the Busbar Design

The design of the busbars not only needs to consider the electrical aspects, but also needs to consider the thermal aspects of it. The objective of the thermal design of the busbars is to keep the temperature of the busbars below its maximum temperature; it includes the dimensions design of the busbar and the cooling system design.

There are different types of the busbars, the advantages and disadvantages are compared in The first step of the design is to calculate the total power loss on the busbar, which can be given by (19). Here, the resistance of the busbar includes the DC resistance and the AC resistance.

$$P_{loss} = I^2 R \tag{19}$$

The next step is to calculate the heat dissipation capability of the designed busbar. The heat can be dissipated through convection and radiation. The calculation of the radiation dissipation is given by (20).

$$P_r = k\varepsilon A\left(T_m{}^4 - T_{amb}{}^4\right) \tag{20}$$

where, k is the Stefan-Boltzmann constant; ε is the relative emissivity of the object; A is the exposed area from which heat energy is radiated; *Tamb* is the absolute ambient temperature.

The convection dissipation can be calculated by (21).

$$P_c = \bar{h}A(T_m - T_{amb}) \tag{21}$$

Table 1. The laminated structure busbar has some advantages over others structures, it is selected to be used in the system, and the following design is on the base of this structure. The cross section of the laminated busbar is shown in Fig. 4-33, the dimensions of the busbar are firstly design on the basis of electrical criteria. The maximum temperature of the busbar is limited by the material and its application, and assume it is T_m.

The first step of the design is to calculate the total power loss on the busbar, which can be given by (19). Here, the resistance of the busbar includes the DC resistance and the AC resistance.

$$P_{loss} = I^2 R \tag{19}$$

The next step is to calculate the heat dissipation capability of the designed busbar. The heat can be dissipated through convection and radiation. The calculation of the radiation dissipation is given by (20).

$$P_r = k\varepsilon A\left(T_m{}^4 - T_{amb}{}^4\right) \tag{20}$$

where, k is the Stefan-Boltzmann constant; ε is the relative emissivity of the object; A is the exposed area from which heat energy is radiated; T_{amb} is the absolute ambient temperature.

The convection dissipation can be calculated by (21).

$$P_c = \bar{h}A(T_m - T_{amb}) \tag{21}$$

Table 1. Comparison of different structures of the busbar.

	Advantages	**Disadvantages**
Wire Harness	. Inexpensive . Readily available . Can be Homemade . Flexible	. Higher self inductance . Larger geometry than solid cross-section of bus bar
Printed Circuit Board	. Suitable to low current application . High reliability in low current case	. Cannot carry higher current . Vias used to connect different layers cause the space and reliability problems
Bare Copper Bus Bar / Planar Side by Side	. Widely used in industry	. Do not provide the lowest effective mutual inductance for the distribution path . To minimize the mutual inductance, the bus bar would need to be placed directly on the top of one another
Laminated Bus Bar	. Lowest possible effective inductance . The AC conductors can be laminated into the bus assembly . Low contact resistance between the bushing surface and the conductor plates	

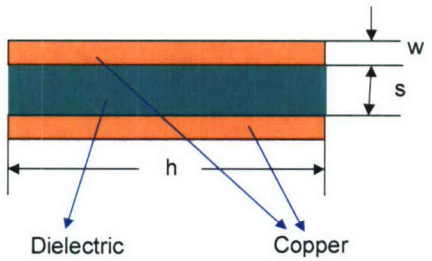


Fig. 4-33. Cross section of the laminated busbar.

where, $\bar{h}$ is the average value of the heat transfer coefficient, A is the exposed area from which heat energy is dissipated. The total heat dissipated is the sum of the radiation dissipation and the convection dissipation.

The calculation of the average value of the heat transfer coefficient is given by (22)-(25).

$$\bar{h} = \frac{\bar{N}_u * k}{L} \tag{22}$$

$$\bar{N}_u^{1/2} = 0.825 + \frac{0.387 R_a^{1/6}}{\left[1 + (0.492/P_r)^{9/16}\right]^{8/27}} \tag{23}$$

$$R_a = G_r * P_r \tag{24}$$

$$G_r = \frac{g\beta(T_w - T_\infty)x^3}{v^2} \tag{25}$$

VI.2. Using Poynting Vectors for Storage/Dissipation Analysis

A. Conduction Losses

The laminated busbar is shown in Fig. 4-34 which is used to derive the conduction loss by equations (26)-(34).

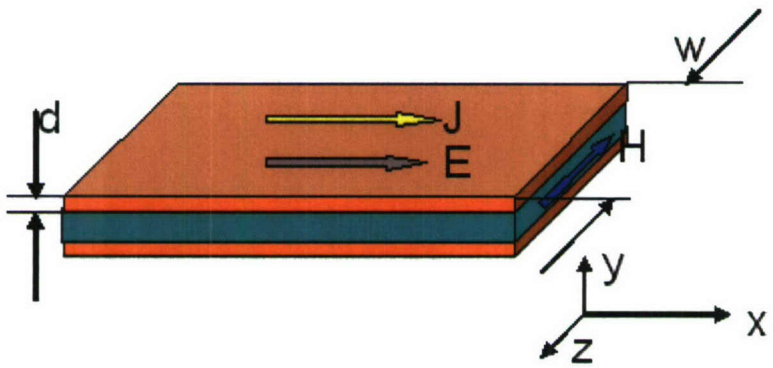


Fig. 4-34. Laminated busbar structure used for conduction loss calculation.

$$\nabla \times \vec{H} = \vec{J} \tag{26}$$

$$H = \int_0^d J dy \tag{27}$$

$$\vec{J} = \sigma \vec{E} \tag{28}$$

$$E = \frac{J}{\sigma} \tag{29}$$

$$\vec{S} = \vec{E} \times \vec{H} \tag{30}$$

$$S = EH = \frac{J}{\sigma} \int_0^d J dy \tag{31}$$

$$S = \frac{1}{2\sigma} \int_0^d J^2 dy \tag{32}$$

$$P = \oint_s \vec{S} d\vec{s} \tag{33}$$

$$P = \frac{1}{2\sigma} \int_0^w \int_0^d J^2 dy dz \quad \text{W/m} \tag{34}$$

Equation (34) indicates conduction loss per unit length.

B. Electric Field Energy Exchange of the Laminated Structure

For the structure shown in Fig. 4-34, the electric field exchange is calculated as derived by

$$S = EH = E \int_0^d J dy \tag{35}$$

$$P = -\oint_s \vec{S} \cdot ds = \iiint_v \left(\frac{\partial \left(\frac{\varepsilon \vec{E}^2}{2} \right)}{\partial t} \right) dv \tag{36}$$

$$W = \int_0^t P dt \tag{37}$$

$$W = \frac{\varepsilon \omega E_0^{\ 2}}{2} \quad \text{J/(m}^3\text{s)} \tag{38}$$

where,

E_0 = the peak value of electric field strength.

Equation (38) indicates electric field energy exchange per second per unit volume.

C. Magnetic Field Energy Exchange of the Laminated Structure

For the structure shown in Fig. 4-34, the magnetic field exchange is calculated as derived by

$$S = EH = \mu H \int_0^h \frac{\partial H}{\partial t} dy \tag{39}$$

$$P = -\oint \vec{S} \cdot d\vec{s} = \iiint \left(\frac{\partial \left(\frac{\mu \vec{H}^2}{2} \right)}{\partial t} \right) dv \tag{40}$$

$$W = \int_0^t P dt \tag{41}$$

$$W = \frac{\omega \mu d J_0^{\,2}}{2} \tag{42}$$

where,

J_0 = the peak value of current density

Equation (42) indicates magnetic field energy exchange per second per unit volume.

VII. Conclusion

Poynting vector provides a unique perspective on how energy flows through the various electrical components and structures and how energy is dissipated and converted into thermal energy. Due to the geometrical dependence of energy flow, Poynting vector offers an alternate design tool to build a well partitioned system and modules that provides the best trade-off in terms of electrical and thermal parameters.

The potential to validate and create partitions using Poynting vectors and the associated time constants was explored in this chapter. Several electrical components and structures were analyzed using Poynting vector and a view of how energy flows throughout the structure was attained. Definite partition validations of the standard cell hierarchy were not completed during this phase of the project, but the work conducted in this phase has provided a good foundation for any future work. Lumped element parameters were looked upon in order to acquire any insight that could be garnered to be applied towards the standard cell hierarchy partition. A further intra-layer partition was proposed in order to simplify and facilitate inter-layer partition validation. Finally, the thermal design of a DC busbar was performed using

these tools, determining its conduction losses as well as characterizing by means of the Poynting vector the magnetic and electrical energy exchange parameters of it.

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Chapter 5 PEBB INTERFACE CHARACTERIZATION

I. Introduction

The Power Electronics Building Block (PEBB) or module was conceived to become a fundamental piece of future power electronics conversion systems, providing the required modularity to enable complete system designs based on desired functions as opposed to designs based on detailed involved electromagnetic specifications. The goal of the PEBB interface characterization presented in this chapter has been to initiate research and discussions leading to establishing a true basis for PEBB model-based specification at the system level. Specifically, this study defines standard interfaces for the PEBB as an example of hierarchical system partition. It serves as a step towards the development of standard-cell PEBB-based converter system design, which shall result in significantly reduced design cycles, but most importantly allowing non power electronics specialists to completely design and build a system. Or simply put, filling in the knowledge gap between power converter specialists and system engineers.

The approach to PEBB interface characterization is based on existing plug and play (PnP) PEBB hardware in order to facilitate easy characterization and validation. The characterization undertakes a multi-physics approach with interface characteristics covering electrical, control, thermal, and mechanical aspects. The study will provide a behavioral model to go along with the list of parameters that range from detailed list (model) to simplified list. Development and verification of the study will be achieved through a PEBB based design using the interface characteristics.

II. Electrical Characteristics

The PEBB interface characterization overview is depicted in Fig. 5-1. The five-type of interface characteristics are manifested on top of the bus in the figure. The electrical characteristics are analyzed in this section.

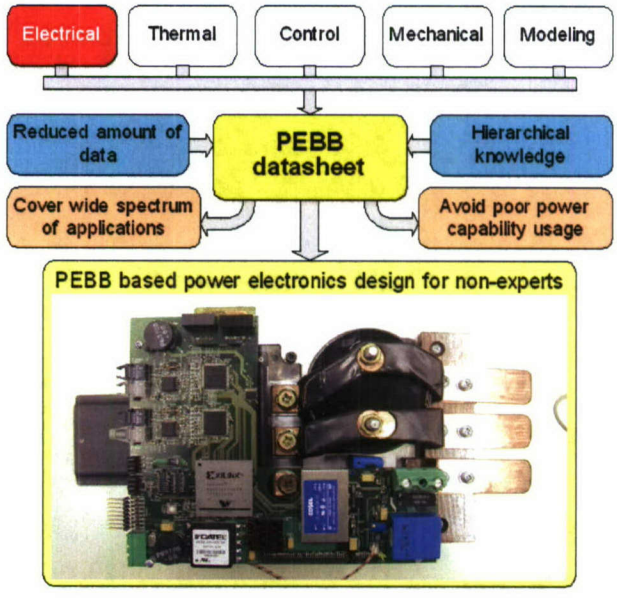


Fig. 5-1 . PEBB interface characterization overview.

A PEBB provides a determined set of functions throughout all the applications present in a system. The degree of details in a PEBB description can be expressed as functions, parameters and ranges, and mathematical relations. The common set of functions at the PEBB level can be stated as follows:

1- Switching control (modulation)

2- Pulse gating

3- Safe commutation enabling

4- Primary protection of devices

5- Energy storage at the DC bus

6- Energy storage at the AC bus

7- Vdc measurement

8- Iac measurement

9- PEBB auxiliary power supply

10- Data communication

In particular the functions at the switching-cell level, which is located one level below PEBB in the hierarchy under question, are given as follows for a voltage-source type converter:

1- Bi-directional I conduction

2- One-directional V blocking

3- Ability to control on-off state

The listed set of functions is provided by the different components in the PEBB. Those components can be generally grouped into four categories:

- Power Module (IGBT): transistor, diode, primary protection
- Energy Storage requirements: AC side, DC side
- Sensing: DC Voltage, AC current (AC voltage)
- Auxiliary power supply

The behavior of the PEBB is the result of the combination of the characteristics of all the components in it. Some of those characteristics are seen directly from the interface while some others are modified due to interaction among the PEBB components. As already mentioned, the main interest here is to find the PEBB characteristics seen from the outside of the PEBB, i.e., its terminal connections. This concept is schematically shown in Fig. 5-2.

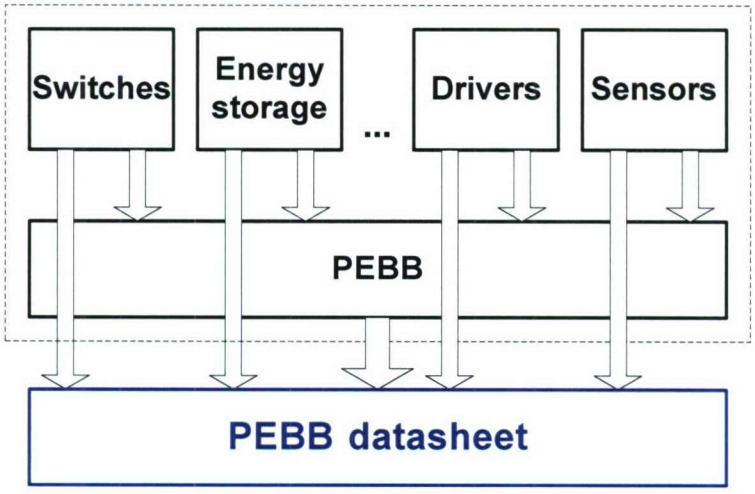


Fig. 5-2 PEBB description seen from its interface.

II.1. Simplification of the Behavioral Model

When looking for the information needed to describe the PEBB from its interconnection terminals, i.e., the interface to the rest of the system, it is important to consider how the PEBB will be integrated in a converter. It is also important to analyze the design process of a PEBB based converter, as the characteristics that are relevant for design will also be relevant for the type of PEBB description we are looking for. Previous to this, the classical or non-modular design process of a power converter must be analyzed in order to find what data is required in that process.

There exist already in the market intelligent power modules or IPM's. These modules integrate the power semiconductors together with their gate drivers, protection functions and current, voltage and temperature sensors. Analysis on how these sub-systems were integrated can provide good insight for our task of describing the characteristics of the PEBB. At the intelligent power modules, the devices are integrated together with their gate drivers in a way that their operation in the safe operation area (SOA) is guaranteed. A basic protection scheme is added to ensure that this is fulfilled. After this integration is achieved, most of the device data characteristics like the SOA description are not necessary when a circuit is implemented using this module. Therefore, all that information does not describe device characteristics that are needed for its implementation and hence they are not relevant when looking from the module interface. The same concept is applied when the power module and other components are integrated into the PEBB. This process of simplifying the information required when using the device in a module is represented in Fig. 5-3. The first degree of simplification in the description was achieved while integrating the intelligent power module. As was explained, it greatly simplifies the converter system design process. Therefore, integrating the module into the PEBB will further simplify the design of power converters based on the PEBB concept while reducing the amount of detail in the data required for such design. This is represented by the second simplification step shown in **Error! Reference source not found.**.

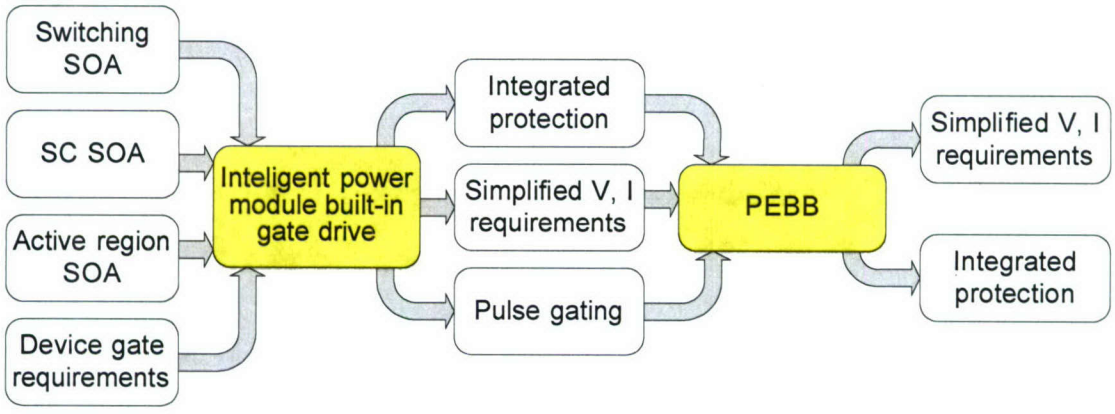


Fig. 5-3 The information describing the power devices from their connection point of view.

The idea discussed in the previous paragraph can also be applied to other aspects of the PEBB integration. Fig. 5-4 shows the simplification in the amount of information describing the semiconductor devices when all are integrated in PEBB. In this case, obtaining the PEBB description requires combining the device data together with the characteristics of the other components that compose the module cooling system. In addition, other data requirements related to the way the converter will operate may be needed, like the commutation type and modulation scheme.

II.2. PEBB Electrical Interface Characterization

The final interface characterization for the electrical aspect of the study is given by Table 5. 1.

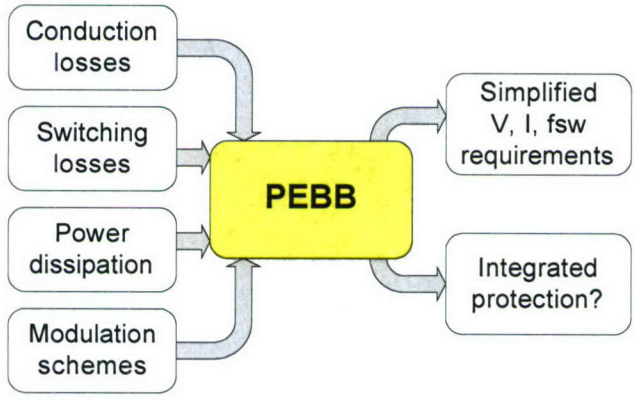
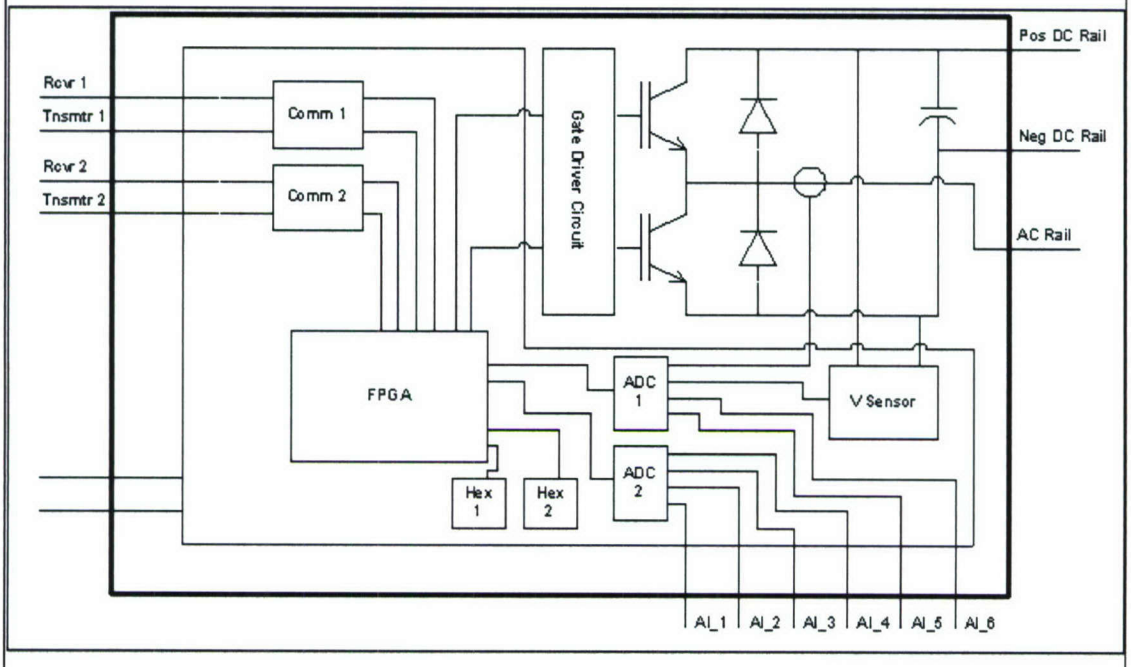


Fig. 5-4 Losses and dissipation information for PEBB description from its interface.

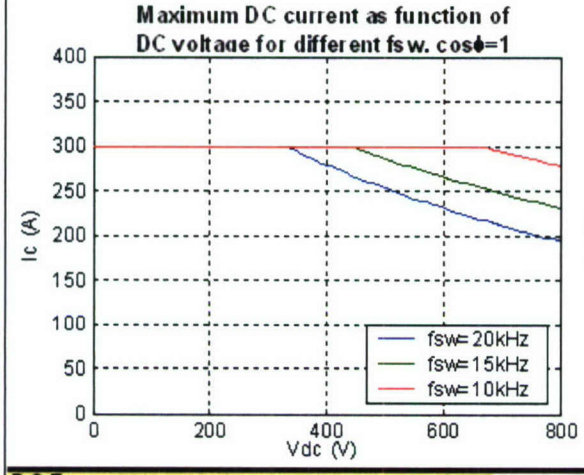
Table 5. 1. PEBB electrical interface characterization.

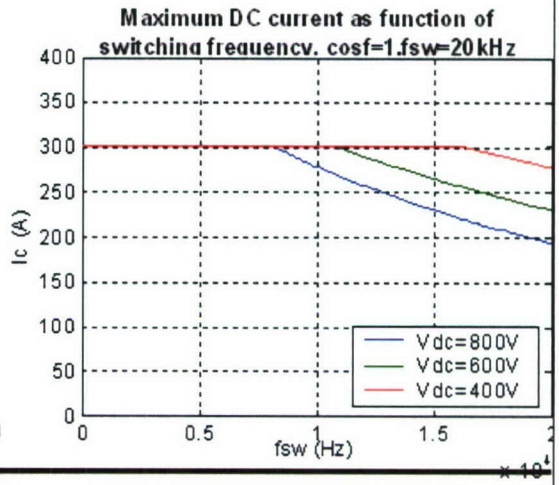
Equivalent circuit



General requirements	name	type	conditions	values
Maximum DC voltage	V	Vdc		800
Maximum switching frequency	f_{PWM}	kHz		<20
Maximum power dissipation in switch	Pc	Pavg	Tc=25°C	1380
Insulation test voltage	Visol	Vrms	1 min	2500

Power-cell functions	name	type	conditions	values
Collector emitter max voltage	Vces	V pk	Tj=25°C	1200
Maximum DC voltage	Vcc(surge)	V dc	Tj=25°C	1000
Maximum DC voltage protected by SC	Vcc(prot)	V dc	Tj=25°C	800
DC current (IGBT, forward diode)	Ic	I dc	Tc=25°C	300
Peak current (IGBT, forward diode)	Icp	I pk	Tc=25°C	600
Arm shoot through blocking V	tdead	msec	per signal	>3.5





DC Energy storage				
DC capacitance	Cdc	uF	Ta=25°C	35
Stray inductance	L	nH		25
maximum current rms	A	I rms	Ta=25°C	72.6
Equivalent series resistance	ESR	mohm		1.02

Primary protection	name	type	conditions	values
Short circuit trip level	SC	A dc	-20°C<Tj<125°C	330<SC<425
Short circuit current delay time	toff (SC)	usec	rated Vsupply	10
Over-temperature trip level	OT	deg C	rated Vsupply	110
Over-temperature reset level	OTr	deg C	rated Vsupply	95
Auxiliary supply under V trip level	UV	V dc	-20°C<Tj<125°C	12
Auxiliary supply under V reset level	UVr	V dc	-20°C<Tj<125°C	12.5

Sensing characteristics	name	type	conditions	values
Voltage range	V_{PN}	V inst		10-1500
Overall voltage accuracy	X_G	%	max V_{PN}, Ta=25°C	0.8
Current measuring range	I_P	A inst		0-300
Current accuracy	X	%	max I_{PN}, Ta=25°C	0.65
Response time	t_r	usec	90% range	<25

Auxiliary power supply	name	type	values
Voltage supply for power module, sensors	V_{aux}	V dc	5
Voltage power module tolerance	$\%V_{aux}$	%	10
Current supply for PEBB	I_{aux}	mA dc	50

Ambient conditions	name	type	values
Operating temperature	Ta	deg C	0-40
Humidity	relative	%	95
Altitude		m	<1000
Lifetime		years	>20
Reliability		hrs	>8760
Shock	Mil-Std-810B		15g,11ms, any axis
Vibration		0.32mm pk accel	<57 Hz
Seismic	seismic code		zone 4
Acoustic noise		dB	<78

III. Thermal

The PEBB phase-leg topology under study is shown in Fig. 5-5. The actual components used to build the physical PEBB phase-leg is given by Table 5. 2. The heat generation in a PEBB phase-leg is caused by the IGBT, diode, power passives, and busbar. Heat dissipation is undertaken by the heat sink and fan. Temperature sensing/monitoring is also implemented within the IPM.

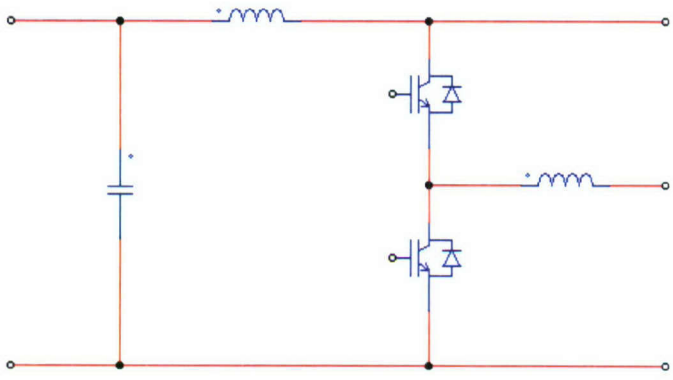


Fig. 5-5 Generic PEBB phase leg.

Table 5. 2. Data relevant for interface description of the components used in the PEBB under study.

IGBT	PM300 DVA120
Busbar	Alloy 100 copper
Heat sink	Surface area = 152.4mm x 203.2mm Fin No. = 60
Cooling method	Forced air cooling

The parameters to be included in the characterization are:

- Ambient temperature
- Maximum working temperature
- Minimum cooling ability
- Suggested cooling system
- Maximum continuous power

If the users want to design the thermal function, then the following parameters are also needed in the characterization, otherwise that information can be considered internal to the PEBB:

- Thermal impedance of module
- Equations or graphs to calculate the module temperature under given voltage, current and frequency

The final thermal interface characterization is included with the electrical interface characterization as shown in Table 5. 1 due to the fact that the thermal criteria is very much an integral part of the electromagnetic aspect of the converter.

IV. Control

This section studies the converter level control, in particular the interface between the power converter and the PEBB controls as shown in Fig. 5-6. The control interface defined in this characterization is shown in Fig. 5-7. At this interface, the converter controller sends control commands (typically duty cycles) to the power stage, and receives feedback from the power stage. Before we define this interface, two assumptions are made:

1. All the information exchanged at this interface is digital;
2. The analog-to-digital (A/D) and digital-to-analog (D/A) conversions are implemented inside the PEBBs.

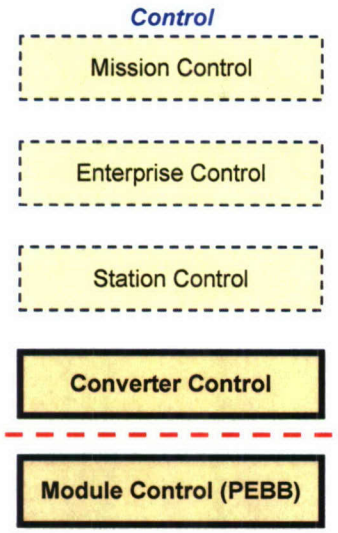


Fig. 5-6 Hierarchical control reference model.

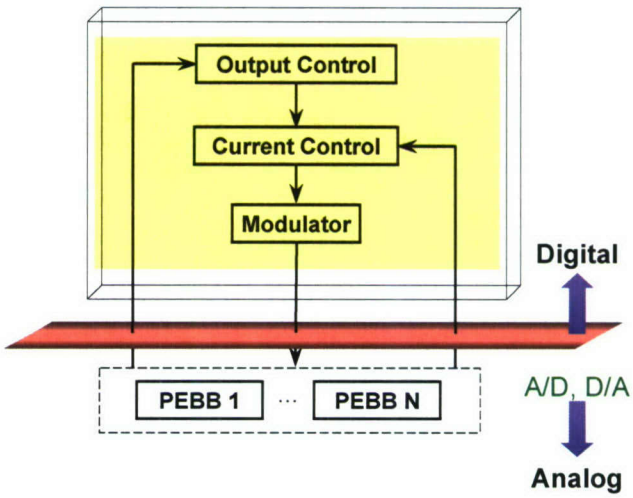


Fig. 5-7 Control structure in PEBB-based power conversion systems.

Table 5. 3. Application requirements.

Speed Regulator Response	with Tach 132 Rads/Sec, t=7.1ms @ 1.5Khz without Tach 15 Rads/Sec
Torque Requlator Response	Tpk=3.0ms @ 1.5Khz
Torque Bandwidth	1047 Rads/Sec @ 1.5Khz
Torque Accuracy	<2% of Rated Torque
Starting Torque	Up to Current Limit
Field Weakening Point	20 - 200 Hz Adjustable
Dynamic Braking	0.5PU Continuous Braking, 1.OPU for 60 sec (700 A Load)
Efficiency	>96% at Rated Load
Switching Frequency	20Khz
Modulation Type	PWM
Modulation Method	Right-aligned, center-aligned, left-aligned, etc
Transient Response	0.2 ms at step load
THD	IEEE-519
DC Bus Voltage/Current	800V with 5% ripple
AC phase voltage/current	200V with 2% ripple/120A

The design and composition of the control is dictated by the requirements of applications. Table 5. 3 shows a list of requirements of an example application based on what the converter level control can also be defined. It can be seen that some requirements can be achieved through selected control algorithm and computation parameters, such as the requirements on torque. With the definition of hierarchical control in power conversion systems, these are the features that may be transparent to the module level control. On the other hand, in the application requirements, there are some features that are directly related to the specifications of the lower level power modules, such as switching frequency, transient response, etc. Commercially, there are many power modules available today with integrated gate drivers and local protections such as the Toshiba IPM described by Table 5. 4.

Table 5. 4. Control characterization of a Toshiba IPM.

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Control Circuit Current	High Side	$I_{D(H)}$	V_D=15V	—	8	—	mA
	Low Side	$I_{D(L)}$		—	24	—	
Input-On Signal Voltage		$V_{IN(on)}$	V_D=15V, I_C=50mA	1.3	1.5	1.7	V
Input-Off Signal Voltage		$V_{IN(off)}$	V_D=15V, I_C=50mA	2.2	2.5	2.8	V
Fault Output Current	Protection	$I_{FO(on)}$	—	8	10	12	mA
	Normal	$I_{FO(off)}$		—	—	1	
Over Current Protection Trip Level	Inverter	OC	V_D=15V, T_j=125°C	75	100	—	A
	Brake			40	—	—	
Short Current Protection Trip Level	Inverter	OC	V_D=15V, T_j=125°C	110	150	—	A
	Brake			60	—	—	
Over Current Cut-Off Time		$t_{off(OC)}$	V_D=15V	—	5	—	μs
Over Temperature Protection	Trip Level	OT	Case temperature	110	118	125	°C
	Reset Level	OTr		—	98	—	
Control Supply Under Voltage Protection	Trip Level	UV	—	11.0	12.0	12.5	V
	Reset Level	UVr		—	12.5	—	
Fault Output Pulse Width		t_{FO}	V_D=15V	1	2	3	ms

Since the interface of the power module is analog, the characterization mainly describes the electrical and thermal aspects. From control point of view, PEBB is defined as a half bridge power module that can

receive voltage reference and send out the local current and voltage measurements as feedback, as depicted by Fig. 5-8.

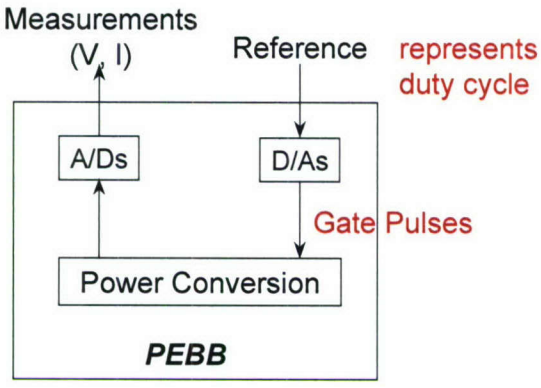


Fig. 5-8 Control interface definition of PEBB.

So, based on the definition of PEBB, the interface characterization of the control aspect at the converter level is given by Table 5. 5. The transitions between operational states of the PEBB module are given by Fig. 5-9.

Table 5. 5. Characterization of the control interface.

Parameter	Description	Ratings and Values
Input		
REF	represents duty cycle of top switch	Ref(min) to Ref(max) 32-bit integer
CNTL	control commands	Start, Stop, Sync, Config, etc. 4-bit binary
Output		
Measurements:		
I	sensed cuttrent	32-bit floating point Fs = 1MHz Accuracy 0.1%
V	sensed voltage	32-bit floating point Fs = 1MHz Accuracy 0.05%
STAT	PEBB operational states	Normal, Fault, ...etc 4-bit binary
Properties		
C_DLY	communication delay	1ns
Thru	transmission throughput of optic fiber	125Mbps

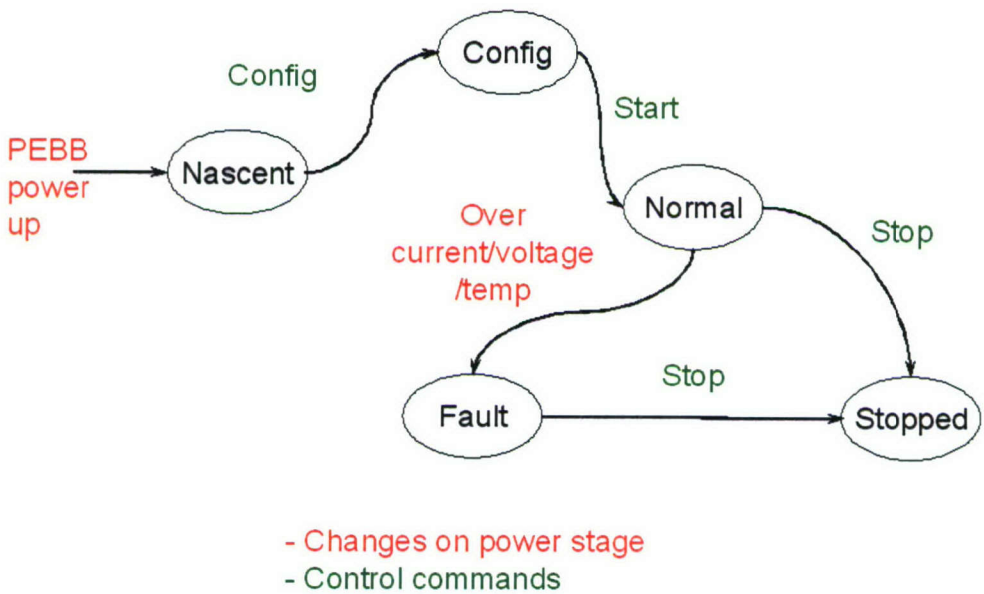
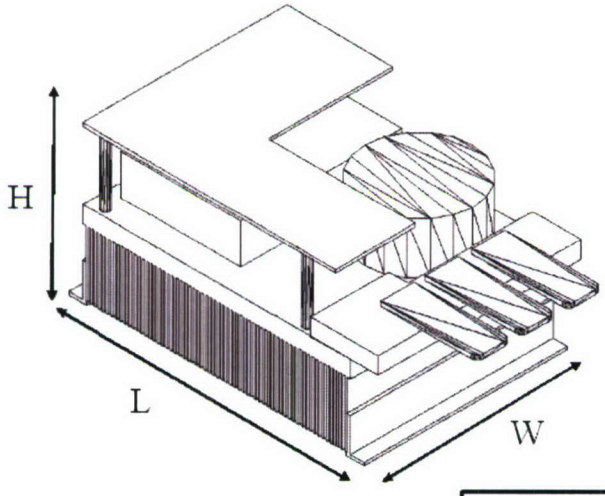


Fig. 5-9 PEBB operational state transitions.

V. Mechanical

The mechanical characteristics of the current PEBB phase leg module are demonstrated by Fig. 5-10. The external connections required by this module are given by Table 5. 6. When designing the mechanical aspect of a PEBB, there are various issues to be considered such as vibration, shock/impact, acoustic noise, humidity, thermal expansion, and mechanical stresses. These issues must be addressed in the interface characterization.



Length:	8.75" (eff.)
Width:	6"
Height:	5.5" (eff.)
Weight:	9.8 lbs.

Mounting:	Sliding Rails
Required Cooling:	Forced convection

Fig. 5-10 Mechanical characteristics of the current PEBB phase leg.

Table 5. 6. External connections.

+5 V, GND Bias:	2-terminal Phoenix Connector
DC Link (+):	Copper-blade bus connector
DC Link (-):	Copper-blade bus connector
AC (Midpoint):	Copper-blade bus connector
Transmitter:	(2) Fiber-optic transmitters
Receiver:	(2) Fiber-optic receivers
Analog inputs:	(6) Mini-SMB connectors

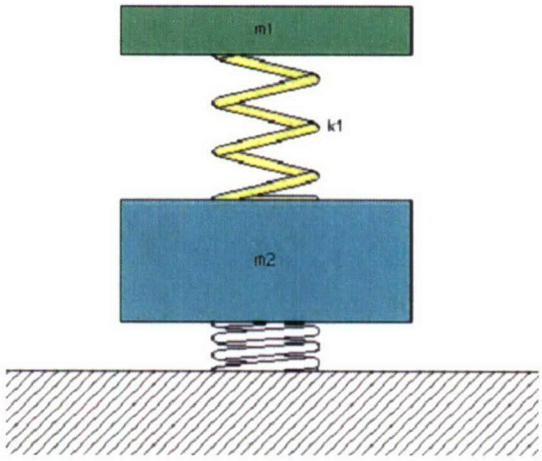


Fig. 5-11 Vibration model.

So a simplified specification is drawn up. For example, if a device is mounted as follows:

- Not mounted upside down

Then, the following can be guaranteed:

- Withstand certain vibration intensity
- Acoustic noise is below certain specified level.

VI. Modeling

The typical design and modeling approach towards realization of a system is depicted by **Error! Reference source not found.**. The goal of the modeling aspect of interface characterization is to realize an exact and precise model of the power system through physics-based mathematical description of the power system by capturing electro-magneto-thermo-mechanical phenomena occurring throughout the system.

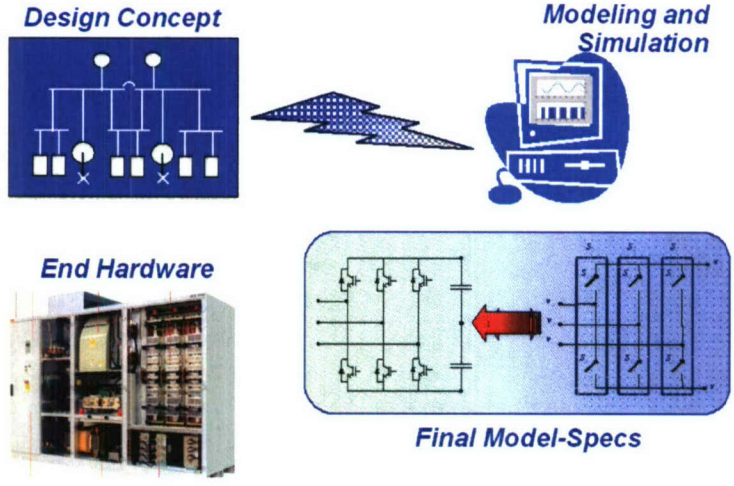


Fig. 5-12 PEBB/modeling design approach.

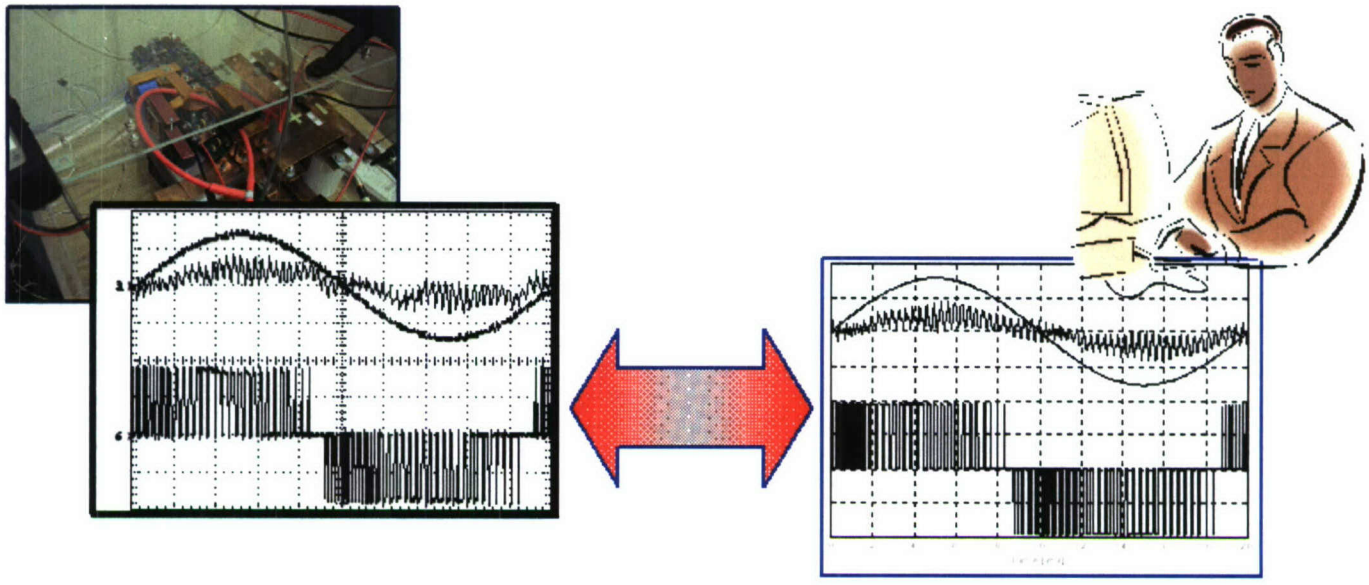


Fig. 5-13 Perfect match between model and hardware implementation.

The goal will be achieved when the hardware and model exhibit a perfect match in behavior and performance as shown by Fig. 5-13

The PEBB is supported by two types of software models developed in VTB, namely a switching and an average model. The former is a physics-based model and hence captures all electro-thermal phenomena generated by the switching action of the PEBB, while the latter is solely an electrical model operating at the fundamental frequency usable for control design and power system studies. The switching model and average model is demonstrated by Fig. 5-14 and Fig. 5-15 respectively.

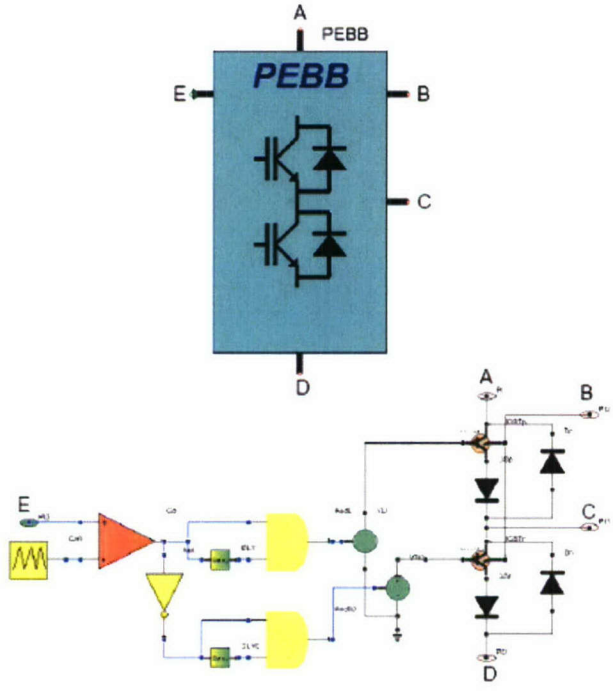


Fig. 5-14 Physics-based switching PEBB model.

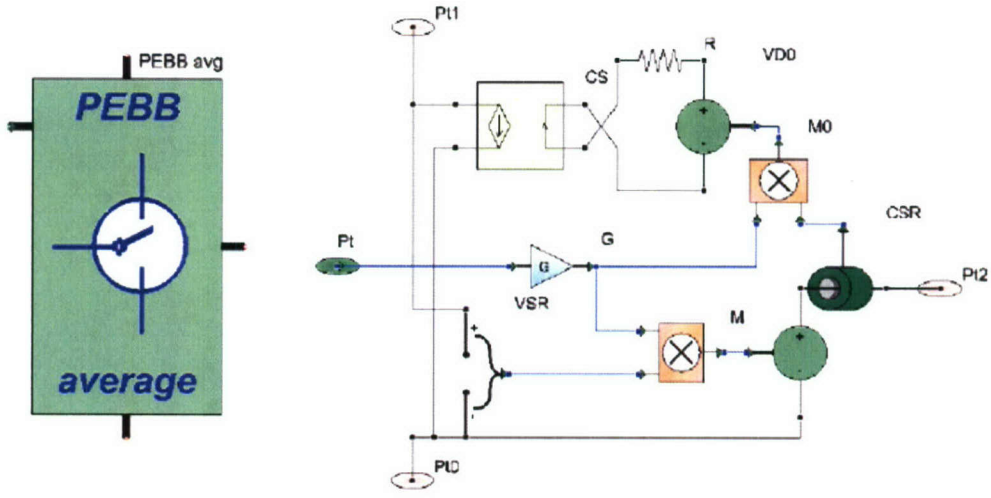
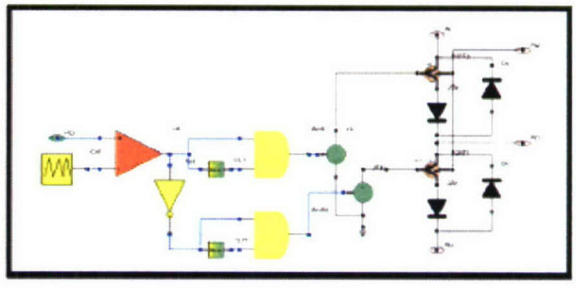


Fig. 5-15 Transfer function based on average PEBB model.

As an example, the vibration model is depicted in Fig. 5-11 The system is first designed and simulated in a computer. Vibration and other mechanical aspects are included as part of the parameters. Complete computer simulation is to be used before building a prototype. Iterative building processes are eliminated. However, such a lengthy process may be too detailed and cumbersome for the end-user. The description of the switching model in VTB is given by Table 5. 7 with the IGBT model parameters given by Table 5. 8 . The description of the PEBB average model is given by Table 5. 9.

Table 5. 7. PEBB model description in VTB.

Terminal	Type	Name
A	Power	DC Bus +
B	Thermal	Losses
C	Power	AC Pole
D	Power	DC Bus -
E	Control Input	M Signal



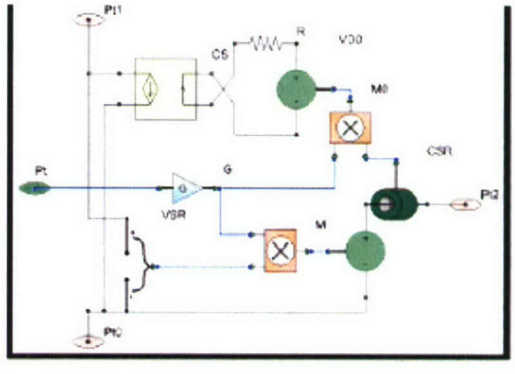
Parameter	Description	Usage notes
fsw	PEBB switching frequency	Set in carrier signal generator
M	Modulating signal	Maximum amplitude is '1'
Delay	Gating signal deadtime	Regulated through sampling period and actual delay samples
AND	AND gates	Output values must be set at 0 and 15 V
IGBT	PM300DVA120	Turn-on/off times modified through its Gate capacitance and resistor values
DS	Series-connected diode	Required to block negative currents
D	Flywheel diode	- - -

Table 5. 8. IGBT model parameters.

Name	Description	Value	Units
Resistance_1	Thermal Resistance1 R1	0.00673	Ω
Resistance_2	Thermal Resistance2 R2	0.0021	Ω
Resistance_3	Thermal Resistance3 R3	0.001609	Ω
Resistance_4	Thermal Resistance4 R4	0.0005588	Ω
Capacitance 1	Thermal Capacitance1 C1	5.067	F
Capacitance 2	Thermal Capacitance2 C2	52.002	F
Capacitance 3	Thermal Capacitance3 C3	303.164	F
Capacitance 4	Thermal Capacitance4 C4	886.218	F
Gate Resistance	Gate Resistance Rg	13.0	Ω
Gate Capacitance	Gate Capacitance Cg	150 E-9	F
Voltage on	Controlling Voltage for on state	10	V
Voltage off	Controlling Voltage for off state	5	V
On Resistance	Resistance of Rs for on state	0.00008	Ω
Off Resistance	Resistance of Rs for off state	1 E+6	Ω
Re_300	Linearized on-state resistance at 300K	0.00315	Ω
VE_300	On-state voltage at zero current at 300K	2.25	V
Alpha	Temperature dependence exponent for on-state resistance	1.17	n/u
Beta	Temperature dependence exponent for on-state voltage at zero current	0.37	n/u
Vce_max	Maximum collector-emitter voltage	6500	V
Ic_max	Maximum collector current	600	A
Tj_max	Maximum junction temperature	423	°K

Table 5. 9. PEBB average model description in VTB.

Terminal	Type	Name
A	Power	DC Bus +
B	Power	AC Pole
C	Power	DC Bus -
D	Control Input	M Signal



Parameter	Description	Usage notes
M	Modulating signal	Maximum amplitude is '1'
Gain	Voltage Gain	Set at 0.5
Current Sensor	AC current sensor	Series resistance kept lower than 1mΩ
Current Source	PEBB input current	Its gain must be reciprocal of controlled voltage source resistance
Voltage Source	Generates input current	
R	Voltage Source resistance	Its value must be reciprocal to the controlled current source gain

VII. Conclusion

The requirements on the PEBB were obtained through analyzing the converter design process. It has been shown that integration of components in standard modules simplifies the design of complex systems. There also exists a hierarchy in the interface characterization such as the one in the system modeling. Specifically, a set of PEBB functions were defined from the electrical, thermal, and control point of view. The requirements and interfaces for each of these aspects were analyzed and summarized. Additionally, an approach to simplification of the mechanical characterization of the PEBB was also presented. A characterization for switching (detailed) and average PEBB models was introduced.

Chapter 6 PEBB HARDWARE

I. Introduction

The continuing improvement of the PEBB initiative has been one of the aims of this project. Following a second production run of the PEBB controller boards, named Hardware Managers, the PEBB and the PEBB-based converter test bed have been fully tested and its operation improved. The converter finally operates as an integrated unit having all its components working in unison. This has been made possible by the collaborative effort of the team, in tackling problems ranging from hardware and software issues found in the Hardware Manager and PESNet communications protocol.

I.1. Background

The premise of the PEBB concept is that the traditional power converter is now partitioned in standard units (Fig.6-1) [1]. Therefore, practically any converter could be "synthesized" from these modules [2]. With the specifics about the power modules untouched, the user is left responsible for the application control only. This is purely a software task, and can itself be modular in construction [3]. This concept has already been embraced by industry [4-5]. The PEBB Hardware (Fig. 6-2) embodies the familiar half-bridge topology. The PEBB module includes the power switches (half-bridge IGBT IPM), a high-quality film dc-capacitor, the Hardware Manager, and a supporting heatsink (see Fig. 6-3).

The aim of the project is thus to make a PEBB module whose operation is self maintained and that, for the upper-level control layers, appears as an ideal single-pole double-throw switch (SPDT) as shown in Fig. 6-4. For this to be true, the PEBB controller must be able to compensate for inverter non-idealities and be responsible for every aspect of the power processing functions. These functions include the modulator – gating of the power switches and all related aspects– as well as voltage and current sensing, local protection, and communication with other PEBB modules or simply nodes in the communications network.

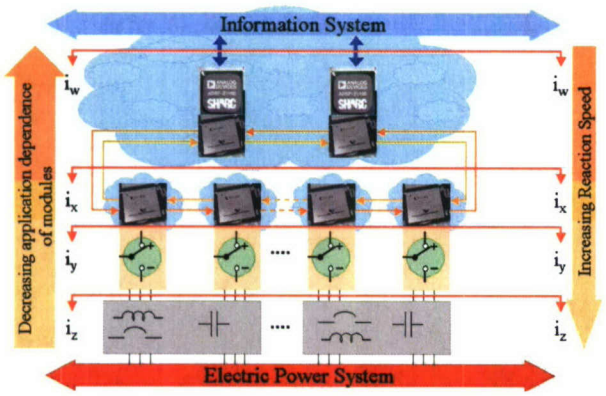


Fig.6-1. PEBB-based distributed power conversion system. Hierarchical diagram showing PEBBs, Universal Controllers, and system partitioning layers.

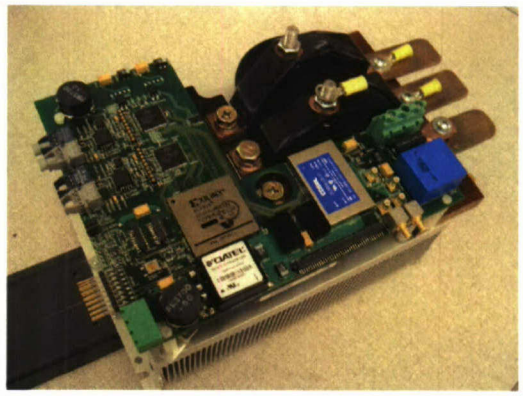


Fig. 6-2. 33 kW PEBB module with HM, IPM, film capacitor, I and V sensors, and heatsinks.

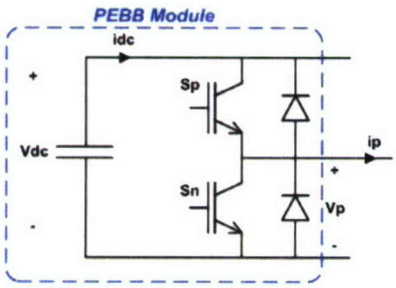


Fig. 6-3. Topology of the PEBB module.

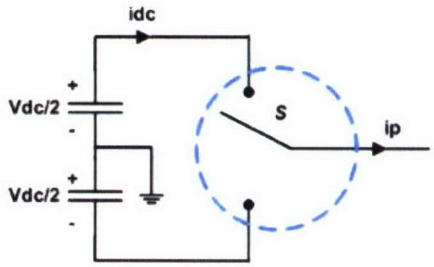


Fig. 6-4. Modeling of the PEBB as SPDT switch based "power gate."

A. Original topologies

The PEBB concept revolves around a module, the PEBB, which can be easily combined to assemble different topologies. In the hardware side, this would entail only the mechanical interconnections between modules, dc-bus, etc. Thus the converter itself is unmodified in hardware, regardless of topology. The only true change is the application level control, which is a purely software task. Some of the topologies that can be synthesized with our PEBB module are shown below, in Fig. 6-5.

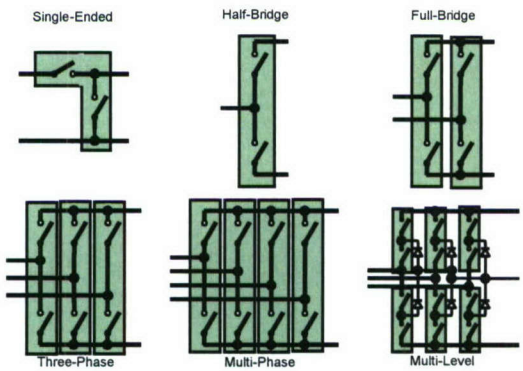


Fig. 6-5. Various topologies synthesized with the PEBB module.

II. Work

II.1. Hardware Manager Manufacturing

The Hardware Manager board prototype has undergone two manufacturing and population runs during the past two years of the project. The board design and layout obtained in the previous project was used for the first production, in which six boards were manufactured, and two populated. These tasks were outsourced to companies that we have had good contact and experiences in the past. As expected with any prototype, there were some setbacks, including the loss of one of the prototype boards. The boards design was corrected and improved, and subsequently sent for another production run.

Before the second manufacturing run, several modifications were made to the board design in hopes of, firstly, correcting the flaws that led to the failure of one of the prototypes, and secondly, to the improvement of the board reliability. These modifications are discussed in what follows. Additionally, the prototype productions details are listed.

A. Design Modifications

As mentioned above, the initial prototype production run resulted in two populated boards, one of which survived. Upon contact with the manufacturer and the company that performed the part population, it was concluded that the cause was the faulty placement of the vias (throughways for signals to connect to different layers of a PCB) that access the FPGA, combined with the not thorough etching of the board plating. Some of the vias had been placed too close to the device, and that could have led to the escaping of the solder bumps through the very vias. This could have also led to the shorting of signals, as the solder bump could have shorted to another via.

The problem was to be fixed before the second production run. This was a time consuming task, involving the replacement of several hundred vias which, in many occasions, involved the re-routing of many signal lines. This was very important, however, since it essentially guaranteed that no such faults would occur again. Fig. 6-6 illustrates the correction, showing a "before" and "after" picture of a portion of the FPGA.

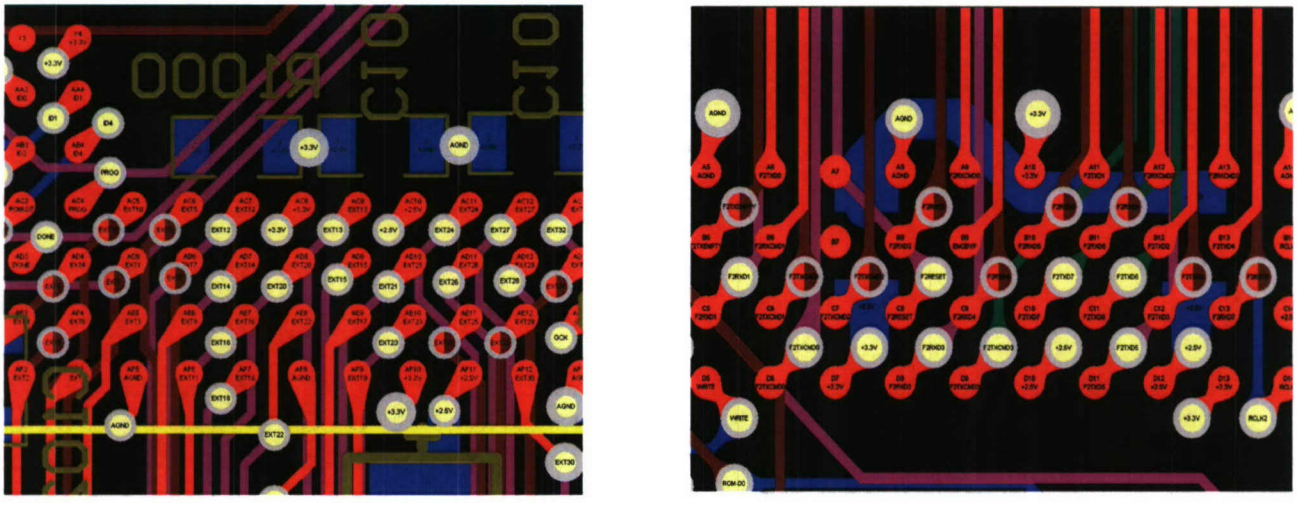


Fig. 6-6. Routing of vias to the FPGA before (left) and after (right) correction.

Another modification made was to the high-speed communications area. Following the white-paper published by Agilent for use with their high-speed transmitter and receivers, the layout of the traces were modified to be thicker (at least 20 mils) and to follow as close as possible the shape and positioning as recommended by the manufacturer. Fig. 6-7 shows the improvement in this area.

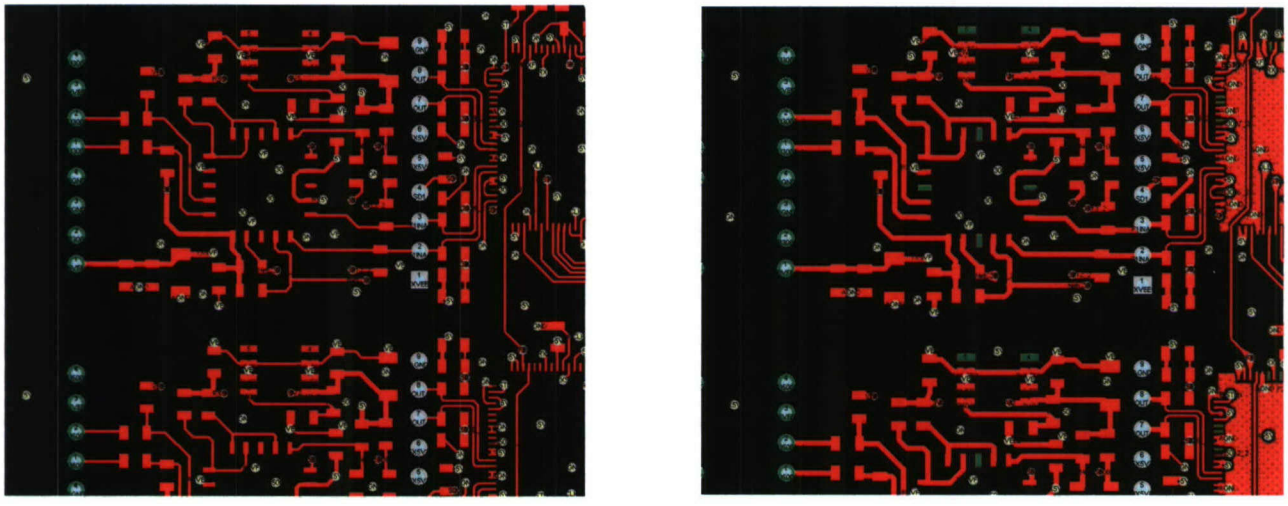


Fig. 6-7. Traces of the fiber optic transceiver circuit, before (left) and after (right) improvements.

Additional circuits and corrections were added to the present version of the Hardware Manager, including a solid-state circuit breaker, improved analog input connectors, and corrected LED interface. The solid-state circuit breaker adds another level of protection, ensuring a fast protection to the control circuitry. The breaker uses an IC from Maxim (MAX4370) to control and monitor the slew rate of the input current to the board. The chip uses a negligible amount of power, and the external MOSFET was selected for its very low on-resistance. Using two internal comparators, the chip is able to control current spikes, as well as shut down in case of a short-circuit. This proved especially important in the initial testing stages, when shorts frequently occur due to the faulty components, incorrect polarity of components, as well as possible routing mistakes.

Improved analog connectors substituted a simple dual-row header connector. The new connectors were of the "mini-coax" type, a small version of coaxial connectors. These are traditionally suitable for low noise RF applications, and should prove useful in our power converter. The Hardware Manager has six available analog inputs, which can be used for remote current or voltage sensing, a heatsink temperature sensor, or many other detection or protection functions.

B. Production Details

This section summarizes the production details of the two manufacturing runs of the Hardware Managers. The manufacturing process of this board is a time-consuming process, magnified by the complexity of the board, and the number of components.

Table 1. Summary of prototype production costs and quantities.

Prototype, date	PCB Manufacturer	# of manuf. Boards	Fixed Costs (manuf)	Cost per board	Assembler	# of pop. Boards	Fixed Costs (population)	Cost per board
First, May 2003	NCI	6	$700.00	$173.78	UMAI	2	$675.00	$279.75
Second, March 2004	NCI	20	$700.00	$166.18	UMAI	10	$850.00	$171.75

II.2. Hardware Manager Testing and Verification

Following the prototype manufacturing and component population, the Hardware Manager boards were tested and trouble-shooted. This important stage in the prototype development requires the designer to ensure that the board was manufactured to specifications, that all hardware components are correctly wired and working, and that the software modules are functioning as desired.

The first step was to verify that no shortcircuits existed, and that all components were functioning properly. Simple details, such as the polarity of small 1812-package capacitors, can make this verification process difficult. In this subsection, the testing of the different portions of the Hardware Manager is detailed. This includes the communications testing, hex displays, power consumption, sensors, and analog-to-digital converter.

A. Hardware Tests

Testing of the Hardware Manager revealed a few mistakes in the design. None of the mistakes were fatal, and fixing them proved simple. In order to test the current sensor, a test current was supplied from an external power supply. To multiply the measured current, the cable was wrapped around the sensor multiple times. The measured value's eight most significant bits were mapped to the hex displays for verification. The following table illustrates the collected results.

Table 2. Current sensor and ADC test measurements.

Output Current	Measured Current	Secondary current	Vsens (to ADC)	Decimal	Binary	Hex	Test	Check
-5.1	-15.3	-0.00765	-0.3825	-78.336	1110110010	FFFFFFFFB2		
5	15	0.0075	0.375	76.8	1001100	004C	4	ok
5.3	15.9	0.00795	0.3975	81.408	1010001	0051	5	ok
10	30	0.015	0.75	153.6	10011001	0099	9	ok
15	45	0.0225	1.125	230.4	11100110	00E6	0E	ok
13.8	41.4	0.0207	1.035	211.968	11010011	00D3	0D	ok
17.1	51.3	0.02565	1.2825	262.656	100000110	0106	10	ok
-4.9	-14.7	-0.00735	-0.3675	-75.264	1110110101	FFFFFFFFB5	FB	ok
-10	-30	-0.015	-0.75	-153.6	1101100111	FFFFFFFF67	F6	ok
-12	-36	-0.018	-0.9	-184.32	1101001000	FFFFFFFF48	F4	ok
-14.9	-44.7	-0.02235	-1.1175	-228.864	1100011100	FFFFFFFF1C	F1	ok
-17	-51	-0.0255	-1.275	-261.12	1011111011	FFFFFFFEFB	EF	ok

The current sensor gain, which is very important to scale feedback data in closed-loop control mode, are found by the following expression:

$$\frac{1}{K_{isens}} = \frac{1}{2000} \cdot 50 \cdot \frac{2^{12}}{20V} \Rightarrow K_{isens} = 0.1953125$$

The voltage sensor gain is given by the following:

$$K_{vsens} = \frac{1}{80 \cdot 10^3} \cdot \frac{2500}{1000} \cdot 300 \cdot \frac{2^{12}}{20} \Rightarrow K_{vsens} = 0.52083$$

B. Software Tests

The software tests included testing all of the VHDL modules, including analog-to-digital converters, communications, and the modulator. Upon testing the analog-to-digital converter, another mistake was encountered: some of the ADC control signals were cross wired on the board. That, however, was easily solved by changing the definition of the FPGA pins to match the actual routing. The following corrections were applied to the output pin (.pcb) file:

Table 3. Correction to ADC control pin assignments.

Net Name	Original Pin Assignment	Corrected Pin Assignment
AD1_CS_L	P23	P24
AD1_RD_L	P24	P23
AD2_CS_L	M23	M24
AD2_RD_L	M24	M23

II.3. Modulator Design and Evaluation

The modulator is perhaps the most important software function of the PEBB. This module is what links the control command –as a duty cycle reference– to the switch commands. A simple duty cycle reference is used to construct the switching pattern that is used to drive the switches. However, unknown to the application control, it is at this level that many of the non-idealities of the inverter must be resolved. Dead- or blanking-time is applied at this module, as is the compensation strategy for the effects of that very necessary effect. Functionally, to the control layers, the modulator is where the partition is made between the Universal Controller (UC) and the Hardware Manager. In fact, the modulation function is split between the two; for example, in SVM (Space Vector Modulation), actions such as sector identification to vector times calculation is still done in the UC. However, implementation of the phase-leg switching transitions, dead-time, etc, is done in the Hardware Manager.

The design of the modulator begins with a brief analysis of the desired functions to be included in the module, followed by a review of the dead-time compensation algorithm and ending with the software implementation of all of the described functions.

A. Modulator Requirements and Functions

Several functions are required of the modulator block, in order to have a truly generalized half-bridge module. Some of these target requirements are:

- Synchronization to the system (network) clock
- Frequency adjustment
- Carrier edge selection
- Local fault protection
- Dead-time compensation
- Protection against large/small duty commands

These requirements are indeed basic characteristics of a universal power switch module. The most important feature is that of synchronization: this is the defining characteristic of the PEBB modules, that although distributed, all nodes in the system are closely synchronized. Frequency adjustment should be accomplished without reprogramming the FPGA, and possibly on-line, while carrier edge selection could be a useful addition for some converter topologies.

The modulator must contain mechanisms to protect the local power switch in case of fault (over-current, over-temperature, under-voltage) by opening both switches. Additionally, the modulator must be sensitive to very large or very small duty cycle commands. Since some binary arithmetic is involved in the process, extreme commands could provoke a carry, transforming a small number into a very large one.

Dead-time compensation is absolutely necessary for the high performance inverters, and is thus included in the modulator block. The compensation strategy is commented upon in details on the following section. However, it is noted that the option to have this compensation or not should be available to the system controller, and this will thus be an adjustable parameter. The duration and application of dead-time is not adjustable; however, this could be modified should the user deem necessary.

B. Dead-time Compensation

Dead-time is widely known to be the worst inverter non-ideality, affecting drives and other medium- to high-power converters in particular [6]. Dead-time, or blanking-time, is the time applied purposefully in an inverter phase-leg in which neither switch is turned-on (please see Fig. 6-8), in order to prevent fatal shoot-thru faults (Fig. 6-9).

However necessary, the application of dead-time introduces much distortion to the output waveforms, and leads to a drastically reduced output voltage, as shown in the simulation results in Fig. 6-10. The reason for the distortion is the disruption of the converter's volt-second balance. Much work has already been done on the subject, and many proposed solutions achieve very good results. Of the types of compensation existent in literature, there are two distinct types: average compensation techniques, as in [7], which correct the volt-second balance at every fundamental cycle, or real-time compensation techniques, which adjust the commanded voltage at every switching period to reflect the unbalance created by dead-time [8, 9].

Fig. 6-8. Application of dead-time in gate waveforms.

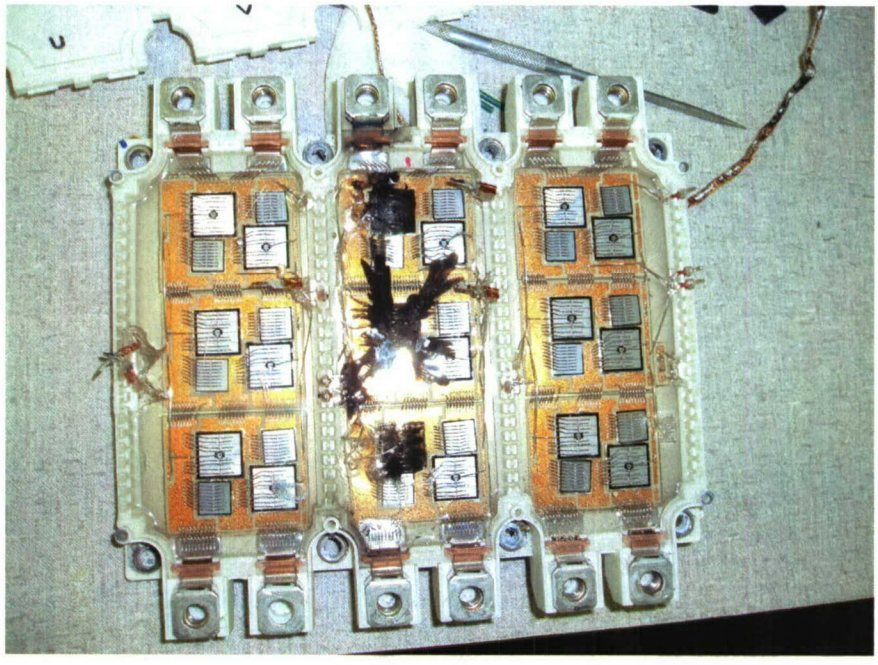


Fig. 6-9. Shoot through fault destroys IGBT module.

Due to the nature of our partitioned converter, a logical choice for dead-time compensation strategy is the real-time, or pulse-based, algorithms. These algorithms can be easily implemented in the Hardware Manager's FPGA, thus reducing the computational workload on the UC's DSP. Additionally, this solidifies our claim that the PEBB is truly an ideal power switch to the upper control layers.

To understand why dead-time introduces such a great distortion to the converter waveforms, it is useful to observe the phase leg current flow during different conditions. Fig. 6-11 to Fig. 6-14, below, show the current paths for all possible situations, before and during the dead-time period.

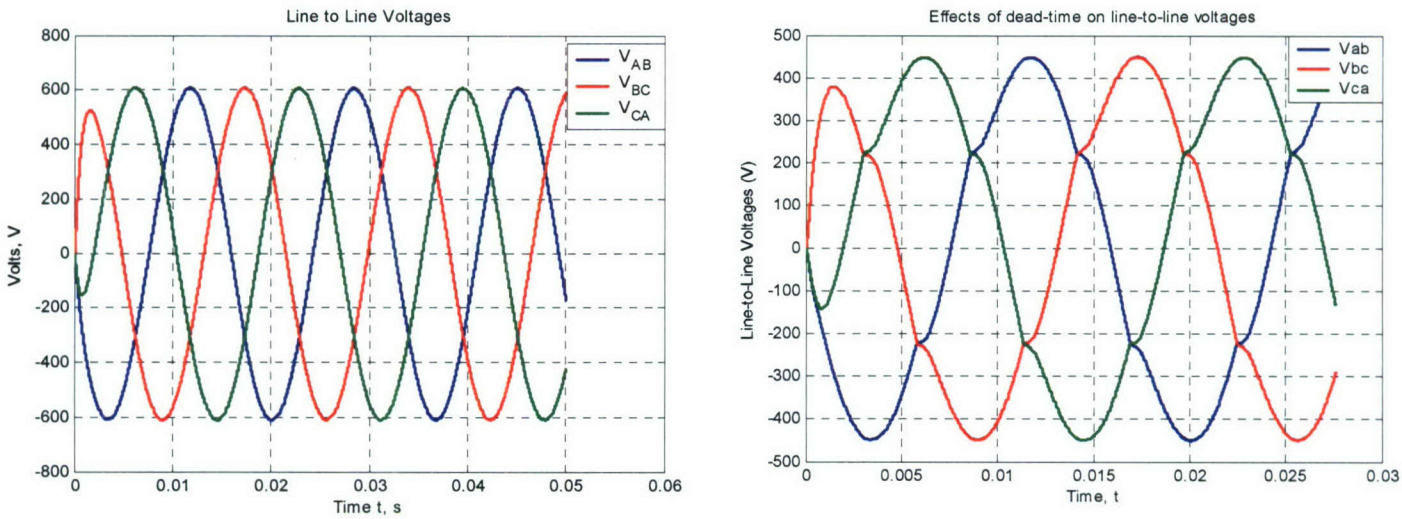


Fig. 6-10. Line-to-line output voltages without (left) and with (right) dead-time.

Taking Fig. 6-11 (first) as an example, we examine the case when the phase current is flowing in the positive direction (defined as out) and the top switch is about to transition to the "on" state. Currently presently flows through the bottom anti-parallel diode (Fig. 6-11 (a)); in an ideal situation, that is, without any dead-time, the top switch would turn-on and immediately start conducting. However, during dead-time application, both switches are held off, and the current free-flows through the bottom diode. This indicates a loss in the volt-second balance operation of the converter.

Fig. 6-14 examines a different case: this time current is negative (flowing in) and the bottom switch is about to transition to the "on" state. Instead of flowing down the bottom switch, as in the ideal case shown by Figure 6 (b), the current keeps flowing up the top anti-parallel diode, thus providing a gain to the volt-second balance. Understanding the different situations enables us to correct the reference quantity (please see Table 4, below) in order to adjust the overall volt-second balance in the converter. The adjustment made in this technique is simply the value of the applied dead-time [8]. However, another algorithm suggests that other factors, such as transistor turn-on and turn-off times, as well as the saturation voltage and the on-voltage of the IGBT and diode, respectively, should be included in the dead-time compensation scheme [9]. While true, the effect of such parameters is both uncertain (as they change depending on the operating point) and minimal.

The ideal versus compensated gate waveforms are shown for the two cases where adjustment is required, in Fig. 6-15, below. Therefore, this compensation technique is solely dependent on the phase-leg's own current, and on the dead-time duration (a fixed, known variable). This technique thus fits very well with the current partitioning of the module control, and is suitable for execution at the Hardware Manager level.

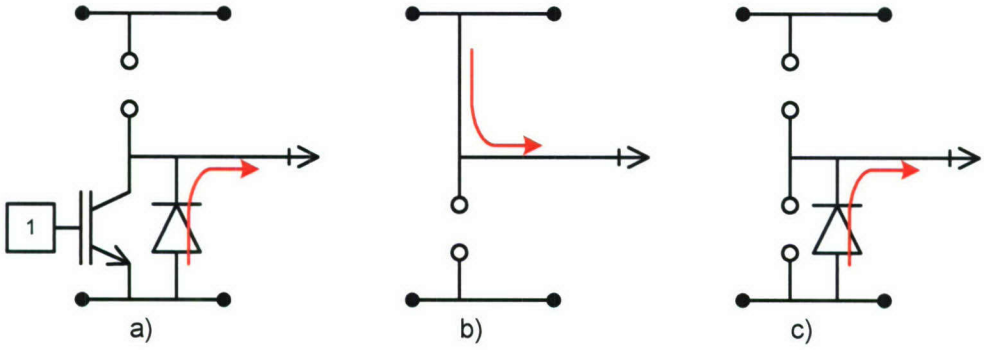


Fig. 6-11. Top switch turn-on, i_ph > 0. (a) State before commutation. (b) Ideal switching. (c) State during dead-time.

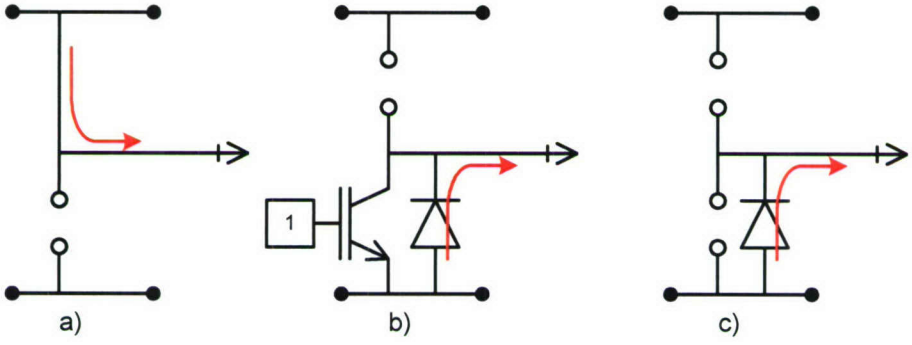


Fig. 6-12. Top switch turn-off, i_ph > 0. (a) State before commutation. (b) Ideal switching. (c) State during dead-time.

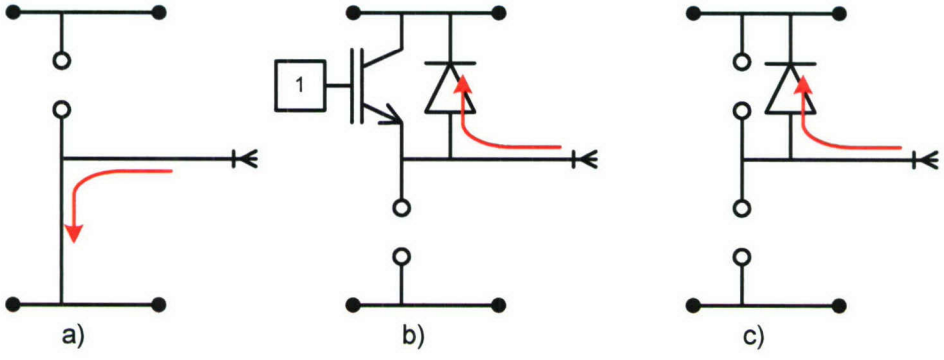


Fig. 6-13. Top switch turn-on, i_ph < 0. (a) State before commutation. (b) Ideal switching. (c) State during dead-time.

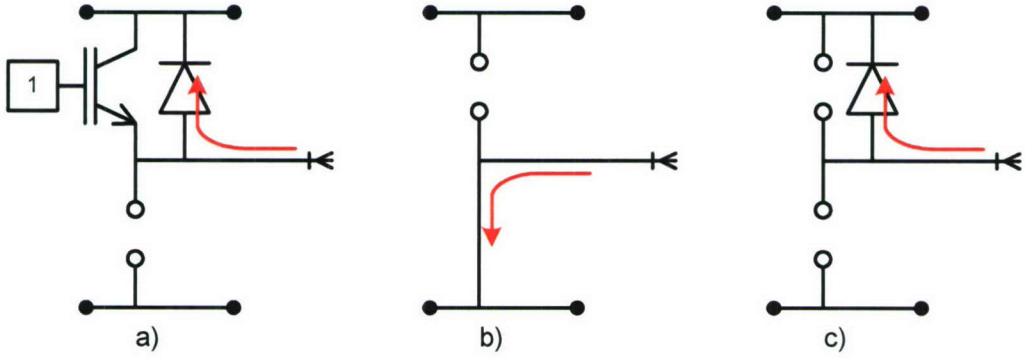


Fig. 6-14. Top switch turn-off, i_ph < 0. (a) State before commutation. (b) Ideal switching. (c) State during dead-time.

Table 4. Correction matrix for dead-time compensation scheme.

Phase current Polarity	*Switch Transition*	*Adjustment*
+ ($i_{phase} > 0$)	Turn-on (off → on)	Subtract DT
	Turn off (on → off)	None
- ($i_{phase} < 0$)	Turn on (off → on)	None
	Turn off (on → off)	Add DT

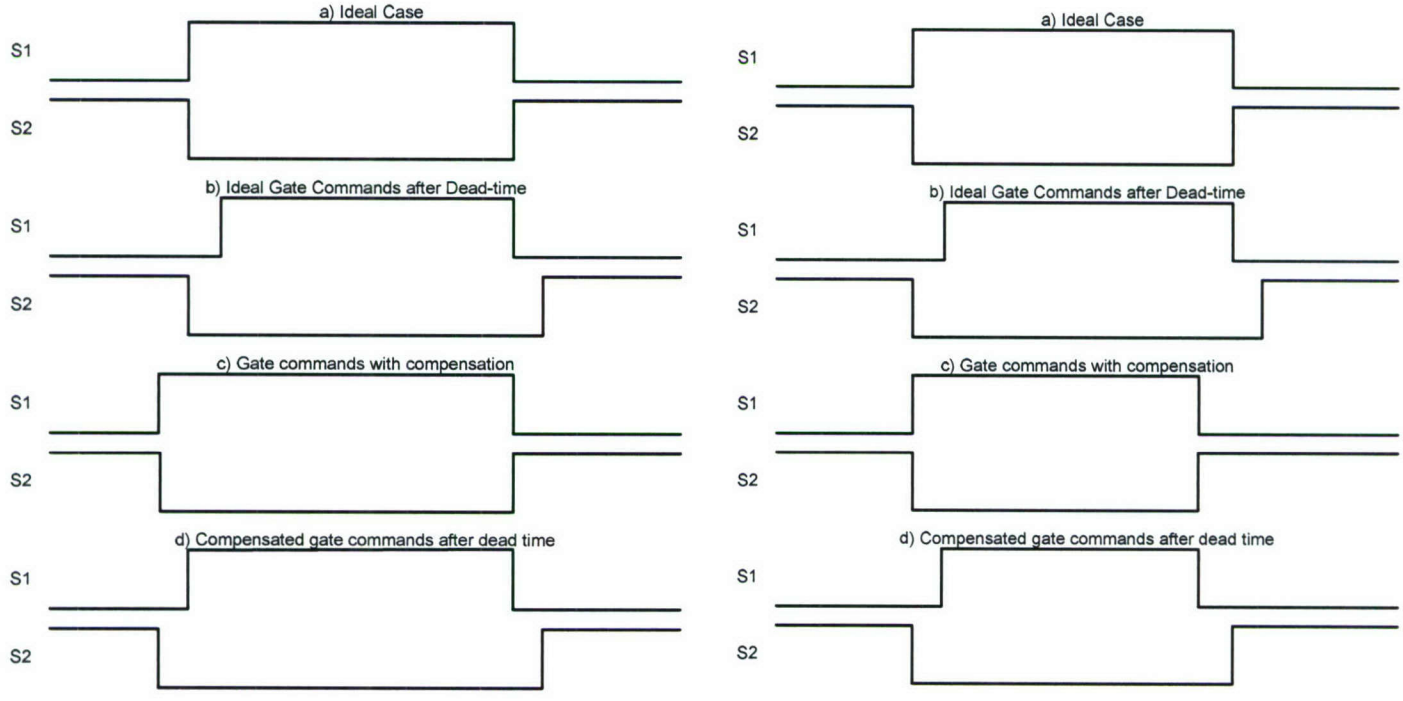


Fig. 6-15. Ideal versus compensated gate command examples for i_phase > 0 (left), and i_phase < 0 (right).

C. Software Implementation

The software implementation of the modulator, as is the case with all Hardware Manager modules, is done in a hardware description language, VHDL. Above all, this ensures that the code is truly portable to other hardware implementations.

The implementation of the modulator may be done in several ways, as shown in literature [10, 11]. However, an important challenge introduced by the particular system at hand is the clock frequency. The DSP 80 MHz frequency dictates the FPGA's internal clock, which must be set to that same frequency. This is also a requirement for the high-speed, real-time communications protocol. These requirements impose tough restrictions on the efficiency of the software modules of the Hardware Manager: all must synthesize at speeds greater than 80 MHz to ensure proper operation. Therefore, the designs here were optimized in order to obtain the highest possible performance. This performance is a combination between device (FPGA) choice, and the VHDL construction. The Virtex FPGA present in the Hardware

Manager is a "big" device among the FPGA families, and has a high speed grade. This facilitates the implementation of the communications protocol and the other functional modules.

Beyond the synthesis frequency, the style of the modulator can be done in different manners. The original design is based on comparators, just as an analog modulator would be built. The performance of this construction has so far been very good; however, it has proven a bit inflexible to change. Under this construction, the switching frequency would be limited to a few – predetermined – discrete values. Additionally, low switching frequencies would have low synthesis speeds.

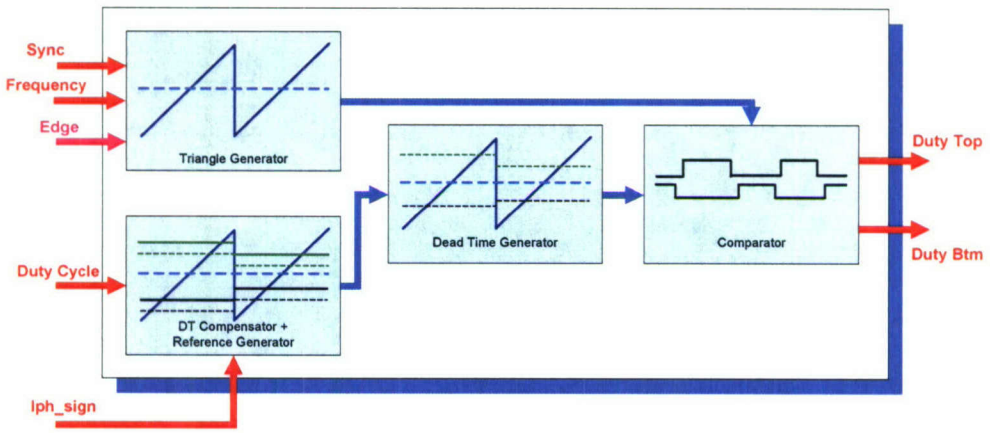


Fig. 6-16. Block diagram of the comparator-based modulator.

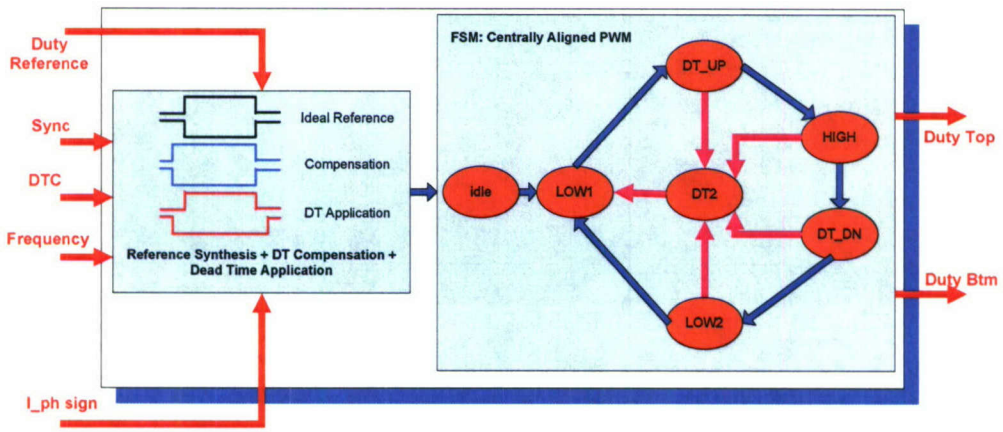


Fig. 6-17. Block diagram of the finite state machine (FSM) modulator.

A second design, based on a finite state-machine (FSM), was also constructed to better tackle some of the requirements imposed on the modulator (as listed above). This design has proven more flexible in meeting all of the requirements, such as a flexible switching frequency choice and ease in clamping the gate signals up or down. Although more flexible, this construction has not been improved to the level of performance of the previous design.

II.4. PEBB Hardware Verification

The PEBB Hardware went through several tests to validate its operation as a truly distributed power converter. As such, there were several aspects to these tests, ranging from the control design and

implementation, to the completion of all software modules in the Hardware Manager. Perhaps the most important factor, however, was the communications protocol.

The communications protocol – which is covered in more detail in Chapter VII of this report – is what ties the PEBB converter together. Without it, the converter is left unsynchronized, and incapable of any advanced operation beyond very simple open-loop operation. Thus the implementation of a successful PESNet was absolutely required for the operation of the PEBB hardware.

This section addresses, in addition, the control design for a 3-Phase VSI (Voltage-Source Inverter), the control implementation in C-code, as well as the modeling of the PEBB-based converter in SABER, and concludes with experimental results.

A. Communications Protocol

The communications protocol is thoroughly described in Chapter VII of this report. The aim of this section is to reiterate the work that was done to adapt the protocol to present working condition. Besides the correction of some bugs in the different data managers (extended, normal), changes included the transformation of the structure of the protocol in order to obtain a shorter digital delay.

Under normal designed operation, the protocol is completely synchronously: upon receipt of a package addressed to it, a node will reply with a prescribed response package. This means that, upon receipt of duty cycle information, a node will reply with its sensor information. However, this implies that the minimum digital delay present in the system is 2 switching cycles. This can be a big burden on the control bandwidth, thus the need to shorten this time.

Under the new, modified operation, each node forms a response packet as soon as the analog-to-digital conversion process is completed, sending the information to the prescribed master node. The conversion still happens synchronously to the network clock at the carrier wave peaks in order to ensure no switching at the sampling time. This alteration results in a much shorter delay of 1 switching cycle.

B. Control Design

For early hardware experimentation stages, the three-phase VSI is a good choice of topology due to the relative ease of control, and its "bucking" nature of operation. Therefore it was selected to be the testbench used for the verification and further development of the PEBB modules and the PEBB-based converter.

The initial control design was a single loop approach, with a synchronous frame current controller. This simple approach allowed the thorough testing of the entire system, from the PESNet communications protocol to the execution of the Hardware Manager functions under closed loop conditions. Testing proceed by verifying the feedback data from the sensors on the Hardware Managers, followed by determining (and reducing) the digital delays introduced partly by the protocol.

The control design is done based on a linearized average model of a VSI; the control laws are used on a synchronous frame (DQ0 coordinates) to facilitate the control. The average model of the VSI is shown below:

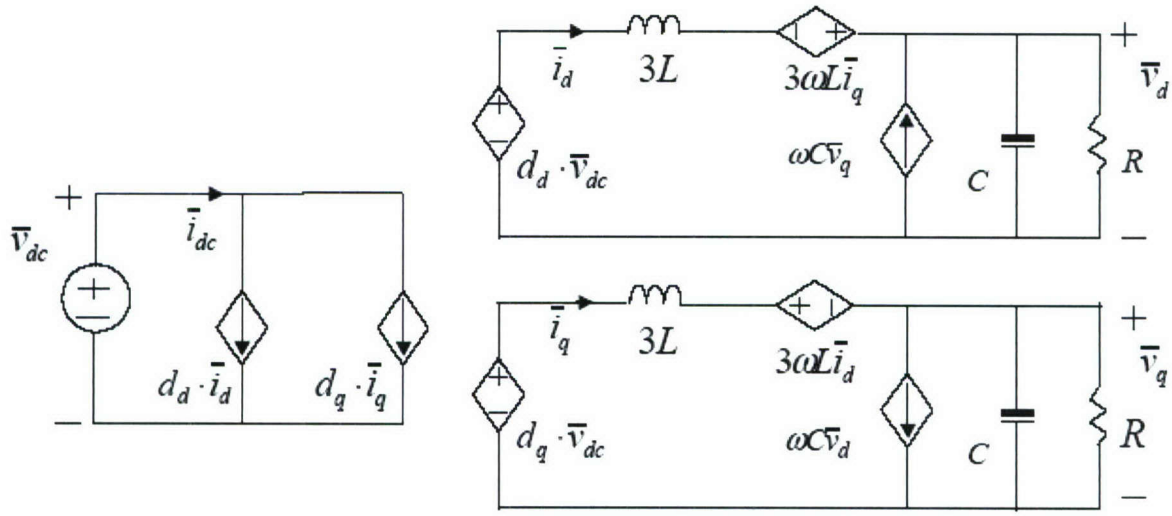


Fig. 6-18. Average DQ model of the VSI.

This model is then linearized about an operating point, and reduced to the following small-signal model:

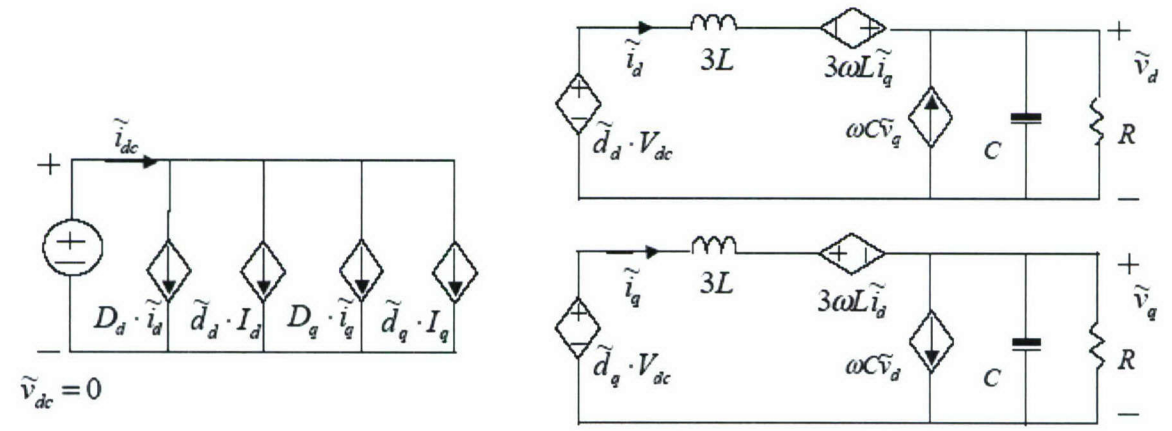


Fig. 6-19. Small-signal model of the VSI.

The following operation of the converter is desired:

$$V_{dc} = 150V, \quad V_m = 50V$$

$$V_d = \sqrt{\frac{3}{2}} \cdot V_m = 61.23V$$

The steady-state operating point was found based on the above selections for the fundamental frequency, dc-link voltage and the desired output voltage by solving the following simultaneous equations:

$$I_d = \frac{V_d}{R} - \omega C V_q \qquad I_q = \frac{V_q}{R} + \omega C V_d$$

$$D_d = \frac{V_d - 3\omega L I_q}{V_{dc}} \qquad D_q = \frac{V_q + 3\omega L I_d}{V_{dc}}$$

Only a d-channel current controller was designed, leaving the q-channel current to move freely. The current controllers were implemented with PI (proportional integral) controllers, designed in MATLAB, and the average model transient performance evaluated in SIMULINK:

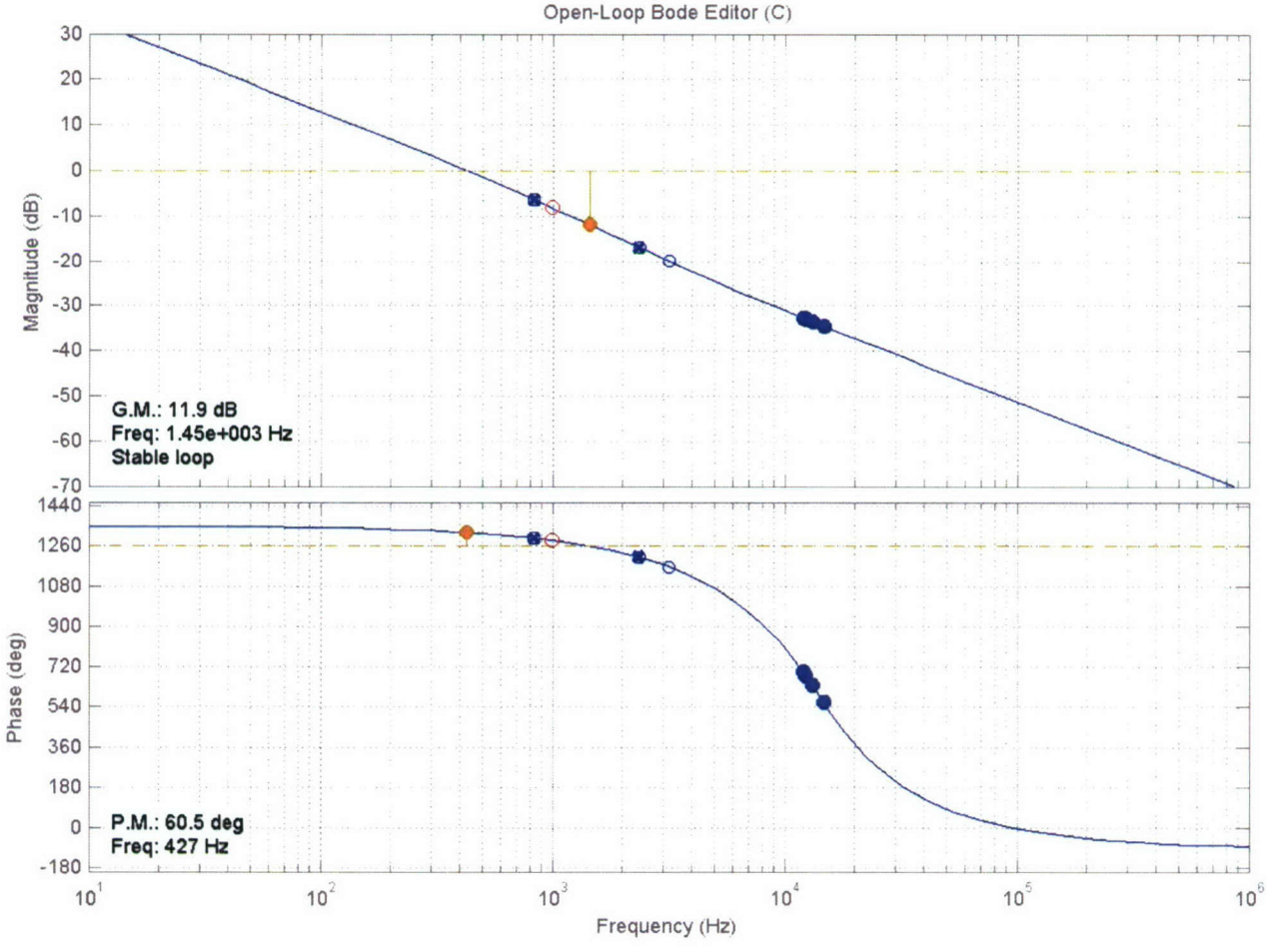


Fig. 6-20. Closed loop gain from d_d to i_d, after addition of current compensator.

The d-channel current controller was of the following type:

$$K_{id}(s) = K_p + \frac{K_i}{s}, \qquad \text{where} \quad K_p = 0.0049, \;\; K_i = 30.8$$

The controller designed above were implemented in C-code using the IDE software by Analog Devices, the manufacturer of the SHARC series DSP present in the UC. Implementing this control law, albeit simple, involves several operations, such as: ABC to DQ0 coordinate transformation, scaling of the feedback data, implementation of the control law, and the transformation to ABC (phase) from DQ0 (line-to-line) coordinates.

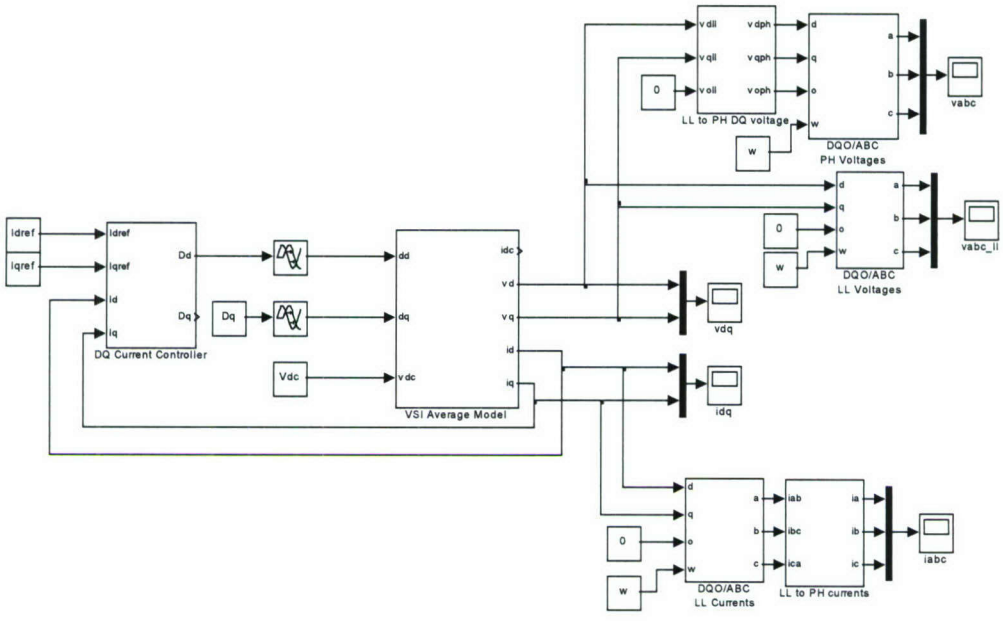


Fig. 6-21. Simulink model used to evaluate controller transient performance.

$$T_{\alpha\beta\psi/abc} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

$$T_{dq/\alpha\beta} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}$$

```
//***************** ABC to DQ transformation ******************
void abc_dq(void)
{
      float x_alpha, x_beta;

      x_alpha = One_Over_SQRT_6*(xa-xb);
      x_beta = SQRT_2_Over_6*(xa+xb)-SQRT_2_Over_3*xc;
```

```
//************* DQ_ln to DQ_ph transformation ******************
void dqln_dqph(void)
{
      float xd_ln, xq_ln;

      xd_ln = xd;
      xq_ln = xq;
```

```
//************** DQ to ABC transformation **************
void dq_abc(void)
{
      fDutyA = SQRT_2_OVER_3 * ( xd*cos_theta - xq*sin_theta );

      fDutyB = SQRT_2_OVER_3 * ( 0.5 * ( -cos_theta*xd + sin_theta*xq ) )
                  + One_Over_SQRT_2 * ( sin_theta*xd + cos_theta*xq );

      fDutyC = SQRT_2_OVER_3 * ( 0.5 * ( -cos_theta*xd + sin_theta*xq ) )
```

```
//********************** PI regulator ************************
void regulator(void)
{
      float xd_err, xq_err;
      float temp1;

      xd_err = Id_ref - xd;
      xq_err = Iq_ref - xq;

//PI regulation
      dd = Kp_Id*xd_err + Ki_Id_over_Fs*xd_err + Id_integ - xq * Three_WL_Over_Vdc;

      if (dd < -dd_ref_lmt) {
            dd = -dd_ref_lmt;
      }
```

C. Modeling of the PEBB

The modeling effort described in Chapter XI of this report was combined with additional modeling of some of the functions implemented in the Hardware Manager in order to obtain a true model of the hardware. This model was used subsequently to verify the control design, and to thoroughly simulate the system before any power experiments.

Of greatest interest was the modeling of the dead-time mechanism, as well as the dead-time compensation algorithm. Additionally important was the inclusion of digital delays, and naturally, the control design described above. The dead-time and dead-time compensation, as well as the digital delays are included in the model below (Fig. 6-22), and were implemented with analog control blocks from the SABER library.

Additionally, the model of the PEBB power stage was included (please see Chapter XI) in order to model the switch and diode non-idealities.

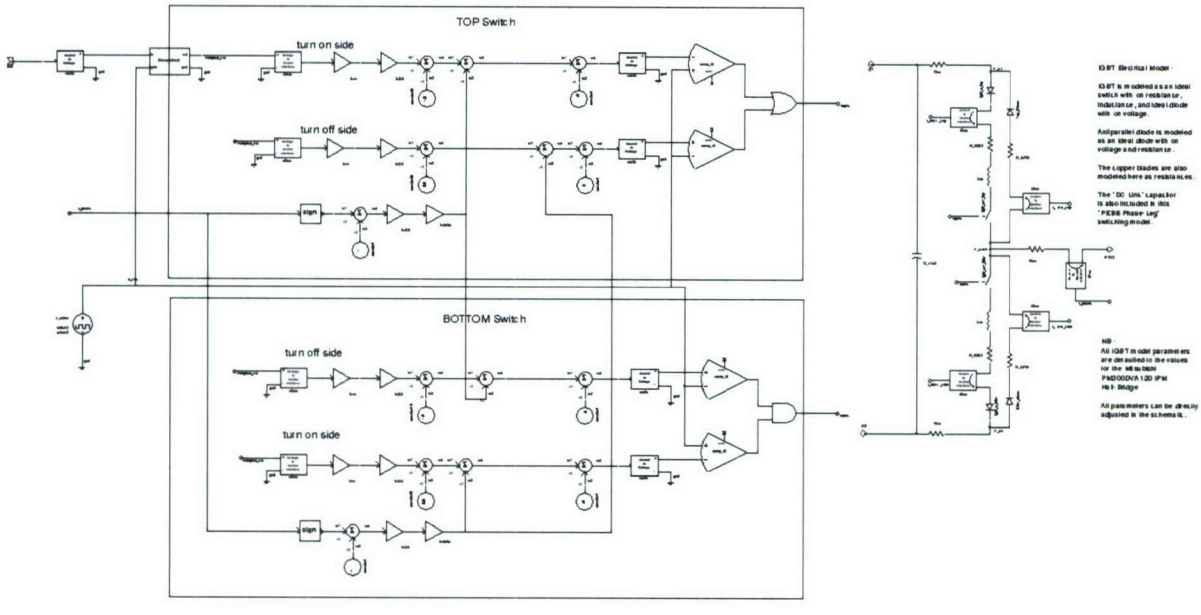


Fig. 6-22. SABER model of the PEBB, including switch non-idealities, and dead-time application and compensation.

D. Simulation of experimental results

The model developed above was used to simulate the performance of the converter at the targeted operating points. The model for the PEBB-based VSI is show in Fig. 6-23. It features three of the building blocks shown above, as well as the functional blocks for the DQ-coordinate transformation, and control and delay blocks.

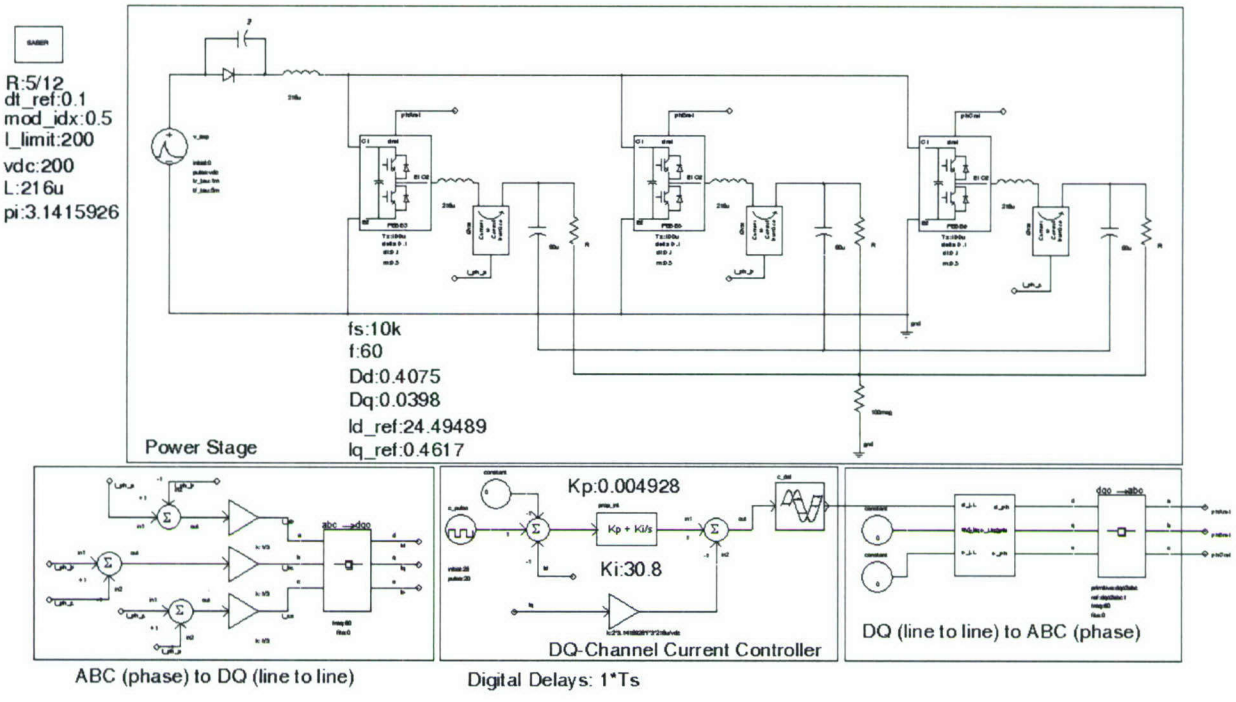


Fig. 6-23. Saber model of PEBB-based voltage source inverter and control

Simulating the switching model above with SABER, the following results were obtained. They signaled that the control design was indeed correct, and was seemingly appropriate.

E. Experimental Results

The experimental testing of the PEBB-based system was done under the following conditions, as verified by simulation:

- Vdc = 150 V
- fs = 10 kHz
- L = 216 uH
- C = 50 uF
- R = 5/6 ohms
- Id_ref = 24.5 A

The dc-link voltage was slowly brought up in open-loop mode, and one the current reached a certain threshold, the loop was closed automatically. Fig. 6-25 shows the operation of the PEBB-based VSI in open-loop mode, while Fig. 6-26 shows the same converter in closed-loop mode. In order to evaluate controller transient performance, the Id current reference was toggled in the DSP, thus producing the waveform shown in Fig. 6-27.

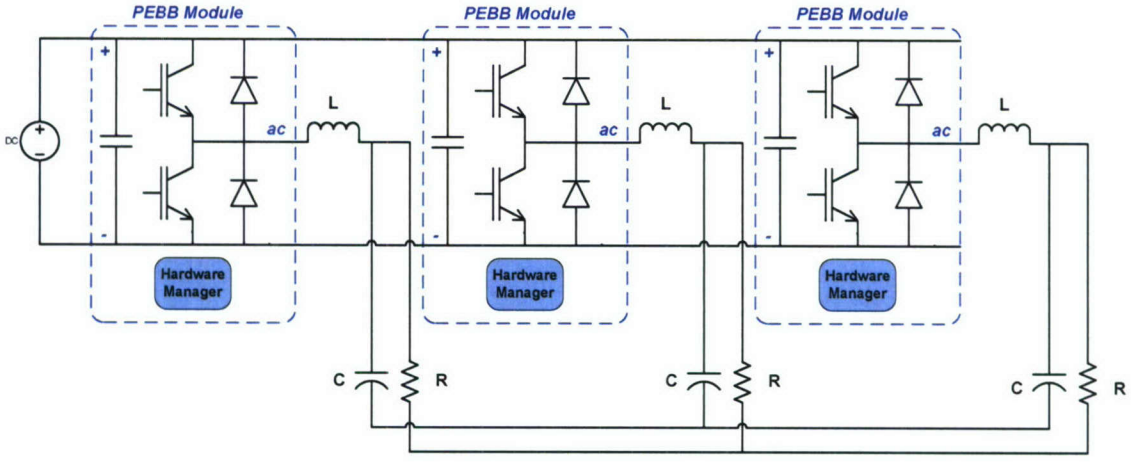


Fig. 6-24. Topology of the PEBB-based VSI used in experimental tests.

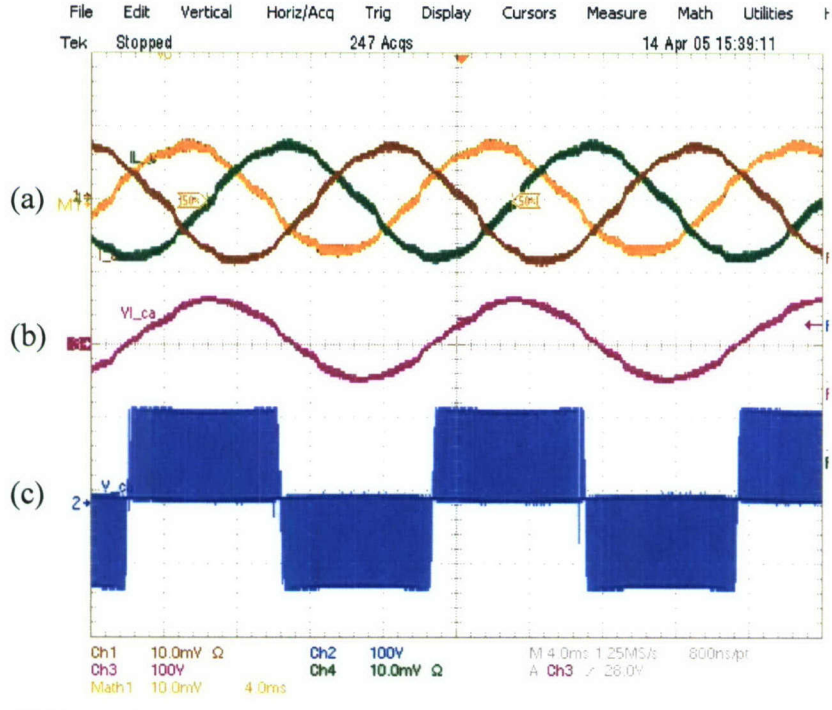


Fig. 6-25. Open loop VSI experimental results. (a) Three phase currents. (b) Load voltage. (c) Line-to-line leg voltage

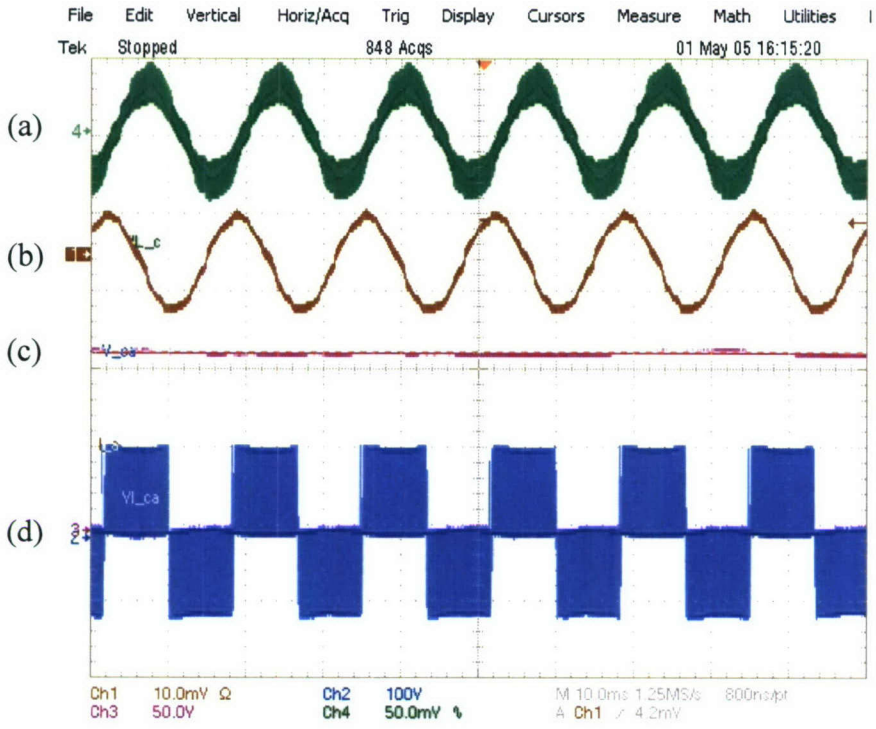


Fig. 6-26. Closed-loop VSI experimental results. (a) Inductor current. (b) Load Current. (c) DC-link voltage. (d) line-to-line leg voltage.

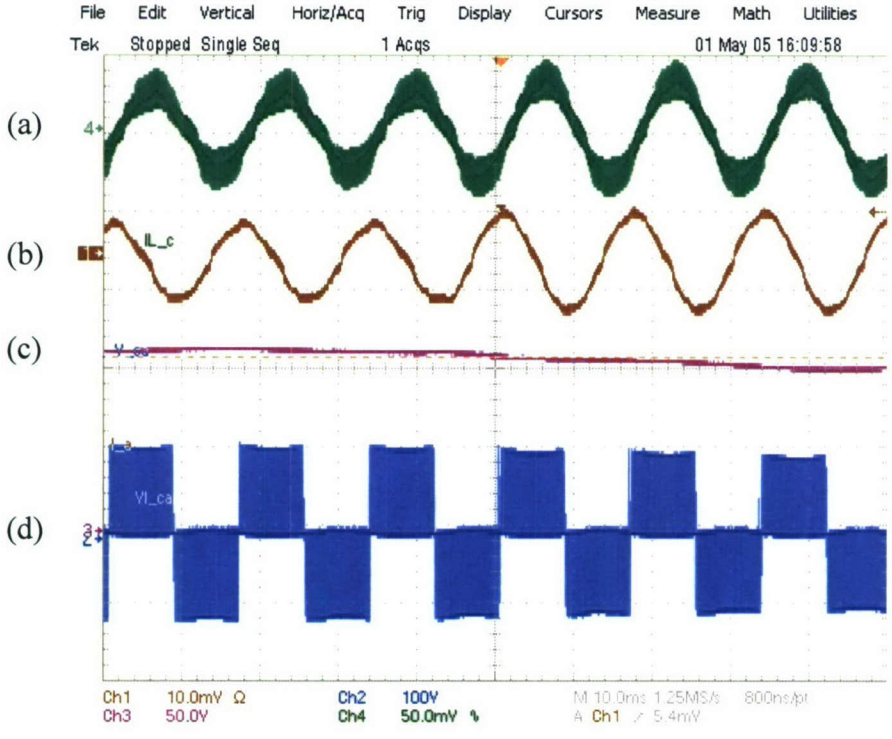


Fig. 6-27. Closed-loop VSI transient experimental results. (a) Inductor current. (b) Load current. (c) DC-link voltage. (d) Line-to-line leg voltage.

F. Additional testing

Two PEBBs were combined to work as a full-bridge (H-bridge) inverter. Fig. 6-29, below, shows one of the resulting waveforms collected from experiments with this topology. This test was run in open-loop mode.

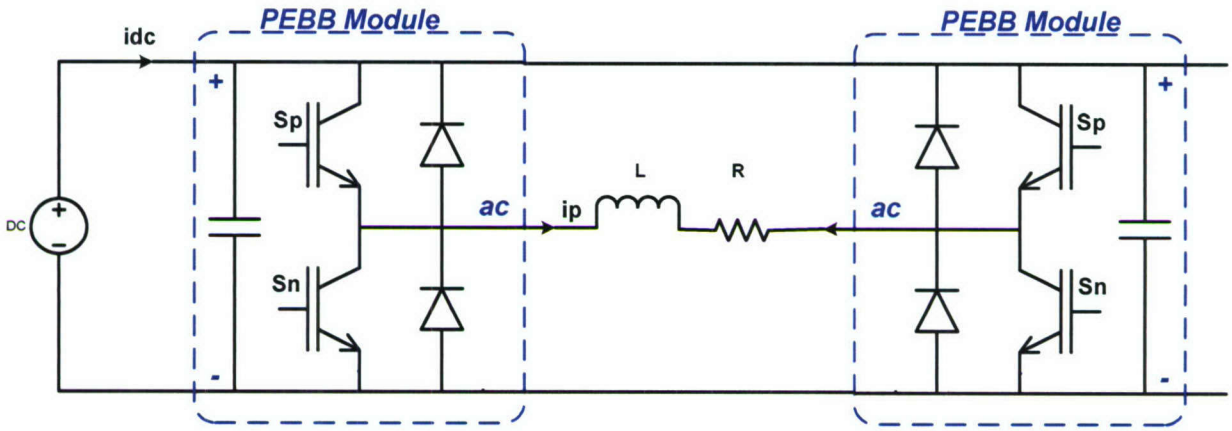


Fig. 6-28. Topology of the PEBB-based, H-bridge inverter.

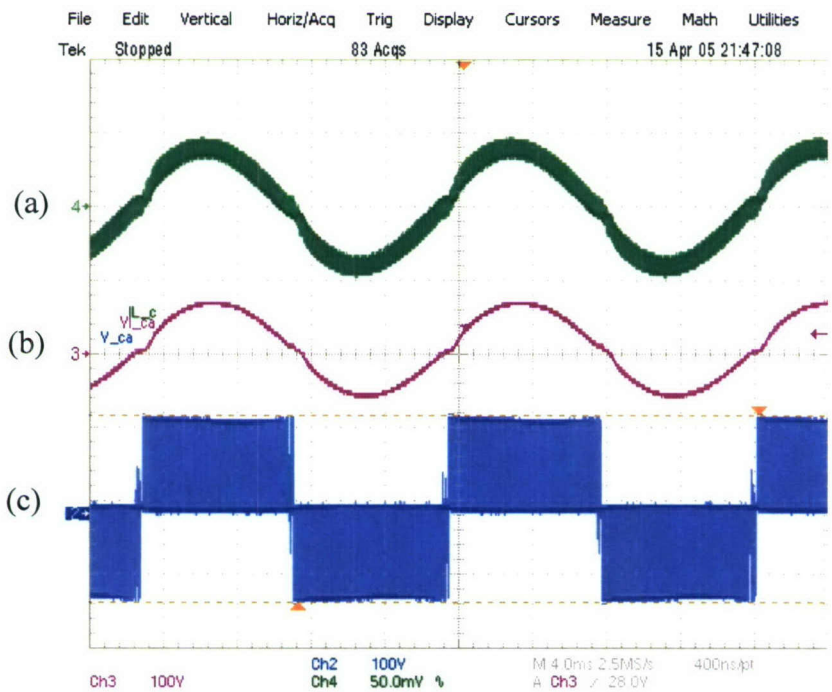


Fig. 6-29. H-bridge experimental test results. (a) Inductor current. (b) Load voltage. (c) Line-to-line voltage.

III. Evaluation

Although the tasks that were necessary to successfully complete this work were large, and the obstacles daunting, the team pulled together to surmount all challenges. The PEBB system is indeed complex,

involving many different parts which must all work and work together. This included the Universal Controller, the Hardware Manager, and the communications protocol.

The test results have been encouraging, and the performance of the PEBB and the PEBB converter has been very good. Furthermore, the concept has been thoroughly verified and proven with a hardware setup. This is indeed encouraging for the progress and distribution of the concept throughout industry and academia.

IV. Conclusion

The PEBB module has been tested and evaluated as a PEBB-based converter. The hardware is currently in working condition, and will be very useful for a plentitude of future studies. This will hopefully demonstrate once again the power and flexibility of the concept. With applications to distributed generation, motor drives, and advanced control of topologies, the value of the concept and the study will increase even more. Furthermore, due to the partitioned architecture, there are many unexplored issues and also room for improvement or change.

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Chapter 7 PESNET COMMUNICATIONS PROTOCOL FOR PEBB-BASED POWER ELECTRONICS CONVERSION SYSTEMS

I. Introduction

In medium to high power electronics systems, modularization and open system architecture are more and more announced. The PEBB research aims at developing a wide range of power electronics applications from multi-functional and universal hardware and software building blocks to increase production volume and reduce system redesign efforts and maintenance cost. Thus, the so-called "plug and play" can be implemented in power electronics systems, in analogy to that in the computer industry. In PEBB systems, control architecture tends to be distributed, which requires communication networks. Some features of power electronics systems, such as hard real-time, life-critical, etc., impose severe considerations in the design of digital communication networks, which should provide efficient information interchange and system protection mechanisms. For instance, EMI immunity is taken as an important consideration to perform the design of the network topology, since communications most likely are carried out in rather noisy environments.

PESNet has been designed for digital communication in power electronics control systems. We present in this chapter the extended and improved design of the basic network peer-to-peer data communication protocol based on the previously developed version of PESNet. In order to implement "plug and play", the multi-functional and universal PEBB modules must be correctly configured according to requirements of a specific application during the system startup time. Thus, a configuration protocol is necessary to provide system level parameters negotiation among nodes in the network and configuration of each node. Another issue that will be discussed is data synchronization, as delay introduced by digital communication is inevitable. Thus, the synchronization of distributed modules becomes critical, and especially so for power electronics applications. Accordingly, the synchronization mechanism introduced in PESNet supports extremely fast synchronization at phase-leg or PEBB level.

II. Protocol Specifications

The PESNet communications protocols discussed in the document that specify the lowest four layers in the ISO OSI reference mode: physical layer protocol (PLP), link layer protocol (LLP), network layer protocol (NLP) and application layer (AP), as shown in Fig. 7.1.

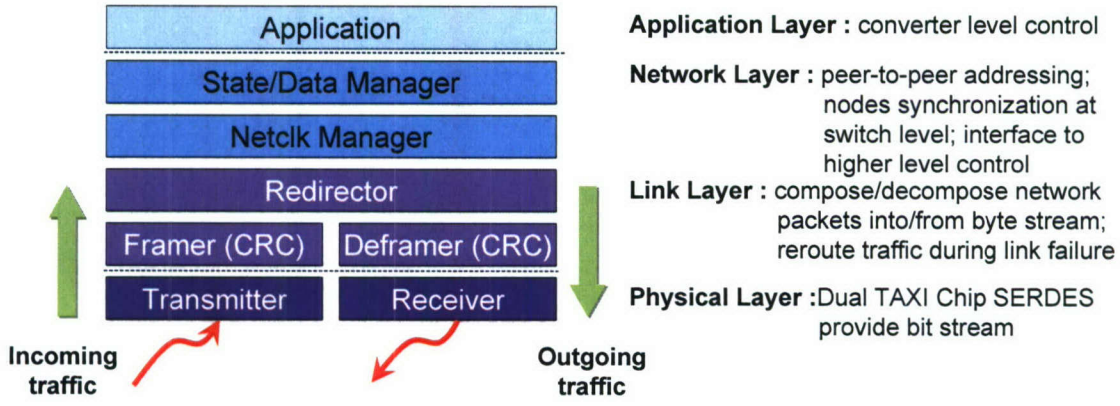


Fig. 7-1. PESNet II protocols stack.

PLP specification defines the characteristics of the transmission medium, such as fiber-optic links, optical connectors and other components, frequency, power levels, and bit level encoding/decoding mechanisms.

LLP specification defines how to access the medium and make upper layer protocols independent of the physical layer, such as data frame format, addressing, error detection and correction, media configuration, node initialization, insertion and removal, and fault isolation and recovery.

NLP specification defines communication between a pair of a source and a destination, such as packet format, and routing methods.

III. Physical Layer Protocol

At the physical layer, 125Mbps optic fiber is used to achieve high transmission throughput and EMI immunity. The transceivers are Cypress CY7C9689-AC Hotlink transceivers. The transceivers take a single character from the FPGA and convert it into a serial stream to be transmitted to the next node on the network. There are two types of characters. One is a command character, and the other is a data character. These characters are encoded using 4B/5B encoding prior to transmission, which takes four bits and converts it to five bits. After the character is encoded, it is serialized. The transceiver uses NRZI (non-return to zero, inverted) encoding to transmit the clock and the data using the same signal. This signal leaves the TAXI chip via a differential PECL (pseudo emitter coupled logic) pair that connects to the optical transmitter. The optical transceiver converts the differential signal to a 650nm optical signal at a bit rate of 125 Mbps. The fiber used to transmit the signal is 1 mm plastic optical fiber. The receiver converts the optical signal back to a differential PECL signal, where it enters the transceiver of the next node. The transceiver recovers the clock and data from the NRZI signal, deserializes the stream, decodes the character, and places it on the parallel interface that leads to the FPGA on that node. If there was an error in transmission, the transceiver will not be able to decode the character, and will indicate this to the FPGA.

One consideration in PESNet design is open network architecture. In this document, only ring type optic network will be discussed. As it will be shown further, the single ring protocols are designed as a subset of dual ring protocols. If there is one node in the network that can only support single ring, the whole network will be configured as single ring structure. If every node in the network supports dual ring connection, the network has the option to be configured as dual ring structure. Compared to single ring structure, dual ring network can be designed to tolerate a single network failure. Single only has a primary ring, while dual ring has a primary ring and secondary ring. If a network is configured as a dual ring,

during normal operation, only the primary carries data packets, and the secondary is in idle. When a failure occurs along the network, the secondary will be used to reroute the ongoing data packets to their destinations.

IV. Link Layer and Network Layer Protocol

IV.1. Ring Structure

The network discussed in the document supports single network connection. The network structure and components are shown in Fig. 7-2. A master node is often a universal controller, which is able to configure the network and application, and send out control information to other nodes. A slave node is typically a hardware manager and the hardware module it controls, which is an agent for a hardware module in the network and is able to handle network data transmission. The basic functionality of PESNet 2.2 is data transfer for control of distributed power hardware. This requires that PESNet 2.2 be able to transport switch control commands from UC to HMs, and transport sensing data acquired at each HMs back to UC. All these actions may be periodic and may require synchronization between actions. To achieve the real-time control and synchronization between distributed power hardware, a net clock is maintained at every node, with the value (net time) comply to that of the net clock at a node called net clock master, of which the mechanism will be explained in detail later. Another basic functionality of the PESNet 2.2 protocol is to support startup configuration of network nodes to setup or negotiate application specific parameters among network nodes.

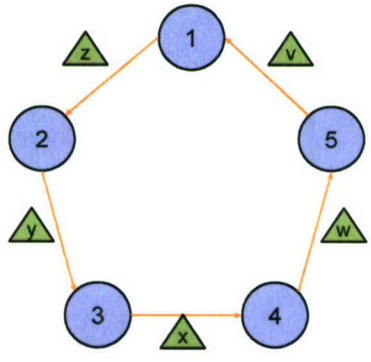


Fig. 7-2 Network layer structure and components.

V. Data Packets

Along the network, every node has to send a packet has to send out a packet every packet clock. If a node does not have useful packet to send out, it should also send out an empty packet instead.

V.1. General Data Packet Format

A general data packet format is shown in Table 1. It contains 7 fields.

Table 1.Packet Size and Breakdown by Mode

	JK SYNC	CMD*	DEST ADDR	SRC ADDR	NET TIME	FLT ADDR	DATA PLD	EDC
Full Mode	8 Bits	4 Bits	8 Bits	8 Bits	8 Bits	8 Bits	10 Bytes	8 Bits
Reduced Mode	8 Bits	4 Bits	6 Bits	6Bits	6 Bits	6 Bits	4 Bytes	8 Bits

* The total size is the size of the useful data. There are two more bytes sent of JK characters used for processing data

** The 4 Bit command is still encoded as though it was 8 bits

The definition for each field is shown in Table 2.

Table 2. Packet Field Descriptions

Field	Description
JK SYNC	Two JK Characters used to restore byte alignment if it has been lost prior to receiving packet
CMD	The command describes the packet type. The nature of a command byte is such that it also indicates the beginning of a packet, as it is encoded differently that normal data
DEST ADDR	The network address of the destination node of the packet. 0xFF is reserved for broadcast address
SRC ADDR	The network address of the source node of the packet
NET TIME	The net time when the packet arrives at the next node.
FAULT ADDR	The address of a faulted node. Zero if no node is faulted.
DATA PLD	The data content of the packet. The format of this array depends on the command.
EDC	Error detection and correction.

One benefit of PESNet 2.2 is that the packet size can be set at startup configuration. One would use a smaller packet if there were more nodes that need to be controlled, and it is acceptable to use less information to control each node. Otherwise, one would use a larger packet size if there were fewer nodes. The reduced packet size allows more packets to be sent and received within a shorter amount of time, which is useful for higher switching frequencies. The tradeoff is the amount of data sent to each device, as well as the maximum size of the addresses, and network clock. Under the full mode, the size of the packet is 16 bytes. Under the reduced mode, the size of the packet has been reduced to 9 bytes. Since only full mode packet was tested. This report wil only consider full mode in the rest of the content.

V.2. Data Packet Types

In order to determine what data the node should support, it is important to look at the applications that this version of PESNet should support. While PESNet 1.1 was focused primarily on the steady state operation of a single converter, PESNet 2.2 tries to extend this to consider configuration, startup, failures, shutdown, and reconfiguration. But most basic operations of PESNet 2.2 startup configuration and data transfer for power converter control.

There are events that occur during these other states that must be supported, some of which also have a requirement to be synchronized. Other objectives, such as plug and play support require information to be set and read by the slaves for configuration purposes. This information has no relationship to time. Examples of this information would be a manufacturer ID that would describe who manufactured the PEBB, or a revision number. There are always unexpected events, such as failures, limit crossings, or emergency shutdowns. All of these types of data must be handled by the protocol.

PESNet 2.2 has four types of information that can be transmitted on the network. Corresponding commands indicate the type of data that is represented in the data array within the packet. These data types are listed below:

- Normal data
- Synchronous data
- Asynchronous data
- Events

The data type is defined by the **CMD** field in a packet. Since **CMD** is a 4-bit field, up to 16 commands can be defined. This report will focus on the basic data types that have been debugged and tested, which are listed in Table 3.

Table 3. PESNet 2.2 commands.

Command Name	Pattern	Description
NORMAL	0001	Set the normal data and reply with the normal sensor data
SET_ASYNC	0011	Set a node's asynchronous attributes
NULL	0110	Specifies an empty packet
EXTENDED	0111	Set some configuration parameters

A. NORMAL Packet

NORMAL packet is data that is transferred periodically, typically used for information exchanged every switching cycle in PWM converter control. This information can be a duty cycle related command for a phase leg from UC sent to a HM, or can be a sensing data from a HM back to UC. NORMAL is specially designed for real-time control.

The general format of the DATA PLD field for a NORMAL packet is shown in Fig.7.3 (a). DIR is the field that indicates the packet transfer direction: "0" means UC → HM, and "1" means HM→UC. Byte 1-

9 will have different definitions for use of duty cycle or sensing data. As shown in Fig.7.3 (b), if a NORMAL packet is used to send a duty cycle to a HM, byte 1 will be used to indicate the scheduled net time that the duty cycle information specified in byte 2-3 will start to take effect. Byte 4-5 is switching frequency information that will be used by the modulator in the HM. When a NORMAL packet is used for sensing data, with the format shown in Fig.7.3(c), byte 1 is the net time that this packet is formed. Byte 2-3 is reading of current senor (after ADC value) at the HM. Byte 4-5 indicates the current related status of the power module. Similar to the byte 6-9 are used for the voltage sensor.

	0	1	2	3	4	5	6	7	8	9
Full Mode	DIR	TIME	DATA1		DATA2		DATA3		DATA4	

(a) General format of DATA PLD field of NORMAL packet.

	0	1	2	3	4	5	6	7	8	9
Full Mode	0x00	SCHD TIME	Duty Cycle		Switching Frequency		*(Unused)*			

(b) Format of DATA PLD field of NORMAL packet used for duty cycle.

	0	1	2	3	4	5	6	7	8	9
Full Mode	0x01	CUR TIME	Current Sensor Reading		Current Faults		Voltage Senor Reading		Voltage Faults	

(c) Format of DATA PLD field of NORMAL packet used for sensing data.

Fig. 7-3. Data payload format of NORMAL packet.

B. SET_ASYNC Packet

Asynchronous data is data that does not depend on the value of the network clock. As soon as a packet arrives at the node with asynchronous data, that data immediately becomes active. The data is called asynchronous because the time when the data becomes valid cannot be synchronized with any other node. SET_ASYNC is mainly used for network startup configuration. Normally SET_ASYNC packets are sent from UC to HMs. The format of SET_ASYNC packet is shown in Fig. 7-4. ATTR is the name a attribute and VALUE is the value to be set.

	0	1	2	3	4	5	6	7	8	9
Full Mode	RESERVED	ATTR1	VALUE1		ATTR2	VALUE2		ATTR3	VALUE3	

Fig. 7-4. Data payload format of SET_ASYNC packet.

The asynchronous data array that has been defined so far is the following:

```
ASYNC_DATA_IN(0) <= ASYNC_DATA_DIR; -- '1' from packet, '0' from device
ASYNC_DATA_IN(1) <= X"00"& ID; -- slot ID
ASYNC_DATA_IN(2) <= OPEN_LOOP_MODE_INDEX &
CLOSED_LOOP_NETCLK & "0" & PKT_ALIGNMENT & "000" & PKT_LENGTH;
ASYNC_DATA_IN(3) <= X"1"& AD1_A1;
ASYNC_DATA_IN(4) <= X"2" & AD1_A2;
ASYNC_DATA_IN(5) <= HEXVAL & X"05";
ASYNC_DATA_IN(6) <= X"0006";        --line contactor status word
ASYNC_DATA_IN(7) <= X"0007";        --
ASYNC_DATA_IN(8) <= X"0008";        --position code
ASYNC_DATA_IN(9) <= X"0009";        --device temperature
ASYNC_DATA_IN(10) <= X"000A";       --master address
ASYNC_DATA_IN(11) <= X"000B";       --device class
ASYNC_DATA_IN(12) <= X"1012";       --hardware id
ASYNC_DATA_IN(13) <= X"0001";       --manuf id
ASYNC_DATA_IN(14) <= X"000E";       --hw revision
ASYNC_DATA_IN(15) <= X"0100";       --fw revision
```

Fig. 7-5. Asynchronous Attributes Definition.

C. NULL Packet

NULL packet is an empty packet with no meaning. It provides a space for a new packet to be placed on the network. The data payload format of NULL packet is shown in Fig. 7-6.

	0	1	2	3	4	5	6	7	8	9
Full Mode	Zeros									

Fig. 7-6. Data payload format of NULL packet.

D. EXTENDED Packet

The NS_EXTENDED packet is for extending **CMD** field, such as set network address, set network clock, etc. The general format of NS_EXTENDED is shown in Fig. 7-7. EXT_CMD defines an extended command. DATA1 specify the value.

	0	1	2	3	4	5	6	7	8	9
Full Mode	EXT_CMD	DATA1	*(Unused)*							

Fig. 7-7. Data payload format of EXTENDED packet.

The extended commands defined so far are listed in Table 4.

Table 4. Extended commands.

Extended Command Name	Pattern	Description
EX_CMD_SETCLK	0x11	Set the local network clock
EX_CMD_SETADDR	0x22	Set network address
EX_CMD_MSTADDR	0x23	Copy master node address
EX_CMD_SYS_RST	0x99	Reset

VI. Network Operations

VI.1. Network Configuration

Before nodes could perform normal network operations, network configuration is necessary. This configuration is done by the master node, which is normally the universal controller (UC). If there are multiple master nodes in the network, only one would be selected as configuration master. The configuration mainly includes:

- Set data packet length;
- Assign node addresses;
- Adjust time discrepancy between transmission clock and receiver clock.

VI.2. Synchronization between Network Nodes

Restrict synchronization are necessary between PEBBs in voltage-fed converter systems. However, for the ring structure, there is no natural synchronization between network nodes. A network clock mechanism is designed so that all the nodes in the network can be synchronized at us level with around 80ns jitter, which should be sufficient for switching power applications up to 50kHz. The synchronization is illustrated in Fig. 7-8.

For every node, a packet is received and sent out per 2us. Even if a node does not have data packet to send out, it will pad the network with a NULL packet. And every node keeps a so-called network clock (NETCLK) which is synchronized to the packet sending. So every 2us when a packet sent out, the NETCLK should also get incremented. Every node also maintains a packet receiving clock, which is started by the arrival of a packet at the transmitter. From the sending of a packet at one node until the sending of a packet at the next node, the time elapsed is set to be 2us. By pre-adjust the delay between packet sending clock and packet receiving clock, it is possible to adjust all the nodes to send packet at roughly the same time. The jitter is caused by a higher resolution bit stream clock of TAXI chipset, and is around 80ns.

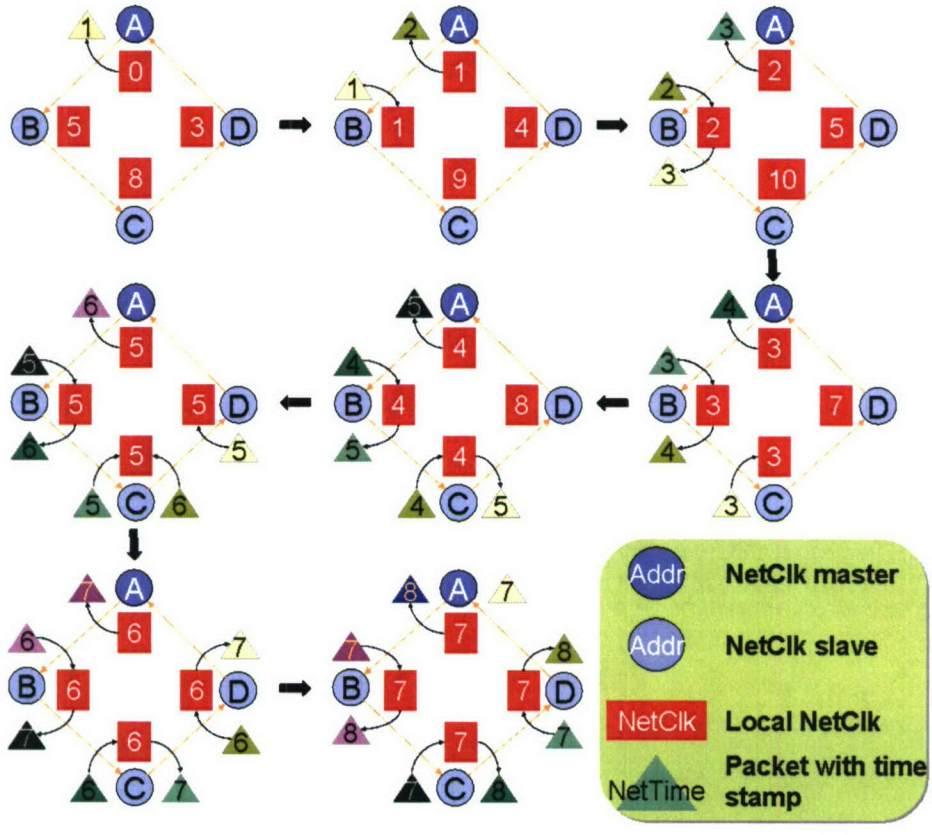


Fig. 7-8. Synchronization mechanism in PESNet II.

If NETCLK is set to be increment with the packet sending, the increment action of NETCLK at different nodes can be synchronized. The problem left is how to adjust the value of NETCLK at every node, so that they have the same clock value. For this purpose, one and only one node in the network is selected as a NETCLK master, which starts it NETCLK with an arbitrary value, and then increment NETCLK every time it sends out a packet. For the rest nodes in the network, they will adjust its own NETCLK to the value in a packet sent from the NETCLK master. Thus, all the nodes can have the same NETCLK value. For operations taken by different nodes but need to be synchronized, the sender of these operations specifies the schedule net time for these operations to be fired. When a node receives such a packet for a time stamped operation, it will fire the operation when its own NETCLK reaches the schedule time.

VI.3. Normal Operations

After network configuration and net clock adjustment and synchronization, every node in the ring is ready to perform normal operations. The most important point is to keep the network clocks synchronized every node has to send a packet every packet clock. If a node does not have any data to send out, it should send out a NS_NULL packet.

VII. FPGA Implementation of Link Layer and Network Layer

The link layer and network layer protocols are mainly implementation in a Xilinx FPGA. The function block diagram is shown in Fig. 7-9. These layers are responsible for:

- Composing/decomposing the packet

- Checking the integrity of the packet
- Managing the network clock
- Filtering commands
- Redirecting packets during faults
- Adding and removing packets from the network and replacing them with NULL packets if necessary
- Implementing attributes
- Implementing simple DSP interface

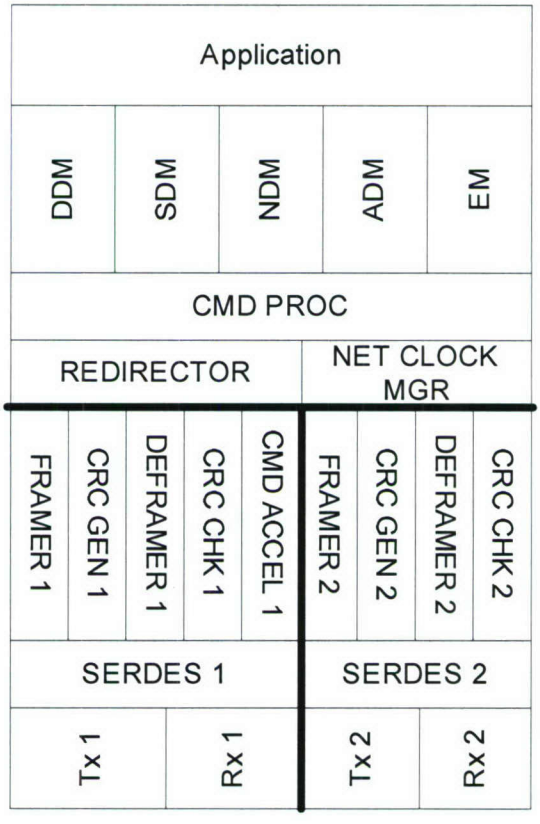


Fig. 7-9. FPGA implementation of link layer and network layer protocols.

For data transmission, the data flow is shown in Fig. 7-10.

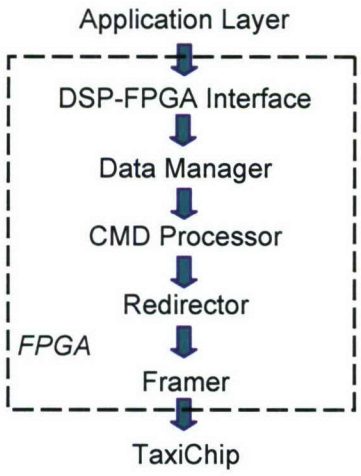


Fig. 7-10. Data flow of transmission.

Data will start from the application layer. For the UC, data will go through the DSP-FPGA interface; otherwise, for HMs, the data will directly go to a data manager. The data will be processed by a data manager according to the data packet type. The purpose of data manager is to form a data frame from application to the format of network layer. If it is a NORMAL data, then it will be processed by Normal Data Manager (NDM); and if it is EXTENDED data, it will be processed by the Extended Data Manager (EDM). The origination of a NULL packet is a little bit different. The CMD Processor is responsible for inserting a NULL packet to the traffic if necessary. The core role of CMD processor is to decide which packet goes to the lower layer if multiple data packets are ready from data managers. The typical handshaking signals between a data manager and the CMD processor is shown in Fig. 7-11. When a data manager has a data packet ready, it will assert the BLOCK_PKT_RDY signal to inform CMD processor. When this packet gets accepted by CMD processor to send out, the CMD processor will inform the origin data manager of this packet that this packet has been processed, which also means that the origin data manager can pass new data packet to the CMD. Otherwise, this data manager has to wait. Each data manager maintains a state machine for cooperating with CMD processor. Fig. 7-12 shows the state machine in normal data manager. Then the data packet will be passed to the redirector, which will direct the packet to the Framer, which is responsible for insert necessary JK characters to the beginning of a packet and sending the content of the packet to the transmitter byte by byte.

It should be pointed out, that for NORMAL packet handling, at UC side it is performed by Direct Data Manager (DDM), and at HM side it is performed by NDM.

```
-- From this data manager to CMD processor to indicate whether a data packet is ready
for sending out. '1' means ready.
BLOCK_PKT_RDY: out std_logic;

-- From CMD process to this data manager to indicate whether a data packet has been
processed. '0' means yes.
BLOCK_PKT_CLR: in std_logic;
```

Fig. 7-11. Handshaking signals between a data manager and CMD processor.

```
process( STATE, BLOCK_PKT_GOOD, BLOCK_DATA_IN, CMD_NORMAL,
BLOCK_PKT_CLR ) is
begin
        case( STATE ) is
        when idle =>
                BLOCK_PKT_RDY <= '0';
                --wait for a normal packet that is destined for this node
                --if( BLOCK_PKT_GOOD = '1' and BLOCK_DATA_IN(1)(0) = '0' and
CMD_NORMAL = '1') then
                if( PKT_RDY_X2 = '1' and PKT_RDY_X1 = '0' ) then
                        NEXT_STATE <= ready;
                else
                        NEXT_STATE <= idle;
                end if;
        when ready =>
                BLOCK_PKT_RDY <= '1';
                --wait for clr to go high, indicating packet is absorbed
                if( BLOCK_PKT_CLR = '1' ) then
                        NEXT_STATE <= waitclr;
                else
                        NEXT_STATE <= ready;
                end if;
```

```
        when waitclr =>
                BLOCK_PKT_RDY <= '0';
                --wait for clear to fall back to 0 and for the packet to end
                --wait for block_pkt_clr to fall to prevent re-entry
                if( BLOCK_PKT_CLR = '0' and BLOCK_PKT_GOOD = '0') then
                        NEXT_STATE <= idle;
                else
                        NEXT_STATE <= waitclr;
                end if;
        when others =>
                BLOCK_PKT_RDY <= '0';
                NEXT_STATE <= idle;
        end case;
end process;
```

Fig. 7-12. State machine in NORMAL data manager.

For data receiving, Fig. 7-13 shows the data flow direction.

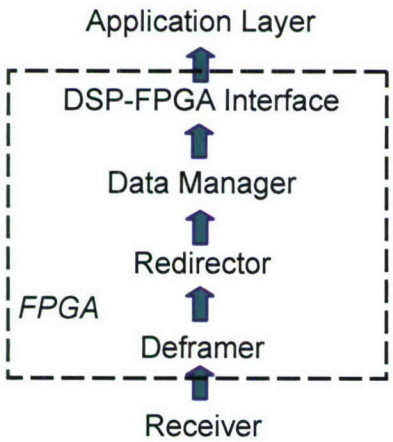


Fig. 7-13. Data flow direction of receiving packet.

When a receiver receives a byte it will pass it to the Deframer, which is responsible to collect all the packets for a complete packet and pass it to the Redirector. Then the redirector will pass the packet to the corresponding data manager according to the **CMD** field. Then the data manager will process this packet, and pass information to the application layer if necessary.

Next, the main parts of the link layer and network layer implemented in FPGA will be described.

VII.1. Interface between Link Layer to Optic Fiber

The interface between the link layer to the optic fiber is defined in UCTOP.vhd for UC communication and HMTOP.vhd in HMs, as shown in Fig. 7-14.

```
-- Transmission line halt
F1_TXHALT: out std_logic;

-- Selection of command or data
F1_TXSCD: out std_logic;

-- Transmission clock
F1_TXCLK: in std_logic;

-- Transmission command
F1_TXCMD: out std_logic_vector( 3 downto 0);

-- Transmission data
F1_TXDATA: out std_logic_vector( 7 downto 0 );

-- Transmission buffer empty
F1_TXEMPTY: in std_logic;

-- Transmission buffer full
F1_TXFULL_L: in std_logic;

-- Transmission enable
F1_TXEN: out std_logic;

-- Receiver part
F1_RXCMD: in std_logic_vector( 3 downto 0 );
F1_RXDATA: in std_logic_vector( 7 downto 0 );
F1_RXSCD: in std_logic;
F1_RXEMPTY_L: in std_logic;
```

```
F1_RXEN_L: out std_logic;
F1_RESET_L: out std_logic;
F1_RXCLK: in std_logic;
F1_LFI_L: in std_logic;
F1_VLTN: in std_logic;
RCLK: in std_logic;
```

Fig. 7-14. Interface definition between link layer and optic fiber in FPGA.

VII.2. Redirector

The redirector controls the dual ring fault tolerance. When an error occurs on one ring, the data is redirected to form a larger ring. Above the redirector on the LLI stack, there is no concept of dual rings, just commands coming in and going out.

VII.3. CMD Processor

The CMD processor is to coordinate between sending part of all data managers when multiple data packets are ready to send out. CDM processor also responsible for decision whether a receive packet should be forwarded, or a NULL packet should be inserted to the traffic. The following is the VHDL code that defines the priority of data packets.

```
if( COPY_PKT = '0' ) then
        if( EXT_PKT_RDY = '1' ) then
                OUTMODE <= EXTENDED;
        elsif( FORWARD_RDY = '1' and EXT_PKT_ABSORB = '0' ) then
                UTMODE <= FORWARD;  --still need to not forward bad packets
        elsif( NORMAL_PKT_RDY = '1' ) then
                OUTMODE <= NORMAL;
        elsif( SCHED_PKT_RDY = '1' ) then
                OUTMODE <= SCHED;
        elsif( UNSCHED_PKT_RDY = '1' ) then
                OUTMODE <= UNSCHED;
        elsif( EMGR_PKT_RDY = '1' ) then
                OUTMODE <= EVENT;
        elsif( DDM_PKT_RDY = '1' ) then
```

```
            OUTMODE <= DDM;
    else
            OUTMODE <= NULLPKT;
    end if;
```

Fig. 7-15. Priority of data packet types in CMD Processor.

VII.4. Net Clock Manager (NCM)

The net clock manager determines the correct value of the network clock. The correct value is based on inputs from packets coming from both sides, as well as the previous value of the network clock. As described before, the NCM should be able to adjust the local net clock according to the configuration. If the node is a net clock master, then the net clock should be incremented in open-loop mode; otherwise, it should be incremented in closed-loop mode.

VII.5. Direct Data Manager (DDM)

At UC side, NORMAL data packets are handled by DDM. Normally the control software in DSP computes duty cycles and will be sent out as NORMAL packets. On the other hand, when a NORMAL packet containing sensing data is received, it should be finally passed to the control software. So DDM is actually the interface between DSP and FPGA for NORMAL packets.

VII.6. Normal Data Manager (NDM)

At the HM side, NORMAL packets are handled by NDM. When DDM receives a NORMAL packet with DIR = 0x00, which means this is a duty cycle command that should be fired when it local net time equals to the value specified in data payload byte 1. For example that a HM receive a NORMAL packet addressed to itself with the following data payload:

0	1	2	3	4	5	6	7	8	9
0x00	0x50	0x1000		0x0020		*(Unused)*			

The NDM will send 0x1000 to the local modulator at net time 0x50.

VII.7. Asynchronous Data Manager (ADM)

The asynchronous data manager handles NS_SET_ASYNC and NS_GET_ASYNC commands. This data typically contains the manufacturer and vendor information for the node, local DIP switch settings, HEX values, and other data that is not time critical, such as protection thresholds set prior to converter operation, and even water cooling information.

VII.8. Packet Construction

There are several blocks responsible for the construction of the actual data packet. The framer takes the data in a series or array of bytes, and manages the pointer to the current byte to transmit. The EDC generator generates XOR check code used to verify that the packet is valid. The deframer takes a packet that has arrived, and decomposes it into pieces significant for command processing, such as the addresses, time, data and such. Depending on the packet format, the deframer will deframe the packets differently.

VIII. Application Layer Protocol

This section will describe the interface between control software running in DSP and the communications protocol in FPGA. The information exchanged is mainly through the memory mapped registers and arrays in the FPGA.

IX. Sending interface

When control software intends to send data to another node, there are two ways to do it: special packet or normal data packet.

IX.1. Special Packets

A special packet is defined at the application layer, which can be any type of data packets discussed in previous section. The memory mapped registers for transmitting special data packet are:

```
//PESNet Pointers for Special Data Packets
volatile UINT* const g_cpwSPECIAL1 = (UINT*)(0x10000010); //CMD|From|To|Nettime
volatile UINT* const g_cpwSPECIAL2 = (UINT*)(0x10000012); //Data1
volatile UINT* const g_cpwSPECIAL3 = (UINT*)(0x10000014); //Data2
volatile UINT* const g_cpwSPECIAL4 = (UINT*)(0x10000016); //Data3
```

Every special data packet register is 4-byte, and the content in g_cpwSPECIAL1 to g_cpwSPECIAL4 will be used to form one data packet.

And there is a control register associated with special packets transmission:

```
//Control register for special data packet
volatile UINT* const g_cpwSPECIAL_XFER    = (UINT*)(0x1000001E);
```

By writing to **g_cpwSPECIAL_XFER**, FPGA knows that data from DSP is ready to send out. And the network layer and link layer protocol will be started to form a packet. The following code shows an example function, which is used for composing a special packet in DSP control software. This function has six parameters, which is **CMD** code (nCmd), source address (nFrom), destination address (nTo), data payload byte 0-3 (nData1), data payload byte 4-7 (nData2), and data payload byte 8-9 (nData3) respectively.

```
void CommSendSpecialPkt( UINT nCmd, UINT nTo, UINT nFrom, UINT nD1, UINT nD2,
UINT nD3 )
{
        UINT nSp1 = nCmd << 28;
        nSp1 = nSp1 | (nTo << 16 );
        nSp1 = nSp1 | (nFrom << 8);

        *g_cpwSPECIAL1 = nSp1;  //special command
        *g_cpwSPECIAL2 = nD1;
```

```
        *g_cpwSPECIAL3 = nD2;
        *g_cpwSPECIAL4 = nD3;

        *g_cpwSPECIAL_XFER = 0x00000000;  //transfer special packet by writing to this
location

        volatile UINT* pStatus = (UINT*)(0x1000000C);

        //For now, wait for packet to be sent (do not stomp over)
        while( (0x00100000 & (*pStatus)) != 0x00100000 )
        {
                asm("nop;");
                asm("nop;");
                asm("nop;");

        }
}
```

For example, special packet can be used to send out a network address assignment packet, and the function call of **CommSendSpecialPkt()** would look like:

```
CommSendSpecialPkt( 0x7, 0x7F, 0x7F, cNewAddr1 | 0x22000000, 0x00, 0x00 );
```

This will ask the communication protocol stack to form an NS_EXTENDED packet, which **CMD** = 0x7. 0x22 means this is a network address assignment command. Before network addresses are assigned, every node has a default address, which is 0x7F. The source and destination addresses are both 0x7F, which actually means this NS_EXTENDED packet is a broadcast packet. Any node whose network address is still the default address 0x7F can take this packet, and set its own network address to be **cNewAddr1.**

Before normal operation, the master node needs to configure the network: assign network addresses → adjust packet alignment and set network clock working mode. The following code is a typical network configuration for a ring shown in Fig. 7-16. And configuration code is shown in

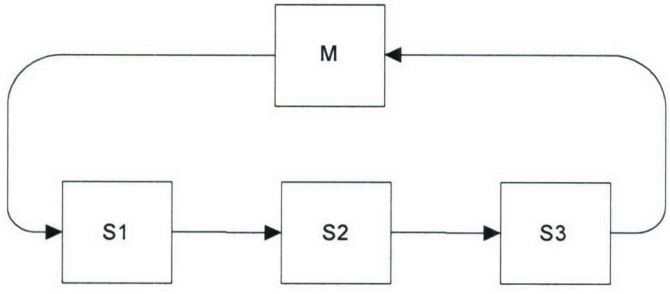


Fig. 7-16 A PESNet contains one master node and three slave nodes.

```
void SetupNetwork()
{
        UINT nTemp;
        static const UINT g_cnPktAlign = 0x0600;
        //Change packet address
        const UINT cNewAddr1 = 0x00230000;  //address 23
        const UINT cNewAddr2 = 0x00850000;  //address 85
        const UINT cNewAddr3 = 0x00460000; //address 46
        const UINT cNewAddr4 = 0x00980000; //address 98
```

```
        const UINT cNewAddr1L = cNewAddr1 >> 16;
        const UINT cNewAddr2L = cNewAddr2 >> 16;
        const UINT cNewAddr3L = cNewAddr3 >> 16;
        const UINT cNewAddr4L = cNewAddr4 >> 16;

        const UINT cChgAddrCmd1 = cNewAddr1 | 0x22000000;  //22 = change addr
command
        const UINT cChgAddrCmd2 = cNewAddr2 | 0x22000000;
        const UINT cChgAddrCmd3 = cNewAddr3 | 0x22000000;
        const UINT cChgAddrCmd4 = cNewAddr4 | 0x22000000;
// assign network addresses
        CommSendSpecialPkt( 0x7, 0x7F, 0x7F, cChgAddrCmd1, 0x00, 0x00 );
        CommSendSpecialPkt( 0x7, 0x7F, 0x7F, cChgAddrCmd2, 0x00, 0x00 );
        CommSendSpecialPkt( 0x7, 0x7F, 0x7F, cChgAddrCmd3, 0x00, 0x00 );
        CommSendSpecialPkt( 0x7, 0x7F, 0x7F, cChgAddrCmd4, 0x00, 0x00 );

// set net clock working mode of each node
        //unlock async memory for writing (1st slave node, 0x23)
        CommSendSpecialPkt( 0x3, 0x23, 0x98, 0x0080FFFF, 0x00000000, 0x00000000 );
        //set net clock of 0x23 to work in open loop mode
        CommSendSpecialPkt( 0x3, 0x23, 0x98, 0x00824018 | g_cnPktAlign, 0x00000000,
0x00000000 );

        //unlock async memory for writing (2nd node, addr 85)
        CommSendSpecialPkt( 0x3, 0x85, 0x98, 0x0080FFFF, 0x00000000, 0x00000000 );

        // set net clock of 0x85 to work in open loop mode
        CommSendSpecialPkt( 0x3, 0x85, 0x98, 0x00824018 | g_cnPktAlign, 0x00000000,
0x00000000 );

        // unlock async memory for writing (3rd node, addr 46)
        CommSendSpecialPkt( 0x3, 0x46, 0x98, 0x0080FFFF, 0x00000000, 0x00000000 );
        // set net clock of 0x46 to work in open loop mode
        CommSendSpecialPkt( 0x3, 0x46, 0x98, 0x00824018 | g_cnPktAlign, 0x00000000,
0x00000000 );

        // unlock async memory for writing (4th node, addr 98)
        CommSendSpecialPkt( 0x3, 0x98, 0x98, 0x0080FFFF, 0x00000000, 0x00000000 );
        // since 0x98 is the master node, set net clock of 0x98 to work in open loop mode
        CommSendSpecialPkt( 0x3, 0x98, 0x98, 0x00828018 | g_cnPktAlign, 0x00000000,
0x00000000 );
}
```

It should be noticed that in this configuration, **g_cnPktAlign** is the number of packet periods the transmitter clock lagging the receiving clock. The value needs to be manually adjusted until all the net clocks in the network are synchronized.

IX.2. Normal Data Packet

There is a memory mapped array of size 8 in the FPGA especially used for DSP to send PWM commands to slave nodes. The transmission table (TxTable) is:

	Dest Addr	Data1	Data2	Data3
0x10008000	*Reserved*			
0x10008100				
0x10008200				
…				
0x10008700				

After network configuration, the TxTable should also be initialized. The **Dest Addr** fields should be filled with the node addresses that the master will receive data packets from. If still using the example above, after initialization, the TxTable should be:

	Dest Addr	Data1	Data2	Data3
0x10000000	*Reserved*			
0x10000100	0x23			
0x10000200	0x85			
0x10000300	0x46			
…	(not initialized)			

Similarly as sending special packets, there is a control register related to TxTable, which is:

```
volatile UINT* const g_cpwENO        = (UINT*)(0x1000000E);
```

The register **g_cpwENO** is a place holder, with each bit corresponding to each row of the TxTable. Once a bit is set means the corresponding row in TxTable is ready to be sent out. Then normal data manager in FPGA will read in the row and form a NS_NORMAL data packet.

X. Receiving Interface

The RxTable collects NS_NORMAL packets addressed to the master node. Unlike TxTable, RxTable is a column array.

	SRC Addr 0x10008008	Data1 0x10008100	Data2 0x10008200	Data3 0x10008300
+0	0x23			
+2	0x85			
+4	0x46			
+6				
…				

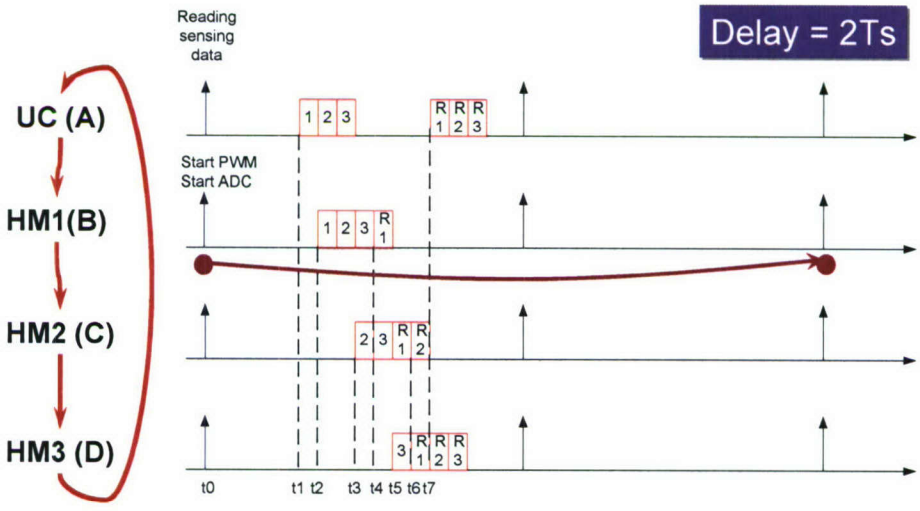
XI. Latency due to Communication

Due to the limited bandwidth of communication network and all the digital components signal processing speed, there will be digital delays associated with the PEBB system, as shown in Fig. 7-17. Digital delay could detrimental overall control performance as will be discussed later.

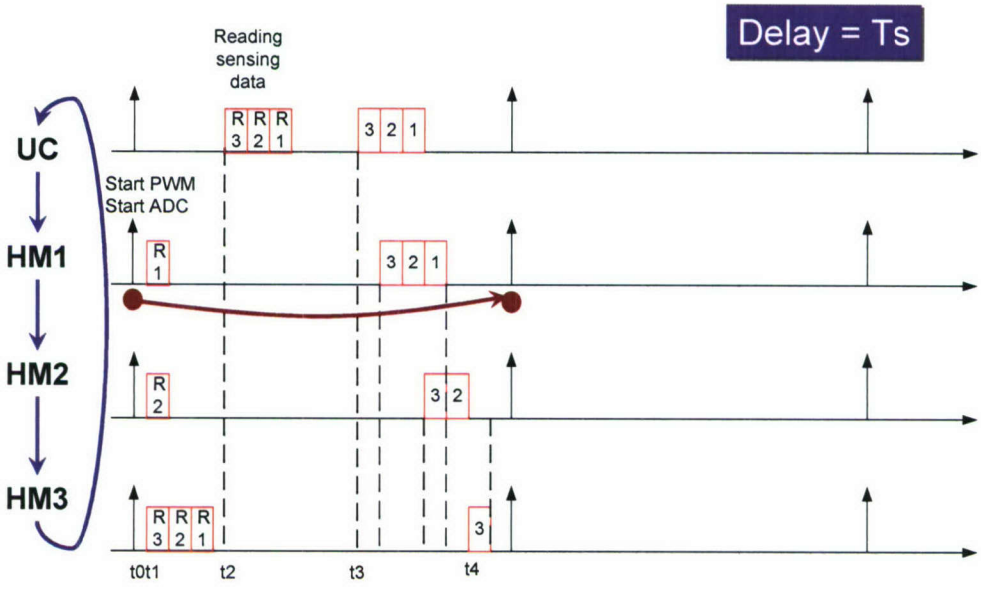
Different digital delays may occur due to the sequence of handshaking between UC and HMs. For an open loop control, the digital delay is defined as the real time elapsed from a switch command computes until a switch begins to act. In a closed-loop control, the digital delay will be defined as the time elapsed from a measurement (voltage, current, etc.) gets sensed until an associated switch operation get taken. The

digital delay is more critical to closed-loop system since it will affect the system transient response and even stability.

Fig. 7-17 (a) shows if at the beginning of a switching period, the UC reading in all necessary sensing data for closed-loop computation, which is actually acquired at HMs in the previous switching period, and then generates switch commands and send to every HMs. These commands will decide the action of PEBBs at the beginning of next switching period. Thus, the digital delay in this case will be 2 switching periods. If data sensing, ADC conversion at HMs and UC reading sending data, computing and sending commands to HMs can be arranged in one switching period, then the digital delay can be reduced to one switching period, as shown in Fig. 7-17. In the former case, UC could have longer time for computation; while in the latter case, the control loop can have higher bandwidth and better performance.



(a) 2Ts delay



(b) Ts delay

Fig. 7-17. Different digital delay caused by communication.

XII. Conclusions and Future Improvements

Several aspects can be considered as improvements to PESNet 2:

- Power stage hardware protection: the mechanism to detect, report and handle failure or exception in power stage hardware;
- Extend to dual ring protocol: fault tolerance of network link or node failure or exception;
- Improved DSP/FPGA communication interface: support of emergency interrupt.

Chapter 8 PROTECTION SYSTEMS FUNCTION DEFINITION

I. Hierarchical protection systems

Protection systems, like control systems, are a part of the power converter system and its application. Protection systems exist to contain faulty behavior and prevent it from spreading from the subsystem into other systems. Previous work on protection systems has been done using monolithic approaches, where the protection system (implemented in hardware and software) is not a solution that can be standardized across applications.

The protection system fits into the standard cell open architecture control system model, as shown in Fig. 8-1.

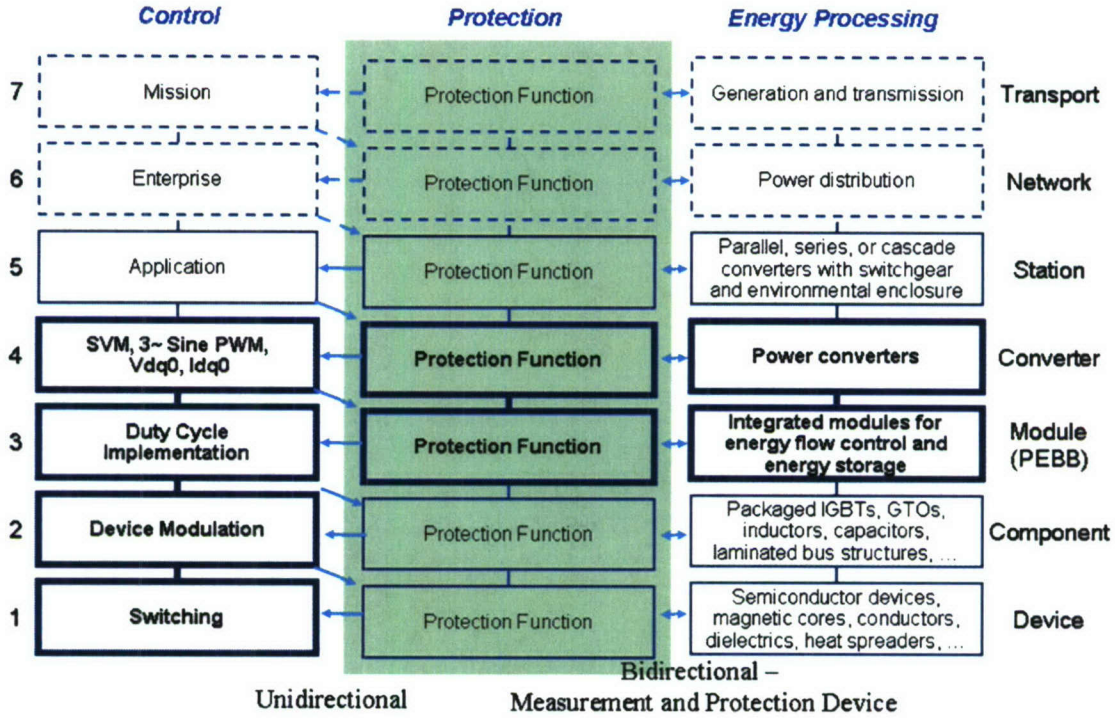


Fig. 8-1 Hierarchical system for standard-cell open architecture power electronics conversion systems

Here, a significant difference from previous layers is that the protection system acts on the control system using information from the electric power system as well as from the control system layer above it. However, the control system does not influence the protection system at that layer (unidirectional relationship).

In addition to the protection system affecting the control, it also has some actuation devices of its own to limit energy buildup. Such devices are solid state circuit breakers, solid state crowbars, contactors, and transfer switches. They react to commands given from the control system, and they affect the energy processing system, as shown in Fig.8.1.

As the layers go up, the protection functions (shown in the middle) become more abstract and possibly application specific, involving variables that may not be measured, but may be the result of computation, such as limiting DQ0 variables.

II. Protection System Architecture

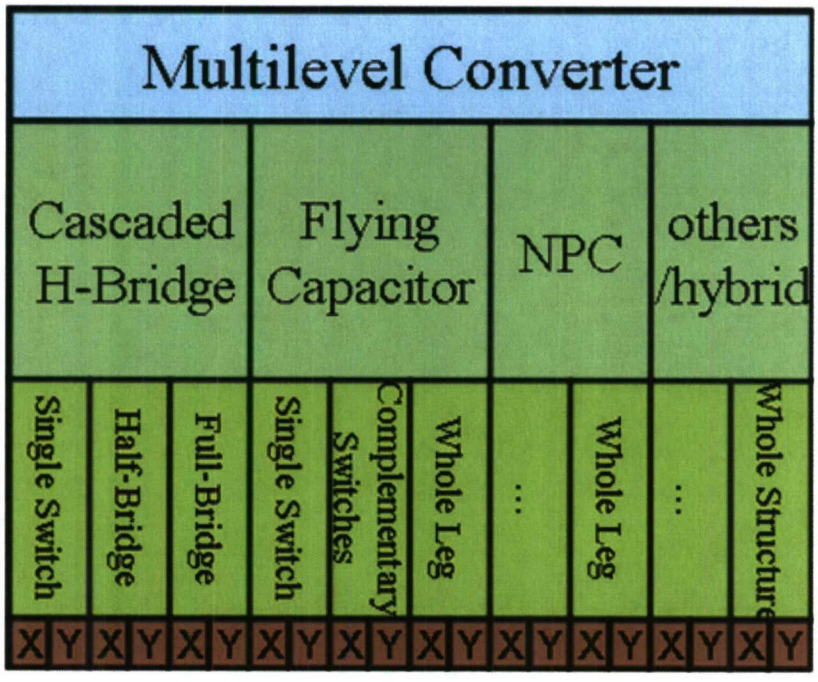


Fig. 8-2 Components diagram for a three-level NPC converter.

As an attempt to partition the protection system, a relationship between the components of the physical protection system is needed. Here, it is shown that a converter can be made of several different technologies (phase legs), which are in turn, can be made of several different technologies (phase leg segments), which are in turn made of several different technologies themselves (devices).

How the devices are controlled, and their device specific behavior should not influence the protection system of the converter at the converter level. Similarly this can be applied to all subsystems. The hierarchy appears as an aggregation of subsystems at every level, and only the ideal behavior of that subsystem will propagate upwards, abstracting the detail at each layer. Hence, a failure at each layer is treated as an atomic failure, forcing a response from the layer above it, such as the use of a redundant module. If the detail of each module has to be decided, the model no longer is compatible at the interfaces (internal information is needed to operate the system).

As the modules become more complex and intelligent, it may be possible for the module to operate at a reduced capability. For example, if a module is overheating, it may be feasible to operate the module at a reduced switching frequency at the cost of performance. The challenge is to define the interface between the device (which is overheating) and the switch combination, and so on so that the converter level function for switching frequency can be adjusted.

III. Protection Function Locations

It is important to design the protection system so that the converter design is standardized, and selection of components is independent of protection functions at other levels (hierarchical and interchangeable module design).

At a converter level, a typical I/O diagram of the converter protection function block looks as shown below:

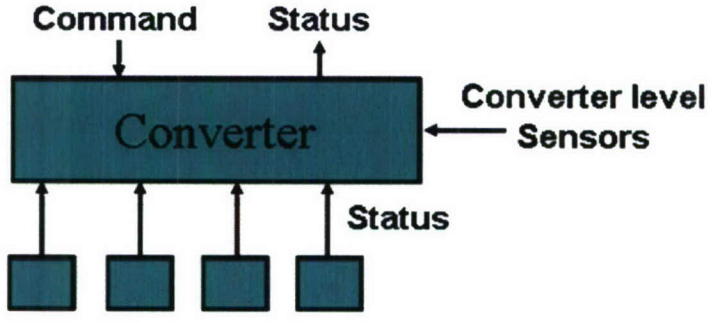


Fig. 8-3 Basic I/O block diagram for a converter protection system.

It is necessary to define which protection functions will appear at which layers. Previously, the entire system was integrated into one. However, it is necessary to now classify protection system functions as internal functions to a module and interface protection functions, which protect information and energy flow across module and subsystem interfaces. Such an example is given below, for a DC/DC converter.

A DC/DC converter can be represented in an average sense by the following set of differential equations:

$$duty \cdot V_{dc} = Ri + L\frac{di}{dt} + v$$

$$C\frac{dv}{dt} = i + \frac{v}{Rl}$$

These equations can be mapped to a new set of variables via a diffeomorphism (nonlinear, invertible change of variables). The new states of the converter can be chosen to be energy and power. From here, it can be calculated what the maximum energy of the converter is given the desired maximum operating point. A protection mechanism can be used here that limits the energy of the converter, as the energy in the inductor will transfer to the capacitor. To do simply voltage limiting will still cause overshoot, and then over-voltage. However, by considering energy, the duty cycle can be blocked when the operating point in these new coordinates are out of the safe area. A simulation was done to prove this works for a large transient in the output or input. The results can be seen below. These measurements were taken at the converter's electrical interface, and were used to limit the duty cycle to the converter (information input).

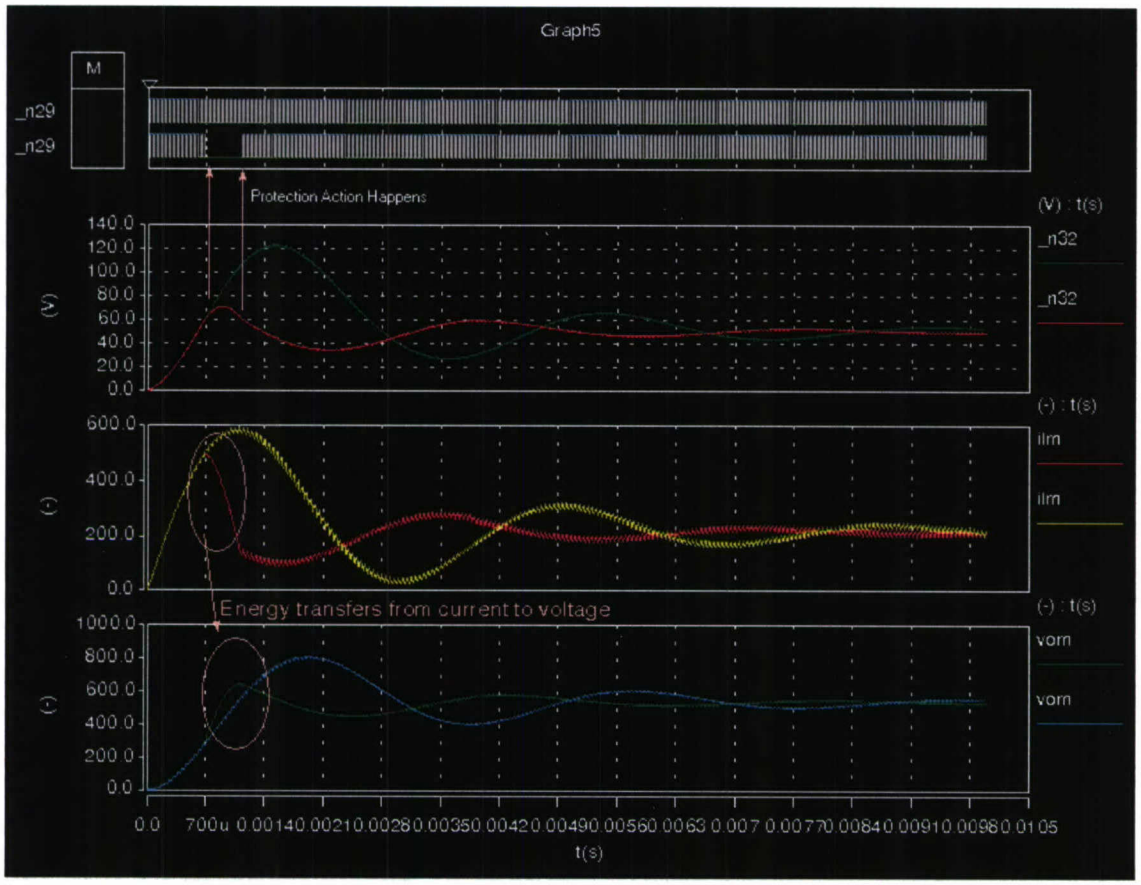
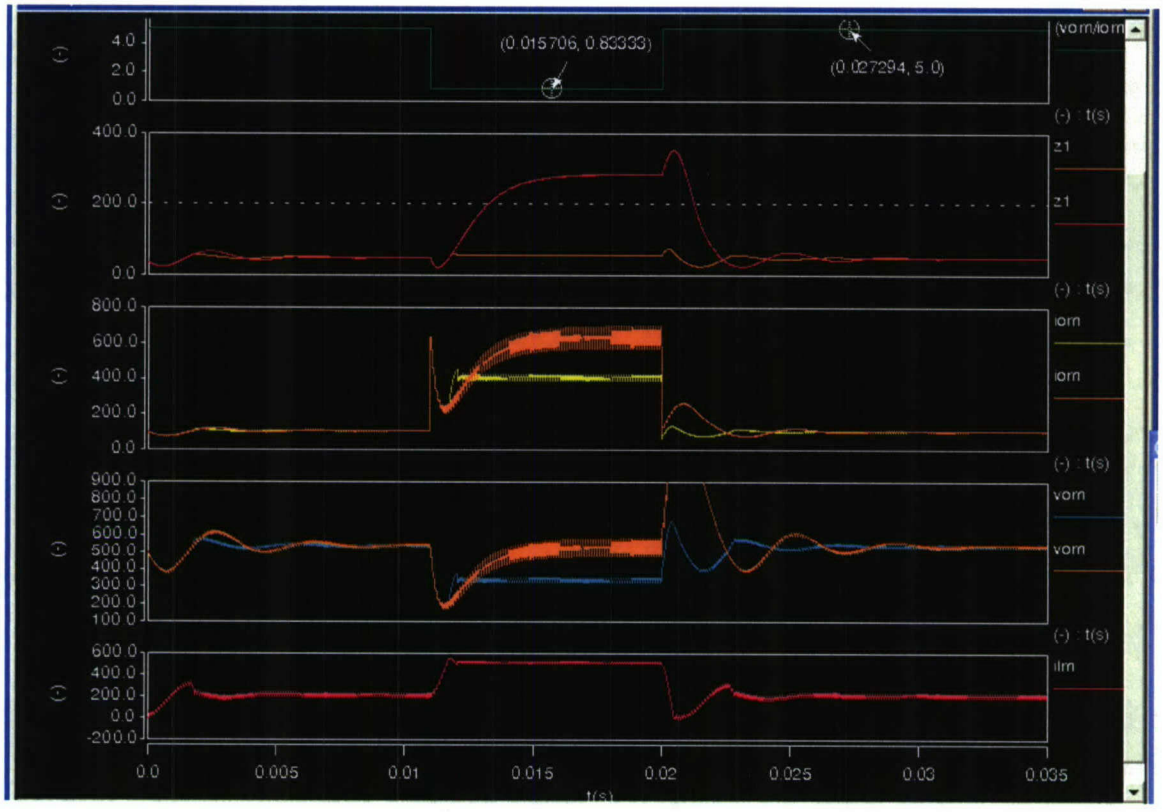


Fig. 8-4 Simulation waveforms of a converter under test.

Similarly, shorting the load can be seen, and an internal protection event can occur to limit the energy of the converter. The superimposed waveform is the unprotected converter, which will exceed the give power limits for the converter module. Since this is a function of the converter itself, and not the converter's position within the system, this becomes an internal protection function, and not an interface protection function.

Furthermore, this does not interrupt energy flow as do circuit breakers. Shorting various points in the converter will lead to the protection scheme to activate such as shorting the output as demonstrated in simulations. Similarly, moving to a load that requires too much power will also cause the protection scheme to activate. One major issue learned from research and classes is that it is more important to have a secure network than a dependable one. That is, protection schemes should only activate when necessary and not act "pessimistically", as this can lead to cascading failures. Here, because a protection action limits the energy as opposed to taking that node from offline, it may be possible that it can act at reduced capacity, allowing for additional modules to take over in a coordinated effort.



I. **Fig. 8-5 Simulation waveforms of a converter under faulty conditions.**

IV. Coordinated Protection Systems

In traditional systems (without converter communication between components), an over-voltage condition on a DC link will fire a crowbar. This crowbar will short the DC link, causing the current into the converter to rise until a circuit breaker is tripped. While this is effective, it will cause a large transient in the system in which the converter exists. By coordinating the crowbar with the circuit breaker, the large current transient can be avoided. The DC link voltage monitoring is at least a converter level protection function (if not a station level protection function in the case of parallel converters). Current into these subsystems needs to be managed.

V. Design of a Protection PCB

To accommodate this research, and test the theory against a physical system, a PCB has been designed that allows a protection system to be implemented. This PCB is designed to work with either a gate driver for a IGBT based solid state circuit breaker or an SCR based crowbar. A conceptual schematic of the device operating as a circuit breaker is shown below. Ports are made available for coordinated protection events as well as sensing. High speed AD converters are used due to the nature of protection events within a circuit.

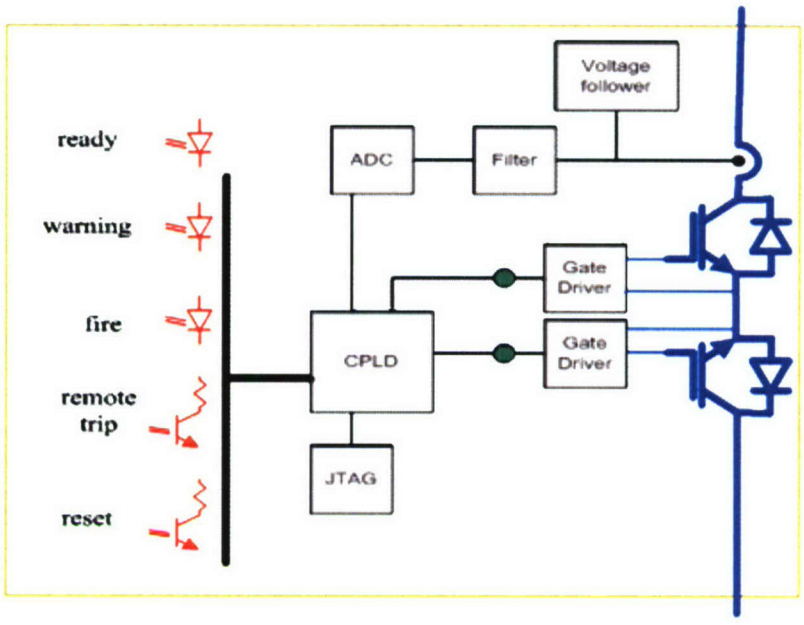


Fig. 8-6 Schematic of protection PCB.

The PCB itself is shown below:

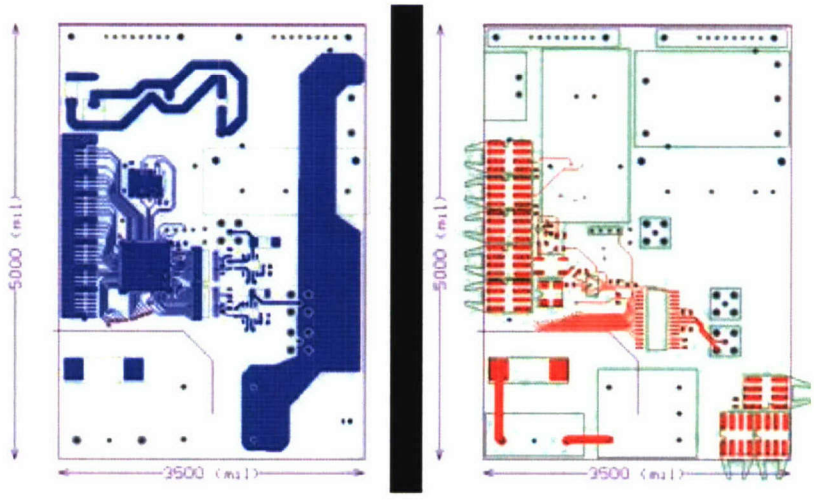


Fig. 8-7 Protection PCB diagram.

This PCB can also connect to the existing hardware manager to make a protection type PEBB.

VI. Summary

This Chapter has presented an overview of protection systems and the feasibility of utilizing the standard-cell open architecture reference model to modularize and standardized their implementation. For specific implementation needs, an energy-based approach has been analyzed discussing the main advantages it could provide if such a protection scheme is used for power electronics converters. Finally, in an effort to support the experimental work using PEBB-based systems conducted at CPES, a protection board was designed and built for IGBT semiconductors.

Chapter 9 APPLICATIONS TO DISTRIBUTED GENERATION

I. Introduction

As the demand for more reliable and secure power systems steadily increases, Distributed Generation (DG) and intentional islanding have become progressively more popular; especially in the aftermath of the Californian energy crisis and the northeastern blackouts. Through the control of power electronics based Power Conversion Systems (PCS), the interconnection of DG resources (or DERs) to three-phase (3Φ) power systems can realize benefits such as increased power system reliability and security [1], [2]. Control of the PCS can bring other advantages such as: power supply support (peak shaving) during critical demand times, uninterruptible power supply to area electric power systems (Area EPS) during grid disturbances, and harmonic and phase unbalance correction [3]. However, there are challenges to overcome when connecting DERs to utility systems, while fully reaping the benefits that DG and intentional islanding can provide. Some of these issues and concerns include: modes of control operation, detection of islanding events, and re-closure detection, while adhering to accepted standards (such as IEEE 519, 929, & 1547).

The proposed control strategies and novel active detection and re-closure schemes allow for fast disconnect times, a zero non-detection zone (NDZ) and autonomous operation from the grid. The detection and re-closure schemes work with the switched-mode operation of the control to permit the PCS to continuously supply power to the loads. The control, detection and re-closure algorithms presented are compared to other schemes and verified through simulation.

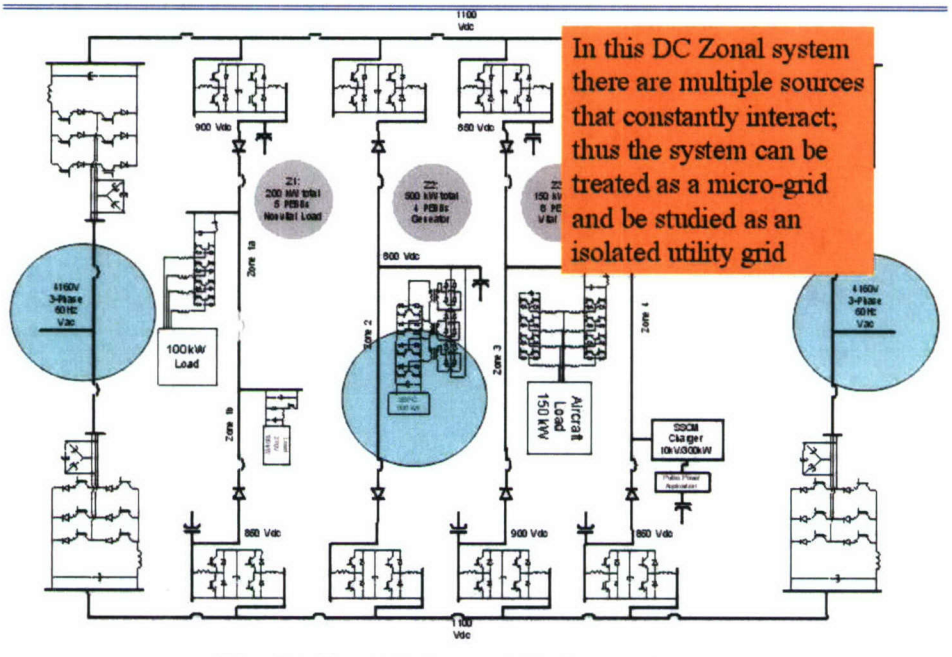


Fig. 9-1 Zonal "micro-grid" of a naval vessel

By studying the utility distribution system, the results can be easily translated to other distributed systems, a naval ship for example. DG units can be (and are being) implemented quickly and effectively on naval ship systems. The idea is that a ship can have main generating sources, but also have several smaller sources backing up and complementing the main generators. Since these sources are spread out through the ship, the ship's entire electrical system can be regarded as a "micro-grid"; with reconfiguration capabilities in the event of a sector of the "micro-grid" failing. The DG units can reconfigure themselves such that the "micro-grid" can still operate on or above minimum specifications when a fault occurs. As seen in Fig. 9-1,

the distribution scheme used for ship electrical systems resembles that of DG utility systems. In the "micro-grid" setup of the ship, such issues as reconfiguration and paralleling can be explored through the utility system setup.

I.1. Background

Distributed generation is defined to be the interconnection of energy resources to the existing utility in an effort to change the system from having large, centralized power plants to that of a network of distributed energy producing sources located throughout the grid system [3], as depicted in Fig. 9-2

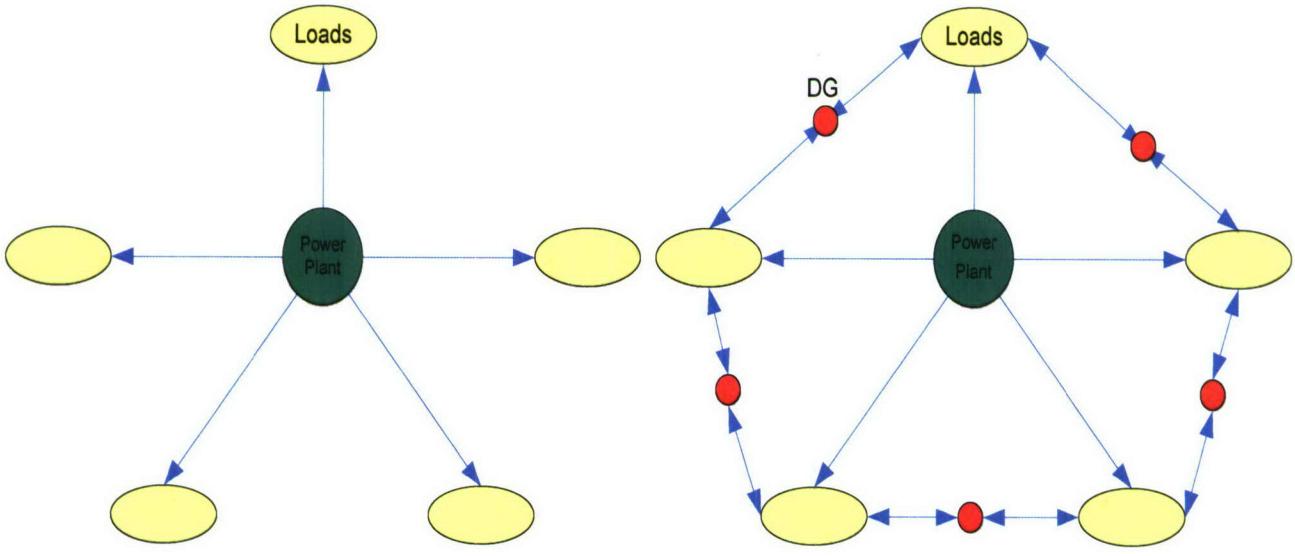


Fig. 9-2 Centralized (Left) & Distributed (Right) power systems

With the use of DERs throughout the utility, an ability previously unavailable on a wide scale can now be implemented; the purposeful sectionalization of the utility during utility wide disturbances. When a disturbance occurs, sections of the utility isolate themselves and use the DERs to maintain nominal operating conditions [2]. This concept, also called "intentional islanding", can lead to benefits such as uninterruptible power supply.

With intentional islanding, a DG system connected to the utility has two basic topological modes of operation: Grid-connected mode and Islanding mode. These two modes of operation have very different control requirements, and it is shown that a switched-mode control with detection and re-closure algorithms scheme can regulate the output while changing between the two modes of operation.

In Fig. 9-3 below, Area EPSs are seen in relation to the utility. In this setup, one of the Area EPSs can be disconnected from the utility through the point-of-common-connection (PCC), and still have the ability to provide load demand by means of the DER and PCS [4], [5]. A more detailed block diagram of the DER, PCS and grid interconnection is presented in Fig. 9-4 below.

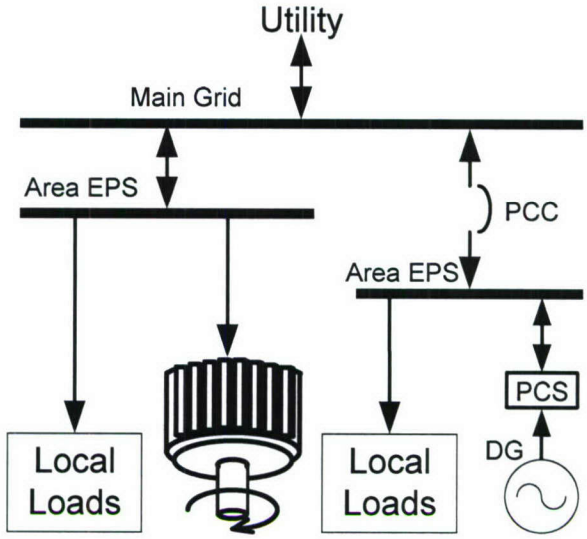


Fig. 9-3 Area EPSs of a Utility System showing DG interconnection

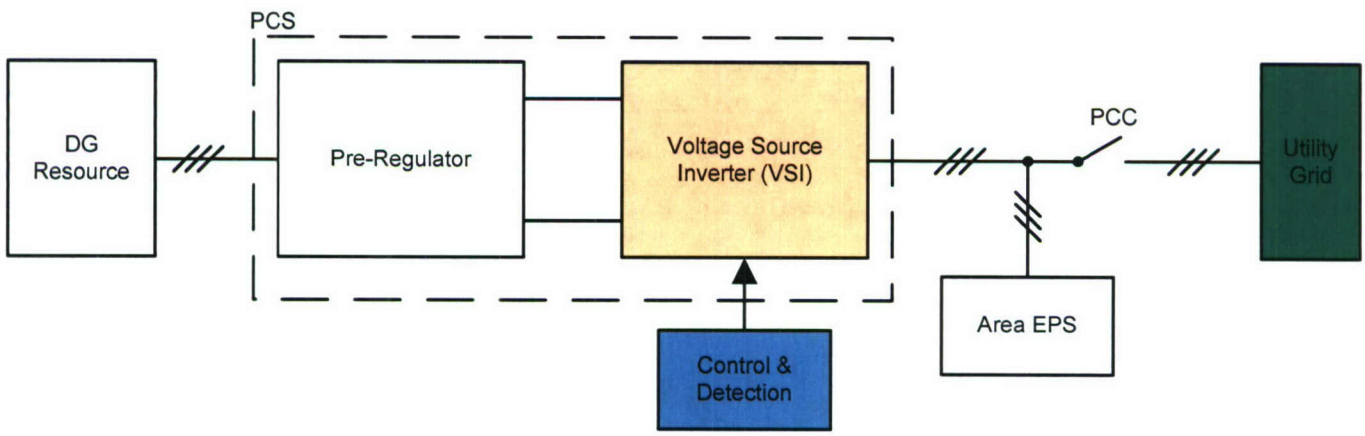


Fig. 9-4 Block diagram of DER, PCS, and grid interconnection

For the system to properly switch between the types of control that intentional islanding demands of it, the ability to detect the mode of operation the system should be must be present within the control. Islanding detection and grid re-closure algorithms are therefore employed and presented in detail in the following sections.

II. Assumptions

This work makes the following assumptions of the system:

1) Utility is dominant and voltage regulation is maintained by utility while system is grid-connected
2) DER has two modes of operation with respect to the utility
    a. Grid-connected (in parallel operation)
    b. Islanded
3) Only the grid-interfacing portion of the PCS is designed for, DC voltage within PCS that feeds VSI is assumed to be well regulated from previous conversions within PCS
4) Standards would allow system to reconnect to utility while still energized

5) Utility is a 3Φ, 3-Line system

6) Ideal models for switching converters

These assumptions can be extended and generalized to multiple systems (ie: system can be modified to multiple phases, multi-level, as well as parallel operation of DERs themselves).

III. Work

A. Converter Modeling and Control – ABC & DQ0

The standard switching model of a VSI can be seen below in Fig. 9-5 There are numerous papers that describe how to calculate an average model, such as those presented in [7], [8], [9]. These models range from the basic, idealized to complex, non-linear cases. For simplicity, this paper uses an ideal, lossless average phase model of the VSI, similar to that presented in [9].

Each phase-leg of the inverter can be analyzed, then combined to create the model generalized by (1). The 3x1 vectors V_{ABC} and i_{ABC} represent the voltages of the phases across the load resistances and current through phase inductors (respectively), while s_{ABC} is a switching function of the top switches, with s = 1 being switch closed, and s = 0 being switch open.

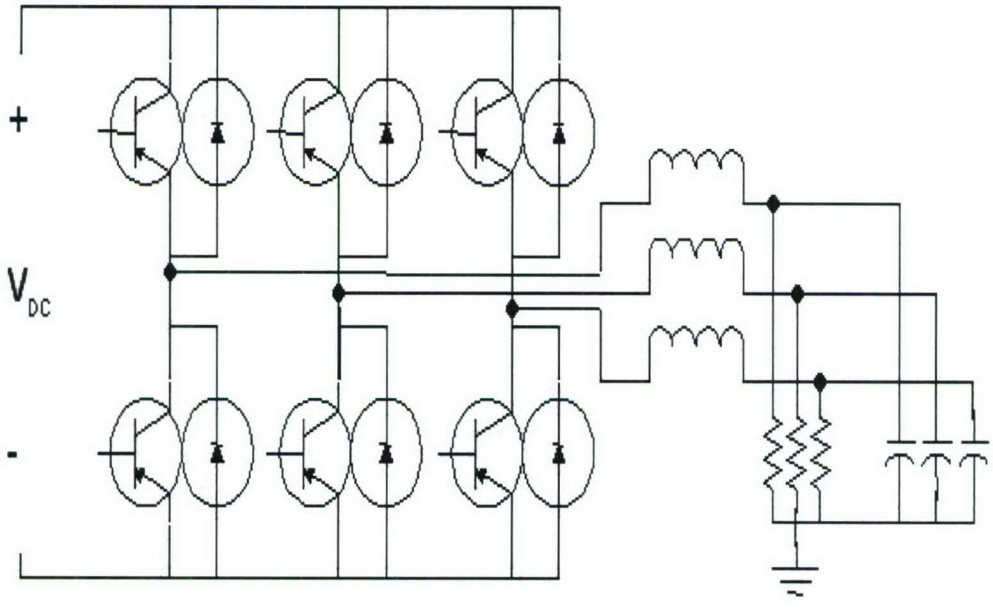


Fig. 9-5 Switching Model of VSI.

The bottom switch must act complementary to the top switch, or else the DC bus will be shorted.

$$\begin{aligned} \vec{V}_{ABC} &= \vec{s}_{ABC} v_{DC} - L\frac{d}{dt}\left(\vec{i}_{ABC}\right) \\ \vec{i}_{ABC} &= \frac{\vec{V}_{ABC}}{R} - C\frac{d}{dt}\left(\vec{V}_{ABC}\right) \\ i_{DC} &= \vec{s}_{ABC}^{T}\,\vec{i}_{ABC} \end{aligned} \tag{1}$$

An approximated moving-averaging technique, (2), is then applied to create the equivalent, mathematical model of (3). This approximation to a moving-average function is only valid as long as the switching frequency, $f_S = 1/T$, is much greater than any transient effect frequencies, such that the effects look constant over a switching-cycle. Example shown in (2):

$$\begin{aligned}
&\bar{x} = \frac{1}{T}\int_{t-T}^{t} x(\tau)d\tau \quad \& \quad assume \\
&\overline{\frac{d}{dt}(x)} = \frac{d}{dt}(\bar{x}) \qquad \therefore \\
&x_1 = x_2 x_3 - \frac{d}{dt}(x_4) \qquad \downarrow \\
&\bar{x}_1 = \frac{1}{T}\int_{t-T}^{t}\left[x_2(\tau)x_3(\tau) - \frac{d}{dt}(x_4(\tau))\right]d\tau \\
&\bar{x}_1 \approx \bar{x}_2\bar{x}_3 - \frac{d}{dt}(\bar{x}_4)
\end{aligned} \tag{2}$$

With the vector d_{ABC} being the moving-average of the vector s_{ABC}. Drawn as an electrical diagram, (3) is seen in Fig. 9.6 below.

$$\begin{aligned}
&\bar{\bar{V}}_{ABC} = \bar{d}_{ABC}\bar{v}_{DC} - L\frac{d}{dt}\left(\bar{\bar{i}}_{ABC}\right) \\
&\bar{\bar{i}}_{ABC} = \frac{\bar{\bar{V}}_{ABC}}{R} - C\frac{d}{dt}\left(\bar{\bar{V}}_{ABC}\right) \\
&\bar{i}_{DC} = \bar{d}_{ABC}^{T}\bar{\bar{i}}_{ABC}
\end{aligned} \tag{3}.$$

The models seen in Fig. 9-5 and Fig. 9-6 were tested under open-loop conditions and the outputs of the average model closely match the switching model.

The control itself is done in a rotating coordinate frame, thus a sinusoidal signal is regulated as a DC signal. To convert from a stationary coordinate frame (ABC) to rotating (DQ0), a version of Park's transformation, (4), needs to be applied to the ABC signals.

$$\begin{bmatrix} X_d \\ X_q \\ X_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin(\theta) & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix}$$

where (4)

$X = V \text{ or } I \quad \& \quad \theta = \omega t + \theta_o$

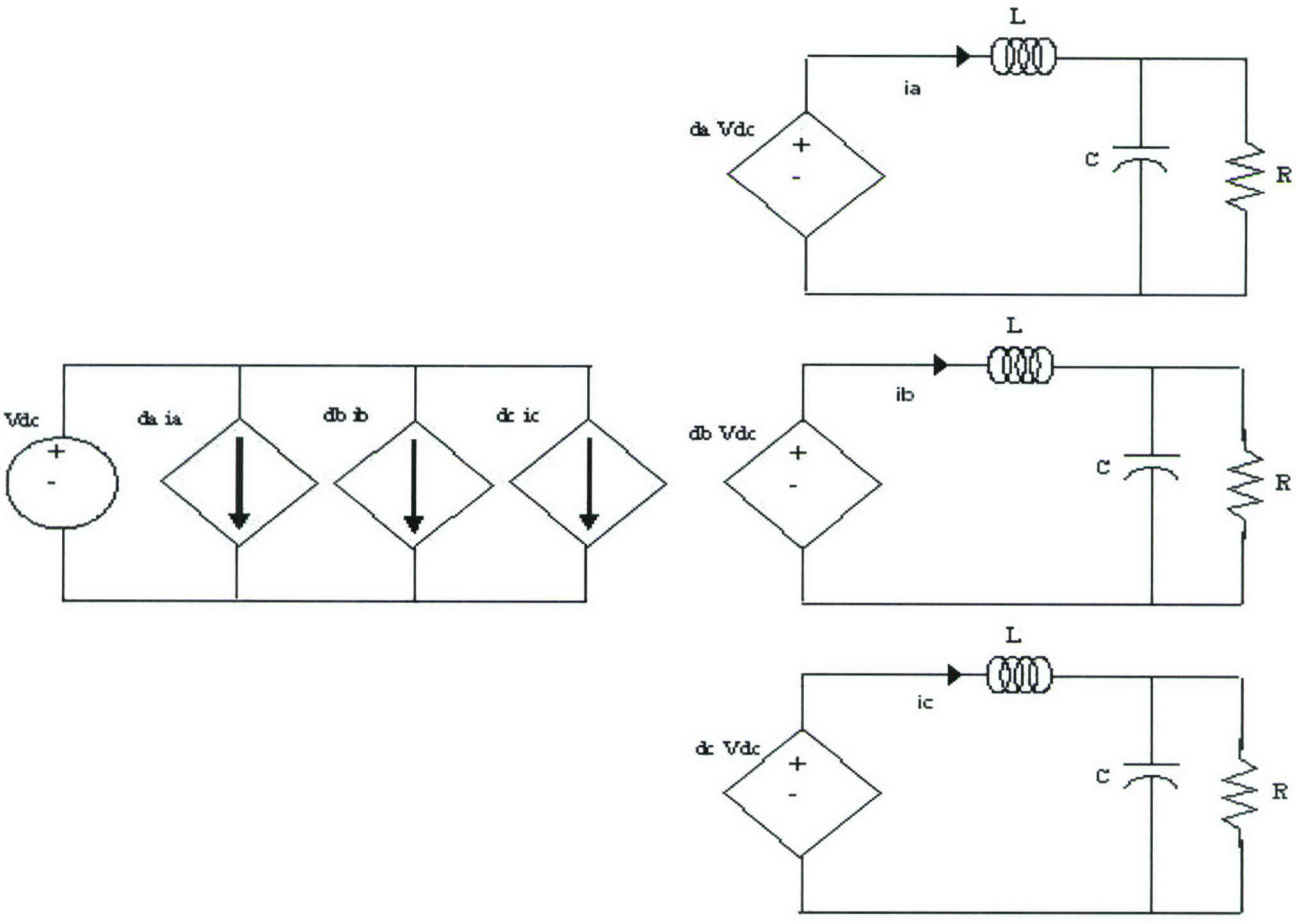


Fig. 9-6 Diagram of VSI Average Model.

The D-channel from the set of DQ0 signals corresponds to the real power, while the Q-channel refers to the reactive power. Applying this transformation to the ABC average model of the VSI, (5) is produced.

From (5), the terms from the Q-channel appear in the D-channel equations and vice-versa; therefore, for the controller channels to have independency from one another, the system needs to be decoupled.

$$\bar{\bar{V}}_{dqo} = \bar{\bar{d}}_{dqo}\bar{v}_{DC} - L\frac{d}{dt}\left(\bar{\bar{i}}_{dqo}\right) - \begin{bmatrix} 0 & -\omega L & 0 \\ \omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \bar{\bar{i}}_{dqo}$$

$$\bar{\bar{i}}_{dqo} = \frac{\bar{\bar{V}}_{dqo}}{R} - C\frac{d}{dt}\left(\bar{\bar{V}}_{dqo}\right) - \begin{bmatrix} 0 & -\omega C & 0 \\ \omega C & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \bar{\bar{V}}_{dqo} \tag{5}$$

$$\bar{i}_{DC} = \bar{\bar{d}}_{dqo}^{T}\,\bar{\bar{i}}_{dqo}$$

By replacing the duty-cycle terms accordingly, the coupling terms can be cancelled through the control. This is shown for the D-channel in (6).

$$\bar{V}_d = d_d\bar{v}_{DC} - L\frac{d}{dt}\left(\bar{i}_d\right) + \omega L\,\bar{i}_q$$

$$d_d \rightarrow \left[-\frac{\omega L}{\bar{v}_{dc}}\bar{i}_q + (x_{dREF} - \bar{x}_d)H_{xd}\right]$$

$$H_{xd} = compensator, \quad \therefore$$

$$\bar{V}_d = \left[-\frac{\omega L}{\bar{v}_{dc}}\bar{i}_q + (x_{dREF} - \bar{x}_d)H_{xd}\right]\bar{v}_{DC} \tag{6}$$

$$-L\frac{d}{dt}\left(\bar{i}_d\right) + \omega L\,\bar{i}_q$$

$$\bar{V}_d = \left[(x_{dREF} - \bar{x}_d)H_{xd}\right]\bar{v}_{DC} - L\frac{d}{dt}\left(\bar{i}_d\right)$$

In (6), "x" is the controlled state (either V or I). This controller setup is depicted for all channels in Fig. 9.7 below.

The compensators H_{Xk} (k = d, q, o) are classically designed PID controllers, and are designed based on which mode of operation the system is running in, X = V for voltage mode (VM, islanding mode) and I for current mode (IM, grid-connected mode).

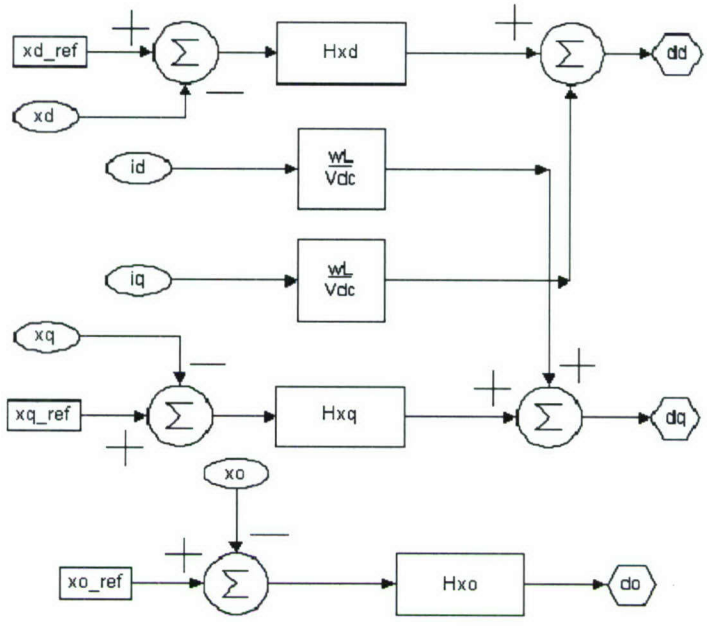


Fig. 9-7 Control loops with decoupling.

B. Past & Present Schemes and Algorithms

i) Control Strategies

Past and present control strategies are limited to provide only forms of current regulation, due to standards. These standards dictate that the DER shall not be used to directly regulate the voltage upon the grid; voltage harmonics and distortions must be corrected through current injection techniques. These restrictions all limit the use of the DERs, and prevent further benefits from being implemented.

There are many different means by which the current is ultimately regulated; ranging from using current, voltage, frequency, phase, and power measurements to perform the regulation [10], [11], [12], [13], [14]. From these, the regulation can be performed by classical PID control techniques, droop methods, or other hybrid techniques. The preferred method of control for DG implementation with intentional islanding is the classical PID regulators.

Droop methods have draw backs, especially in 3Φ systems [15]; such as that they inherently produce small errors in the output and the system can never achieving zero steady-state error; also, droop control cannot properly regulate harmonic distribution between the phases due to non-linear loads and line conditions, and line impedances for 3Φ systems also significantly influences the reactive power and cannot be easily solved by droop control techniques. Droop control is great for load sharing control, but when a system that needs to change between modes of operation and thus control operation, droop control is not a favorable choice.

Hybrid systems mixed master/slave and droop control systems which combine the useful features of each type of control while eliminating some of the undesirable ones [16]; but like the classical droop control, when the hybrid style is used in a system that needs to change modes of operation due to a topology shift it is not a favorable choice either.

ii) Islanding Detection

Commonly referred to as "Anti-Islanding" detection, these algorithms use sensed parameters to determine if the system has entered an "islanded" state; a condition where the system remains un-intentionally energized during utility disturbances. This condition can lead to various and numerous safety and operating issues best to be avoided.

Detection techniques can be classified as either passive or active (with the active ones incorporating aspects of the passive ones) [17]. Passive techniques include all detection algorithms that use only sensed and/or calculated parameters (such as voltage magnitude, phase shift, frequency deviation) to detect an islanding event [18], [19]. Passive techniques also are susceptible to NDZs. Active schemes can overcome these but at a price. Active techniques include those detection schemes that use passive techniques in conjunction with control loops which help influence the output of the converter. These active techniques are much better at detecting islanding events (even the ones passive detection cannot), but they require for their active control portions to constantly perturb the output of the converter; this affects the performance of the system negatively [17], [20], [21].

iii) Re-closure

Currently, to reconnect a DER that is energizing an isolated Area EPS to the utility after an islanding event has passed, the Area EPS must wait for at least 5 minutes once the disturbance has pasted; then the Area EPS has to be completely de-energized, then it can be reconnected to the grid, and finally the DER can start to provide power to the system (from IEEE 1547). These requirements to reconnect cause unnecessary and prolonged downtimes that can be avoided with new control standards.

C. Proposed New Scheme and Algorithms

i) Control Strategies

Due to standards and regulations, when a DER is interconnected to the utility, the system cannot actively regulate the voltage. But when the system incorporates concepts of DG and intentional islanding, voltage regulation becomes necessary for the proper operation of the Area EPS. This need arises from the change of system topology and operation between the grid-connect and islanding modes of operation.

It is proposed that by having switch-mode control, the system can be effectively implemented to operate in both modes of operation; while still adhering to present standards and regulations.

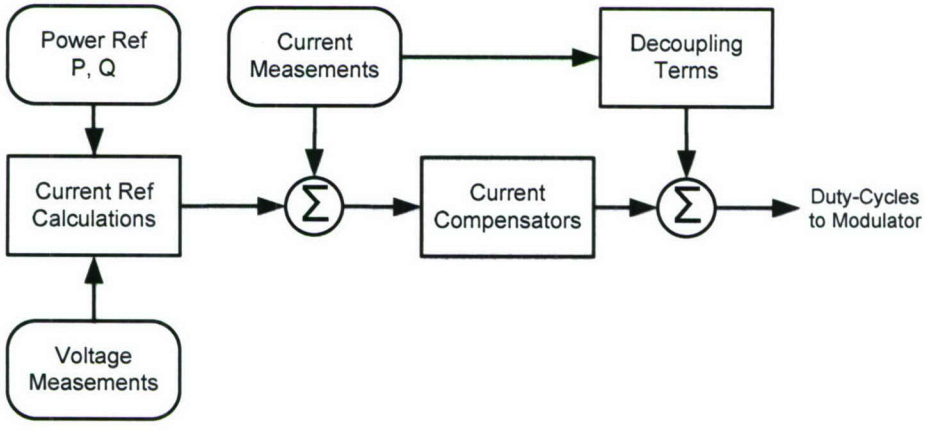


Fig. 9-8 Block diagram of Control during grid-connected mode of operation

During parallel operation with the utility, grid-connected mode, all standards must continued to be followed; therefore the control and system looks and behaves has other classically controlled DG systems. The system was selected to regulate the power flow, between the PCS and the grid as seen in the control block diagram of Fig. 9-8, [5], [10], [11], [12], [13], [14], [22].

Conversely, the islanding mode of operation requires that the control system actively regulate the output voltage of the inverter to guarantee the Area EPS in the nominal operating range. This mode of control operation generates current references via voltage compensation. This form of voltage control allows for current limiting for device and system protection as well as the imbalance and harmonic correction. Fig. 9-9 shows the block control diagram of this islanding mode of control operation [5], [10], [11], [14].

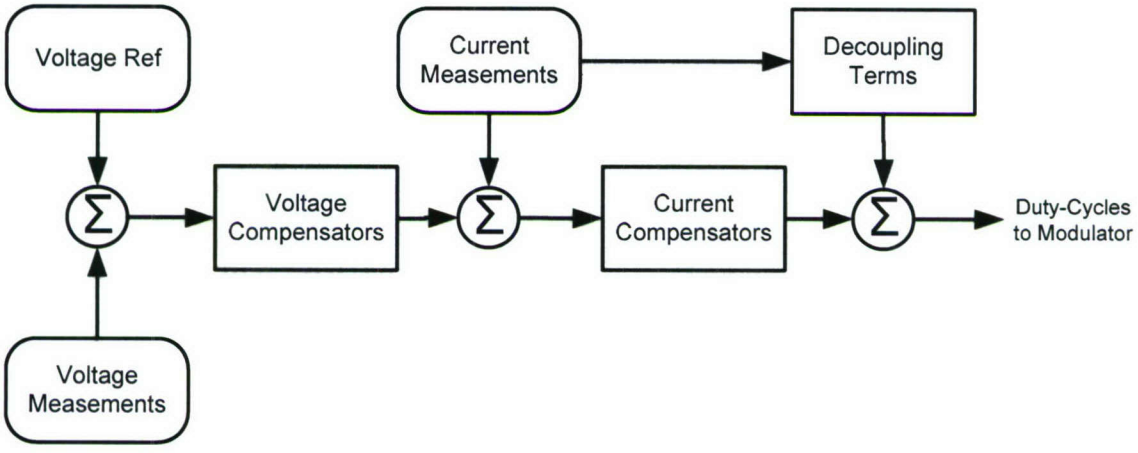


Fig. 9-9 Block diagram of Control during islanding mode of operation

From these two diagrams of the control operation, it is seen that there are similarities between the two modes. If the current reference for the system could somehow be switched between being generated by either the power reference calculations or the voltage compensators then the two could be combined, as of that seen in Fig. 9-10

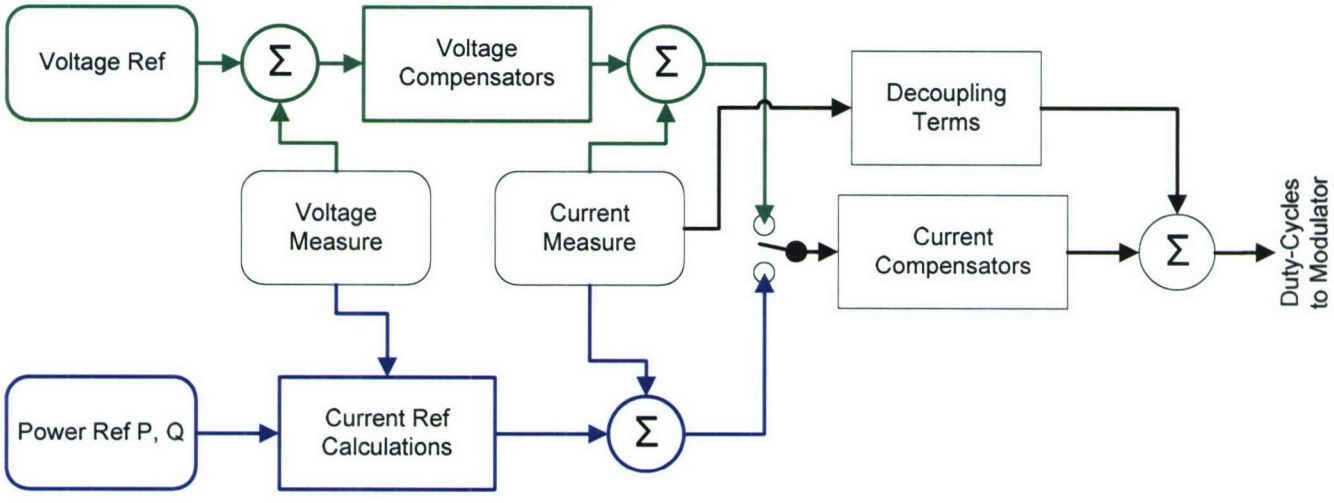


Fig. 9-10 Block diagram of Control for switch-mode implementation

In Fig. 9-8 and Fig. 9-9 it is seen that the two modes of operation can share the current compensators, voltage measurements and decoupling terms. The error signals of the current from the two modes of operation are fed into the current compensator and are connected to a SPDT switch in Fig. 9-10. This

switch regulates what mode of operation the system is running in; if grid-connected mode is needed, the switch will connect the error signal from the power flow path (bottom, blue). If islanding mode is needed, then the error signal from the voltage regulation path (top, green) will be fed into the current compensators. The switch position is determined by detection/re-closure algorithms presented in the next sub-sections.

ii) Detection

As previously described, detection algorithms can be classified as either active or passive. The following scheme is an active one, used not only to determine when islanding events occur and disconnect the system from the utility grid, but also used to govern the control's mode of operation.

The passive element of the active detection can be described by the flowchart found in Fig. 9-11 below.

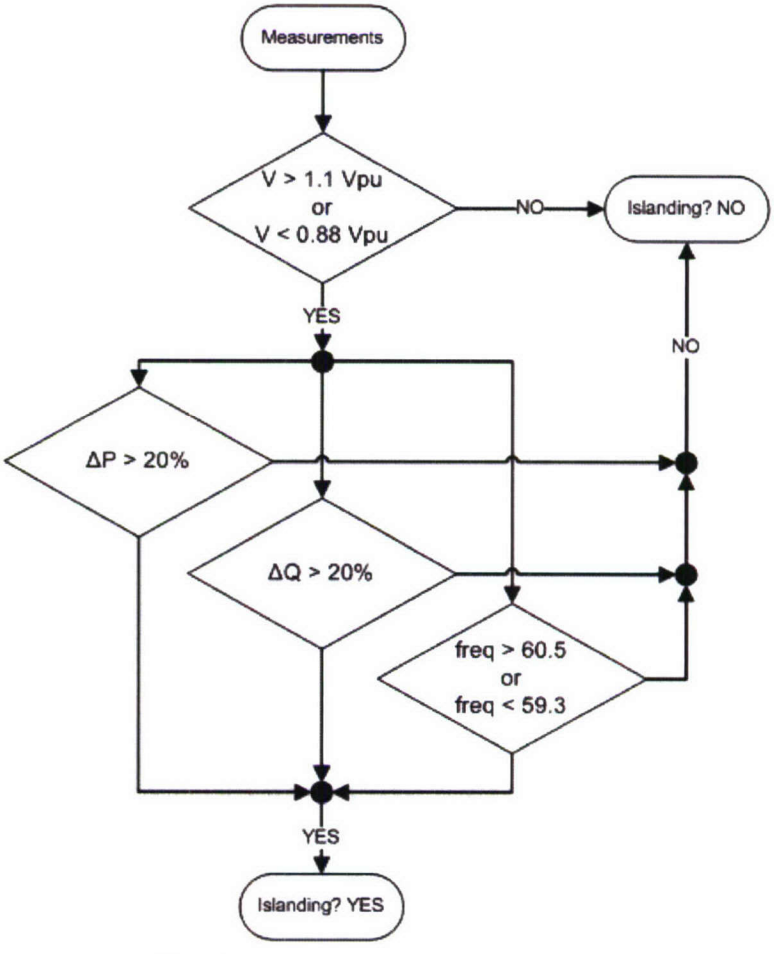


Fig. 9-11 Islanding Detection Flowchart

This passive scheme is enhanced by the active detection that is embedded within the control.

Most active detection techniques continuously perturb the output reactive power by ± 5%, and then use measurements with a passive scheme, [17], [18], [19], [20], [21]. The flaw of these techniques is that their output reactive power needs to be continuously perturbed for the passive detection to be able to detect islanding events. This constant perturbation in the reactive power can have negative impacts upon the system, especially if the DGs are being used to compensate for large amounts of reactive on the utility. This will cause the utility to absorb larger and larger amounts of reactive power, as well as the fact that if many

DERs are connected to the utility then the summation of collective perturbations between each DER system will be very large and undesirable.

The active detection algorithm that is proposed only perturbs the output when there are possible islanding events present upon the utility system. It does this through a Band-Pass Filter (BPF) loop from the voltage measurements within the grid-connected mode control system, seen in Fig. 9-12, [23].

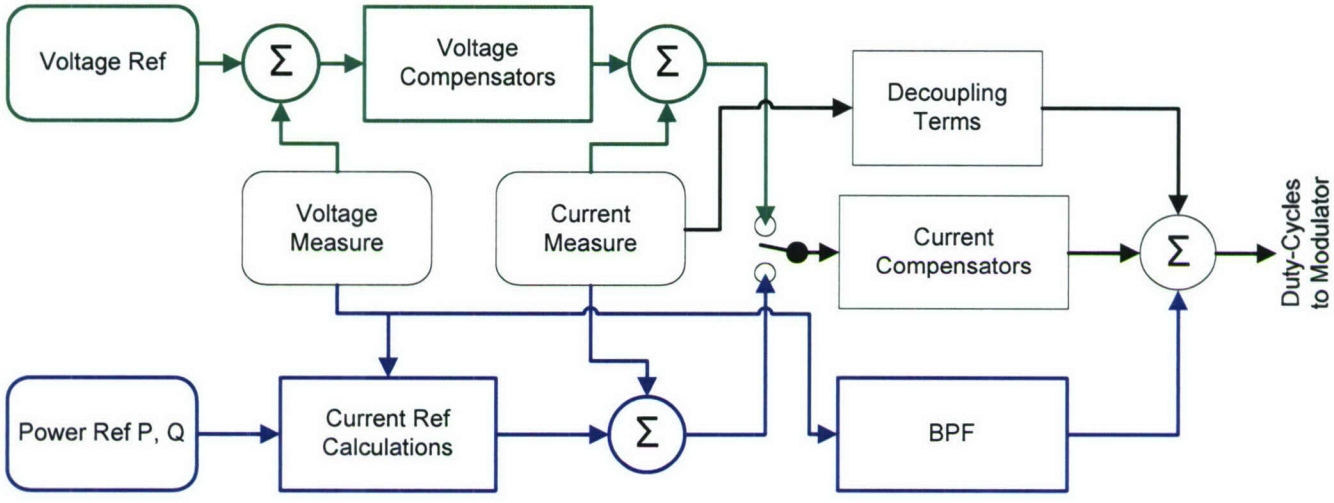


Fig. 9-12 Control System with embedded Active Detection

This BPF has dual behavior, it behaves both as a feed-forward (FF) and a feed-back loop depending upon system conditions. When the system is operating under nominal conditions, the voltage is independent of the output current of the VSI, due to the assumption that the utility is dominant over the PCS and thus regulates the voltage. The BPF loop is therefore a positive FF loop; however when the system experiences an islanding disturbance, the grid voltage in a vast majority of the cases will lose dominance, and thus the voltage will no longer be independent of the current, cause the BPF loop to become a positive FB loop. This positive FB loop naturally creates instabilities in the output, causing the system to leave the nominal operating range, which in turn helps the passive detection identify disturbances, [23].

iii) Re-closure

As outlined previously, to re-close an Area EPS to the main utility there are many guidelines that must be followed, which create undesirable downtimes. The proposed method uses a re-close algorithm along with Phase-Lock Loops (PLLs) to synchronize the voltage of the VSI to the re-established utility voltage. Once the two voltages are in sync, the algorithm makes sure that it is safe to reconnect. With this setup, the Area EPS reconnects to the utility without ever having to de-energize, thus eliminating downtimes needlessly created by today's standards.

The re-closure uses four basic measurements to determine if synchronization is complete and it is safe to reconnect the Area EPS to the utility: VSI voltage, utility voltage, VSI frequency and phase difference between VSI and utility voltage. As long as *ALL* of these fall within a defined set of nominal operating conditions, then the algorithm will deem the system ready to reconnect to the utility. A flowchart of these requirements for reconnection can be seen in Fig. 9-13 below.

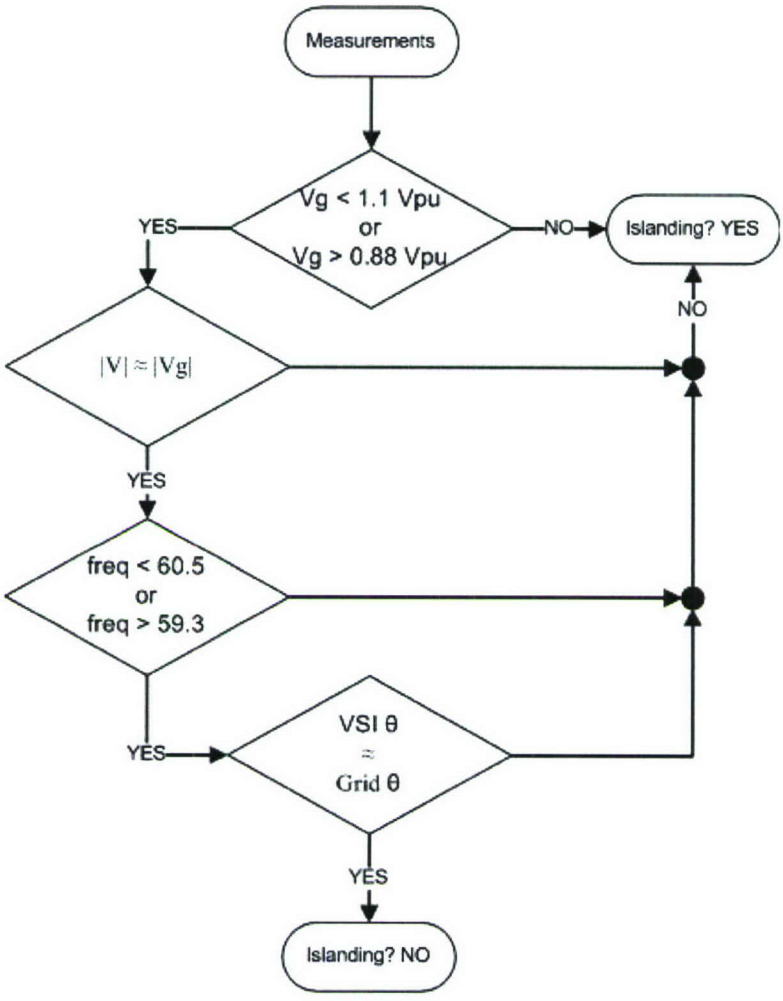


Fig. 9-13 Re-closure algorithm flowchart

The PLLs of the system provide information not only for the re-synchronization of the VSI to the utility, but also frequency and phase information for islanding detection as well. There are two PLLs that are based upon the ABC to DQ0 transformation of the voltage, [24]. PLLs are used to transform the ABC voltages of the VSI and the utility into DQ0 voltages, and to obtain frequency and phase information about the two.

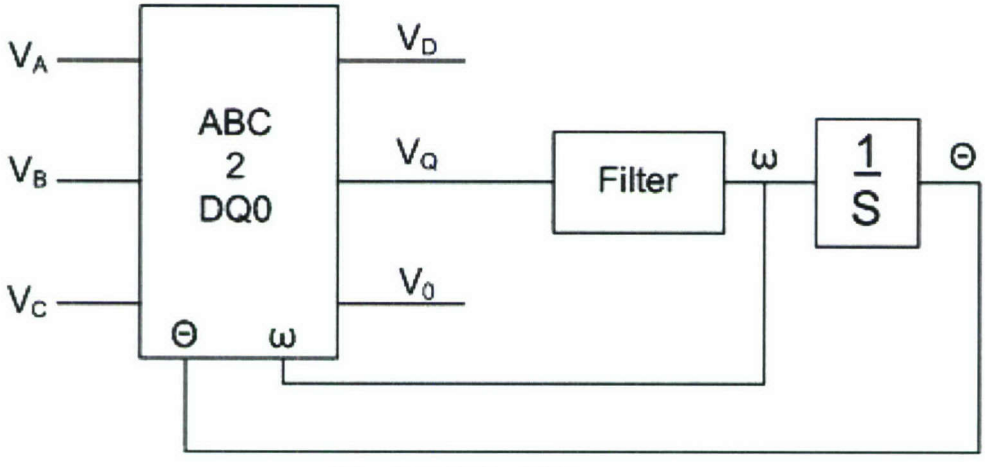


Fig. 9-14 PLL of DG system

In the ABC to DQ0 transformation V_Q ideally equals zero, because of this, we can filter the actual signal to achieve a frequency, integrate that to find an angle, and finally feed the angle back into the transformation (as seen in Fig. 9-14). This will cause the system to track the frequency and provide a phase measurement by forcing the system to make $V_Q = 0$, which will correspond to the proper frequency, [24].

IV. Simulation Results

The generalized system diagram presented in Fig. 9.15 shows the system used in design and simulations. Control design was done in MATLAB's Simulink and SISO toolboxes, and electrical simulation was done in SABER.

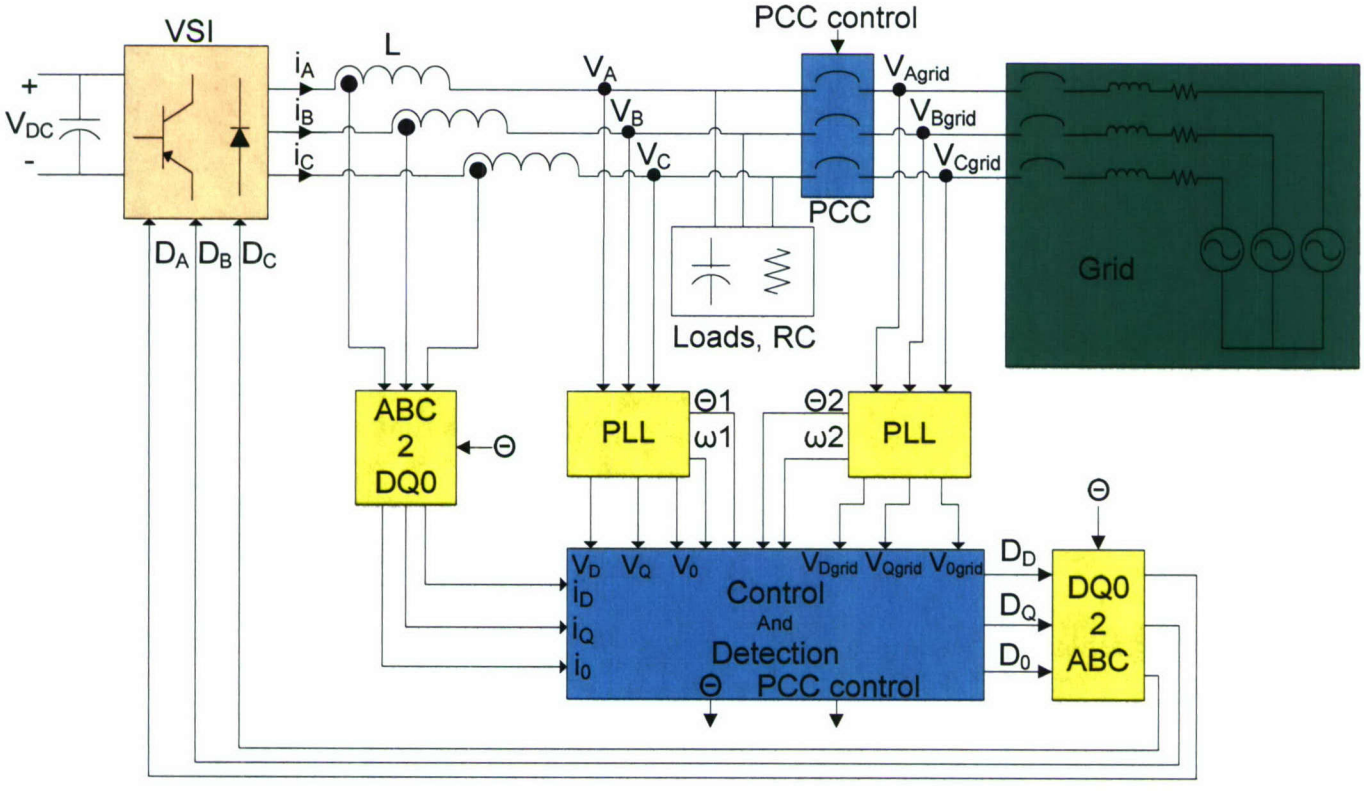


Fig. 9-15 Detailed system diagram used in design and simulations

i) Modeling (Open-Loop Results)

When simulated and compared, the average model derived from the switching model in section III.A above, matches the switching results quite well (Fig. 9-16). This matching confirms that the model accurately represents the switching system, and can therefore be used hence forth in simulations to greatly reduce simulation times, especially for control design and simulation.

In Fig. 9-17 and Fig. 9-18, the open-loop (OL) output currents and voltages (respectively) are shown during grid-connected and islanding modes. These figures clearly show, and reinforce, the need for current/power flow control during grid-connected mode, and voltage regulation during islanding mode.

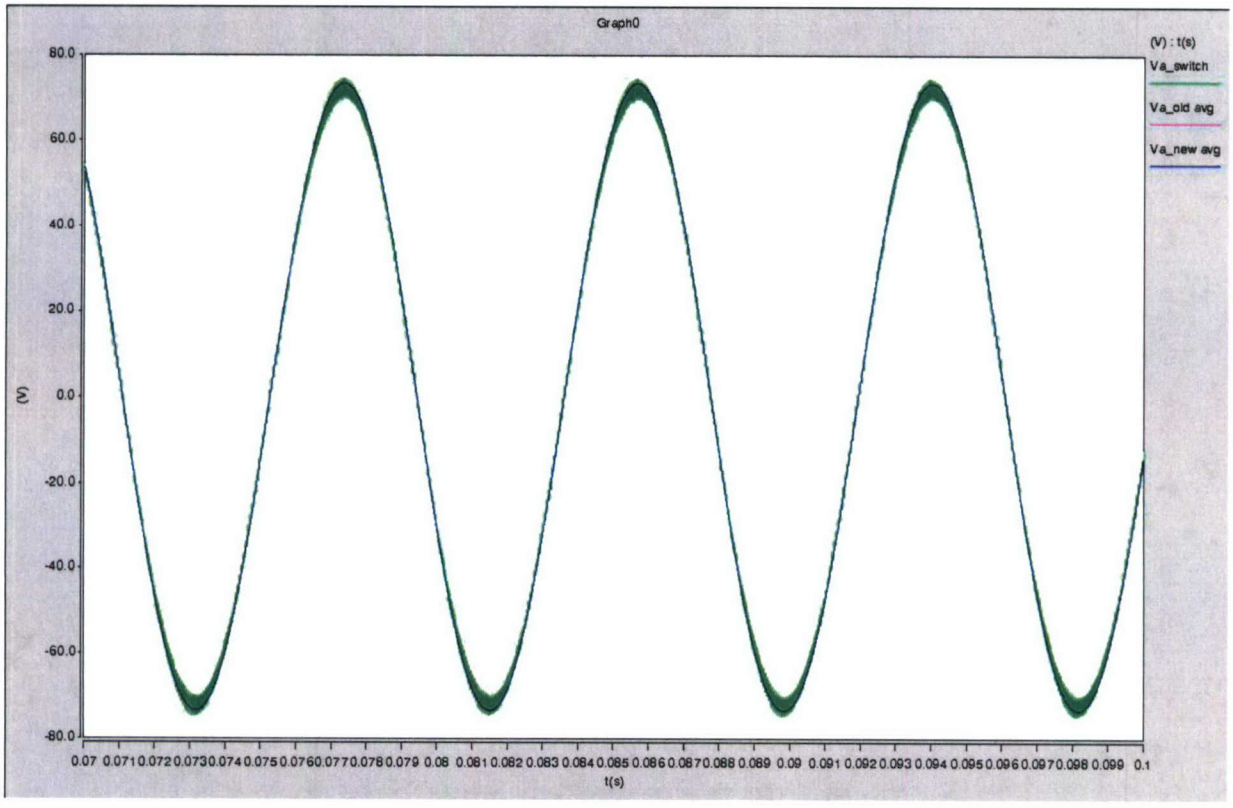


Fig. 9-16 Switching & Average Model output comparison

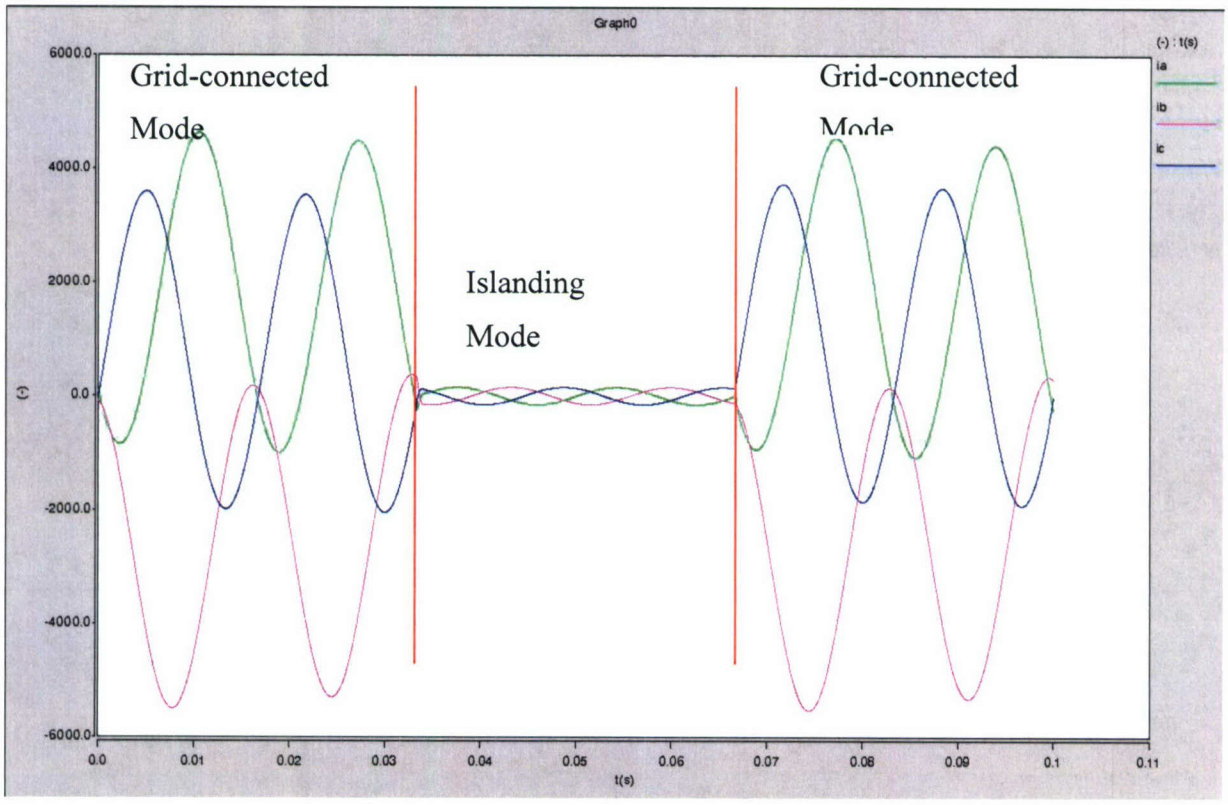


Fig. 9-17 OL Average model output current during grid-connected and islanding mode

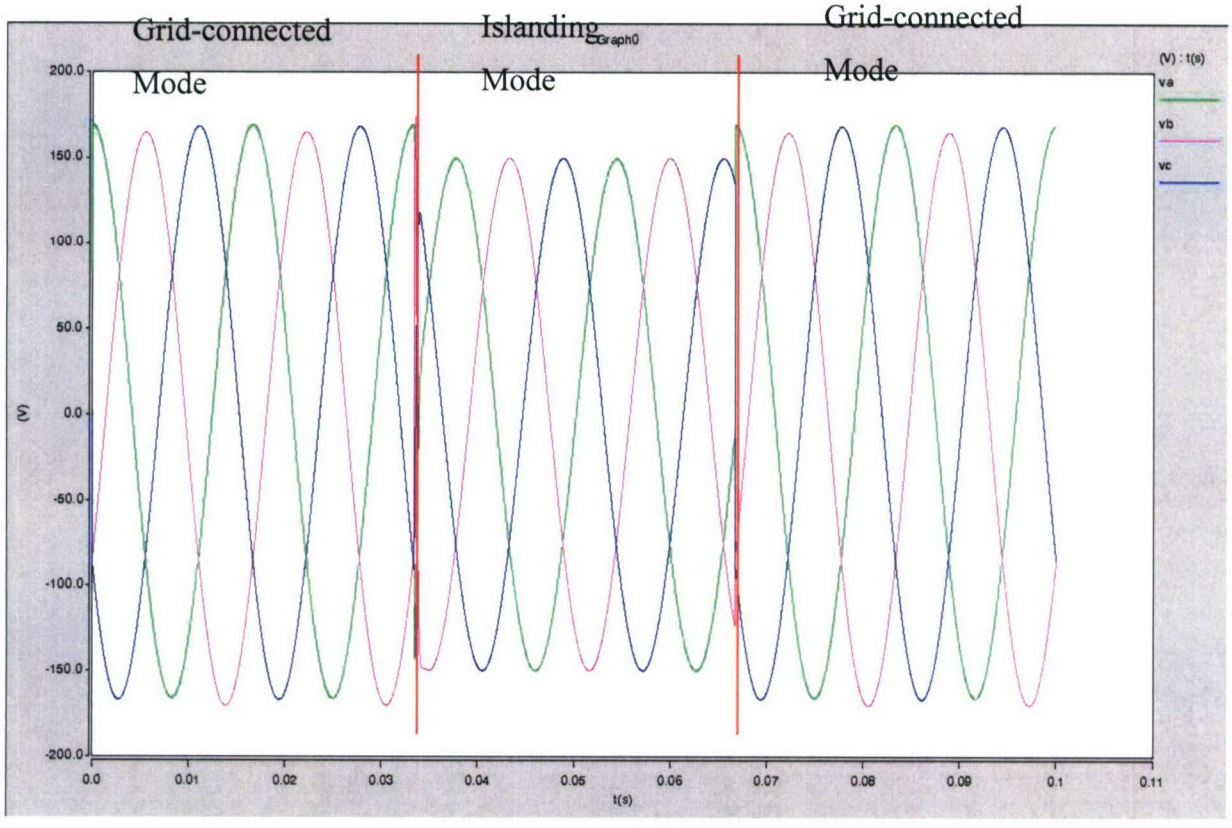


Fig. 9-18 OL Average model output phase voltage during grid-connected and islanding mode

From these results it is apparent that two different types of control are required to implement the DG system with intentional islanding. These control modes and strategies are discussed in the following sub-section.

ii) Control Implementation

As stated above the two modes of operation, grid-connected and islanding modes, require two different control types. The former current regulation, while the latter voltage regulation. To complicate matters further, the grid-connected mode cannot, due to standards, have any type of direct voltage regulation. Because of this the "switched-mode" control was proposed and implemented.

The equations from (5) and (6) were used to create MATLAB Simulink models (Fig. 9-19 and Fig. 9-20). From this model the controllers from Fig. 9-12 were designed.

System parameters:

- Input Voltage = 500 V_{DC}
- Output Voltage = 208 $V_{RMS\text{-}LL}$ (120 $V_{RMS\text{-}Ph}$) @ 60 Hz
- R = 1 Ω (P_{Total} = 43.2 kW)
- P_{VSI} = 20 kW (during grid-connected mode)
- L = 216 µH
- C = 82 µF
- SPWM modulation
- Switching frequency, f_S = 20 kHz

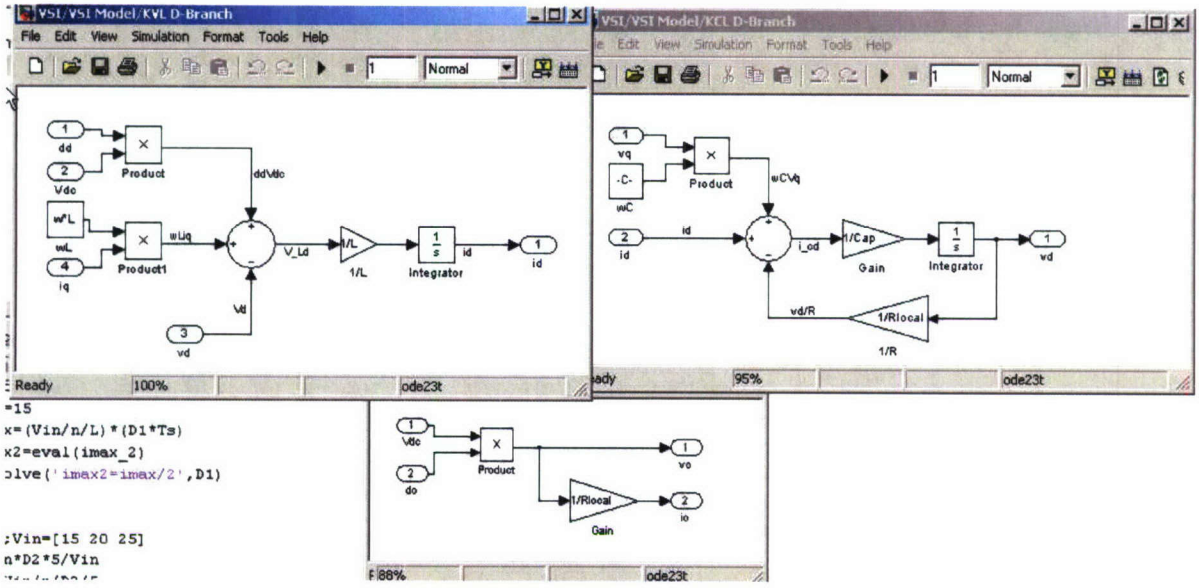


Fig. 9-19 MATLB DQ0 models used for Controller design

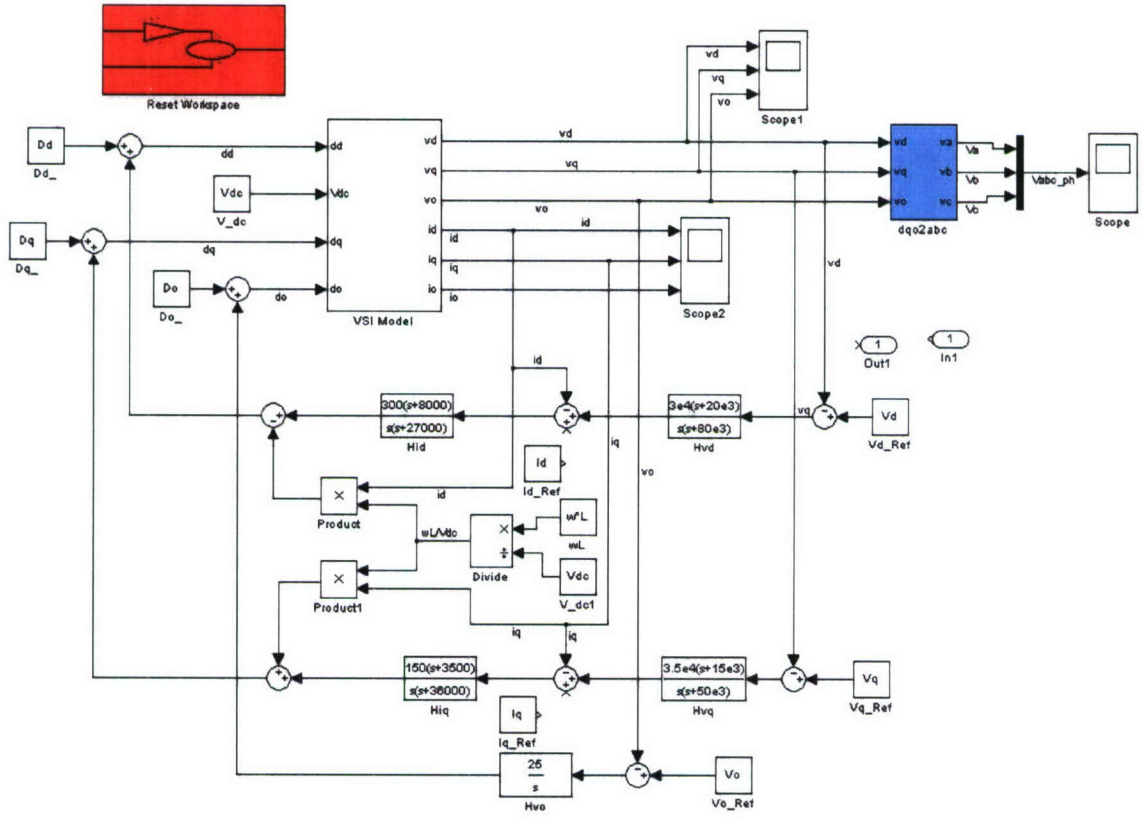


Fig. 9-20 MATLAB DQ0 system showing VSI model and FB control loops

After verification in MATLAB of the controllers' stability, they were transferred to SABER and simulated. The results of Fig. 9-21, Fig. 9-22, Fig. 9-23 and Fig. 9-24 show the control system simulated under forced switched conditions (ie: detection not implemented and islanding event signal that would govern control mode of operation was supplied by user).

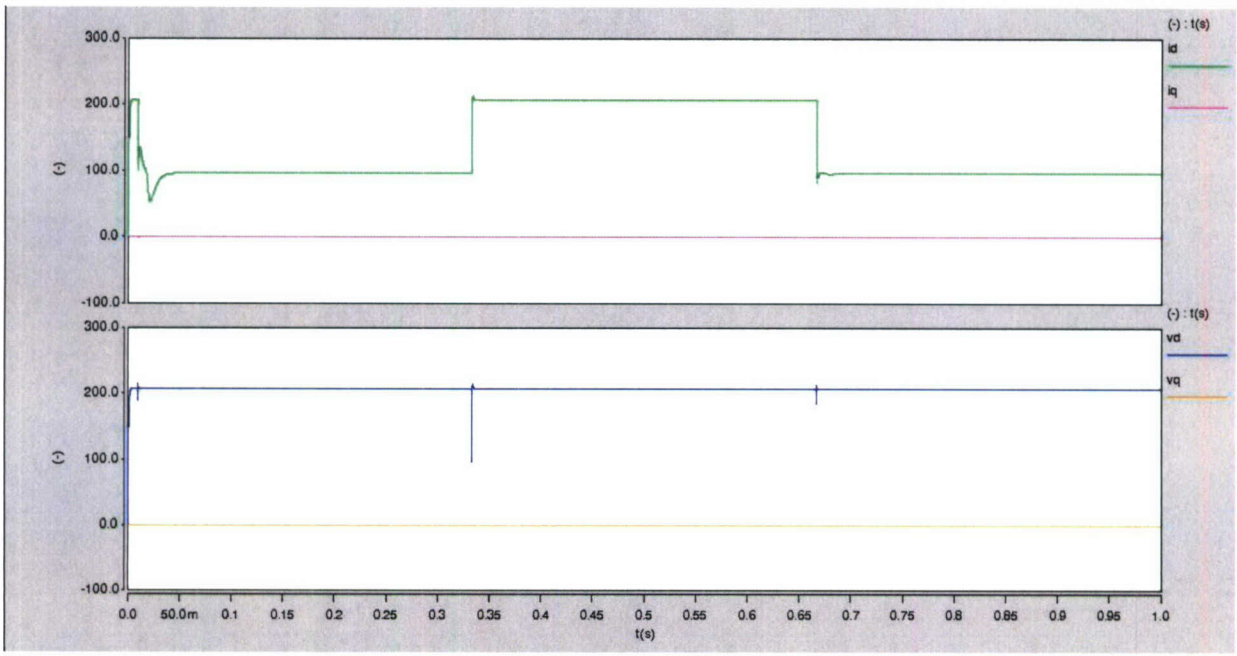


Fig. 9-21 DQ current (top) and voltage (bottom) of the VSI during grid-connected and islanding modes

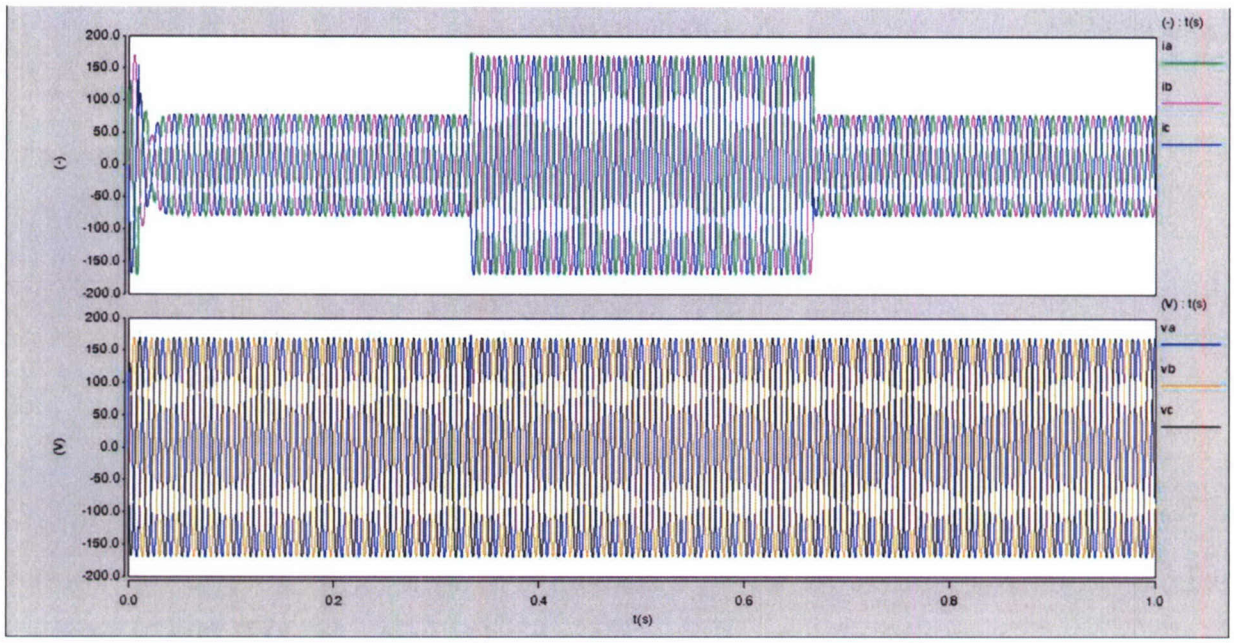


Fig. 9-22 ABC current (top) and phase voltage (bottom) of the VSI during grid-connected and islanding modes

From Fig. 9-21 and Fig. 9-22 it is easy to see that the control during grid-connected mode regulates the current to a set value that outputs 20 kW from the VSI; when an islanding event occurs the system changes to voltage regulation, the current is increased to output the full-load demand of 43.2 kW and voltage is held constant at 120 $V_{RMS\text{-}Ph}$ (V_D = 208 V). Also they show the re-closure event from voltage back to current regulation.

These changes in modes of operation are zoomed in and presented in Fig. 9-23 and Fig. 9-24. From these figures it is easier to see the transient effects of change in the control and system's mode of operation, to which the control minimizes these transient effects.

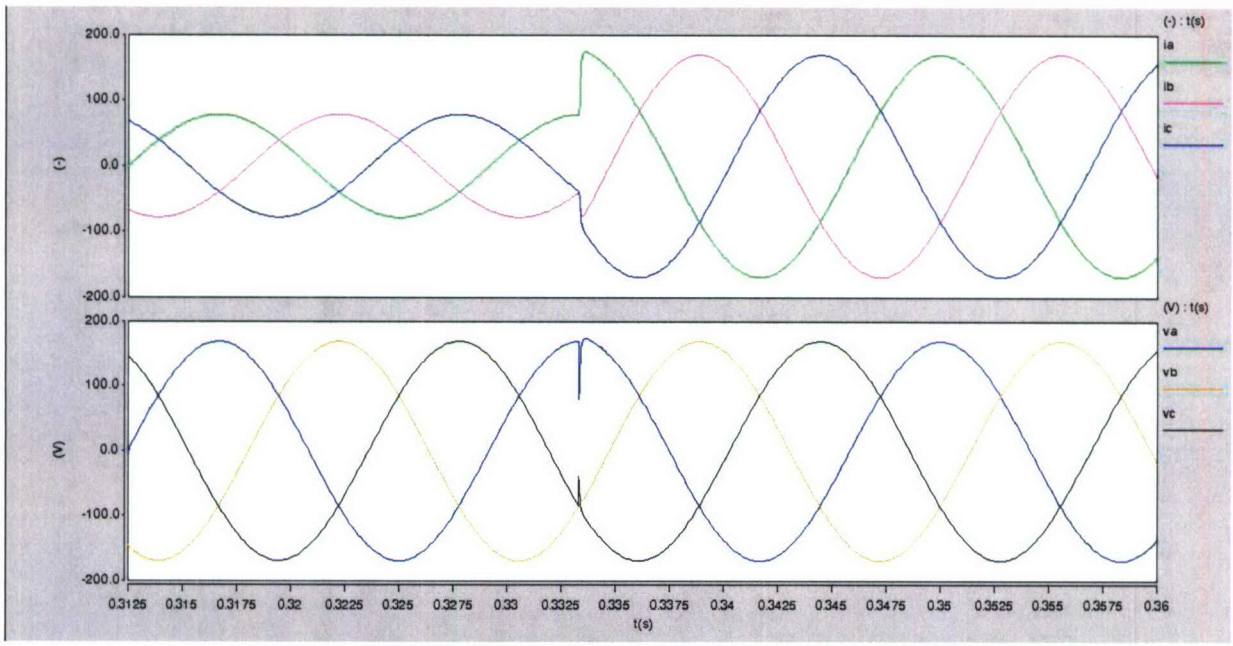


Fig. 9-23 Zoomed in ABC current (top) & voltage (bottom) showing islanding event

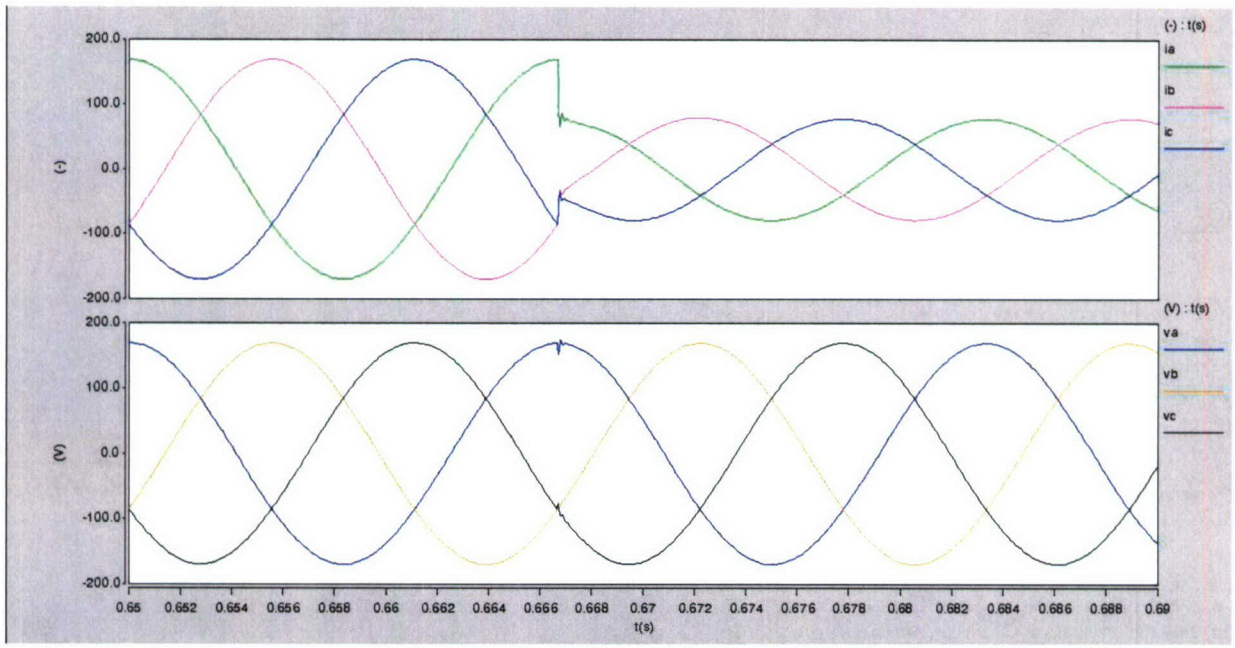


Fig. 9-24 Zoomed in ABC current (top) & voltage (bottom) showing re-close event

From here, detection is added to give the control the autonomy it needs to act independently of the utility and outside control.

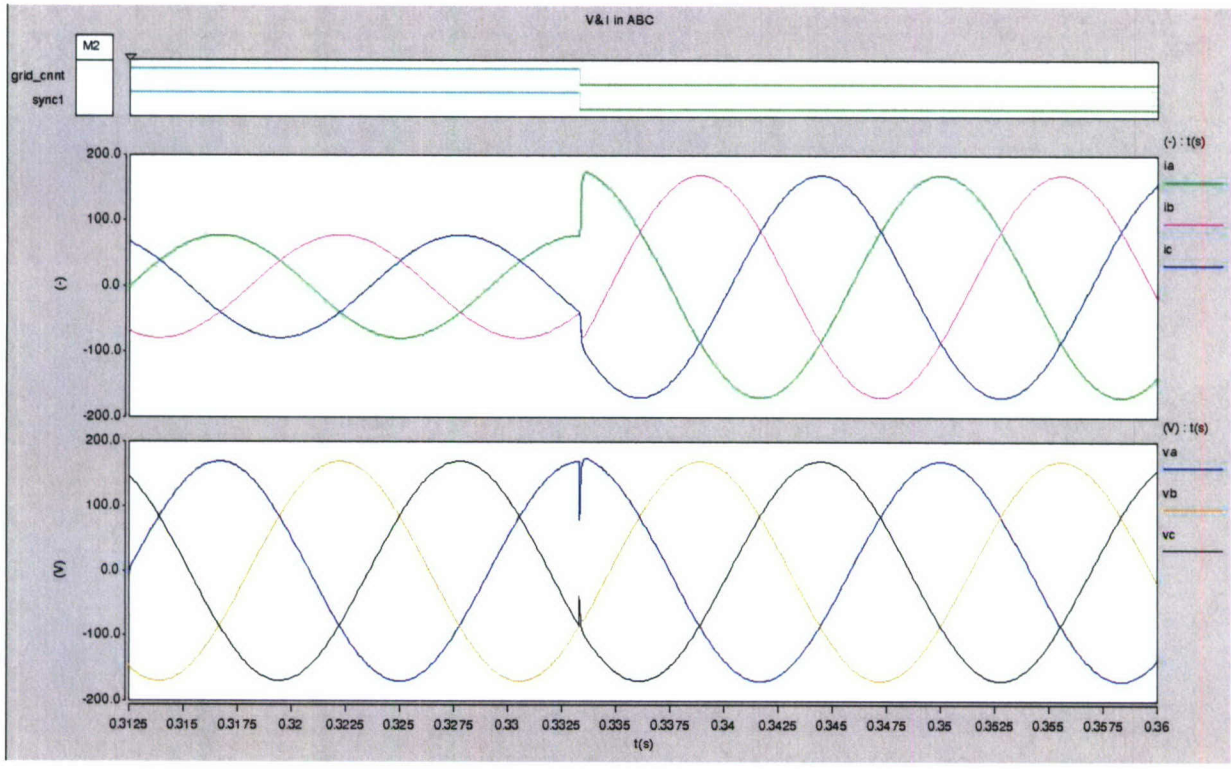


Fig. 9-25 Zoomed in ABC current (top) & voltage (bottom) showing islanding event and detection signal

iii) Detection

When the passive detection component was added to the control system, it was able to detect the islanding event and successfully change from current to voltage regulation, as seen in Fig. 9-25. In Fig. 9-25, at the very top of the figure, there are two logic signals; the first is the user controlled signal that creates an islanding event, while the second is the control signal that the detection algorithm created (logic high = grid-connected, logic low = islanding).

With the passive scheme verified to be working correctly, the active portion of the detection (the BPF) was implemented. The same results as those presented in Fig. 9-25 were obtained.

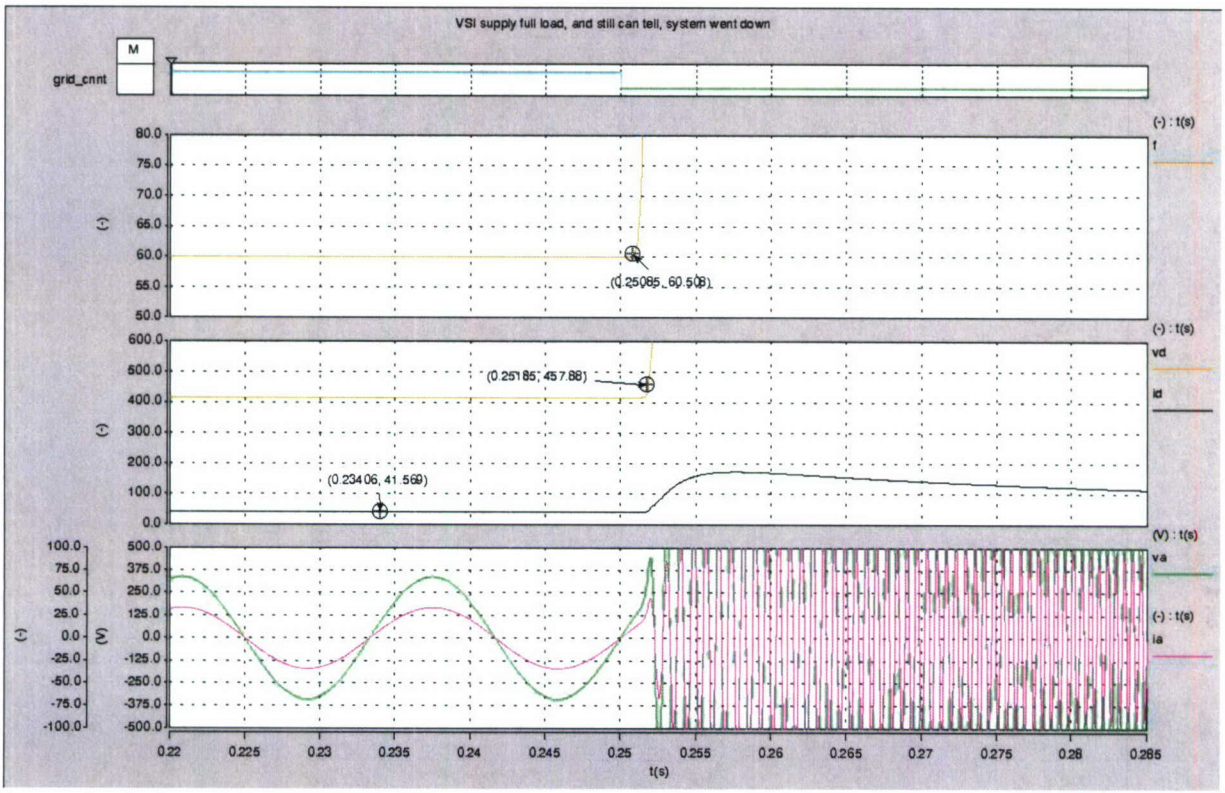


Fig. 9-26 Load-matching test of Active detection for NDZ; frequency (top), V_D & i_D (mid), V_A & i_A (bottom)

An additional test of the active detection was performed under the conditions that the VSI supply full-load demand during grid-connected mode to check that there was not a NDZ. If the output power of the VSI closely matches the load demand, then there is a good possibility that an islanding event will go undetected, because the passive detection cannot see a change from the nominal operating range. The results in Fig. 9-26 show that when the system experiences an islanding event, the positive FB BPF portion of the control loop causes the system parameters to go unstable and thus creating an easily detectable event for the passive algorithm.

iv) Re-closure

When the re-closure algorithm was implemented the results were same as in Fig. 9-24 and seen in Fig. 9-27. Also seen below in Fig. 9-27 are the logic signals, top signal is user controlled for generating disturbances (logic high = grid normal, logic low = grid disturbance present) and bottom signal is re-closure controlled, with the algorithm able to detect when a disturbance has passed and change the mode of operation back to current regulation from voltage regulation.

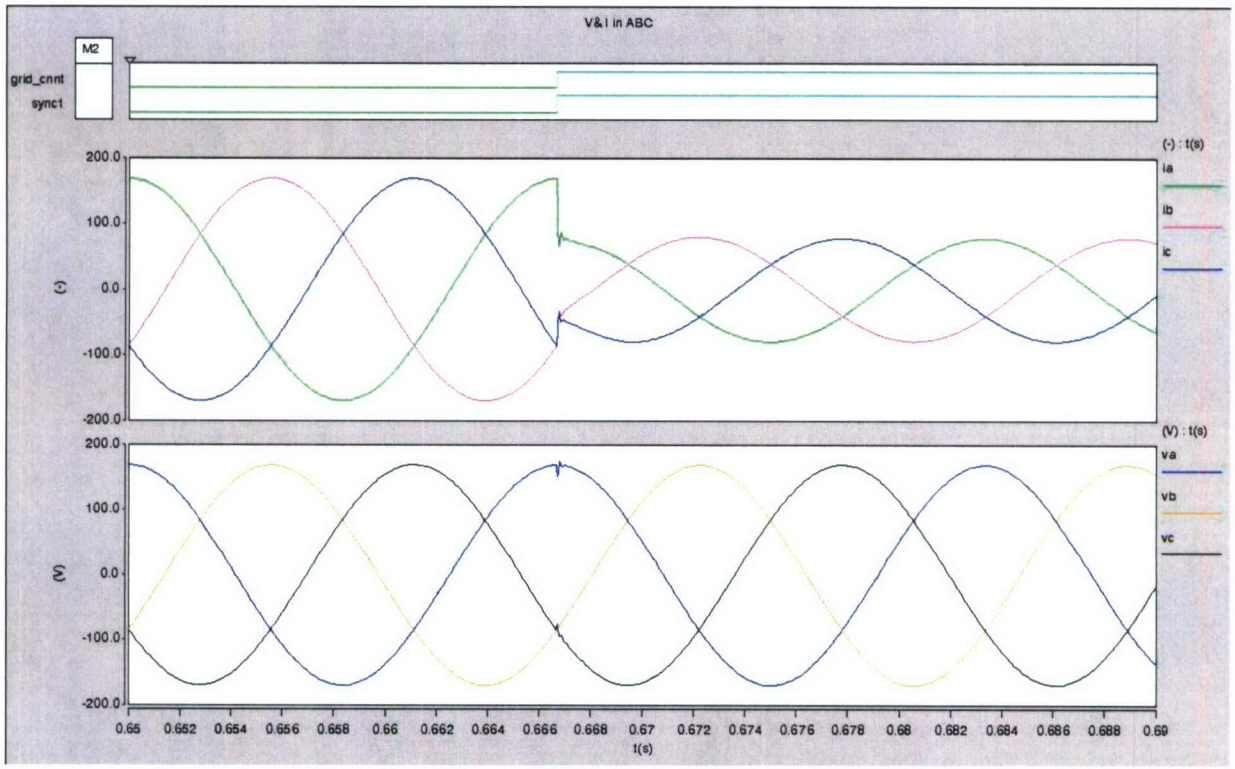


Fig. 9-27 Zoomed in ABC current (top) & voltage (bottom) showing re-close event with Re-close implemented.

Fig. 9-27 used an ideal case in that the VSI system never lost synchronization with the utility. The following show the results of the test performed when after the system switched to voltage regulation, the grid voltage shifted 90° to simulate a loss of synchronization between the two systems. Once the phase shift occurred and the disturbance passed, the PLLs kicked in and re-synchronized the VSI to the utility before re-closure. When the re-closure algorithm was satisfied with the level of synchronization between the VSI and grid voltages, the VSI system reconnected to the utility and the control changed from voltage to current regulation.

Fig. 9-28 shows the re-synchronization of the VSI voltage once the disturbance passed, and other than a brief transient (red circled) when the PLLs start the re-synchronization process, the VSI tracks the grid and then re-closes to it (red line).

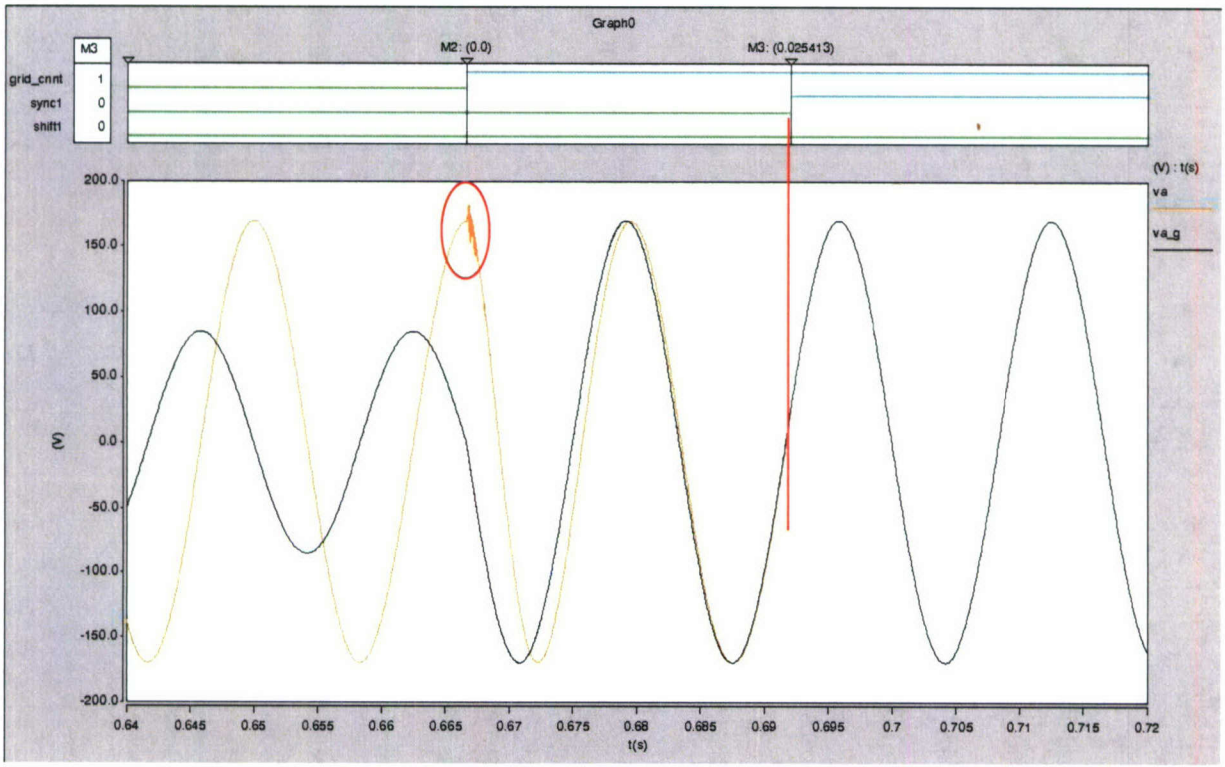


Fig. 9-28 Re-closure showing Phase A voltage of VSI (orange) and grid (black) w/ logic signals (top)

V. Experimental Verification

i) Discretization of Continuous System

The first step in transforming continuous time systems into discrete systems, is to understand the relationship between the Laplace and Z domains. From (7) we see that by a simple expression, a Taylor series expansion, and some algebra the relationship between s and z becomes fairly simple.

$$z = e^{sT_s}, \qquad w/\ T_S = sampling\ \ time$$

$$Taylor\ \ series\ \ on\ e^{sT_s}\ \ gives$$

$$z = 1 + \frac{sT_S}{1!} + \frac{(sT_S)^2}{2!} + \ldots \tag{7}$$

$$looking\ \ only\ \ up\ \ to\ \ the\ \ first\ \ order\ \ terms$$

$$z = 1 + sT_S \qquad \leftrightarrow \qquad s = \frac{z-1}{T_S} = \frac{1 - z^{-1}}{T_S\ z^{-1}}$$

The simple relation found in (7) allows for the continuous time Laplace TFs to be solved for in the Z-domain. Equation (8) shows the Z-domain equivalent of the pure integrator (like the ones used in the PLLs); the other transfer function conversions were found using the MATLAB "c2d" function and can be seen in Appendix C. This program function converts Laplace to Z-domain functions in the exact same manner as (7).

$$f(s)=\frac{1}{s} \xrightarrow{Z[f(s)]} f(z)=\frac{1}{\left(\frac{z-1}{T_s}\right)}=\frac{T_S}{z-1}$$

$$\underline{\underline{f(z^{-1})=\frac{T_S\ z^{-1}}{1-z^{-1}}}} \tag{8}$$

As seen in (7) and (8), the functions are solved in terms of z^{-1}. This is done, because the term z^{-1} corresponds in digital systems as a one sampling period delay. Therefore, when implementing complex TFs and filters, shift registers can be used to simplify the coding. Coding of the TFs and the system in general can be found in Appendix C.

ii) System Conditions

Once the PEBBs connected to one another and the code loaded into the UC and HMs, the VSI system was tested under various conditions (for more details about hardware implementation and test setup see [49, 50]). The system was tested under the following conditions:

- Simulated 40 $V_{RMS\text{-}LL}$, 3Φ @ 60 Hz grid connection, with V_{DC} = 150 V
- Code simulates utility voltages
- Simulated 30% line-sag
- 800 W and 1.3 kW output from VSI during IM
- 1.6 kW total resistive loading

The reason for simulating the utility voltage is to ensure the algorithms and controllers are functioning properly under low-power tests; such that there is a reduced risk of operator and equipment damage if the system fails.

iii) Current Mode and Grid Disconnect

When operating in IM, the system regulated the current to a desired output power level. Fig. 9-29 shows the phase voltage (B and C), the line-to-line switching voltage (V_{CA}), and the output current for phase C, for an output power of 800 W. The voltages and currents are seen to be distorted; this is due to the fact that the device ratings for the PEBB hardware far exceed the levels being applied. When the output power is increased to 1.3 kW (approximately 80% loading), as in Fig. 9-30, the voltages and current become much more sinusoidal (and as seen in the VM of operation the system outputs at full-load demand are even less distorted).

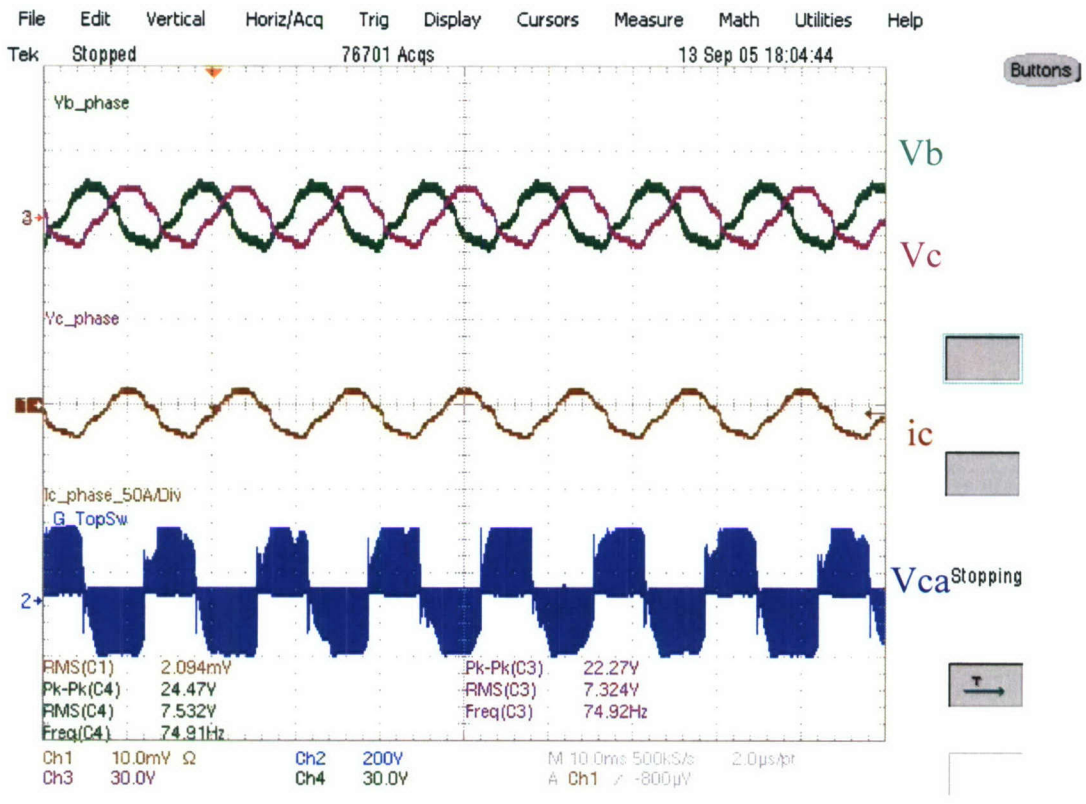


Fig. 9-29: Steady-State operation in IM @ 800W output

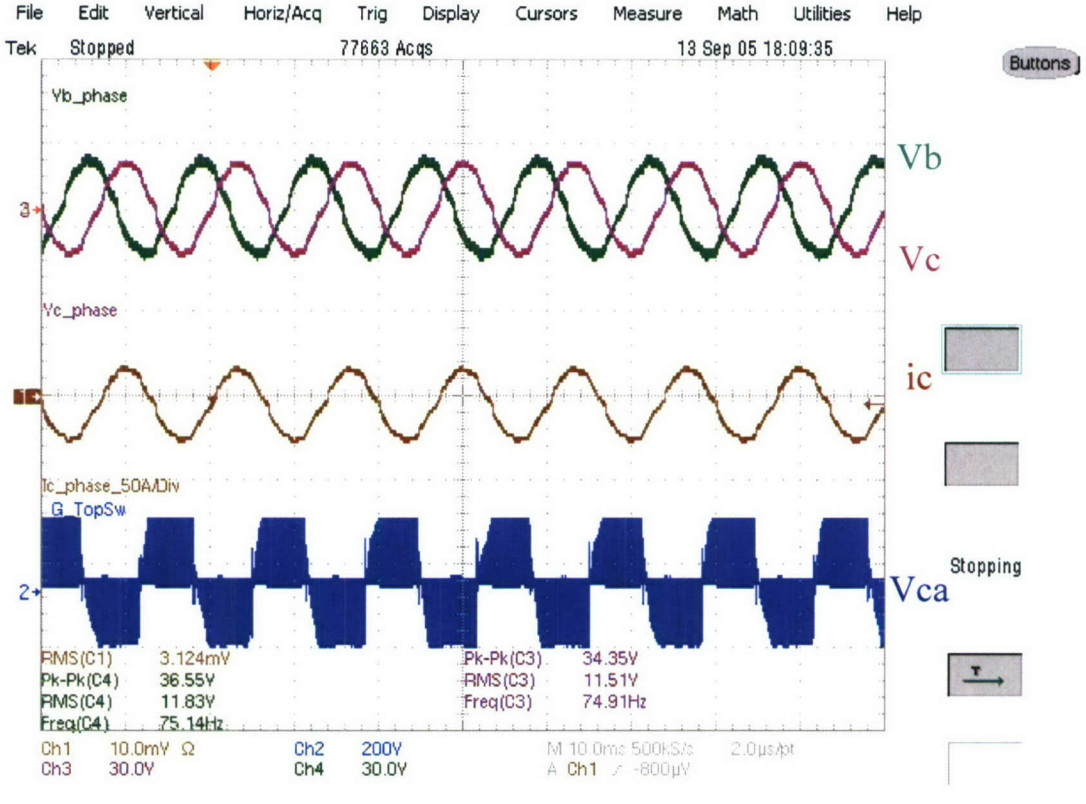


Fig. 9-30: Steady-State operation in IM @ 1.3kW output

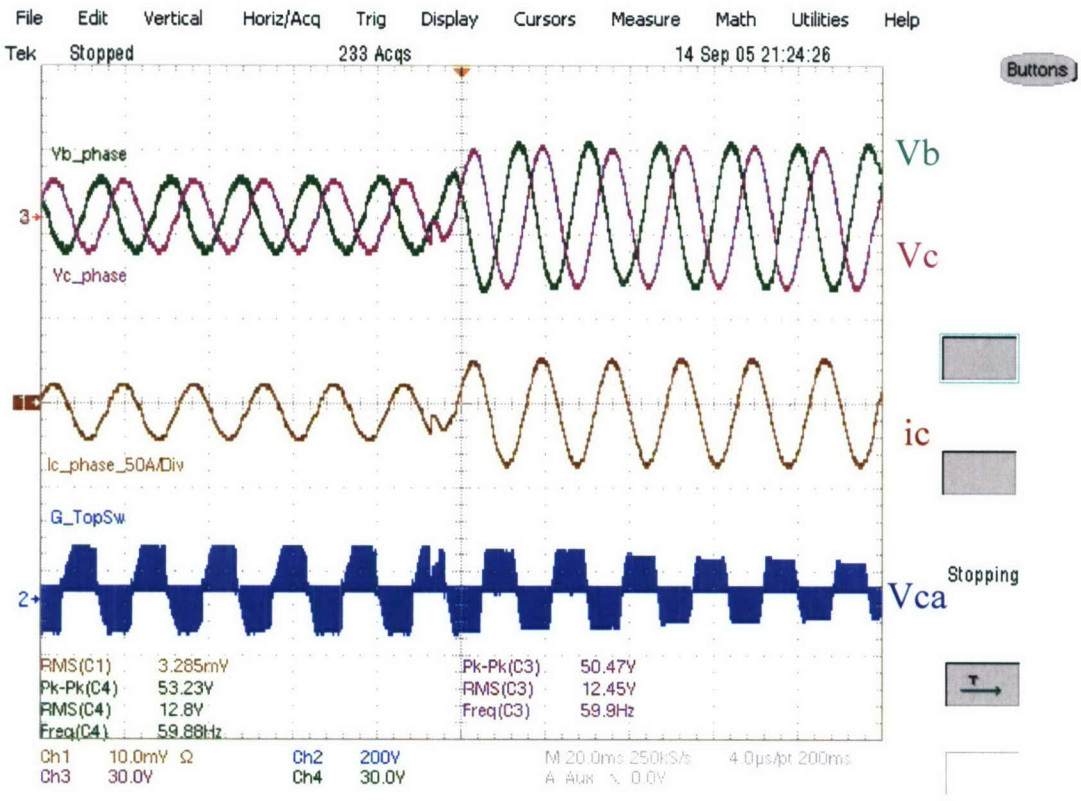


Fig. 9-31: Sensed disturbance with transient from IM to VM

When a disturbance is introduced into the simulated grid voltage, the detection algorithm senses this, and enters the system in the VM of operation. Fig. 9-31 shows the transients of the voltages and current when during the change the control mode of operation.

iv) Voltage Mode and Grid Reconnect

When operating in VM, the system regulated the voltage to the desired RMS, LL voltage of 40V (23.1V RMS, Phase), as in Fig. 9-32. Here it is clearly seen that as the system operating levels are increased, the distortions are decreased. The frequency and voltage angle are shown in Fig. 9-33, taken from the VSI's PLL. It shows the desired constant frequency and saw-tooth signal for the angle; signal ramps up to 2π radians and then resets to 0 radians (this keeps the DSP from creating an overflow error within the code).

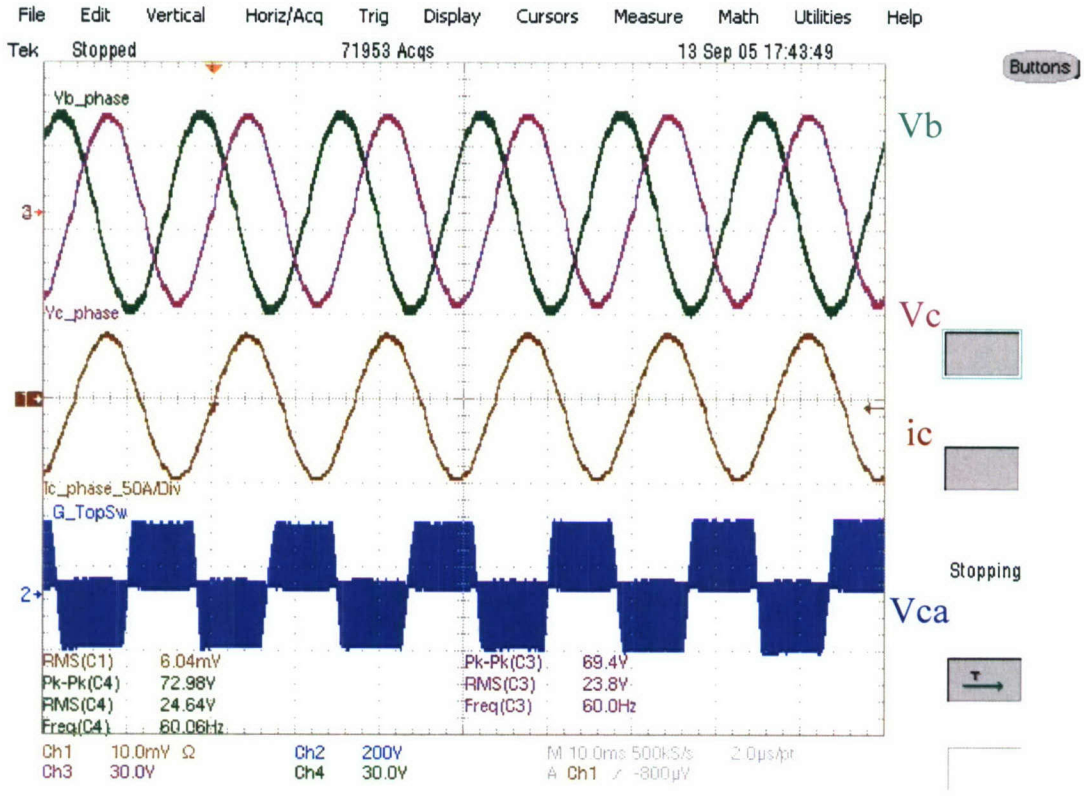


Fig. 9-32: Steady-State operation in VM

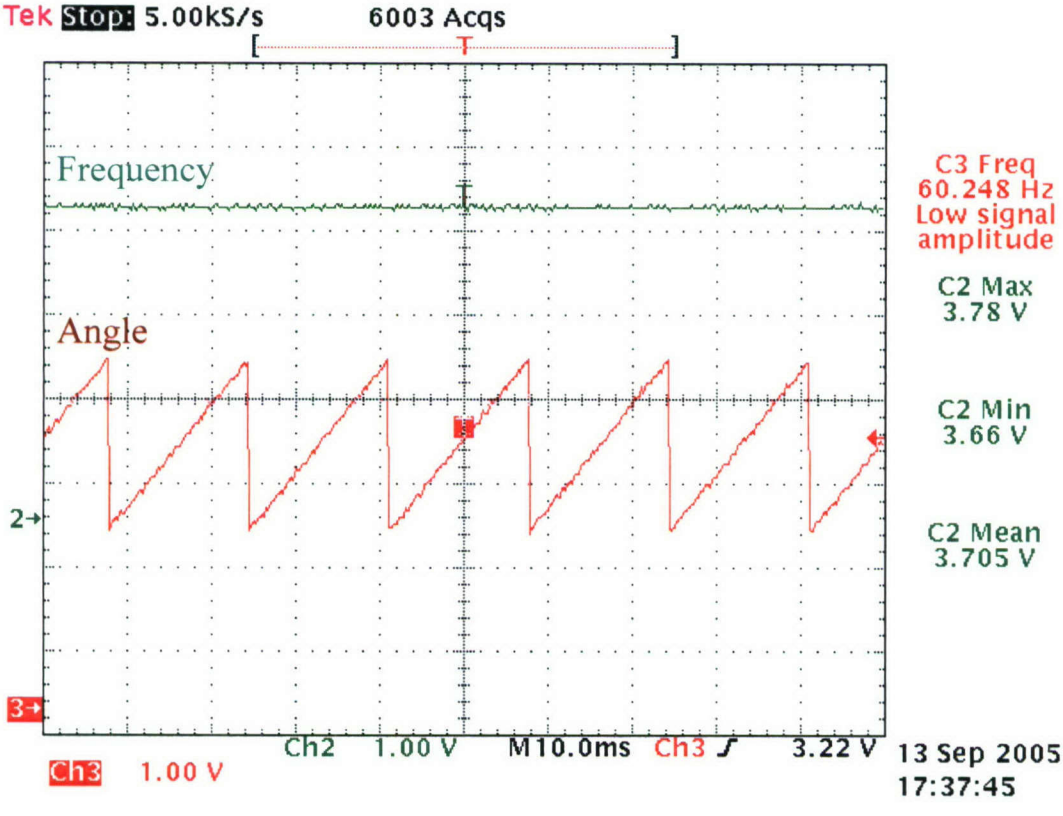


Fig. 9-33: VSI's PLL Angle and frequency during steady-state operation in VM

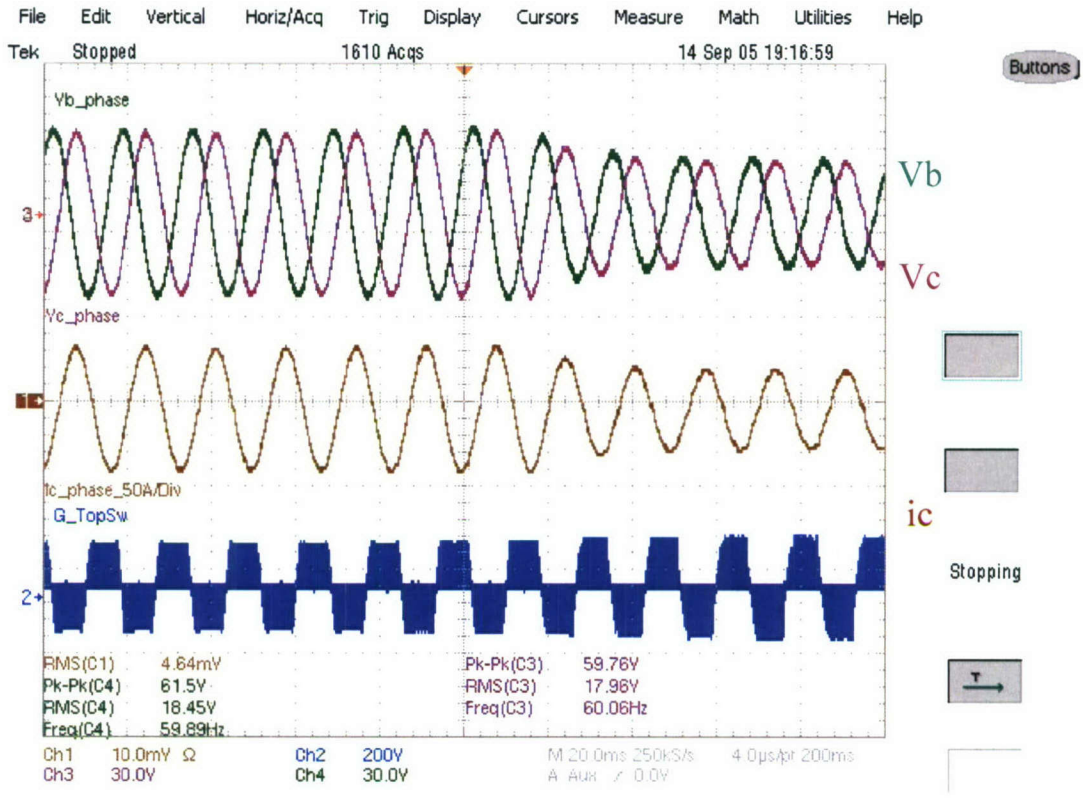


Fig. 9-34: Sensed grid re-established, re-closure transient from VM to IM

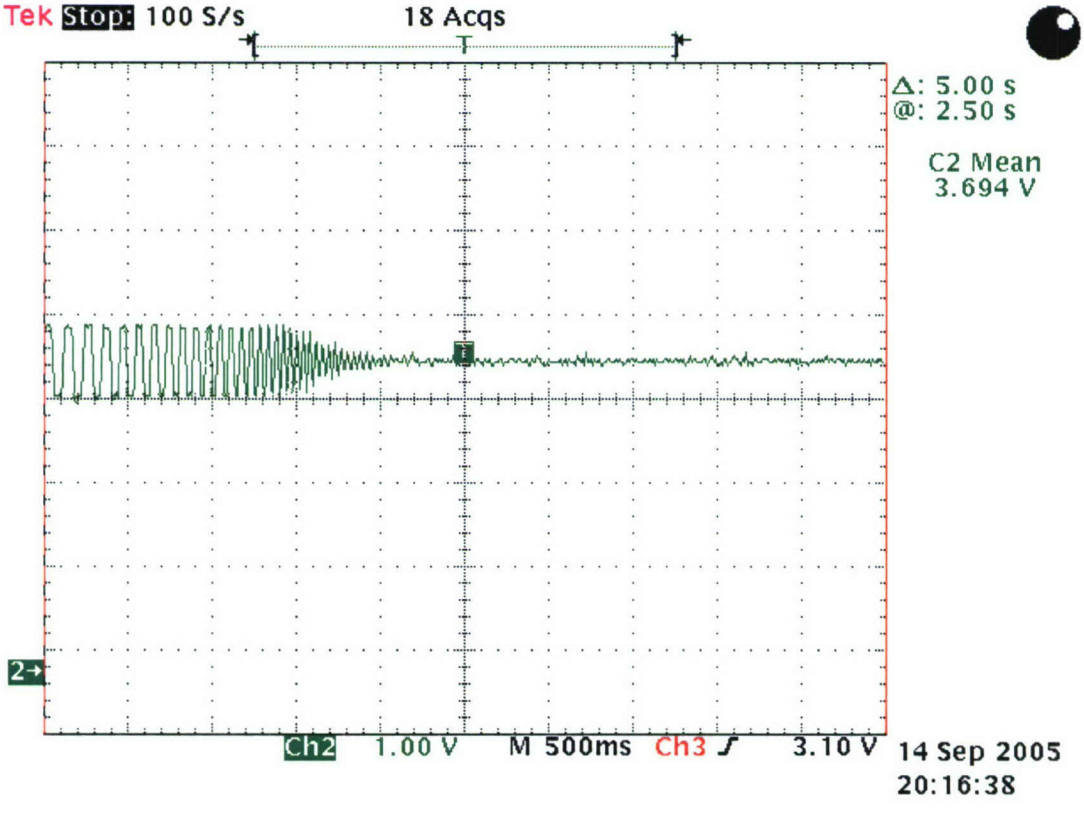


Fig. 9-35: VSI's PLL frequency resynchronizing with grid and ultimately re-closure

The re-closure of the system to the grid is seen in Fig. 9-34; here the disturbance upon the grid voltage equations is lifted, and the system resynchronizes with the grid and ultimately reconnects to it. The

transients from the switch between VM to IM of operation are very nice. The current eases into it's new value with not sudden spikes or other disruptive transients. The frequency of Fig. 9-35 is shown for the period of time the control was resynchronizing with the grid voltage. The frequency oscillates as it catches up (or slows down) and finally settles to the same frequency as the grid voltage; at this point the system re-closes and changes from VM, to IM.

VI. Conclusion

Through this study, the feasibility of DG implementation with an intentional islanding scheme was verified through design, simulation, and hardware experimentation. The switched-mode control, active detection algorithm, and re-closure with PLL algorithms were all designed and tested through simulation.

Table 1 below summarizes various operating conditions and the times it took for each case to either detect an islanding event or reconnect once the disturbance had passed. The detection was tested under the conditions that the VSI supplied half the load demand and approximately full-load demand. The re-closure was tested under various degrees of phase shift; representing the amount of phase difference between the VSI and grid.

Table 1: Simulated Detection (Left) / Re-closure (Right) Times

	$P_{VSI} = \frac{1}{2} P_{Load}$	$P_{VSI} \approx P_{Load}$	±30° Shift	±90° Shift	±120° Shift
Time (ms)	< 0.01	< 5.0	≈ 19.8	≈ 25.4	≈ 25.8

The hardware experiments verified what the simulations predicted would happen. The two modes of control were successfully operated under their respective steady-states, but also the changes between the two modes were showed to be stable and work quite well. The PLL implementation was able to synchronize with an internal signal to the UC as well.

The proposed concepts for the implementation of a DER's PCS connected to the utility system has henceforth been shown to be feasible and that the algorithms tested can successfully distinguish between islanding events and disturbances on the grid. The improvements to the active detection scheme over previous active schemes allow the system to operate more efficiently. These improvements along with the addition of a re-closure scheme bring advantages such as increased grid security and reliability, continuous power supply to Area EPS, and re-connection to the utility while still allowing the Area EPS to remain energized. Also, by having DER's PCS autonomously perform the detection and re-closure, it can not only better protect itself and the Area EPS, but also provides a less centralized control of the power distribution of the grid reducing the chances of utility system wide failures.

Future works upon this subject are to expand the hardware tests by increasing the voltage and power levels, synchronizing with external signals to the UC, and actual interconnection with the utility in lab. Other possible works can include refined or redesigned controllers, more robust protection algorithms, and load-shedding.

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Chapter 10 POWER ELECTRONICS SYSTEM MODELING REVIEW

I. Introduction

Power electronics systems are made of a set of power electronic converters together with other types of electrical equipment. The distinctive characteristic of power electronic converters is the presence of the power switch along with inductors, capacitors, connectors, and other electrical devices. The switch is a complex physical device and so is the mathematical representation of its electrical behavior. When modeling a power electronic converter, the inclusion of all the electromagnetic phenomena can lead to an extremely complex and involved mathematical model. Although the problem has been largely studied and a wide range of models have been proposed to represent the different phenomena, the study and analysis of such complex system requires a large amount of resources. Additionally, the complexity level increases when the system surrounding the power converter needs to be included in order to analyze its interaction with the converter under study. In the case that computer simulations are required, a large amount of processing resources are hence needed. As what is common practice in engineering, when a problem becomes too complicated, a way to make it tractable is sought, and in this case the simplification comes the separation of the main issues. One way to simplify the analysis is by isolating the physical components and/or the issues to study. In the case of modeling, this has been reflected in a wide variety of models that have been proposed to solve specific issues.

All this work and need to solve real world problems has resulted in the development of numerous methods, techniques and modeling strategies capturing the essential information required for the analysis of power converters and the power systems where they operate. The analysis and development of power electronic converters by means of mathematical models has therefore become a standard practice [1],[2]. In this Chapter we present a detailed study and review of models and their modeling techniques, covering from the power system level down to the very switching device. Based on this comprehensive work and analysis, valuable insight and ideas are obtained on the requirements for achieving a better modeling of power electronic systems.

II. Characteristics of Power Electronic Systems and their Mathematical Representation

Power systems are generally represented by an aggregation of the models of the different components present in the system. Based on this fact, power electronic systems can be mathematically modeled by a set of differential, algebraic, and discrete-time equations. The differential equations, which can be linear or non-linear according to the modeling assumptions and simplifications, represent the system dynamics. Initial and boundary conditions are given by the system operation conditions and the physical configuration. The algebraic equations generally represent energy conservation conditions, like power balance. Examples of these conditions are given by the Kirchoff's laws. Additionally, the discrete time equations are present in case that digital control is used. Then, the general formulation can be mathematically written as:

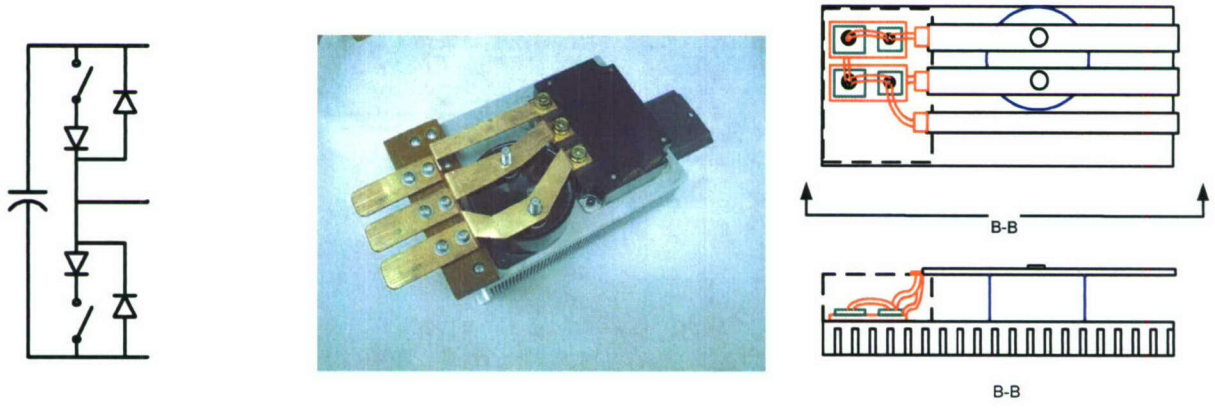
$$\begin{aligned} \dot{x} &= f(x, y, z; p) \\ 0 &= g(x, y, z; p) \\ z_{k+1} &= h(x, y, z_k; p) \end{aligned} \tag{1}$$

Where x are the variables that represent the dynamic of the system, y are the variables defined by the algebraic constraints, z the discrete time variables, and the parameters are represented by p. This formulation is presented in [65].

The characteristic of the sub-set of differential equations is its stiffness, which means that a wide separation exists among the different time constants. This represents an inconvenience when the system has to be simulated in a computer because the time step integration of the complete system equations would need a large amount of calculations. In addition, the functions representing the system can have discontinuities for example when the network topology changes during a fault condition and the consequent disconnection of part of the circuit. In any case, the model structure is generally pretty well known while the knowledge of the model parameters is usually less accurate. This fact has to be considered when the model is being validated.

III. Models of Power Electronic Systems

When modeling power electronics systems, like in other fields, the purpose and solution methods set the model characteristics. A primary classification of models separates them in behavioral and physic based. A behavioral model considers the object of modeling as a "black box" and only represents its behavior seen from the external system. On the other side, physics based models describe the system by the physical laws coming from the materials used, construction characteristics, and ambient influences. Behavioral models are generally simpler, require less simulation resources and at a given range of operation conditions can be accurate enough; but when the range of operation is wide, they generally loss accuracy. Otherwise, physics based models are generally more detailed, complex and therefore more difficult to use, but they represent the object of modeling more accurately in a wide range of conditions [56]. Fig.10-1 (b) shows a picture of a 33kW phase leg with a behavioral model in (a) and a geometric model based on the physic construction. It is worth mentioning that for both model types there a variety of models available. For example, there exist a variety of electric behavioral models based on circuit schematics that have different degree of detail. The model shown in Fig. 10-1 (a) represents only the main components in the phase-leg. Nevertheless, the construction of the physical phase-leg inevitably creates other electric elements that may be undesired and are generically known as parasitics.



(a) Circuit schematic **(b) Phase leg** **(c) Geometric model**

Fig. 10-1 Phase leg (b) and two different models for it. (a) Simple circuit schematic showing the main components, and (c) Geometric model with physical dimensions

The literature on modeling efforts is concentrated in three areas of study: the system itself, the power converter and the single component. In any of these areas, from the physics based to the "black-box" model there are a variety of intermediate models as shown in Fig. 10-2. Considering the phase-leg presented in Fig. 10-1, it can be considered also as a converter (half-bridge). The circuit schematic correspond to a simplified switch model where the device is represented with a piece-wise linear model (on-off). In case this model is used in the model of a system it can provide information on the transient stresses that the converter can produce on other components of the system. There exists a relationship among the types of model being used in anyone of the areas. In Fig. 10-2 the models used at the component, converter and system level must be compatible. The next section presents and describes the different models that have been proposed in these three areas.

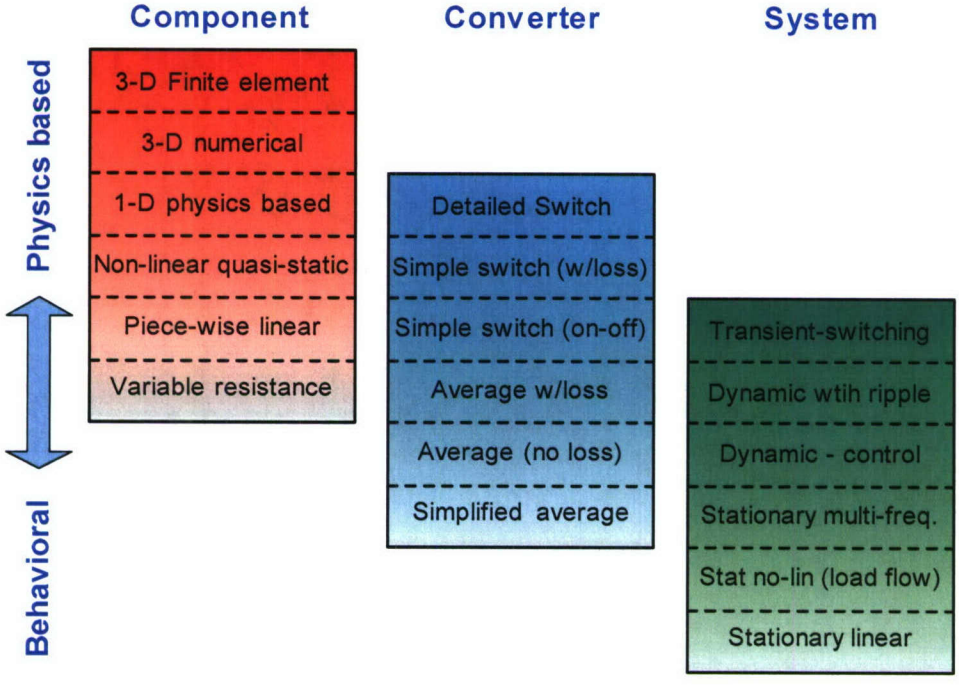


Fig. 10-2 Power device, converter and system modeling classification

III.1. Component models

A. Switch model

The power switch is taken as reference for the single component modeling description. A complete model based on the semiconductor physics uses a three-dimensional representation of the device geometry and solves the set of differential equations of the physical process, like the Poisson and Continuity equations, numerically or by some approximation method [62]. This complete models are many times simplified reducing the equations to the two or one-dimensional case [60]. Simplification of the device equations can lead to further simplified models [61]. Other approaches do not reduce the model dimensions; instead they approximate the spatial behavior simplifying the physic equations [63]. One of the techniques is to use transmission line methods, however, as approximations these methods do not represent the device as accurately as the original physics based methods. A lot of effort in device modeling has been done in obtaining models suitable for circuit simulation.

Non-linear quasi-static is a simplified model that still calculates the total charge in the semiconductor, but do not consider its spatial distribution [59]. This approximation, called the Hammerstein model combines non-linear static plus a set of linear dynamic equations. These models are used when simulation speed and

flexibility in model synthesis are required. Piece-wise linear models are usually good enough to predict the behavior of the power device in the circuit [57],[58]. They can estimate the reverse recovery in a diode and predict some stresses created at the power device commutation that are necessary for snubber design. The simplest case is the ideal switch model where the switch is represented as a varying resistance, which commutes from a very large (open switch) to a very small value (closed switch).

B. Energy storage component model

With the benefits in performance obtained from using higher electric stresses: voltage, current and switching frequency; appropriate models of the inductor and capacitors present in the power electronic converters are needed. Depending on the degree of detail they can be classified in a similar way than the models of the power switch.

Most detailed inductor and capacitor models integrate Maxwell differential equations using finite elements. In the case of inductors the goal is to represent the parasitic capacitances, leakage inductances, and flux distribution [47]. This type of model is used in high-energy-density capacitors to study the electric field distribution, corona effect and changes in the dielectric properties [49]. Simplifying the model, but still considering the electromagnetic equations, the model can become easier to handle. Considering an inductor electric model coupled with the core model, the saturation and magnetic losses in the inductor can be predicted [46]. Simplifying the model, a lumped representation of the passive component is obtained. In the case of an inductor this degree of simplification still includes its parasitic resistance and capacitance. Similarly, in the case of a capacitor it includes the parasitic inductance and series resistance. This type of model is generally used for EMI studies [45],[48]. Finally, the simplest description of a passive element is an ordinary differential equation describing the time domain behavior of the element.

In any of the models discussed an accurate determination of the parameters is important for appropriate results. If the power converter is represented using a lumped model, those parameters need probably to be extracted from a more complex one using a procedure like the one schematically represented in Fig. 10-3. The models of other auxiliary components, like connectors, switches, etc. follow the same pattern regarding the different degrees of detail in which they can be represented.

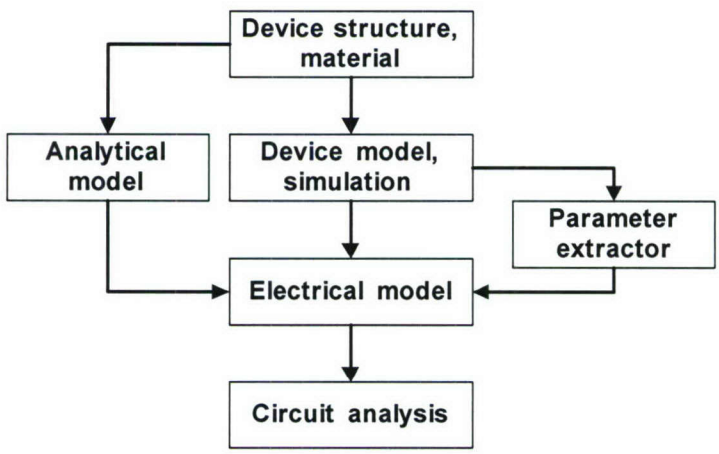


Fig. 10-3 Device parameter extraction for modeling in a circuit simulator

III.2. Power converter models

A. Switching models

A type of detailed models of power electronic converters is used to study EMI. Accurately modeling EMI noise generation and propagation in power converters is the first step to predict and manage the EMI noise in the system. Recent research shows that the switching power modules are the noise emission sources [116]-[124]. Two basic approaches have been used to characterize and model conducted EMI noise sources: device physics-based model [116]-[118] and device behavioral model [119]-[124]. The device physics-based model requires intimate knowledge of the device structure and device physics mechanism, such as carrier concentration and lifetime. It is cumbersome to apply this method in power electronics systems, since it is difficult and time-consuming to model all the devices in the system. It is also not suitable for a parametric study of the system because of the modeling process. The behavioral device model is widely used in the prediction process because of its simplicity. It is an equivalent circuit for the EMI noise emission. Some of the behavioral models can simulate EMI noise in frequency-domain, which can reduce the simulation time dramatically. The drawback of this behavioral modeling method is the poor accuracy for the entire frequency range (150 kHz -30 MHz), and the difficulty in using a single model to predict the EMI noise for the system with variable operating conditions, such as DC-AC converters. The other drawback of the behavioral models is that it is difficult to model the impedance of the device, such as wire-bonding inductance and device output capacitance, which will significantly affect the high-frequency EMI noise. For the noise propagation, there are two basic methods: 1) Mathematics-based models [119]-[120], and 2) Measurement-based models [121]-[126]. The finite element analysis (FEA) is widely used to model EMI noise propagation path. The advantage of the mathematics-based method is that it can obtain path parameters before the entire propagation path is built up. However, some of the components' characteristics are very complex and need not be simulated, for example, commercial electrolytic capacitors. The measurement-based method includes measuring individual component parameters and path network characteristics. For large power converter systems, this method is difficult to use since it is almost impossible to measure every component impedance in the system. The converter-level EMI model is the combination of different noise generation and propagation models.

B. Average models

The utilization of averaging in power electronics was reported for the first time by Wester and Middlebrook [5]. They proposed to average the duty cycle over a switching cycle and justify their approach from the fact that in a well-designed converter the time constants of the circuit involved are greater than the switching period. This is schematically represented in Fig. 10-4 with the presence of the low-pass filters connected at the input and output of the switching network. The result of the averaging process is a continuous model that neglects the switching action but keep the slow non-linear behavior of the converter. These models can be linearized around the operating point allowing designers to use all the linear system theory tools for control design and asses the stability of the converter under small perturbations. After [5] different averaging techniques were developed and can be classified as: state-space average [6],[7], circuit average [8], switch average [9],[10], and generalized average [11] which in essence will lead to the same average model [12].

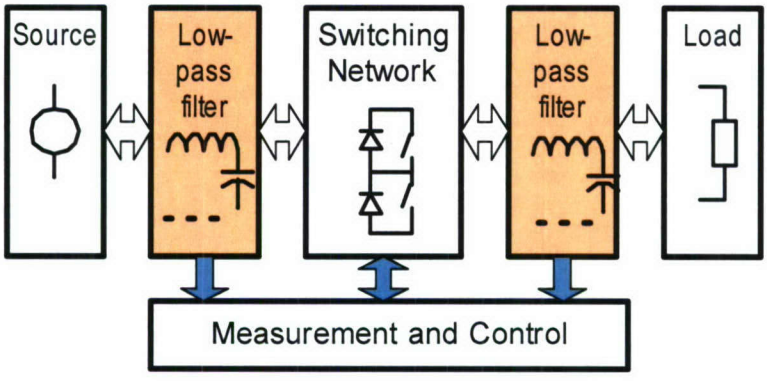


Fig. 10-4 Power electronics converter schematic

The switching circuit in Fig. 10-4 can be described by the two sets of differential equations. The first one corresponds to the circuit with the device switch being open and the second describes the circuit during the switch conduction time.

$$\dot{x} = A_1 x + B_1 v_g \qquad 0 \le t \le t_{on}$$
$$v_0 = C_1 x$$
$$\dot{x} = A_2 x + B_2 v_g \qquad t_{on} \le t \le T_s$$
$$v_0 = C_2 x$$

The next step in the process of developing average models was to include the effects of variables that affect the real behavior of the converter but were neglected during the average process. Those models are described in the next paragraphs.

i) Unified discontinuous conduction mode and continuous conduction mode average model

Initially Average models were differentiated between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) even though it was known that DCM model is a general version of CCM models [6],[9],[10],[13]. Hence unified representations were proposed in order to model cases like power factor correction (PFC) circuits were the converter works between these two modes of operation [15],[16].

ii) Average model with ripple estimation

Krein and Bass [17] took the theory developed in [18],[19] and gave a mathematical justification of averaging in power electronics. Their work confirmed the theorems presented in [19] and proposed a methodology to recover the ripple information from the average values. The ripple estimation allow designer to obtain information about currents and voltage ripples without the need for switching simulation [20].

iii) Frequency dependant average model

As mentioned above average model give very good approximation to the behavior of the original circuit when there exist a time scale separation between the time constant of the power stage and the switching time period. However, this dependence is not explicit in the models. And when used in cases with high

ripple condition, the regular average model fails to predict the evolution of the system. Hence, average models that depend on the switching frequency were proposed in [21]-[23].

iv) Average models with current control

By controlling the current and the voltages was possible to improve the dynamics of the converter; especially for those topologies with a zero in the right half plane [24],[25]. Also, it makes easy the study of paralleling power stages and very well suited for converters which must draw sinusoidal input current from an ac power system. Today the most used techniques to control the inductor current are peak current, average current and charge control.

The first average models for converters under peak current control were accurate at low frequencies [26],[27]. But they were not able to predict a sub-harmonic instability for duty cycles above 0.5 [28]. Ridley [29] propose a model that combines a simplification of the sample-data models with the three terminals switch model that is valid until half of the switching frequency and can predict sub-harmonics instabilities. Based on the same idea a state space model was presented in [30]. And a so-called unification of the models was proposed in [31]. Average models were also proposed for average current mode control and charge control [32]-[34].

C. Discrete models

Discrete models do not attempt to transform a switched-mode converter into a continuous one; rather, the system is described in terms of a sequence of samples, one per switching cycle. Researchers thought that discrete models were the best modeling approach, because of the discrete nature of the power converter [35],[36]. Hence, the converter is represented by a difference equation that is non-linear and time invariant. Then, after linearization around the operating point a small signal discrete models is obtained. The idea is represented in Fig. 10-5.

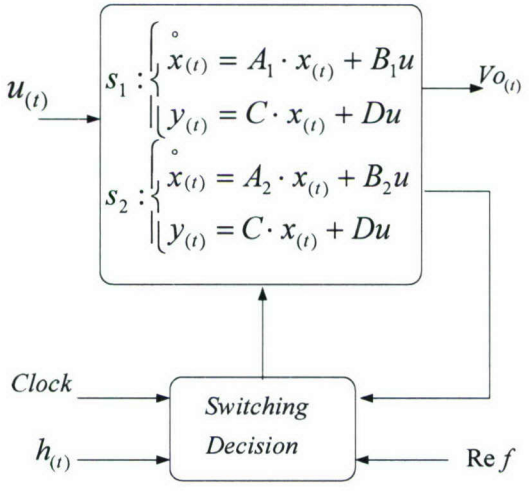


Fig. 10-5 Discrete time modeling of a power converter

The small signal models obtained using discrete methods are more accurate at high frequencies than average models and predict the instability of the converter under current mode control for duty cycles greater than 0.5. Even though, the notable accuracy of this models they are not very much used because

designers are not accustomed to discrete models and the dependency on numerical methods do not give any insight on the behavior of the converter. Hence, simplified discrete models called sample data models were proposed in [37],[38].

Sample data model, which is basically a combination between continuous average models and discrete models, is the one that has evolved and is used currently for digital control design of converters [39],[40].

Today more attention is given to discrete models because they are very well suited to study nonlinear phenomena in power electronic circuits. For instance, phenomena such as bifurcation, limit cycles and chaos can be predicted [41],[42]. This is not possible using average models. Besides, since discrete models describe the evolution of the state variables sampling the state variables, tools like Poincaré maps and stroboscopic map can be used [43],[44].

D. Thermal Models

Today efforts of increasing the power densities found a big challenge in how to dissipate the heat generated by the switching devices especially because over-heating is one of the principal causes of failure in semiconductor switching devices [50]. Hence, is important to understand the thermal effect on the switching elements and have models that help designers to identify hot spots during the design stage. Basically two models are used most frequently.

Finite elements: it is a three dimensional thermal simulation that is able to model steady state and transient heat transfer and parametrical studies. Complete geometrical description of the package and type of material used is needed in order to build the model [51].

Electro-thermal network: The mathematical representation of the heat flow in one dimension is the same as a lumped parameter Resistance and Capacitor network. Where the current in the circuit represent the power loss and the voltage in the capacitor represent the temperature in that layer [52],[53]. Usually, this model is obtained directly from the finite element software or from the geometry and materials of the package.

III.3. Power electronic system models

This section focuses the analysis on models of systems that process electric energy using power electronic converters. A wide range of systems is included, which comprises from energy transmission systems using FACTS devices to computers. Traditionally the models proposed to study the behavior of such systems are an aggregation of the individual models [64]-[66]. The set of equations describing the whole system is composed of the linked equations of the individual components including initial and boundary conditions.

A. Transient modeling

When the transient behavior of the system has to be determined, the model of the power converters needs to include the power switch [85]. Different types of switch models can be included, but most commonly, the model to use is less complex than a quasi-static non-linear one. In most cases, a piece-wise linear model is used, and commutation circuits like snubbers are included if present. The converter components other than the switch are modeled with lumped circuit elements, which can include parasitics. The controller model is related to the magnitude of the time constants involved. If the transient is considered short, the action of the control system can be neglected. Otherwise, the controller is included partially

(reduced order) or totally. Because of the stiffness of power electronic systems the two time scale model is proposed to represent both the dynamics and the ripple effects [92].

B. Dynamic models

The next degree of simplification comes when it is required to study the dynamic behavior of the system. For these cases, average models of the power converters are generally used. Generalized, or multi-frequency average models [11], which uses a Fourier series with variable coefficients, providing better representation of rapid dynamics under large perturbations can be used for large signal stability analysis [78]. Dynamic phasor modeling can be seen as another generalization of the average method and applied to three-phase systems produces a similar representation than the d-q transformation [95]. Moreover, it has the advantage that the harmonics can also be included in the model [68]. Dynamic phasor has already been applied to model dynamically power systems [96], but these approaches only consider a first harmonic approximation.

The unified average switch model, suitable for large-signal stability analysis in large DC-DC power networks is presented in [77]. This model averages a switching cell composed of switch, diode, and inductor. In this way, in addition to the average representation, the model is able of estimate the inductor current ripple.

Stability in a distributed power system can be analyzed in frequency domain through the comparison of the input and output impedances seen at the interconnecting point. The circuit is shown in Fig. 10-6 with the method idea represented in Fig. 10-7. The method is based on the Nyquist criteria, but different approaches have been proposed. This method was first proposed for the small-signal linearized case [93] and then extended to the large signal case [94]. In any case, the proposed model and methodology are limited to systems with DC-DC converters. A similar methodology formulated in a way more suitable for AC systems is presented in [69] for voltage stability study, but using small-signal models. However, most common models to study small-signal stability or control loop design are based on linearized small-signal models like [70],[73] obtained by perturbation and linearization of the large signal case. An example on the use of these model types can be the current sharing scheme for controlling parallel converters [76]. Equivalent current injection sources can be used to represent power converters in the model of an electric network used for control and stability studies. Some examples using equivalent source modeling for large systems are found in [72],[79].

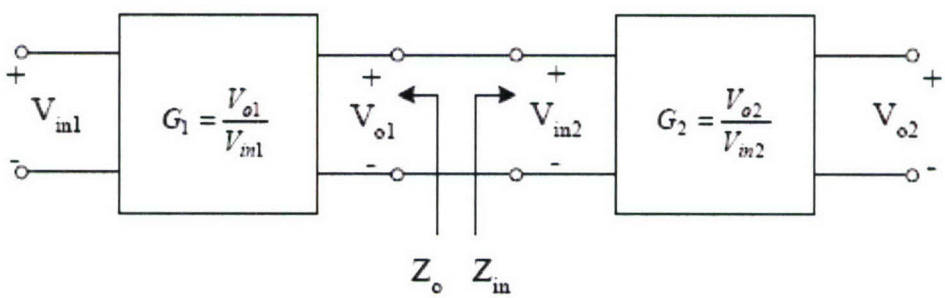
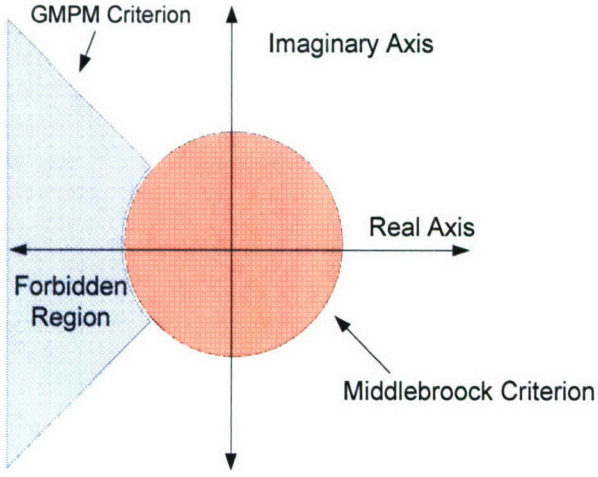
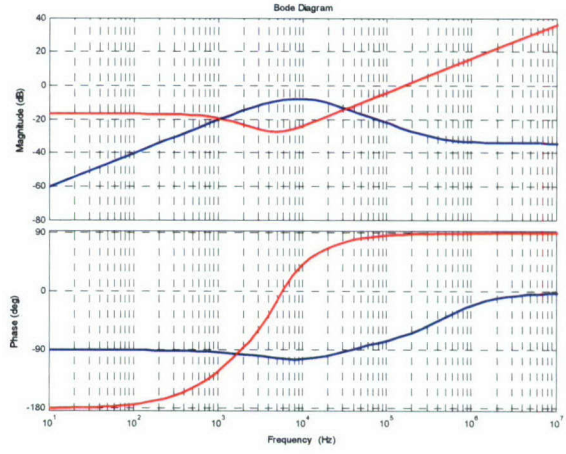


Fig. 10-6 Cascade connection of two converters and points for impedance evaluation according to the criteria presented in [93]



(a) Different criteria based on Nyquist



(b) Input/output impedances of the cascaded converters

Fig. 10-7 Stability of two interconnected DC-DC converters analysis by input/output impedance criteria

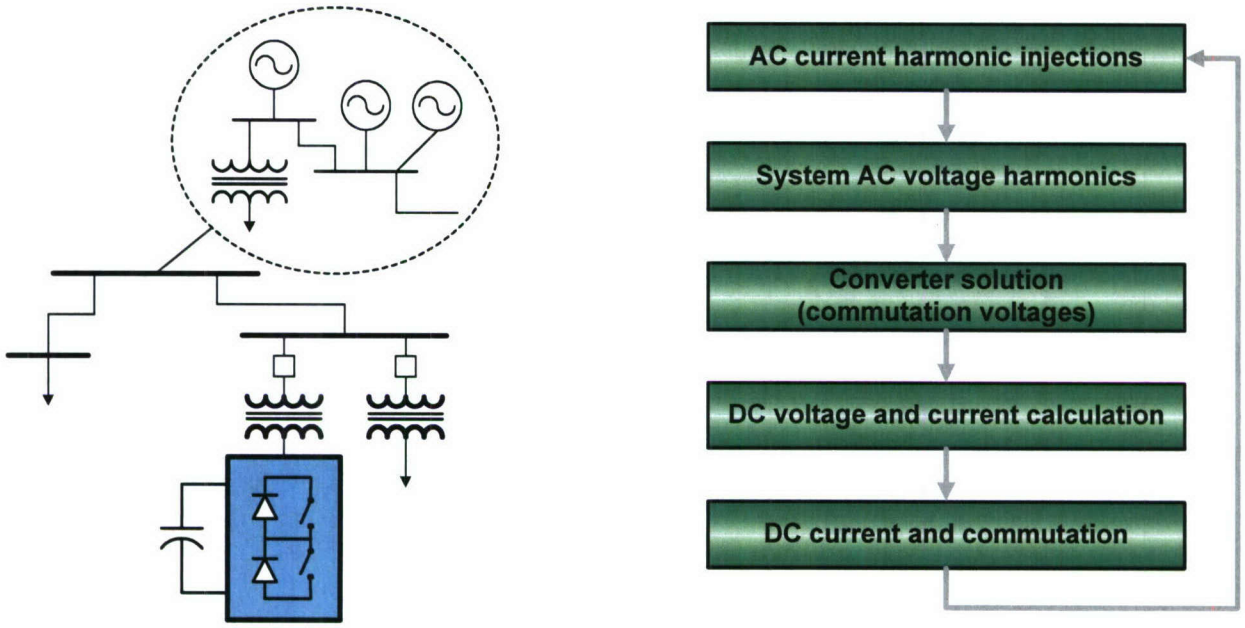
The modeling of converters in three-phase systems for the purpose of control design is generally approached using a Park's type transformation [87]. In case of an unbalanced system, positive and negative sequence component appear in the line voltage. Handling of these system conditions have been analyzed in [97] and [98] with different approaches on how to improve the converter control performance. Same type of rotating reference frame transformation is used in [99] to obtain a small-signal linearized model used for the control of parallel converters.

C. Steady-state models

Steady state models are employed when the interest is on the stationary operation of the system, which usually involves harmonics. Several model formulations have been proposed to study the harmonic propagation in power systems. Some of the formulations are based on time domain switching model of the converter [82], which includes the control system even though in many cases the interest is only in the steady-state values. This is not the most effective way to study harmonic propagation if the network is large in number of components.

The use of equivalent current sources is an approach generally used to represent power converters connected to a network [89]. The current source injection model considers typical harmonics produced by the converter as constants regardless of the conditions of the network. In this approach no interaction network-converter is taken into account; so, the results are not very accurate. Therefore, other formulations have been proposed in time or frequency domain like: transfer function, Norton equivalent, Harmonic-domain, or three-pulse models [83],[88]. Many of the models proposed to study harmonic propagation in power systems dealt with line-commutated inverters because these are most commonly used in high voltage networks. Nevertheless, the modeling of PWM converters for harmonic propagation follows same guidelines. In [100] a Thevenin equivalent source in the harmonic domain is proposed; while in [101] pulse models are used with emphasis on the determination of the inter-harmonics. The previously mentioned models of power converters are then combined with the rest of the network to find the harmonic propagation using harmonic balancing principles [84] like harmonic load flow algorithms [102]. A case of harmonic propagation in a power system study is represented in Fig. 10-8, with the iterative calculation process in Fig. 10-8 (b). A different approach to the power quality issues of

harmonics and reactive power, but specific for the case of compensation is based on the instantaneous power theory [81] used to analyze the interaction between a power electronic load and the network.



(a) Power system equivalent circuit **(b) Harmonic injection calculation iterations**

Fig. 10-8 Study of harmonic propagation in a power system

Stationary models of some power electronic equipment appropriate for studying the load flow in networks are proposed in [74],[75]. A representation of FACTS devices following the classical representation of load flow algorithms, with added constraints, is presented in [90].

IV. Towards a Classification of Power Electronic System Models

Power electronic engineering deals with the operation, design, and construction of power electronic converters. The necessity of knowing the converter operating magnitudes in order to select the circuit components, design the control loop, and take decisions about the construction has led to the proposition of the many different types of models presented in the previous section. The ability to study the behavior of the electric system through modeling and simulation has become an engineering necessity [3]. The proposed models have a different degree of detail, which is in accordance to its physic-based or behavioral orientation discussed before. Detailed models of a complete system involves a large amount of information and its simulation can become unmanageable, even if the technical resources were enough to simulate the behavior, this will not guaranty a good understanding of the system operation [1]. Therefore, it is necessary to approach the modeling issue in a systematic way.

A classification of models that come from the previous section description is based the degree of detail. A general formulation of a power electronic system was shown in equation (2-1). This equation take different forms according to the assumptions and simplifications assumed for the modeling. Fig. 10-9 shows most commonly known math forms.

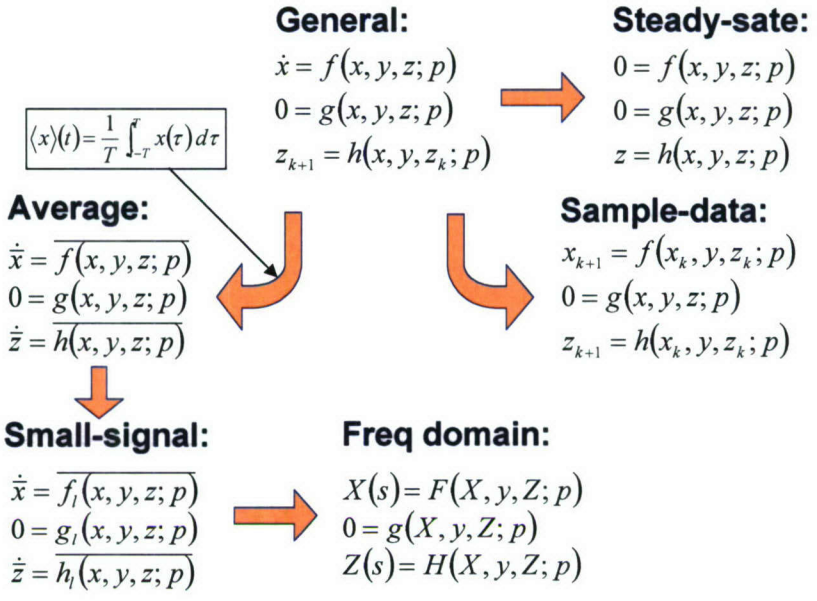


Fig. 10-9 Math formulations of different model types proposed for power electronic systems

It was also observed that the models can be classified according to type of problems they are used to analyze. In addition, the description of the studied electromagnetic phenomena is based on a defined time resolution. Therefore, a first way of classifying the models is by the time scale they are based on their definition. Schematically, this idea is represented in Fig. 10-10

It was also observed that the models can be classified according to type of problems they are used to analyze. This is more evident at the system level and a classification of system issues and the type of model to use is shown in Table 10-1. Some phenomena like EMI require quite a lot of development at the system level. The state-of-art converter-level EMI model can help to predict the conducted EMI noise for converters in a certain frequency range, but it lacks generality for practical system-level design.

The combination of the solution tools and the modeling purpose produce a model classification that can be summarized like in Table 10-2. Because power electronics is a complex system, several subsystems can be identified:

- System: switching converter, loads, machines, and interconnection
- Converter: power stage, control system
- Components: electronic switch, energy storage

The system model is composed by an aggregation of subsystem models. Although it can be some mixing, the sub-models have to be in agreement with the characteristics of the global model.

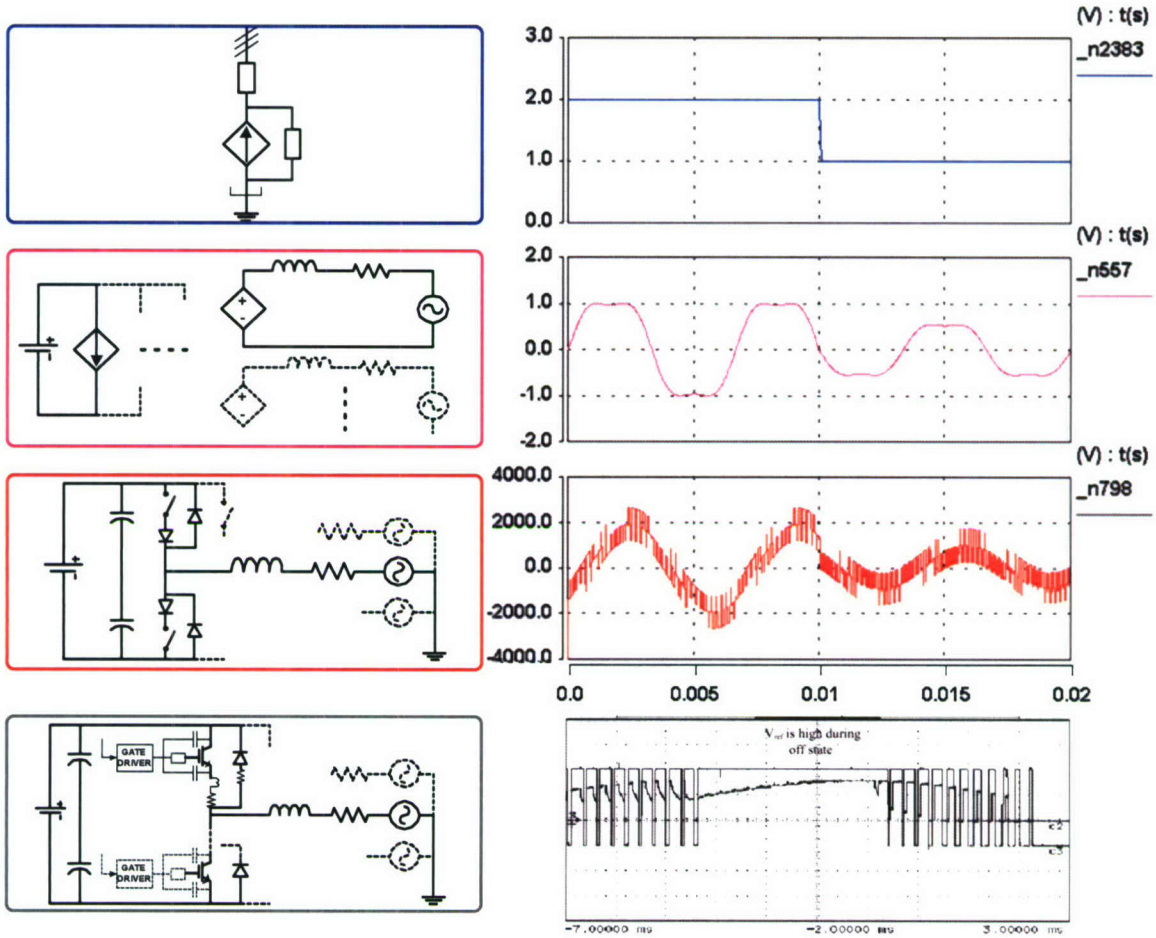


Fig. 10-10 Circuit schematic of types of models and results produced by them (waveforms)

Table 10-1Time-scale classification of Power system models

Phenomena	Time scale	Model characteristics
Steady-state, Load flow	Steady-state	Quasi-steady state model
Harmonics	1-100 ms	Ideal switching model or harmonic sources
Control and stability	0.1-10 ms	Average model of power converter, detailed controls
Electromagnetic transients	0.1-1000 us	Detailed circuit, Switching device model
EMI	1-100 ns	Detailed circuit model inc. parasitic, detailed switch

Table 10-2 Classification of Power Electronic System Models

Solution method / Purpose of study		Stationary	Average			Frequency domain		Switched
			DC-DC large signal	3-ph large signal	Small signal	Transfer function	Large signal	Piece-wise linear
Steady-state	Power flow	Stationary eqs. PQV load flow						
	Harmonics	Harm source Harm balance		Fourier Instant power		Harm. domain	Equiv. source	On-off switch
Dynamic	Control & stability		Gen. Average Avg. switch	Dyn. phasor d-q transform	Perturb+linear(*) Dyn. phasor	TF from (*) I sharing	Eq. dyn. source	
	Stability only					Zi/Zo ratio Incr. network	Zi/Zo+non-lin I injection	
Electrom. transient			Average+ripple Two-time scale	Average+ripple				Switch+ commutation

V. Modeling in the Design Process of Power Electronic Systems

Given the system requirements, usually a top-down approach is followed, which means that first the requirements on the system are analyzed [86]. Models like the mentioned in Table 3-1 are used to determine the requirements on the components, (converters in our case). Later the study of the converter design will determine the requirements on the elements, switches, passives, sensors, etc. However, the design process is not only top-down, after the system components are determined; the behavior of the whole system needs to be verified. Usually, several iterations are required to complete the design process because when all the components are determined, it can happen that the complete system does not behave as expected, or the requirements determined previously were not enough accurate. If accurate models of the components in the system were employed, it could be that the requirements over them were accurate. In addition, accurate models of the components in the system will accurately predict the system behavior. The converter design process is achieved by solving the following tasks:

1- Determination of the converter form and function: topology, switching & commutation states, selection of switching and sampling frequency, inductor design, DC voltage level selection, power device pre-selection.

2- Device commutation strategy: Computation of inverter V & I harmonics, commutation sub-circuits

3- Loss determination: Computation of device currents and losses, efficiency

4- Control system: Control loop design, Computation of DC voltage regulation

5- Power quality: power factor and current harmonics

6- Protection, and other additional issues like geometry

Along the design process different models are used to represent the power electronic converter operation. To determine the converter form and function, it is necessary to study the magnitude steady-state ratings, type of waveforms and related basic stress at the components. The model used is usually a quasi-stationary model including a piece-wise linear switch model for the converter that operates in a stable

operation point; so, no control loops are included. This model can also predict the harmonic generation and be used to select a modulation strategy if necessary.

To study the losses and efficiency, the switch model needs to be fairly detailed, representing commutation and conduction losses with accuracy. Usually, a quasi-static non-linear model of the switch, together with a lumped representation of the energy storage will produce appropriate results. A three dimensional geometric description of the components linked to detailed elements is required to study the mounting and spatial distribution of the system.

Since low pass filters are provided at the input and output, and the goal of the control loops is to control average type value of input/output magnitudes, controller design uses average type models. For linear control design [87], linearized small-signal models are used, from where the transfer function can be extracted. Otherwise, large signal average models are used to design non-linear controllers [103]. Although not widely used, sampled data models can provide some advantage in case digital control is used. System issues like transient response, harmonic generation, and quality of the regulation in the system are studied using the models in section III. Some methodologies have been proposed for designing a power converter [104], but there is still a lack in systematic approaches for designing a power system. The design process is usually completed after more than one iteration of analysis of the different system issues. Fig. 10-11 approaches schematically the system design process. The next section presents some ideas on the design of a ship power system. By looking at this design process is also possible to see with an increased degree of detail the use and how the different models were derived.

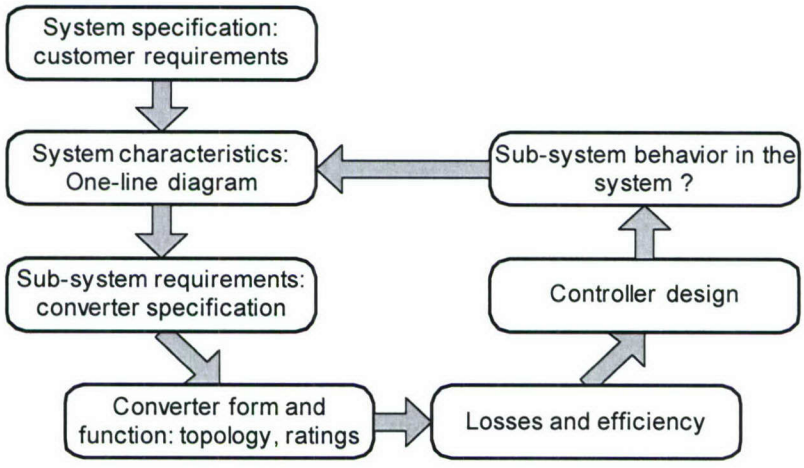


Fig. 10-11 Flow-chart of a single converter design process and the model types that can be used

VI. Design Outline of a Ship Power System

The general information of the power system is given by the requirements set by the "electric customers". The load and available energy source impose the specification for voltage level and regulation, peak load, demand and diversity factors, power factor, and system reliability. A General description of the ship power system was presented in Chapter 2. With the basic information mentioned, a one-line diagram like Fig. 10-12, for the AC portion of the system, constitutes the basic model of the system. This model, although simple, it already includes basic information about the system operation like voltage levels and power for each converter.

For the AC system, steady state models are used to asses the system reliability making a quantitative comparison of the failure rate and the forced downtime in hours per year for different circuit arrangements including radial, primary selective, secondary-selective, or simple spot [105]. Also this analysis will determine whether the degree of redundancy that the system requires. Geometrical and constructive characteristics must also be taken into account. In this example a secondary selective scheme with redundant generation is chosen.

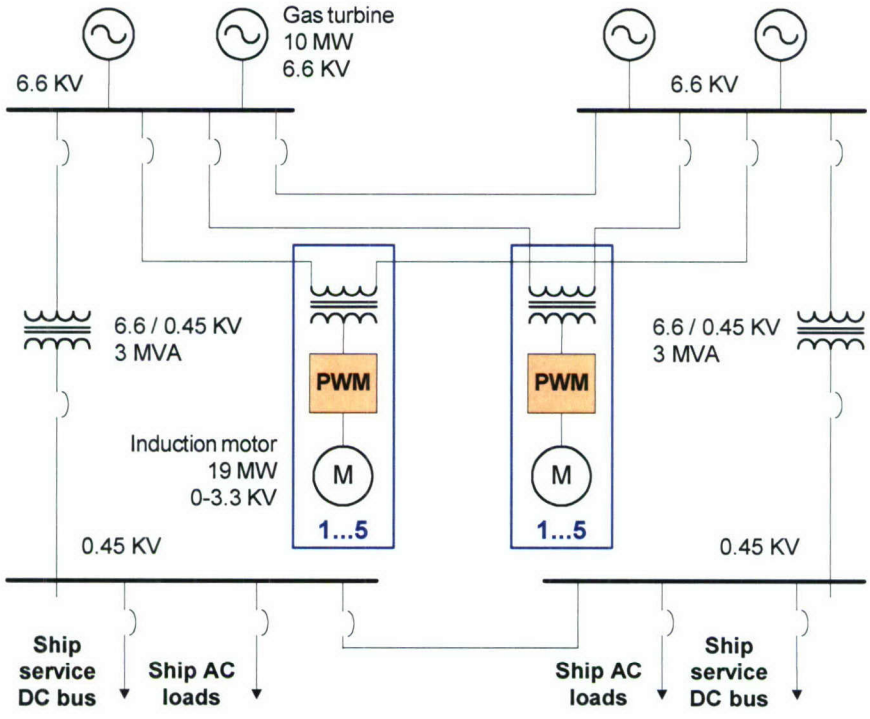


Fig. 10-12 One-line diagram of the AC system and steady-state model of a converter

Once the power system configuration is determined a load flow analysis is used to calculate the transformer and conductors' size, and verify that the system is capable of providing power to all equipment within published voltage limits under all normal operating conditions [106].

In a power system, the next step is to study the dynamic behavior of the system. In a system with several non-linear loads, it is important to study the system level stability because of the recognized sensitivity of the system to voltage variation when constant power loads are dominant. The presence of this type of loads in a ship is dominant in the DC portion of the system. That DC portion is connected to the AC through the service buses. For a DC interconnection, it has been shown that in case of linear loads a power flow analysis always has an equilibrium solution and is unique. But in presence of constant power loads there is more than one possible solution [108]. In a simplified model like Fig. 10-13 there are two equilibrium points if;

$$R < \frac{Vs^2}{4P_o}$$

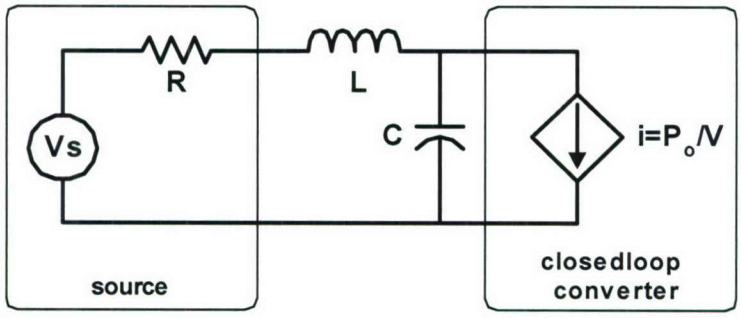


Fig. 10-13 Simplified schematic of the constant power load interconnection case

Therefore, in case of a voltage disturbance known as sags, the system can experience a complete failure. In relation with the filter, the condition for stability is determined by:

$$\sqrt{\frac{L}{C}} < R < \frac{Vs^2}{4P_o}$$

Steady-state models are also used to calculate short-circuit currents at all sub-system components. The maximum short-circuit current values are used for selecting protection schemes and circuit breakers, and checking the ability of the system components to resist mechanical and thermal stresses. The minimum current failure values are used to establish the required sensitivity of protective relays [109]. The steady state model provides voltage levels and power ratings based on load requirements and source availability. In the case of the AC system the selection of the voltages at each portion of the system is based on standard and common practices based on the power requirements. A geometrical representation of the system is used to determine the location of each converter.

For the DC system it is up to the designer to choose the voltage level because there is no real standardization as in AC power systems. The configuration of the DC system for a ship has been carefully studied according to the necessities of the different DC users [110]-[112]. Based on those studies a representative portion of the DC power system is shown in Fig. 10-14.

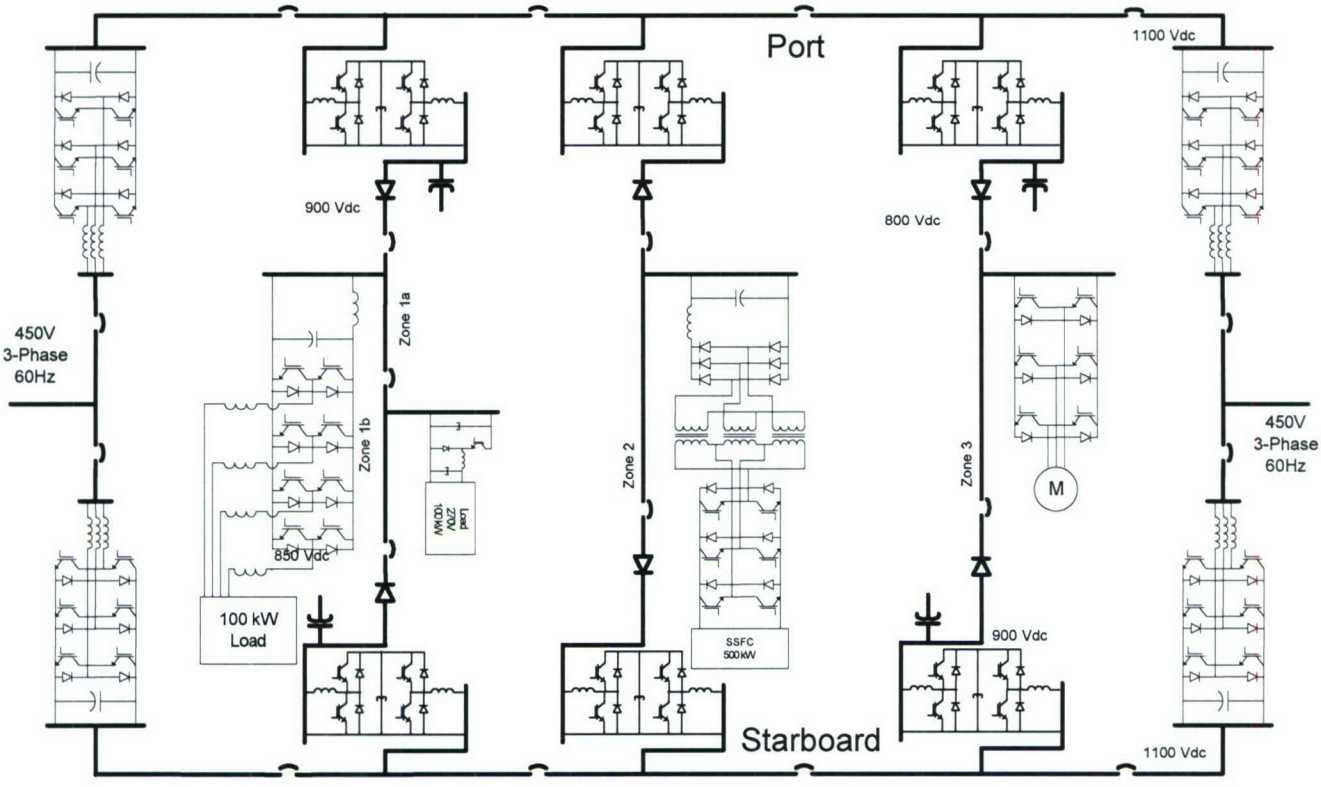


Fig. 10-14 AC-DC Converter geometrical representation

The specification of the individual equipment is determined based on the requirements established during the system study. Up to this stage it was assumed that at the input of the AC-DC converter modules have a sinusoidal voltage and the interactions between the AC-DC converter and the AC power system are minimal. However, as the design process advances, the assumption of no interaction between system components cannot be kept. For the converters connected at the DC bus, as demonstrated in [113], the input impedance of a converter behaves as a negative resistance up to the crossover frequency of the voltage loop gain. Hence, for analysis and design at this level, the load converter can be replaced by the ratio between the input voltage and current [114]. With this information, initial values for output and input impedance of intermediated filters, and output impedance of AC-DC converters can be specified. The information collected in this analysis will serve as input for the converter and filter design from the point of view of the system. In addition to the system level specification there are also requirements from the load that the converter must meet to guarantee a good design. However the information provided is still limited, thus designers often divide the design in two stages; conceptual stage and definition stage design.

During the conceptual stage, the information collected from the load and the system is used for power stage and close loop control specification. Thus, a model of the converter using piece-wise linear switch model, average models and ideal description of inductors and capacitors is used. This analysis provides information for device and passive component selection. Once the devices are selected, designers can estimate its power losses using an appropriate switch model. Then, power losses are used as input for thermal analysis and heat sink design. In this process electro-thermal and finite element models are used. At this point all the information for a detailed simulation is available in order to verify the design.

From the control point of view the approach is very similar. During the conceptual design, control components are selected using small signal models; so, input and output impedance, overshoot and settling time requirements are met. Subsequently during the definition stage the control design is verified

using more detailed models such as large signal average models and switch models. In this way, different types of models are required for the design of the power system. The use of the models at the different stages of the design is represented in Fig. 10-15.

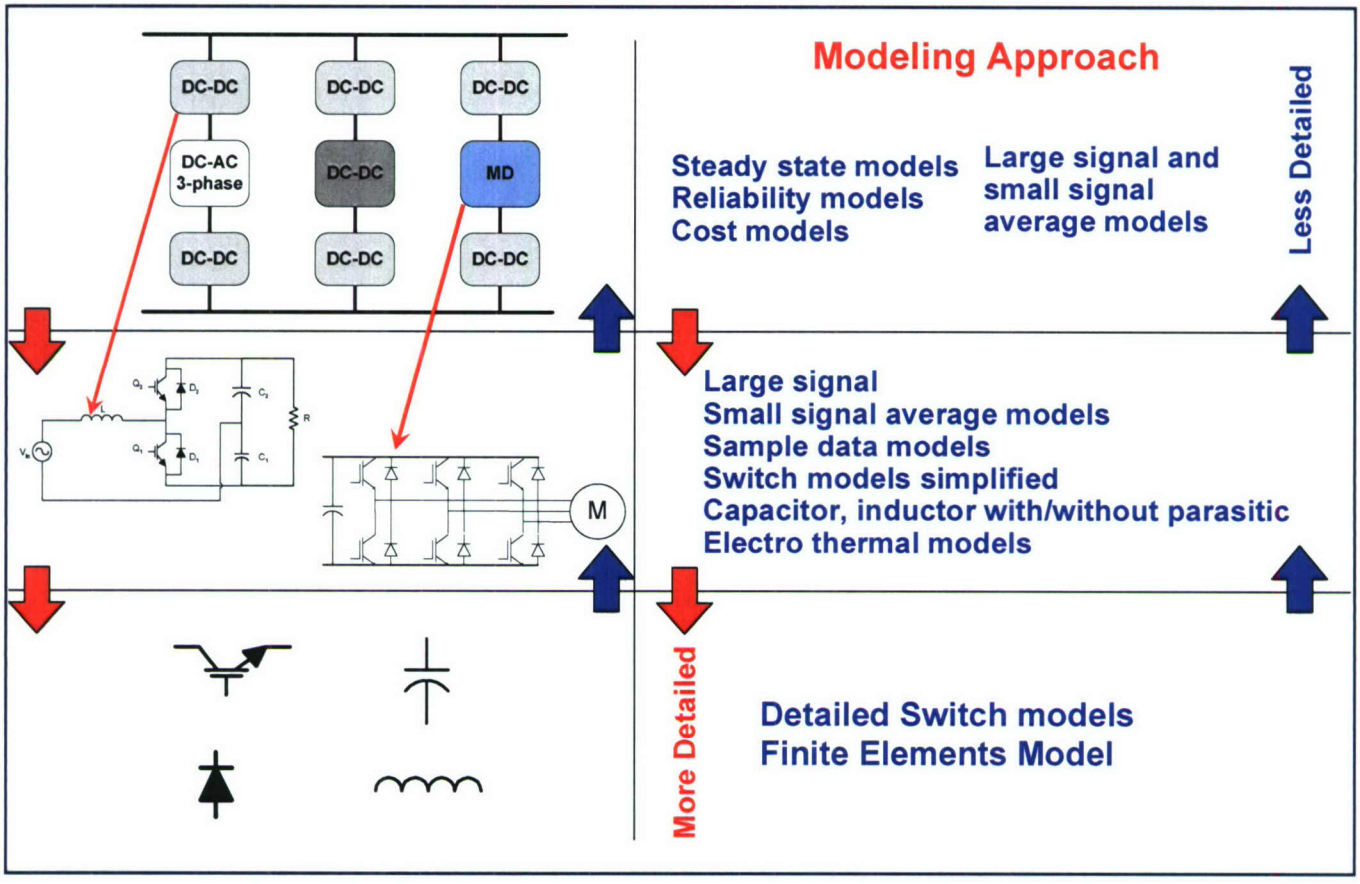


Fig. 10-15 Use of different types of model in the design process

VII. Discussion and Conclusions

There exists a wide variety of models for analyzing power electronic systems. Due to the complexity of those systems all the electric phenomena cannot be covered by only one model and several of them are usually involved. In addition, the results obtained from the models are not always totally accurate, and after the calculation and simulation stages, the design process usually requires prototype testing. If accurate models were available allowing prediction of the system behavior, the power electronics system could be designed in the computer and then directly built saving time and money, and reducing failures and re-design effort. Therefore, there is still a considerable work to be done in order to enhance the way power electronics systems are modeled. The following paragraphs approach some ideas and suggestions for this work.

Many model approximations were originated by the necessity of having models able to be handled by the available computation resources. Nevertheless, even if the possibility of simulating detailed models of large system would exist, this will not automatically guarantee a good design because a good understanding of the phenomena would still be lacking. In some cases partial models help better to understand the behavior of a particular system. Therefore, some organization on the way the models are used would certainly be a helpful for the analysis and design. Due to the stiffness of power electronic

systems, time constant separation has been used as a key in power system modeling, simplification and order reduction. Phenomena with similar time constant are included with detail in the same model. Otherwise, when the time constant difference is large, portions of the model are simplified or neglected. However, time-scale separation becomes a complex issue when it comes to system studies due to the increased levels of interaction between components.

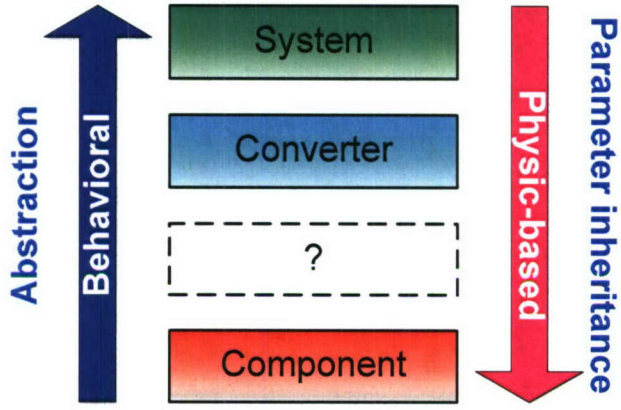


Fig. 10-16 Organization of power electronic models towards a hierarchy

The EMI noise interactions in a multi-converter system are not well understood. The current practice for reducing system interference is generally to add a filter to each converter, which is clearly a local, converter-level solution rather than a more efficient system-level solution. Understanding and characterizing the complex EMI phenomena through accurate modeling and prediction of the EMI noise emission and propagation is a necessary first step for achieving an efficient filtering solution and for managing the EMI/EMC issue at the system level.

For a complete, complex power system there is still a lack of unified, comprehensive modeling. A hierarchical model is probably a good approach to the problem of modeling complex power systems, and some attempts in this path have already been made [1]-[3]. It is possible that guidelines and models taken from other technological domains [86],[115] can help in providing a reference for an organized way of modeling power electronic systems. For this, the behavioral and physic based model classification can provide a basis to define hierarchy levels and relation between models. An organized reference and a systematic way of linking the different models will most probably facilitate the analysis and design of power electronic systems.

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Chapter 11 HIERARCHICAL MODELING OF POWER ELECTRONICS BUILDING BLOCK –BASED POWER CONVERTERS

I. Introduction

This Chapter focuses on the hierarchical modeling of Power Electronics Building Blocks (PEBB), presenting the different analyses and implementations carried out in order to achieve accurate mathematical and physics-based representations of PEBB-based converters. Generally speaking, a precise software model of a power converter topology is a powerful tool to perform its electromagnetic and thermal design. Simplified functional models are more appropriate when designing the controls that are to govern the converter within desired operational specifications. If these modeling tools are precise enough, models themselves become the specifications or specs of the actual hardware embodiment. Hence, a significant reduction in design cycles may be achieved by going directly from models to production, skipping over the up to now required and time and cost consuming hardware prototyping. This hierarchical modeling approach matches perfectly the concept behind PEBB -based power converters, which intrinsically represent hierarchical power conversion structures. The main objective of this Chapter is then to obtain a suitable model of the PEBB developed and recently upgraded in CPES ONR-sponsored projects, the final goal being to create elementary simulation blocks for power processing permitting the simulation, design and synthesis of more involved power conversion structures.

The first stage in the PEBB modeling entails a detailed characterization of the switching devices. In this process, it was necessary to analyze the specifications supplied by the manufacturer's datasheet while capturing the behavior of the actual device by means a mathematical physics-based model, which faithfully reproduced its particular characteristics nonetheless limiting the total computational load enabling reasonable simulation runs. This is important since in long time domain simulations, certain aspects of the behavior of the converter lose relevance respect to the speed on the simulation. In such long simulations, inherent characteristics of the switching process can be disregarded, and the average model of the power converter becomes the most suitable tool. The design of this average model is the second goal of this chapter.

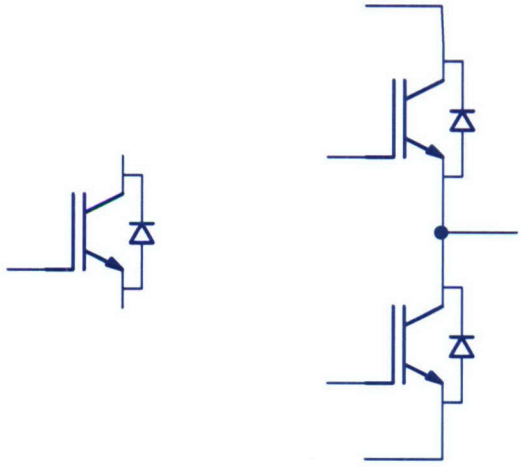
In addition, in an effort to support the Electric Ship Research and Development Consortium (ESRDC), all mathematical models developed in the previous studies have been implemented in VTB (Virtual Test Bed). This simulation platform supports hierarchical model structures thus perfectly blending into the proposed modeling approach for PEBB-based converters.

II. PEBB's Device Modeling

The first step to develop a model of a voltage-source converter phase-leg PEBB module is to accurately model each and every of its components. The basic topology of the current bi-directional switching cell, seen in Fig.11-1, is a combination of a semiconductor witch (IGBT) and anti-parallel diode (APD). These two devices are nonlinear and therefore to obtain a mathematical model reflecting exactly its physical behavior can be a very hard matter. To simplify the model complexity, trying to obtain equations that can be easily understood and processed, the actual characteristic of the IGBT and APD need to be linearized.

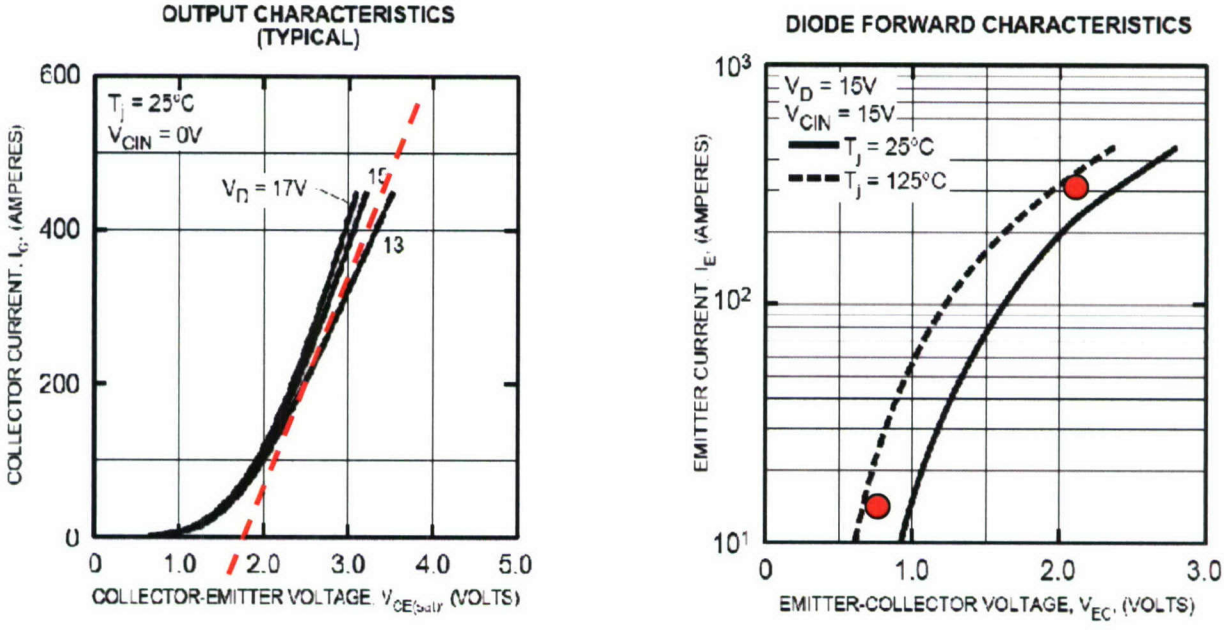
The core of the physical PEBB phase-leg is the Mitsubishi PM300DVA120 IPM. This IPM responds to the half-bridge topology shown in Fig. 11-1 b). From this component datasheet the necessary information needed can be extracted to linearize the characteristics of the IGBT and APD of the switching cell. From the datasheet, the curves shown in Fig. 11-2 depict the characteristics of the two non-linear devices.

In Fig. 11-2, the dashed line indicates the linearization of the IGBT, while the dots are the end points of the line that linearizes the APD (only dots shown because it is a semi-log graph).



(a) (b)

Fig. 11-1 (a) Switching Cell, (b) Half-Bridge



(a) (b)

Fig. 11-2 (a) IGBT characteristics, (b) APD characteristics.

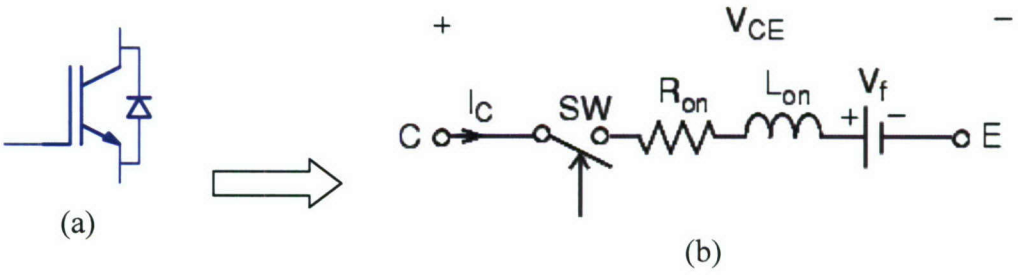


Fig. 11-3 **(a) IGBT, (b) Equivalent circuit with linear devices**

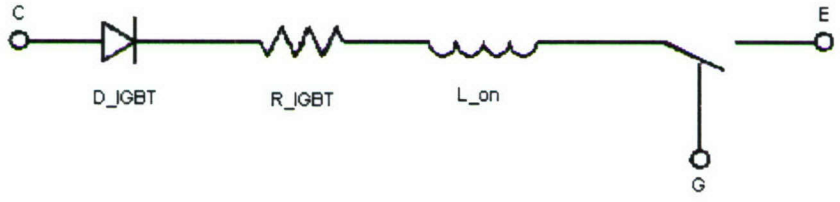


Fig. 11-4 **Equivalent circuit for simulation (using SABER as simulation tool)**

II.1. IGBT Linearization

A good approximation describing the behavior of an IGBT can be obtained by means of the circuit shown in Fig. 11-3. Translation of the equivalent circuit shown in Fig. 11-3(b) into another one more suitable for simulation purposes yields the schematic shown in Fig. 11-4. In Fig. 11-4, the forward voltage of an ideal diode (with zero forward resistance and infinite reverse resistance) replaces the constant voltage source. Therefore, the voltage drop on the ideal diode is a constant and the voltage drop in the forward resistor (R_IGBT) is linearly proportional to the current flowing through it. The voltage loss of the inductor is negligible. From Fig. 11-5, the points {V_{CE} = 2V, I_C = 100A & V_{CE} = 3V, I_C = 400A} can be used to create the linearized characteristic depicted by the dashed line.

The idealized linear characteristic of the IGBT responds to the equation:

$$V_{CE} = I_C \, R_{IGBT} + V_{IGBT} \tag{1}$$

Introducing in (1) the two points considered in Fig. 11-5, the values of $\mathbf{R_{IGBT}}$ **= 3.33 mΩ** and $\mathbf{V_{IGBT}}$ **= 1.67 V** are determined.

The points at which the device was linearized were chosen because this particular device is rated at a max average current of 300A, which falls in this linearized region. A more precise model for the IGBT can be achieved by means a voltage controlled current polynomial source. From Fig. 11-2, the IGBT characteristic can be described by:

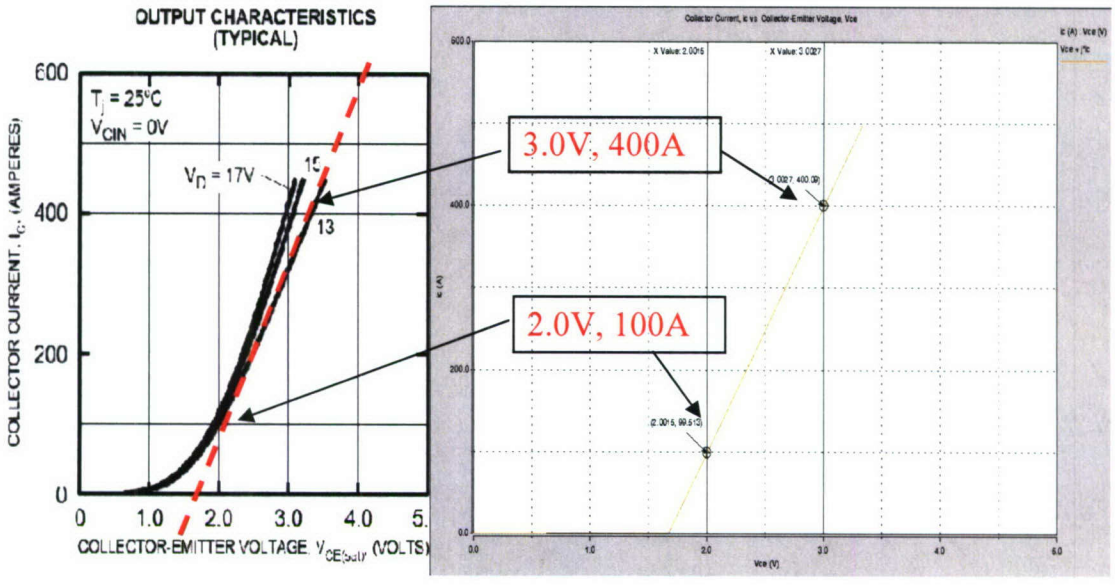


Fig. 11-5 **IGBT Linearized Curve comparison to Datasheet Curve**

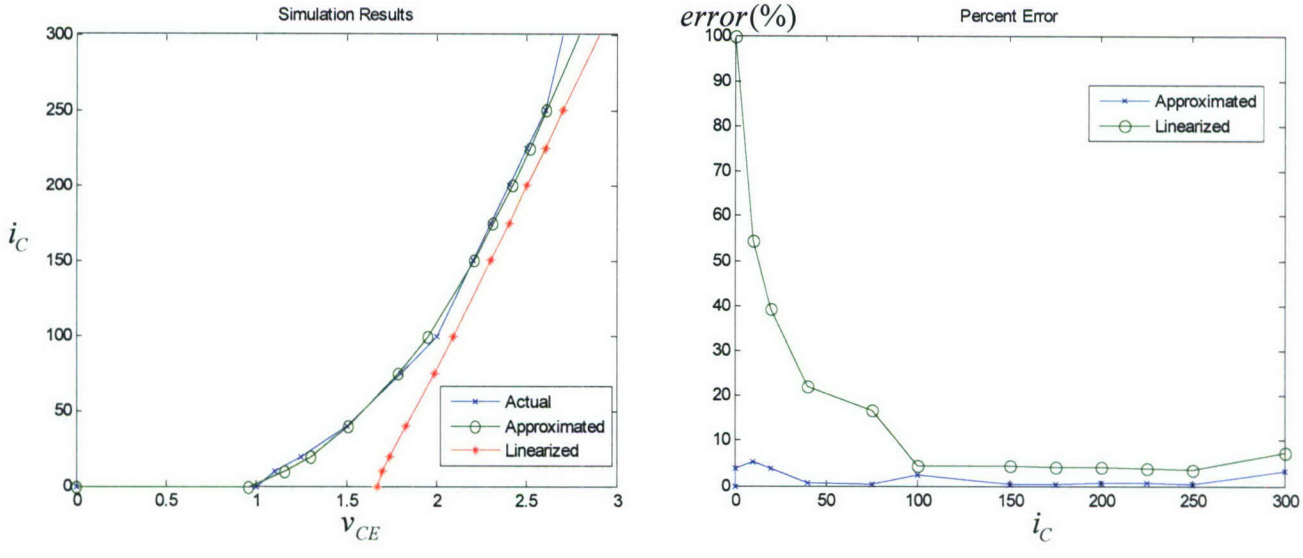


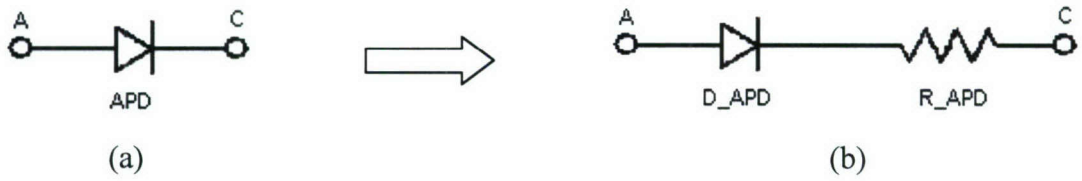
Fig. 11-6 **Linearized and polynomial model comparison**

$$i_{DS} = 27.97 \cdot v_{DS}^3 - 18.8 v_{DS}^2 - 7.74 v_{DS} - 0.37 \quad \textbf{(2)}$$

Obviously, as Fig. 11-6 shows, the polynomial model achieves a smaller error than the linearized model, but its computational cost is too high, which gives rise too slow simulations. This slowness in the simulation makes the polynomial model a not suitable option form a practical point of view.

II.2. APD Linearization –

The APD characteristic can be linearized in same manner as the IGBT was. Therefore, the APD behavior can be depicted by the circuit shown in Fig. 11-7.



(a) (b)

Fig. 11-7 (a) APD, (b) Equivalent circuit with linear devices

Assuming D_APD is an idealized diode with a constant forward voltage and zero forward resistance, the conduction characteristic of the APD can be described as:

$$V_{EC} = I_E \, R_{APD} + V_{APD} \tag{3}$$

Taking two work points from the characteristic shown in Fig. 11-2 {V_{EC} = 2.5V, I_E = 350A & V_{EC} = 1.0V, I_E = 15A } the parameters of (3) can be easily calculated. This yields **R_{APD} =4.478 mΩ** and **V_{APD} = 0.9328 V**. Fig. 11-2 b) shows the two selected work point and the linearized characteristic of the APD.

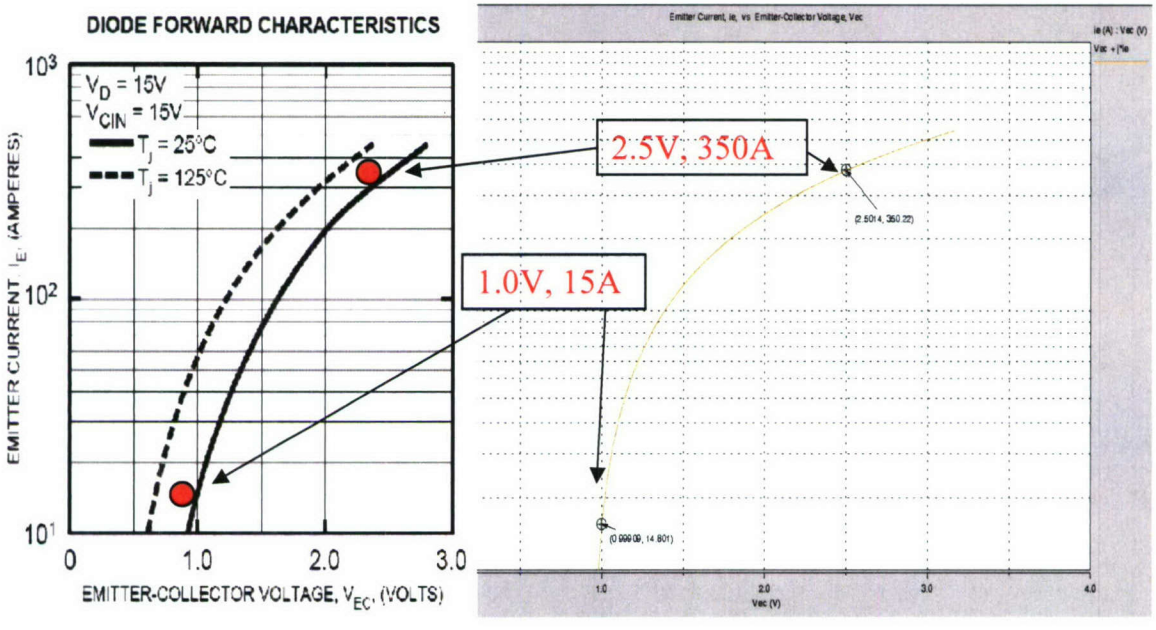


Fig. 11-8 IGBT Linearized Curve comparison to Datasheet Curve

The points at which the device was linearized were chosen because this particular device is rated at a max average current of 300A, which falls in this linearized region.

Like in the IGBT modeling, a more precise model of the APD can be obtained by means the use of a polynomial function. From the APD characteristic, such polynomial function is shown in (4). Although the simulation results are more precise when the APD model is based in (4), its computational cost is too high making it inoperative for practical purposes.

$$i_E = 2.52 \cdot v_{EC}^3 + 76.52 v_{EC}^2 - 66.56 v_{EC} - 0.73 \tag{4}$$

III. PEBB Switching Model

Once the switching devices have been modeled, it is possible to develop the model of a phase-leg constituted by two IGBT's and its APD diodes. In Fig. 11-9, a linearized component based model for the phase-leg is presented. However, a more realistic model of the phase-leg should include not only the switching devices, but also all the rest of components associated to this elementary power processor. Therefore, capacitors and parasitic components due to bus bars need to be modeled as well.

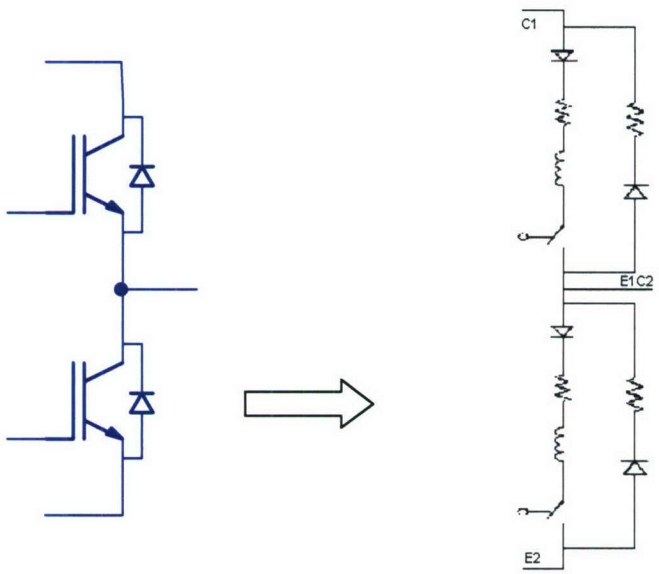


Fig. 11-9 Equivalent circuit for phase-leg

Each PEBB phase-leg has a 35 μF capacitor across the collector of the top switching cell (C1) to the emitter of the bottom switching cell (E2), for an AC system this would be across the "DC Link" terminals. There are also copper bus bars and "blades" used to connect the half-bridge to the rest of the system. The parasitics associated with these copper bus bars are dominated by the resistive losses; therefore they can be modeled by simple resistors and governed by (5).

$$R_{CU} = \frac{\rho \ell}{A} \tag{5}$$

In (5), R_{CU} is the resistance, ρ is the conductivity, ℓ is the length of bus bars, and A is the cross-sectional area of the bus bars. After measurements and calculations it is found that each copper blade that connects the half-bridge to the rest of the system is $\boldsymbol{R_{CU} \approx 60\ \mu\Omega}$.

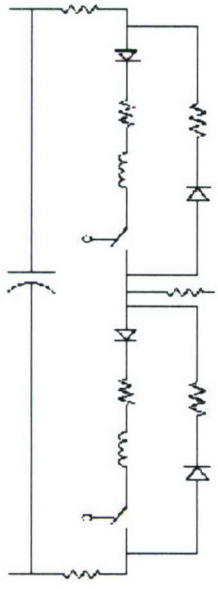


Fig. 11-10 Switching Model of PEBB phase-leg

The final model of the PEBB phase-leg, including the DC-link capacitor and the connector resistance, is shown in Fig. 11-10. Combination of several PEBB models permits to simulate more complex topologies of power converters. In this way, an open-loop (OL) three-phase (3Φ) voltage source inverter (VSI) was simulated using three PEBB phase-legs in parallel. It is seen in Fig. 11-11 and Fig. 11-12 that under the following OL test conditions the switching model is a close match to the actual hardware results.

OL Test conditions 1:

- $V_{DC} = 30V$
- Balanced loads @ $^{5}/_{6}\ \Omega$
- Sinusoidal Pulse Width Modulation (SPWM)
- Modulation index, M = 0.5
- 5 μs dead-time in the control to switch path

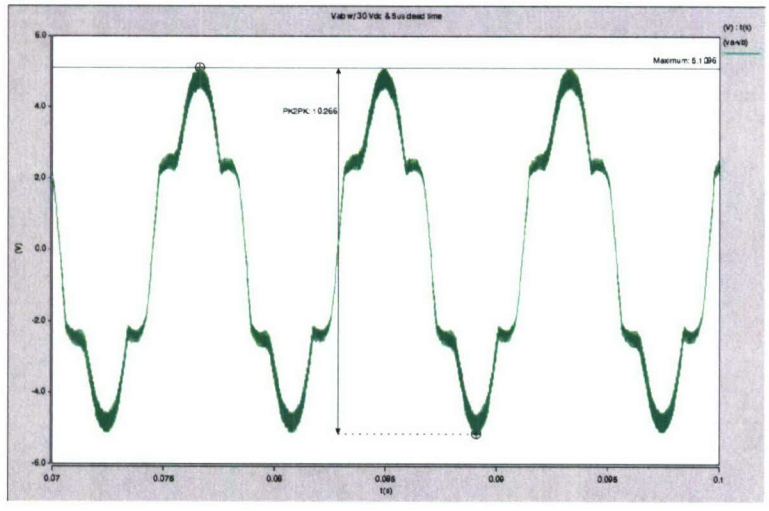


Fig. 11-11 Line-to-Line Voltage @ 30 VDC and 5 μs dead-time

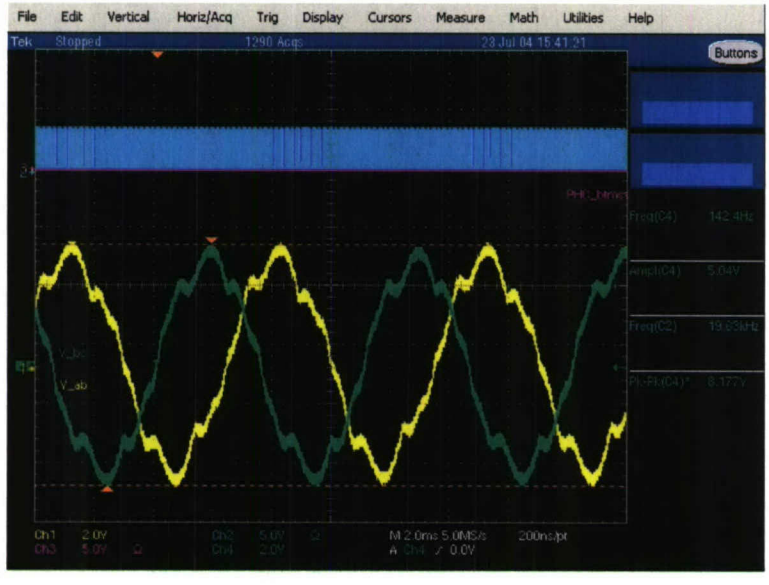


Fig. 11-12 Line-to-Line Voltage from Hardware @ 30 VDC

After verifying that the switching model accurately captured the electrical behavior of the hardware, this same model was simulated under higher power levels still in OL conditions.

OL Test conditions 2:

- $V_{DC} = 300V$
- Balanced loads @ $^{5}/_{6}\ \Omega$
- Sinusoidal Pulse Width Modulation (SPWM)
- Modulation index, M = 0.5
- no dead-time in the control to switch path

Note that the dead-time from control to the switch was removed. This is so because a dead-time compensator can be implemented in the hardware manager (HM) to remove the effects the dead-time has on the system (see HM section in Chapter 06 for more about dead-time compensation).

Fig. 11-13 shows the results of the system at 300 V_{DC} and *with* 5 µs dead-time; while Fig. 11-14 is without the dead-time. Notice how the harmonics and extra losses that arise from the dead-time disappear in Fig. 11-14, and a cleaner sinusoid is left.

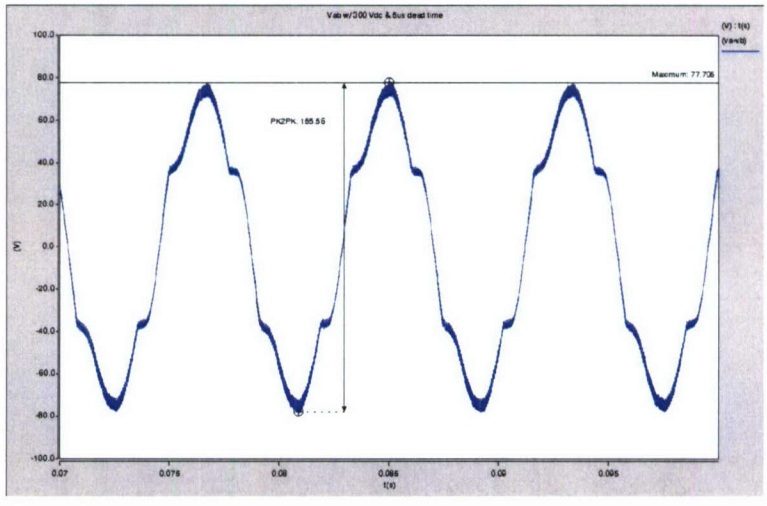


Fig. 11-13 Line-to-Line Voltage @ 300 VDC & 5 µs dead-time

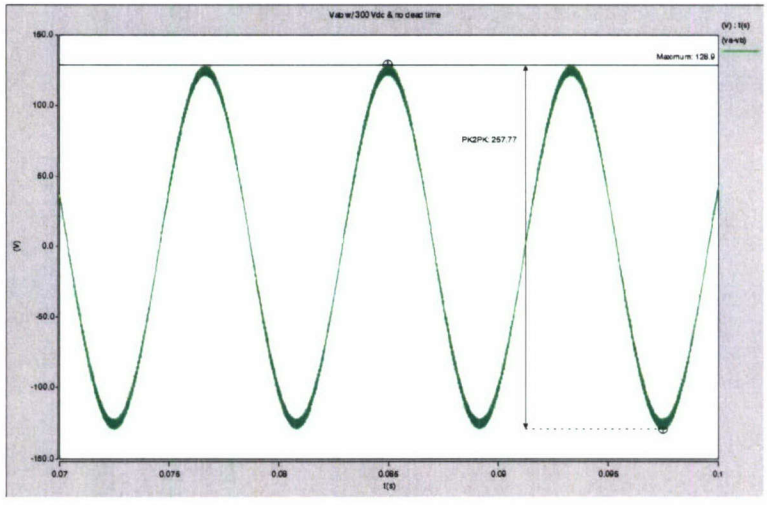


Fig. 11-14 Line-to-Line Voltage @ 300 VDC & no dead-time

IV. Average Modeling of PEBB-Based Converters

An average model of the PEBB phase-leg based on the switching model, described above, is derived in this section. Averaged equations can be developed by writing equations based on the circuit depicted in Fig. 11-15 and then averaging over a switching cycle.

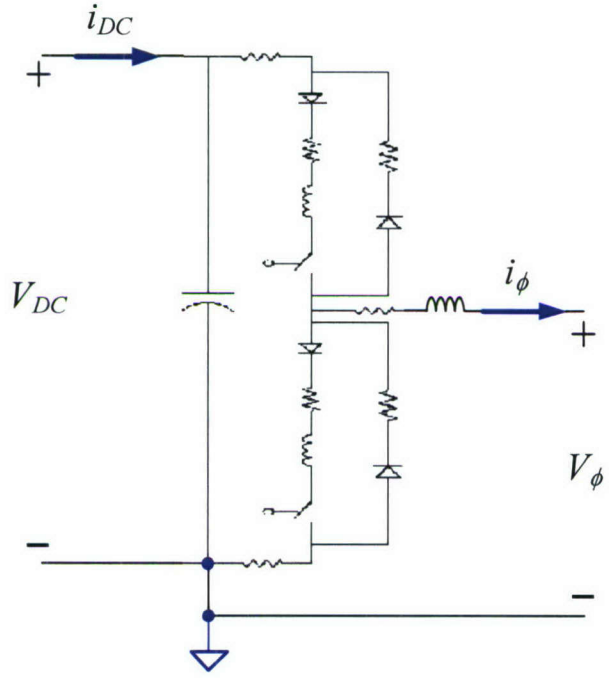


Fig. 11-15 One Phase from a 3Φ VSI

Functions control of the top and bottom switches can be denoted as:

$$S_{\Phi_T} = \begin{cases} 1 \\ 0 \end{cases} \begin{matrix} switch\ is\ on \\ switch\ is\ off \end{matrix}$$
$$S_{\Phi_B} = \begin{cases} 1 \\ 0 \end{cases} \begin{matrix} switch\ is\ on \\ switch\ is\ off \end{matrix} \qquad (6)$$

In the phase-leg, always a switch is *on* state and never the two switches are *on* estate simultaneously. Therefore, it should be accomplished that:

$$S_{\Phi_T} + S_{\Phi_B} = 1$$
$$S_{\Phi_T} \cdot S_{\Phi_B} = 0 \qquad (7)$$

Let the average percentage of time that the top switch is *on*, or the duty-cycle, over a switching period be represented by d_Φ, and the percentage of time the bottom switch is *on* be d'_Φ. Governed by the same rational behind (7), it can be said that:

$$d'_\Phi = 1 - d_\Phi \tag{8}$$

IV.1. Voltage Equations

Writing voltage equations for the VSI, it is found that:

$$\begin{aligned} & d_\Phi V_{DC} - V_S - 2 i_\Phi R_{CU} - V_L - V_\Phi = 0 \\ & V_L = L \frac{d}{dt} i_\Phi \\ & V_S = \textit{voltage drop across switches} \end{aligned} \tag{9}$$

To solve for V_S, the currents through the top and bottom switching cells needs to be analyzed. Seen in Fig. 11-16, it is noted that when $i_\Phi > 0$, it is the top IGBT or the bottom APD which is conducting; and when $i_\Phi < 0$, it is the bottom IGBT or the top APD which is. Therefore the voltage drop across the switching cells can be stated as:

$$V_S = \begin{cases} \left.\begin{matrix} V_{IGBT} + R_{IGBT}\, i_\Phi + V_{L_{on}} \\ V_{APD} + R_{APD}\, i_\Phi \end{matrix}\right\} & \textit{during } t_{on,\Phi},\ i_\Phi > 0 \\ \left.\begin{matrix} V_{APD} + R_{APD}\, i_\Phi \\ V_{IGBT} + R_{IGBT}\, i_\Phi + V_{L_{on}} \end{matrix}\right\} & \textit{during } t_{off,\Phi},\ i_\Phi < 0 \end{cases} \tag{10}$$

It is also noted from the figure and (10) that because the control is SPWM, that the duty-cycles for when $V_\Phi \geq 0$ are the exact opposite of when $V_\Phi < 0$; therefore the losses during the second half of the line-cycle are the exact same as the first half. This simplifies (10) to that in (11).

$$V_S = \begin{cases} \left.\begin{matrix} V_{IGBT} + R_{IGBT}\, i_\Phi + V_{L_{on}} \\ V_{APD} + R_{APD}\, i_\Phi \end{matrix}\right\} & \begin{matrix} \textit{during } t_{on,\Phi} \\ \textit{during } t_{off,\Phi} \end{matrix} \end{cases} \tag{11}$$

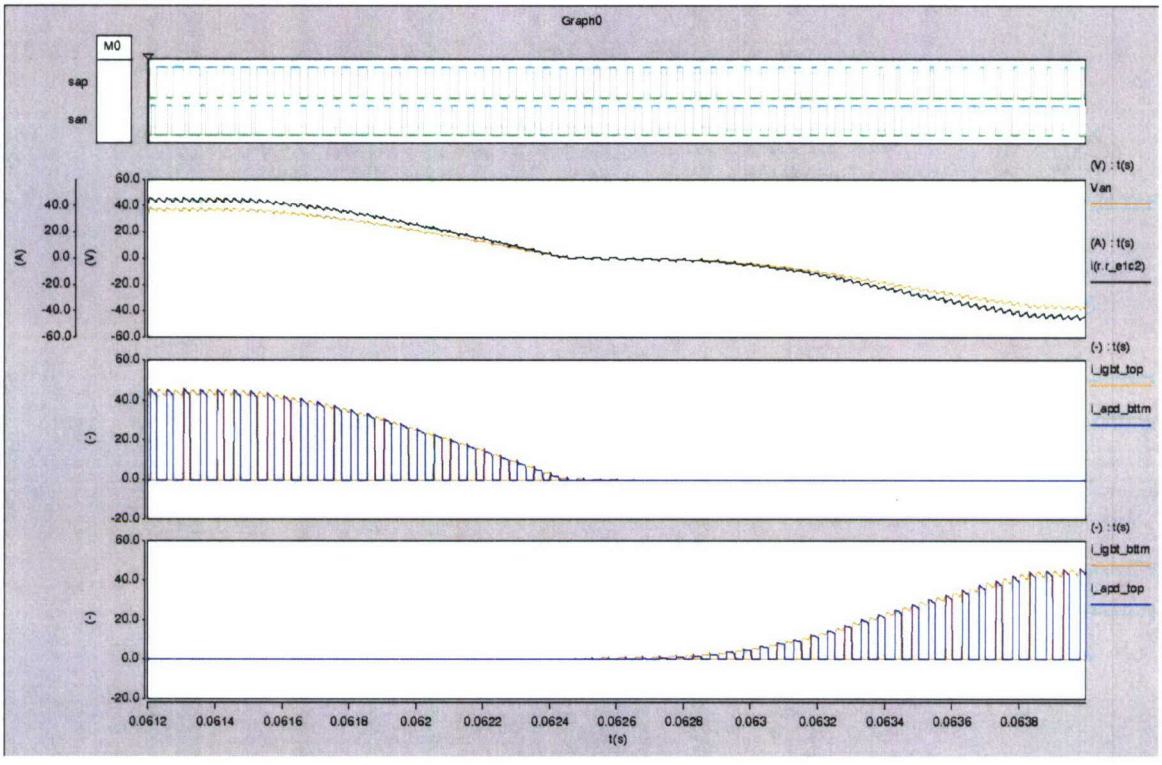


Fig. 11-16 Waveforms showing when "IGBTs" and "APDs" are conducting

It is further noted that voltage across the inductor of the "IGBT", V_{Lon}, complicates the equations greatly; however this voltage can be ignored when averaging. This voltage can be neglected because, when averaged over a switching period, it is very small compared to the other voltages, especially V_{Φ}. The fact that this voltage can be neglected can be seen in Fig. 11-17 in the following page.

Though the inductor voltage in the "IGBTs" is ignored for the average model, it is still very important, and should not be ignored for the switching model. The losses associated with the inductor help accurately model the ripple and instantaneous transients in the switching model.

Since V_{Lon} can be ignored, (11) is reduced to that in (12).

$$V_S = \begin{cases} V_{IGBT} + R_{IGBT}\, i_{\Phi} \\ V_{APD} + R_{APD}\, i_{\Phi} \end{cases} \begin{matrix} during\ t_{on,\Phi} \\ during\ t_{off,\Phi} \end{matrix} \tag{12}$$

Averaging (12), the average voltage drop across the switching cells of the phase-leg is as follows:

$$\langle V_S \rangle_{T_S} = \overline{V}_S = d_{\Phi}\left[V_{IGBT} + R_{IGBT}\, i_{\Phi}\right] + d'_{\Phi}\left[V_{APD} + R_{APD}\, i_{\Phi}\right] \tag{13}$$

Plugging (8) into (13), the average switching cell voltage is obtained as a function of d_{Φ}

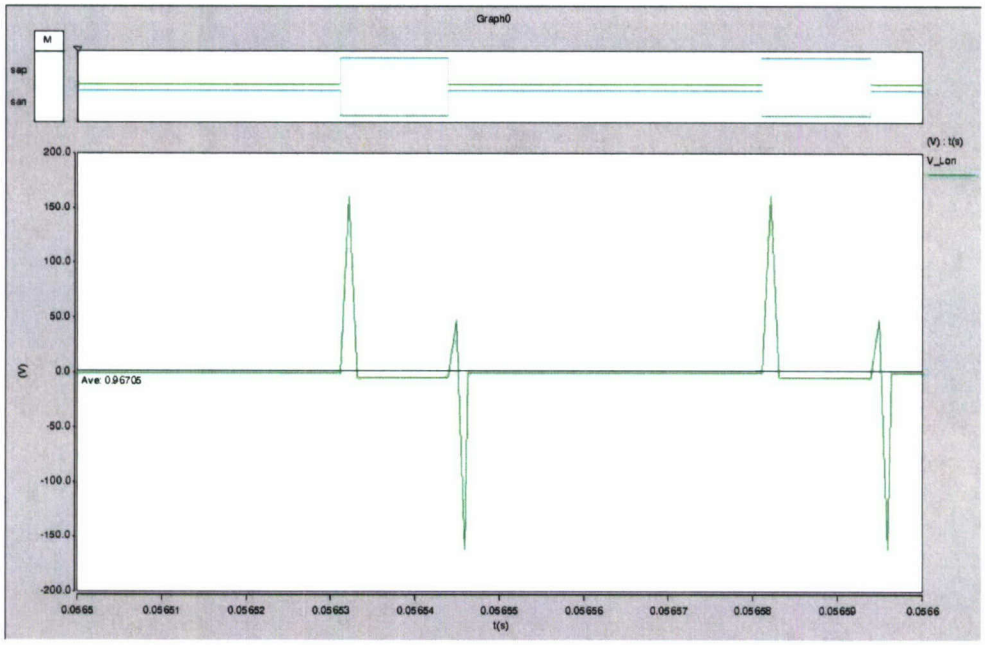


Fig. 11-17 Waveform showing that VLon is negligible over a switching period

$$\overline{V}_S = d_\Phi \left[V_{IGBT} + R_{IGBT}\, i_\Phi\right] + \left(1 - d_\Phi\right)\left[V_{APD} + R_{APD}\, i_\Phi\right]$$
$$let\ \delta_\Phi = d_\Phi\, i_\Phi,\ \therefore$$

$$\overline{V}_S = d_\Phi V_{IGBT} + R_{IGBT}\delta_\Phi + V_{APD} + R_{APD}\, i_\Phi - d_\Phi V_{APD} - R_{APD}\delta_\Phi$$
$$= d_\Phi \left[V_{IGBT} - V_{APD}\right] + \delta_\Phi \left[R_{IGBT} - R_{APD}\right] + V_{APD} + R_{APD}\, i_\Phi \qquad \textbf{(14)}$$

Defining the following vectors:

$$\vec{d}_{abc} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix},\ \vec{i}_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix},\ \vec{\delta}_{abc} = \begin{bmatrix} d_a i_a \\ d_b i_b \\ d_c i_c \end{bmatrix},\ \vec{V}_{abc} = \begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} \qquad \textbf{(15)}$$

and combining (9) and (14), the vector equation for the voltage loop can be written as follows:

$$L\frac{d}{dt}\vec{i}_{abc} = \vec{d}_{abc} V_{DC} - \vec{V}_{Sabc} - \vec{i}_{abc}\, 2R_{CU} - \vec{V}_{abc}$$

where:

$$\vec{V}_{Sabc} = \vec{d}_{abc}\left[V_{IGBT} - V_{APD}\right] + \vec{\delta}_{abc}\left[R_{IGBT} - R_{APD}\right] + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} V_{APD} + \vec{i}_{abc} R_{APD} \qquad \textbf{(16)}$$

IV.2. Current equations

Writing current equations for the VSI, it is found that

$$i_{DC} = \vec{d}_{abc}^{\,T}\, \vec{i}_{abc} \tag{17}$$

$$\vec{i}_{abc} = \frac{\vec{V}_{abc}}{R} \tag{18}$$

In a VSI system, like the one seen in Fig. 11-15 the converter usually contains output filter capacitors in parallel with the load resistors. These are not implemented in the current hardware setup, and this is reflected in (18). If these capacitors were to be applied to the hardware setup, then (18) becomes that in (19).

$$C\frac{d}{dt}\vec{V}_{abc} = \vec{i}_{abc} - \frac{\vec{V}_{abc}}{R} \tag{19}$$

IV.3. Average Model

Using (16), (17) and (19), the block diagram shown in Fig. 11-18 can be drawn.

The capacitors in Fig. 11-18 are dashed to show that they are not implemented in hardware, but in a proper VSI they would exist. Also, when this average model is converted to the DQ0 coordinate system, the capacitors will couple states together, and have a noticeable impact on the system.

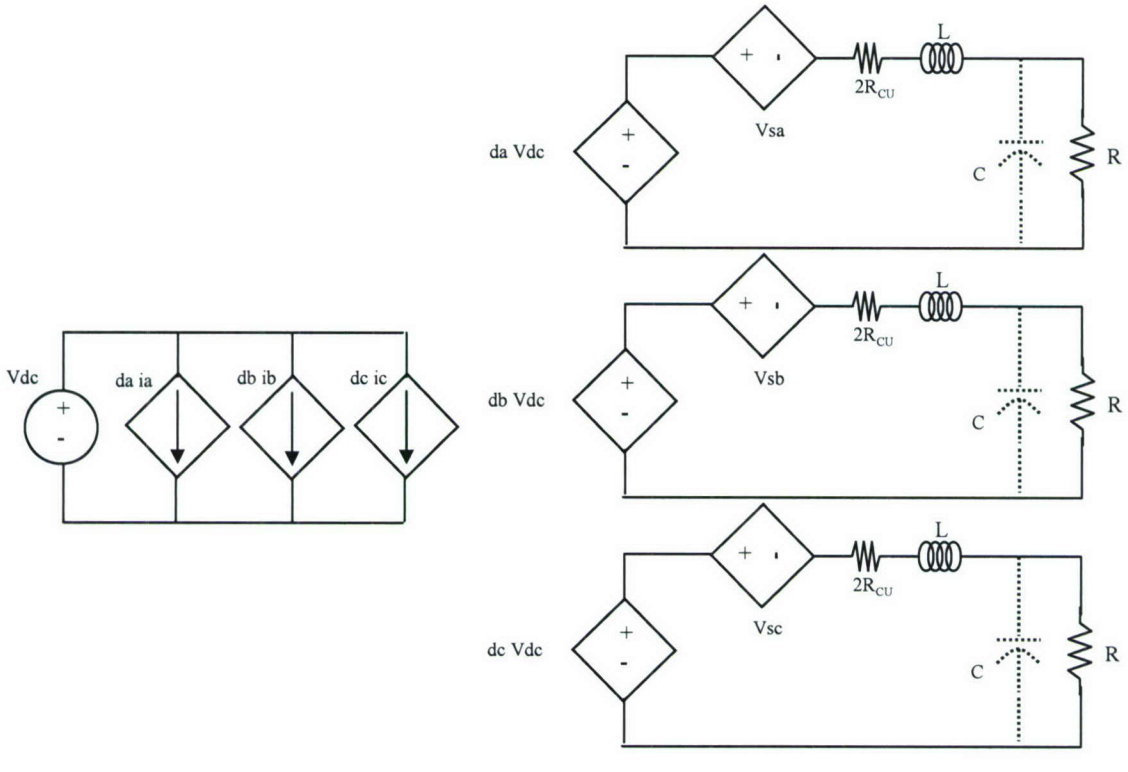


Fig. 11-18 Average model of 3Φ-VSI

The average model of a PEBB phase-leg can be extracted from the average model of the VSI in Fig. 11-18, and can be seen in Fig. 11-19.

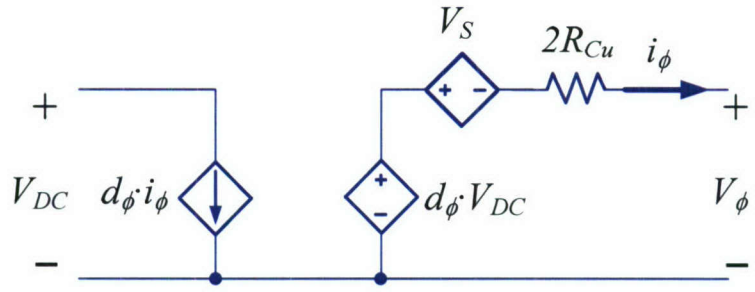


Fig. 11-19 Average model of PEBB phase-leg with losses

Using the average model of the PEBB phase-leg to create the 3Φ-VSI system depicted in Fig. 11-18 (without the capacitor) in simulation, and using the second set of OL test conditions that were used in the switching model simulation, the following waveform in Fig. 11-20 was acquired.

Comparing the switching and average model waveforms, Fig. 11-21, it is seen that the average model overlaps the switching model's waveform; which verifies the accuracy of the average model to the switching model.

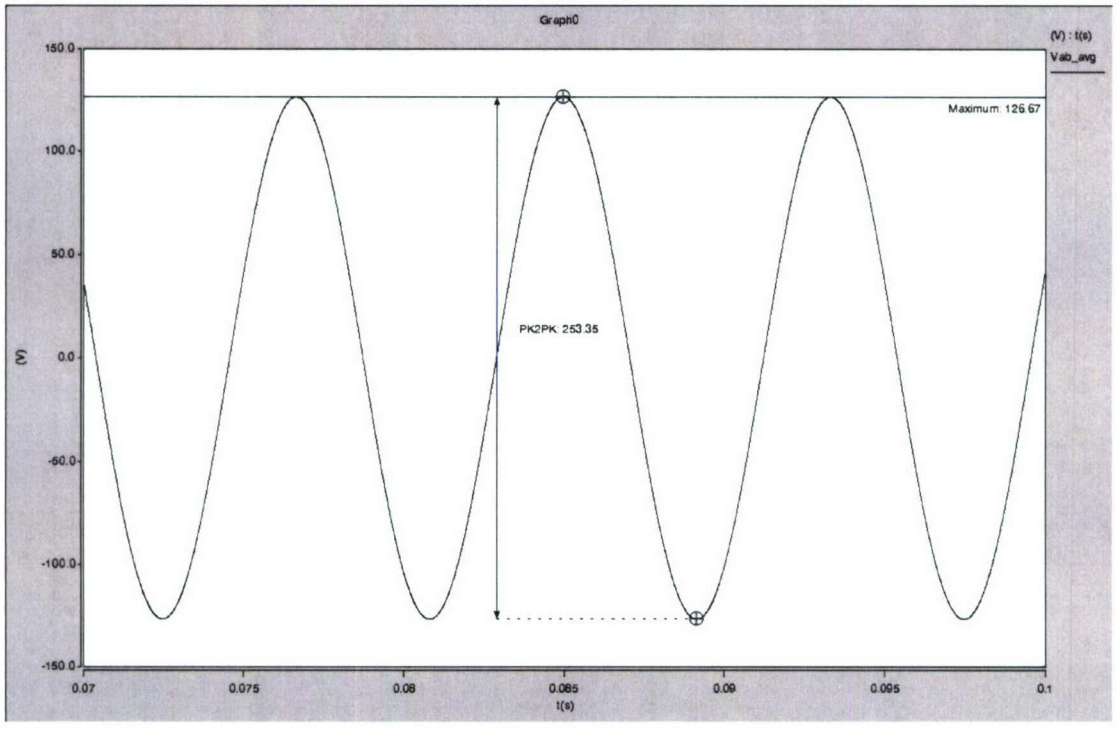


Fig. 11-20 Line-to-Line Voltage from average model simulation

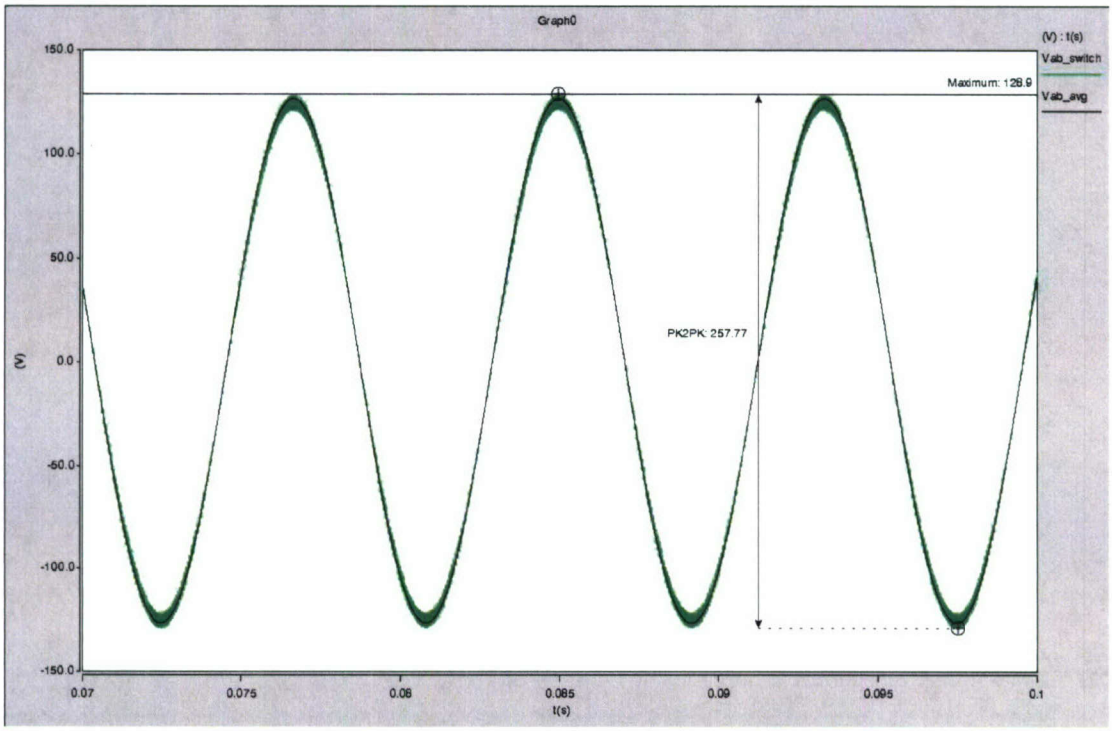


Fig. 11-21 Comparison of Switching and Average model waveforms

V. PEBB Switching Model in VTB

In order to take advantage of the great modularity and ease of usage of PEBB systems, not just for their actual usage but for modeling, design and simulation purposes, the PEBB model under consideration was also developed in VTB (virtual test bed). VTB has an advanced graphics capability and a flexible user interface, which combined with the modularity of PEBB's per se make it a powerful simulation tool.

The PEBB model was developed based on the PEBB modeling and simulation of voltage-source converter systems. Fig. 11-22 shows some basic topologies implemented with a phase-leg PEBB. The PEBB model is built per the transfer function concept in terms of a simple single-pole double-throw (SPDT) switch as shown in Fig. 11-23. The PEBB model in VTB is built over an IPM hierarchical model, which is later combined with the controls and passive components in order to create a higher hierarchical entity under the name PEBB. In a first approach to the IPM modeling, the IGBT model Level-I included in VTB was employed. Default parameters of this transistor model were modified to meet the parameters and performance of the IPM used, Mitsubishi IPM PM300DVA120. The model of such IGBT is shown in Fig. 11-24. In this figure, Rs is actually a voltage-controlled resistor which simulates the ideal switch, changing from 80 μΩ to 1MΩ, depending on the value of the controlling voltage V8. Accordingly, the on and off states of the switch are realized. Re and VE are the forward resistance and voltage, respectively, and they are temperature dependent. In this model, the delay in the switching on/off is simulated by means the Rg-Cg network connected in the gate circuit. The lower part of the figure represents the thermal equivalent circuit used to calculate the junction temperature based on data sheet parameters.

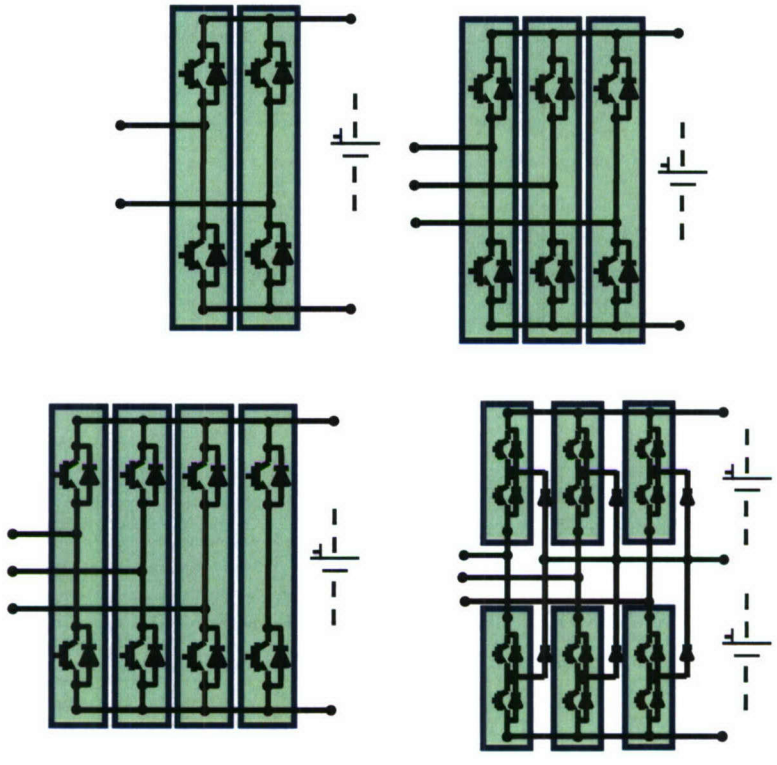


Fig. 11-22 Voltage-source converters with phase-leg PEBB modules.

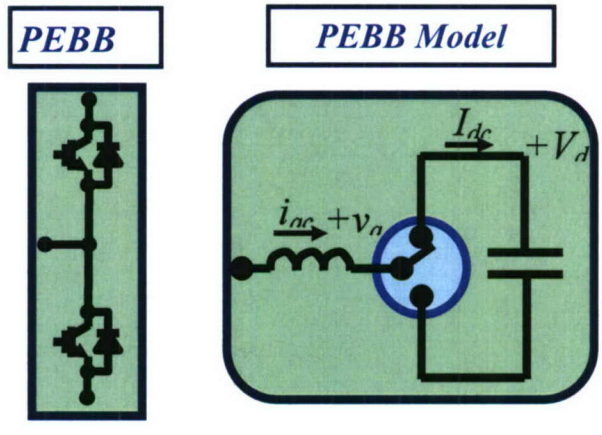


Fig. 11-23 PEBB model and equivalent circuit using an SPDT switch.

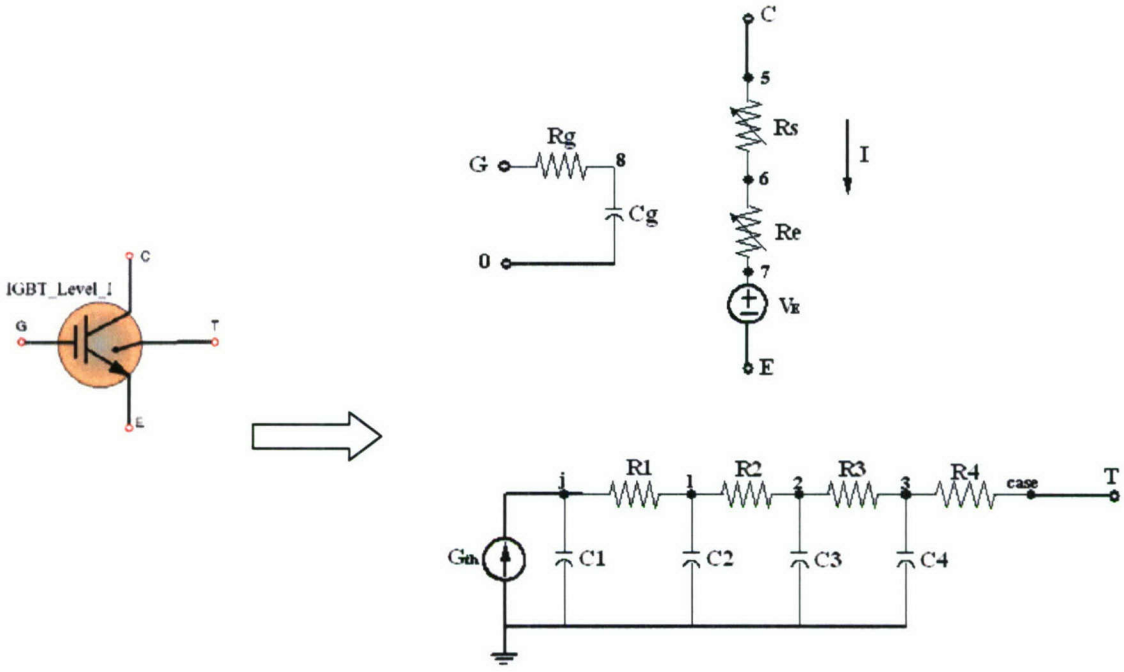


Fig. 11-24 VTB model for IGBT Level-I

The model depicted in Fig. 11-24 shows how may be studied the thermal and transitory phenomena in IGBT using VTB capabilities. However, in order to speed up the simulation process, a simpler yet accurate model was developed and shown in Fig. 11-25.

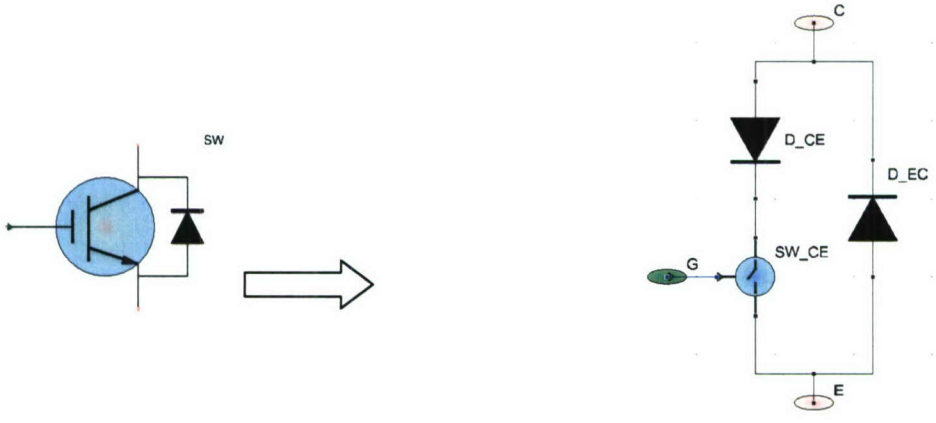


Fig. 11-25 Linearized model for the IGBT and the antiparallel diode

In the model of Fig. 11-25, the switch SW_CE is actually a discrete controlled resistance, presenting six programmable resistance states when it switches from *on* to *off* and vice versa. In this model, the diode D_CE avoids any reverse current circulation and simulates the forward voltage and resistance. The diode D_EC is the antiparallel diode. Both diodes respond to the model shown in Fig. 11-7 and the value of its parameters were justified in Section II.

The IPM model is shown in Fig. 11-26. In this case, the VTB model for the IGBT Level-I has been used, for this reason, the antireverse and antiparallel diodes has been explicitly connected. In this IPM model, the port Pt3 offers the package temperature.

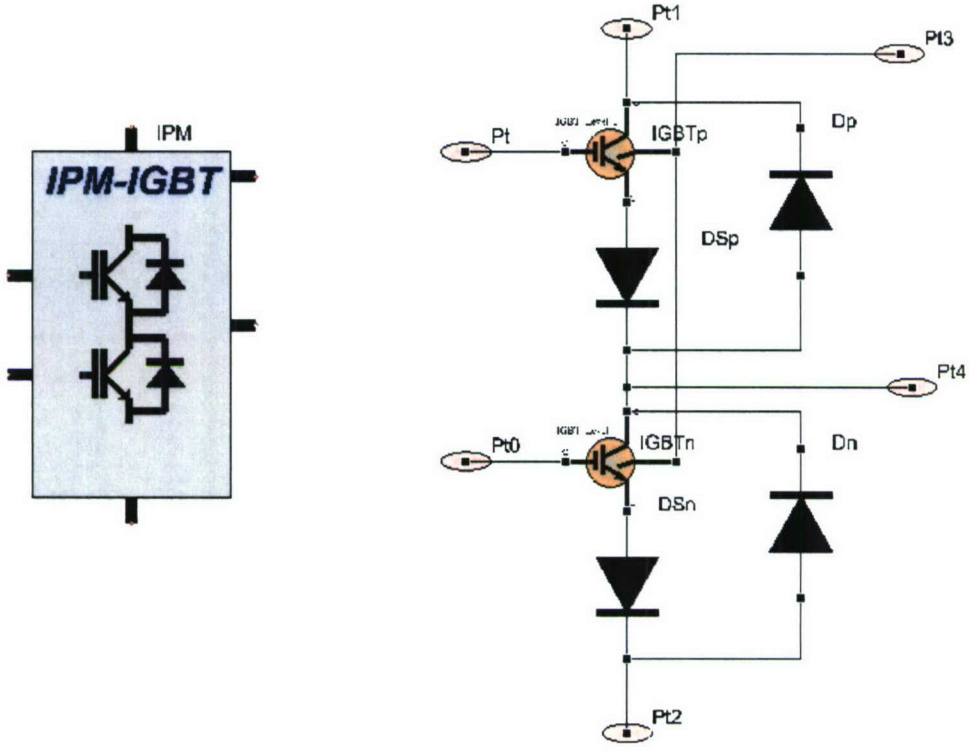


Fig. 11-26 IPM block model using IGBT Level-I.

Fig. 11-27 shows the structure of the IPM hierarchical block when the linearized models (presented in Section II) for the IGBT and the antiparallel diode are used. An important difference between the models of Fig. 11-26 and Fig. 11-27 is the type of signals used for their control. In the model of Fig. 11-26, the IGBT switching action is implemented by means of a variable resistance and the IGBT gate is driven by electrical signals supplied by a voltage source. In the model of Fig. 11-27 on the other hand, the IGBT switching action is realized by an ideal switch which is directly driven by the command control signal as shown in Fig. 11-25. In such switch, the control signal can only take discrete integer values from 1 to 6, being possible to program the resistance value corresponding to each one of these six switching states. In this case, the resistance for the state 1 was of 1mΩ, whereas for the state 6 was of 1MΩ (the rest of the states took intermediate resistance values). This kind of discrete control signals is processed faster than an analogical signal based on float point numbers. Moreover, using only two of the six switching states, it is possible to achieve a boolean behavior, which makes easier the design of the driver.

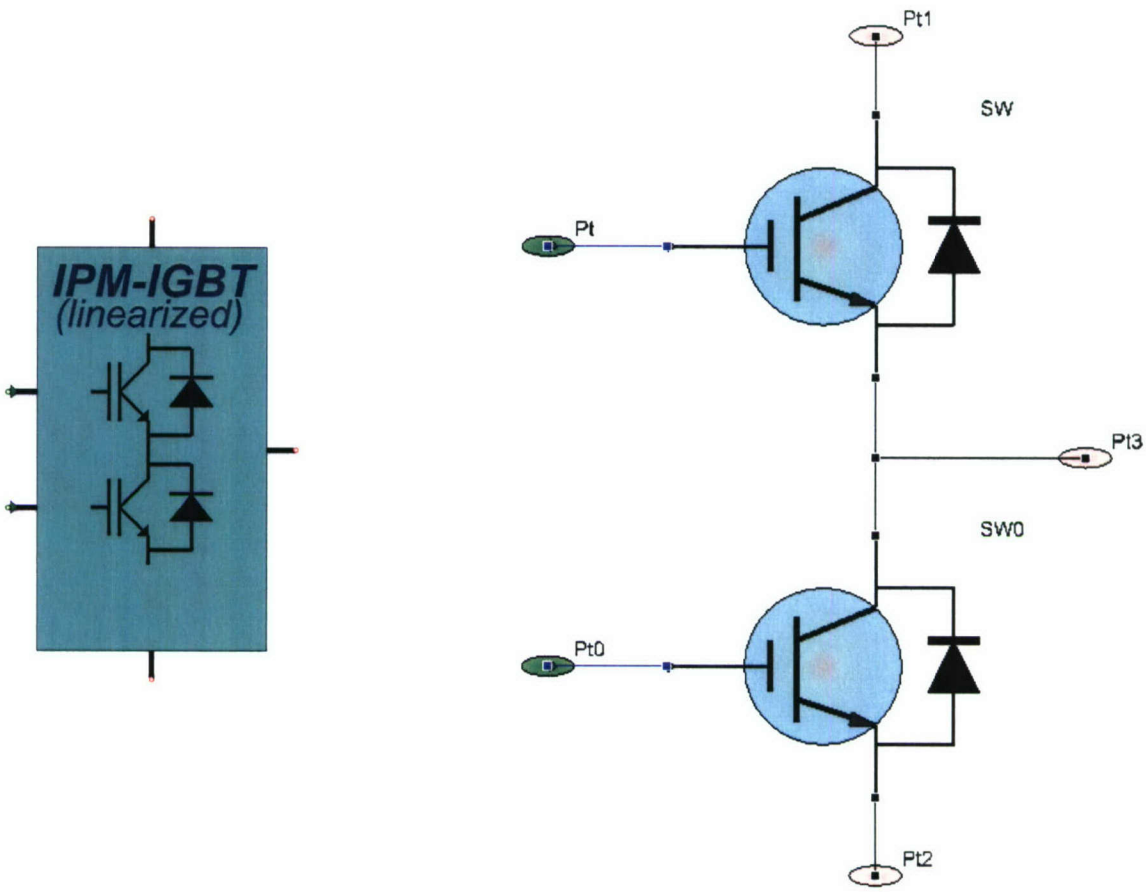


Fig. 11-27 IPM block model using ideal IGBT models.

The gate drivers of the IPM based on IGBT's Level-I are implemented in a hierarchical entity. The components of this block are shown in Fig. 11-28, consisting of carrier-based S-PWM, a deadtime generator and the controlled voltage sources driving the IGBT gates. Fig. 11-29 shows the content of a similar gate driver block, but now the output signals are adapted to control the IPM based on idealized IGBT's.

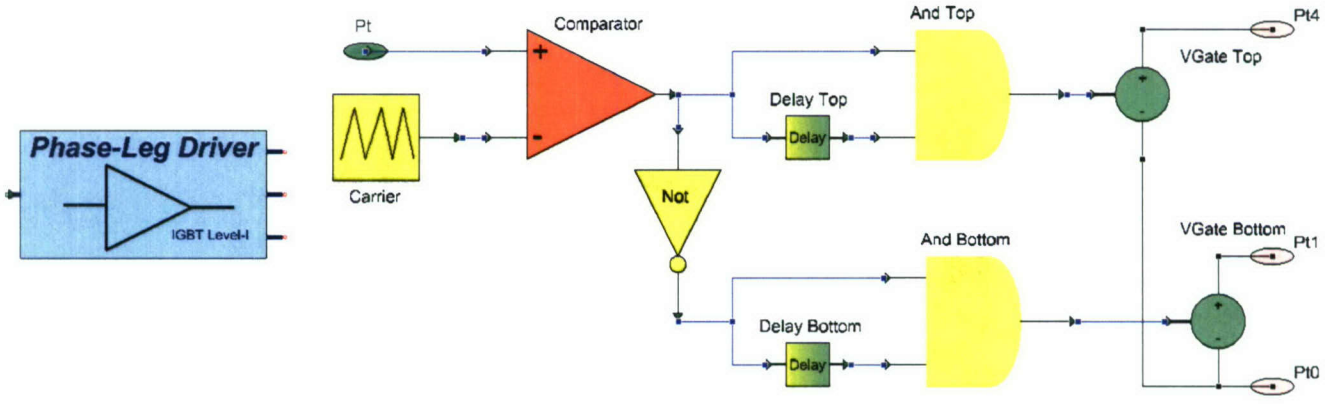


Fig. 11-28 Gate-driver block for the IPM using IGBT Level-I model.

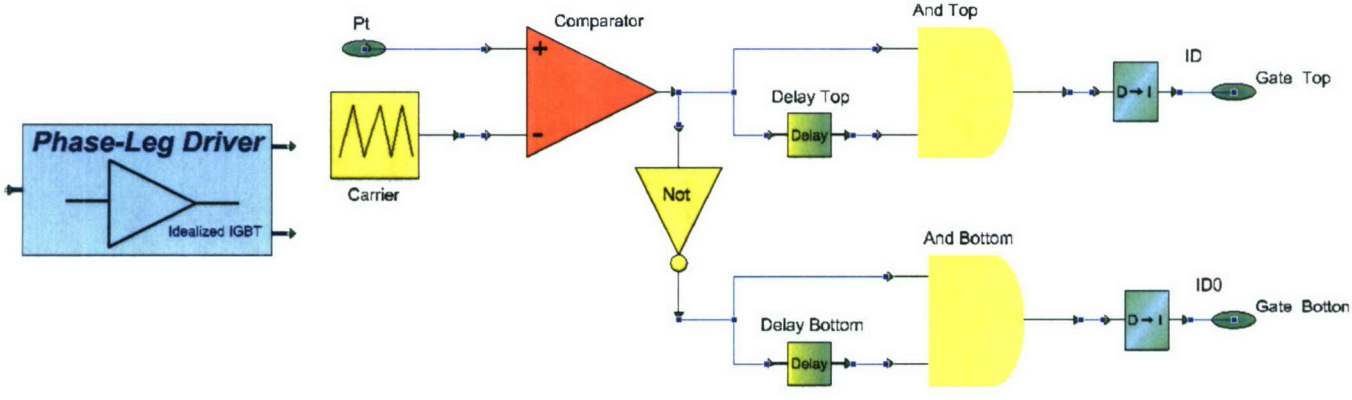


Fig. 11-29 Gate-driver block for the IPM using the idealized IGBT model.

Finally, the PEBB block comprising the IPM and phase-leg driver circuits is shown in Fig. 11-30. In this case, the PEBB is implemented using IGBT's Level-I, existing another idealized PEBB based on the IPM of Fig. 11-27 and the gate driver of Fig. 11-29.

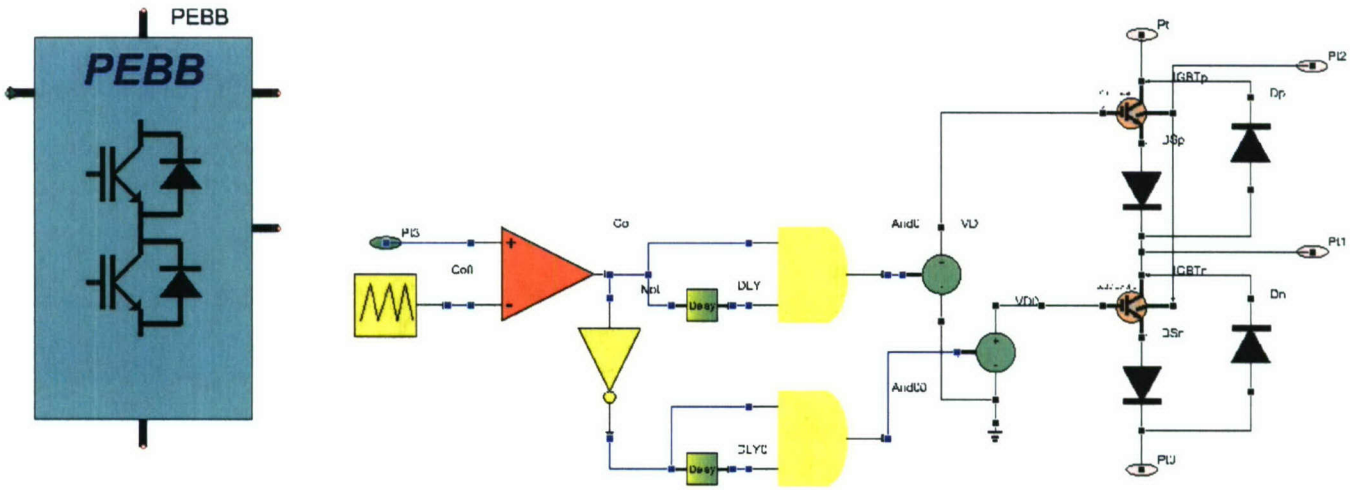


Fig. 11-30 PEBB hierarchical model in VTB.

The block shown in Fig. 11-30 can be simply drag and drop to form different converters as the ones shown in Fig. 11-31.

In order to show the ease of implementation of PEBB-based systems and the actual ease of simulation under VTB, Fig. 11-32 presents some simulation results using a single PEBB operating in dc mode (buck dc-dc converter). These simulation results include: dc power supply voltage and current, output filter voltage and current, current through the respective PEBB switches, as well as the instantaneous power dissipation in the PEBB and the IGBT junction temperature evolution. The advantage of this approach is the simple drag and drop process required to set up such a simulation. Just as in real PEBB systems, the complexity of power electronics is withhold within the PEBB for the power electronics specialist, delivering the system designer from them.

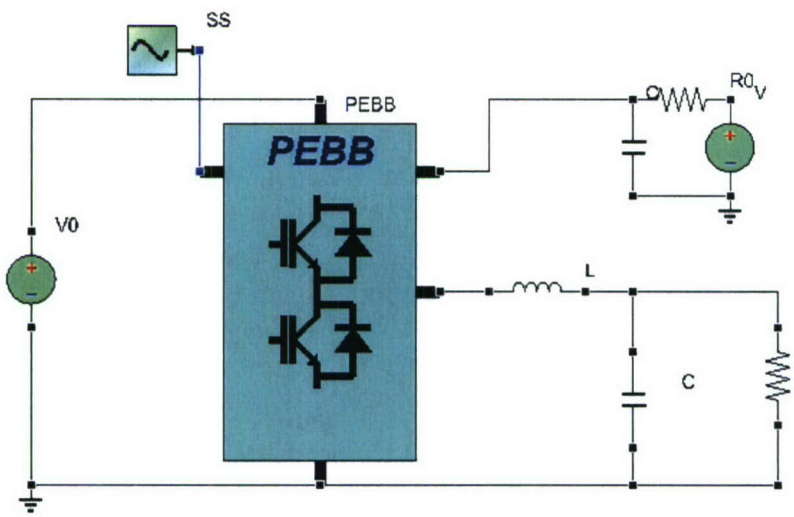


Fig. 11-31 DC-DC buck converter implemented with a single PEBB module.

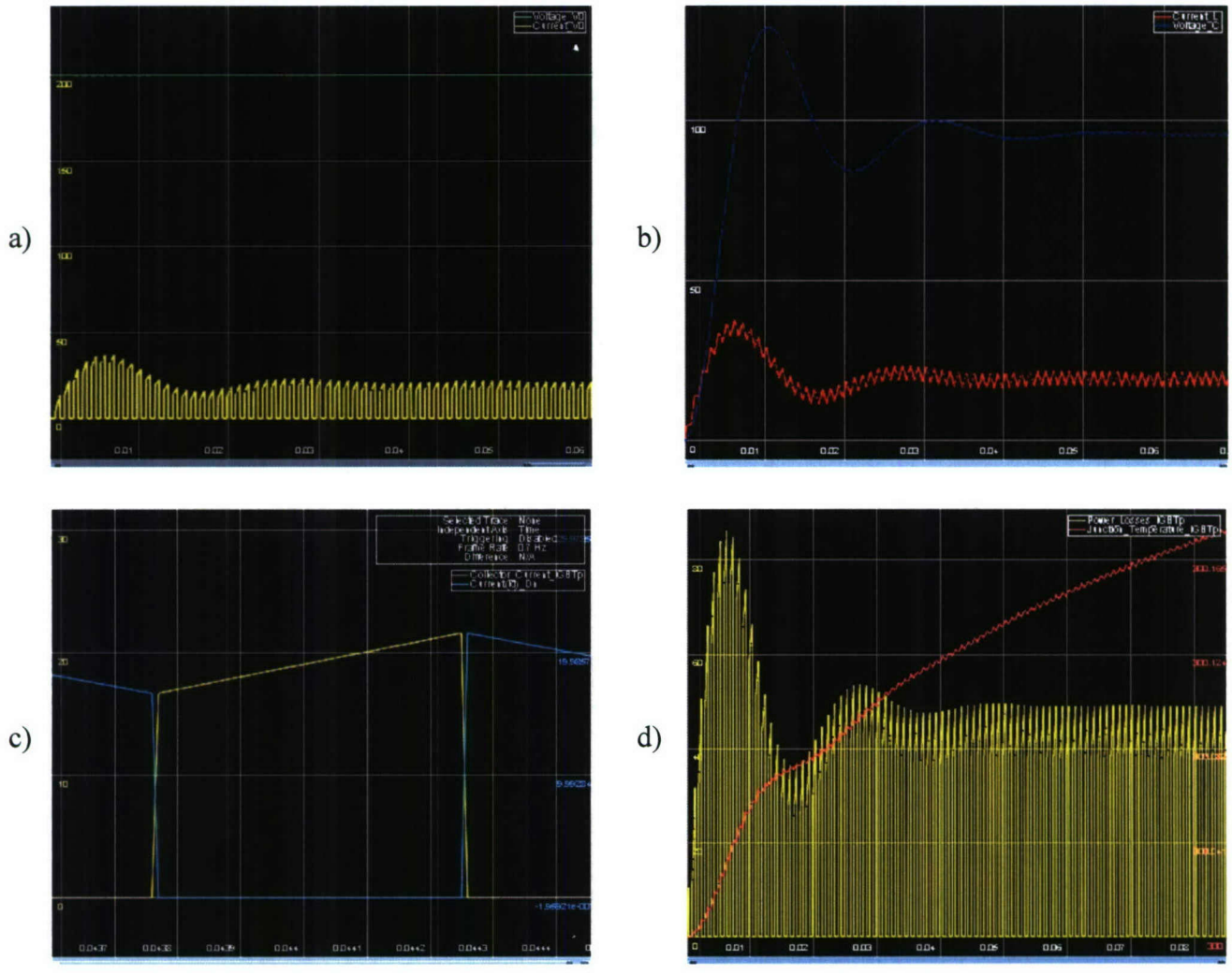


Fig. 11-32 Simulation results of single PEBB converter operating in dc-mode. Figures show a) Input voltage and current, b) output voltage and current, c) IGBT and diode current, and d) power losses and junction temperature.

Another simulation example of a PEBB-based system simulated under VTB is shown in Fig. 11-33. In this case, from the earlier dc-dc converter, and simply by adding another PEBB module, a single phase inverter can be implemented provided appropriate control signals are generated. The resultant simulation waveforms are depicted also in Fig. 11-33 showing the dc power supply voltage and ripple current, as well as the output ac voltage and current.

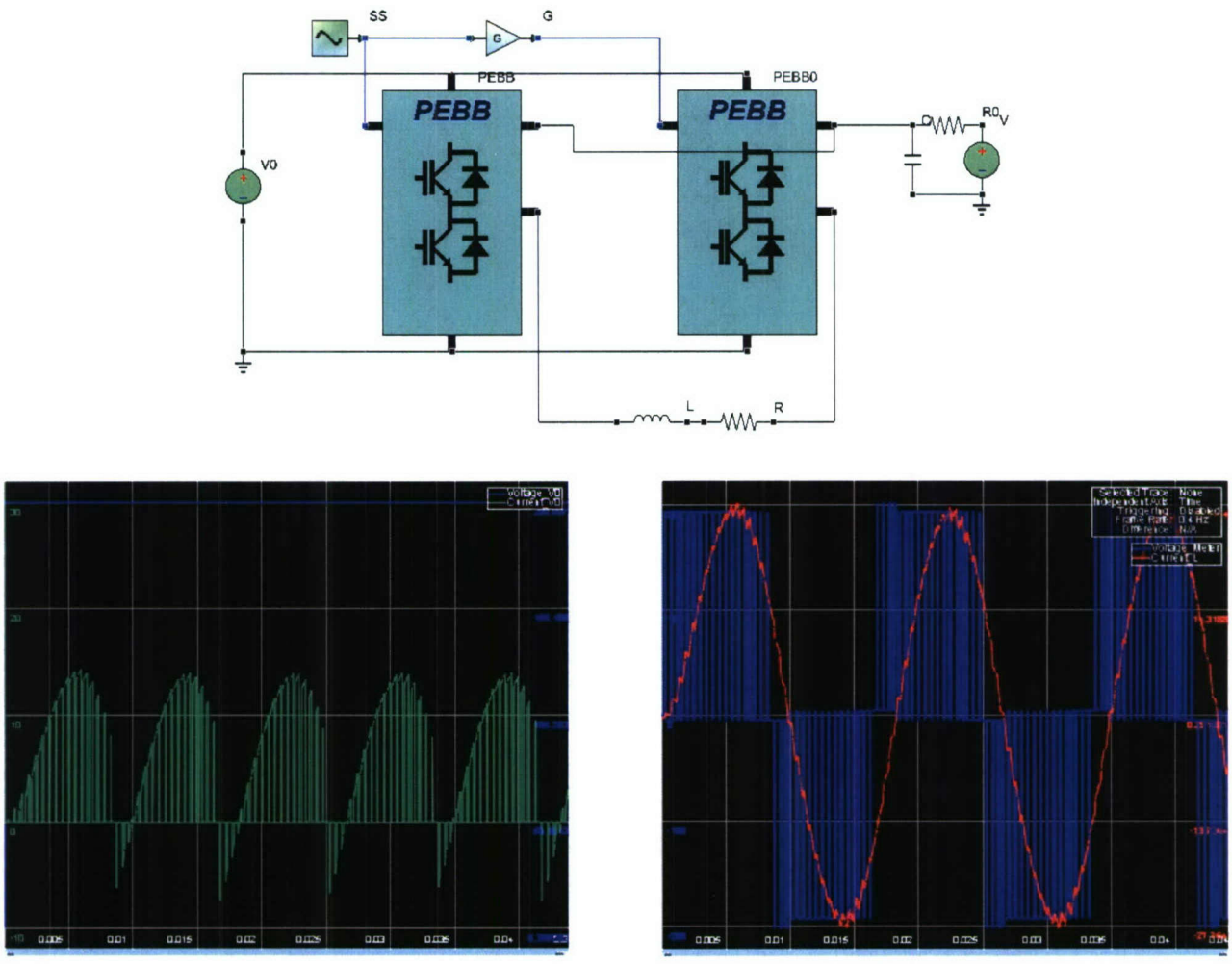


Fig. 11-33 Single phase voltage-source inverters with two PEBB modules feeding a single R-L load. The waveforms below show the dc voltage and current, and output ac voltage and sinusoidal load current.

As a last example, Fig. 11-34 shows a three-phase voltage source inverter (3Φ-VSI) implementation using three PEBB modules this time. By appropriately connecting the three-phase load and modifying the control signal a three-phase converter may be easily and rapidly simulated in VTB exploiting the PEBB concept. Resultant waveforms of this simulation are shown in Fig. 11-35, depicting the dc voltage and ripple current, output ac line-to-line voltage, output phase-voltage, and line currents.

As seen, the ease of implementation and simulation of PEBB systems in VTB is significant, reducing development times for system studies by a great extent compared to other simulation software. Once the flexibility of the PEBB-based system concept has been evinced, the next step in this study is to develop a hierarchical model for a more realistic three-phase converter coinciding with the actual hardware available in the power electronics lab. In the design of this converter, not only the 3Φ-VSI will be considered, but also the sensors used in the actual hardware.

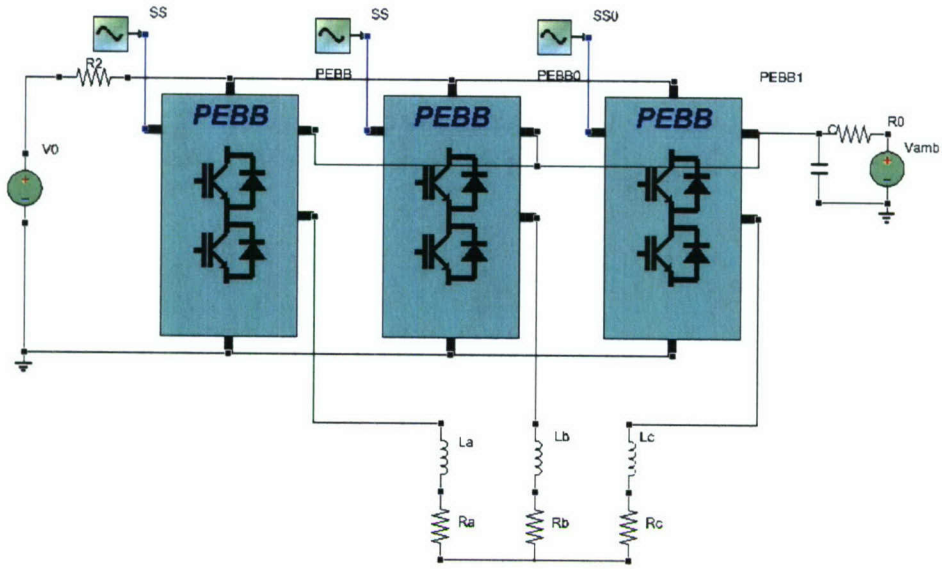


Fig. 11-34 **Three-phase VSI implemented with three PEEB modules and feeding a three-phase R-L load.**

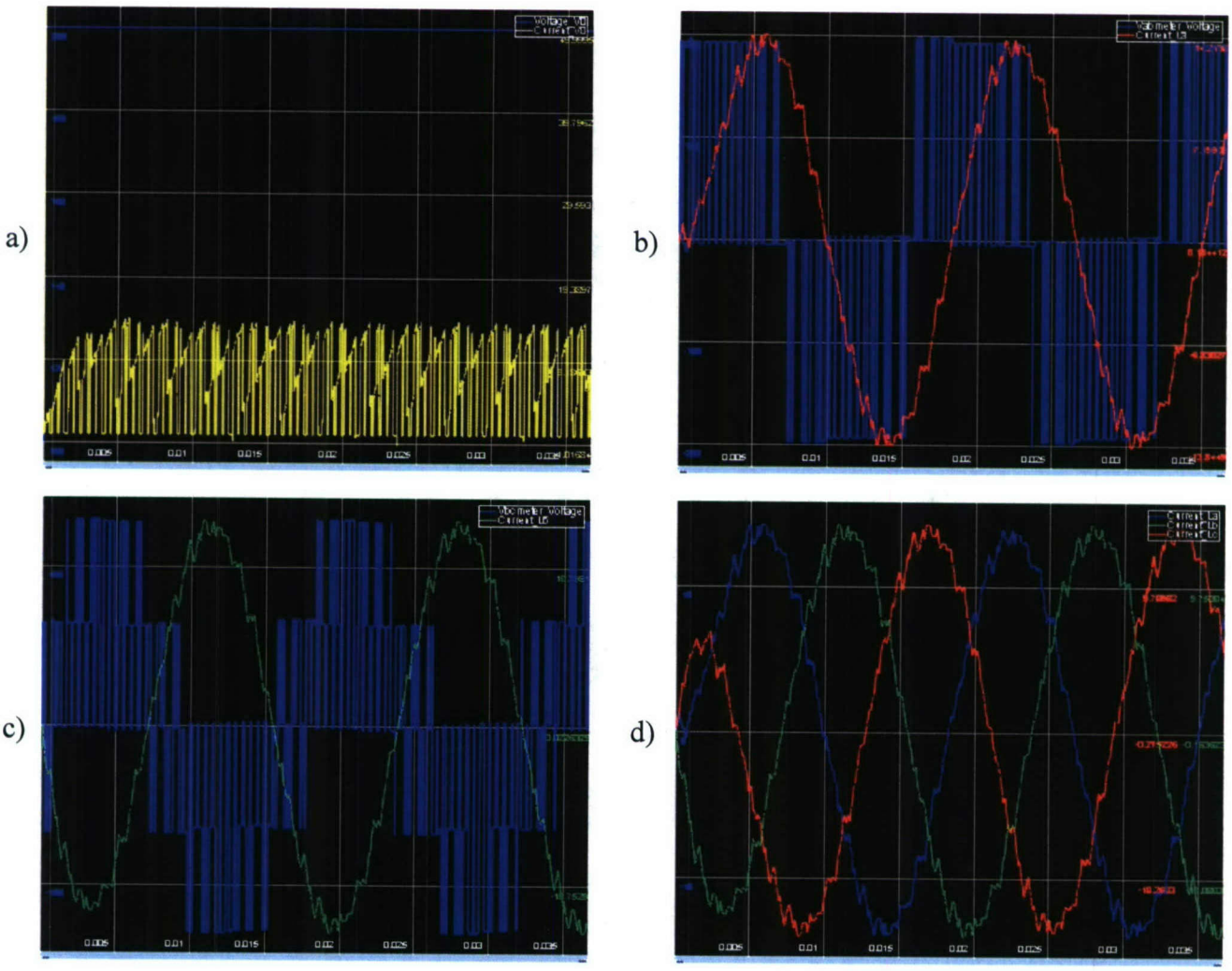


Fig. 11-35 **Simulation waveforms of the three-phase voltage-source inverter. a) DC voltage and current, b) output ac line-to-line voltage and current, c) output phase voltage and current, and d) three-phase currents.**

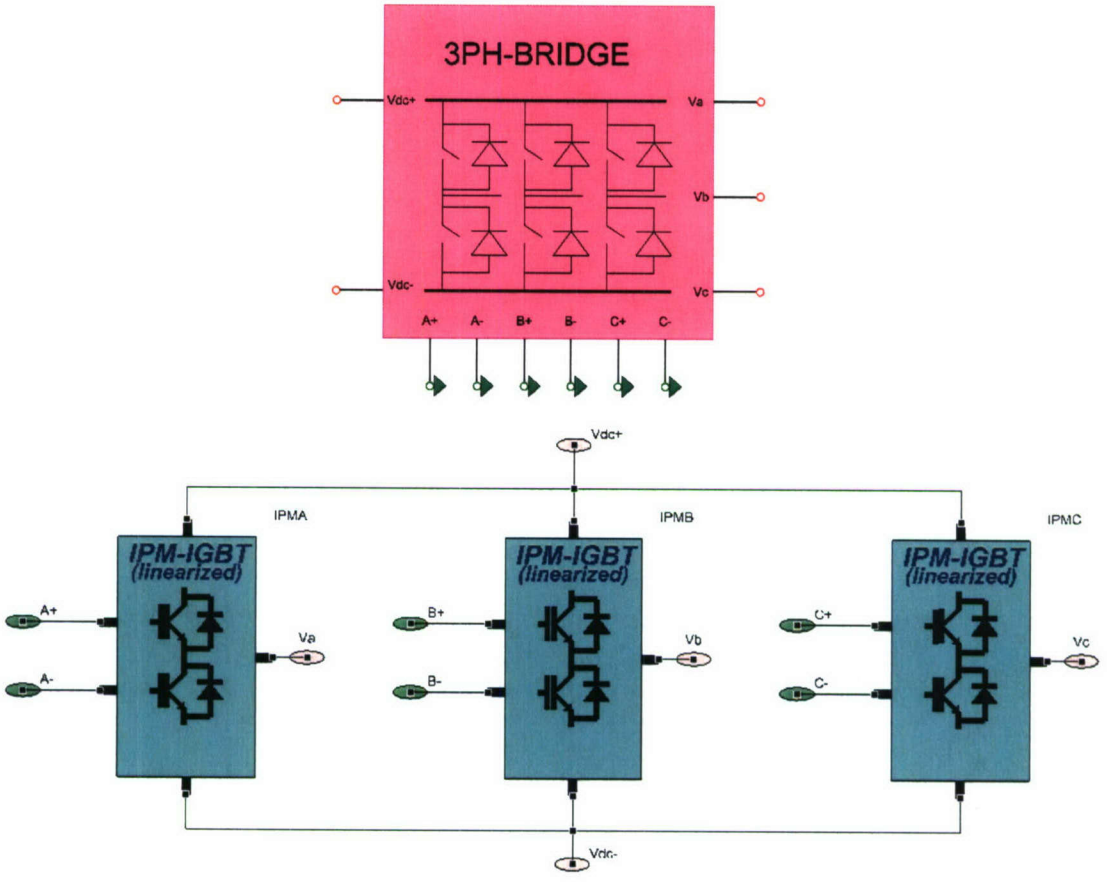


Fig. 11-36 Hierarchical model of the three-phase VSI.

Fig. 11-36 shows the hierarchical structure of the 3Φ-VSI (3PH-Bridge). In this example it is shown how the inverter is implemented by means of three linearized IPM's, however, it has also been implemented as a three-phase inverter based on IPM's with IGBT's Level-I. In such hierarchical block, there is a multiplexed output sensing the temperature in each IPM.

Fig. 11-37 shows the hierarchical block implementing the actual 100kW PEBB converter developed in previous CPES ONR-sponsored projects. This block has the same inputs and outputs as the physical prototype. Therefore, the design in VTB of a controller for this converter should closely match its design using the actual hardware embodiment. The inputs to the converter in Fig. 11-37 are the duty-cycles of the three phase-legs. These inputs are multiplexed constituting a digital control bus. The modulator block demultiplexes this input duty-cycle bus and generates the gate signals for each IGBT by means of the driver blocks like the ones shown in Fig. 11-28 and Fig. 11-29. The outputs of this converter are the signals from the sensing of the phase-leg currents and the DC-bus voltage. In this case, the leg current signals are also multiplexed into a single digital-control output.

Simulations using the model shown in Fig. 11-37 give rise to results that closely match those obtained using the physical prototype. However, when using the IGBT Level-I model to run these simulations, the computational time is significant. This is naturally solved when implementing the average model of the PEBB in VTB, which will be presented hereinafter.

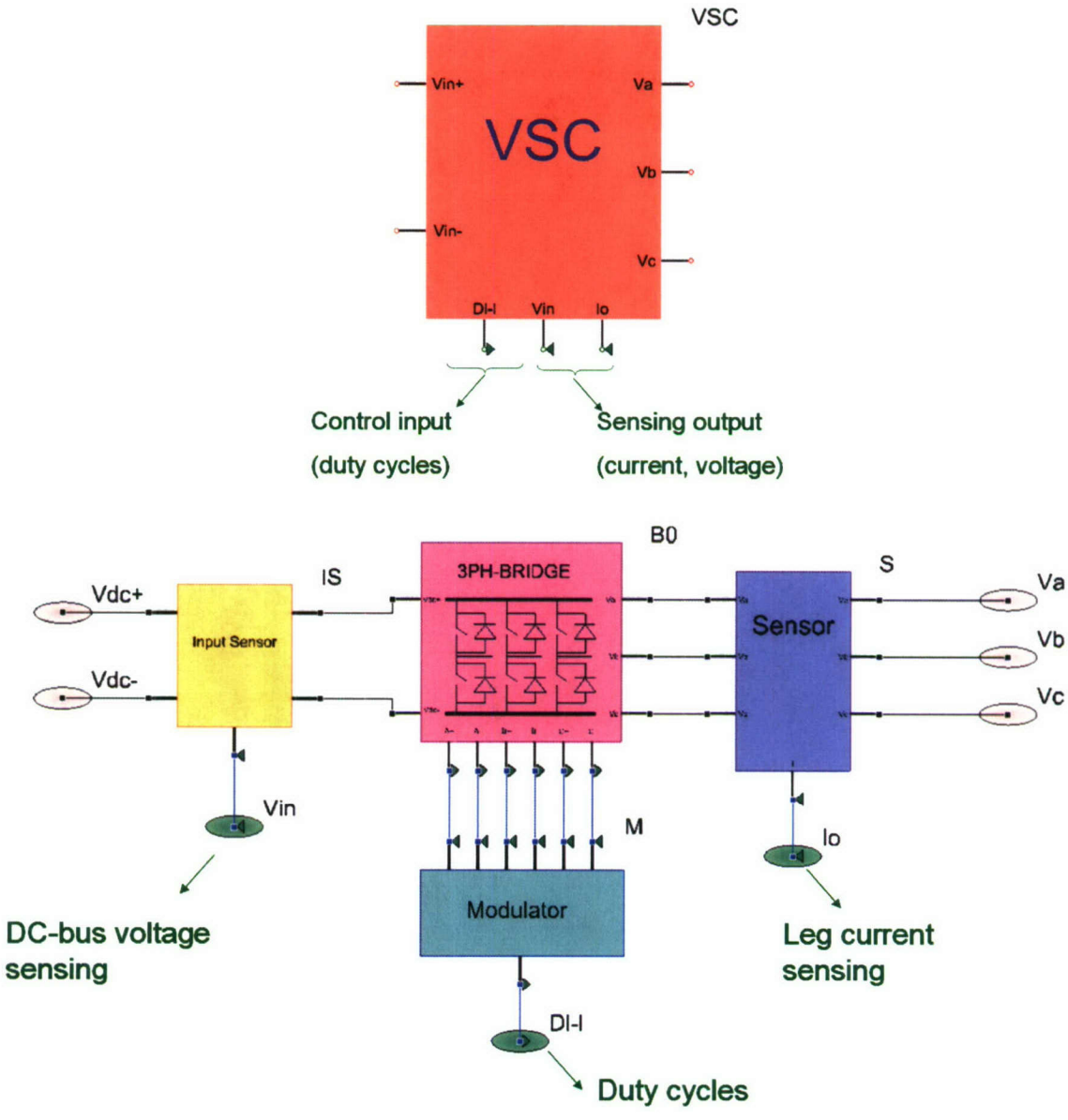


Fig. 11-37 Hierarchical structure of the three-phase converter.

VI. Average Model of PEBB Module in VTB

The average model implementation of the PEBB in VTB is significantly simpler than the corresponding switching model. It just corresponds to the model depicted in Fig. 11-19. Its embodiment and equivalent circuit diagram per the transfer function concept are shown in Fig. 11-38. The ease of usage of this block model is just as for the switching PEBB model. The following figures show the implementation of a single phase inverter and a three-phase inverter using the average PEBB module. Specifically, Fig. 11-39 the circuit schematic of the single-phase inverter implemented with the average PEBB module. As seen, the schematic looks identical to that implemented with the switching PEBB model. The simulation results depicted are the power supply dc voltage and current –with a strong second order harmonic intrinsic to single-phase inverters-, and the output ac voltage and current.

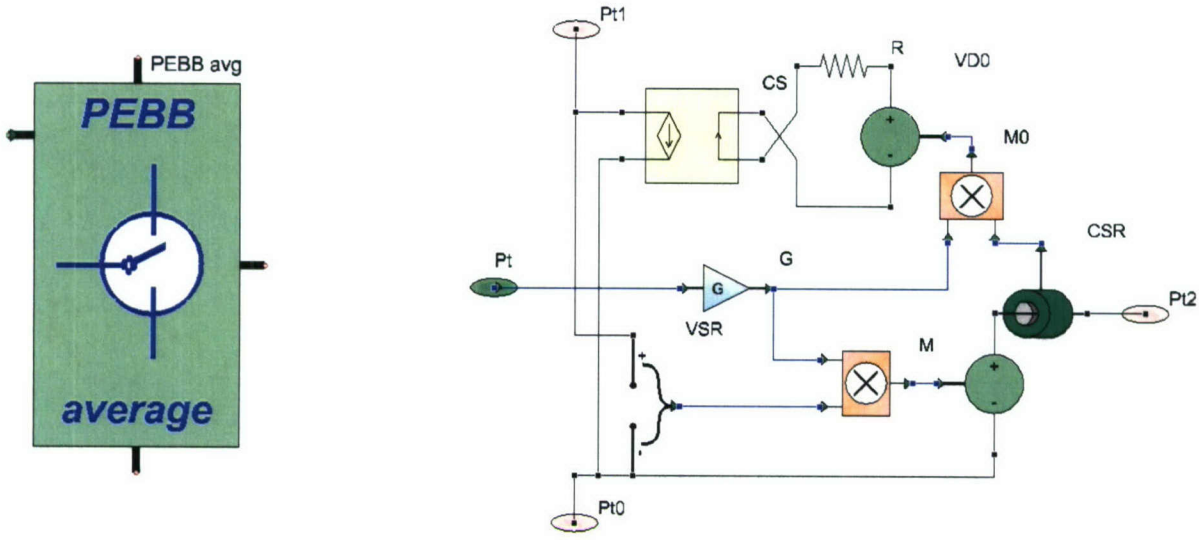


Fig. 11-38 **Average model of the PEBB in VTB, block diagram and equivalent circuit per the transfer function.**

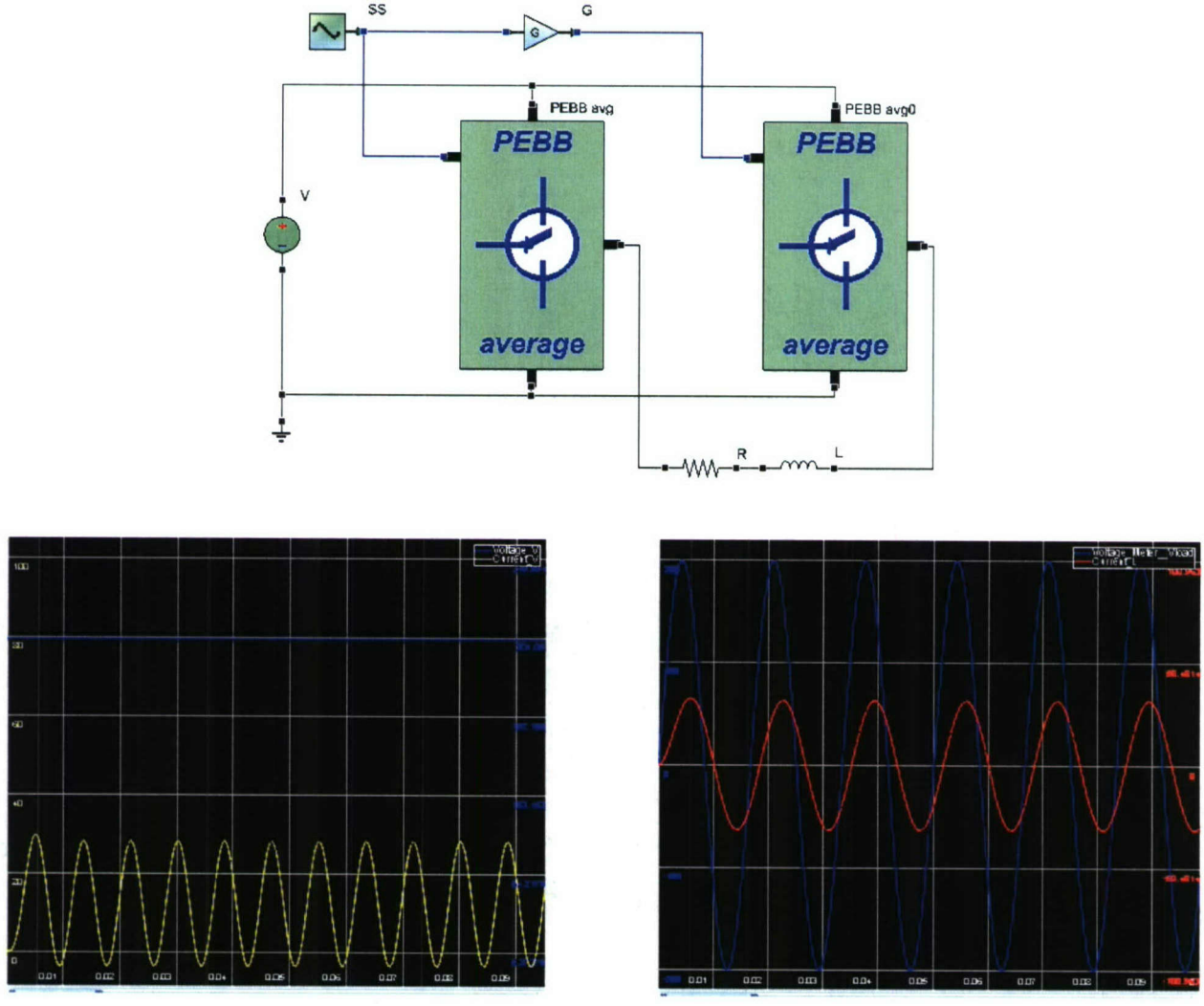


Fig. 11-39 **Single-phase inverter implementation using the two average PEBB modules and resultant simulation waveforms, namely dc voltage and current and ac voltage and current.**

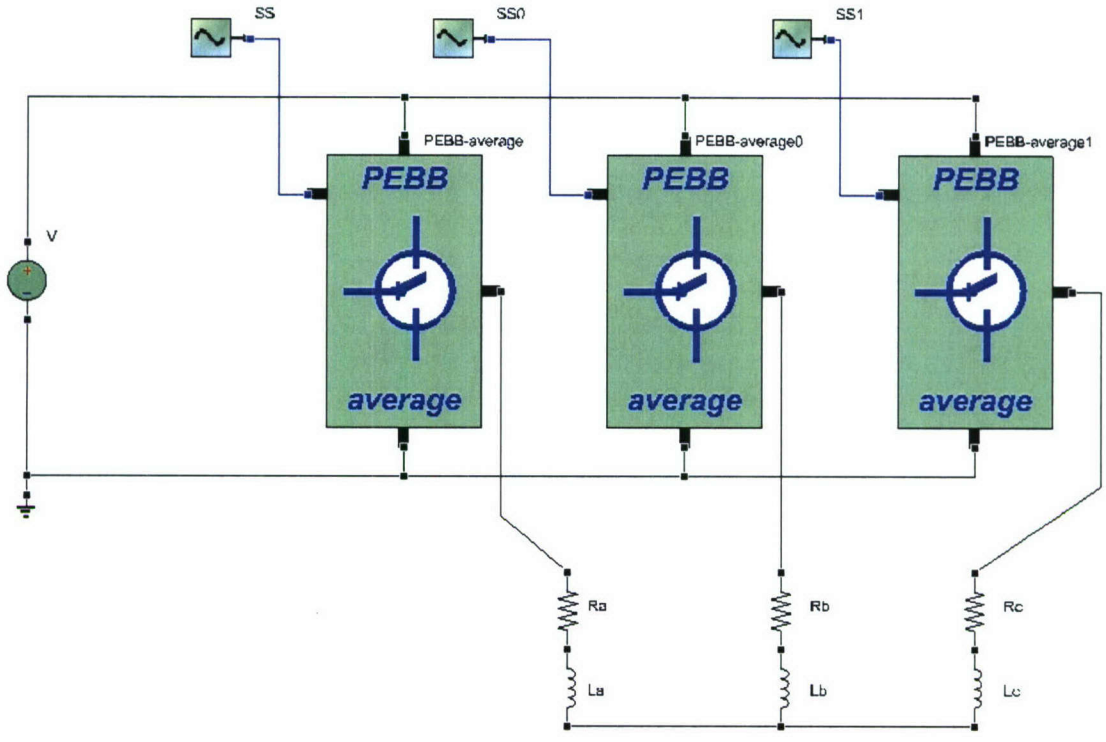
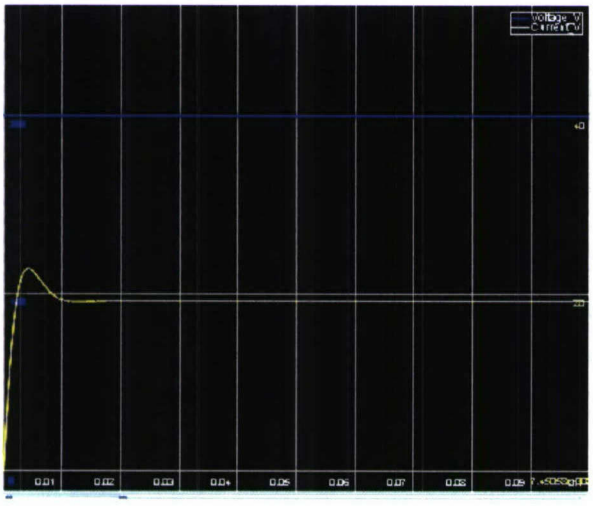


Fig. 11-40 **Three-phase VSI implemented with three PEEB modules and feeding a three-phase R-L load.**

Fig. 11-40 shows the schematic of a three-phase inverter implemented with the average PEBB module. It's diagram also looks identical to that of the switching model, thus making apparent the ease of implementation and simulation of PEBB-based power conversion systems in VTB. Fig. 11-41 and Fig. 11-42 show the resultant waveforms, respectively dc power supply voltage and current, output line-to-line voltage, output line currents, and the currents drawn by one, two and all three PEBB modules seen from the dc side.

a)



b)

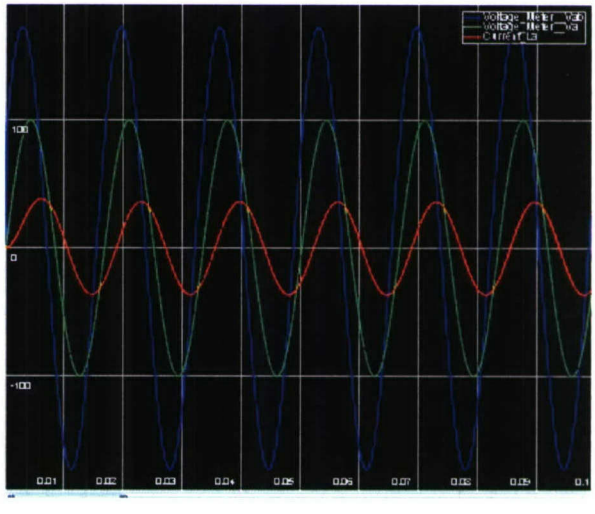
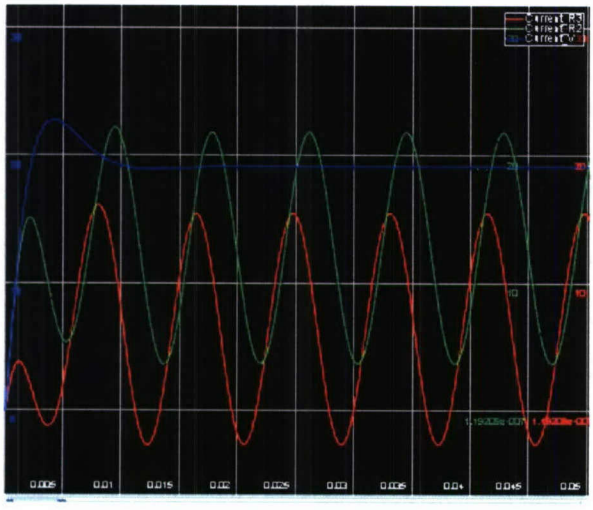


Fig. 11-41 **Simulation waveforms of the three-phase voltage-source inverter with average PEBB modules. a) DC voltage and current, b) output ac line-to-line voltage, phase voltage, and line current.**

a)



b)

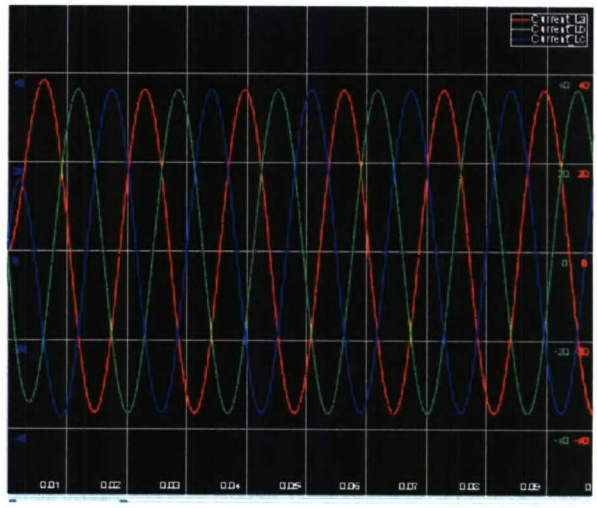


Fig. 11-42 **Simulation waveforms of the three-phase voltage-source inverter with average PEBB modules. a) Dc current output phase voltage and current, and b) three-phase currents.**

VII. Universal Controller in VTB

Once the PEBB-based converter has been modeled and simulated, it is necessary to devote one's attention to the simulation of the controls of such converter. Flexibility and modularity of the PEBB concept should go together with a modern control system meeting the same requirements. Therefore, the synchronous distributed digital control architecture proposed as part of PEBB Plug and Play ONR-sponsored project at CPES becomes an attractive alternative to implement the controls of PEBB-based systems. This control architecture is basically implemented by means of the Universal Controller (UC), which is responsible for all control functions that are supervisory in nature to any PEBB, i.e., application controls.

The UC contains the control algorithm for the converter level of operations, and in doing so, may collaborate with other controllers at this level. Therefore, in a UC it will be possible to design two kinds of control algorithms. In a first level are the algorithms destined to control the converter states. Generally these algorithms offer basic functionalities such as output current control or dc-bus voltage control. These algorithms are based on the sensing or estimation of states variables and their outputs are the PWM duty-cycles for every PEBB. The references for these basic controllers are supplied from higher level controllers or simply put application controllers. Application controllers on the other hand receive commands from control panels or higher level entities and are the responsible for controlling system level variables such as speed, torque, power, harmonics, etc.

Fig. 11-43 shows a functional diagram of what is the UC. Logically, every different application needs a different control structure, therefore the UC model in VTB cannot be a rigid block, but on the contrary embodies a reconfigurable structure which depends on the kind of application being simulated. What remains constant from application to application are the necessary set of specialized low and high level control blocks. These have to be connected by the user in order to implement the complete controls of the power converter in order to meet the desired operational specifications.

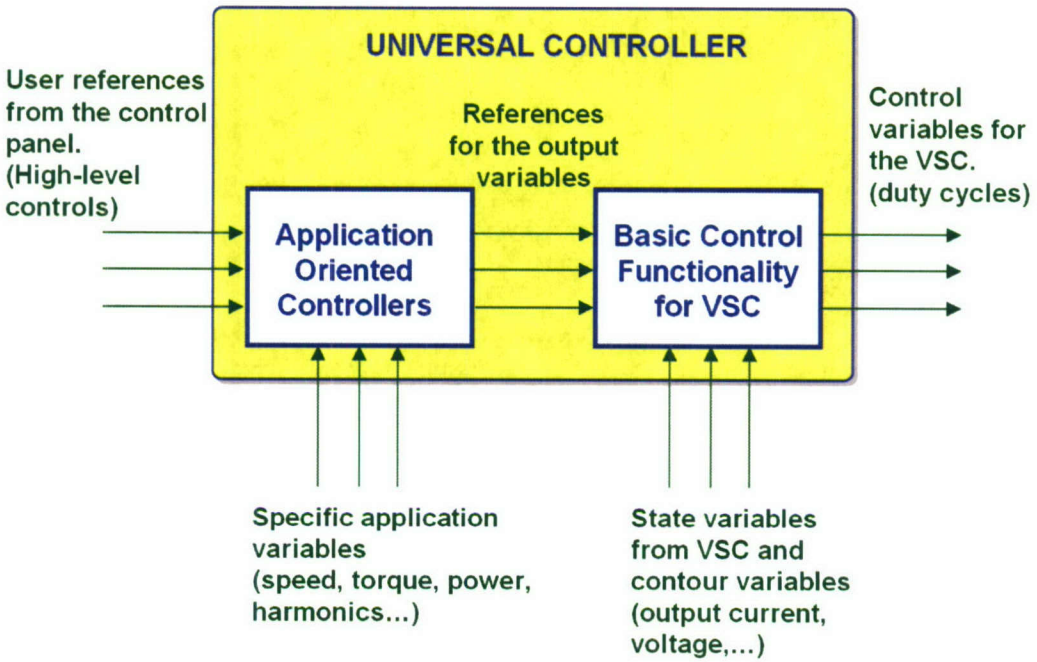


Fig. 11-43 **Functional diagram of the UC.**

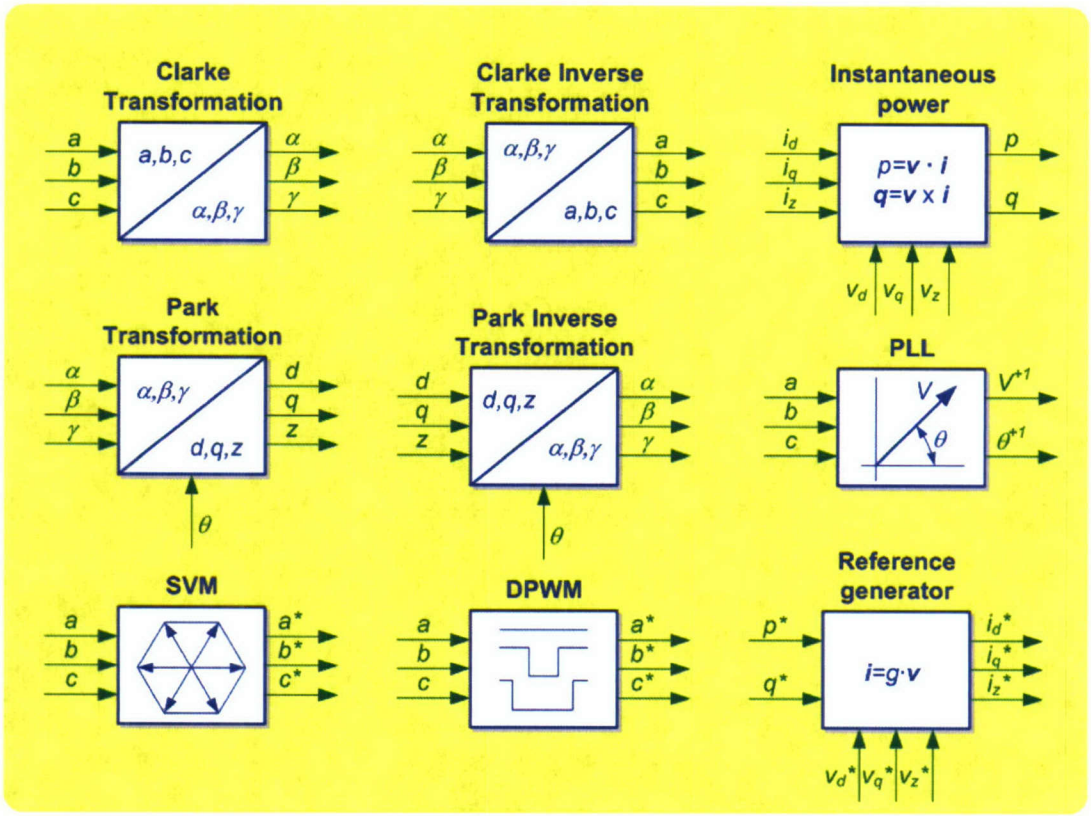


Fig. 11-44 **Set of control blocks used into the UC.**

Fig. 11-44 shows the schematics of a set of common controls blocks constituting a final control application in the UC. Several of these blocks are available in the standard version of VTB, however new ones have been specifically designed for this study, as is for instance the Phase-Lock Loop (PLL) block.

In order to show the structure of a final application in VTB, the circuit in Fig. 11-45 was designed. In this case, this circuit corresponds to a unity power factor three-phase boost rectifier. For the implementation of this circuit, the hierarchical blocks earlier presented were used. The UC is connected to the VSC by means of multiplexed buses simulating the actual fiber optic PESNet communicatios. The UC has additional inputs from the sensing of the utility voltages and currents. In this simulation, the references are supplied as constant blocks to the UC, although they could come from higher level systems or from other UC blocks.

Fig. 11-46 shows the blocks used inside the UC for the control of the three-phase boost rectifier under consideration. This is a conventional control structure working on the *d-q* synchronous reference frame. An important block in this controller is the PLL which gives information about the phase angle of the utility voltage vector.

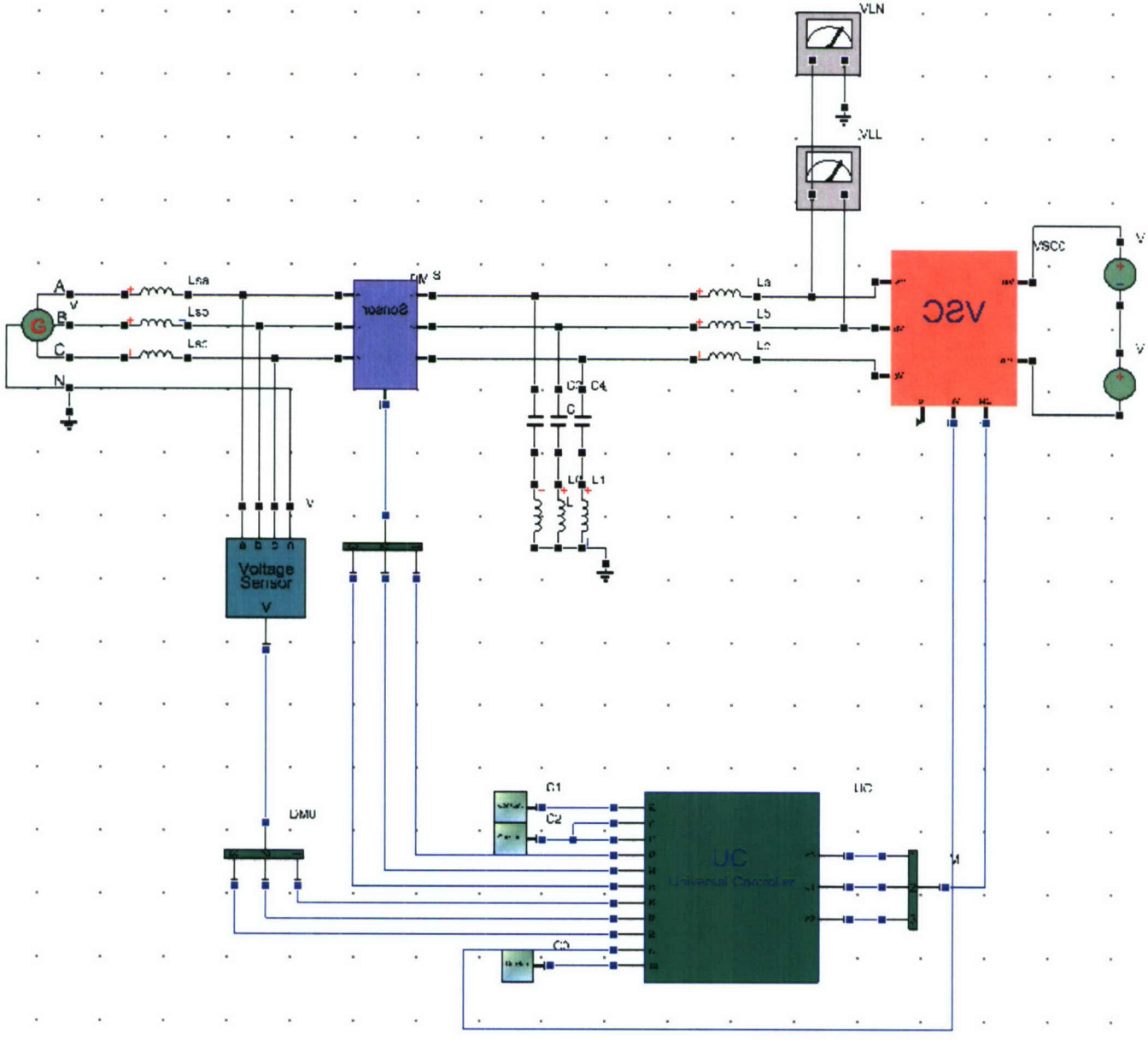


Fig. 11-45 Unity power factor three-phase boost rectifier in VTB.

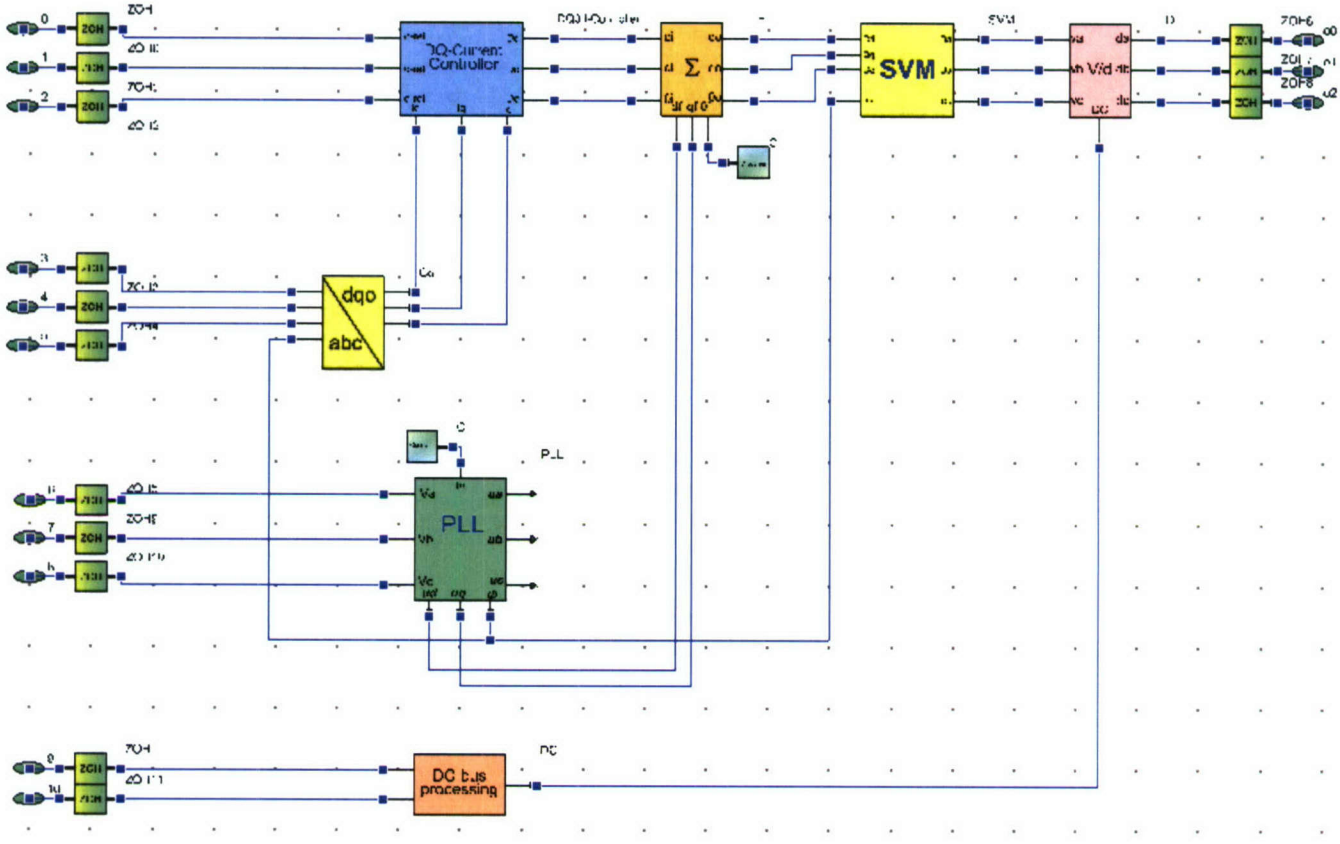


Fig. 11-46 Inner structure of the UC for the three-phase boost rectifier control.

In the control of Fig. 11-46, using the detected utility phase-angle, the currents sensed are translated to the *d-q-0* reference frame. The block labeled as DQ-Current Controller implements three linear controllers which regulate the currents in the *d-q-0* reference frame. The block labeled with the symbol of "Σ" implements a feed-forward loop introducing the utility voltage. This feed-forward loop decouples the injected currents from the utility voltage. The block labeled as SVM generates the references for the carrier-based space vector modulation in the *a-b-c* natural reference frame. Finally, the block labeled as V/d makes the translation from voltages to duty-cycles as a function of the dc-bus voltage. In the UC of Fig. 11-46, it is worth to say that the delay related to the sample time of the input variables and the delay related to processing time has been taken into account by means of zero sample hold (ZOH) bocks connected in the input and output ports of the UC.

Fig. 11-47 shows some results form the simulation of the circuit shown in Fig. 11-45. The signals shown in this figure are respectively the utility currents (up-stream of the L-C filter), the output line-to-line converter voltage, the line-to-neutral converter voltage and the line-to-neutral utility voltage.

As a final test, the VSC of Fig. 11-45 was substituted by another one using average model based PEBB. The structure and parameters of the UC stayed unchanged. In Fig. 11-48 it is possible to appreciate as the line currents using the switching and the average model are practically identical.

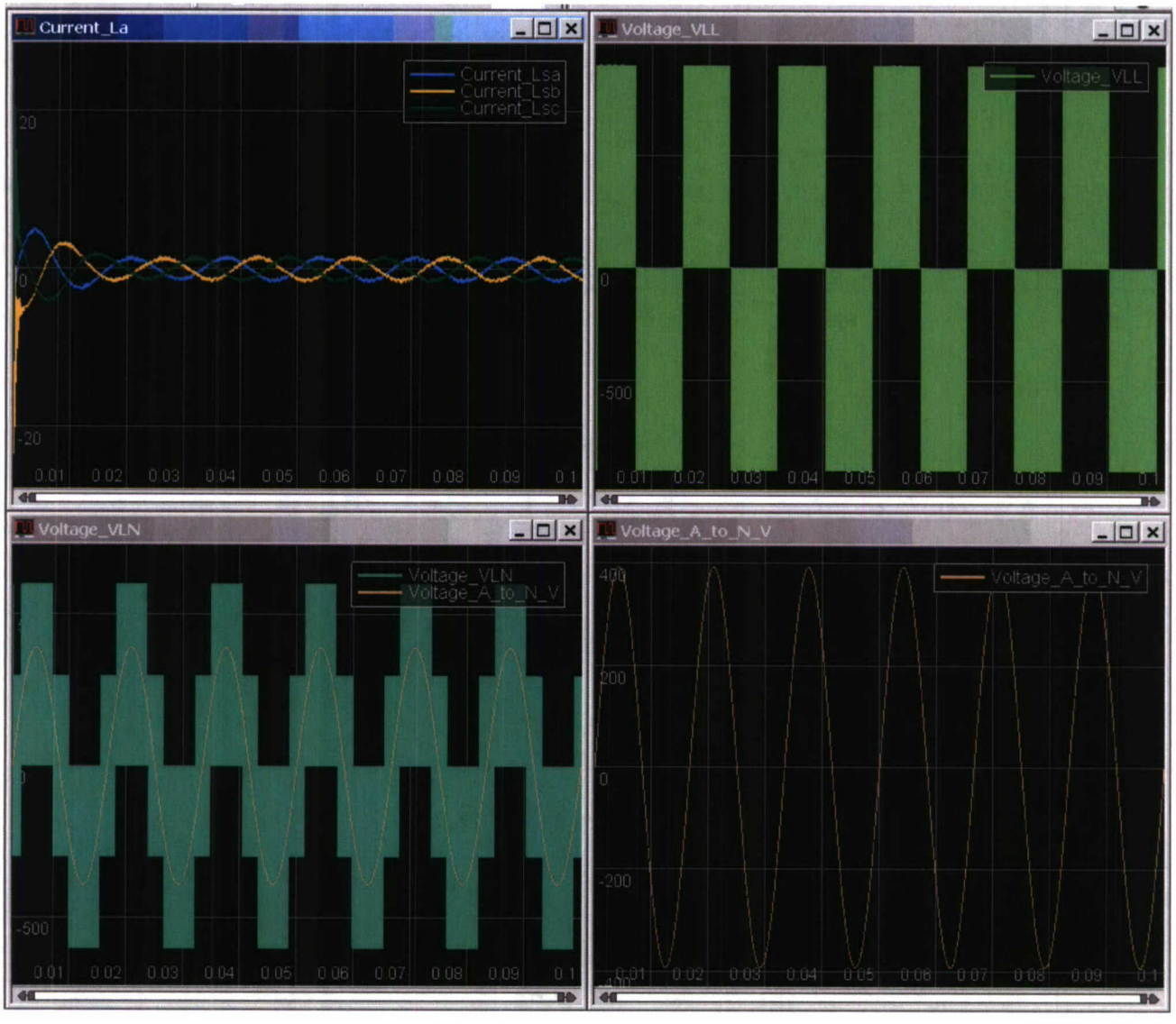


Fig. 11-47 **Simulation results of unity power factor three-phase boost rectifier.**

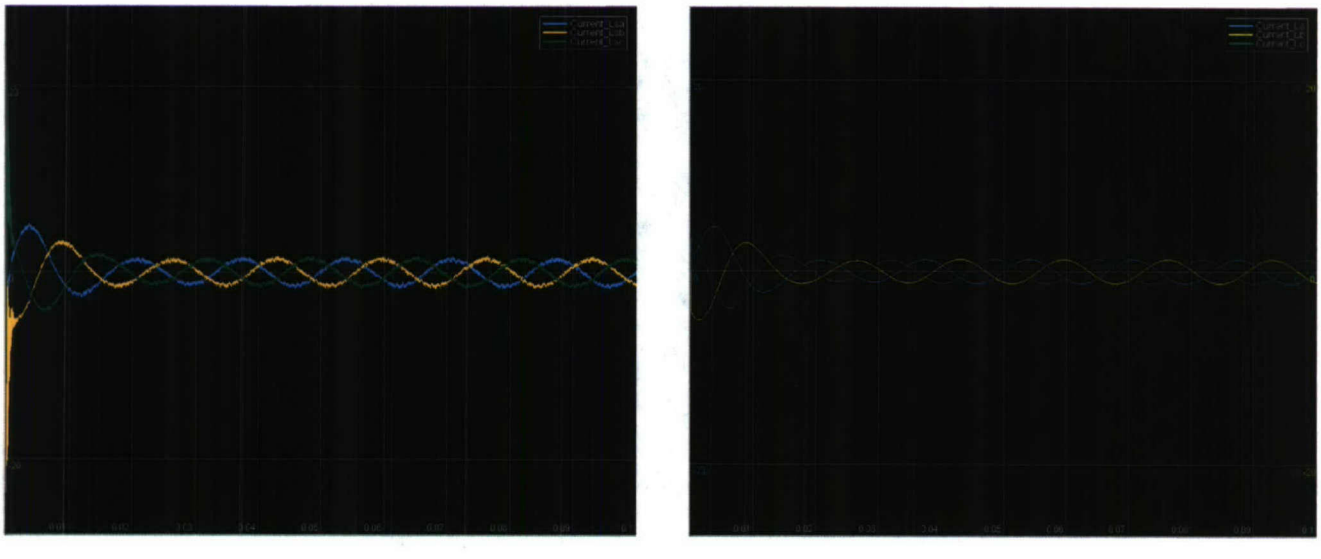


Fig. 11-48 **Simulation results using switching (left) and average (right) model.**

VIII. Conclusion

This Chapter has presented the hierarchical modeling approach undertaken to capture the electromagnetic behavior of PEBB-based power converters. Following the Standard-Cell Open Architecture concept, this Chapter has shown the feasibility of applying the same concepts inherent to the PEBB, that is modularity, flexibility, scalability, and reconfiguration, to the modeling process of power converters. The advantages obtained are significant, simplifying the electromagnetic design, control design, and system evaluation by employing physics-based, switching behavioral and average level models for each of these tasks. In this way, the model is the spec concept becomes closer to being a full design and manufacturing methodology. This has been possible to a great extent due to the final implementation of models in VTB, which thanks to its intrinsic hierarchical structure perfectly adheres to the Standard-Cell model concept presented in this Chapter. Additionally, and in an effort to support ESRDC's effort on the development and evaluation of new shipboard power electronics distribution systems, a UC model was developed and evaluated with the PEBB models developed as part of this project. This has represented a significant step towards the complete design and evaluation of more electric ships, enabling the simulation of UC networks controlling the power system itself.

Chapter 12 ASSESSMENT AND VERIFICATION OF DATAFLOW SOFTWARE ARCHITECTURE

I. Introduction

In this chapter, the open control architecture implemented using the dataflow approach will be assessed regarding feasibility as well as complexity of software development. Four control applications with different complexity will be used to compare dataflow-based software with a corresponding monolithic C version. Furthermore, to verify the dataflow control architecture, the dataflow-based control software for a 3-phase VSI will be implemented on a PEBB-based hardware system.

II. Dataflow Architecture Assessment

The reason that dataflow was chosen as the implementation style for the proposed open control architecture is the reduced complexity of control software composition and maintenance, the flexibility to transplant to different hardware platforms and the ease of adapting to adapt to distributed computation environment. While the software engineering benefits of using a compositional, component-based architectural design are well known [90], the perceived overhead imposed by dataflow may become a serious obstacle to the feasibility of dataflow software in the real-time control application. The dataflow architecture for power conversion system control is assessed regarding these two folds.

II.1. Dataflow Applications

We implemented the embedded control software in several of applications using a dataflow architecture. The open-loop, three-phase inverter is the simplest application, while the four-leg inverter is a fairly complicated application.

A. Open-Loop Three-Phase Inverter

The dataflow graph (DFG) for the open-loop, three-phase inverter application is shown in Fig. 12-1. This is the simplest application used in our experiments. The control algorithm is sinusoidal PWM (SPWM). It consists of three *Lookup_Sin* ECOs that receive a *Start* signal from their Boolean input data channels. They look up a value from a circular table that they maintain using a table pointer. After every look-up, the table pointer is incrementally increased. The table source and the modification step for the table pointer are stored as part of the ECO's configuration information. The output values of the three ECOs have a phase difference of 120 degrees. In combination, these form input for the *Modulator* and activate it to produce three floating-point results that form inputs to the three *PEBB_drivers*. The *PEBB_drivers* convert the data from the floating-point format to a format of control information that can be understood by the power stage. In the following two applications, the inputs are relatively more sophisticated than those of the open-loop application.

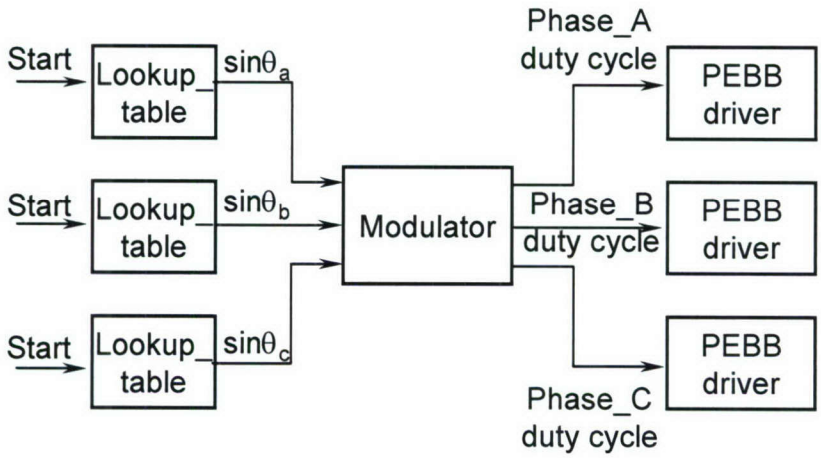


Fig. 12-1. Open-loop, three-phase inverter.

B. Boost Rectifier

Fig. 12-2 shows a dataflow graph for a three-phase boost rectifier with closed-loop control. There are two control loops: the current loop and the voltage loop. The voltage loop should be executed first in order to generate a reference for the current loop. For the three-phase current loop control, the dq transformation technique is used.

All sensed data are implemented using interrupt-driven data channels, and are synchronized by the switching clock. The rising edge of the switching clock causes the execution of the corresponding interrupt handler, in which all the sensed data, phase currents and voltages, and DC voltage are updated. The ADC drivers then translate those sensed data to their correct values.. At this point, the ECO *1-D regulator* and *synchronize* commands ready. The DC voltage is regulated in the ECO *1-D regulator*, and the current loop reference d_{d_ref} is generated. The *synchronize* ECO tests the phase voltages and generates a Boolean output to indicate whether or not the phase angles need to be synchronized.

The two *lookup_table* ECOs have two different behaviors depending on different inputs' combinations. At the normal condition, if the phase voltages do not need synchronizing, the *lookup_table* ECOs incrementally increase their table pointers and output the table value; otherwise, the table pointers will be reset. Through the ECO *duplicator*, the sin and cos values are copied and directed to two different ECOs. So far, the *abc_dqo* ECO is ready to transform the phase currents in abc coordinates to dqo coordinates. Then the *2-D regulator* performs the current loop regulation using the reference generated from the voltage loop. The regulated currents in dqo coordinates will then be transformed back into $\alpha\beta\gamma$ coordinates through ECO *dqo-αβγ*. Then, the ECO *3-D Modulator* is ready to synthesize duty cycle information for each phase. In the *PEBB_driver* ECO, the duty cycle information will be translated to the form that can be used to generate a switch pulse at the phase leg.

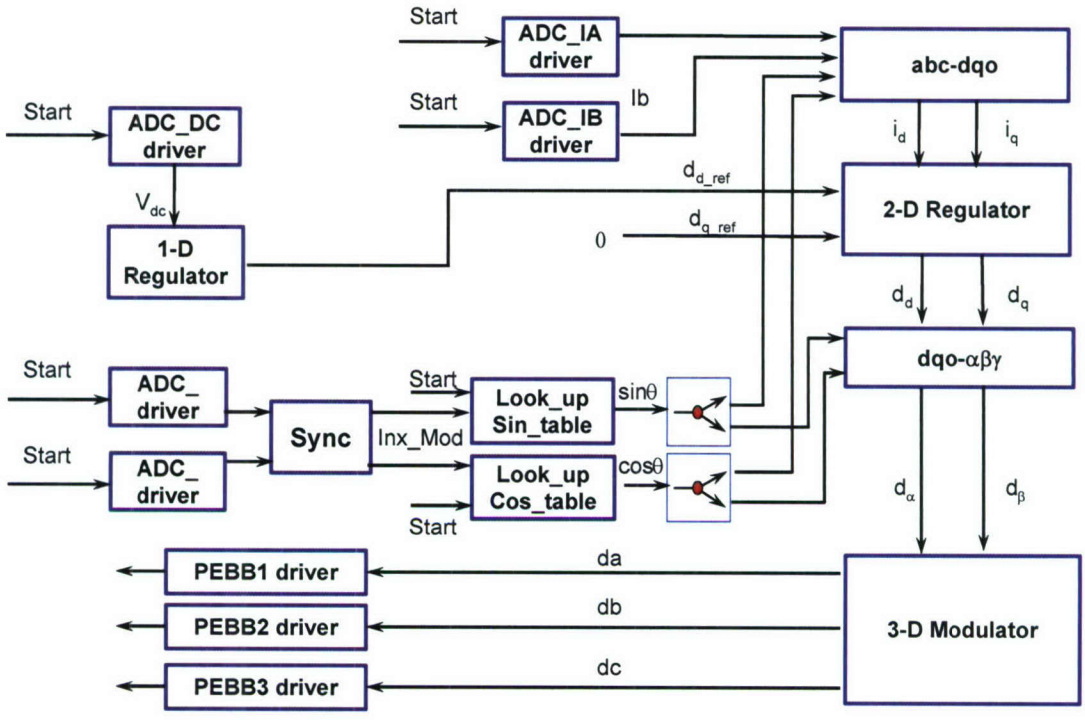


Fig. 12-2. Closed loop control for three-phase boost rectifier.

C. Closed-Loop Three-Phase Inverter

Fig. 12-3 shows an ECO-based application for closed current loop control of a PEBB-based three-phase inverter. The dq transformation technique is used to simplify the control. At the beginning of a switching period, the driver ECOs for A/D converters are fired to read feedback information (phase currents) from sensors; the two *Lookup_table* ECOs are fired to output sin and cos data. Since the same sin and cos data are used more than once in the dataflow graph, a *1-to-2 Duplicator* ECO? is used to send the same data to two places. "In the *abc-dqo* ECO, the phase currents in abc coordinates are transformed into dqo coordinates. The *2-D Regulator* ECO performs PI regulation in dqo coordinates. The *dqo_αβγ* ECO transforms the duty cycles back into αβγ. Then the *3-D Modulator* performs modulation on the duty cycles. The *3-D Modulator* generates the duty cycle information for the whole power stage. Depending on the physical distribution of the power stage, the *PWM Dispatcher* synthesizes the duty cycle information for each separate hardware asset, in this case, phase-leg PEBBs. Each PEBB driver will then translate the floating-point format duty cycle into the proper format for the driving circuit on the PEBB.

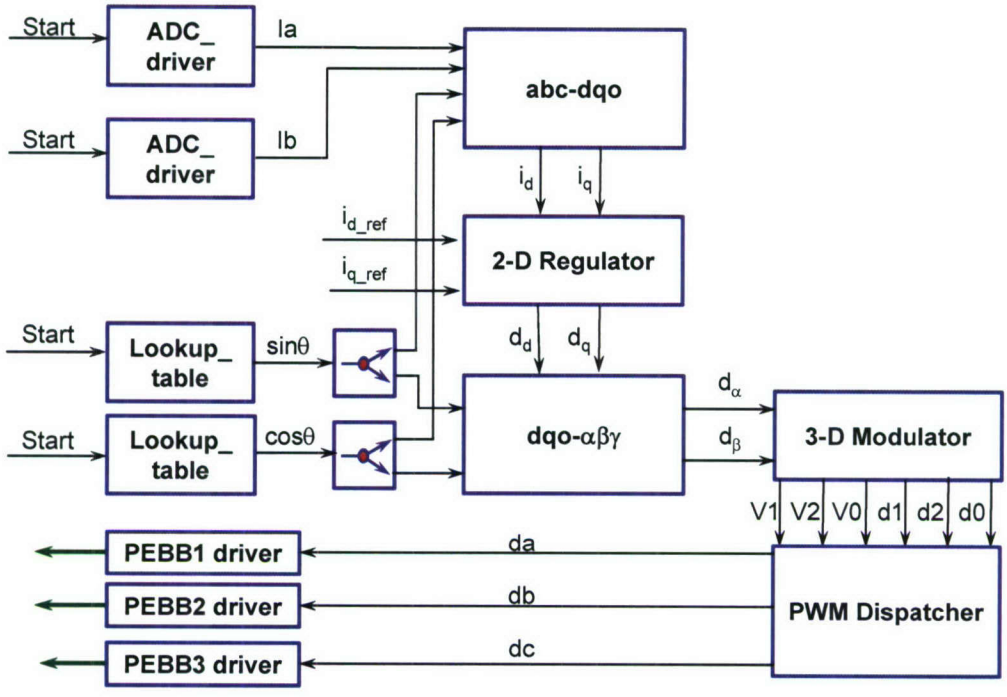


Fig. 12-3. Closed-loop three-phase inverter.

D. Closed-Loop Four-Leg Inverter

Fig. 12-4 shows an ECO-based application for closed voltage loop control algorithm of a PEBB-based, four-leg inverter. The dq transformation and SVM techniques are still used, but different ECOs will be used because the dq transformation and SVM in the four-leg inverter have one more dimension than those in the three-phase inverter control application. Since in this application, the four phase voltages are the feedback information, different *ADC driver* ECOs are used for the A/D converters on the four PEBBs. The *Lookup_table* ECO is reused. If the PEBBs are the same as in the previous application, the *PEBB driver* ECOs can also be reused. One more *PEBB driver* ECO is needed for the fourth leg.

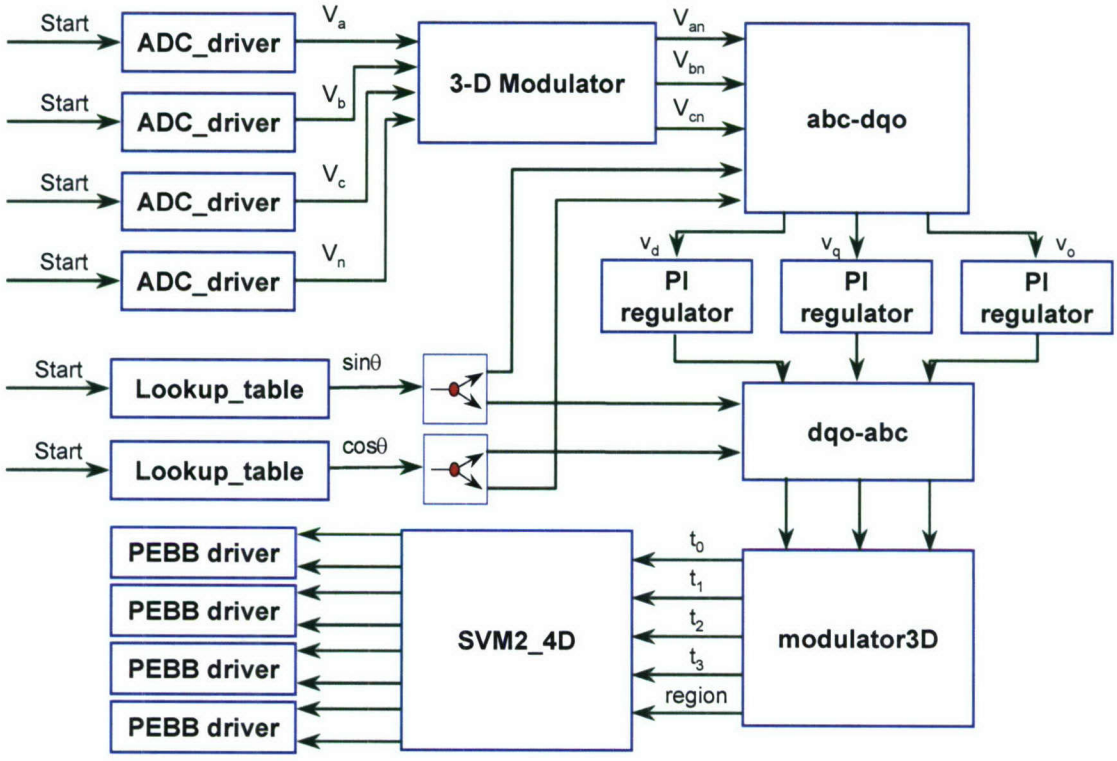


Fig. 12-4. Dataflow graph of voltage close loop control for 4-leg inverter.

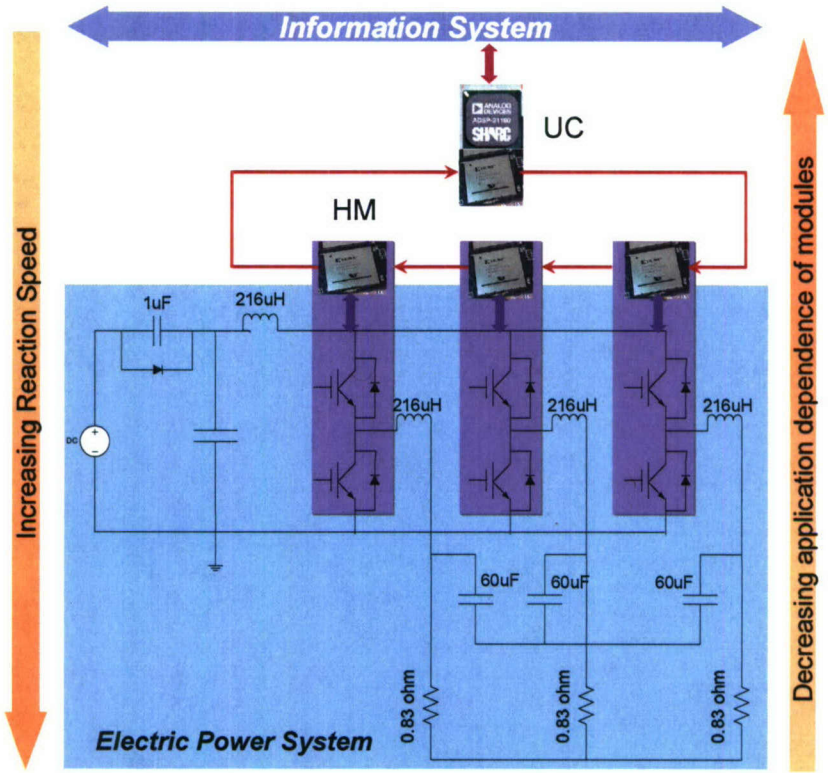
II.2. Feasibility

Given these concerns, the question then arises: is it feasible to use dataflow for power electronics control applications, or are these costs too prohibitive?

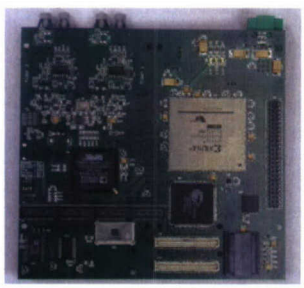
In order to explore the feasibility of applying the dataflow approach to real-time power electronics control tasks, a preliminary study of the performance issues was undertaken. A typical control application – closed-loop current control for a 3-phase PEBB-based inverter as shown in Fig. 12-5 – is implemented under dataflow architecture with different DARK options. To assess the feasibility of the dataflow approach, the code performances of dataflow software will be compared to those from the legacy custom-designed C code and from the Real-time Workshop Embedded Coder [106]. All implementations were written in C.

The specifications of the three-phase VSI are:
Input: Vdc = 200 V;
Outputs: balanced three-phase sinusoidal with line-to-line voltage of 200 V;
Switching frequency: fs = 10 KHz;
For each phase:
Switches: 1200 V, 300 A HB IPM
Output inductance L = 216 uH at each phase;
Output capacitance C = 60 uF at each phase.
Load resistance R = 0.83 ohm.

The current loop is designed to have a phase margin of 35 degrees and 10dB gain margin. The dataflow graph of the embedded control for the three-phase inverter is shown in Fig. 12-3.

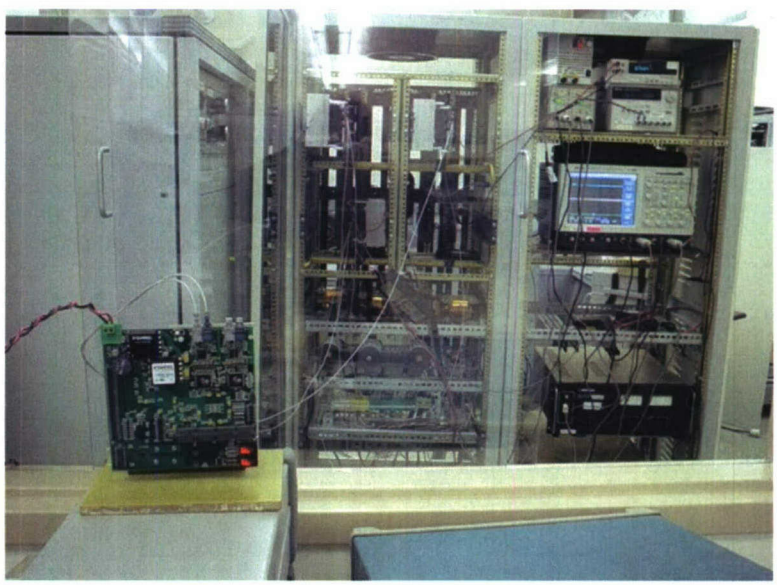


(a) Block diagram of the system.



(b) Universal Controller.

(c) PEBB module.



(d) Test setup.

Fig. 12-5. A PEBB-based power converter.

The code performance is measured by the actual execution time of one round of the complete control loop for different versions of dataflow architecture running on the same Analog Device 80MHz SHARC DSP (ADSP) 21160. For multi-thread scheduling, normally people refer this kind of response time as sojourn time. With the help of profiling tool in software development environment provided by Analog Device, it is possible to count the number of DSP instruction cycles used for the execution of specified

trunk of software. One instruction cycle of ADSP is 1/80 MHz, i.e. 12.5 ns. 21160 Thus, the actual execution time of one round of the control loop can be estimated fairly accurately as (number of instruction cycles * 12.5 ns).

Fig. 12-6 shows the performance comparison between the three versions of the three-phase closed-loop control inverter application. For the dataflow architecture, the performances of the same dataflow graph with various DARK options is shown. The measurement of execution time is also categorized by different operations. From Fig. 12-6, the additional overhead imposed by the use of concurrent processes is evident. The instruction cycles devoted to "data channel operations" were those executed by the data channel read and write system calls made by ECOs in the dataflow design. The "ECO scheduling" instruction cycles were those devoted to determining which ECO was to be executed next. The "context switching" instruction cycles were those devoted to saving or restoring register contents when switching from the currently active process to the RTOS, or when switching from one active process to another.

The DARK used for this comparison employed streamlined choices for how to manage ECO processes in order to provide a picture of what may be feasible. It supported ECOs by providing non-preemptive scheduling and by supporting single-unit data channels (instead of multi-item queues). More comprehensive RTOS features, including preemptive task switching, full support for dynamic process priorities, and arbitrarily sized data channels, are all possible. The "mailbox" messaging method provides faster connections between ECOs, but with less protection against data loss due to different update frequencies of source and sink ECOs. The "queue" messaging method, on the other hand, is slower at passing data but provides a buffer between ECOs with different updating frequencies. When the ECO execution sequence can be predicted, static scheduling introduces the least performance overhead for context switching and process scheduling. If there are control events occurring at different frequencies, dynamic scheduling allows for more flexibility in control. The multi-thread allows better concurrent control in the system, and pre-emptive scheduling makes the control software capable of responding to the most critical events in the order of highest priority. These features will each introduce additional run-time overhead, however.

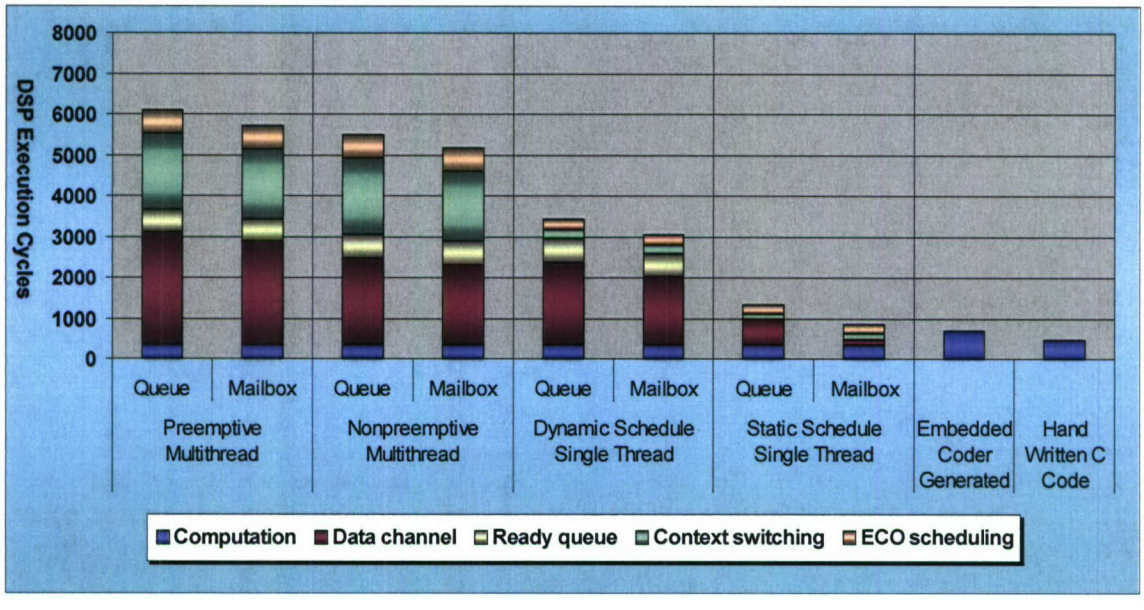


Fig. 12-6. Code performance comparison.

For the closed-loop, three-phase inverter control application, the DARK with the smallest footprint – mailbox and static single thread – is sufficient to provide full control to the power processing system. Fig. 12-6 shows that with this DARK feature, the performance of the dataflow software can be compared to

the C code generated from the Real-time Workshop Embedded C Coder, which is also adopted by many industry control software platforms, such as ABB OPCoDe.

From Fig. 12-6, it is also clear that inter-process communication, in the form of data channel actions, dominated the overhead introduced by the ECO approach. Context switching and process scheduling were also important factors in the increased time required by the ECO application. Nevertheless, the application still ran within the limits necessary for proper performance.

Also, it is important to note that this experiment does not provide an accurate picture of the relative fraction of time spent on overhead issues versus the time spent in computation. That is because the computational aspects of this control algorithm are so small as to be negligible. This provides a much better picture of the absolute amount of overhead introduced, but does little to give a true impression of how this compares to a realistic computational burden.

II.3. Engineering Effort Endeavored to Control Software Development

Under the main-program-and-subroutine style, because the software is close coupling to hardware, almost every new application needs to develop from the scratch. Under the dataflow-based open architecture, the control software development is naturally component-based and mainly is to express the control with its corresponding dataflow graph. The written code size in terms of characters is also measured to show to some extent the impact of software architecture and style on the complexity of software development.

Fig. 12-7 shows the rewritten code sizes under main-program-and-subroutine and dataflow style, respectively, for the four applications presented previously in this chapter. For the main-program-and-subroutine style control software development, the written code size is roughly the size of the control code itself; while for dataflow style software, the rewritten code size in text-based development environment will be the size of text used to describe an application specific dataflow graph. Since code size is a factor of software complexity, Fig. 12-7 also shows the larger the code size, the more reduced rewritten effort involved in the dataflow software development compared to main-program-and-subroutine style software. It is worth to mention that code size is not the only measurement of software complexity, the context is also important. For dataflow style, the text-based software development is specifying the selection of ECOs and connection of ECOs. For main-program-and-subroutine style software, the software development still includes math or logic manipulation as well as hardware interfaces.

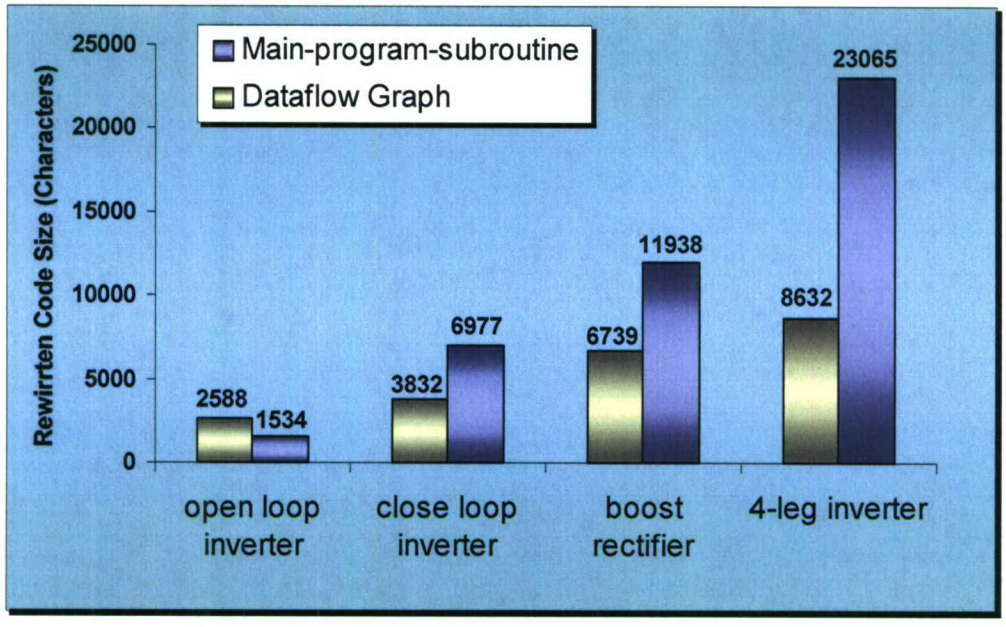


Fig. 12-7. Comparison of code size.

III. Dataflow Architecture Verified on PEBB-base Converter Hardware System

After the preliminary assessment of dataflow architecture from a software point of view, this approach is also verified on a PEBB-based 3-phase inverter system, which aims at modularization and standardization of power hardware.

III.1. PEBB-based Converter System

The PEBB-based converter system designed at CPES is shown in Fig. 12-5. The power hardware system is composed of PEBBs and passive components. The control system is composed of Universal controller (UC) and hardware managers (HM). UC conducts converter level control, HM is integrated with PEBB for local intelligence such as gate signal synthesis and local protection. UC and HMs communicate through a so-called PESNet (power electronics system network), which is actually an optic fiber ring.

The UC has been designed to address the needs of the majority of power electronics applications in medium to large power electronics converters. Large systems need communication interfaces, status indicators, debugging tools, advanced control algorithms and fault tolerance. Fig. 12-8 [107] shows a function block diagram of UC. The CPU is composed of an SHARC ADSP 21160 and Xilinx FPGA XC18V04-VQ44C. The DSP is taking most of the computation of control and the FPGA provides support to various peripherals. All the control software written in C is finally complied into machine code is downloaded and running in the DSP.

The role of HMs is actually interfaces between the control and the power stage. On one side, the HM connects into the information system via optical fibers arranged in single or dual ring structure. On the other side, the HM connects to the power stage through a phase leg, forming a basic PEBB. Fig. 12-9 [107] shows the function block diagram of an HM. The core of HM is a Xilinx FPGA, which collaborates gate drives, ADCs and communication to higher level control.

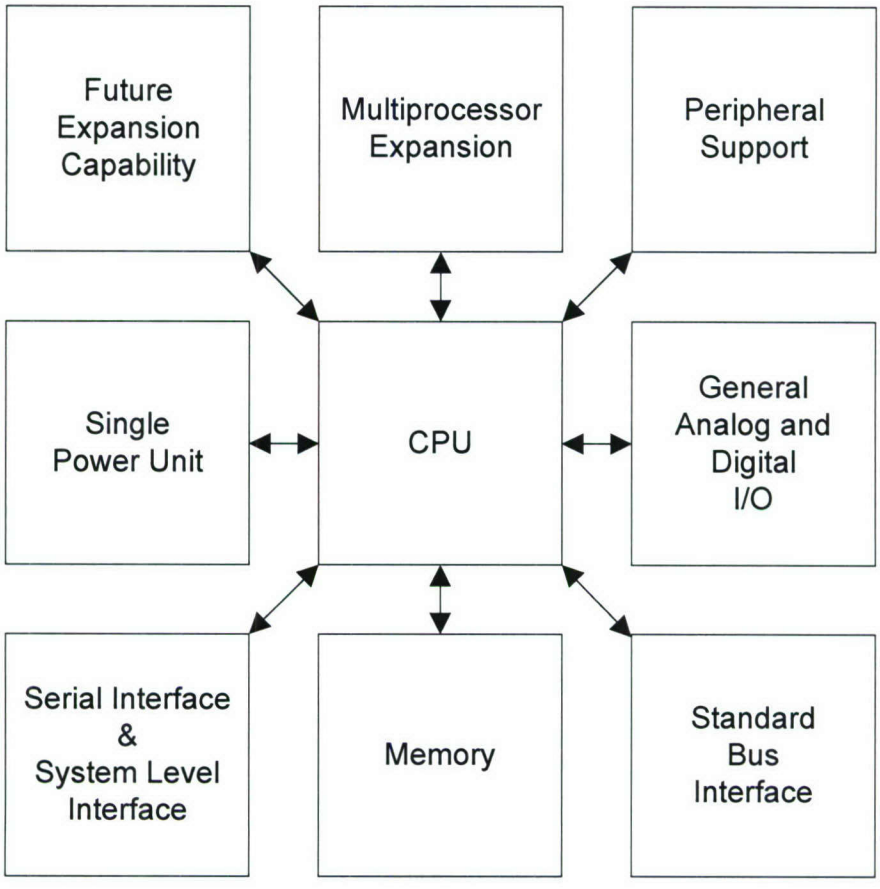


Fig. 12-8. Function block diagram of UC.

In such a PEBB-based power converter system, the massive computation related to converter control is carried by UC. The switch control commands are sent to each HM, and will be interpreted into gate signals by HM. For closed-loop control, HM will also be responsible for sending sensing data acquired at local sensors back to UC. The key of connection between UC and HMs is the so-called PESNet.

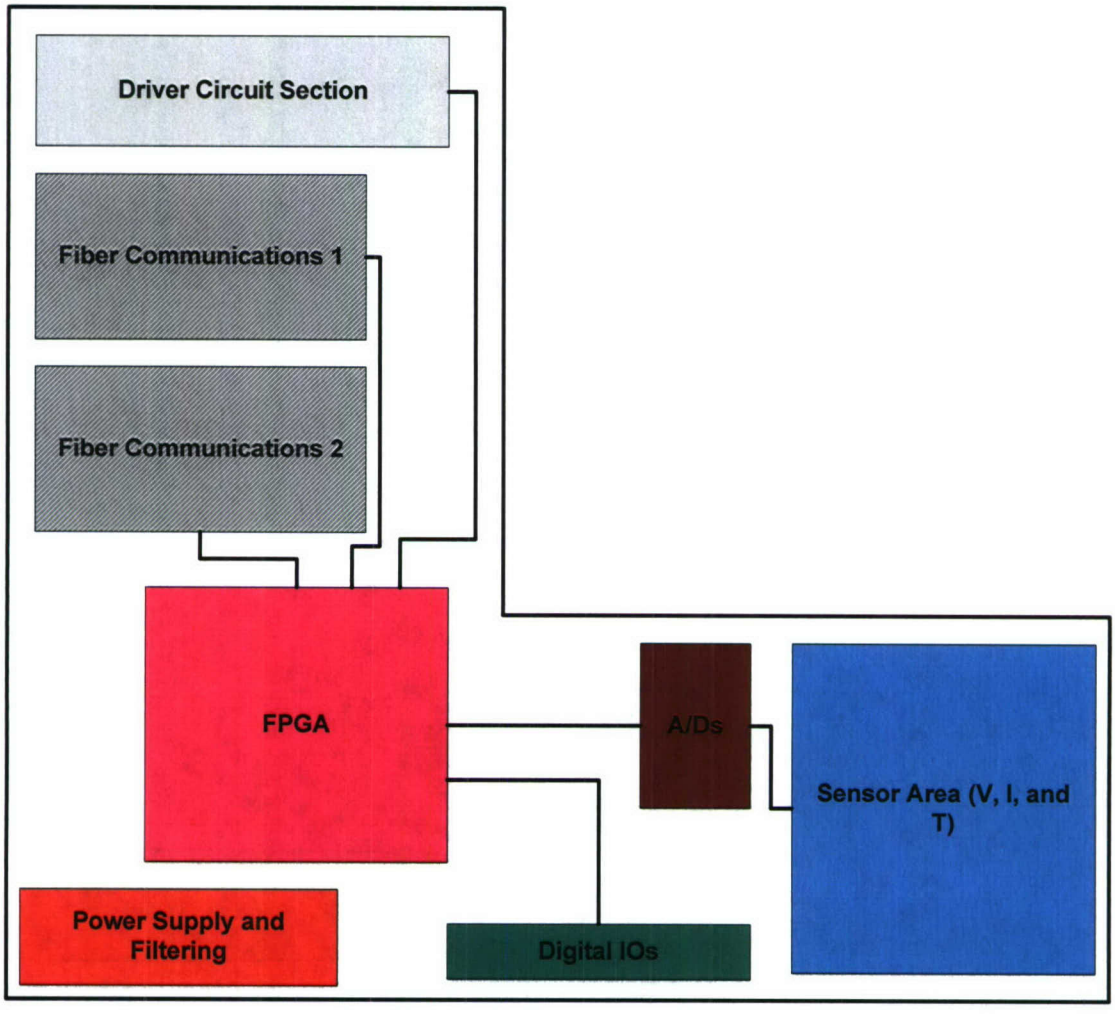


Fig. 12-9. Function block diagram of HM.

III.2. Power Electronics System Network II (PESNet II)

In PEBB systems, control architecture tends to be distributed, which requires communication networks. Some features of power electronics systems, such as hard real-time, life critical, etc., impose intense considerations in design digital communication networks, which should provide efficient information interchange and system protection mechanism. This will address several important issues in design of digital communications in power electronics systems. First, to provide fast communication and support flexible system construction, the candidate network topologies will be explored. Meanwhile, the EMI immunity is taken as an important consideration to design the network topology, since the communication is most likely carrying on in a rather noisy environment. To address these issues, a fiber optic ring structure is selected, as shown in Fig. 12-10, for the digital communication in PEBB-based system.

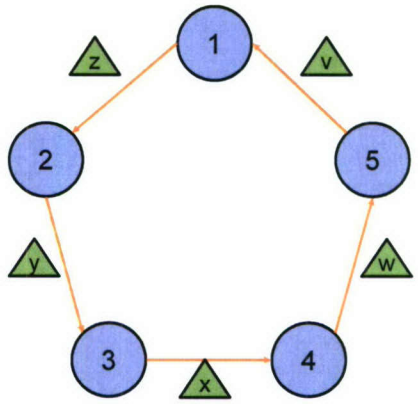


Fig. 12-10. Optical fiber ring structure.

A. PESNet II Structure

The so-called PESNet II protocol has been design for the optical fiber ring to support fast communication between UCs and HMs and closed-loop control capability. The protocol stack contains four layers: physical layer, link layer, network layer and application layer. The physical layer includes the optical fibers and TAXI chipset used as transmitter and receiver. The link layer and network layer are implemented in the FPGA of both UCs and HMs, while application layer is implemented in the DSP of UC and serves as interface for control software to connect into the information network in PEBB system.

At the network layer, the PESNet support peer-to-peer communication. In PESNet II, the network address for a node is dynamically assigned by UC. The packet format is shown in Fig. 12-12. The packet header CMD is a 4-bit field that indicates the type of a packet. Five basic types of packets are defined. Among them, NORMAL packets are specially designed for switch turn on/off control and exchange of sensing data for closed-loop control. EXTENDED packets are used for network configuration. SRCADDR is an 8-bit field specifying the sender of the packet, and DSTADDR is also 8-bit for the receiver of the packet. NETTIME is an 8-bit field used for nodes synchronization, which will be discussed in more detail later. DATA is the data payload of a packet with configurable length. CRC is an 8-bit field for fault diction and correction.

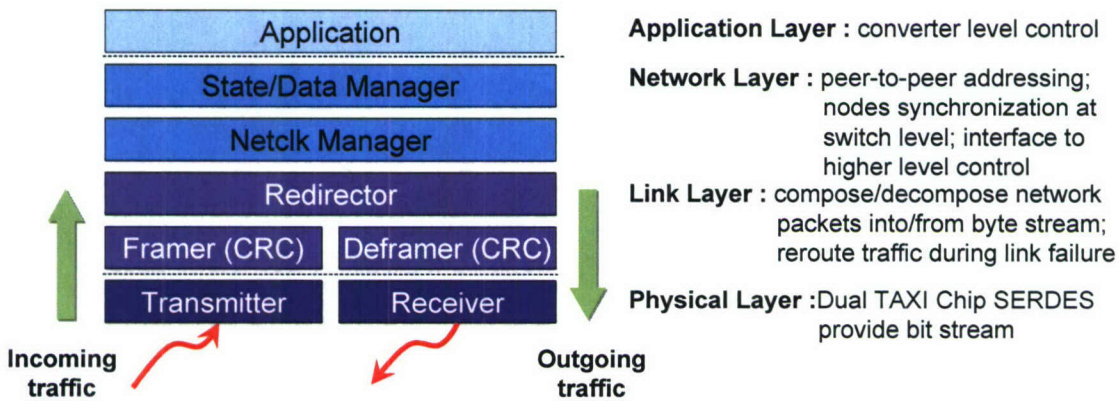


Fig. 12-11. PESNet II protocol stack.

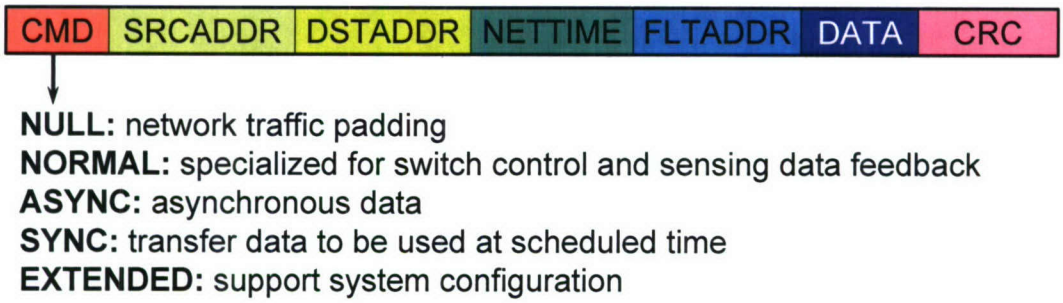


Fig. 12-12. Data packet format.

B. Nodes Synchronization Mechanism

Restrict synchronization are necessary between PEBBs in voltage-fed converter systems. However, for the ring structure, there is no natural synchronization between network nodes. A network clock mechanism is designed so that all the nodes in the network can be synchronized at us level with around 80ns jitter, which should be sufficient for switching power applications up to 50kHz. The synchronization is illustrated in Fig. 12-13.

For every node, a packet is received and sent out per 2us. Even if a node does not have data packet to send out, it will pad the network with a NULL packet. Every node keeps a so-called network clock (NETCLK) which is synchronized to the packet sending. So every 2us when a packet sent out, the NETCLK should also get incremented. Every node also maintains a packet receiving clock, which is started by the arrival of a packet at the transmitter. From the sending of a packet at one node until the sending of a packet at the next node, the time elapsed is set to be 2us. By pre-adjust the delay between packet sending clock and packet receiving clock, it is possible to adjust all the nodes to send packet at roughly the same time. The jitter is caused by a higher resolution bit stream clock of TAXI chipset, and is around 80ns.

If NETCLK is set to be increment with the packet sending, the increment action of NETCLK at different nodes can be synchronized. The problem left is how to adjust the value of NETCLK at every node, so that they have the same clock value. For this purpose, one and only one node in the network is selected as a NETCLK master, which starts it NETCLK with an arbitrary value, and then increment NETCLK every time it sends out a packet. For the rest nodes in the network, they will adjust its own NETCLK to the value in a packet sent from the NETCLK master. Thus, all the nodes can have the same NETCLK value. For operations taken by different nodes but need to be synchronized, the sender of these operations specifies the schedule net time for these operations to be fired. When a node receives such a packet for a time stamped operation, it will fire the operation when its own NETCLK reaches the schedule time. The center aligned gate signals for top switch at 3-phase PEBB converter system is shown in Fig. 12-14.

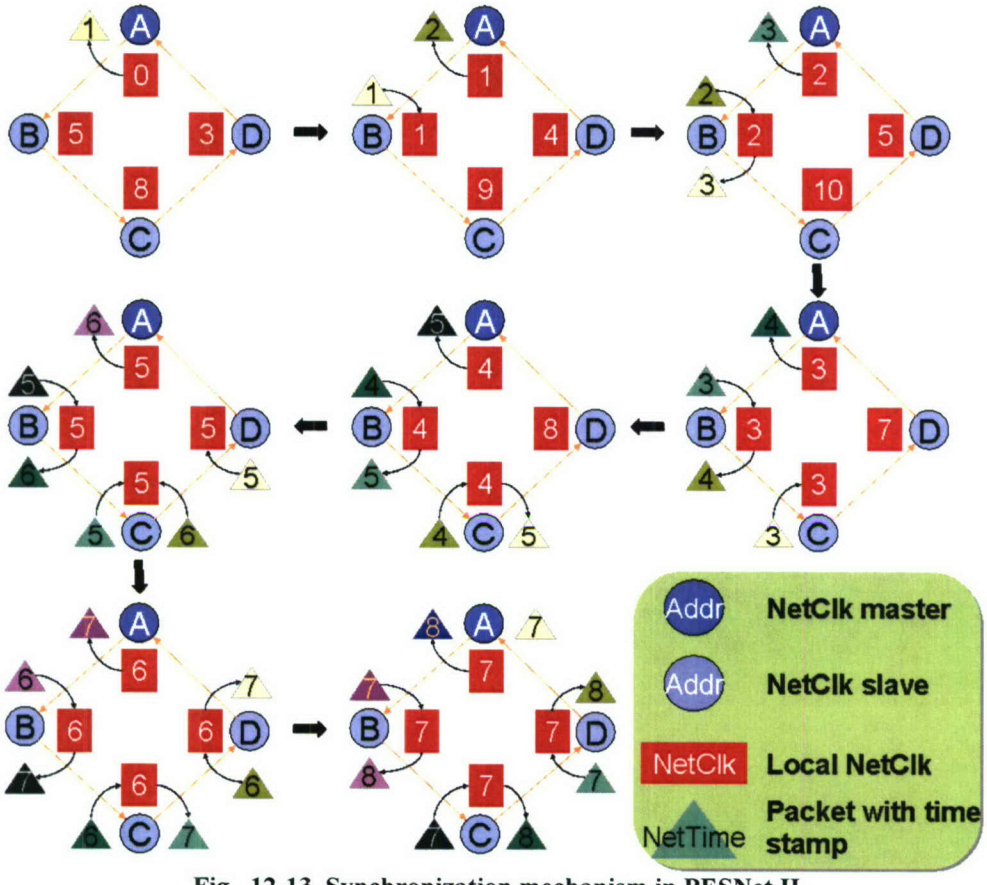


Fig. 12-13. Synchronization mechanism in PESNet II.

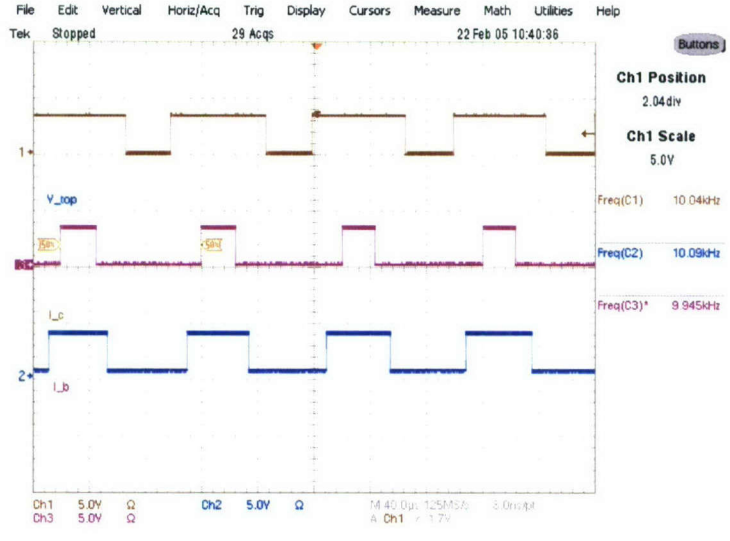


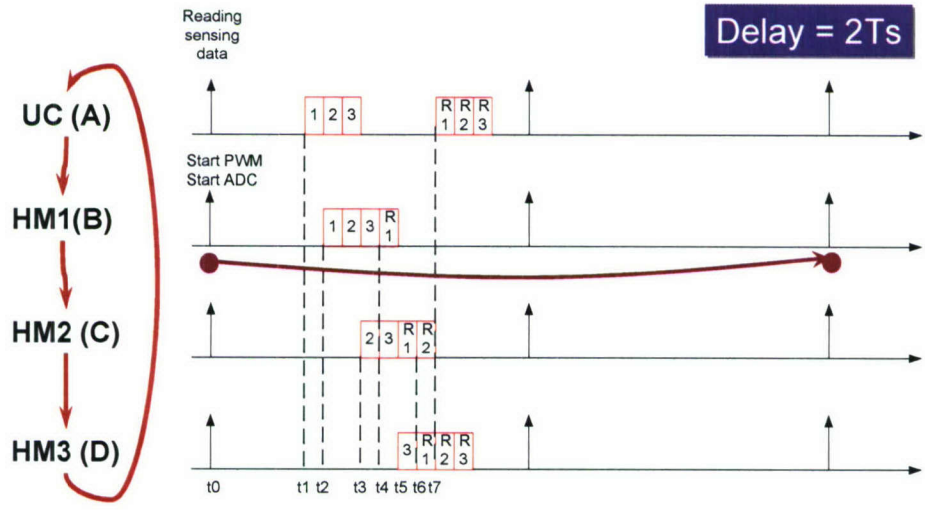
Fig. 12-14 Synchronized center aligned gate signals.

C. Latency

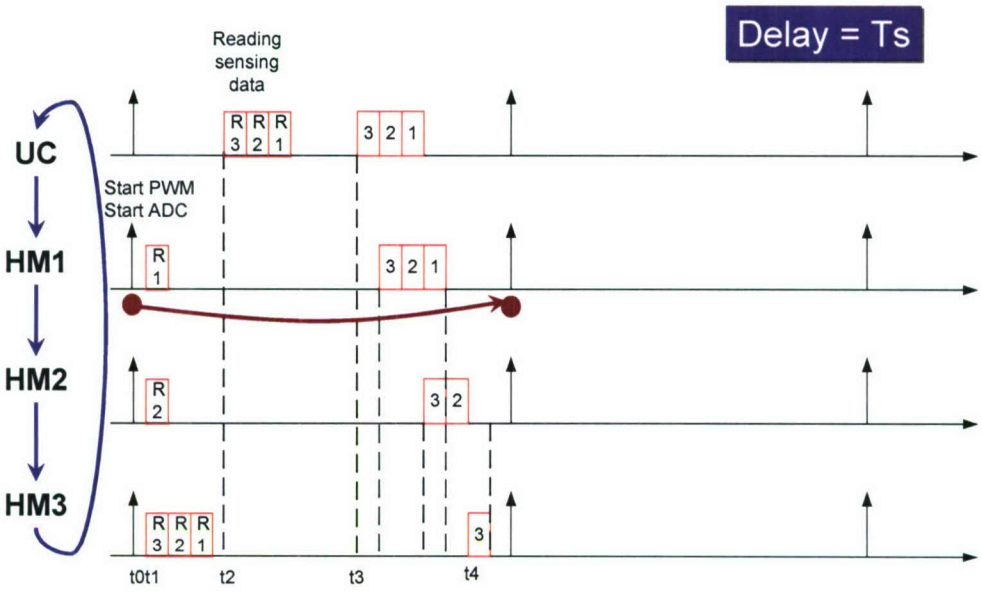
Due to the limited bandwidth of communication network and all the digital components signal processing speed, there will be digital delays associated with the PEBB system, as shown in Fig. 12-15. Digital delay could detrimental overall control performance as will be discussed later.

Different digital delays may occur due to the sequence of handshaking between UC and HMs. For an open loop control, the digital delay is defined as the real time elapsed from a switch command computes until a switch begins to act. In a closed-loop control, the digital delay will be defined as the time elapsed from a measurement (voltage, current, etc.) gets sensed until an associated switch operation get taken. The digital delay is more critical to closed-loop system since it will affect the system transient response and even stability.

Fig. 12-15 (a) shows if at the beginning of a switching period, the UC reading in all necessary sensing data for closed-loop computation, which is actually acquired at HMs in the previous switching period, and then generates switch commands and send to every HMs. These commands will decide the action of PEBBs at the beginning of next switching period. Thus, the digital delay in this case will be 2 switching periods. If data sensing, ADC conversion at HMs and UC reading sending data, computing and sending commands to HMs can be arranged in one switching period, then the digital delay can be reduced to one switching period, as shown in Fig. 12-15. In the former case, UC could have longer time for computation; while in the latter case, the control loop can have higher bandwidth and better performance.



(a) 2Ts delay



(b) Ts delay

Fig. 12-15. Different digital delay caused by communication.

III.3. Experimental Results

Two control applications were verified on the 3-phase PEBB-based converter system – open loop SPWM VSI and closed-loop VSI. The applications were simulated first in Saber, with the circuit diagram shown in Fig. 12-16.

When the switching frequency is 20 kHz, considering the stringent timing requirements, the minimal footprint DARK option–mailbox and single thread static scheduling – is chosen. Fig. 12-17 shows the testing waveforms of the open loop SPWM application.

For the current closed-loop VSI application, a proportional-integration (PI) integrator is used as the compensator. The control design is based on average small signal model in continuous time domain, and then discredited. Again for DARK, mailbox and single thread static scheduling is chosen as the real-time option. Two times switching periods is considered as the digital delay. Fig. 12-18 shows the testing waveforms with step-up and step-down transient response respectively.

With the improved PESNet protocol, one switching period delay is achievable. The transient tests were repeated for this case. However, if the switching frequency is 20 kHz, the computation time will be too stringent for the $1*T_s$ digital delay case. For a fair comparison in order to show the impact on system performance of digital delay, all the rest tests are carried with f_s = 10 kHz. The shorter the digital delay, the shorter computation time, which means DARK has to run with lower footprint. On the other hand, the shorter the digital delay, the higher system bandwidth can be achieved and hence faster transient response. Fig. 12-19 shows the test waveforms for the same VSI working at 10 kHz switching frequency. Fig. 12-20 shows the transient experimental results under $2*T_s$ digital delay. The DARK option is single thread static scheduling and mailbox styled data channel. Fig. 12-21 shows the transient experimental results under T_s digital delay. The DARK option is single thread dynamic scheduling and mailbox data channel.

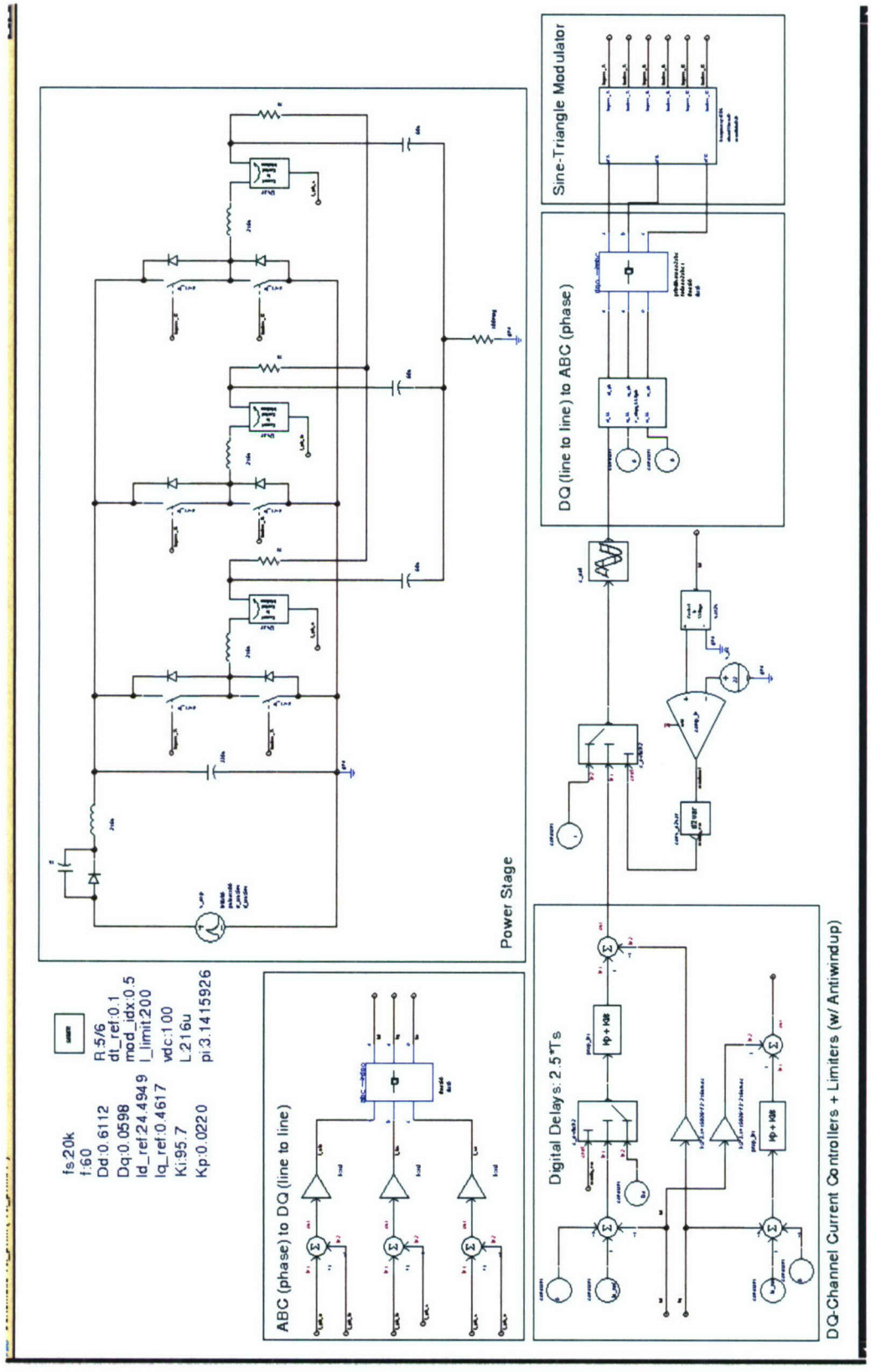


Fig. 12-16. Saber simulation.

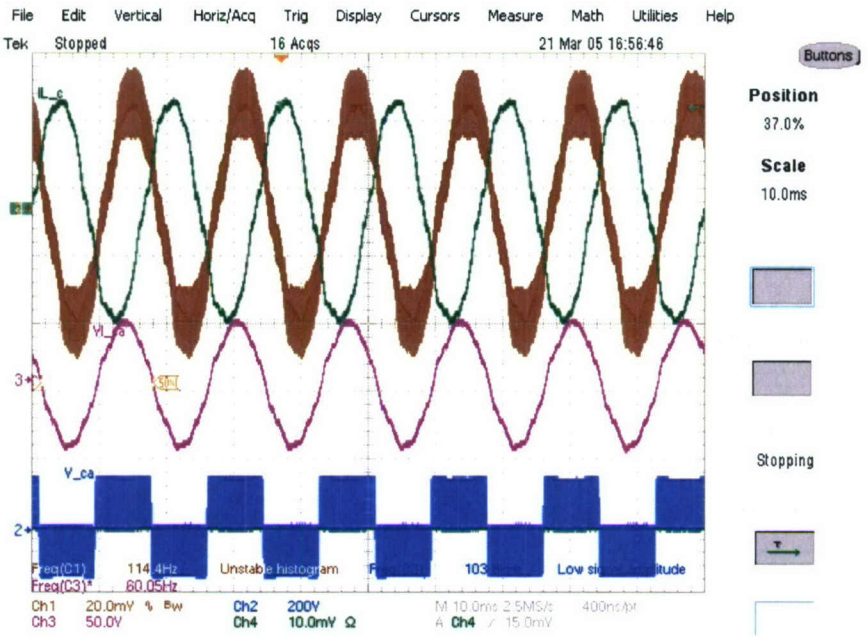
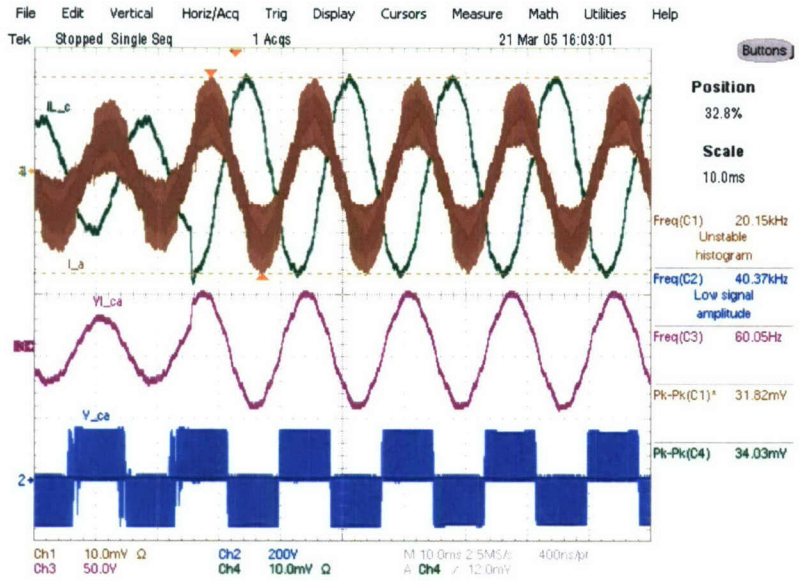
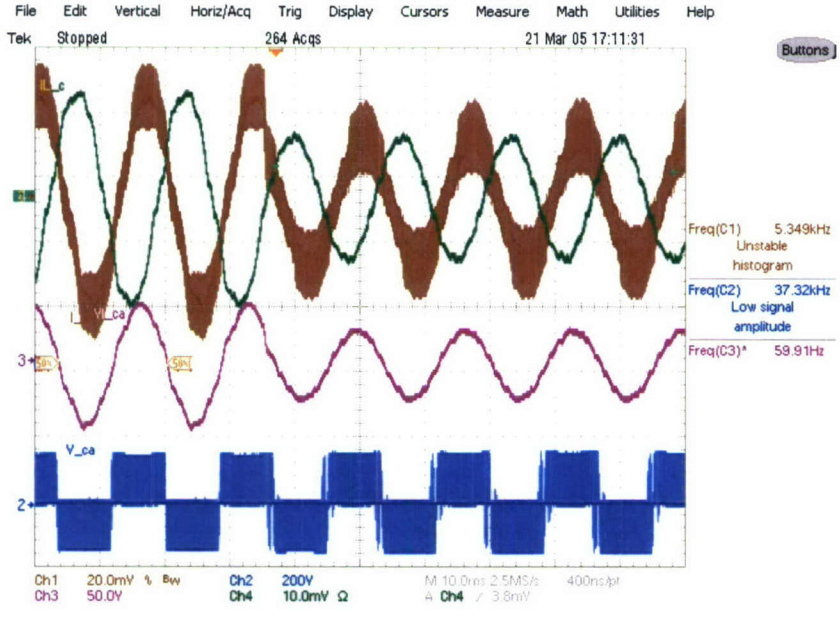


Fig. 12-17. Open loop test waveforms.

Fig. 12-17 shows inductor current, which is in brown, phase load current, which is in green, line-to-line voltage, which is in green and switch node voltage, which is in blue. Both in the voltage and current waveforms, distortions can be observed at waveform peaks and zero-crossings. Par of those distortions are due to the relatively long deadtime implementation at the HM. The IPM used does not have built-in deadtime function. And the necessary deadtime control is implemented in the FPGA of HM. The rise time and falling time if the IPM module is around 1 us, and the deadtime for each transition is designed to be 5 us for safety consideration. When the switching frequency is pushed to 20 kHz, 5 us will be 10% of the switching period, which could cause significant distortion when the duty cycle reaches it minimum or maximum values, or when the phase current is changing its direction. This kind of distortion occurs with highest frequency up to switching frequency, and will be hard to be reduced through traditional feedback control. The deadtime compensation at the HM can alleviate this issue, but will not get rid of it.



(a) Step-up



(b) Step-down

Fig. 12-18. Closed-loop test waveforms.

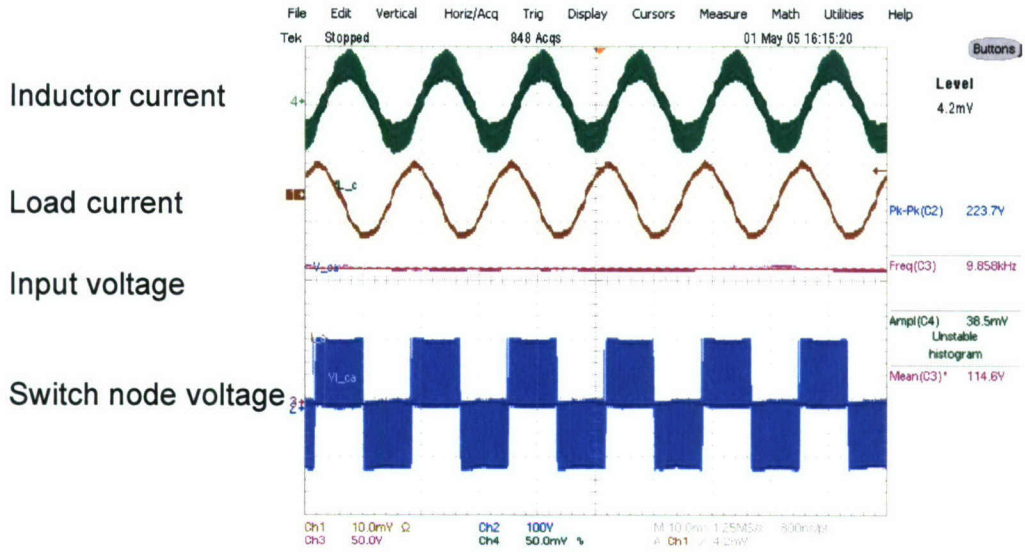
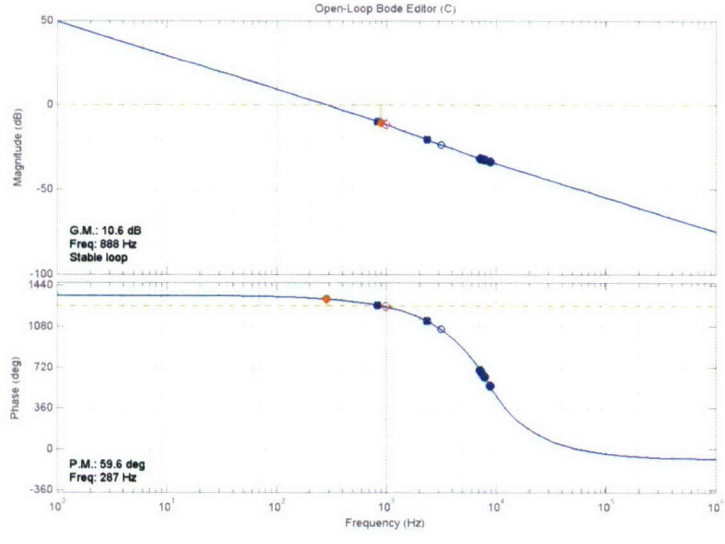
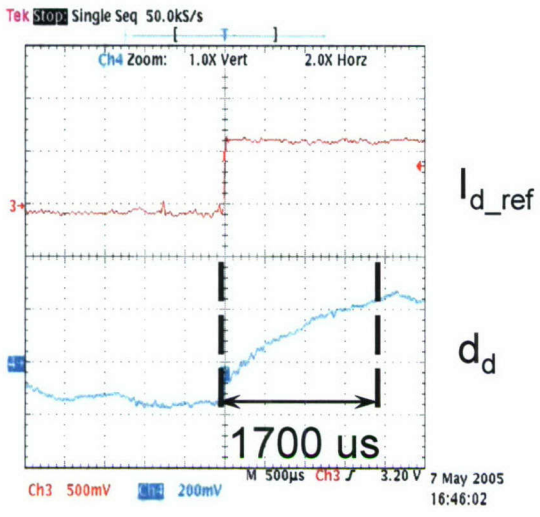


Fig. 12-19 Open loop test waveforms for f_s = 10 kHz.

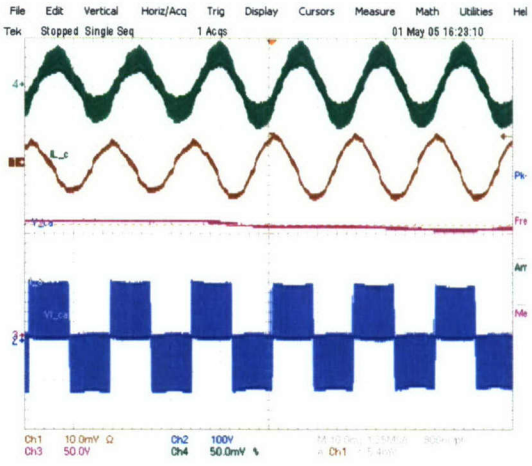
The control network latency affects system performance, especially the transient response. With longer delay, the lower the control bandwidth regarding to achieve the same gain margin (G.M.) and phase margin (P.M.), as shown in Fig. 12-20.



(a) Loop gain design for t_{delay}=2*T_s, f_c = 287 Hz.

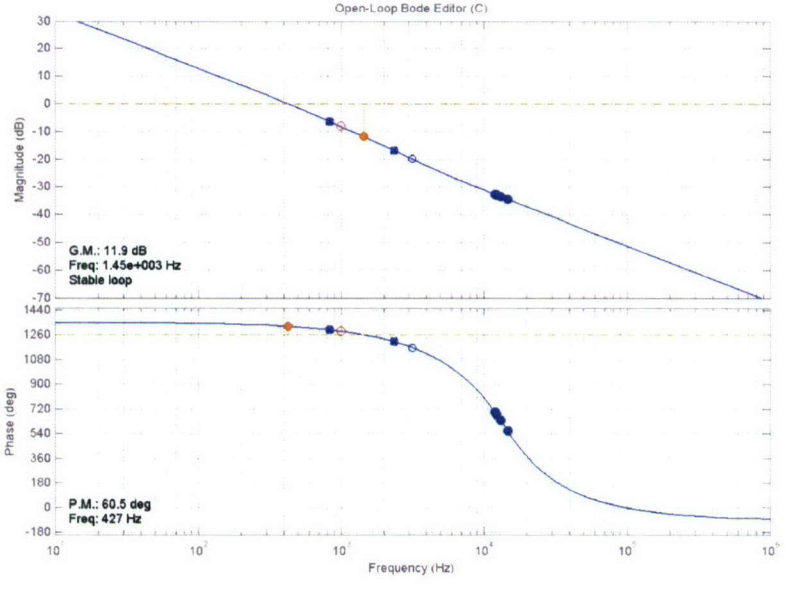


(b) Measurement of transient response.

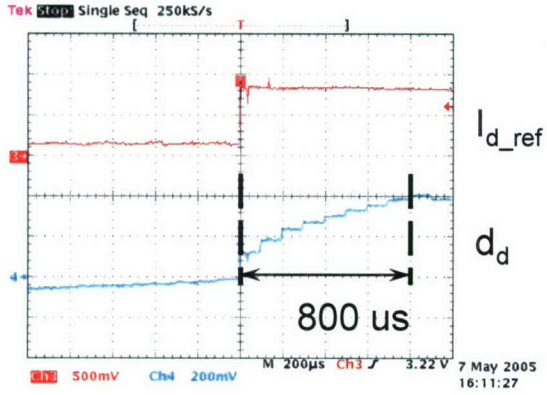


(c) Test waveforms during step up transient.

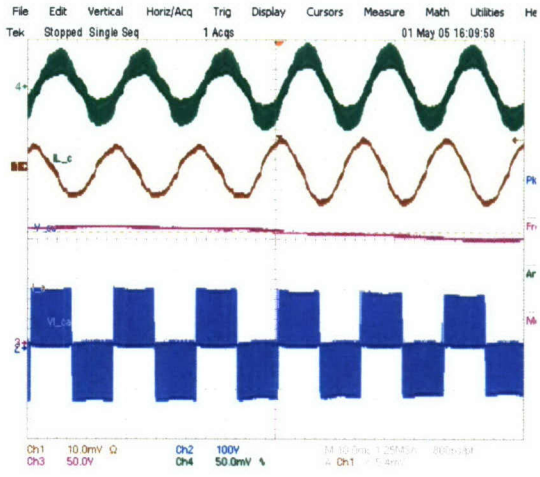
Fig. 12-20. Control design and transient response for $t_{delay} = 2*T_s$.



(a) Loop gain design for $t_{delay}=T_s$ $f_c = 427$ Hz.



(b) Measurement of transient response.



(c) Test waveforms during step up transient.

Fig. 12-21. Control design and transient response for $t_{delay} = T_s$.

IV. Future Direction and Conclusions

IV.1. Towards Reconfigurable Control Software

If a fault or exception is detected by the system hardware, the simplest way to handle it is to shut down the whole system. This is a safe practice, but in some cases is an overreaction. For example, if only one current sensor is malfunctioning but the all power switches and gate drivers can still conduct normal operations, it is possible to modify the control to continue without current loop, instead of shutting down. However, if one of the phases fails in the multi-phase converter system, or an over current or over voltage situation is detected, it is probably safer to shut down the whole power stage. From the two examples presented above, it is desirable for the control to provide certain level of adaptability to failures or changes in the power hardware.

Shutting down the system is still a common practice in case of any hardware failure. One reason from the software point of view is there no easy way to implement online reconfiguration if the control software is not well structured.

In the dataflow architecture, the ECOs are executed independently and solely connected through data channels, and a control application is defined by a dataflow graph. These properties not only reduce the engineering effort for control software development and redesign, but also open the possibility from software point of view to reconfigure the control software on the fly to adapt to changes in the outside world without introducing massive complexity to the software development.

IV.2. Reconfiguration Mechanism

The open control architecture proposed in Chapter 3 provides a feasible path for implementing reconfiguration without involving too much complexity to the control software composition. In the open control architecture, the relationship between control software and its controlled power hardware is encapsulated in the application layer. If the reconfiguration can also be performed in the application layer,

this will leave all the lower level layers and upper level layers unaffected. The basic procedure of control reconfiguration is shown in Fig. 12-22. The control tracks the status of every component in the power hardware. Once there is a status change, the control will apply certain rules to decide whether a software transition is necessary and what transition should take. The rest of the discussion assumes that the system has the structure shown in Fig. 12-24. The design of control software reconfiguration includes:

1. Representation of power hardware status in control software;
2. Track of power hardware status;
3. Rules of control software reconfiguration according to power hardware changes; and
4. Software reconfiguration implementation.

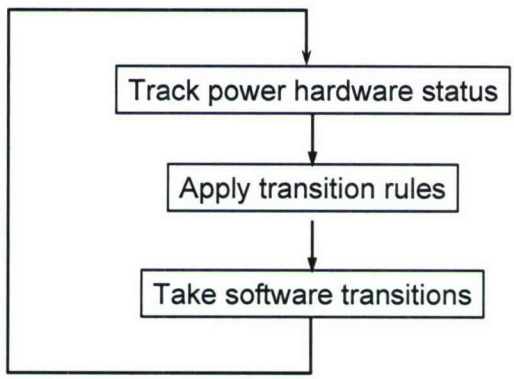


Fig. 12-22. Procedure of software configuration.

A. Track Power Hardware Status

Since the reconfiguration is based on the power hardware changes, the control software must keep the up-to-date hardware status. Fig. 12-23 shows the table in the application layer used for the tracking of power hardware status.

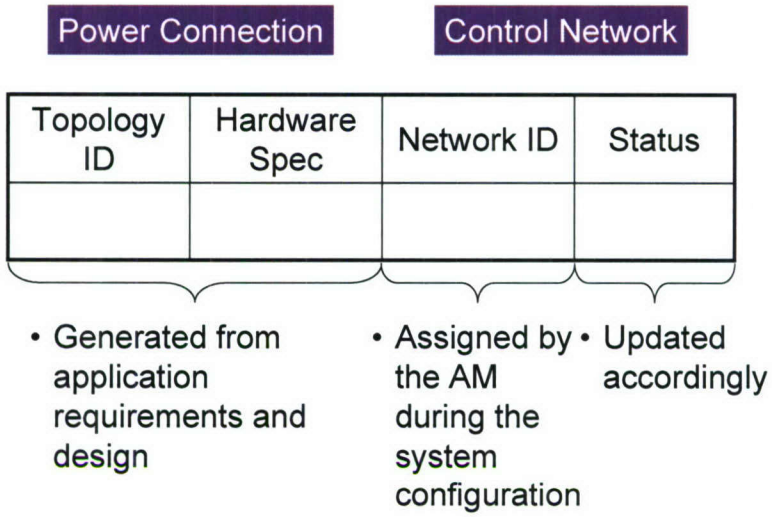


Fig. 12-23. Current hardware status table

In the hardware status table, the "*Topology ID*" indicates the position and function of a hardware component in the whole power processing system. Typical hardware components in the multi-phase converter system can be phase leg, current sensor or voltage sensor. But only the hardware type cannot uniquely express the function of a hardware component in a converter system to implement certain application. For example, even a same voltage sensor can be used to measure DC link voltage in one application, and phase voltage in another application. "*DC voltage sensor*" and "Phase A voltage sensor" are two different topology ID.

"*Hardware Spec*" is used to describe the specification of every hardware component. For a voltage sensor, the typical specification may include the sensing range, conversion rate, offset, etc. With the specification, the control should be able to decide whether a hardware component can serve the role that the "*Topology ID*" indicates.

When an application is defined, the control application designer should have the list of all the hardware components that will serve for the application. During the configuration stage after the system starts up, if the control software also has chance to enquire specifications from every hardware component, it can then decide whether a hardware component is suitable in the application.

If the system is composed from distributed hardware nodes, the control intelligences may communicate with each other and every hardware component is assigned a "Network ID". It should be noticed that several hardware components may have the same "Network ID". For example, in the PEBB-based converter system presented in previous chapter, the hardware components in one PEBB module – phase leg, voltage sensor and current sensor – will share the same network ID in PESNet.

The last column in the current hardware status table stands for the status of each component. In the simplest implement of software reconfiguration, the hardware status is defined as a Boolean type variable, which indicates that a hardware component is under either the two states – normal or failed. Suppose that every hardware component is able to report its status to the control software periodically, the control software should be able to capture changes of a hardware component: either from normal condition to failure condition or vise versa.

B. Define System States and Software Transition

When every hardware component in a system is operational, the control software may perform with the full functionality as designed. When the system loses some hardware components, the control software may reconfigure itself to a degraded operational version. When the failed hardware component gets replaced or repaired, the control software may be able to switch back to it full featured version. Thus a system state is defined as a combination of a set of hardware components with normal conditions and a corresponding operational control software version. A software transition means the control software switch from one operational version to another as the system state changes. For conventional brute-force shut down approach to handle hardware exceptions and failure, the system only has two states: the normal state and the shutdown state. The control software only has two operational versions–the full featured version and the shut down commands. This research proposes to introduce more system stats and operational control software versions according to the nature of the power hardware and application.

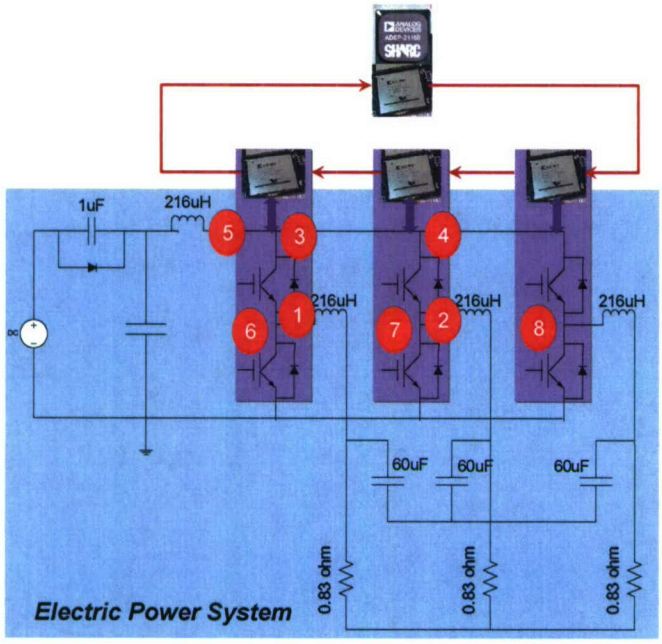
Rules must be defined that when a hardware change is captured the system should stay in the current state or should change to another state. In this research work, all the software transition rules are predefined.

With the dataflow architecture proposed in this research work, all the software reconfiguration can be implemented in the control application layer without tackling individual ECOs, control host interface and network interface. The software transition can be achieved by activating/deactivating sets of ECOs.

IV.3. Implementation of Control Software Reconfiguration under Dataflow Architecture

In this subsection, a 3-phase PEBB-based inverter system will be used as a design example to show the implementation of software reconfiguration. Fig. 12-24 shows the system structure. The position of every hardware component is also marked. With the presence of DC link voltage sensor and phase voltage and current sensors, the full featured control for this converter can be a dual loop control: a DC link voltage feed forward control loop and a current feedback control loop. The dataflow control block diagram that incorporates the two control loops is shown in Fig. 12-25. The DC link voltage is sensed, the DC link voltage error after regulation will be used as reference in the phase current feedback loop.

Table 12-1 shows a possible current hardware status after system start up, which supposes that after the system startup, every hardware component is operational. In the communications network, there are one UC and three HMs, and assigned network address 0x01, 0x02, 0x03, 0x04, respectively. The dataflow styled control software is running on UC. It also supposes that with the support of the communications protocol PESNet, the status of every hardware component is been able to report to UC periodically.



Hardware components:

1. Phase A current sensor
2. Phase B current sensor
3. Phase A voltage sensor
4. Phase B voltage sensor
5. DC bus voltage sensor
6. Phase A
7. Phase B
8. Phase C

Fig. 12-24. A PEBB-based 3-phase inverter with hardware component list and position.

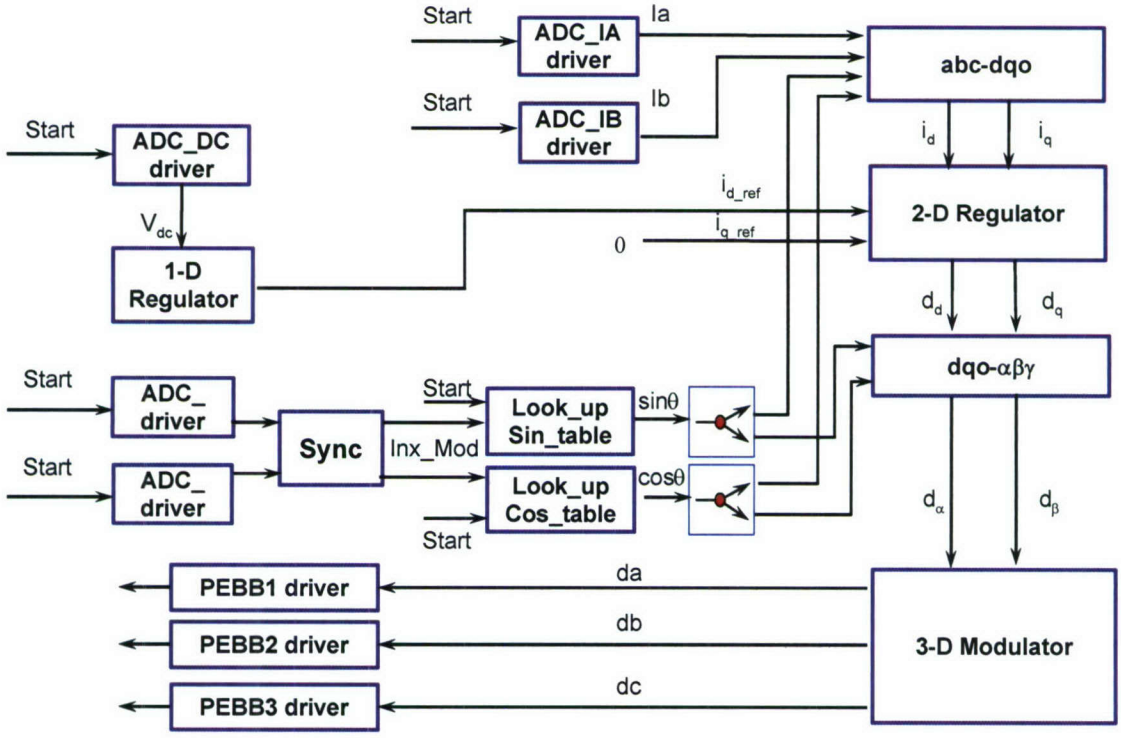


Fig. 12-25. Dataflow graph of a 3-phase inverter control with DC link voltage feed forward and phase current feedback control loops.

Table 12-1. Current Hardware Status.

Topology ID	*Spec*	*Network ID*	*Status*
0x01	Current sensor; 12-bit	0x02	Normal
0x02	Current sensor; 12-bit	0x03	Normal
0x03	Voltage sensor; 12-bit	0x02	Normal
0x04	Voltage sensor; 12-bit	0x03	Normal
0x05	Voltage sensor; 12-bit	0x04	Normal
0x06	Phase leg; half-bridge	0x02	Normal
0x07	Phase leg; half-bridge	0x03	Normal
0x08	Phase leg; half-bridge	0x04	Normal

Table 12-2. Four operational system states for the 3-phase inverter application.

System State	*Hardware Status*	*Applicable Control Algorithm*
S0	All hardware components working in normal condition	DC link voltage feed forward + phase current feedback control
S1	DC link voltage sensor fails; other hardware components are normal	Phase current feedback control
S2	Any current sensors fails; other hardware components are normal	Open-loop control
S3	Any phase leg fails; other hardware components are normal	Shut down

Table 12-2 lists the four operational system states according to the presence of hardware components. Under the dataflow architecture, every state has an applicable control algorithm and therefore has a corresponding dataflow graph. When system loses some hardware components, the system can change from one state to another; also when the failed hardware component(s) is repaired or replaced, the system stats may also change. The possible transitions between the four states S0-S4 caused by hardware status changes is shown in Fig. 12-26. Every arrow between two states is a transition. For example:

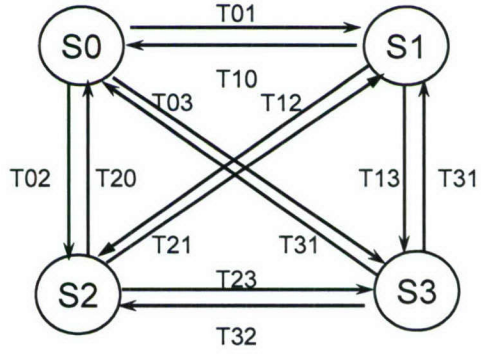


Fig. 12-26. State transitions.

T01: lose DC link voltage senor;

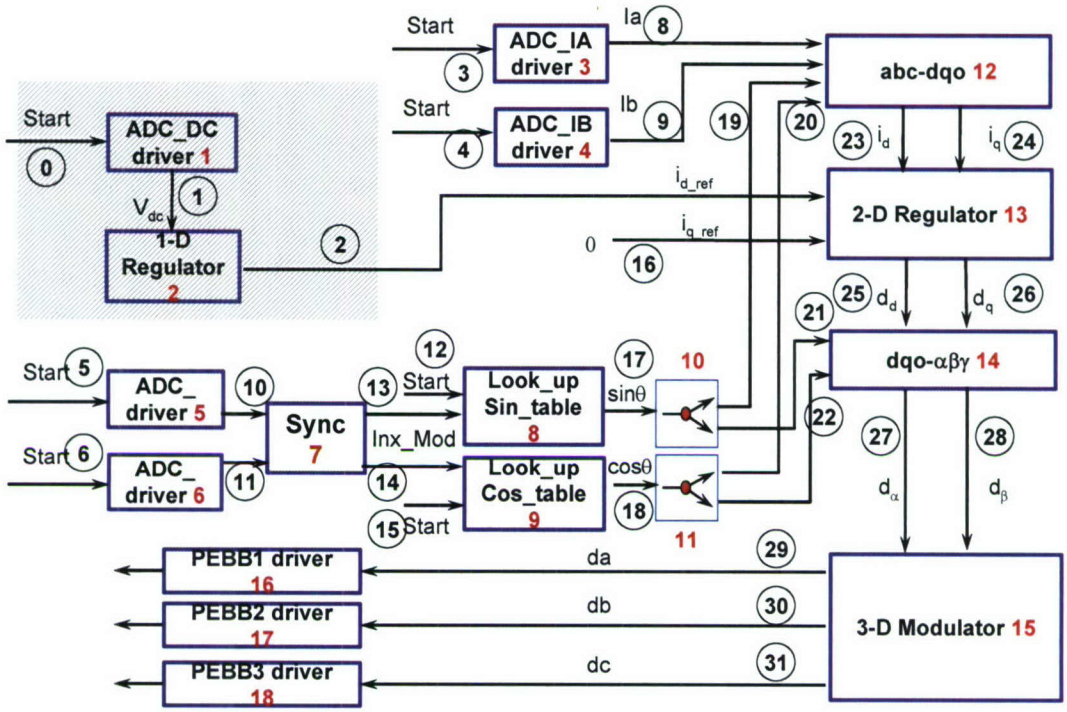
T10: DC link recovers;

T02: lose any current sensor;

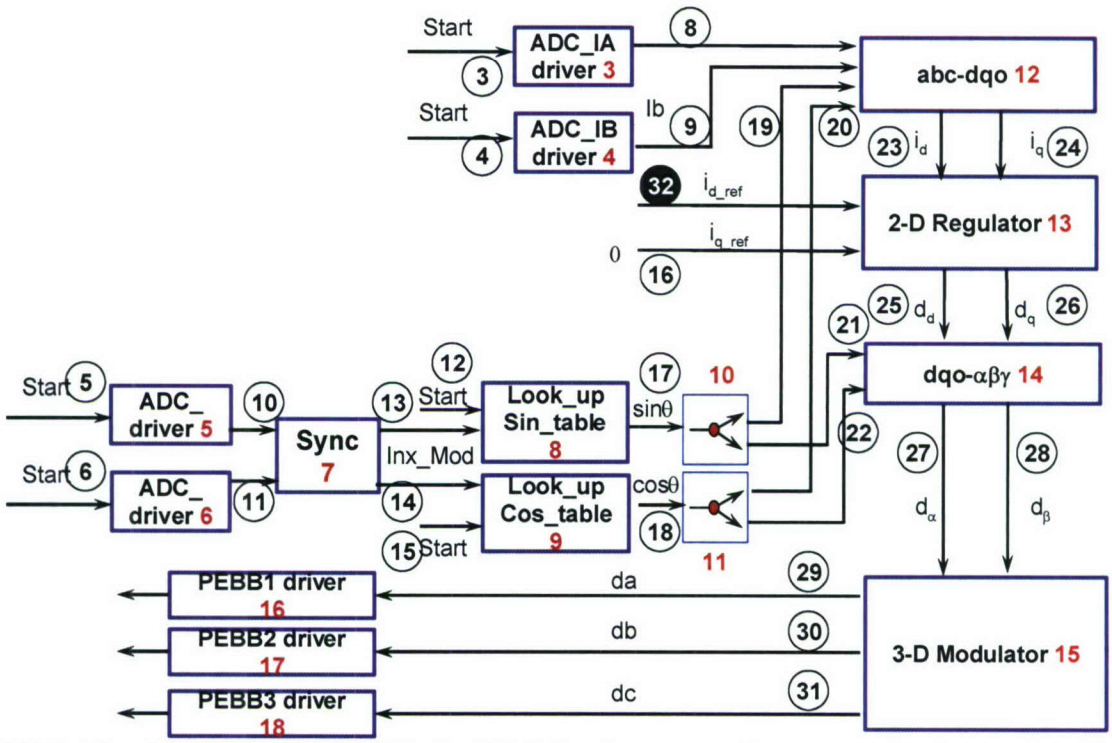
T20: the failed current sensor recovers;

....

Every system state has a corresponding dataflow graph to represent the applicable control algorithm. If all the hardware components are working in normal condition, the system is state S0 and the applicable control can be a DC link feed forward loop and a phase current feedback loop, as shown in Fig. 12-27 (a). The feed forward loop is supposed to help on system transient response to line voltage variations. In the real code implementation of a data flow graph, every ECO process possesses a unique ECO ID, and the same for data channels.



(a) Working dataflow graph (DFG0) when all hardware components are operational.



(b) Working dataflow graph (DFG1) after DC link voltage sensor is not operational.

Fig. 12-27. Dataflow graph transition caused by the loss of the DC link voltage sensor.

If the DC link voltage sensor gets failed, the feed forward sensing data of the DC link voltage is invalid and the system is in state S1. Thus, the feed forward loop should be excluded from the control algorithm,

while the current feedback control loop is still conductible if the current reference is set to be a fix value instead of taking the result from the feed forward voltage control loop in previous case. The corresponding dataflow graph is shown in Fig. 12-27 (b). However, the performance of control is degraded. This transition T01 (S0→S1) is caused by the loss of the DC link voltage sensor. The reconfiguration of control software can be implemented by switching the dataflow graph under execution from DFG0 to DFG1, which means the following:

- In the ECO processes set, ECO 1 and ECO 2 should be deactivated;
- In the data channel set, data channels 0, 1, 2 should be deactivated, and data channel 32 should be activated.

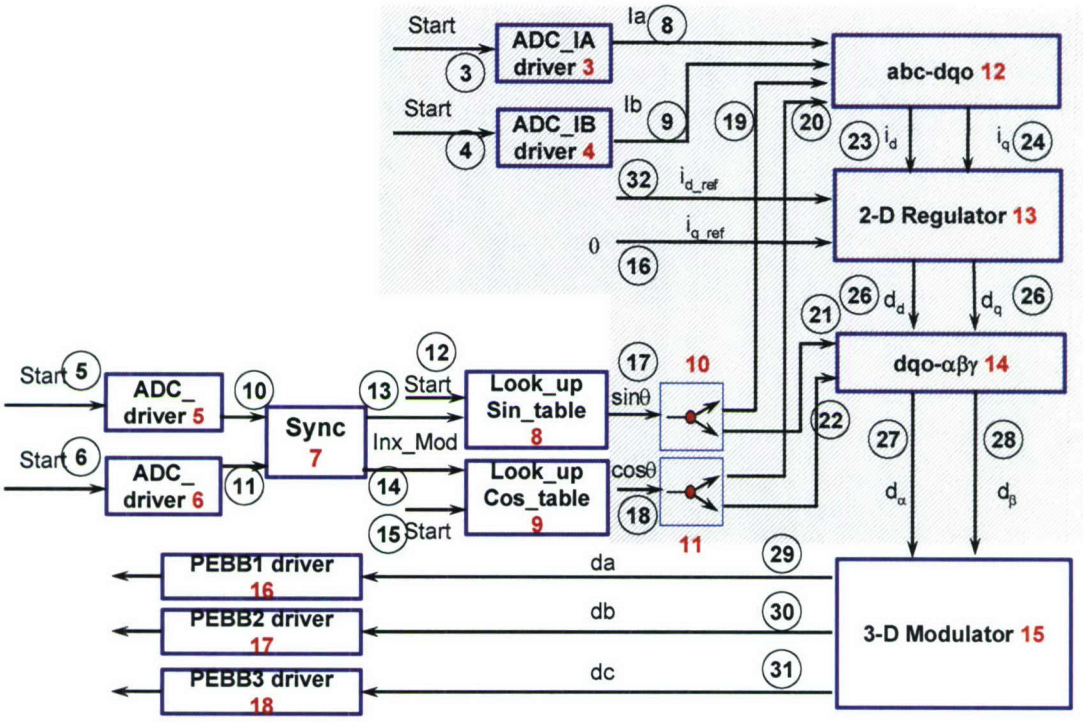
The changing part in the dataflow graph is shaded in Fig. 12-27 (a).

In the case of any current sensor failure, the system will be in state S2 and the control will have to be degraded further to an open loop version, as shown in Fig. 12-28 (b). The reconfiguration of control software can be implemented by switching the dataflow graph under execution from DFG1 to DFG2, which means the following:

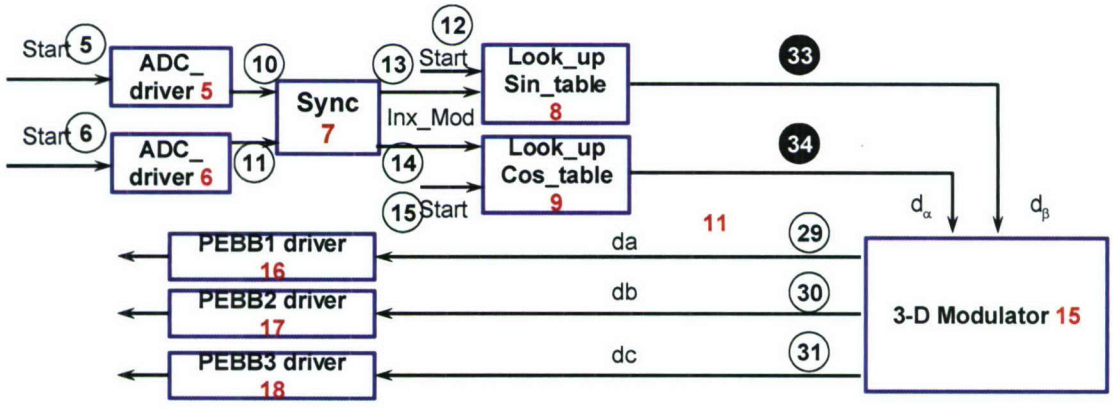
- In the ECO processes set, deactivated ECOs 3, 4, 10, 11, 12, 13, 14;
- In the data channel set, deactivated 3, 4, 8, 9, 16-28, 32, and activate 33 and 34.

In the case of any phase leg failure, for example reported over current or over voltage in any power module, the system will be in state S3 and the control should shut down all switches in order to prevent further damage to the system.

When the system state transition occurs, the control can be reconfigured through the transition of dataflow graphs. For example, when transition T01 happens, the system state changes from S0 to S1. For the control, DFG1 should substitute DFG0 to be the working dataflow graph. The transition of dataflow graphs can be implemented through deactivating the ECOs and data channels, as shown in Fig. 12-28 (a) and (b).



(a) Working dataflow graph (DFG1) when the system loses the DC link voltage sensor.



(b) Working dataflow graph (DFG2) after the system loses any one of the current sensors.

Fig. 12-28. Dataflow graph transition caused by the loss of any one of current sensors.

Since every state is related to hardware status, the transition rules between states can be defined according to the presence and absence of hardware components. Every state is associated with two masks – a hardware presence mask and a hard absence mask. In this design example 8-bit binary array will be used as mask. In the presence mask of a state Si, '1' at jth bit means a hardware component with topology ID j has to be in normal condition for state Si. '0' means optional. In the absence mask of a state Si, '1' at kth bit means a hardware component with topology ID k is required to be in failed condition. For S0, it requires that all hardware components are normal. So the presence mask for S0 will be:

Mask(0, 0) = b11111111= 0xFF.

The absence mask for S0 will be:

Mask(0,1) = b00000000 = 0x00.

Similarly, the masks for other states can be derived, and all the masks can be expressed as a two-dimensional binary array:

```
Mask[4][2] = {
        {0xFF, 0x00};
        {0xF7, 0x08};
        {0x07, 0xF8};
        {0x00, 0x07}
}
```

An 8-bit binary array (Current_Hardware_Status) can be used to represent status of the 8 hardware components, in which '1' means normal, and '0' mean failed. Every time when the Current_Hardware_Status gets changes, it will be compared to the pair of masks of each state as follows:

- ***Check 1:*** (mask1 & new_sys_state) = = mask
- ***Check 2:*** (mask2 & !new_sys_state) ! = 0

If both checks are satisfied for a state, the state will be the next state of the system. According to the current state and next state, whether a transition is necessary and the reconfiguration actions can be uniquely decided. Since for different state there is a unique dataflow graph associated with, the reconfiguration action for a system state transition can be interpreted into activation of a certain set of ECOs and data channels and deactivation of another set of ECOs and data channel. A reconfiguration matrix is such a table that records reconfiguration actions for every transition defined for the system. The declaration of the reconfiguration matrix is:

Table 12-3. Data structure declaration of reconfiguration action

```
typedef struct
{
        Transition_Priority priority;
        int *deactivate_eco;
        int *deactivate_dc;
        int *activate_eco;
        int *activate_dc;
}Reconfig_Data;
```

The transition priority means when more than one transition is possible, which transition will have the highest priority. For example, the reconfiguration action for transition S0→S1 will be defined as:

Table 12-4. Reconfiguration action for transition S0 → S1.

```
Reconfig_action[0][1] = {
        0; // transition priority
        {1, 2}; //deactivated ECOs
       {0, 1, 2}; //deactivated DCs
        {}; //activated ECOs
        {32}; //activated DCs
};
```

Thus, a reconfiguration matrix can be defined as:

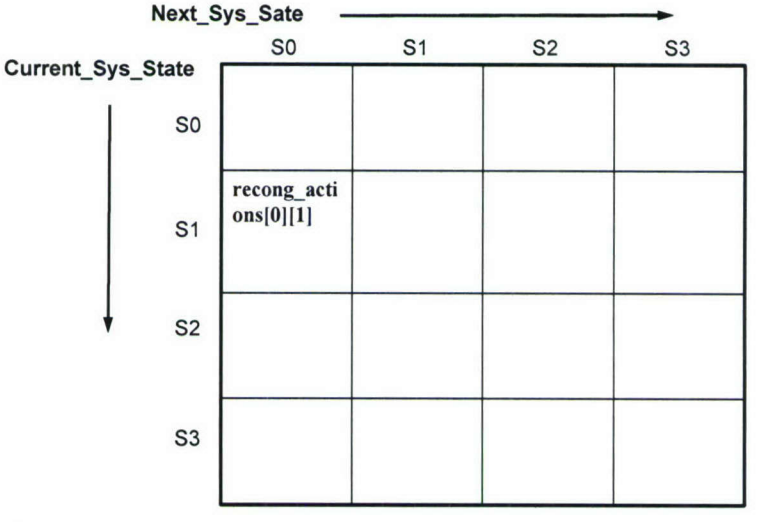


Fig. 12-29. Reconfiguration matrix.

IV.4. Further Issues Related to Online Control Reconfiguration

So far the feasibility of control reconfiguration was only been considered from the software implementation point of view. There are still several issues that need to be clarified from control point of view.

The first question is fault and exception detection. For some kinds of hardware failures, such as over current or over voltage for a power module, the detection is easy and normally a built-in function of commercialized products. But definitions for some other kinds of hardware failures are difficult or ambiguous. For example, if a reading from a sensor is abnormal, it is hard to tell whether it is due to the malfunction of the sensor or of the sensed object. The failures and exceptions in a communications network are even more complicated.

The second issue the latency of control reconfiguration. Some time will be required for the control software to reconfigure. We can define the reconfiguration latency as the time elapsed from a failure occurs until the control software responds. The question then will be how fast the control could respond to a hardware failure and what is the tolerance of this reconfiguration latency.

Another critical issue is how control reconfiguration will affect the overall system stability and whether possible transients due to control software reconfiguration are tolerable to the hardware system. In other words, for all the software components related to post-reconfiguration control and also incorporate states, how to set the values of those states to prevent system instability and help transient.

The last issue is how one can simulate dataflow control software and reconfiguration cases to analyze the performance of control software and effects of software reconfiguration.

V. Conclusions

Due to close coupling between control software and hardware, and to a lack of standardization, the legacy proprietary approach to real-time embedded control software design in power conversion systems has a number of problems. After analyzing real-time embedded control from various aspects–functionality, real time, and interactions with the real world–this research work has proposed an open control architecture to localize and encapsulate control software design dependencies from other areas in power conversion systems in order to reduce the overall design time and cost of software development. This solution provides a better mechanism for managing complexity within the problem domain. Based on the exploration of mainstream software styles, the dataflow style is chosen for open control architecture. To assess the feasibility of dataflow-based control software in power conversion systems, four design applications are implemented in this style; these range from a relatively simple open-loop, SPWM three-phase inverter to a fairly complex four-leg inverter. The levels of performance for dataflow software are compared to both handwritten main-program-and subroutine code and generated code from SimuLink + Real-time Workshop.

The advantages of the dataflow-based open control architecture can be summarized as:

- It leads naturally to a component-based design approach for control software;
- It provides a framework to support modularity, reusability and reconfigurability for software designers;
- It reduces overall development cost and time;
- It decreases the complexity of development and testing;
- It minimizes redesign effort;
- It allows designers to focus easily on key design areas;
- It facilitates system expansion and upgrades.

The main disadvantage of the dataflow architecture is the performance overhead it incurs. Initially, this overhead might be considered to be far too great for dataflow to be practical. The preliminary study reported here indicates otherwise, however. In addition, the use of hard real-time scheduling strategies to pre-compute ECO execution sequences is a fruitful avenue for exploration, offering the potential for dramatic increases in performance.

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