



**PARAMETRIC RELIABILITY OF SPACE-BASED FIELD PROGRAMMABLE
GATE ARRAYS**

THESIS

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AFIT/GE/ENG/07-19

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THESIS

Presented to the Faculty

Department of Electrical and Computer Engineering

Graduate School of Engineering and Management

Air Force Institute of Technology

Air University

Air Education and Training Command

In Partial Fulfillment of the Requirements for the
Degree of Master of Science in Electrical Engineering

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March 2007

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Abstract

The high cost of failure for microelectronic devices operating in the space environment has led to a need for an accurate characterization of a device's reliability prior to being deployed. In addition, significant cost savings can be achieved by determining this reliability prior to fabrication. High performance and flexibility requirements for many space applications have led to an integration of small feature-sized field programmable gate arrays (FPGA) into system designs. Specifically, feature sizes as small as 130, 90, and 65 nm. In this research, a characterization of the space environment is constructed specifically to address the typical conditions that can affect the performance and functionality of small feature-sized FPGAs, centered on temperature, non-ideal supply voltage, and radiation effects. A simulation technique is developed to determine the reliability of a microelectronic device prior to fabrication and deployment into the space environment. The technique is based on identifying the key elements of a circuit, simulating these key elements under each characterized condition individually, and then a comprehensive simulation of the elements under all enumerated combinations of the characterized conditions at the transistor-level using the HSPICE device simulation tool. Reliability calculations are performed based on simulation results and identified critical performance criteria. A demonstration of the technique is accomplished showing the poor reliability of non-radiation hardened small feature-sized commercial-off-the-shelf (COTS) FPGAs in four common satellite orbits around the earth. The results are then compared to an established, radiation hardened FPGA.

Acknowledgments

I would like to thank fiance for her patience and understanding.

Joseph C. Pomager

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PARAMETRIC RELIABILITY OF SPACE-BASED FIELD PROGRAMMABLE GATE ARRAYS

I. Introduction

1.1 Overview

This chapter will discuss the following topics:

- 1) Motivation for this work,
- 2) Presentation of problem statement,
- 3) Plan of attack to address this statement,
- 4) Contributions this work will provide.

1.2 Motivation

The world that people interact with has expanded. Everyday, resources are used that are non-terrestrial to complete routine tasks. This is even more evident in military objectives. To maintain expected performance on military operations, space-based assets are extensively used. The reliability of these assets can determine success or failure for a given operation. During the first Gulf War in 1991, capabilities provided by Global Positioning Satellites (GPS) allowed coalition forces to successfully maneuver without landmarks to their objectives. A failure in the GPS system during these maneuvers would have caused a greater loss of life. This reliance on space-based assets also applies to portions of the civilian sector. Companies invest a great deal of capital to acquire the capabilities offered by space-based systems. For every second an acquired space-based

system is inoperable, an amazing amount of money is lost. Reliability of performance is key to both military and civilian space-based assets.

Project costs of space-based applications are very large and most project failures are catastrophic. The upfront development costs create most often a single production item. These developmental costs, as well as the cost to put the asset in an operational position, increase the cost of failure. In 1998, the space industry lost a total of \$1.8 billion from all causes of failures [8]. Though the majority of the costs were generated through launch failures, a significant portion were caused by failures attributed to the space environment. From 1998 to 2004, there were 12 satellite failures found to be caused by radiation events that lead to a loss of \$500 million [28]. The majority of these losses could have been prevented by simulation of the effects caused by the space environment prior to placement of the microelectronic device in the system design.

FPGAs have the potential to be one of the leading causes of future failures in space-based applications due to the sensitivity of the FPGA's configuration structure. Though sensitive to the space environment, the inherent flexibility and high performance of a FPGA makes it ideal for space-based applications. Because of the increased requirements placed on space-based systems, developers have started implementing smaller feature-sized devices in their designs. The reduction in feature size leads to increased performance, but also to increased sensitivity to the harsh environmental conditions of space. There is no comprehensive research on the reliability of small feature-sized FPGAs in the space environment to include temperature, non-ideal supply

voltage, and radiation. Both COTS and radiation hardened FPGAs should be evaluated under these conditions for likely operational orbits.

1.3 Problem Statement

There is both a civilian and military demonstrated need to develop a technique to simulate or test the reliability and performance of microelectronic devices prior to fabrication and insertion into the space environment. The most notable of these devices is the FPGA due to the inherent sensitivity of its configuration mechanisms to radiation and non-ideal operating conditions. To accomplish this reliability determination, the space environments effects on a microelectronic device must first be characterized. Next, a simulation technique must be developed to test a proposed device under these effects in common operating orbits. Finally, reliability needs to be determined based off published parameters.

1.4 Plan of Attack

In this thesis, the parametric impacts on reliability caused by radiation, temperature, and dynamic power levels are explored for devices with feature sizes of less than or equal to 130 nm. A technique to simulate the cumulative effect of these impacts is developed. The simulation technique will be demonstrated by determining the parametric reliability of circuits representative of commercial-off-the-shelf (COTS) small feature-sized FPGAs. The reliability of performance will be calculated for these devices deployed in four different commonly used orbits. Architectural enhancements are then

proposed for the critical portions of a FPGA that are determined to be the most vulnerable to these effects. Finally, simulations of these modifications are performed to determine if any increase in reliability has been achieved.

1.5 Contributions

The five major contributions contained in this thesis are as follows:

- 1) A characterization of space environmental effects on bulk silicon complementary metal oxide semiconductor (CMOS) microelectronic devices in common orbits.
- 2) Development of techniques to simulate these effects using device-level circuit simulation tools prior to manufacturing.
- 3) A demonstration of this technique to show the limited expected reliability of small feature-sized non-radiation hardened FPGAs in the space environment.
- 4) Modifications to critical portions of a small feature-sized FPGA's architecture and simulations to determine if an increase in reliability of performance has been achieved.
- 5) Comparison of COTS radiation hardened FPGA reliability versus non-radiation hardened.

II. Background Information

2.1 Overview

The materials covered in this chapter are

- 1) Description of the causes of space radiation effects,
- 2) Discussion of specific radiation effects encountered by microelectronics,
- 3) Effects of non-ideal temperature to metal oxide semiconductor field effect transistor (MOSFET) devices,
- 4) Effects of non-ideal supply voltage levels to MOSFET devices,

2.2 Space Radiation Environment

Platforms that leave the protection of the Earth's atmosphere, are exposed to increased radiation hazards. Without the atmosphere to protect them, they are vulnerable to strikes by particles that travel through space with energies up to hundreds of GeVs. The three major sources of these particles are galactic cosmic rays (GCR), solar events, and particles trapped by the Earth's magnetic field.

The three major types of solar events that cause radiation effects in microelectronics deployed in a space environment are solar flares, anomalous large solar flares (ALS), and coronal mass ejections (CME). These events follow a nine to thirteen year cycle of activity. One average eleven-year cycle is composed of seven years of high activity, followed by four years of relatively quiet activity. The cyclical nature of solar events is shown in Figure 1. This model was generated using data recorded over a thirty year period by spacecraft, rockets, balloons, and satellites. The spikes in proton fluence of over 10^9 protons/cm² are defined as ALSs.

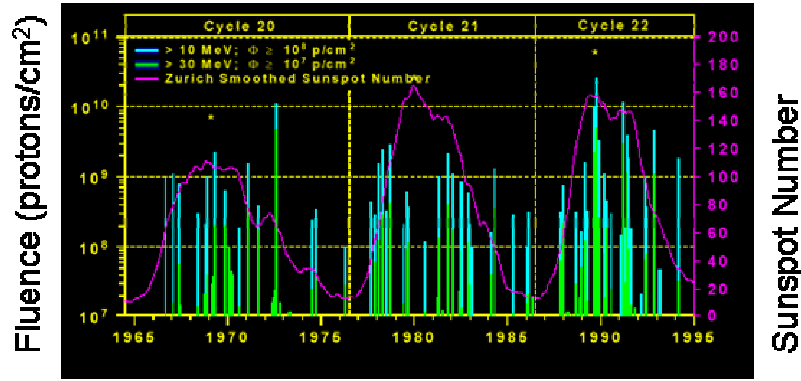


Figure 1. Solar events of >30 MeV proton fluences [8].

The most significant of these events is the CME. This event is caused by the explosive energy generated by a plasma eruption on the sun's surface. This energy rapidly accelerates particles into the solar wind. These particles can have energies up to 1 GeV, with non-trivial fluxes of $10^5 \text{ cm}^{-2}\text{s}^{-1}$. The composition of this injection of particles into the solar wind is greater than 90 % protons and only 0.1 % heavy ions [21]. Figure 2 shows the low instance rate of proton strikes greater than 92.5 MeV caused by solar events over a 22 year period.

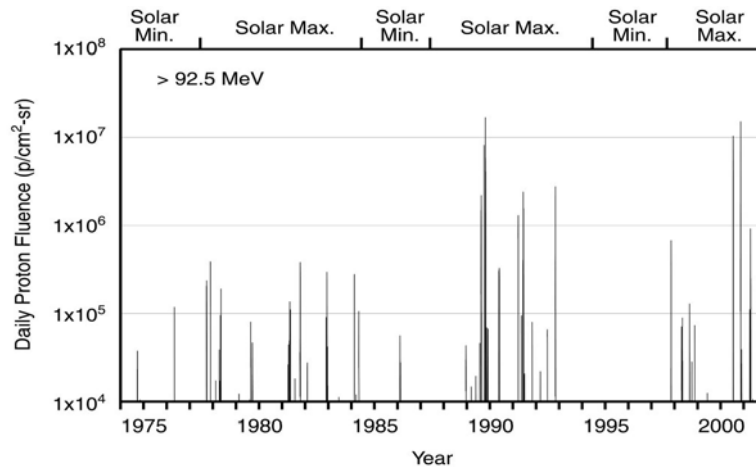


Figure 2. Intensity of protons from solar events with energies over 92.5 MeV [21].

According to Kenneth LaBel of NASA, system developers can plan for significant solar event conditions to compose only 2 % of mission time over a typical solar cycle [31]. Typical solar flare fluences are less than trapped proton fluences of similar energy. ALS and CMEs, due to their high energies and fluxes, cannot be hardened against, but must be mitigated through programming and layout techniques.

GCRs are composed of particles that originate from outside the solar system. In theory, these particles are generated by supernovas of far off stars, or maybe even during the “big bang”. These particles can have energies in the GeV range but have much less flux ($\text{cm}^{-2} \text{s}^{-1}$) than other sources of particles.

Table 1. Distance above mean sea level for common orbits.

Low Earth (LEO)	Medium Earth (MEO)	Geosynchronous (GEO)
200 km to 2000 km	2000 km to 35,786 km	35,786 km

Lower energy ($< 100 \text{ MeV}$) GCR particle strikes have a low effect on microelectronic devices in LEO and MEO due to deflection of the particles by the Earth’s magnetic field. Figure 3 shows the relationship between flux and GCR energy for GEO and interplanetary missions. The flux GCRs with a LET value of greater then 10 MeV is negligible to all calculations in this work. These events will occur less than one time a day and the strength of these events is accounted for by proton particle tolerance.

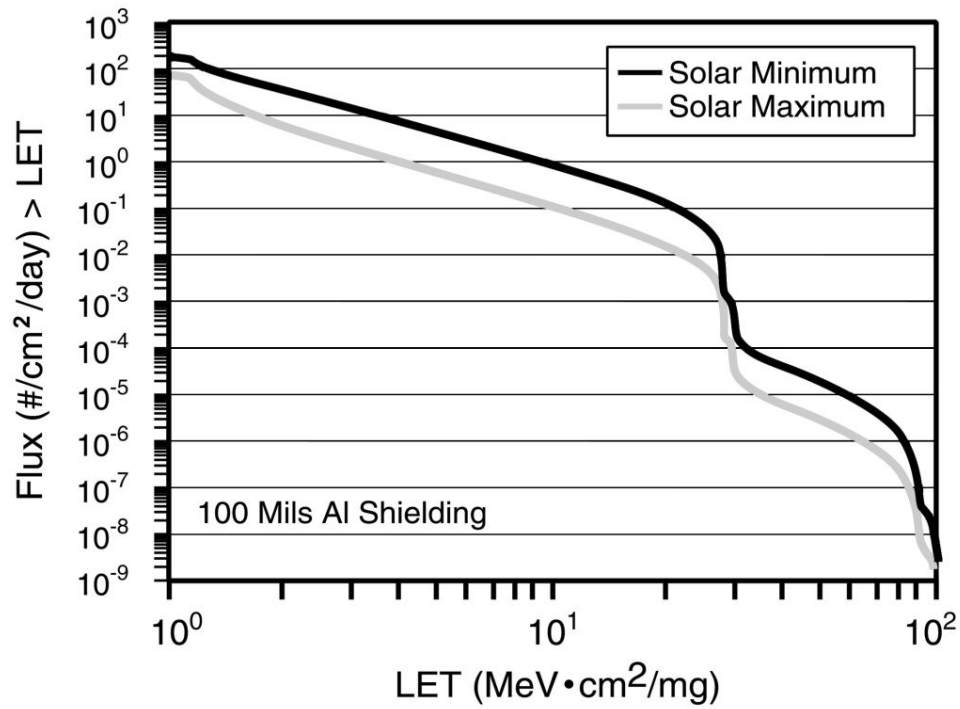


Figure 3. GCR energy vs. flux for GEO [21].

As can be seen in Figure 4, the most abundant particles in GCRs are hydrogen through iron (atomic numbers 1-26). Due to the extremely high energies and low occurrence of strikes over a mission lifetime, it is not feasible to radiation harden a CMOS microelectronic device to the extreme GCR particle strikes that are greater than 100 MeV. Lower energy strikes, as discussed prior, are at equivalent energy levels of trapped proton strikes, but at lower flux levels. Thus, the effect on reliability of these lower energy GCRs can be disregarded if trapped proton reliability effects are calculated.

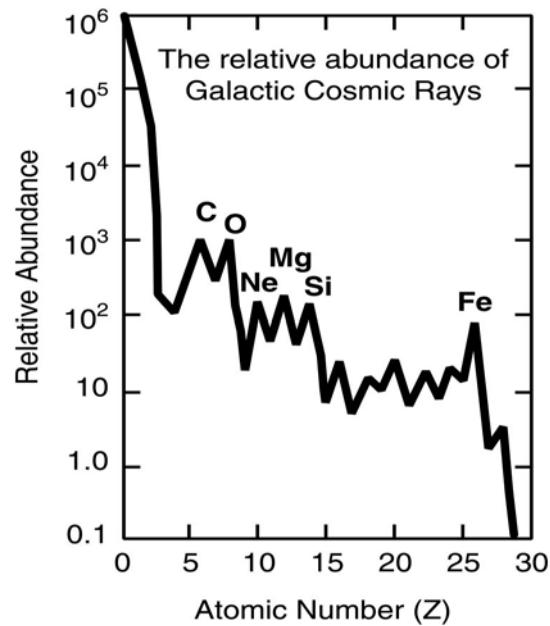


Figure 4. Abundance of elements in GCRs [21].

Particles trapped by the Earth's magnetic field can be a major radiation hazard. This trapped particle belt is composed of protons and electrons. Trapped electrons can have fluxes of up to 10 MeV at fluxes of up to $3 \times 10^6 \text{ cm}^{-2} \text{ s}^{-1}$. Light shielding prevents the majority of strikes from trapped electrons [8]. The main particle for system designers to be concerned about are protons that have been captured in the Earth's magnetic field. These particles can have energies of up to 100 MeVs at fluxes of $10^5 \text{ cm}^{-2} \text{ s}^{-1}$. If the mission allows, a platform can be placed in a LEO that is between the two major belts of these trapped particles. The Earth's magnetic field then acts as a shield to capture or deflect the majority of particles moving on the solar wind prior to reaching the sensitive electronics of these platforms in a LEO and MEO orbits. Figure 5 shows the Earth's magnetic field deflecting and trapping particles incoming toward Earth from the solar wind.

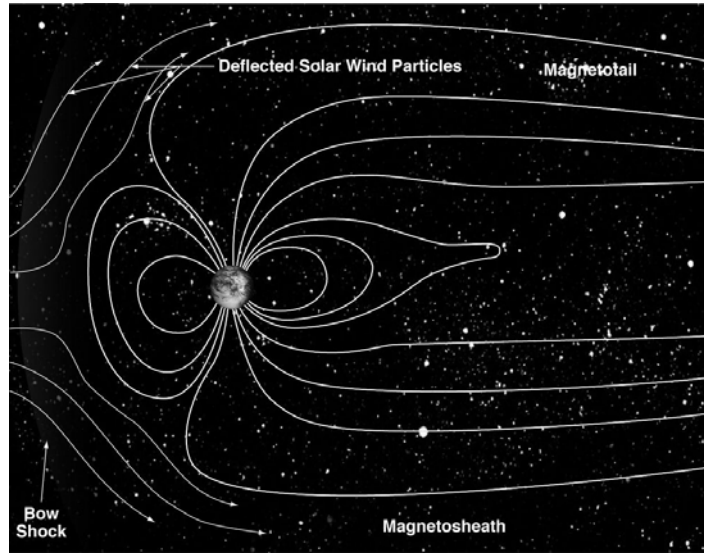


Figure 5. The Earth's magnetosphere [21].

2.3 Radiation Effects

Detrimental radiation effects are primarily caused by strikes of protons, electrons, or heavy ions. For the purpose of this work, we can disregard the effect of electron strikes due to the relatively light shielding required to protect against them. It requires only 200 mil of aluminum to negate the effects of most electron strikes [8].

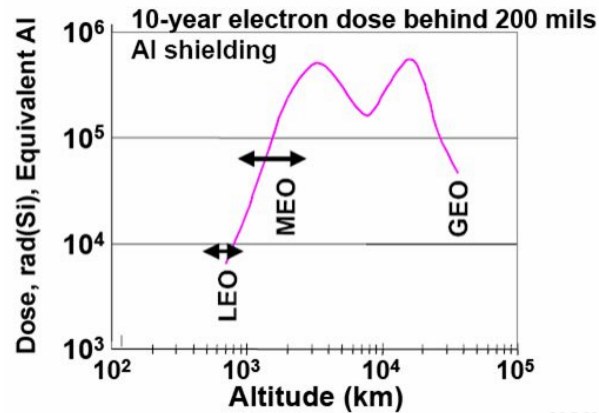


Figure 6. Electron dose over a 10-year period with 200 mils of shielding [8].

Proton and Heavy ion strikes caused by the phenomenon discussed in the space radiation environment can lead to both recoverable and non-recoverable faults in MOSFET transistors.

A strike by these particles will create electron and hole pairs along the path of penetration. The “funnel” created by the strike will dissipate quickly, but momentarily a channel will be formed between the surface and the substrate. This behaves like a wire, connecting the portion of the MOSFET hit by the particle strike to the body of the device. Figure 7 shows the funnel created in a MOSFET device. The depth of these penetrations are determined by the energy of the particle, the type of particle, and the material it is striking. This characteristic of a particle is described as its linear energy transfer (LET). LET is the amount of energy deposited in a material by a particle as it penetrates in units

of $\left(\frac{\text{MeV} \cdot \text{cm}^2}{\text{mg}} \right)$.

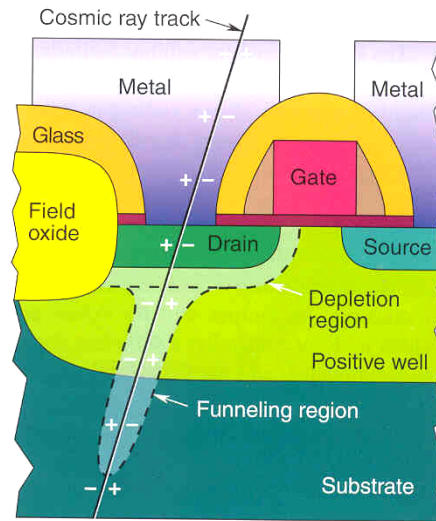


Figure 7. Electron/hole pairs created by particle strike [43].

The main consequence of one of these particle strikes to designers of CMOS circuits are single event effects (SEE). This effect is the result of a change in voltage level on the affected area due to a momentary connection to the substrate. The results of SEEs are transient pulses in combinational or linear circuits, 'bit-flips' in storage devices, or latch-up in older, low performance technologies.

Another effect caused by a single particle strike is displacement damage (DD). This happens when the particle passing through a material penetrates the crystal lattice of the silicon. This penetration results in a displacement of atoms that can have a negative effect on the drain to source current of a MOSFET. This result has minimal effect on the actual performance of MOSFET transistors and is not discussed further in this work.

Single event latch-up (SEL) is also caused by single particle strikes. SEL can be described as the state a MOSFET is in when the channel created by the particle strike allows current to flow unregulated between areas of potential difference in the device. This effect can cause permanent damage to a transistor, but is not a significant problem for modern electronics due to the popular use of an epitaxial layer in the construction of most devices.

Over time, a device will be struck by multiple particles. Each of these strikes leaves a residual charge that can accumulate over time and reduce the performance of the device. Holes will slowly migrate to the top of the gate oxide. After enough are there, the device will be inoperable, with either a permanently open or closed channel. This effect is classified as total ionizing dose (TID), and is primarily caused by electron or ion strikes.

As was shown in Figure 6, light shielding can decrease the amount of dose accumulated. This effect will not be addressed in this work.

Table 1 contains a summation of the sources of particles and their effects on MOSFET devices. An analysis of the data in the table shows that with the exception of GCRs, radiation hardening a circuit to a proton strike of 100 MeV at a flux of $10^5 \text{ cm}^{-2}\text{s}^{-1}$ will classify a circuit as radiation hardened. GCR and ALS must be addressed through mitigation techniques such as redundancy and strategic programming due to their high worst-case energies. Particle energies and fluxes that a microelectronic device will encounter are mission specific. The strength and abundance of a particle over time is dependant on orbit, solar cycle, and shielding. Characteristics for customized orbits can be estimated using modes such as AP-8, AE-8, CRÈME, and SOLPRO [34],[35],[36].

Table 2. Summary of radiation phenomena and their effects on MOSFETs.

Phenomena	Energy MeV	Intensity $\text{cm}^{-2}\text{s}^{-1}$	Effects
Trapped Protons	Up to 100s	$< 1 \times 10^5$	TID, DD, SEE
Trapped Electrons	< 10	$< 3 \times 10^6$	TID, DD
Galactic Cosmic Rays	Up to 1000s	< 10	SEE
Solar Events	Up to 100s	$< 1 \times 10^5$	TID, DD, SEE

2.4 Temperature Effects

Electronic components utilized in a space environment need to be able to operate correctly at a wide range of temperatures. According to guidelines published by the Defense Supply Center [7] normal operating temperatures in a satellite range from -35 °C to 60°C. However, at worst case the guide recommends designers to plan for operation at temperatures as low as -45 °C and as high as 90 °C. At these temperatures, the transistors that make up the critical components of a FPGA can behave in an undesirable manner. This can lead to incorrect operation or even failure of the device. The two major effects of non-ideal temperature are threshold voltage shift for transistors in the “off” state, and a decrease in saturation current for transistors in the “on” state.

The threshold voltage of a MOSFET transistor is very dependent on temperature. The following approximation in equation (1) shows the linear relationship of threshold voltage to temperature

$$V_t(T) = V_t(T_r) - k_{vt}(T - T_r) \quad (1)$$

where V_t is threshold voltage in Volts, T is the absolute temperature in Kelvin, T_r is the room temperature in Kelvin, and k_{vt} is a fitting parameter [1]. Equation (1) shows that an increase in temperature will lead to a decrease in threshold voltage. This decrease results in a higher leakage current, which can lead to an undesired operation of critical portions of a circuit, as well as increased power consumption.

An increase in temperature will also lead to an decrease in saturation current. This is due to the saturation current of a MOSFET being directly related to mobility as can be seen in

$$I_{ds} = \mu C_{ox} \left(\frac{W}{L} \right) (V_{gs} - V_t)^2 \quad (2)$$

where I_{ds} is the drain to source saturation current in amps, C_{ox} is the gate oxide capacitance, W is the width of the channel, L is the length of the channel, V_{gs} is the gate to source voltage, V_t is the device threshold, and μ is the mobility [29].

Mobility can be described as

$$\mu = \frac{E}{v} \quad (3)$$

where μ is mobility in $\text{cm}^2/\text{V}\cdot\text{s}$, E is electric field between the source and drain, and v is average carrier velocity in the channel [6]. An approximate relationship between mobility and temperature is shown in

$$\mu(T) = \mu(T_r) \left(\frac{T}{T_r} \right)^{-k_\mu} \quad (4)$$

where T is absolute temperature, T_r is room temperature, and k_μ is a fitting parameter in the range of 1.2 to 2.0 [1].

An example of non-ideal temperature affecting the mission of a satellite occurred in April of 1993. The GOES-7 experienced a one-hour period where communication was unreliable due to an eclipse decreasing the temperature to a point that the frequency of the receiver surpassed its 5 kHz frequency limit [5]. This was due to the decrease in threshold voltage and increase in saturation current of the MOSFET transistors in the receiver. The device operated faster, but at a speed that was out of design constraints.

2.5 Non-Ideal Supply Voltage Effects

Small feature-sized integrated circuits do not have much tolerance for non-ideal supply voltage in their design. To have correct operation of the individual transistors that comprise these circuits, a predictable potential difference between the supply voltage and ground must be maintained. If this voltage increases or decreases by a significant amount, operations will not be performed correctly due to failures in specific transistors or timing of synchronous portions of the circuit.

In a terrestrial environment, the majority of failures for a non-ideal supply voltage are caused by users of the microelectronic device. This is due to the device being deployed in a controlled environment. In a non-terrestrial environment though, there are a number of natural environmental factors that can temporarily or permanently alter the supply voltage to an integrated circuit. According to a NASA case study of over 100 mission failures over a twenty-year period [5], the major causes of non-ideal power conditions are a result of the following five environmental factors:

- 1) Power supply performance due to the thermal environment,
- 2) Shift in floating potential, current loss, and re-attraction of contaminants due to plasma,
- 3) Power allocation due to the solar environment,
- 4) Degradation in solar cell output due to ionizing radiation,
- 5) Induced potential effects due to magnetic fields.

In a MOSFET, when a voltage bias is applied to the gate and passes a certain level, a channel will be formed between the drain and the source of the device. The

conductance of the channel varies depending on the potential difference between the gate and the body. Assuming a potential difference exists between the drain and the source, when a bias voltage is applied to the gate relative to the body and exceeds V_t , a channel will form between the drain and source allowing current to flow.

A change in the supply voltage for a circuit will lead to a change in the maximum voltage able to be applied to portions of a transistor in the circuit. If this level falls below V_t , a transistor will not function. If there is a reduction in supply voltage, but it is still greater than the V_t of a transistor, the switching characteristics of the transistor will change. For a negative-channel metal-oxide semiconductor (NMOS) the amount of time for the drain current to fall to sub-threshold levels will decrease which leads to faster “off” transitions. For positive-channel metal-oxide semiconductors (PMOS) devices, the opposite is true, faster “on” transitions. Timing is crucial to the performance and operation of modern synchronous Complementary Metal Oxide Semiconductor (CMOS) circuits. Changes in states or values of transistors are expected to occur at certain intervals. If these intervals are not in the designed period, the circuit will not behave as designed.

The reduction of the voltage between the gate and the source can also lead to a less robust performance. As supply voltage decreases, the threshold voltage will remain constant due to the threshold voltage being a function of process parameters and temperature as given by

$$V_t \approx \frac{\sqrt{2\epsilon_s q N_A (2\Psi_B)}}{C_0} + 2\Psi_B \quad (5)$$

$$\Psi_B = \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right) \quad (6)$$

where V_t is the threshold voltage in volts, ϵ_s is the permittivity of silicon, q is $1.60218 \times 10^{-19} \text{ C}$, Ψ_B is the potential required for strong inversion, k is boltzmann's constant, C_0 is the gate capacitance per unit area, N_A is the density of carriers, n_i is the intrinsic carrier concentration, and T is temperature [6]. Since the maximum voltage level that can be applied to a node has been decreased, transistors will be more sensitive to unforeseen fluctuations in voltage levels. These unforeseen fluctuations are expected in the operation of an integrated circuit and thus designers implement tolerances or margins in their designs to ensure predictable operation of the circuit. As these tolerances (noise margins, radiation, and manufacturing variations) decrease, the predicted reliability of a circuit becomes unknown.

III. Methodology

3.1 Overview

This chapter discusses the developed simulation method to determine reliability of a microelectronic device prior to deployment in the space environment. The simulation structure is comprised of the following four steps

- 1) Identification of critical components,
- 2) Simulation of each component with respect to each phenomena separately,
- 3) Comprehensive enumerative phenomena simulation for each element in each sensitive state,
- 4) Reliability determination.

The simulation structure is described in general, and in detail of how it applies to the specific FPGA models used for the simulation demonstration.

3.2 Choice of FPGA Models

To demonstrate the low reliability of COTS FPGAs in the space environment models developed were based upon the Virtex II Pro, Virtex 4, and the Virtex 5. All of the Virtex family of FPGAs have similar architectures, but have implemented newer technologies in each generation. Specifically the generational reduction in feature size has lead to a higher transistor density on the device. This leads to a decrease in the reliability of the FPGA in the space environment due to the increased number of total radiation sensitive areas and the reduction in radiation induced noise tolerance. Table 3 and Table 4 list parameters of a minimum, nominal, and maximum instance of each device. The number of configuration bits is especially important when determining space

reliability of a FPGA. As can be seen, the number of configuration bits range from 1.3 million bits to 82 million bits. Each of these bits plays a key role in the configuration of the devices. Configurable logic blocks (CLB) are the heart of FPGA functionality. These are cells or blocks in the device that can be configured to perform multiple functions. CLBs are what give FPGAs the flexibility that makes them so useful. Feature size of the FPGAs is of particular importance to space reliability. The length of the channel between the drain and source of a MOSFET directly affects the area on a device that is sensitive to particle strikes. It is shown in Table 3 and Table 4 that the feature size or channel length ranges from 130 nm to 65 nm. The last parameter of interest is the maximum clock frequency. This parameter will be used in reliability calculations to determine the impact of the space environment on FPGA reliability.

Table 3. Significant Virtex II Pro and Virtex 4 parameters [11], [12], [13], [14], [15].

	Virtex II Pro			Virtex 4		
	Min	Nominal	Max	Min	Nominal	Max
Product Number	XC2VP2	XC2VP40	XC2VP100	XC4VLX15	XC4VSX55	XC4VFX140
Conf Bits	1.3 M	12 M	35 M	5 M	24 M	50 M
CLBs	5,632	77,568	176,384	24,576	98,304	272,672
Feature Size nm	130	130	130	90	90	90
Max Clock MHz	400	400	400	500	500	500

Table 4. Significant Virtex 5 parameters [17], [18], [19].

	Virtex 5		
	Min	Nominal	Max
Product Number	XC5VLX30	XC5VLX110T	XC5VLX330T
Conf Bits	8 M	31 M	82 M
CLBs	19,200	69,120	207,360
Feature Size nm	65	65	65
Max Clock MHz	500	500	500

3.3 Determining Critical Portions of Circuit

Analysis of a circuit is the first step of the simulation procedure. By careful examination of the design of a microelectronic device, certain information can be gained to limit the number of simulations. It is unreasonable to simulate every device, in every state to perform reliability calculations. The focus of the analysis is centered on the following three main points:

- 1) Identification of elements that failures are non-recoverable,
- 2) Identification of the most abundant elements in a design,
- 3) Identification of the least radiation tolerant elements.

Failures in microelectronic devices can be classified into the following categories: recoverable, non-recoverable, and transparent. The most catastrophic failure is the non-recoverable case, which leads to permanent circuit damage. Early identification of the elements and their sensitivity to the space environment effects that can cause non-recoverable failures is paramount to a reliability determination. Recoverable errors do

not have the drastic effect of circuit damage, but can cause a decrease in circuit performance because of the time it takes for a circuit to recover. Transparent failures of a device result in no noticeable effect to circuit performance or functionality. These failures can be disregarded during circuit analysis.

As discussed earlier, modern FPGAs have the built in functionality to be reprogrammed. This is accomplished by rerouting the interconnect of the device. Bits that direct both the data and control interconnect are stored in static random access memory (SRAM). The SRAM's output controls a pass transistor that acts like a switch for the interconnect, see Figure 8. These two elements have been demonstrated to be the leading cause of failure in SRAM based FPGAs [23]. The majority of SEEs in a FPGAs are considered recoverable or transient in nature and can be detected, then corrected through efficient programming of the device. Failures or bit upsets in the configuration logic are not possible to detect through these methods though, and lead to errors that are not recoverable without a time consuming reset of the device.

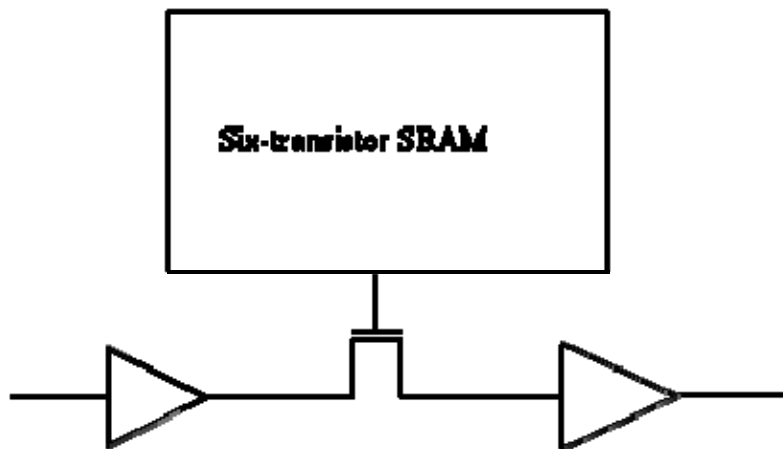


Figure 8. SRAM controlling a pass transistor.

The most widely used configuration storage structure in SRAM-based FPGAs is the six-transistor SRAM cell. The configuration shown in Figure 9 is a representation of the SRAM cell used for the simulations in this work. The SRAM consists of two cross-coupled inverters that constantly refresh each other. This continual refreshing of the stored bit makes the cell vulnerable to particle strikes.

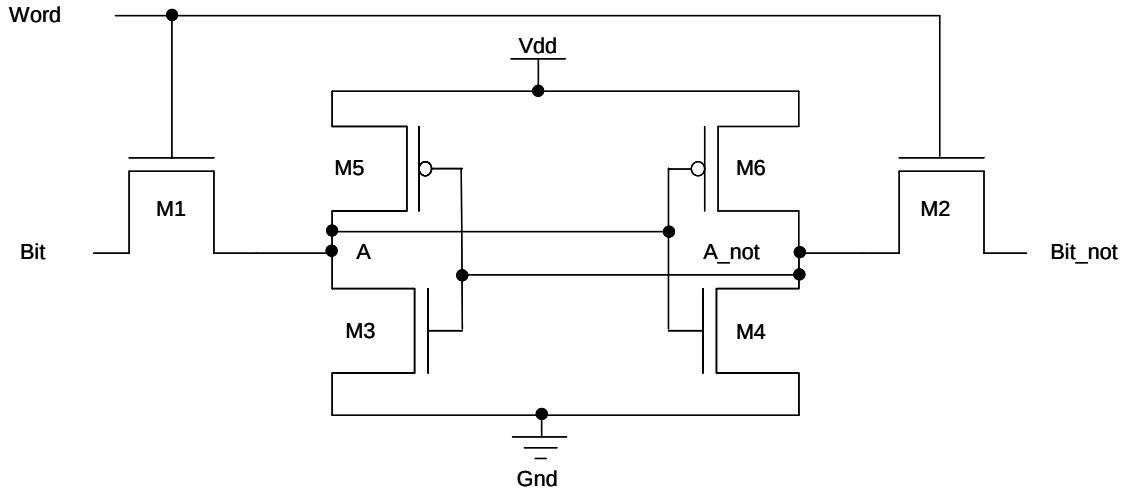


Figure 9. Six Transistor SRAM cell [29].

The pass transistor portion of the configuration cell, though an integral part will not be addressed by this work. This work focuses on the effects of non-ideal temperature, power, and particle strikes affecting the pn junction of the drain on a CMOS minimum-sized NMOS transistor and appropriately sized PMOS transistor that have equal rise and fall time delays. A strike forming a channel between the gate and the body is the main weak spot for the pass transistor. This phenomena will be discussed in future works..

Combinational logic is the cornerstone of data routing and manipulation in FPGAs. It forms the multiplexers, as well as the logic to perform operations. With the exception of TID effects, the majority of failures seen in combinational logic are transient. The duration of these transient effects is investigated in simulation to determine effects on reliability

Synchronous operation and temporary data storage are required by most applications. The critical component of a FPGA that gives it the option to have this flexibility are flip-flops (FF). The sensitivity of a FF to the space environment will not be discussed in this work, as it has already been addressed in prior works [24].

3.4 Technique for Radiation Simulation

The worst-case radiation effects to microelectronics in the space environment are caused by particles from GCR and CME. These particles have extremely high energies, up to the GeV range, but low flux. Many platforms never experience a strike of this magnitude [26]. The effects from these events must be addressed with mitigation. As discussed earlier, if a device can be radiation hardened to handle 100 MeV proton strike, the device will be able to tolerate SEEs from other particles. The energy transferred to the device as a particle passes through is directly related to the incident energy of the particle, the type of element, and the substrate material. Figure 10 shows the energy absorbed by silicon per micrometer for different elements. With the exception of krypton, which has a low instance rate in space, iron has the greatest stopping power of common elements at 100 MeV.

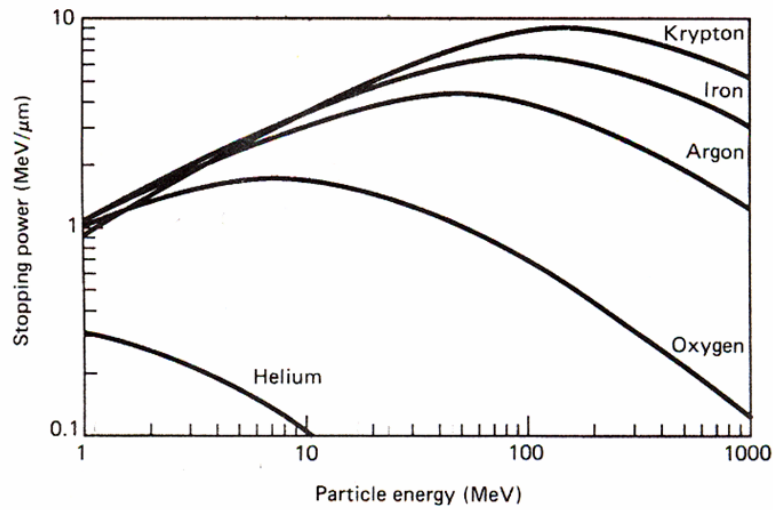


Figure 10. Stopping power vs. different ions in silicon [30].

It is concluded that a proton strike at 100 MeV will be a comprehensive representation of likely particle strikes. If the circuit tolerates the effects caused by this strike, it will be able to tolerate strikes by particles with lesser energies.

To simulate this strike using SPICE, a method was needed to mimic the behavior of the node in question. As discussed earlier, when an ion penetrates the drain of a device, a temporary channel is formed by residual electron and hole pairs left in the material. This will cause a momentary connection or funnel between the drain and the body of a MOSFET device. Figure 7 shows the funnel created by the electron/hole pairs.

This effect can be represented in SPICE as a current source on the node of the drain that has been penetrated by a particle. Figure 11 is a transistor level representation of a particle strike on the drain of M5 in a SRAM cell.

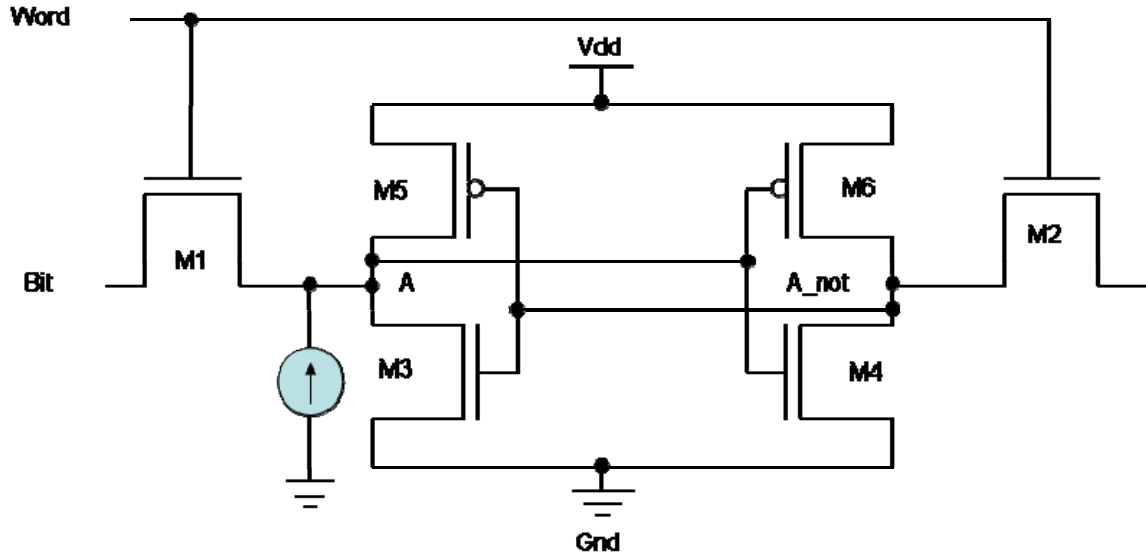


Figure 11. SRAM cell with current source injected to simulate particle strike.

The current source characteristics were developed using a model based on the Dorkel Model for estimating carrier mobilities in silicon [24], [25]. A graph of the magnitude of the current source used to simulate the proton strike is shown in Figure 12. There is a quick 100 ps spike, followed by an exponential decay of the current magnitude as the electron/hole pairs dissipate.

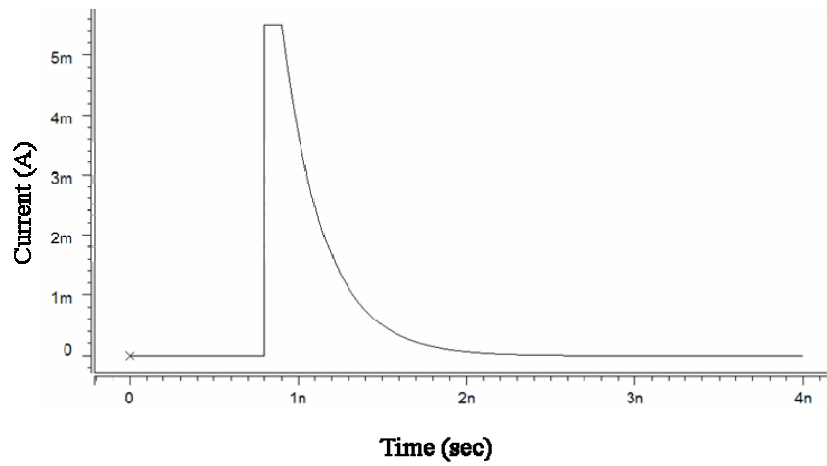


Figure 12. Current source representation of 100 MeV Fe proton strike.

The current source is injected at states and nodes during the simulation when the effects will not be transparent. For NMOS transistors on sensitive nodes, the current source is connected between the node and the body of transistor when the drain is at a positive voltage level. For PMOS transistors on sensitive nodes, the current source is connected when the drain is at the reference voltage level (gnd). These nodes and states will be different for each circuit of interest and are discussed in more detail later.

The measure of a particle strikes effect on the reliability of an element is dependant on the function of the element. For combinational logic, the amount of time that erroneous data is output is considered. This effect can have significant effects on synchronous devices. If the erroneous data propagation time is greater than the clock or setup/hold time of the next synchronous element in the signal path, the erroneous data may be latched and become permanent. Asynchronous devices see little effect from this type of error. Storage elements main criteria for failure is a 'bit-flip'. This is when the strike changes the value of the stored data. The main criteria for failure for a synchronous device such as a FF is a state change. The sudden current spike and change in potential on some nodes may cause the state of the FF to change.

The inverter implemented in the simulations and shown in Figure 13 is vulnerable in two different states.

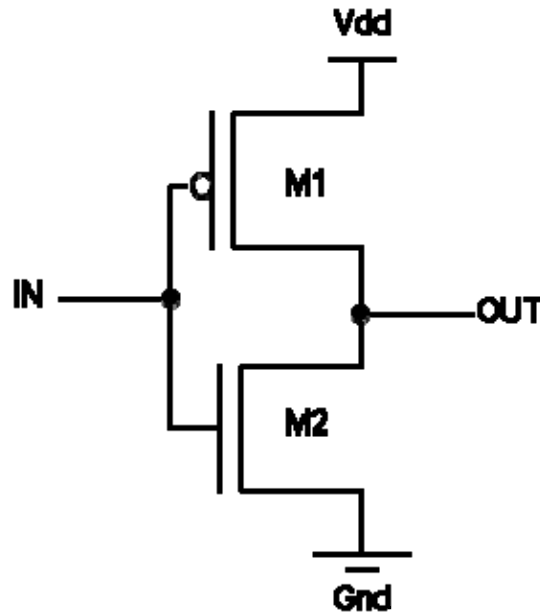


Figure 13. Inverter cell [29].

The first vulnerable area is the drain of M1 when the input is a '1'. The current source discussed earlier is applied for the specified period from the body of M1 (Vdd) to the OUT node. The other vulnerable area is the drain of M2 when the input is '0'. To simulate the effect using SPICE, the current source was injected from the body of M2 to the OUT node. To determine the impact on reliability, the time the difference of the out node of the load circuit's voltage level and supply voltage was more than 50% of the supply voltage level was measured.

There are three main areas of the implemented NAND gate in Figure 14 that when hit with a proton strike, the effects will not be transparent. The three areas are the drain of M1 or M2, the drain of M3, and the node MIDN. The drain of M1 or M2 is susceptible when both IN1 and IN2 are '1'. The momentary channel formed will create a path between the drain of M1 or M2 and the body of the PMOS transistor that is at Vdd.

When the inputs to the NAND gate are at $IN1 = '0'$ and $IN2 = '1'$, the drain of node MIDN is a point of interest. For a short period, current will flow from the OUT node, through M3, and to the body of the NMOS along the path created by the electron hole pairs that are left behind by the proton strike. The last vulnerable area is the drain of M3. Anytime $IN1$ is '0' or $IN2$ is '0' and there is a particle strike to the drain of M3, there is a possibility of wrong output values on the OUT node. To determine the impact on reliability, the time the difference of the out node of the load circuit's voltage level and supply voltage was more than 50% of the supply voltage level was measured.

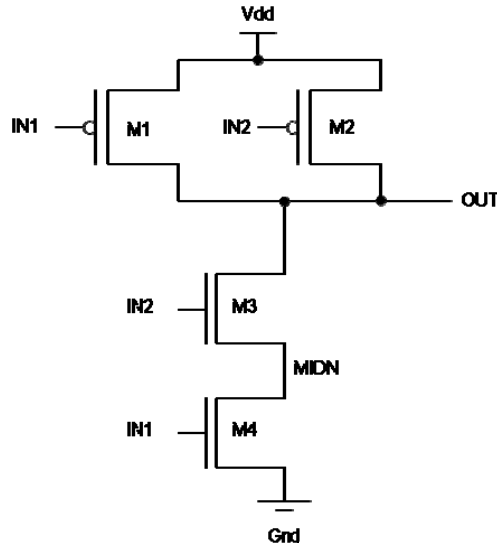


Figure 14. NAND gate [29].

The technique for simulating a 100 MeV iron proton strike on a XOR gate is similar to that of the NAND gate with the exception of more vulnerable areas. The implementation of the XOR gate can be seen in Figure 15 with all nodes labeled.

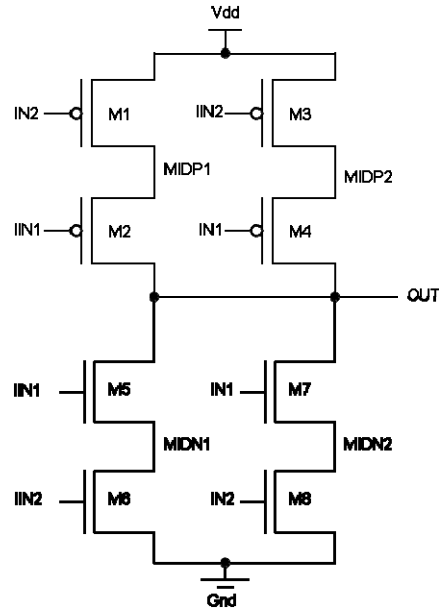


Figure 15. XOR gate [29].

The XOR gate has a total of eight vulnerable states and nodes that will have transient effects on the output. The eight states and nodes of interest are shown in Table 5.

Table 5. States of interest for XOR proton strike simulation.

Strike Location	IN1	IN2	Current Direction
Node MIDP1	Vdd	Vdd	Vdd to MIDP1
Node MIDP2	Gnd	Gnd	Vdd to MIDP2
Node MIDN1	Gnd	Vdd	MIDN1 to Gnd
Node MIDN2	Vdd	Gnd	MIDN2 to Gnd
Drain of M2	Gnd	Gnd	Vdd to OUT
Drain of M4	Vdd	Vdd	Vdd to OUT
Drain of M5	Vdd	Gnd	OUT to Gnd
Drain of M7	Gnd	Vdd	OUT to Gnd

The results of a proton strike on nodes that have the same transistor characteristics and paths from their source to the output will be the same. This allows the reduction of the number of states to simulate to four: drain of a PMOS transistor on the OUT node, drain of a NMOS transistor on the OUT node, a MID node in the PMOS portion of the XOR, and a MID node in NMOS portion of the XOR. Like the other combinational logic tested in this work, the time the strike effects the output of the next circuit in the load is measured. The measurement is performed for the time the output of the next circuit in the load is greater than 50 % of the supply voltage for low to high effects and less than 50 % of the supply voltage for high to low effects.

A six-transistor SRAM cell has similar vulnerable states. The SRAM cell shown in Figure 9 is representative of the cell used in the configuration logic of many FPGAs. The main states of interest for proton strike simulations are the ones that will disrupt the stored value temporarily or even permanently change its value. The states where this is possible are listed in Table 6.

Table 6. States of interest for SRAM ion strike simulation

Strike Location	Stored Value	Current Direction
Drain of M1	Vdd	A to Gnd
Drain of M3	Vdd	A to Gnd
Drain of M5	Gnd	Vdd to A
Drain of M2	Gnd	Vdd to A
Drain of M4	Gnd	Vdd to A
Drain of M6	Vdd	A to Gnd

Strikes at the drain of M1 and at the drain of M3 will have similar effects. This is also true for strikes at the drain of M2 and drain of M4. Due to the strikes having the same effect on the circuit, only one of each case was simulated as representative of the strike.

3.5 Technique for Temperature and Non-Ideal Power Simulations

As discussed earlier, MOSFET devices are very sensitive to non-ideal temperature and supply voltage levels. The expected operating conditions for COTS FPGAs is room temperature with an ideal supply voltage. Tolerances are built into devices to handle normal variations in the environment. Microelectronic devices are fabricated with commercial, industrial, and military standards. The specific ranges of these temperatures are shown in Table 7. Microelectronics in the space environment have a normal operating temperature of -35°C to 60°C , but the defense supply center states that in worst-case conditions, system developers should plan for a temperature range between -40°C to 90°C [37]. Simulations were performed using the -40°C to 90°C range based on the recommendation.

Table 7. Operating temperature standards for microelectronic devices.

Commercial	Industrial	MIL-PRF-38535 [37]
0°C to 70°C	-40°C to 85°C	-55°C to 125°C

The Virtex family of FPGAs have a recommend internal supply voltage range of 5 %. Studies from NASA have indicated a non-ideal supply voltage over time due to

factors listed in Chapter 2. Because of this, reliability simulations were performed using a supply voltage range from 70 % to 130 % of nominal.

The NAND gate shown in Figure 14 has three states of interest to both power and temperature simulations. The first state is when both NMOS transistors are allowing current to flow due to a '1' being applied to both the inputs, which leads to a '0' on the output. To determine the effect on delay of both temperature and power in this state, the inputs IN1 and IN2 were both initially set to '0'. After .5 ns, both inputs were increased to the supply voltage level with a rise time of .07 ns and held there for 1.59 ns. Both the rise time and period were estimated from data listed in the Xilinx publications [11],[15],[19]. Propagation delay measurements were then performed using the measure function in SPICE. Measurements were started when IN1 was at 50 % of the supply voltage and completed when OUT was equal to 50 % of the supply voltage. The next state is when either of the PMOS transistors have a channel formed from source to drain due to a '0' being applied to either inputs. The same technique that was utilized to measure the propagation delay for the first state is used with minor changes due to the 0 to 1 transition. The final state of interest is when both PMOS transistors have channels formed from their source to drain. Simulations are run for each of these three states sweeping the power and supply voltage levels for each. The delay is recorded for each temperature and supply power level to demonstrate the effects.

The techniques used for simulation of the XOR gate shown in Figure 15 to demonstrate effects of non-ideal temperature and power are the same techniques that were used for the NAND gate. The differences are in the states that are of interest to this

work. The first state of interest is when both inputs are initially at '0'; this leads to a '0' on the output. Either of the inputs are then changed to the supply voltage level to force a low-to-high transition on the output. The propagation delay is then measured. The two other states follow the same basic method, but are looking at a high-to-low transition on the OUT node. To achieve a starting condition of a high value on the output, IN1 and IN2 are stimulated with opposite values. After 0.5 ns, both inputs are made high for the second state and both inputs are forced low for the last state.

To characterize the changes in behavior of the SRAM cell in Figure 9 due to non-ideal supply voltage and extreme temperature operating conditions simulations were performed. After analysis of the cell, only two states required simulations. The delay was measured on the output of the load circuit during both a low-to-high and high-to-low transition. These simulations were repeated for all temperature and voltage ranges discussed earlier.

3.6 Comprehensive Simulation Technique to Determine Reliability

Each of the simulation techniques discussed earlier focus on one area that could cause a disruption or failure in critical portions of CMOS circuits. To determine reliability, the simulation method shown in Figure 16 was used. It combined simulations for non-ideal power, extreme temperatures, and particle strikes to sensitive portions of a circuit. For example, a proton strike on a sensitive node will have a greater effect on a circuit when the supply voltage has dropped by 30 % and temperature has dropped below 0 °C.

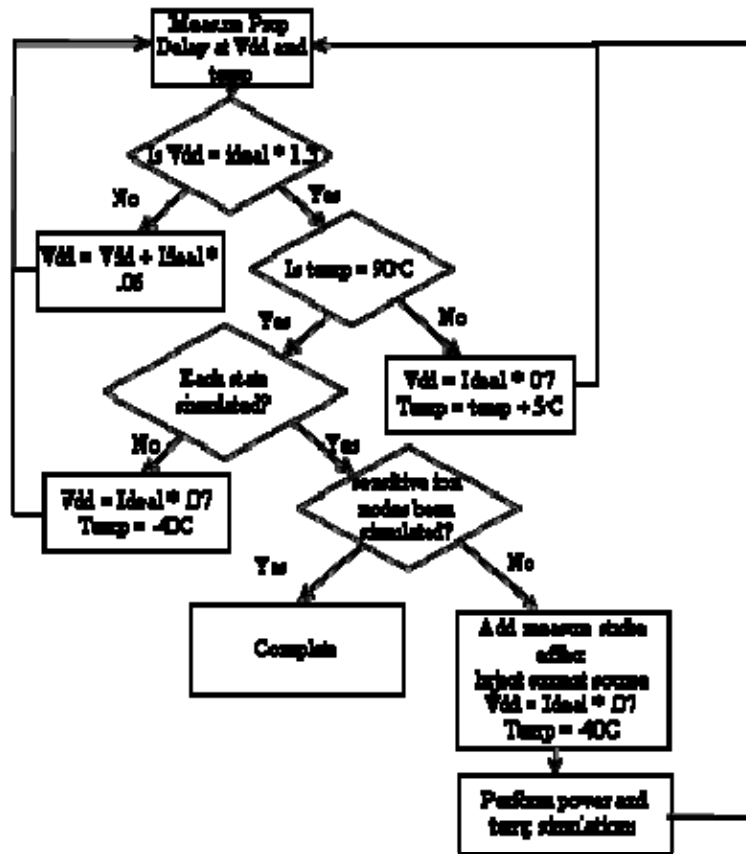


Figure 16. Simulation flow chart.

The developed method first establishes a baseline of operation for the circuits of interest by determining propagation delays for significant transitions at ideal temperature and voltage levels. For the purpose of this work, ideal temperature is considered 25 °C. Ideal voltage is considered 1.5 V for 130 nm, 1.2V for 90 nm, and 1 V for 65 nm feature sizes. The next step is to cycle through each supply voltage level. For the purpose of this work, a voltage range of $\pm 30\%$ was determined to be within the tolerances of popular COTS FPGAs and the possible conditions a microelectronic device in the space environment might be expected to operate under. Now that a baseline effect has been determined for non-ideal supply voltages, simulation across the range of temperatures is

performed. As discussed earlier, microelectronics in the space environment are expected to operate at temperatures between -40 °C and 90 °C. When the performance of the circuit in question has been determined for each temperature at each voltage level, the next step is to simulate a 100 MeV Fe proton strike at critical nodes. If the circuit can tolerate a strike by a iron proton at this energy, the circuit will be able to tolerate all but the most extreme and rare electron, neutron, ion, and proton strikes a electronic device might encounter in LEO or MEO orbits. This technique goes beyond just determining the impacts of a strike on a critical node, by determining the impacts of a strike with both temperature and supply voltage variations. Each sensitive node and state of the circuit is simulated at each supply voltage and each temperature in the range. This method gives a clear picture of any elements performance in the space environment.

3.7 Failure Rate Calculations

To determine the reliability of a microelectronic device in the space environment the number of failures over time is calculated for different common orbits. The generic equation for failure rate of an element in this work is

$$\lambda = \text{flux} \cdot (n_p \cdot \text{area}_p + n_n \cdot \text{area}_n) \cdot N \quad (7)$$

where λ is in failures/s, flux is in protons/(cm⁻²s⁻¹), n_p is the number of sensitive PMOS nodes in a element, area_p is the sensitive area on a PMOS transistor, n_n is the number of sensitive NMOS nodes in a element, area_n is the radiation sensitive area on a NMOS transistor, and N is the number of instances of the element in the circuit. The flux, the number of particles passing through a given area over time, will vary for different orbits.

Calculation of the total reliability is achieved by a summation of the reliabilities of each critical element as seen in the following equation

$$\lambda_{\text{total}} = \lambda_{\text{element1}} + \lambda_{\text{element2}} + \lambda_{\text{element3}} \dots \quad (8)$$

where λ_{element} is the reliability of separate elements.

3.8 Failure Criteria for Critical Elements of FPGA Models

It is possible for each element in a circuit to have separate criteria's for failure. For the specific FPGAs modeled in these simulations, there are only three criteria for failure: propagation delay, bit-flip, and erroneous data propagation time. For temperature and non-ideal supply voltage simulations of combinational logic, propagation delay is the measure used to determine reliability. Propagation delay is compared to values listed in Table 8 to determine effects on reliability. For particle strike simulations, the criterion for failure is the amount of time erroneous data is propagated from the output of the combinational element. These measurements are then compared against the values in Table 8 to determine if a failure state has occurred.

Table 8. Propagation delay criteria for failure of FPGA Models.

FPGA	Virtex II Pro	Virtex 4	Virtex 5
Clock Min PW	0.37 ns	0.28 ns	0.35 ns
Min Setup/Hold	0.21 ns	0.36 ns	0.36 ns

The main criterion for failure in a SRAM device is a 'bit-flip'. This occurs when the stored value permanently changes. If a 'bit-flip' does not occur, the erroneous data

propagation time is measured. This is the time that the wrong value is output from the SRAM cell while it is recovering.

3.9 Architecture Options to Increase Reliability

When a developer designs a circuit, he is in a constant state of dilemma dealing with the engineering decisions or “trade-offs” that must be made to meet different project requirements. This is even more of a factor for microelectronics deployed in the space environment. Due to the expense of replacing a failed circuit, developers design for the highest reliability possible with less regard to cost (both in terms of area and dollars) and performance.

Some common techniques are used to make a circuit more tolerant to particle strikes. The first technique is to resize the transistors of the circuit. By increasing the width of the diffusion area and maintaining the ratio of the PMOS to NMOS, a CMOS circuit will become less sensitive to radiation strikes. This technique was used in simulations, but was limited to an increase of 10 % in the effective width of both the PMOS and NMOS transistors. An increase of greater than 10 % was deemed to be too drastic a cost, and not representative of the technologies of interest to this work. Mark Martin successfully used this method to create a radiation hardened triple mode redundant sense amplifying flip-flop (TMR-SAFF) [24].

Another common technique for use with SRAM cells is to make internal portions redundant [27]. This technique adds two more inverters (double the power and area), see Figure 17, but gives the SRAM cell the ability to recover and most often prevent ‘bit-flips’ caused by particle strikes. In the dual interlocked storage cell (DICE), every

sensitive node is protected by two other nodes. This architecture was only tested to demonstrate functionality of the concept on small feature sizes and was not run through the gambit of simulations the non-hardened circuits were.

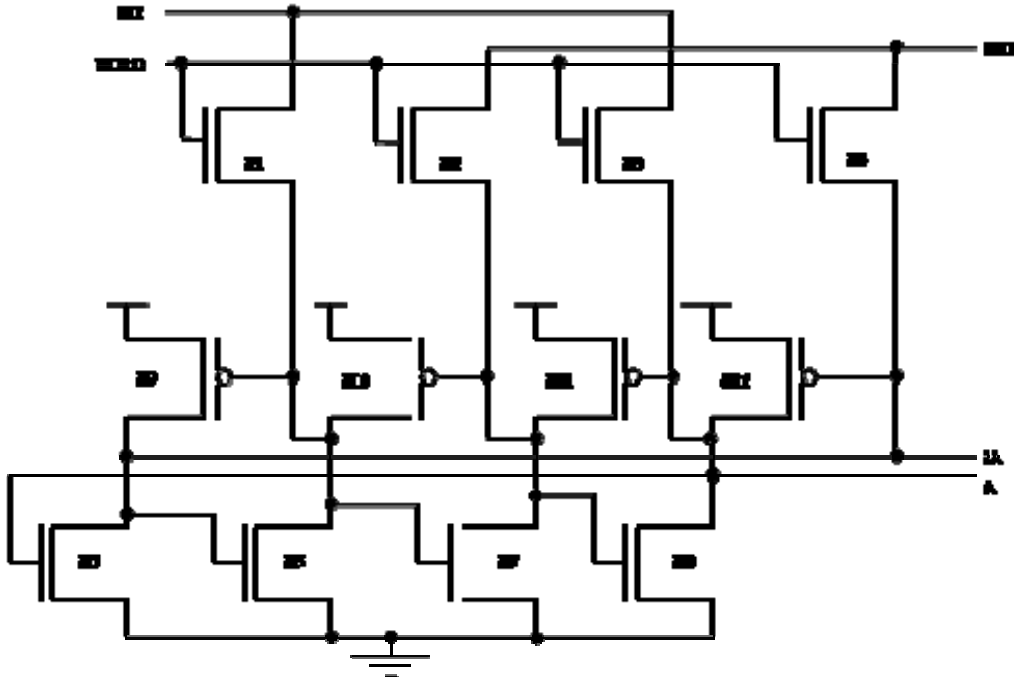


Figure 17. DICE SRAM [27].

IV. Analysis and Results

4.1 Overview

This chapter will cover the following material:

- 1) Performance of critical FPGA elements under temperature and non-ideal voltage simulations,
- 2) Results of particle strike simulations,
- 3) Reliability estimations of COTS FPGAs in the space environment,
- 4) Simulation results of radiation hardened critical FPGA elements,
- 5) A comparison of a COTS hardened and non-hardened FPGA.

4.2 Non-Ideal Temperature and Supply Voltage Simulations

All critical configuration elements were simulated under every combination of temperature and supply voltage. Propagation delay was measured to determine performance under these conditions. Table 9 shows the largest propagation delay measured for each critical element. None of the elements failed according to the criteria for failure listed in Table 8. The worst-case delays were observed during the same conditions for each device, minimum supply voltage and maximum temperature.

Table 9. Maximum propagation delays for temperature and voltage simulations.

Feature Size	NAND	XOR	INV	SRAM
130 nm	38.9 ps	79.6 ps	39.6 ps	42.2 ps
90 nm	39.9 ps	80.1 ps	40.1 ps	50.0 ps
65 nm	42.2 ps	80.3 ps	41.0 ps	50.0 ps

Figure 18 shows the propagation delay increasing with temperature and decreasing with changes in supply voltage for all three versions of the NAND gate with a 1-to-0 transition. This expected trend is seen on each device. Each ‘tooth’ in the graph represents simulations taken at a constant temperature, over the full range of supply voltage levels. Temperature values start at -40 °C, and increase in increments of 5 °C for each ‘tooth’.

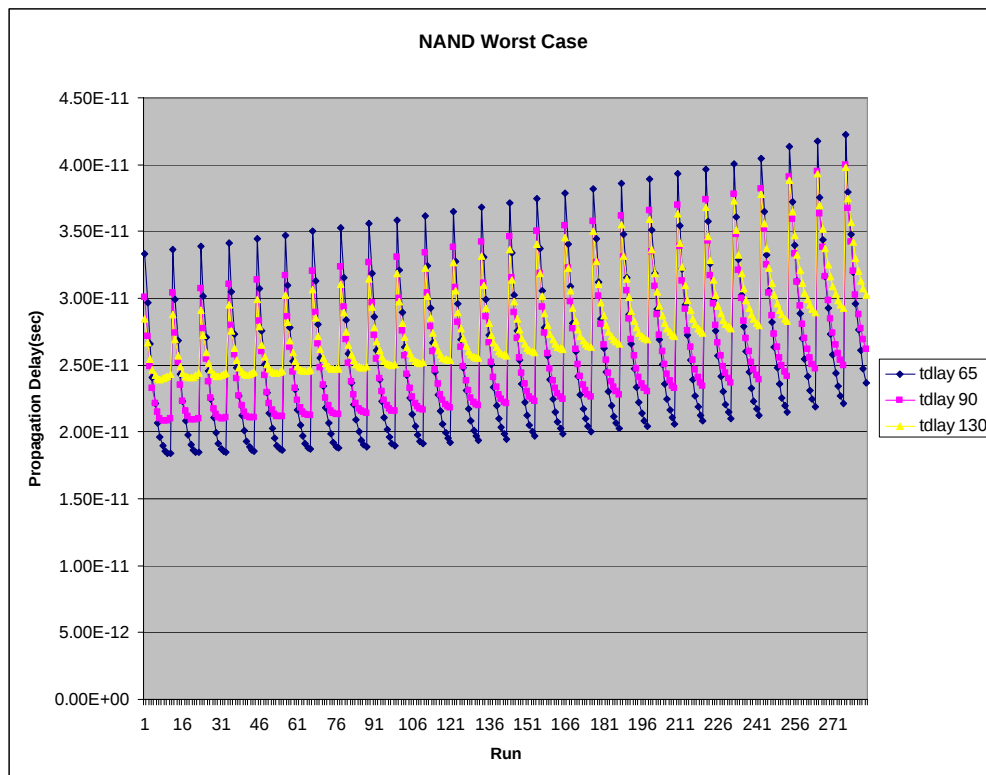


Figure 18. Effect on propagation delay of supply voltage and temperature.

4.3 Particle Strike Simulations

A proton strike with an energy of 100 MeV was simulated using SPICE for all critical elements in the configuration logic of the FPGA models. With the exception of the inverter, simulations of the strike on all the combinational logic elements at all temperature and voltage levels had the same result, failure to meet the manufactures noise tolerances found in Table 8. The largest erroneous data times can be found in Table 10. It is shown that as feature size decreases, the erroneous data propagation times will increase. This demonstrates the reduction of radiation tolerance in smaller feature-sized devices. Simulations on the SRAM cell resulted in a ‘bit-flip’ for every iteration of the simulation.

Table 10. Maximum erroneous propagation times for critical configuration elements.

Feature Size	NAND	XOR	INV	SRAM
130 nm	1.07 ns	1.445 ns	0 ns	Bit-flip
90 nm	1.08 ns	1.519 ns	0 ns	Bit flip
65 nm	1.66 ns	1.782 ns	0 ns	Bit flip

4.4 COTS FPGA Reliability Estimations

Predictions of reliability of the FPGAs modeled were centered on the performance of the configuration structure of the devices. The only non-recoverable failure observed in the configuration structure of the device was the bit-flips of the SRAM elements.

Reliability estimations were calculated using SPICE models, equation (7), and manufactures data from Table 3 and Table 4. The $area_n$ and $area_p$ variables in equation(7) were calculated using parameters extracted from the SPICE NMOS and PMOS models in the following equation

$$area = W_{drain} + 3 \cdot \left(\frac{L}{2} \right) \quad (9)$$

where area is the radiation sensitive area in cm^2 , W_{drain} is the width of the channel, and L is the length of the channel. To determine the depth, common design rules were used from [1] that stated the depth of the drain active area was

$$depth_{drain} = 3 \cdot \lambda \quad (10)$$

where depth is in cm, and λ is half the channel length, L. The number of instances of the SRAM configuration cell in each device is found in the number of configuration bits listed in Table 3 and Table 4.

The first set of reliability estimations, see Table 11, are based on a worst-case orbit at the edge of the trapped proton belt. From the AP-8 model we use a $10^5 m^{-2}s^{-1}$ flux [34]. Since this is the worst case, the following assumptions were integrated with the reliability calculation: proton strikes are evenly distributed across the die and that 100 % of the configuration bits were being used. The results of these calculations showed a massive number of failures per second. This is an unusual set of conditions and is not representative of an average mission.

Table 11. Failure rates for worst case orbit.

Device	Channel Length	Ion Flux	SRAM Sensitive Node Area	Number of Elements	Failure Rate
Virtex II Pro XC2VP2	130 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.608 \mu\text{m}^2$	1,300,000	790 failures/sec
Virtex II Pro XC2VP40	130 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.608 \mu\text{m}^2$	12,000,000	7,301 failures/sec
Virtex II Pro XC2VP100	130 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.608 \mu\text{m}^2$	34,292,768	20,860 failures/sec
Virtex 4 XC4VLX15	90 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.292 \mu\text{m}^2$	5,000,000	1,458 failures/sec
Virtex 4 XC4VSX55	90 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.292 \mu\text{m}^2$	24,000,000	6,998 failures/sec
Virtex 4 XC4VFX140	90 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.292 \mu\text{m}^2$	50,811,136	14,820 failures/sec
Virtex 5 XC5VLX30	65 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.152 \mu\text{m}^2$	8,000,000	1,271 failures/sec
Virtex 5 XC5VLX110T	65 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.152 \mu\text{m}^2$	31,000,000	4,715 failures/sec
Virtex 5 XC5VLX330T	65 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	$0.152 \mu\text{m}^2$	82,696,192	12,580 failures/sec

The next three simulation orbits are considered common. The simulations were performed with more realistic assumptions of proton strike distribution and configuration bit usage. For these calculations, 66% of the particles were assumed to strike the cross section of the device individually. This leads to a reduction of the flux by a third. According to observed data from [40] Virtex FPGAs average usage of configuration bits is 25 % of the total number of configuration bits. Using this observation, the number of sensitive elements in equation (7) was reduced by 75%.

The results of reliability calculations for a LEO is shown in Table 12. The LEO orbit used for this set of calculations was a 400 km circular orbit at an inclination of 51.6%. The LEO polar orbit, results in Table 13, was an 800 km circular orbit at an inclination of 98 %. Seen in Table 14 are the results of the elliptical MEO orbit of 2000 km x 26,570 km at an inclination of 63.4 %. Due to the lower proton flux at LEO orbits described in Chapter 2, the failure rate is reduced. It is shown that the more configuration bits, the higher the failure rate. This data shows that COTS are not reliable in space.

Table 12. LEO failure rate estimations.

Device	Channel Length	Ion Flux	SRAM Sensitive Node Area	Number of Elements	Failure Rate
Virtex II Pro XC2VP2	130 nm	65 ions cm ⁻² s ⁻¹	0.608 μm ²	325,000	0.085 failures/sec
Virtex II Pro XC2VP40	130 nm	65 ions cm ⁻² s ⁻¹	0.608 μm ²	3,000,000	0.783 failures/sec
Virtex II Pro XC2VP100	130 nm	65 ions cm ⁻² s ⁻¹	0.608 μm ²	8,573,192	2.238 failures/sec
Virtex 4 XC4VLX15	90 nm	65 ions cm ⁻² s ⁻¹	0.292 μm ²	1,250,000	0.156 failures/sec
Virtex 4 XC4VSX55	90 nm	65 ions cm ⁻² s ⁻¹	0.292 μm ²	6,000,000	0.751 failures/sec
Virtex 4 XC4VFX140	90 nm	65 ions cm ⁻² s ⁻¹	0.292 μm ²	12,702,784	1.589 failures/sec
Virtex 5 XC5VLX30	65 nm	65 ions cm ⁻² s ⁻¹	0.152 μm ²	2,000,000	0.131 failures/sec
Virtex 5 XC5VLX110T	65 nm	65 ions cm ⁻² s ⁻¹	0.152 μm ²	7,750,000	0.506 failures/sec
Virtex 5 XC5VLX330T	65 nm	65 ions cm ⁻² s ⁻¹	0.152 μm ²	20,674,048	1.349 failures/sec

Table 13. LEO polar failure rate estimations.

Device	Channel Length	Ion Flux	SRAM Sensitive Node Area	Number of Elements	Failure Rate
Virtex II Pro XC2VP2	130 nm	5.3 ions cm ⁻² s ⁻¹	0.608 μm ²	325,000	0.007 failures/sec
Virtex II Pro XC2VP40	130 nm	5.3 ions cm ⁻² s ⁻¹	0.608 μm ²	3,000,000	0.064 failures/sec
Virtex II Pro XC2VP100	130 nm	5.3 ions cm ⁻² s ⁻¹	0.608 μm ²	8,573,192	0.182 failures/sec
Virtex 4 XC4VLX15	90 nm	5.3 ions cm ⁻² s ⁻¹	0.292 μm ²	1,250,000	0.013 failures/sec
Virtex 4 XC4VSX55	90 nm	5.3 ions cm ⁻² s ⁻¹	0.292 μm ²	6,000,000	0.061 failures/sec
Virtex 4 XC4VFX140	90 nm	5.3 ions cm ⁻² s ⁻¹	0.292 μm ²	12,702,784	0.13 failures/sec
Virtex 5 XC5VLX30	65 nm	5.3 ions cm ⁻² s ⁻¹	0.152 μm ²	2,000,000	0.011 failures/sec
Virtex 5 XC5VLX110T	65 nm	5.3 ions cm ⁻² s ⁻¹	0.152 μm ²	7,750,000	0.041 failures/sec
Virtex 5 XC5VLX330T	65 nm	5.3 ions cm ⁻² s ⁻¹	0.152 μm ²	20,674,048	0.11 failures/sec

Table 14. MEO elliptical failure rate estimations.

Device	Channel Length	Ion Flux	SRAM Sensitive Node Area	Number of Elements	Failure Rate
Virtex II Pro XC2VP2	130 nm	290 ions cm ⁻² s ⁻¹	0.608 μm^2	325,000	0.378 failures/sec
Virtex II Pro XC2VP40	130 nm	290 ions cm ⁻² s ⁻¹	0.608 μm^2	3,000,000	3.493 failures/sec
Virtex II Pro XC2VP100	130 nm	290 ions cm ⁻² s ⁻¹	0.608 μm^2	8,573,192	9.983 failures/sec
Virtex 4 XC4VLX15	90 nm	290 ions cm ⁻² s ⁻¹	0.292 μm^2	1,250,000	0.68 failures/sec
Virtex 4 XC4VSX55	90 nm	290 ions cm ⁻² s ⁻¹	0.292 μm^2	6,000,000	3.349 failures/sec
Virtex 4 XC4VFX140	90 nm	290 ions cm ⁻² s ⁻¹	0.292 μm^2	12,702,784	7.09 failures/sec
Virtex 5 XC5VLX30	65 nm	290 ions cm ⁻² s ⁻¹	0.152 μm^2	2,000,000	0.582 failures/sec
Virtex 5 XC5VLX110T	65 nm	290 ions cm ⁻² s ⁻¹	0.152 μm^2	7,750,000	2.256 failures/sec
Virtex 5 XC5VLX330T	65 nm	290 ions cm ⁻² s ⁻¹	0.152 μm^2	20,674,048	6.019 failures/sec

4.5 Implementation of Radiation Hardened Options Results

Functional simulations were performed on two different radiation hardened versions of the configuration SRAM cell with differing results. These simulations were performed using worst-case conditions, high temperature and low voltage, to reduce the number of simulations and determine functionality.

The first option explored was an increase to the width of the transistors. This has been demonstrated in prior works to increase the radiation tolerance of CMOS devices

[8], [24], [27]. Transistors ratios were maintained while manually increasing the widths up to 10 % of their original size. This increase had no effect on the SRAM cell's ability to prevent or recover from a 100 MeV proton strike.

The second option explored was the DICE implementation discussed earlier. This implementation of the SRAM cell was able to quickly recover from radiation strikes with no loss of data. The draw backs to this implementation are twice the power consumption and die area used. With the high number of configuration bits in modern small feature-sized FPGAs, it would be inefficient to utilize this architecture.

4.6 Reliability Comparison of Radiation Hardened Versus COTS FPGA

Xilinx has implemented a radiation hardened FPGA (XCV1000) using older technology to try and reach the military and space electronics market. This FPGA is comparable in performance and structure to the Virtex II Pro XC2VP40 [11], [42]. The main difference that applies to space reliability calculations between the two is the proton strike sensitive cross section. Table 15 lists the parameters used and results for reliability calculations.

Table 15. XCV1000 failure rates for different common orbits.

Orbit	Channel Length	Ion Flux	Cross section	Number of Elements	Failure Rate
Worst Case	220 nm	10^5 ions $\text{cm}^{-2}\text{s}^{-1}$	2.2×10^{-14} cm^2	1,532,000	0.0034 failures/sec
LEO	220 nm	65 ions $\text{cm}^{-2}\text{s}^{-1}$	2.2×10^{-14} cm^2	1,532,000	2.2×10^{-6} failures/sec
LEO Polar	220 nm	5.3 ions $\text{cm}^{-2}\text{s}^{-1}$	2.2×10^{-14} cm^2	1,532,000	1.7×10^{-7} failures/sec
MEO elliptical	220 nm	290 ions $\text{cm}^{-2}\text{s}^{-1}$	2.2×10^{-14} cm^2	1,532,000	9.7×10^{-6} failures/sec

Figure 19 is a comparison of the failure rates for these two FPGAs at different orbits. The reliability difference is extreme, up to six orders of magnitude. Another point the graph makes, is that even the radiation hardened FPGA will have significant failure rates under worst-case conditions.

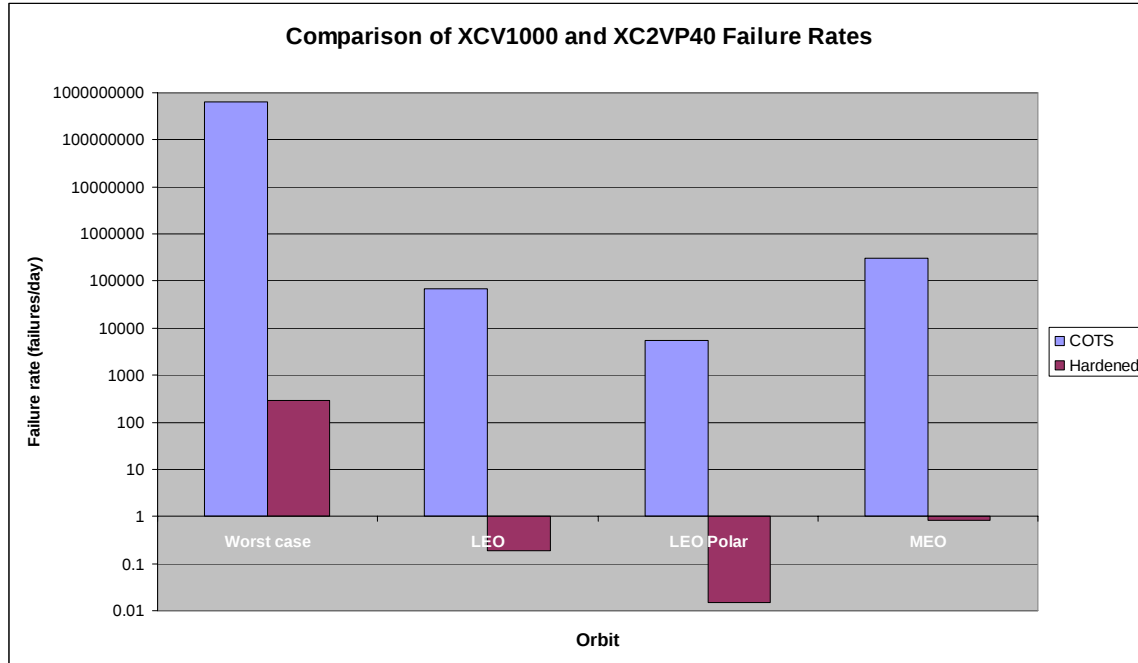


Figure 19. Comparison of COTS hardened and non-hardened FPGAs failure rates.

Table 16 shows the comparison of failure rates for three different COTS FPGAs. The first two, XCV1000 and XC2VP40, failure rates were calculated using the method described in this work. The failure rates for the XQVR300 are the results for two common orbits from lab experimentation [40]. The results of the two radiation hardened versions are similar, but differ due to assumptions in the failure rate calculations. The published failure rates listed assume all configuration bits are being used with ideal temperature and voltage levels. The published results also use the CHIME space

radiation model, as compared to this work using the AP-8 space radiation model. This skews the data slightly, with only a minimal difference in failure rates for the two radiation hardened FPGAs.

Table 16. Experimental failure rates versus simulated for LEO and MEO.

	XC2VP40	XCV1000	XQVR300
Orbit	Failures/Day	Failures/Day	Failures/Day
LEO	293,760	0.19	2.05
MEO	67,651	0.838	2.35

V. Conclusions and Recommendations

5.1 Overview

This chapter contains the following:

- 1) Conclusions of the research,
- 2) A discussion on future works.

5.2 Conclusions of Research

The ability to efficiently characterize a system's reliability is of paramount importance prior to deployment into the space environment. To determine this reliability, key components must be identified and tested. This methodology was migrated to the microelectronics level to provide designers a simple and efficient early reliability determination. Characterization of the space environment was shown to have three major factors that can cause non-recoverable effects in microelectronics: non-ideal power, environmental temperature, and particle strikes. A simulation technique that used common tools was developed to submit determined critical portions of a circuit to expected operating conditions when deployed in the space environment. The failure rate results were similar to those obtained through previous experimental testing [40]. Utilizing these techniques allows a developer to repair problem areas or readdress design limits prior to fabrication of the device.

These techniques were demonstrated by determining the reliability of a modern COTS FPGA in the space environment. After critical portions of the FPGAs were identified, models were generated of these portions using standard to cutting edge technologies. These critical portions were then submitted to a battery of conditions and

effects that represent the space environment. The results of the simulations were as expected. All three versions of the FPGA we deemed unreliable due to the configuration SRAM failing all conditions for a worst-case particle strike.

Some of the modifications to the generic SRAM cells used showed increased reliability. Implementation of the DICE architecture showed a 100% tolerance to particle strikes at sensitive areas while in a static state. The cost/benefit analysis of doubling both power and footprint of the circuit element must be considered before this can be considered a viable alternative architecture. It was proposed and tested that modifying the effective widths of the sensitive transistors in the SRAM would lead to greater particle strike tolerance. Simulation results still gave a 100% failure rate for SRAM cells with the increased widths.

5.3 Recommendations for Future Research

The research and techniques discussed in this work are the building blocks for many other avenues of research in to FPGA reliability in the space environment. New tools are available to expand the simulation technique to from SPICE to three-dimensional simulations utilizing Technology Computer Aided Design (TCAD). This tool will allow the researcher to build simulated data for analysis to include radiation strikes from multiple incident angles. This will be a more representative simulation of the space environment, and not just the worst-case simulations performed by SPICE.

With the data obtained using these simulations a full logic block can be built and tested. This will allow for the development of radiation hardened circuits that are proven prior to tape-out. With a proven design, future researchers will be able to fabricate their

circuit and submit the circuit to physical tests that will demonstrate the effectiveness of the simulation techniques.

Slight modifications of the radiation characterization will allow future researchers to expand the scope of simulations. Anti-tampering researchers will have the ability to test the tolerance of key portions of an FPGA to common reverse engineering techniques. This will allow the fabrication of a more secure processing device for military applications. The researchers will first need to characterize the methods used to stimulate transistors, then apply this characterization to the simulation technique.

Further modifications can determine hardness in terms of electronic warfare. Researchers can characterize the environment to determine the reliability of designed FPGAs to possible wartime conditions. This will give the war-fighter consistent and reliable processing for many applications.

Appendix A SPICE 130 nm Transistor Models

* 130nm NMOS

```
.model nmos nmos level = 54
+version = 4.0  binunit = 1  paramchk = 1  mobmod = 0
+capmod = 2  igcmod = 1  igbmod = 1  geomod = 1
+diomod = 1  rdsmod = 0  rbodmod = 1  rgatemod = 1
+permod = 1  acnqsmode = 0  trnqsmode = 0
* parameters related to the technology node
+tnom = 27  epsrox = 3.9
+eta0 = 0.0092  nfactor = 1.5  wint = 5e-09
+cgso = 2.4e-10  cgdo = 2.4e-10  xl = -6e-08
* parameters customized by the user
+toxe = 2.25e-09  toxp = 1.6e-09  toxm = 2.25e-09  toxref = 2.25e-09
+dtox = 6.5e-10  lint = 1.05e-08
+vth0 = 0.4  k1 = 0.485  u0 = 0.05767  vsat = 100370
+rdsw = 200  ndep = 1.67e+18  xj = 3.92e-08
* secondary parameters
+ll = 0  wl = 0  lln = 1  wln = 1
+lw = 0  ww = 0  lwn = 1  wwn = 1
+lw1 = 0  ww1 = 0  xpart = 0
+k2 = 0.01  k3 = 0
+k3b = 0  w0 = 2.5e-006  dvt0 = 1  dvt1 = 2
+dvt2 = -0.032  dvt0w = 0  dvt1w = 0  dvt2w = 0
+dsub = 0.1  minv = 0.05  voffl = 0  dvtp0 = 1.0e-009
+dvtp1 = 0.1  lpe0 = 0  lpeb = 0
+ngate = 2e+020  nsd = 2e+020  phin = 0
+cdsc = 0.000  cdsb = 0  cdsd = 0  cit = 0
+voff = -0.13  etab = 0
+vfb = -0.55  ua = 6e-010  ub = 1.2e-018
+uc = 0  a0 = 1.0  ags = 1e-020
+a1 = 0  a2 = 1.0  b0 = 0  b1 = 0
+keta = 0.04  dwg = 0  dwb = 0  pclm = 0.04
+pdiblc1 = 0.001  pdiblc2 = 0.001  pdiblc3 = -0.005  drout = 0.5
+pvag = 1e-020  delta = 0.01  pscbe1 = 8.14e+008  pscbe2 = 1e-007
+fprou = 0.2  pdits = 0.08  pditsd = 0.23  pditsl = 2.3e+006
+rsh = 5  rsw = 85  rdw = 85
+rdswmin = 0  rdwmin = 0  rswmin = 0  prwg = 0
+prwb = 6.8e-011  wr = 1  alpha0 = 0.074  alpha1 = 0.005
+beta0 = 30  agidl = 0.0002  bgidl = 2.1e+009  cgidl = 0.0002
+egidl = 0.8
+aigbacc = 0.012  bigbacc = 0.0028  cigbacc = 0.002
+nigbacc = 1  aigbinv = 0.014  bigbinv = 0.004  cigbinv = 0.004
+eigbinv = 1.1  nigbinv = 3  aigc = 0.012  bigc = 0.0028
+cigc = 0.002  aigsd = 0.012  bigsd = 0.0028  cigsd = 0.002
+nigc = 1  poxedg = 1  pigcd = 1  ntox = 1
+xrcrg1 = 12  xrcrg2 = 5
+cgbo = 2.56e-011  cgdl = 2.653e-10
+cgs1 = 2.653e-10  ckappas = 0.03  ckappad = 0.03  acde = 1
+moin = 15  noff = 0.9  voffcv = 0.02
+kt1 = -0.11  kt1l = 0  kt2 = 0.022  ute = -1.5
+ual = 4.31e-009  ub1 = 7.61e-018  uc1 = -5.6e-011  prt = 0
+at = 33000
+fnoimod = 1  tnoimod = 0
```

```

+jss = 0.0001   jsws = 1e-011   jswgs = 1e-010   njs = 1
+ijthsfwd= 0.01   ijthrev= 0.001   bvs = 10   xjbvs = 1
+jsd = 0.0001   jswd = 1e-011   jswgd = 1e-010   njd = 1
+ijthdfwd= 0.01   ijthdrev= 0.001   bvd = 10   xjbvd = 1
+pbs = 1   cjs = 0.0005   mjs = 0.5   pbsws = 1
+cjsws = 5e-010   mjsws = 0.33   pbswgs = 1   cjswgs = 3e-010
+mjswgs = 0.33   pbd = 1   cjd = 0.0005   mjd = 0.5
+pbswd = 1   cjswd = 5e-010   mjswd = 0.33   pbswgd = 1
+cjswgd = 5e-010   mjswgd = 0.33   tpb = 0.005   tcj = 0.001
+tpbsw = 0.005   tcjsw = 0.001   tpbswg = 0.005   tcjswg = 0.001
+xtis = 3   xtid = 3
+dmcg = 0e-006   dmci = 0e-006   dmdg = 0e-006   dmegt = 0e-007
+dwj = 0.0e-008   xgw = 0e-007   xgl = 0e-008
+rshg = 0.4   gbmin = 1e-010   rbpb = 5   rbpd = 15
+rbps = 15   rbdb = 15   rbsb = 15   ngcon = 1

```

* Customized 130nm PMOS

```
.model pmos pmos level = 54
```

```

+version = 4.0   binunit = 1   paramchk = 1   mobmod = 0
+capmod = 2   igcmmod = 1   igbmod = 1   geomod = 1
+diomod = 1   rdsmod = 0   rbodmod = 1   rgatemod = 1
+permod = 1   acnqsmode = 0   trnqsmode = 0
* parameters related to the technology node
+tnom = 27   epsrox = 3.9
+eta0 = 0.0092   nfactor = 1.5   wint = 5e-09
+cgso = 2.4e-10   cgdo = 2.4e-10   xl = -6e-08
* parameters customized by the user
+toxe = 2.35e-09   toxp = 1.6e-09   toxm = 2.35e-09   toxref = 2.35e-09
+dtox = 7.5e-10   lint = 1.05e-08
+vth0 = -0.349   k1 = 0.443   u0 = 0.0077   vsat = 70000
+rdsw = 240   ndep = 1.28e+18   xj = 3.92e-08
*secondary parameters
+ll = 0   wl = 0   lln = 1   wln = 1
+lw = 0   ww = 0   lwn = 1   wwn = 1
+lw1 = 0   ww1 = 0   xpart = 0
+k2 = -0.01   k3 = 0
+k3b = 0   w0 = 2.5e-006   dvt0 = 1   dvt1 = 2
+dvt2 = -0.032   dvt0w = 0   dvt1w = 0   dvt2w = 0
+dsb = 0.1   minv = 0.05   voffl = 0   dvtp0 = 1e-009
+dvtp1 = 0.05   lpe0 = 0   lpeb = 0
+ngate = 2e+020   nsd = 2e+020   phin = 0
+cdsc = 0.000   cdsb = 0   cdsd = 0   cit = 0
+voff = -0.126   etab = 0
+vfb = 0.55   ua = 2.0e-009   ub = 0.5e-018
+uc = 0   a0 = 1.0   ags = 1e-020
+a1 = 0   a2 = 1   b0 = -1e-020   b1 = 0
+keta = -0.047   dwg = 0   dwb = 0   pclm = 0.12
+pdibl1 = 0.001   pdibl2 = 0.001   pdiblc3 = 3.4e-008   drout = 0.56
+pvag = 1e-020   delta = 0.01   pscbe1 = 8.14e+008   pscbe2 = 9.58e-007
+fprout = 0.2   pdits = 0.08   pditsd = 0.23   pditsl = 2.3e+006
+rsh = 5   rsw = 85   rdw = 85
+rdswmin = 0   rdwmin = 0   rswmin = 0   prwg = 3.22e-008

```

```

+prwb = 6.8e-011  wr = 1      alpha0 = 0.074  alpha1 = 0.005
+beta0 = 30      agidl = 0.0002  bgidl = 2.1e+009  cgidl = 0.0002
+egidl = 0.8
+aigbacc = 0.012  bigbacc = 0.0028  cigbacc = 0.002
+nigbacc = 1      aigbinv = 0.014  bigbinv = 0.004  cigbinv = 0.004
+eigbinv = 1.1    nigbinv = 3      aigc = 0.69    bigc = 0.0012
+cigc = 0.0008    aigsd = 0.0087  bigsd = 0.0012  cigsd = 0.0008
+nigc = 1         poxedg = 1      pigcd = 1      ntox = 1
+xrcrg1 = 12      xrcrg2 = 5
+cgbo = 2.56e-011  cgd1 = 2.653e-10
+cgs1 = 2.653e-10  ckappas = 0.03  ckappad = 0.03  acde = 1
+moin = 15        noff = 0.9      voffcv = 0.02
+kt1 = -0.11      kt11 = 0        kt2 = 0.022    ute = -1.5
+ual = 4.31e-009  ub1 = 7.61e-018  uc1 = -5.6e-011  prt = 0
+at = 33000
+fnoimod = 1      tnoimod = 0
+jss = 0.0001     jsws = 1e-011   jswgs = 1e-010  njs = 1
+ijthsfwd = 0.01  ijthsrev = 0.001  bvs = 10      xjbvs = 1
+jsd = 0.0001     jswd = 1e-011   jswgd = 1e-010  njd = 1
+ijthdfwd = 0.01  ijthdrev = 0.001  bvd = 10      xjbvd = 1
+pbs = 1          cjs = 0.0005    mjs = 0.5      pbsws = 1
+cjsws = 5e-010   mjsws = 0.33     pbswgs = 1      cjswgs = 3e-010
+mjswgs = 0.33    pbd = 1          cjd = 0.0005    mjd = 0.5
+pbswd = 1        cjswd = 5e-010   mjswd = 0.33     pbswgd = 1
+cjswgd = 5e-010  mjswgd = 0.33    tpb = 0.005     tcj = 0.001
+tpbsw = 0.005    tcjsw = 0.001    tpbswg = 0.005   tcjswg = 0.001
+xtis = 3         xt1d = 3
+dmcg = 0e-006    dmci = 0e-006    dmdg = 0e-006    dmcgt = 0e-007
+dwj = 0.0e-008   xgw = 0e-007     xgl = 0e-008
+rshg = 0.4        gbmin = 1e-010   rbpb = 5         rbpd = 15
+rbps = 15         rbdb = 15        rbsb = 15        ngcon = 1

```

Appendix B SPICE 90 nm Transistor Models

* Customized 90nm NMOS

```
.model nmos nmos level = 54
```

```
+version = 4.0  binunit = 1  paramchk = 1  mobmod = 0
+capmod = 2    igcmod = 1  igbmod = 1  geomod = 1
+diomod = 1    rdsmod = 0  rbodymod = 1  rgatemod = 1
+permod = 1    acnqsmode = 0  trnqsmode = 0
* parameters related to the technology node
+tnom = 27  epsrox = 3.9
+eta0 = 0.0074  nfactor = 1.7  wint = 5e-09
+cgso = 1.9e-10  cgdo = 1.9e-10  xl = -4e-08
* parameters customized by the user
+toxe = 2.05e-09  toxp = 1.4e-09  toxm = 2.05e-09  toxref = 2.05e-09
+dtox = 6.5e-10  lint = 7.5e-09
+vth0 = 0.408  k1 = 0.486  u0 = 0.05383  vsat = 113760
+rdsw = 180  ndep = 2.02e+18  xj = 2.8e-08
* secondary parameters
+ll  = 0  wl  = 0  lln  = 1  wln  = 1
+lw  = 0  ww  = 0  lwn  = 1  wwn  = 1
+lw1 = 0  ww1 = 0  xpart = 0
+k2  = 0.01  k3  = 0
+k3b = 0  w0  = 2.5e-006  dvt0 = 1  dvt1 = 2
+dvt2 = -0.032  dvt0w = 0  dvt1w = 0  dvt2w = 0
+dsb  = 0.1  minv = 0.05  voffl = 0  dvtp0 = 1.0e-009
+dvtp1 = 0.1  lpe0 = 0  lpeb = 0
+ngate = 2e+020  nsd = 2e+020  phin = 0
+cdsc = 0.000  cdsb = 0  cdsd = 0  cit = 0
+voff = -0.13  etab = 0
+vfb = -0.55  ua  = 6e-010  ub  = 1.2e-018
+uc  = 0  a0  = 1.0  ags  = 1e-020
+a1  = 0  a2  = 1.0  b0  = 0  b1  = 0
+keta = 0.04  dwg = 0  dwb = 0  pclm = 0.04
+pdibl1 = 0.001  pdibl2 = 0.001  pdiblc3 = -0.005  drout = 0.5
+pvag = 1e-020  delta = 0.01  pscbe1 = 8.14e+008  pscbe2 = 1e-007
+fprout = 0.2  pdits = 0.08  pditsd = 0.23  pditsl = 2.3e+006
+rsh = 5  rsw = 85  rdw = 85
+rdswmin = 0  rdwmin = 0  rswmin = 0  prwg = 0
+prwb = 6.8e-011  wr = 1  alpha0 = 0.074  alpha1 = 0.005
+beta0 = 30  agidl = 0.0002  bgidl = 2.1e+009  cgidl = 0.0002
+egidl = 0.8
+aigbacc = 0.012  bigbacc = 0.0028  cigbacc = 0.002
+nigbacc = 1  aigbinv = 0.014  bigbinv = 0.004  cigbinv = 0.004
+eigbinv = 1.1  nigbinv = 3  aigc = 0.012  bigc = 0.0028
+cigc = 0.002  aigsd = 0.012  bigsd = 0.0028  cigsd = 0.002
+nigc = 1  poxedg = 1  pigcd = 1  ntox = 1
+xrcrg1 = 12  xrcrg2 = 5
+cgbo = 2.56e-011  cgdl = 2.653e-10
+cgs1 = 2.653e-10  ckappas = 0.03  ckappad = 0.03  acde = 1
+moin = 15  noff = 0.9  voffcv = 0.02
+kt1 = -0.11  kt1l = 0  kt2 = 0.022  ute = -1.5
```

```

+ual = 4.31e-009 ub1 = 7.61e-018 uc1 = -5.6e-011 prt = 0
+at = 33000
+fnoimod = 1 tnoimod = 0
+jss = 0.0001 jsws = 1e-011 jswgs = 1e-010 njs = 1
+ijthsfwd= 0.01 ijthsrev= 0.001 bvs = 10 xjbvs = 1
+jsd = 0.0001 jswd = 1e-011 jswgd = 1e-010 njd = 1
+ijthdfwd= 0.01 ijthdrev= 0.001 bvd = 10 xjbvd = 1
+pbs = 1 cjs = 0.0005 mjs = 0.5 pbsws = 1
+cjsws = 5e-010 mjsws = 0.33 pbswgs = 1 cjswgs = 3e-010
+mjswgs = 0.33 pbd = 1 cjd = 0.0005 mjd = 0.5
+pbswd = 1 cjswd = 5e-010 mjswd = 0.33 pbswgd = 1
+cjswgd = 5e-010 mjswgd = 0.33 tpb = 0.005 tcj = 0.001
+tpbsw = 0.005 tcjsw = 0.001 tpbswg = 0.005 tcjswg = 0.001
+xtis = 3 xtid = 3
+dmcg = 0e-006 dmci = 0e-006 dmdg = 0e-006 dmcgt = 0e-007
+dwj = 0.0e-008 xgw = 0e-007 xgl = 0e-008
+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15
+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

```

* Customized PTM 90nm PMOS

```
.model pmos pmos level = 54
```

```

+version = 4.0 binunit = 1 paramchk = 1 mobmod = 0
+capmod = 2 igcmmod = 1 igbmod = 1 geomod = 1
+diomod = 1 rdsmod = 0 rbodmod = 1 rgatemod = 1
+permod = 1 acnqsmode = 0 trnqsmode = 0
* parameters related to the technology node
+tnom = 27 epsrox = 3.9
+eta0 = 0.0074 nfactor = 1.7 wint = 5e-09
+cgso = 1.9e-10 cgdo = 1.9e-10 xl = -4e-08
* parameters customized by the user
+toxe = 2.15e-09 toxp = 1.4e-09 toxm = 2.15e-09 toxref = 2.15e-09
+dtox = 7.5e-10 lint = 7.5e-09
+vth0 = -0.356 k1 = 0.443 u0 = 0.00675 vsat = 70000
+rdsw = 200 ndep = 1.53e+18 xj = 2.8e-08
*secondary parameters
+ll = 0 wl = 0 llm = 1 wlm = 1
+lw = 0 ww = 0 lwm = 1 wwm = 1
+lw1 = 0 ww1 = 0 xpart = 0
+k2 = -0.01 k3 = 0
+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2
+dvt2 = -0.032 dvt0w = 0 dvt1w = 0 dvt2w = 0
+dsub = 0.1 minv = 0.05 voffl = 0 dvtp0 = 1e-009
+dvtp1 = 0.05 lpe0 = 0 lpeb = 0
+ngate = 2e+020 nsd = 2e+020 phin = 0
+cdsc = 0.000 cdscb = 0 cdsd = 0 cit = 0
+voff = -0.126 etab = 0
+vfb = 0.55 ua = 2.0e-009 ub = 0.5e-018
+uc = 0 a0 = 1.0 ags = 1e-020
+a1 = 0 a2 = 1 b0 = -1e-020 b1 = 0
+keta = -0.047 dwg = 0 dwb = 0 pclm = 0.12
+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblc3 = 3.4e-008 dROUT = 0.56
+pvag = 1e-020 delta = 0.01 pscbe1 = 8.14e+008 pscbe2 = 9.58e-007

```

```

+fprou = 0.2      pdits = 0.08      pditsd = 0.23      pditsl = 2.3e+006
+rsh = 5          rsw = 85          rdw = 85
+rdswmin = 0      rdwmin = 0        rswmin = 0        prwg = 3.22e-008
+prwb = 6.8e-011  wr = 1          alpha0 = 0.074    alpha1 = 0.005
+beta0 = 30       agidl = 0.0002    bgidl = 2.1e+009  cgidl = 0.0002
+egidl = 0.8
+aigbacc = 0.012   bigbacc = 0.0028   cigbacc = 0.002
+nigbacc = 1       aigbinv = 0.014    bigbinv = 0.004   cigbinv = 0.004
+eigbinv = 1.1     nigbinv = 3        aigc = 0.69       bigc = 0.0012
+cigc = 0.0008     aigsd = 0.0087       bigsd = 0.0012    cigsd = 0.0008
+nigc = 1          poxedge = 1        pigcd = 1         ntox = 1
+xrcrg1 = 12       xrcrg2 = 5
+cgbo = 2.56e-011  cgdl = 2.653e-10
+cgs1 = 2.653e-10  ckappas = 0.03       ckappad = 0.03    acde = 1
+moin = 15         noff = 0.9        voffcv = 0.02
+kt1 = -0.11       kt1l = 0            kt2 = 0.022       ute = -1.5
+ual = 4.31e-009   ub1 = 7.61e-018     uc1 = -5.6e-011   prt = 0
+at = 33000
+fnoimod = 1       tnoimod = 0
+jss = 0.0001      jsws = 1e-011        jswgs = 1e-010    njs = 1
+ijthsfdw = 0.01   ijthsrev = 0.001     bvs = 10          xjbvs = 1
+jsd = 0.0001      jswd = 1e-011        jswgd = 1e-010    njd = 1
+ijthdfwd = 0.01   ijthdrev = 0.001     bvd = 10          xjbvd = 1
+pbs = 1           cjs = 0.0005         mjs = 0.5          pbsws = 1
+cjsws = 5e-010    mjsws = 0.33         pbswgs = 1         cjswgs = 3e-010
+mjswgs = 0.33     pbd = 1             cjd = 0.0005       mjd = 0.5
+pbswd = 1         cjswd = 5e-010       mjswd = 0.33       pbswgd = 1
+cjswgd = 5e-010   mjswgd = 0.33        tpb = 0.005        tcj = 0.001
+tpbsw = 0.005     tcjsw = 0.001        tpbswg = 0.005     tcjswg = 0.001
+xtis = 3          xtid = 3
+dmcg = 0e-006     dmci = 0e-006        dmdg = 0e-006     dmcgt = 0e-007
+dwj = 0.0e-008    xgw = 0e-007         xgl = 0e-008
+rshg = 0.4        gbmin = 1e-010       rbpb = 5          rbpd = 15         +rbps = 15         rbdb = 15
rbsb = 15         ngcon = 1

```

Appendix C SPICE 65 nm Transistor Models

* Customized PTM 65nm NMOS

```
.model nmos nmos level = 54
```

```
+version = 4.0  binunit = 1  paramchk = 1  mobmod = 0
+capmod = 2    igcmod = 1  igbmod = 1  geomod = 1
+diomod = 1    rdsmod = 0  rbodmod = 1  rgatmod = 1
+permod = 1    acnqsmode = 0  trnqsmode = 0
```

* parameters related to the technology node

```
+tnom = 27  epsrox = 3.9
+eta0 = 0.0058  nfactor = 1.9  wint = 5e-09
+cgso = 1.5e-10  cgdo = 1.5e-10  xl = -3e-08
```

* parameters customized by the user

```
+toxe = 1.85e-09  toxp = 1.2e-09  toxm = 1.85e-09  toxref = 1.85e-09
+dtox = 6.5e-10  lint = 5.25e-09
+vth0 = 0.419  k1 = 0.489  u0 = 0.04934  vsat = 124340
+rdsw = 165  ndep = 2.51e+18  xj = 1.96e-08
```

* secondary parameters

```
+ll = 0  wl = 0  lln = 1  wln = 1
+lw = 0  ww = 0  lwn = 1  wwn = 1
+lw1 = 0  ww1 = 0  xpart = 0
+k2 = 0.01  k3 = 0
+k3b = 0  w0 = 2.5e-006  dvt0 = 1  dvt1 = 2
+dvt2 = -0.032  dvt0w = 0  dvt1w = 0  dvt2w = 0
+dsub = 0.1  minv = 0.05  voffl = 0  dvtp0 = 1.0e-009
+dvtp1 = 0.1  lpe0 = 0  lpeb = 0
+ngate = 2e+020  nsd = 2e+020  phin = 0
+cdsc = 0.000  cdsb = 0  cdsd = 0  cit = 0
+voff = -0.13  etab = 0
+vfb = -0.55  ua = 6e-010  ub = 1.2e-018
+uc = 0  a0 = 1.0  ags = 1e-020
+a1 = 0  a2 = 1.0  b0 = 0  b1 = 0
+keta = 0.04  dwg = 0  dwb = 0  pclm = 0.04
+pdibl1 = 0.001  pdibl2 = 0.001  pdiblc = -0.005  drout = 0.5
+pvag = 1e-020  delta = 0.01  pscbe1 = 8.14e+008  pscbe2 = 1e-007
+fprout = 0.2  pdits = 0.08  pditsd = 0.23  pditsl = 2.3e+006
+rsh = 5  rsw = 85  rdw = 85
+rdswmin = 0  rdwmin = 0  rswmin = 0  prwg = 0
+prwb = 6.8e-011  wr = 1  alpha0 = 0.074  alpha1 = 0.005
+beta0 = 30  agidl = 0.0002  bgidl = 2.1e+009  cgidl = 0.0002
+egidl = 0.8
```

```
+aigbacc = 0.012  bigbacc = 0.0028  cigbacc = 0.002
+nigbacc = 1  aigbinv = 0.014  bigbinv = 0.004  cigbinv = 0.004
+eigbinv = 1.1  nigbinv = 3  aigc = 0.012  bigc = 0.0028
+cigc = 0.002  aigsd = 0.012  bigsd = 0.0028  cigsd = 0.002
+nigc = 1  poxedg = 1  pigcd = 1  ntox = 1
```

```

+xrcrg1 = 12      xrcrg2 = 5
+cgbo = 2.56e-011  cgd1 = 2.653e-10
+cgsl = 2.653e-10  ckappas = 0.03      ckappad = 0.03      acde = 1
+moin = 15        noff = 0.9          voffcv = 0.02

+kt1 = -0.11      kt1l = 0           kt2 = 0.022      ute = -1.5
+ual = 4.31e-009  ub1 = 7.61e-018    uc1 = -5.6e-011  prt = 0
+at = 33000

+fnoimod = 1      tnoimod = 0

+jss = 0.0001     jsws = 1e-011      jswgs = 1e-010    njs = 1
+ijthsfwd=0.01    ijthsrev=0.001     bvs = 10          xjbvs = 1
+jsd = 0.0001     jswd = 1e-011      jswgd = 1e-010    njd = 1
+ijthdfwd=0.01    ijthdrev=0.001     bvd = 10          xjbvd = 1
+pbs = 1          cjs = 0.0005     mjs = 0.5         pbsws = 1
+cjsws = 5e-010   mjsws = 0.33       pbswgs = 1        cjswgs = 3e-010
+mjswgs = 0.33    pbd = 1           cjd = 0.0005      mjd = 0.5
+pbswd = 1        cjswd = 5e-010     mjswd = 0.33      pbswgd = 1
+cjswgd = 5e-010  mjswgd = 0.33      tpb = 0.005        tcj = 0.001
+tpbsw = 0.005    tcjsw = 0.001      tpbswg = 0.005     tcjswg = 0.001
+xtis = 3         xtld = 3

+dmcg = 0e-006    dmci = 0e-006      dmdg = 0e-006     dmegt = 0e-007
+dwj = 0.0e-008   xgw = 0e-007       xgl = 0e-008

+rshg = 0.4       gbmin = 1e-010     rbpb = 5          rbpd = 15
+rbps = 15        rbdb = 15          rbsb = 15         ngcon = 1

* Customized PTM 65nm PMOS

.model pmos pmos level = 54

+version = 4.0    binunit = 1    paramchk = 1    mobmod = 0
+capmod = 2      igcmmod = 1    igbmod = 1      geomod = 1
+diomod = 1      rdsmod = 0    rbodymod = 1    rgatemod = 1
+permod = 1      acnqsmode = 0    trnqsmode = 0

* parameters related to the technology node
+tnom = 27      epsrox = 3.9
+eta0 = 0.0058   nfactor = 1.9    wint = 5e-09
+cgso = 1.5e-10  cgdo = 1.5e-10    xl = -3e-08

* parameters customized by the user
+toxe = 1.95e-09  toxp = 1.2e-09    toxm = 1.95e-09  toxref = 1.95e-09
+dtox = 7.5e-10  lint = 5.25e-09
+vth0 = -0.367   k1 = 0.447        u0 = 0.00568     vsat = 70000
+rdsw = 170      ndep = 1.89e+18  xj = 1.96e-08

*secondary parameters
+ll = 0          wl = 0          lln = 1          wln = 1
+lw = 0          ww = 0          lwn = 1          wwn = 1
+lw1 = 0         ww1 = 0         xpart = 0
+k2 = -0.01      k3 = 0

```

```

+k3b  = 0      w0   = 2.5e-006   dvt0  = 1      dvt1  = 2
+dvt2  = -0.032  dvt0w = 0      dvt1w = 0      dvt2w = 0
+dsb   = 0.1     minv  = 0.05     voffl  = 0      dvtp0  = 1e-009
+dvtp1 = 0.05     lpe0  = 0      lpeb   = 0
+ngate  = 2e+020   nsd   = 2e+020   phin   = 0
+cdsc   = 0.000    cdsb  = 0      cdsd   = 0      cit    = 0
+voff   = -0.126   etab  = 0
+vfb    = 0.55     ua    = 2.0e-009   ub     = 0.5e-018
+uc     = 0        a0    = 1.0      ags    = 1e-020
+a1     = 0        a2    = 1        b0     = -1e-020   b1     = 0
+keta   = -0.047   dwg   = 0        dwb    = 0        pclm   = 0.12
+pdibl1 = 0.001    pdibl2 = 0.001   pdiblc = 3.4e-008   drout  = 0.56
+pvag   = 1e-020   delta  = 0.01     pscbe1 = 8.14e+008   pscbe2 = 9.58e-007
+fprout = 0.2      pdits  = 0.08     pditsd = 0.23     pditsl = 2.3e+006
+rsh    = 5        rsw    = 85      rdw    = 85
+rdsmin = 0        rdwmin = 0      rswmin = 0      prwg   = 3.22e-008
+prwb   = 6.8e-011 wr     = 1      alpha0 = 0.074    alpha1 = 0.005
+beta0  = 30       agidl  = 0.0002   bgidl  = 2.1e+009   cgidl  = 0.0002
+egidl  = 0.8

+aigbacc = 0.012    bigbacc = 0.0028   cigbacc = 0.002
+nigbacc = 1        aigbinv = 0.014   bigbinv = 0.004   cigbinv = 0.004
+eigbinv = 1.1      nigbinv = 3        aigc    = 0.69     bigc    = 0.0012
+cigc    = 0.0008   aigsd  = 0.0087   bigsd   = 0.0012   cigsd   = 0.0008
+nigc    = 1        poxedg = 1        pigcd   = 1        ntox    = 1

+xrcrg1 = 12        xrcrg2 = 5
+cgbo   = 2.56e-011 cgdl   = 2.653e-10
+cgs1   = 2.653e-10 ckappas = 0.03     ckappad = 0.03     acde    = 1
+moin   = 15        noff    = 0.9     voffcv  = 0.02

+kt1    = -0.11     kt1l   = 0        kt2    = 0.022    ute     = -1.5
+ual    = 4.31e-009 ub1    = 7.61e-018 uc1    = -5.6e-011 prt     = 0
+at     = 33000

+fnoimod = 1        tnoimod = 0

+jss    = 0.0001    jsws   = 1e-011   jswgs  = 1e-010   njs     = 1
+ijthsfd = 0.01     ijthsrev = 0.001   bvs     = 10      xjbvs   = 1
+jsd     = 0.0001    jswd   = 1e-011   jswgd  = 1e-010   njd     = 1
+ijthdfd = 0.01     ijthdrev = 0.001   bvd     = 10      xjbvd   = 1
+pbs     = 1        cjs     = 0.0005   mjs     = 0.5      pbsws   = 1
+cjsws   = 5e-010   mjsws  = 0.33     pbswgs  = 1      cjswgs  = 3e-010
+mjswgs  = 0.33     pbd     = 1        cjd     = 0.0005   mjd     = 0.5
+pbswd   = 1        cjswd  = 5e-010   mjswd  = 0.33     pbswgd  = 1
+cjswgd  = 5e-010   mjswgd = 0.33     tpb     = 0.005    tcj     = 0.001
+tpbsw   = 0.005    tcjsw  = 0.001    tpbswg  = 0.005    tcjswg  = 0.001
+xtis    = 3        xtids   = 3

+dmcg    = 0e-006   dmci    = 0e-006   dmdg    = 0e-006   dmcgt   = 0e-007
+dwj     = 0.0e-008 xgw     = 0e-007   xgl     = 0e-008

+rshg    = 0.4      gbmin   = 1e-010   rbpb    = 5        rbpd    = 15
+rbps    = 15      rbdb    = 15      rbsb    = 15      ngcon   = 1

```

Appendix D. Inverter SPICE Netlists

```
.subckt INV_130 IN OUT GND VDD
```

```
M1 VDD IN OUT VDD pmos L=.130u W=0.78u
```

```
M2 OUT IN 0 0 nmos L=0.130u W=0.39u
```

```
.ends INV_130
```

```
.subckt INV_90 IN OUT GND VDD
```

```
M1 VDD IN OUT VDD pmos L=.09u W=0.54u
```

```
M2 OUT IN 0 0 nmos L=0.09u W=0.27u
```

```
.ends INV_90
```

```
.subckt INV_65 IN OUT GND VDD
```

```
M1 VDD IN OUT VDD pmos L=.065u W=0.39u
```

```
M2 OUT IN 0 0 nmos L=0.065u W=0.195u
```

```
.ends INV_65
```

Appendix E. NAND Gate SPICE Netlists

```
.subckt NAND_130 IN1 IN2 OUT GND VDD
```

```
M1 OUT IN1 VDD VDD pmos L=.130u W=0.78u  
M2 OUT IN2 VDD VDD pmos L=.130u W=0.78u  
M3 OUT IN2 MIDN 0 nmos L=0.130u W=0.39u  
M4 MIDN IN1 0 0 nmos L=0.130u W=0.39u
```

```
.ends NAND_130
```

```
.subckt NAND_90 IN1 IN2 OUT GND VDD
```

```
M1 OUT IN1 VDD VDD pmos L=.09u W=0.54u  
M2 OUT IN2 VDD VDD pmos L=.09u W=0.54u  
M3 OUT IN2 MIDN 0 nmos L=0.09u W=0.27u  
M4 MIDN IN1 0 0 nmos L=0.09u W=0.27u
```

```
.ends NAND_90
```

```
.subckt NAND_65 IN1 IN2 OUT GND VDD
```

```
M1 OUT IN1 VDD VDD pmos L=.065u W=0.39u  
M2 OUT IN2 VDD VDD pmos L=.065u W=0.39u  
M3 OUT IN2 MIDN 0 nmos L=0.065u W=0.195u  
M4 MIDN IN1 0 0 nmos L=0.065u W=0.195u
```

```
.ends NAND_65
```

Appendix F. XOR Gate SPICE Netlists

```
.subckt XOR_130 IN1 IN2 NOTIN1 NOTIN2 OUT GND VDD
M1 MIDP1 IN2 VDD VDD pmos L=.130u W=0.78u
M2 OUT NOTIN1 MIDP1 VDD pmos L=.130u W=0.78u
M3 MIDP2 NOTIN2 VDD VDD pmos L=.130u W=0.78u
M4 OUT IN1 MIDP2 VDD pmos L=.130u W=0.78u
M5 OUT NOTIN1 MIDN1 0 nmos L=0.130u W=0.39u
M6 MIDN1 NOTIN2 0 0 nmos L=0.130u W=0.39u
M7 OUT IN1 MIDN2 0 nmos L=0.130u W=0.39u
M8 MIDN2 IN2 0 0 nmos L=0.130u W=0.39u
.ends XOR_130
```

```
.subckt XOR_90 IN1 IN2 NOTIN1 NOTIN2 OUT GND VDD
M1 MIDP1 IN2 VDD VDD pmos L=.09u W=0.54u
M2 OUT NOTIN1 MIDP1 VDD pmos L=.09u W=0.54u
M3 MIDP2 NOTIN2 VDD VDD pmos L=.09u W=0.54u
M4 OUT IN1 MIDP2 VDD pmos L=.09u W=0.54u
M5 OUT NOTIN1 MIDN1 0 nmos L=0.09u W=0.27u
M6 MIDN1 NOTIN2 0 0 nmos L=0.09u W=0.27u
M7 OUT IN1 MIDN2 0 nmos L=0.09u W=0.27u
M8 MIDN2 IN2 0 0 nmos L=0.09u W=0.27u
.ends XOR_90
```

```
.subckt XOR_65 IN1 IN2 NOTIN1 NOTIN2 OUT GND VDD
M1 MIDP1 IN2 VDD VDD pmos L=.065u W=0.39u
M2 OUT NOTIN1 MIDP1 VDD pmos L=.065u W=0.39u
M3 MIDP2 NOTIN2 VDD VDD pmos L=.065u W=0.39u
M4 OUT IN1 MIDP2 VDD pmos L=.065u W=0.39u
M5 OUT NOTIN1 MIDN1 0 nmos L=0.065u W=0.195u
M6 MIDN1 NOTIN2 0 0 nmos L=0.065u W=0.195u
M7 OUT IN1 MIDN2 0 nmos L=0.065u W=0.195u
M8 MIDN2 IN2 0 0 nmos L=0.065u W=0.195u
.ends XOR_65
```

Appendix G. SRAM SPICE Netlists

```
.subckt SRAM_130 BIT BIT_NOT A A_NOT WORD GND VDD
```

```
M1 A WORD BIT 0 nmos L=.130u W=0.39u
M2 A_NOT WORD BIT_NOT 0 nmos L=.130u W=0.39u
M3 A A_NOT 0 0 nmos L=.130u W=0.39u
M4 A_NOT A 0 0 nmos L=.130u W=0.39u
M5 A A_NOT VDD VDD pmos L=.130u W=0.78u
M6 A_NOT A VDD VDD pmos L=.130u W=0.78u
.ends SRAM_130
```

```
.subckt SRAM_90 BIT BIT_NOT A A_NOT WORD GND VDD
```

```
M1 A WORD BIT 0 nmos L=.09u W=0.27u
M2 A_NOT WORD BIT_NOT 0 nmos L=.09u W=0.27u
M3 A A_NOT 0 0 nmos L=.09u W=0.27u
M4 A_NOT A 0 0 nmos L=.09u W=0.27u
M5 A A_NOT VDD VDD pmos L=.09u W=0.54u
M6 A_NOT A VDD VDD pmos L=.09u W=0.54u
.ends SRAM_90
```

```
.subckt SRAM_65 BIT BIT_NOT A A_NOT WORD GND VDD
```

```
M1 A WORD BIT 0 nmos L=0.065u W=0.195u
M2 A_NOT WORD BIT_NOT 0 nmos L=0.065u W=0.195u
M3 A A_NOT 0 0 nmos L=0.065u W=0.195u
M4 A_NOT A 0 0 nmos L=0.065u W=0.195u
M5 A A_NOT VDD VDD pmos L=.065u W=0.39u
M6 A_NOT A VDD VDD pmos L=.065u W=0.39u
.ends SRAM_65
```

Appendix H. DICE SPICE Netlists

```
.subckt DICE_130 BIT BIT_NOT A A_NOT WORD GND VDD
```

```
M1 INT1 WORD BIT 0 nmos L=.130u W=0.39u
M2 INT2 WORD BIT_NOT 0 nmos L=.130u W=0.39u
M3 A WORD BIT 0 nmos L=.130u W=0.39u
M4 A_NOT WORD BIT_NOT 0 nmos L=.130u W=0.39u
M5 A_NOT A 0 0 nmos L=.130u W=0.39u
M6 INT1 A 0 0 nmos L=.130u W=0.39u
M7 INT2 INT1 0 0 nmos L=.130u W=0.39u
M8 A INT2 0 0 nmos L=.130u W=0.39u
M9 A_NOT INT1 VDD VDD pmos L=.130u W=0.78u
M10 INT1 INT2 VDD VDD pmos L=.130u W=0.78u
M11 INT2 A VDD VDD pmos L=.130u W=0.78u
M12 A A_NOT VDD VDD pmos L=.130u W=0.78u
.ends DICE_130
```

```
.subckt DICE_90 BIT BIT_NOT A A_NOT WORD GND VDD
```

```
M1 INT1 WORD BIT 0 nmos L=.09u W=0.27u
M2 INT2 WORD BIT_NOT 0 nmos L=.09u W=0.27u
M3 A WORD BIT 0 nmos L=.09u W=0.27u
M4 A_NOT WORD BIT_NOT 0 nmos L=.09u W=0.27u
M5 A_NOT A 0 0 nmos L=.09u W=0.27u
M6 INT1 A 0 0 nmos L=.09u W=0.27u
M7 INT2 INT1 0 0 nmos L=.09u W=0.27u
M8 A INT2 0 0 nmos L=.09u W=0.27u
M9 A_NOT INT1 VDD VDD pmos L=.09u W=0.54u
M10 INT1 INT2 VDD VDD pmos L=.09u W=0.54u
M11 INT2 A VDD VDD pmos L=.09u W=0.54u
M12 A A_NOT VDD VDD pmos L=.09u W=0.54u
.ends DICE_90
```

```
.subckt DICE_65 BIT BIT_NOT A A_NOT WORD GND VDD
```

```
M1 INT1 WORD BIT 0 nmos L=0.065u W=0.195u
M2 INT2 WORD BIT_NOT 0 nmos L=0.065u W=0.195u
M3 A WORD BIT 0 nmos L=0.065u W=0.195u
M4 A_NOT WORD BIT_NOT 0 nmos L=0.065u W=0.195u
```

```
M5 A_NOT A 0 0 nmos L=0.065u W=0.195u
M6 INT1 A 0 0 nmos L=0.065u W=0.195u
M7 INT2 INT1 0 0 nmos L=0.065u W=0.195u
M8 A INT2 0 0 nmos L=0.065u W=0.195u
M9 A_NOT INT1 VDD VDD pmos L=.065u W=0.39u
M10 INT1 INT2 VDD VDD pmos L=.065u W=0.39u
M11 INT2 A VDD VDD pmos L=.065u W=0.39u
M12 A A_NOT VDD VDD pmos L=.065u W=0.39u
.ends DICE_650
```

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Vita

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REPORT DOCUMENTATION PAGE				Form Approved OMB No. 074-0188	
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1. REPORT DATE (DD-MM-YYYY) 22-03-2007		2. REPORT TYPE Master's Thesis		3. DATES COVERED (From - To) August 2005 - March 2007	
4. TITLE AND SUBTITLE PARAMETRIC RELIABILITY OF SPACE-BASED FIELD PROGRAMMABLE GATE ARRAYS				5a. CONTRACT NUMBER	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S) Pomager, Joseph, C., First Lieutenant , USAF				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAMES(S) AND ADDRESS(S) Air Force Institute of Technology Graduate School of Engineering and Management (AFIT/EN) 2950 Hobson Way, Building 640 WPAFB OH 45433-7765				8. PERFORMING ORGANIZATION REPORT NUMBER AFIT/GE/EN/07-19	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Dr James C Lyke james.lyke@kirtland.af.mil AFRL/VSEE 3550 Aberdeen Ave Kirtland AFB, NM 87117-5776 (505)246-5812				10. SPONSOR/MONITOR'S ACRONYM(S)	
				11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT The high cost of failure for microelectronic devices operating in the space environment has led to a need for an accurate characterization of a device's reliability prior to being deployed. In addition, significant cost savings can be achieved by determining this reliability prior to fabrication. With the increased performance needs required for many missions, designers are seeking to utilize devices that have smaller and smaller feature sizes. Specifically, feature sizes as small as 130, 90, and 65 nm. A characterization of the space environment is constructed specifically to address the extreme conditions that can affect the performance and functionality of small feature-sized microelectronic devices. The characterization is centered on temperature, non-ideal supply voltage, and radiation effects. A simulation technique is developed to determine the reliability of a microelectronic device prior to fabrication and deployment into the space environment. The technique is based on identifying the key elements of a circuit, simulating these key elements under each characterized condition individually, and then a comprehensive simulation of the elements under all combinations of the characterized conditions in each significant element operating state. Reliability calculations are performed based on simulation results and identified critical performance criteria. A demonstration of the technique is accomplished showing the poor reliability of non-radiation hardened small feature-sized commercial-off-the-shelf FPGAs in four common orbits. The results are then compared to an established, radiation hardened FPGA					
15. SUBJECT TERMS FPGA, Reliability, Space microelectronics,					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPHONE NUMBER (Include area code)
U	U	U	UU	85	Dr. Yong C. Kim, AFIT/ENG (937) 785-3636, ext 4620 (yong.kim@afit.edu)