

Integrated silicon optical receiver with avalanche photodiode

S.M. Csutak, J.D. Schaub, S. Wang, J. Mogab and J.C. Campbell

Abstract: An optical receiver consisting of an avalanche photodiode integrated with a transimpedance amplifier is reported. The optical receiver was fabricated on a 2 μm thick SOI substrate in a 130 nm unmodified CMOS process flow. The unity gain external quantum efficiency of the photodetectors was $\sim 10\%$ at 850 nm. Optimum sensitivity was achieved for an avalanche gain $M=8$. This gain accounted for 5 dB improvement in receiver sensitivity at 2 Gbit/s. Operation at 8 Gbit/s was achieved only when the photodetector was biased in the avalanche gain regime.

1 Introduction

Silicon optical receivers can be used for short-reach optical datalinks and optical backplanes in conjunction with 850 nm vertical cavity lasers. There have been several reports of monolithically integrated silicon optical receivers [1–5]. However, there are very few reported results for integrated receivers in any materials system using avalanche photodiodes. Bracket *et al.* reported a 45 Mbit/s optical receiver that included an avalanche photodetector and a two-transistor transimpedance amplifier circuit with 70 MHz bandwidth [6]. Yoshida *et al.* [2] reported a 1 GHz SIMOX integrated photoreceiver that showed improved performance due to avalanche gain, but no details regarding the avalanche gain were given. This paper reports the performance of an integrated optical receiver consisting of a silicon avalanche photodiode and a transimpedance amplifier fabricated in an unmodified 130 nm CMOS technology on 2 μm thick high-resistivity SOI substrate.

2 Circuit design and fabrication

The circuit design and fabrication process have been described in [7, 8]. The circuit consists of a three-stage transimpedance amplifier with a 50 Ω output impedance. The first stage has high input impedance to accommodate the photodetector current source. The transimpedance gain was 31 dB Ω , the area of the receiver was 600 $\times$ 800 μm^2 and it dissipated 31 mW power. The SOI thickness was chosen to achieve a compromise between speed and quantum

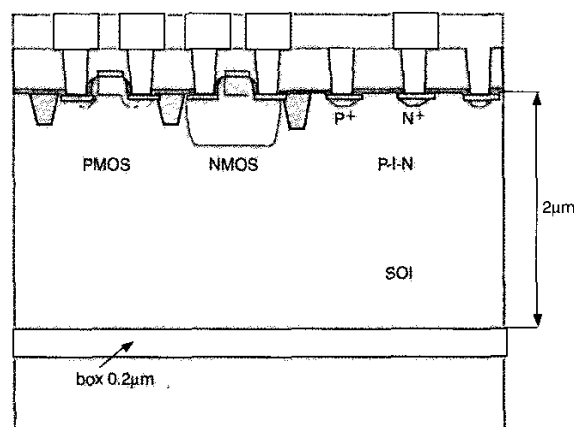


Fig. 1 Schematic cross-section of integrated receiver

efficiency of the lateral interdigitated P-I-N photodetector. A cross-sectional diagram of the device is shown in Fig. 1. The area of the photodetector was 50 $\times$ 50 μm^2 with a 1 μm $\times$ 2 μm electrode width $\times$ spacing. The electrode regions were formed by P-type and N-type implants when the source and drain for the P-channel and N-channel MOSFETs were implanted. The electrodes were salicided during the transistor salicidation process to reduce the series resistance of the fingers. The electrodes also had implants which were used to prevent breakdown in the MOSFET devices. These implants helped to reduce non-uniform breakdown at the edge of the photodetector electrodes and improved the avalanche characteristics.

3 Results

The discrete photodetectors were characterized on-chip and their bandwidth was measured using a directly modulated 850 nm vertical-cavity surface-emitting laser. The frequency response as a function of bias and gain is shown in Fig. 2a. The 3 dB bandwidth was 1.8 GHz at -3 V. The bandwidth increased to 8 GHz when the bias was increased to -28 V. This increase in the bandwidth

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S.M. Csutak, S. Wang and J.C. Campbell are with the Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712, USA. S.M. Csutak is also with Silicon RF/IF Emerging Technologies, Motorola Inc., Austin, TX 78721, USA

J.D. Schaub is with IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA

J. Mogab is with Advanced Process Development and External Research, Motorola Inc., Austin, TX 78721, USA

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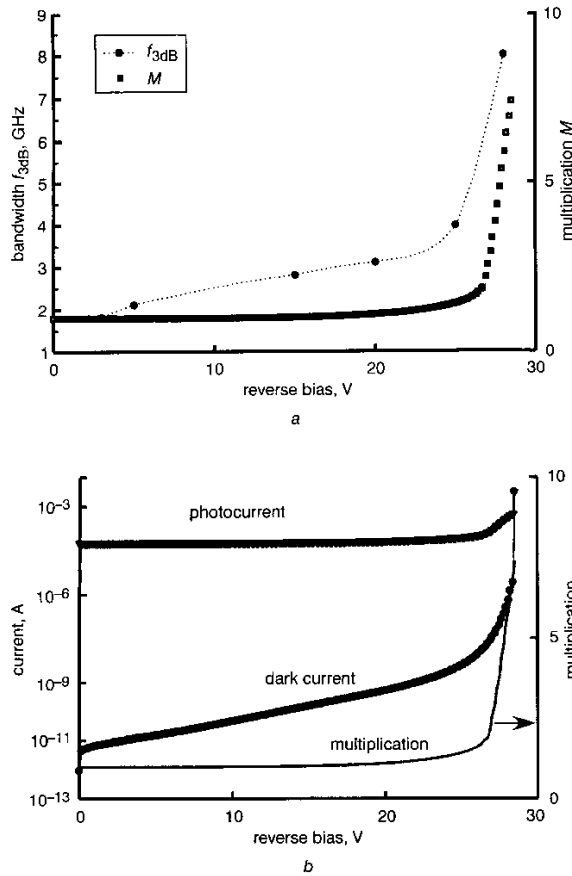


Fig. 2 Photodiode characteristics

a Frequency response against reverse bias for a photodiode with $1\ \mu\text{m} \times 2\ \mu\text{m}$ electrode width $\times$ electrode spacing
b I - V characteristics under illumination and with no illumination for the device presented in Fig. 2*a*

results from higher electric field intensity, particularly in the region near the buried oxide, which enables carriers to reach saturation velocity. The external quantum efficiency was 10% at 850 nm at $-3\ \text{V}$. The photocurrent, dark current, and gain are shown in Fig. 2*b* for a photodiode with $1\ \mu\text{m} \times 2\ \mu\text{m}$ electrode width $\times$ electrode spacing. The dark current was less than 20 pA for a reverse bias of 10 V and the breakdown occurred at $-26\ \text{V}$.

Using an argon UV laser (351/363 nm) as the optical source, the noise power spectral density of the APDs was measured with an HP 8970B noise figure meter at 50 MHz with a bandwidth of 4 MHz. The excess noise factor is a fundamental parameter of the local-field theory [9]. It has become a figure of merit for APD noise performance. Fig. 3 shows the measured excess noise factor against gain. For a multiplication gain $M=8$ the excess noise factor is 2.8. The ratio of the ionisation coefficient k was found to be 0.15. This is higher than the typical k values for Si APDs and is a result of the fact that the interdigitated photodiode structure creates mixed injection into the multiplication region. Fig. 4 presents a comparison between the measured data and the calculated sensitivities for several bit rates. For these calculations [10] the following parameters were used: the sum of the gate-source, gate-drain, photodetector and stray capacitances, $C_{\text{total}} = C_{\text{GS}} + C_{\text{GD}} + C_{\text{PD}} + C_{\text{stray}} = 650\ \text{fF}$, $g_m = 550\ \text{mS/mm}$, total external quantum efficiency,

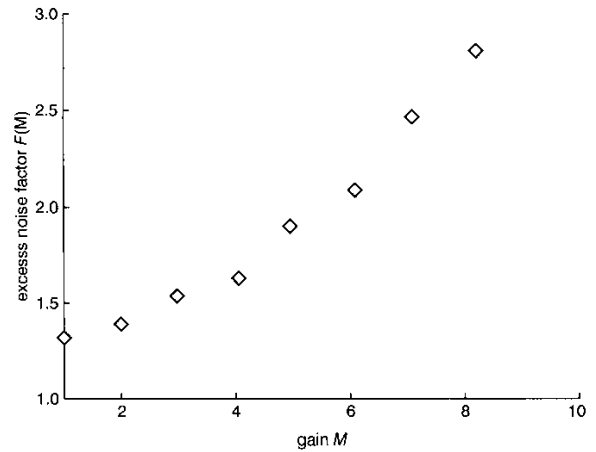


Fig. 3 Excess noise factor $F(M)$ against gain M

$QE = 10\%$, and dark current of the photodetector $I_D = 0.5\ \text{mA}$. The receiver achieved a BER of 10^{-9} at an average optical power of $-17\ \text{dBm}$ at 2 Gbit/s, $-10.9\ \text{dBm}$ at 5.0 Gbit/s, and $+2\ \text{dBm}$ at 8 Gbit/s. The improvement in receiver sensitivity provided by the internal gain of an APD relative to a PIN receiver is given by the expression [10]:

$$\frac{(\bar{P})_{\text{APD}}}{(\bar{P})_{\text{PIN}}} = \frac{1}{M} \left[1 + \frac{qI_1 Q M^2 F(M) B}{(i^2)_c^{1/2}} \right] \quad (1)$$

$\bar{P}$ is the average input optical power required to achieve a given bit error rate (BER), which is typically 10^{-9} for telecommunications applications. The numerator $qI_1 Q M^2 F(M) B$ is the noise current density of the APD. The Personick integral I_1 is a normalised noise-bandwidth integral that has a value of 0.548 for non-return-to-zero input pulses, Q is the signal-to-noise ratio ($Q=6$ for $\text{BER}=10^{-9}$), B is the bit rate, and $(i^2)_c^{1/2}$ is the noise current density of the transimpedance amplifier. When the noise of the APD is much less than that of the amplifier a receiver improvement of M is expected. The optimum gain, which was determined empirically to be approximately $M=8$, occurs when the APD noise is comparable to the amplifier noise. Consequently, the improvement in sensitivity is estimated to be 6 dB. For bit rates up to 5 Gbit/s, the receiver sensitivity increased as the reverse bias was

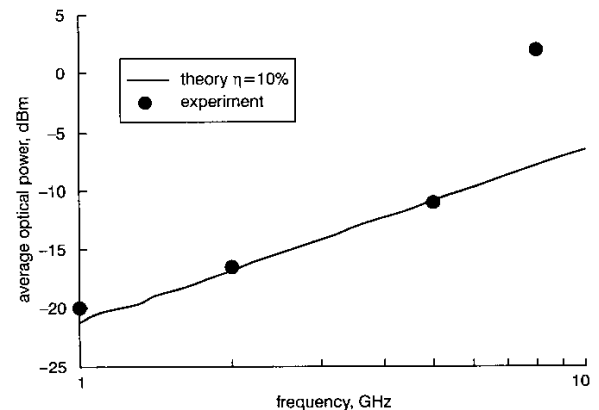


Fig. 4 Measured and calculated minimum average optical input power for $\text{BER} = 10^{-9}$ against bit rate for $V_{\text{PD}} = -27\ \text{V}$

increased; the APD gain accounted for 5 dB improvement in sensitivity. Error-free operation at 8 Gbit/s was achieved only when the photodetector was biased in a region with significant gain.

4 Summary

In this paper, we have reported the monolithic integration of an avalanche photodiode and a transimpedance amplifier in an all-silicon optical receiver. The circuits were fabricated in an unmodified 130 nm salicided CMOS process on 2 μm thick SOI substrates. The receiver achieved a BER of 10^{-9} at an average optical power of -19 dBm at 2 Gbit/s, -10.9 dBm at 5.0 Gbit/s, and $+2$ dBm at 8 Gbit/s. The optimum gain was $M=8$. This avalanche gain improved the sensitivity of the receiver by 5 dB. Error-free operation at 8 Gbit/s was achieved only when the photodetector was biased in the avalanche gain regime.

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