REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Washington Headquarters Service, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington, DC 20503.
PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT DATE	3. DATES COVERED *(From - To)*
8/1/2007	Final Technical Report	03/01/2005 - 5/31/2007

4. TITLE AND SUBTITLE
Development of Process Technologies for High-Performance MOS-Based SiC Power Switching Devices

5a. CONTRACT NUMBER
N00014-05-1-0437

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Dr. James A. Cooper
Dr. Michael A. Capano
Dr. Leonard C. Feldman
Dr. Marek Skowronski
Dr. John R. Williams

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Purdue University
Sponsored Program Services
302 Wood Street
West Lafayette, IN 47906

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
ONR - Ingham A Mack (ONR 312)
875 North Randolph Street
Arlington, VA 22203-1995

ONR -Chicago Office (N62880)
230 South Dearborn, Rm380
Chicago, IL 60604-1595

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
No restrictions

13. SUPPLEMENTARY NOTES

14. ABSTRACT
In this work we developed the technology for 20 kV insulated gate bipolar transistors (IGBTs) in 4H-SiC. The p-channel IGBT is formed on a 175 µm p-type epilayer on an n+ substrate. The n-IGBT is formed on the C-face of a 200 µm n-type free-standing epilayer. When operated at 300 W/cm2, the p- and n-IGBTs carry 30 and 27 A/cm2 respectively, independent of temperature from 23 °C to 175 °C. These results were made possible by advances in epigrowth of thick SiC epilayers with low doping, high carrier lifetime, and minimal basal plane dislocations. Ambipolar lifetimes as high as 1.7 µs and BPD densities as low as 2.6 cm-2 were achieved. The work was further supported by research on the MOS interface on both C-face and Si-face SiC, including studies of threshold voltage and long-term reliability. Oxides on the C-face have comparable mobility to those on the Si-face, but lower breakdown fields and reduced long-term reliability.

15. SUBJECT TERMS
SiC power devices, insulated gate bipolar transistors, IGBTs, SiC epigrowth, ambipolar lifetime, basal plane dislocations, BPDs, point defects, SiC MOS mobility, threshold voltage, SiC MOS oxide reliability

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Dr. James A. Cooper Jr.
U	U	U		441	19b. TELEPONE NUMBER (*Include area code*) (765) 494-3514

Executive Summary

The goal of this project is to develop the technology for conductivity-modulated MOS-based power devices for high blocking voltages, namely 15 – 20 kV. The devices investigated are insulated-gate bipolar transistors (IGBTs) in 4H-SiC.

The IGBT combines the best aspects of MOS and bipolar power transistors. IGBTs can be thought of as a fusion of a MOSFET and a BJT. The MOSFET provides a high input impedance while the BJT provides conductivity modulation of the drift region in the on-state. Electrically, the MOSFET supplies base current to the BJT, and both devices share the total current.

At blocking voltages increase, the drift region of a power device becomes very thick and very lightly doped, in order to hold off the high blocking voltage in the off state. In a MOSFET, the drift region resistance increases as the square of the blocking voltage, due to the increasing thickness and decreasing doping in the drift layer. By merging the *unipolar* MOSFET with an integral *bipolar* BJT, we significantly reduce the resistance of the drift region due to conductivity modulation from the forward-biased BJT.

The IGBT is structurally *identical* to a MOSFET, except that the substrate doping polarity is inverted from that for a MOSFET. Both n-channel and p-channel IGBTs are possible, and both are developed in this project. The n-IGBT requires a p+ substrate, while the p-IGBT requires an n+ substrate. In the past, n-IGBTs have not been feasible, since the resistance of a standard p+ SiC substrate is quite high (~ 1 Ω cm^2). However, in the blocking voltage range above about 15 kV, the drift layer becomes sufficiently thick that it is possible to polish off the p+ substrate and replace it with a thin p+ epilayer, reducing the resistance to a negligible value. This approach is taken in this project. As will be detailed in Section 3 below, the process is arranged in such a way that device fabrication of the n-IGBT takes place on the *(000-1) carbon face* of SiC. This presents unique challenges, since very little is known about device fabrication on the carbon face.

Since the IGBT incorporates an MOS interface, optimization of the MOS interface for both Si- and C-faces of SiC is extremely important. In our project, Task 1 is devoted to MOS interface optimization. The primary goals are (i) characterization of the MOS interface on (000-1) SiC, (ii) improved control of threshold voltage on both (0001) and (000-1) surfaces, (iii) improved stability of threshold voltage under actual device operation, and (iv) characterization and optimization of long-term *reliability* of the MOS interface on both surfaces. The results of this study will be described in Section 1 below.

In either n- or p-channel IGBT, a primary concern is the *ambipolar lifetime* in the drift region. The ambipolar lifetime is the sum of the hole and electron minority carrier lifetimes. Simulations indicate that for effective conductivity modulation, the ambipolar lifetime needs to be ≥ 1 μs. Fortunately, epilayers grown by the hot-wall CVD process, which is routinely used for the thick epilayers required in these devices, typically exhibit lifetimes that border on this range. A major goal of this project is to study the epigrowth process in more detail, to determine the physical factors limiting lifetime and find ways to optimize the growth process to achieve the desired lifetimes.

Another critical materials concern is the stability of the forward voltage drop in pn junctions operated at high current densities. Such junctions are present in the IGBT. It has been shown that SiC material can develop a network of *stacking faults* when subjected to the high levels of carrier injection and recombination. These conditions are present in forward-biased pn diodes, as well as in BJTs, thyristors, and IGBTs. The stacking faults nucleate at *basal plane dislocations* (BPDs) in the material, and propagate along the basal plane, eventually creating a network of defects that increase both the resistance and the forward voltage drop. The stacking fault propagation is driven by the energy dissipated when large numbers of holes and electrons recombine. The most effective solution is to minimize the number of BPDs that serve as nucleation sites for stacking fault propagation. Accordingly, one of the materials goals of this project is to grow thick, lightly-doped epilayers while maintaining a high ambipolar lifetime and minimal basal plane dislocations. These sometimes conflicting objectives are the challenge of Task 2, which is devoted to the material science of SiC epigrowth. The results of this work will be described in Section 2 of this report.

Finally, Task 3 is charged with designing, fabricating, and characterizing both n-channel and p-channel IGBTs on epilayers capable of blocking 20 kV. This requires integrating the MOS interface advances from Task 1 and the materials advances from Task 2 into a coherent fabrication process that will produce the desired devices.

The main results from Task 1 are summarized as follows: With regard to device fabrication on the carbon face, we find that conventional thermal oxidation followed by a nitric oxide post-oxidation anneal produces an MOS interface with an effective mobility comparable to that on the silicon face, but with a higher threshold voltage. This is good news, since the threshold voltage of NO-annealed MOSFETs on the silicon face is often negative, resulting in a normally-on device. In fact, major efforts have been expended to increase the threshold voltage of Si-face MOSFETs. This issue will not be a problem with C-face devices. Unfortunately, oxides on the C-face have

poorer reliability and lower breakdown field compared to those on the Si-face. NO annealing improves the reliability, but has little effect on breakdown strength. The lower breakdown strength requires that the gate voltage in the on-state be de-rated, resulting in a higher channel resistance. This degrades the performance of n-IGBTs on the C-face, and may nullify the advantage over p-IGBTs due to a higher carrier mobility in the inversion layer.

With regard to devices on the Si-face, including both MOSFETs and p-IGBTs, our studies indicate that the projected long-term lifetime is acceptable for power device applications. For devices in which the MOS interface is formed on implanted layers, improving the surface morphology by using graphite-cap implant annealing or by a post-implantation polishing step increases the reliability of the oxides. We also find that nitrided MOS oxides are quite robust against electron injection and trapping during device operation, but they are significantly more susceptible to positive charge trapping when subject to hole injection.

Our results on threshold stability were somewhat disappointing. Flat-band voltage shifts induced by bias-temperature stressing were substantially higher than the program goals. These instabilities are associated with mobile ion contamination in our oxidation process, and are not considered to be 'intrinsic' characteristics of the oxides themselves. Although the instabilities are larger than desired, they are still within the limits of the values allowed for commercial power devices ($\Delta V_T < 1$ V after 1000 hours at $V_G = 20$ V and T = 150 °C).

The main results from Task 2 are summarized as follows: We investigated epigrowth of thick blocking layers on both 4° and 8° off-cut 4H-SiC substrates. It is somewhat easier to achieve low n-type doping on 4° off-cut substrates due to the lower incorporation of nitrogen, but the 4° off-cut substrates exhibit surface macro-steps that depend on the C/Si ratio during growth. Overall, our best results for n-type epilayers were obtained on 8° off-cut substrates (182 µm, 1×10^{14} cm^{-3}). However, basal plane dislocation (BPD) densities are lower on 4° off-cut substrates. Our lowest BPD density is 2.6 cm^{-2} obtained on 4° off-cut substrates at a C/Si ratio of 2.0.

Fabrication of the n-IGBT involves epigrowth on the Si-face followed by device fabrication on the C-face. Since MOS oxides on the C-face are inferior to those on the Si-face (as determined under Task 1), we investigated the feasibility of epigrowth on the C-face, which would allow device fabrication on the Si-face. Our results indicate that growth on the C-face may be feasible, but more work is needed to achieve electrical properties comparable with those on the Si-face.

Minority carrier lifetimes and ambipolar lifetimes are characterized by electron-beam-induced current (EBIC) and time-resolved photoluminescence (TRPL) techniques, while deep level centers in the material are characterized by deep-level transient spectroscopy (DLTS). We found that *the density of deep traps that control the lifetime, namely Z1/Z2 centers and EH6/EH7 centers, decrease with increasing C/Si ratio during epigrowth.* We have further found that in the samples studied, the lifetime is limited by the Z1/Z2 centers, rather than by EH6/EH7 centers. This information provides a mechanism to increase the ambipolar lifetime by optimizing growth conditions. By adjusting the C/Si ratio during growth, lifetimes in the range of 1 – 2 μs have been achieved in our thick, lightly-doped epilayers, meeting the basic needs for IGBT device fabrication. While these results are promising, more work needs to be done to fully optimize growth conditions for high-voltage conductivity-modulated power devices.

The main results from Task 3 are summarized as follows: We designed, fabricated both p-channel and n-channel IGBTs on epilayers capable of blocking 20 kV. A meaningful figure-of-merit for the on-state device operation is the current density that the device can provide without exceeding the power dissipation limit of the package, which we take to be 300 W/cm^2. This figure-of-merit is suitable for comparing all types of devices at low switching frequencies, including unipolar MOSFETs, and bipolar BJTs, thyristors, and IGBTs. As described in Section 3.1, our p-IGBTs exhibited an on-state current density of 30 A/cm^2 at a power dissipation of 300 W/cm^2 and junction temperature between 23 - 177 °C. The on-current density did not degrade with temperature, being essentially unchanged at 177 °C. These values are very close to those predicted by computer simulations. For comparison, the *theoretical maximum* on-current for a SiC MOSFET that would block 20 kV is 15 A/cm^2 at 225 °C. Thus, our *experimentally realized* p-IGBT is a factor of two better than the *theoretical limit* for a SiC n-channel MOSFET. It should be kept in mind that even if the ambient temperature is 23 °C, the *junction temperature* of a device dissipating 300 W/cm^2 will approach 200 °C.

We were also successful in fabricating n-channel IGBTs, although the processing is much more difficult, as described in Section 3.2 of this report. The challenges include (i) polishing off the substrate without breaking the remaining n-type epilayer, (ii) performing all device fabrication operations, including ion implantation, implant annealing, thermal oxidation, and ohmic contact formation, without breaking the thin free-standing epilayer, and (iii) performing all fabrication operations on the carbon face of SiC, where MOS oxidation conditions and oxide quality are different than on the

silicon face. In spite of numerous processing difficulties, our best n-IGBTs exhibited an on-state current density of 27 A/cm^2, almost as high as the p-IGBTs. These values are respectable, but are somewhat lower than the 40 A/cm^2 predicted by numerical simulations. It is our conclusion that the possible slight advantage of n-IGBTs over p-IGBTs does not justify the considerably more difficult processing involved.

In summary, ***this project achieved its primary objectives*** of demonstrating the feasibility of SiC IGBTs for power switching applications in the 15 – 20 kV blocking voltage regime. In the process, we also developed new knowledge about the MOS interface on carbon-face SiC, and new information on the reliability of MOS oxides on both Si- and C-face SiC. We developed the technology for growing thick, lightly-doped epilayers capable of blocking 20 kV with lifetimes in the range of 1 – 2 μs and low basal-plane dislocation density suitable for high-current operation.

The following detailed technical report is divided into three sections. Section 1 deals with Task 1, **MOS Interface Optimization**, performed by John R. Williams at Auburn University and Leonard C. Feldman at Vanderbilt University. Section 2 discusses Task 2, **Growth of Thick Blocking Layers with Long Lifetime and No V_F Drift**, performed by Michael A. Capano at Purdue University and Marek Skowronski at Carnegie Mellon University. Section 3 describes Task 3, **Process Integration and Device Development**, led by James A. Cooper at Purdue University. While sections and figures are numbered consecutively throughout the report, equations and references are numbered within each section, and cited references are collected at the end of each section.

1. MOS Interface Optimization

J.R. Williams, Auburn University
L.C. Feldman, Vanderbilt University

1.1 Introduction

Interface optimization and oxide reliability studies performed in Task I were at aimed at providing support for the following devices: 1) n-channel IGBTs (Purdue), 2) p-channel IGBTs (Purdue) and 3) n-channel DMOSFETs (Northrop Grumman). The device fabrication process used at Purdue for the n-channel IGBT requires source implants, p-well implants and oxidation on the (000-1) C terminated face of 4H-SiC. As a result, a major portion of effort has been directed towards characterizing the SiO_2/(000-1) 4H-SiC interface, since much less was known about oxidation of the C-face compared to the Si-face at the start of our program. The general objectives and the more specific goals of the program were the following.

Objectives:
1) SiO_2 / (000-1) 4H-SiC interface characterization
2) Threshold voltage control during fabrication
3) Threshold voltage stability
4) Long-term reliability

Goals:
1) Suitable threshold voltage for 'normally-off' operation.
2) E_{BDWN} > 8MV/cm at 23C (7MV/cm at 250C).
3) ΔV_{TH} < 100mV after 5hr at 250C and 4MV/cm.
4) Intrinsic long-term breakdown.

The work undertaken at Vanderbilt and Auburn to address each of these objectives will be described in detail in the following sections.

1.2. SiO_2/ (000-1) C-face 4H-SiC interface characterization

1.2.1 Nitridation with NO post-oxidation annealing

Figure 1.1 shows interface trap densities (D_{it}) near the 4H conduction band edge and typical hi-lo C-V curves for C-face (000-1) compared to the conventional Si-face (0001). Trap densities deeper in the band gap are shown in Fig. 1.2. Following a 1175° post-oxidation NO anneal the trap densities very near E_C are similar for both faces; however, deeper in the band gap the (000-1) trap density is higher. The larger amount of negative charge remaining in these traps gives rise to the right shift of the (000-1) C-V curves. As will be discussed later, the presence of these traps is both an advantage and a disadvantage. Trap densities are shown in Fig. 1.3 for measurements made near the valence band edge using p-4H MOS capacitors. NO annealing results in a significant

reduction of D_{it} in the lower half of the band-gap for the C-face compared to a standard dry oxidation process. For the as-oxidized C-face interface an extremely high D_{it} in the lower of the gap pins the surface Fermi level making conventional hi-lo analysis inaccurate (data not shown). The reduction in integrated trap density associated by nitridation (ΔN_{it}) can be estimated to be as high as ~$5x10^{13}$ cm^{-2}. In spite of significant passivation, nitrided C-face interfaces have an order of magnitude higher D_{it} in the lower half of the gap compared to the 'as-oxidized' Si-face (Fig. 1.3). However, for n-channel devices, these traps are expected to be 'donor-like' interface states which when filled in inversion are likely to be neutral. Under such conditions, these states would act as traps and reduce inversion channel carrier density but would not act as scattering centers that degrade carrier mobility. The D_{it} profile of nitrided C-face interfaces will be discussed later in light of field-effect mobility measurements later in this report.

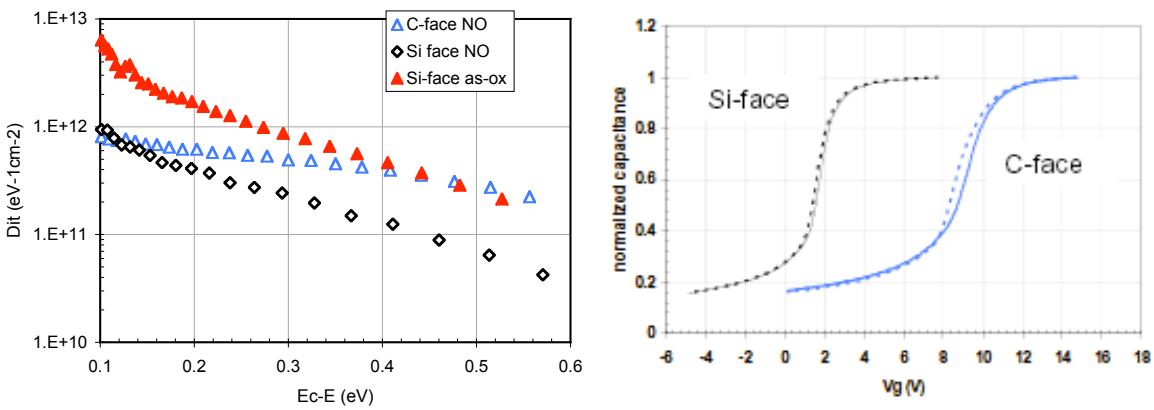


Fig. 1.1. Results of measurements using n-4H-MOS capacitors showing trap densities near the conduction band edge and typical hi-lo C-V curves for the (000-1) and (0001) faces. NO indicates measurement following a standard passivation anneal in nitric oxide (2hr, 1175C, 500sccm).

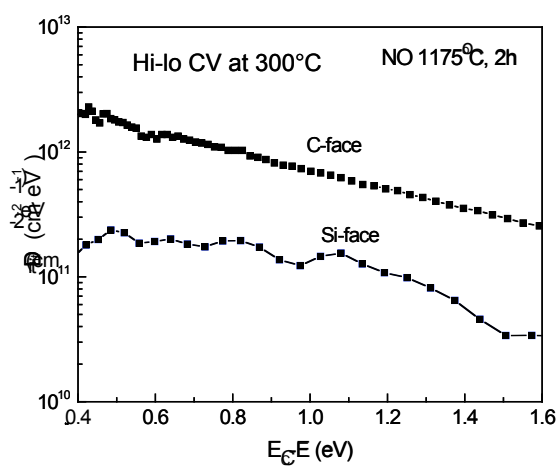


Fig. 1.2. Deep trap densities for the upper half of the band-gap for (000-1) and (0001) 4H-SiC.

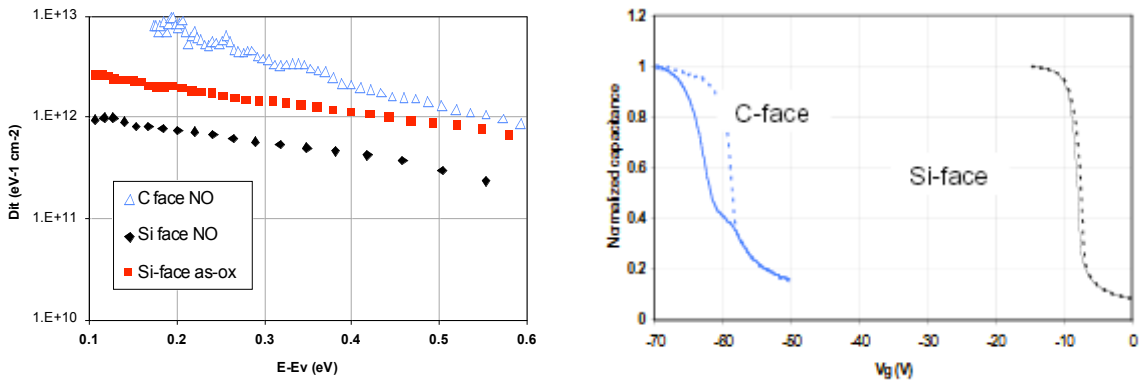


Fig. 1.3. Trap densities near the valence band edge and hi-lo C-V curves for the (000-1) and (0001) faces. 'NO' samples were passivated with a post-oxidation anneal in nitric oxide.

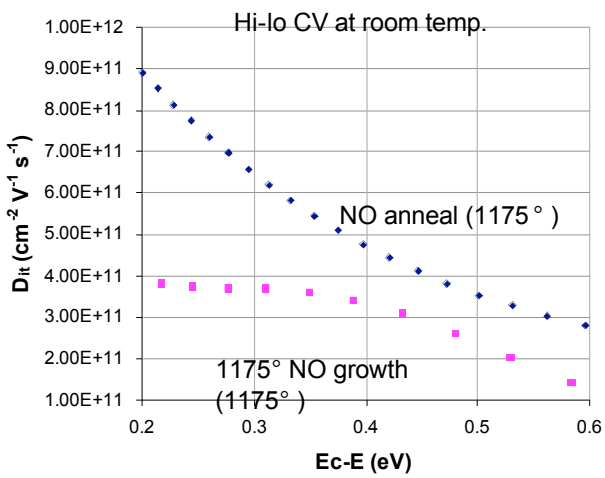


Fig. 1.4. D_{it} extracted from hi-lo CV at room temperature for C-face capacitors processed by NO post-oxidation anneal (blue) and direct oxidation in NO (pink).

1.2.2 Direct oxidation in NO for C-face 4H-SiC

Our standard interface trap passivation process for oxides grown on 4H-SiC has been a dry oxidation followed by a post-oxidation anneal (POA) in nitric oxide NO. As mentioned earlier, for the on the (000-1) C-face, this process yields similar density of interface states (D_{it}) near the conduction band-edge compared to the standard (0001) Si-face (~10^{12} cm^{-2} eV^{-1} at E_c-E ~ 0.1 eV for both faces). Deeper in the bandgap however, D_{it} remains considerably higher for the C-face even after NO annealing (Total N_{it} between E_c-E~0.4 eV and mid-gap: C-face ~10^{12} cm^{-2}; Si-face: 2.2 x 10^{11} cm^{-2}). In spite of the significantly higher D_{it}, field-effect mobility of C-face lateral MOSFETs (NO annealed) is comparable to MOSFETs processed similarly on the Si-face (to be discussed

in detail in the subsequent section). These results warrant substantial improvement of field-effect mobility by further reduction of interface traps for the C-face. Reduction of the deep states is also important in order to obtain smaller flat-band voltages and alleviate temperature related V_{FB} instabilities. We have pursued this by performing oxidation of C-face wafers directly in a flowing NO ambient (i.e. bypassing the first dry oxidation step). It is important to note that oxidation rate in NO is about an order of magnitude lower than in pure O_2 which makes such a process practical to implement only for the C-face due to it's 3-5 times higher oxidation rate compared to the Si-face. Comparison of typical D_{it} profiles obtained by NO POA (1150°C dry O_2, 45 min followed by 1175°C, 2 h NO) and NO direct growth (1175°C, 10 h NO) are shown in Fig. 1.4. It can be seen from the data that the direct NO process results in a factor of 2-3 lower D_{it} near the conduction band-edge compared to the standard NO annealed case. The D_{it} is also low deeper in the gap as evident from the photo-CV measurements shown in Fig. 1.5. Noticeably, the NO POA sample shows a prominent 'interface-state ledge' in the photo CV curve but the ledge is absent for the 'direct NO' sample. The total deep/slow trap density estimated from the photo CV measurements for the two processes are the following: NO POA ~ 1.4 x 10^{12} cm^{-2}; direct NO oxidation ~ 5.4 x 10^{11} cm^{-2}. Therefore, the photo CV measurements also reveal a factor of 2-3 lower D_{it} for the direct NO process, consistent with hi-lo CV. The lower effective negative charge results in a smaller positive flat-band voltage for equal oxide thicknesses. For example, capacitors with 50 nm thick oxides would display flat band voltages ~ 6.0 V and ~ 4.2 V for NO POA and NO direct oxidation processes, respectively.

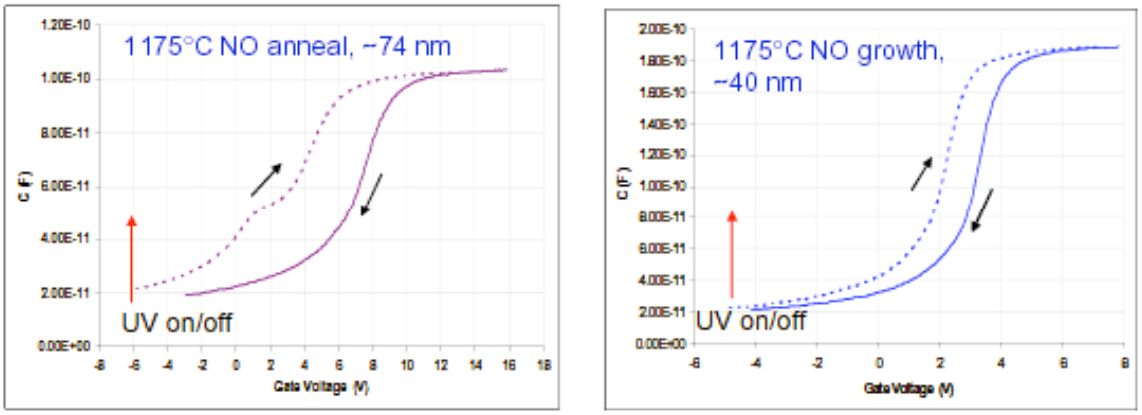


Fig. 1.5. Photo CV measurement on C-face MOS capacitors processed by NO post-oxidation anneal (left) and direct oxidation in NO (right). For the direct NO case, the interface state ledge is absent and the hysterisis is smaller indicating a decrease of slow traps.

These results certainly highlight the potential of the direct NO process for MOS fabrication on the C-face. We have also performed physical characterization of these oxide films using Rutherford Backscattering Spectrometry (RBS) in channeling mode (spectra not shown). Within the sensitivity of RBS, we have not detected any nitrogen in the oxide. This puts a maximum limit to the N content in these films to about ~3x10^{15} cm^{-}

^{2}, indicating that the direct NO process does not incorporate a substantially higher amount of N compared to the NO POA process. At this stage, we speculate that the lower trap density is due to advantageous competition between the nitridation rate (defect passivation rate) and the lower oxidation rate (defect creation rate). Lateral MOSFETs using the direct NO process for measuring field effect mobility will be fabricated and analyzed in the coming months.

1.3. Inversion layer mobility and threshold voltage for C-face MOSFETs

Comparisons of the effective channel mobility are shown in Fig. 1.6 for C-face and Si-face lateral MOSFETs following NO passivation. The higher threshold voltage for the C-face (as determined by extrapolating the linear portion of the I_d-V_g characteristic to zero intercept on the gate voltage axis) is consistent with higher trapped negative charge at the oxide/C-face interface, as evident from D_{it} measurements presented previously. Surprisingly however, the peak value of about 35cm^2/V-s is only slightly less that the peak value of 45 cm^2/V-s for the Si-face following NO-only passivation. This is perhaps an acceptable value, particularly since the threshold voltage is almost 3V higher for the C-face. Field effect mobility and I_d-V_g characteristics of n-channel lateral MOSFETs fabricated with p-well (Al) implants into n-type epitaxial C-face material is shown in Fig. 1.7. The Al implants were activated by annealing at 1650°C in Ar with a graphitic overlayer to alleviate roughness related problems. For these implanted channels, threshold voltages are higher, about ~9 V and ~14V for p-well doping of 7 x 10^{16} cm^{-3} and 2 x 10^{17} cm^{-3}, respectively. It is encouraging to note that effective mobility (~30 cm^2/V-s) for the p-well implanted with 7 x 10^{16} cm^{-3} is almost as high as epitaxial channels. This indicates that no significant additional mobility degradation or carrier scattering is induced by the implantation process up to this dose. At higher Al dose, namely 2 x 10^{17} cm^{-3} a 50% mobility degradation is observed as shown in Fig. 1.7.

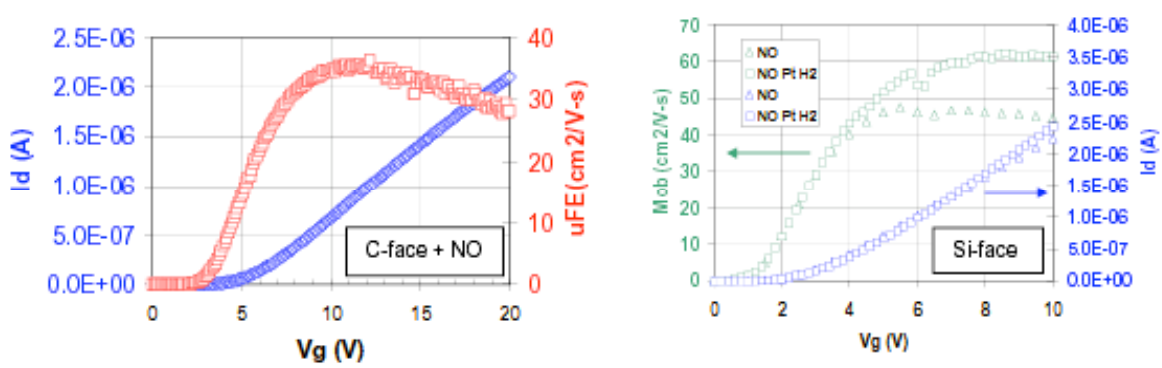


Fig. 1.6. Effective channel mobility for lateral MOSFETs fabricated on (000-1) and (0001) 4H-SiC epitaxial wafers. The MOSFETs were passivated with NO.

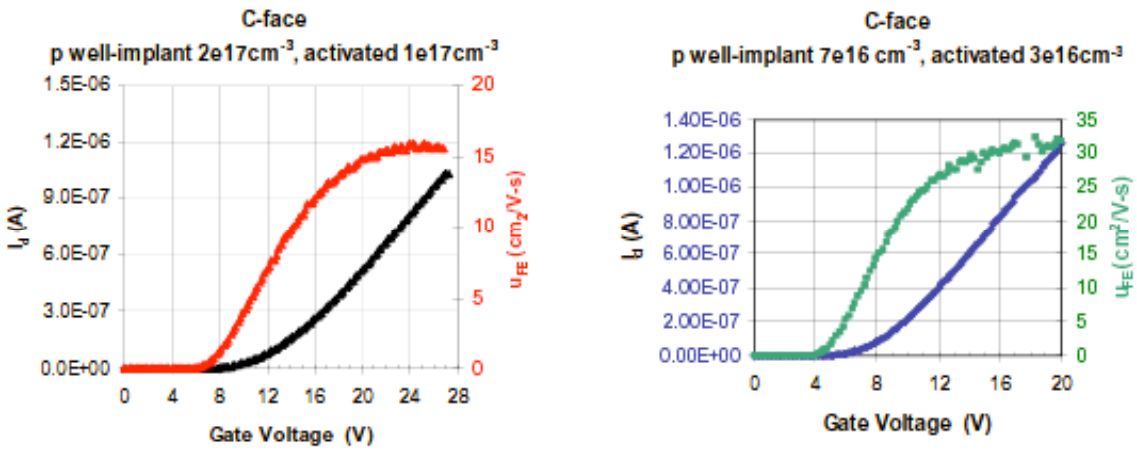


Fig. 1.7. Effective channel mobility and transconductance of lateral MOSFETs fabricated on p-well (Al) implanted (000-1) C-face 4H-SiC. The MOSFETs were passivated with NO.

In general, as the mobility increases for an n-channel inversion-mode device as the result of better interface passivation, the threshold voltage shifts towards zero, and the MOSFET operating characteristics tend towards 'normally-on'. This is equivalent to the negative flatband voltage shift that is observed when n-4H-MOS capacitors are passivated with NO. The effect can be understood by considering the following expression for the MOS capacitor flatband voltage V_{FB}.

$$V_{FB} = \Phi_{MS} - (1/C_{OX})[Q_F + \gamma Q_{OT} + \gamma Q_M + Q_{IT}(\varphi_S)]$$

where Φ_{MS} is the metal-semiconductor work function difference, C_{OX} is the oxide capacitance, Q_F is the fixed charge at the oxide-semiconductor interface, Q_{OT} is the trapped charge in the oxide, Q_M is the mobile charge in the oxide, γ is a weighting factor (= 0 and 1 at the M-O and O-S interfaces, respectively) and $Q_{IT}(\varphi_S)$ is the charge trapped in shallow defect states at the oxide-semiconductor interface. $Q_{it}(\varphi_S)$ depends on the position of the Fermi level at the interface and therefore on the semiconductor surface potential φ_S. Q_{OT} and Q_M are usually negligible in high quality oxides. For wide band gap semiconductors, the fixed charge Q_F consists of two parts

$$Q_F = Q^+ + Q^-$$

where Q^+ is the normal fixed positive charge located very near the O-S interface. The magnitude of Q^+ is determined by the final step of the oxide growth process. Q^- is negative charge permanently trapped in deep interface states whose energies are more than about 0.6 eV from the semiconductor band edges. Q^- is absent for Si which has a narrow band gap; however for SiC, Q^- represents a substantial charge density. Passivation processes such as nitridation with NO reduce Q^-. If Q^+ is not reduced as well – e.g., by modifying the terminal stage of the oxidation process, Q_F becomes a larger positive quantity, and $V_{FB} \sim (\Phi_{MS} - Q_F / C_{OX})$ shifts towards zero. ***With regards to this apparent***

tradeoff between channel mobility and threshold voltage, C-face MOSFETs present a unique advantage over conventional Si-face MOSFETs. After nitridation the effective mobility of C-face MOSFETS is comparable to the Si-face, but the threshold voltage (V_{TH}) is substantially higher (~ +3V for ~ 60 nm nitrided oxides). The most likely reason for this the higher density of energetically deeper D_{it} (Fig. 1.2) at the SiO_2(N)/C-face 4H-SiC interface which act as 'fixed' negative charge and render V_{TH} more positive in accordance with the equation above.

With regards to fundamental mechanisms of channel mobility degradation, these new results obtained for the C-face pose intriguing questions. As noted earlier, the effective mobility obtained on this face after nitridation is comparable to the nitrided Si-face inspite of an order of magnitude higher interface trap density across the band-gap. This result, to a large extent, contradicts the usual interface trap limited mobility degradation mechanism that is believed to be dominant for the Si-face. Detailed investigations are required to understand this apparent contradiction. At this stage, one could speculate that the details of the scattering processes are different on the C-face and Si-face. For example, the higher trap density in C-face could be due near interfacial oxide traps which may scatter the inversion carriers less severely as a result of larger separation from the inversion channel. Another possibility could be a lower atomic scale roughness on the C-face that decreases the effects of interface roughness scattering at higher gate voltages.

Before proceeding with a discussion of several problems with the C-face regarding oxide breakdown and long-term oxide reliability, we present results in Fig. 1.8 for p-channel lateral MOSFETs fabricated using epitaxial layers doped with nitrogen at $8x10^{15}$ cm^{-3}. Trap densities near the 4H band edges are shown together with the effective carrier (hole) mobility in the inversion channel. A maximum effective hole mobility of 8 cm^2/V-s was measured. This value decreased to approximately 7 cm^2/V-s (data not shown) for lateral devices with implanted wells ($3x10^{15}$ cm^{-3} Al-doped epi with a box nitrogen implant of $5x10^{16}$ cm^{-3}). The implanted n-wells and the p^+ source/drain contacts were activated at 1650 °C.

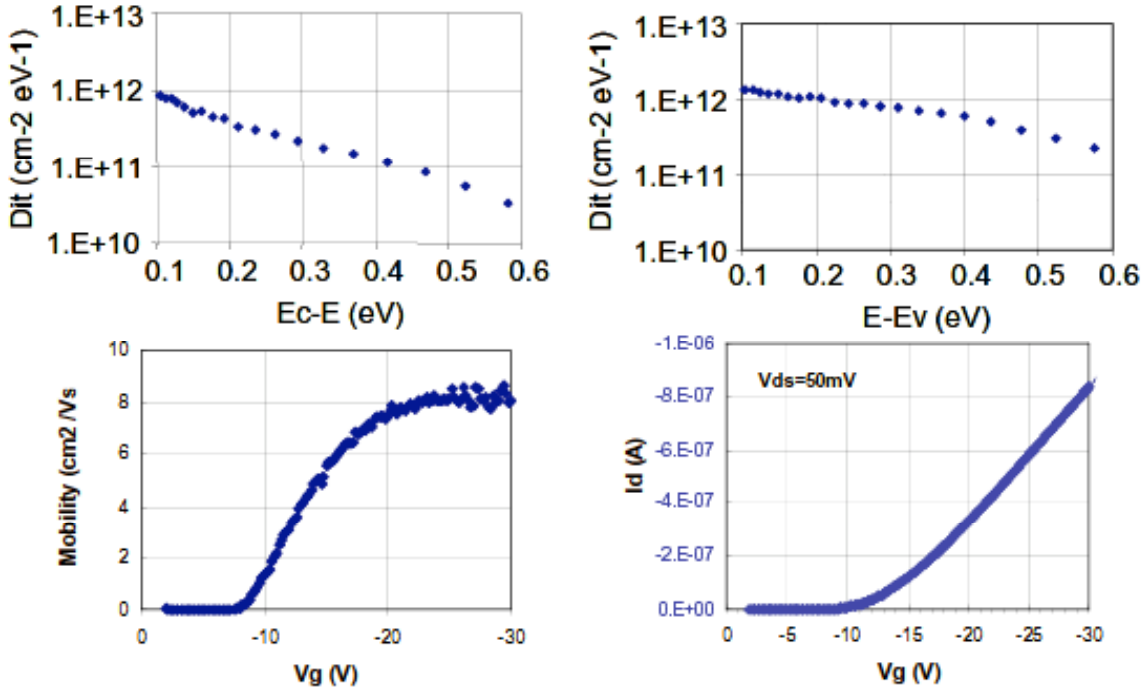


Fig. 1.8. Top – Interface densities near the 4H-SiC band edges. Bottom – Effective channel mobility and I_d-V_g characteristics for an epitaxial p-channel lateral MOSFET.

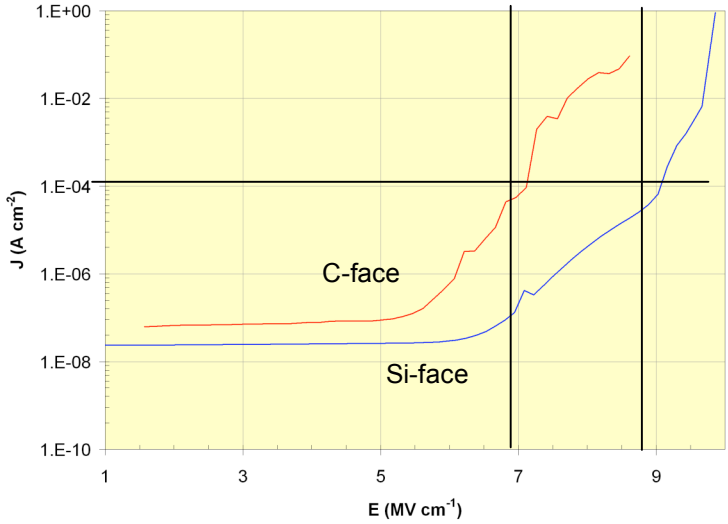


Fig. 1.9. I-V characteristics for oxides on (000-1) and (0001) 4H-SiC epilayers with doping of ~$1x10^{16}cm^{-2}$.

1.4. Oxide reliability

1.4.1 Breakdown characteristics of oxides grown on (000-1) C-face

As discussed in the previous section channel mobility and threshold voltage are acceptable for (000-1) MOSFETs or IGBTs. However, as shown in Fig. 1.9, the oxide breakdown characteristics are significantly worse for the C-face. Comparing the C- and Si-faces for an oxide current density of $1x10^{-4}A/cm^2$, one sees that the field supported by the (000-1) oxide is almost 2 MV/cm lower. The lower breakdown field for the C-face was observed consistently for oxides grown in different ambients (dry O_2 and dry O_2 + HCl) with and without NO passivation [Fig. 1.10 (left)]. As shown in Fig. 1.10 (right), for the (0001) Si-face post-oxidation Pt deposition prior to H_2 annealing (which improves mobility by 25%) damages the oxide and leads to significantly lower breakdown fields. The 'NO only' sample had Mo gate contacts. The detrimental effect on breakdown field is the same following Pt deposition, whether the sample is annealed in H_2 or Ar. Considering the lower breakdown fields measured generally for the C-face and the effects of Pt, we did not perform I-V measurements for (000-1) samples passivated with NO + Pt + H_2.

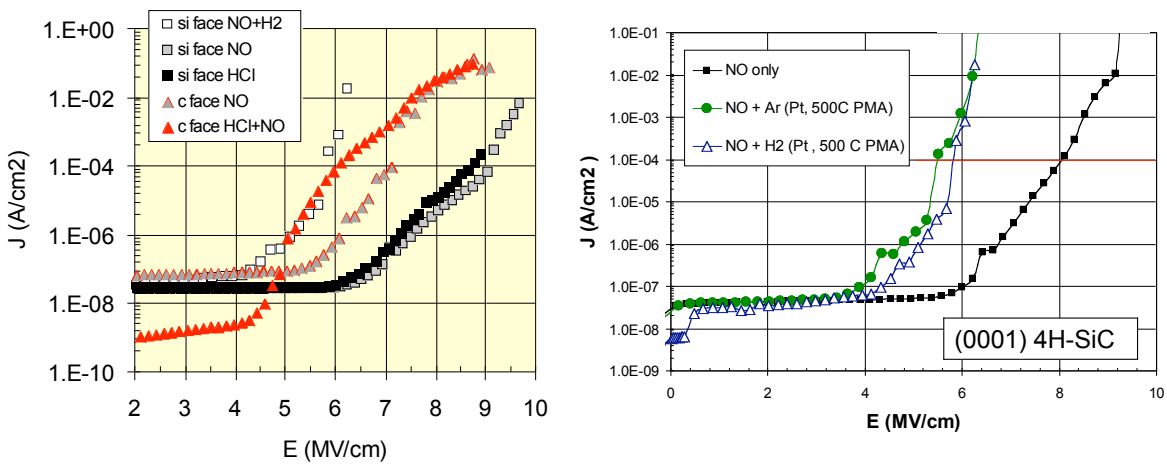


Fig. 1.10. Left – Current-voltage characteristics for (000-1) and (0001) oxides under various growth and passivation conditions. For a given current density, consistently lower fields were measured for the C-face. Right – Oxide damage during Pt deposition prior to hydrogen annealing.

The Fowler-Nordheim (F-N) injection phenomenon is a one of the most important intrinsic oxide degradation mechanism for MOS devices. For this mechanism, the electric field in the oxide results in an emission of carriers from the semiconductor into the oxide or from the gate metal into the oxide. The F-N current J can be expressed as:

$J = AE_{ox}^{2} e^{-\frac{B}{E_{ox}}}$ where E is the field in the oxide; $A \propto \frac{1}{\phi_{FN}}$ and $B \propto \phi_{FN}^{3/2}$ where ϕ_{FN} is the effective barrier height for F-N tunneling. At room temperature, the theoretical value of this barrier for 4H-SiC is ~ 2.7 eV, which is basically the offset between the conduction

bands of 4H-SiC and SiO_2. ϕ_{FN} (at room temperature) has been extracted from I-V measurements as a function of crystal orientation (Si-face and C-face) and interface passivation (with and without NO). The results are shown in Fig. 1.11. For the Si-face, ϕ_{FN} was found to be very close to the theoretical value of 2.7 eV, independent of the NO treatment. On the other hand, for the C-face, the effective barrier was found to be significantly lower (~1.5 eV and 0.4 eV with and without NO, respectively). For the unpassivated C-face sample, a clear F-N regime was not detected, so the result shown here is our estimation of the barrier assuming F-N tunneling applies. *The lower ϕ_{FN} for the (000-1) interface indeed correlates with the lower breakdown strength of these oxides.* A reason for the lower ϕ_{FN} could be the higher amounts of traps in the near-interfacial oxide that lead to severe trap assisted tunneling (consistent with CV measurement results presented previously). Another reason for the apparent lower barrier could be a non-uniform charge distribution in the oxide. This would result in a range of electric fields in the oxide at the same gate bias. As a consequence, some parts of the oxide would experience much higher electric fields, resulting in an inaccurate barrier extraction.

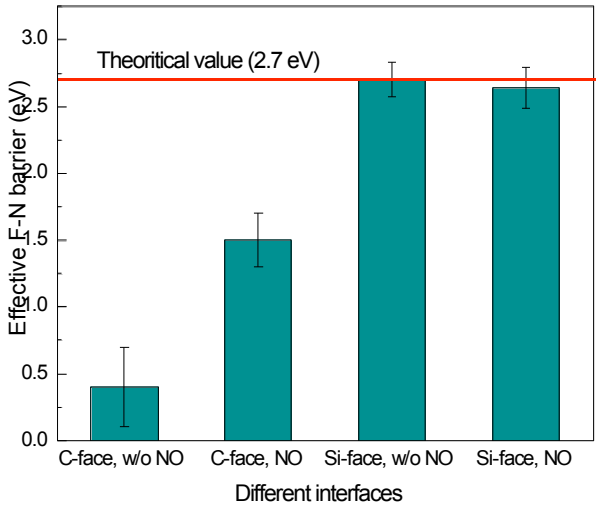


Fig. 1.11. Effective Fowler Nordheim tunneling barriers as a function of 4H-SiC crystal orientation and SiO_2/SiC interface treatment. Note that the error bars are the standard deviation from measurements made on different capacitors, except for the unpassivated C-face where the error bar is calculated from a spread in flat band voltages.

We suspect that the lower breakdown strengths are associated with the higher interface defect densities or with poor C-face wafer quality. Trace amounts of carbon in the bulk of the SiO_2 could also have a detrimental effect on dielectric strength. In general, it is well accepted that the bulk of SiO_2 is 'carbon free' and the presence of excess carbon has only been observed in the interfacial/near- interfacial regions. However, most measurements have been performed on the Si-face, which has a significantly lower oxidation rate than the C-face. Furthermore, the concentration and/or total amount of C is lower than the detection limits of most physical analysis techniques. Previous results with

ion scattering have set a limit for the interfacial C content at ~10^{15} atoms cm^{-2}, and the C concentration in bulk of the oxide was lower than the sensitivity of the technique (~10^{15} cm^{-2}).

In turn, secondary ion mass spectrometry (SIMS) is not sensitive to interfacial C for the SiO_2/SiC system, but has a very high sensitivity to trace concentrations of C in the SiO_2. We used SIMS to obtain depth profiles of carbon in the oxide for both Si-face and C-face samples. The detection limit for C analysis was 10^{19} cm^{-3} (corresponds to 5 x 10^{13} cm^{-2} for a 50 nm oxide with uniform C distribution). The average carbon concentrations for the various samples are shown in Table 1.1. The results indicate approximately equal concentrations of C for NO-annealed C-face and Si-face samples. The as-oxidized C-face sample shows about a factor of two lower C concentrations. However, it should be borne in mind that such a small difference can arise from various experimental factors such as background carbon in the SIMS chamber, ion induced carbon deposition, pin holes in the oxide etc. Therefore, at this stage, *we think that to first order there is no correlation between oxide breakdown and carbon concentrations in the bulk of the oxide*. The SIMS experiment indeed sets a new upper limit of $\leq$ 2 x 10^{20} cm^{-3} for C concentration in the bulk of SiO_2.

Table 1.1. Carbon concentrations in SiO_2 on 4H-SiC. Data shown here are the averages of mid-point oxide concentrations from several measurements.

Sample	Oxide thickness (nm)	Ave. C conc. in oxide (atoms cm^{-3})
C-face, oxidation only	48	6.34E+19
C-face, oxidation + NO anneal	56	1.30E+20
Si-face, oxidation + NO anneal	56	1.62E+20

1.4.2 Time dependent dielectric breakdown (TDDB)

The measurement system shown in Fig. 1.12 was developed for TDDB (time dependent dielectric breakdown) measurements at Auburn to study long-term oxide reliability. A probe card was used to connect 36 MOS capacitors on a 1cm x 1cm sample to the measurement system. The MOS capacitors were monitored continuously one after the other, and an individual device was removed from the measurement sequence and its time of removal was recorded if its leakage current density exceed a preset value (normally 88mA/cm^2) for each of three consecutive measurements. A second TDDB system with similar features has recently come online at Vanderbilt.

The structure of an individual TDDB MOS capacitor is shown in Fig. 1.13. Thin gate oxides (~ 60nm) were grown and passivated after windows were opened in the thick deposited field oxide. Following the TDDB measurements, the 600 micron diameter metal gate contacts were used as an RIE etch mask to define mesas in the SiC epilayer. The sample was the etched in KOH, and the center 150 micron diameter area of the 600 micron diameter mesa was examined for defects and evidence of damage due to oxide breakdown.

Results are shown in Fig. 1.14 for an oxide passivated with NO grown on an (000-1) n-epilayer doped at approximately $8x10^{15}cm^{-3}$. The intrinsic populations in the failure distributions are represented by the straight lines. These distributions were renormalized and used to determine the MTTF values (mean time to failure) that are plotted. As can be seen, the projected lifetime for operation at 145C with an oxide field of 2MV/cm is only 9 months. This value may be compared to the results shown in Fig. 1.15 for an n^- (0001) epilayer where the projected lifetime for operation at 145 °C and 2 MV/cm is around 3000 yr. *Therefore, although (000-1) C-face MOS devices offer higher threshold voltage and comparable channel mobility in comparison to Si-face,*

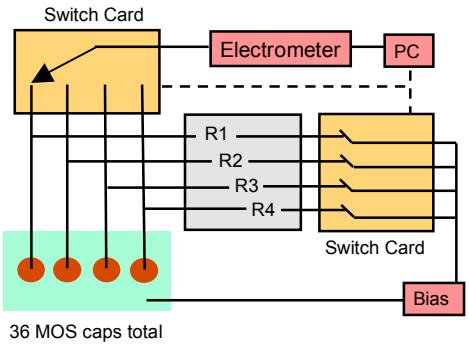


Fig. 1.12. TDDB measurement system. MOS capacitor current is determined by measuring the voltage drop across a known precision resistor.

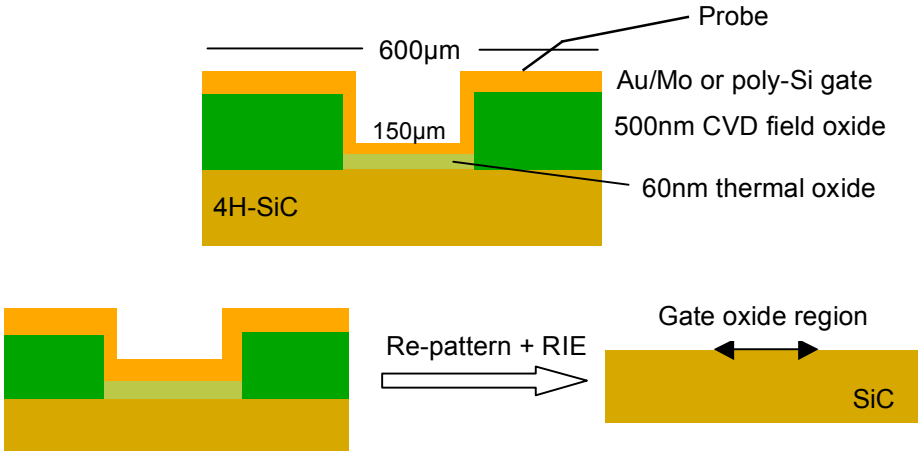


Fig. 1.13. Top - MOS capacitor structure for TDDB measurements. Bottom – Preparation of MOS capacitor for KOH etching following TDDB testing.

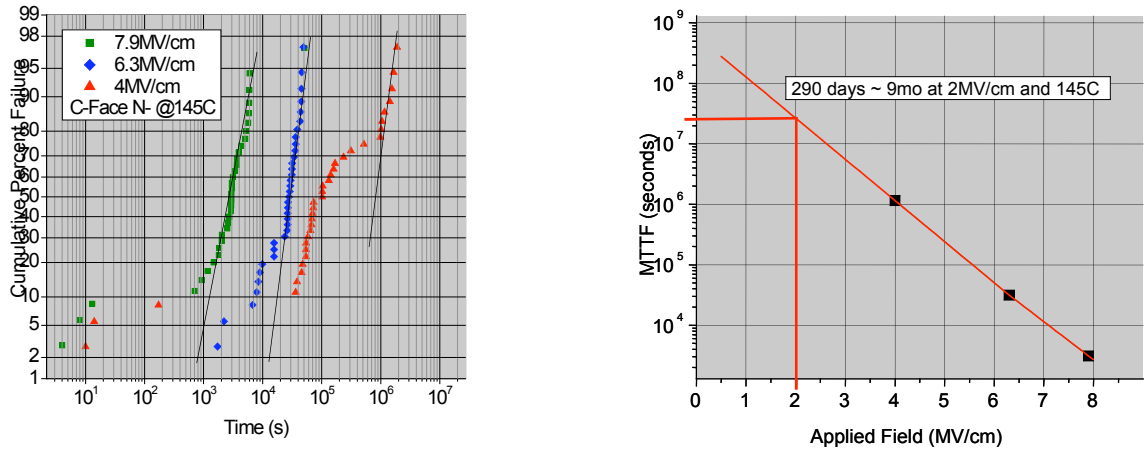


Fig. 1.14. Results of TDDB measurements for oxides grown on n⁻ (000-1) epilayers. Left – failure distribution at 145C. Right – Mean Time To Failure as a function of oxide field strength.

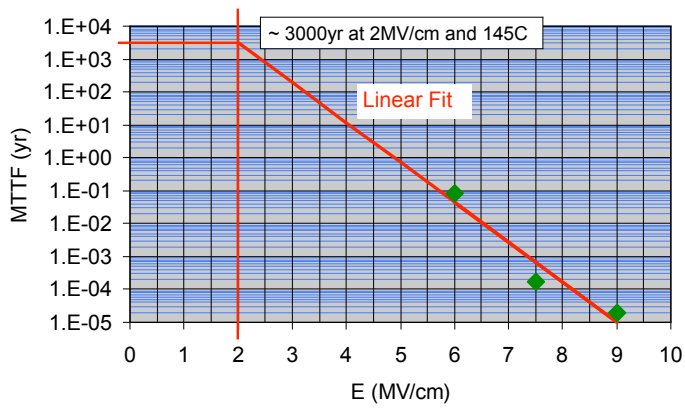


Fig. 1.15. Mean Time to Failure as a function of oxide field strength for oxides grown on (0001) n⁻ epilayers. These results can be compared to those of Fig. 1.14 for (000-1) MOS capacitors.

at this stage, their application to power MOSFETs and IGBTs are seriously limited by the lower breakdown field and the lower average oxide lifetime.

The results of KOH etching following TDDB measurements are shown in Fig. 1.16 for C-face and Si-face MOS capacitors. The features present for the (000-1) MOS capacitor are not material defects but are instead an artifact of the way that the C-face is etched by KOH. These artifacts precluded further etching of (000-1) TDDB MOS capacitors in an effort to correlate breakdown time with defect number. This experiment was however successful for the (0001) Si-face. Fig. 1.17 shows results following KOH etching (500C, 30min) of a (0001) Si face TDDB sample with *in situ* boron doped poly-Si gate. Results for 36 etched MOS capacitors are summarized in the table in Fig. 1.16. Thirty-two TEDs (threading edge dislocation) along with 28 other defects of an unknown type were identified. Interestingly, all 28 of the unknown (??) defects were located on the peripheries of the MOS capacitors, while only 8 of 24 TEDs were so located – the remainder being inside the active area of the MOS capacitors. No correlation between

total number of defects and breakdown time was observed. The presence of the unidentified peripheral defects suggests that breakdown at the edge of the TDDB MOS capacitors may be playing a role. If so, the question becomes whether the integrity of the gate oxide is being correctly evaluated.

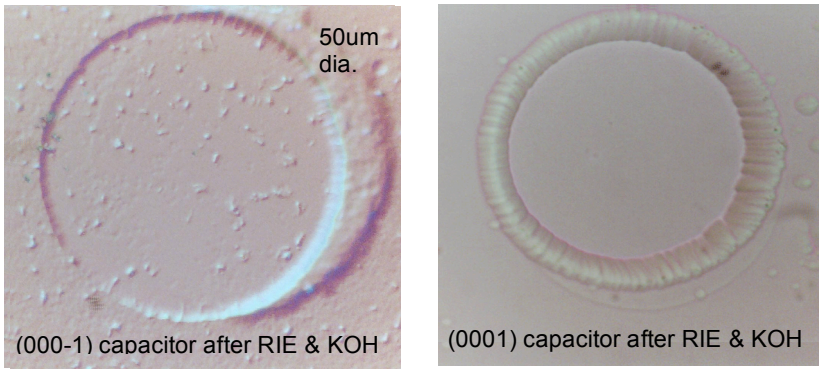
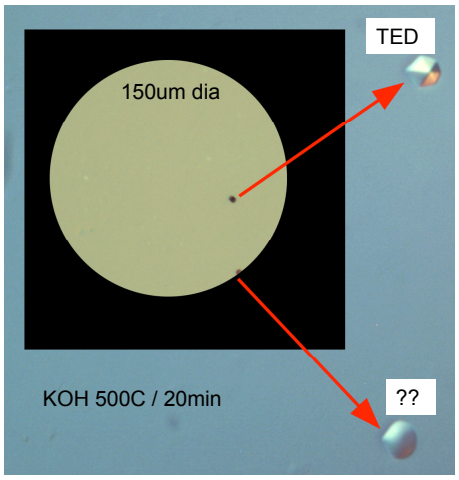


Fig. 1.16. C-face and Si-face MOS capacitors etched with KOH after RIE for mesa definition and oxide removal. The features present for the (000-1) capacitor are not material defects by rather artifacts of the KOH etching process.



Etched (0001) MOS capacitor sample	Edge		Inside	
		??	TED	??
TED				
12 @ 25um	9	3	0	0
12 @ 50um	8	2	0	2
12 @ 150um	11	3	0	22

Fig. 1.17. KOH etching results for 150 micron diameter n^- (0001) MOS capacitors following TDDB testing. ?? represents an unknown material defect type. TEDs (threading edge dislocations) are also identified.

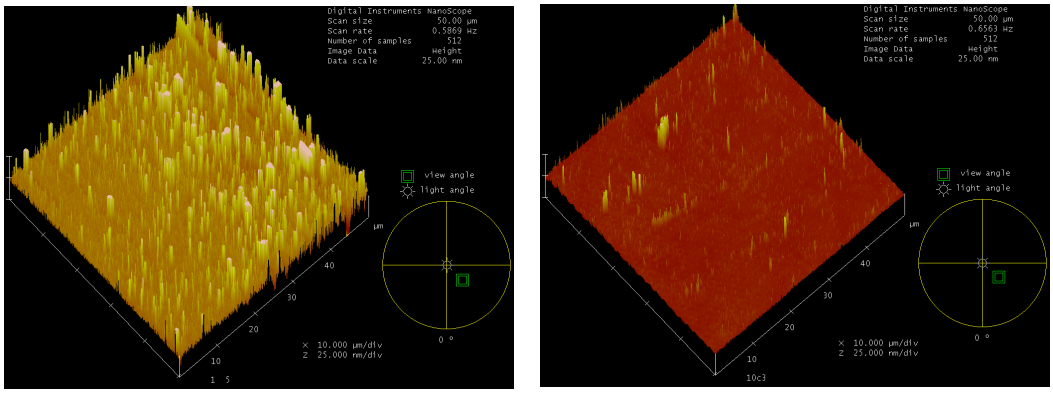
1.4.3 Surface morphology control after post-implantation annealing in relation to oxide reliability

Roughness introduced on SiC surfaces by reconstruction during implantation and activation annealing is an important issue for oxide breakdown and reliability. We have evaluated two independent approaches to obtain smooth surfaces with regards to oxide reliability: (A) Surface 'capping' with graphitic carbon over-layer during annealing and (B) Chemical mechanical polishing (CMP) of surfaces after post-oxidation annealing and before oxidation. Some of the main results will be presented in this sub-section.

(A) Carbon cap process.

AFM scans made on typical C-face samples annealed with and without carbon capping are shown in Fig. 1.18. The data indicate that the use of a C-cap results in significant improvement of the surface morphology. The AFM measurements were supplemented with ion channeling measurements, to determine the surface stoichiometry of samples that undergo activation annealing. In order to increase our surface sensitivity in these experiments, we used grazing angle ion detection geometry. Surface and/or near surface silicon and carbon which is amorphous or reconstructed due to the extreme annealing temperatures can be detected with monolayer sensitivity. Carbon areal density as a function of implantation dose and capping condition is shown in Fig. 1.19. The results show an increase in amount surface C with increasing dose for samples annealed without a C-cap. On the other hand, samples annealed with a C-cap have similar C areal density as that of virgin epilayers. This result suggests that implementing the C-cap process not only preserves morphology but the surface stoichiometry as well.

WITHOUT C- CAP **WITH C- CAP**



R.M.S roughness ~4. 33 nm R.M.S roughness ~ 1. 17 nm

Fig. 1.18. AFM measurements on C-face 4H-SiC samples implanted with 3 x 10^{15} Al cm^{-2} and annealed at 1650°C for 30 mins (left) without and (b) with a carbon capping layer. The scans are 50 µm x 50 µm and the height scale is 25 nm. AFM scans on the 'C-cap' sample have been made after removal of the cap.

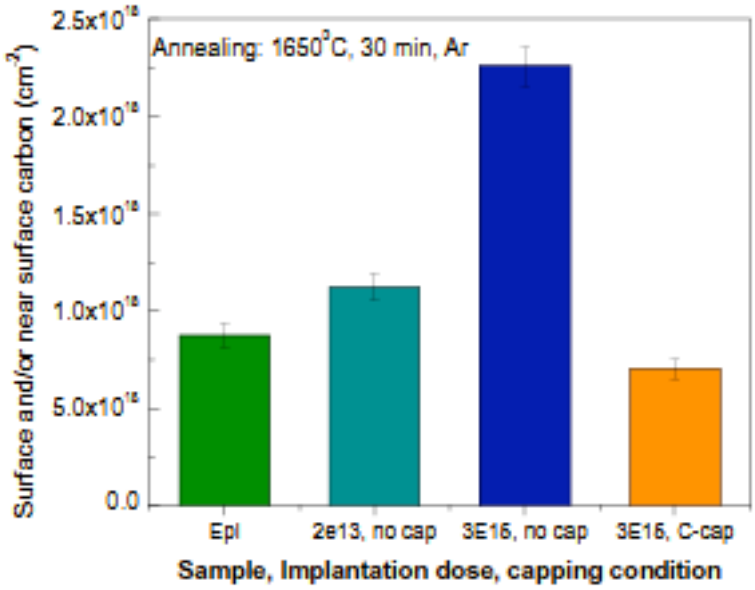


Fig. 1. 19. Surface carbon as a function of implantation dose and capping condition measured by ion channeling. Comparison of the 'C-cap' sample (orange) and the virgin epilayer (green) with the 'no cap' samples (teal and blue) reveal that the C-cap method effectively preserves the surface stoichiometry during the activation anneals.

(B) Post-implantation chemical mechanical polishing.

A new approach to alleviate roughness problems was undertaken by using "touch polishing" based on a patented NovaSiC chemo-mechanical process. This process was evaluated only on (0001) Si-face wafers. (1 cm x 1 cm) with ~10 um epilayer were heavily implanted with N (~6 x 10^{19} cm^{-3}) to a depth of ~650 nm and annealed in an Ar ambient at 1550°C without any capping layer (conditions corresponding to a source implant for a n channel vertical device).The samples were subjected to the NovaSiC, Inc. propriety polishing process. Atomic Force Microscopy (AFM) measurements were made and compared to a control unpolished sample. Typical results are shown in Figs. 1.20 (a)-(c). The results indicate a significant improvement of surface roughness with the disappearance of step bunching and a decrease of R.M.S roughness from ~6.0 nm to between 0.5-1.7 nm. It is important to note that some non-uniformity was observed on the polished surface as shown in Fig. 1.20 (c), but overall the improvement was significant. Secondary ion mass spectroscopy (SIMS) was used to measure the true material removal by comparing the N profile of the polished and unpolished control sample (Fig. 1.21). The experimentally measured value (~ 40 nm) is very encouraging and indicates that a tight control over polishing can be obtained by this process. In order to evaluate the effect of surface morphology on oxide reliability, MOS capacitor samples were fabricated on implanted samples with different surface morphologies for TDDB measurements. NovaSiC polished samples and samples prepared using the C cap process were compared with rough (no cap, no polish) samples as well as virgin epilayers (no implant or anneal). The RMS roughness of the different samples has been tabulated in Fig. 1.22. All samples

were oxidized and annealed in NO under identical conditions to grown ~60 nm oxides. Gate metallization was performed with a Mo/Au stack and samples were fabricated as shown in Fig. 1.13. The TDDB measurements were performed at 150 °C under a constant voltage stress corresponding to an oxide field of 6.5 MV cm^{-1}. The results shown in Fig. 1.22 clearly show a significant improvement of oxide reliability with smoother surface morphology. Clearly, MOSFETs with implanted channels will have a lower reliability if the dopant activation induced roughness is not reduced by C-cap or polishing. In this study, the C-cap process was found to be most superior with regards to oxide mean time to failure. Further efforts are necessary in order to fully optimize the polishing technique, but these initial are encouraging.

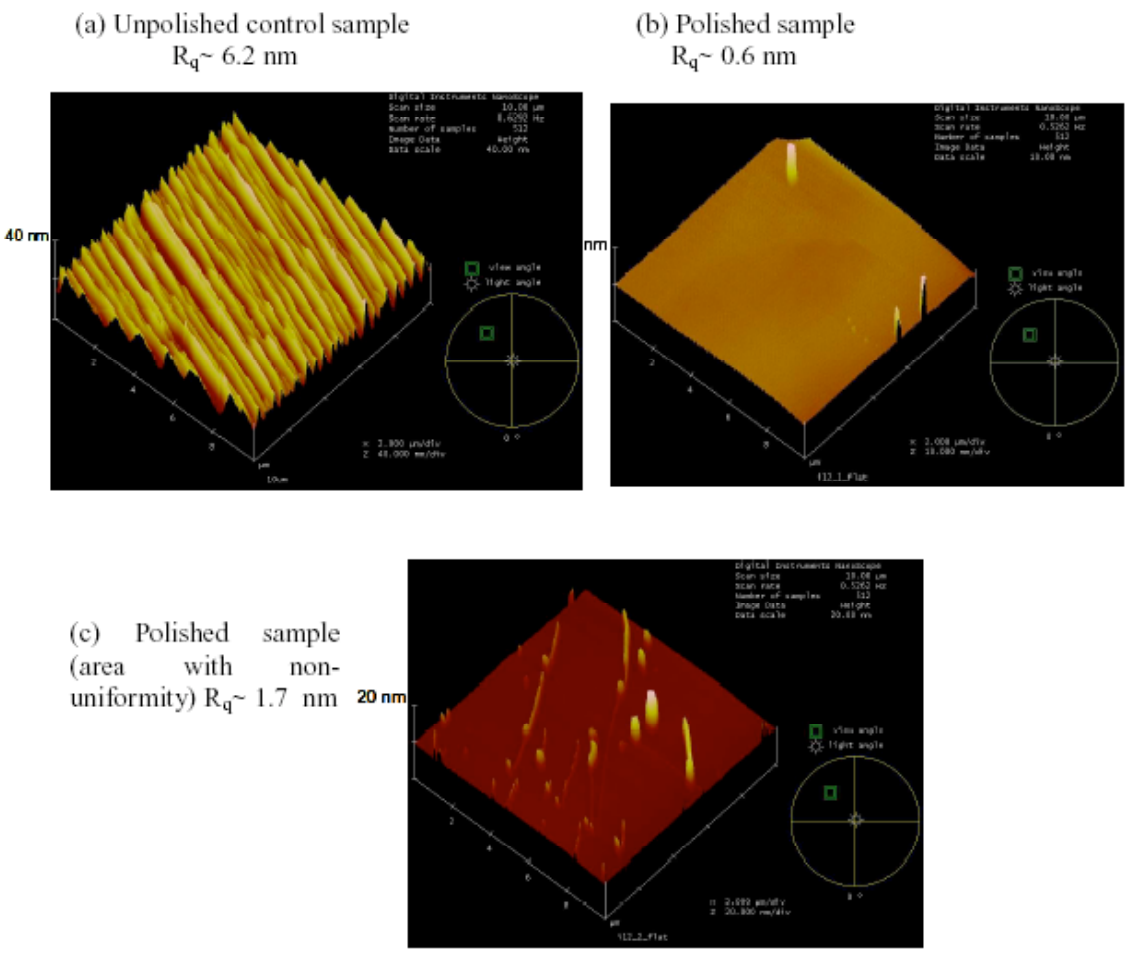


Fig. 1.20. 10 um x 10 um AFM scans on (a) unpolished control sample and (b)&(c) polished sample. N implant ~6 x 10^{19} cm^{-3}, annealed at 1550°C in Ar without graphitic cap.

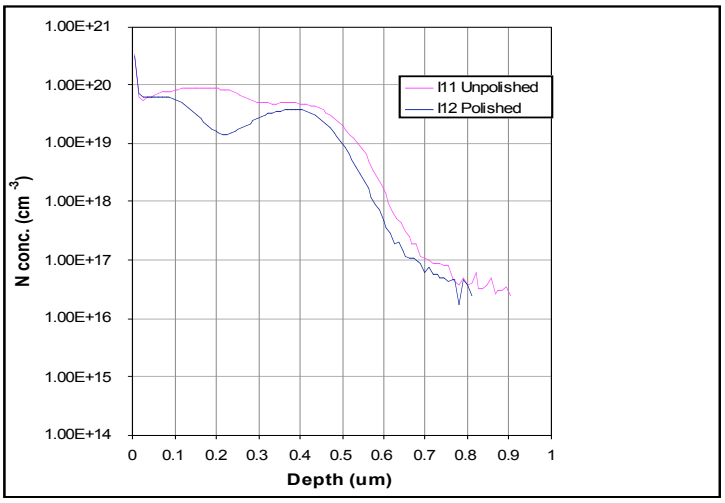


Fig. 1.21. SIMS profile of implanted N for polished and unpolished samples. The difference ~40 nm between the N depths corresponds to the amount of material removed by the polishing.

	Doping	Process	RMS rough ness
Virgin	n^- epi 10^{16} cm^{-3}	No implant, no polish	0.6 nm
Rough	n^+ implant 10^{19} cm^{-3}	1550°C anneal	6.0 nm
C-cap	n^+ implant 10^{19} cm^{-3}	1550°C anneal Carbon cap	0.6 nm
Polished	n^+ implant 10^{19} cm^{-3}	1550°C anneal NovaSiC	~ 0.6-2.0 nm

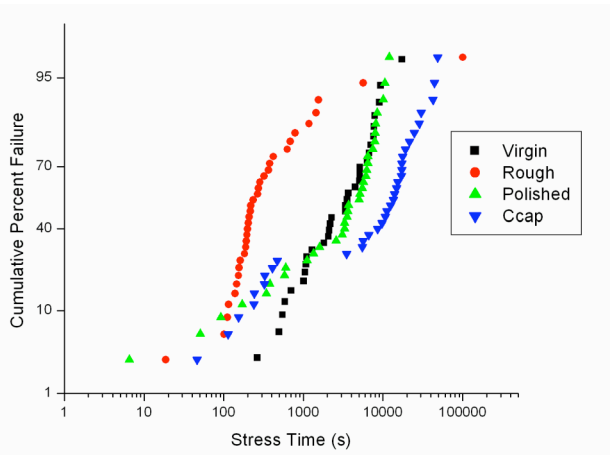


Fig. 1.22. Impact of surface morphology on oxide TDDB characteristics.

1.5. Charge injection and trapping studies

It is known that long term degradation of gate oxides and threshold voltage stability is strongly correlated to charge deposition in the insulating oxide over a period of time. Charge accumulation in the oxide occurs via trapping of electrons and holes at pre-existing trap sites located in the bulk and near-interfacial regions of the oxide as well as by the creation of new traps during charge injection. We have investigated charge injection and trapping in as-grown and nitrided oxides formed on the (0001) Si-face of n-4H-SiC using three charge injection schemes to isolate the effects of injected electrons and holes. The three schemes are ionizing radiation (oxide exposed to both electron and holes), photo-injection of electrons (oxide exposed primarily to electrons) and Fowler-Nordheim tunneling of holes (oxide exposed primarily to holes). *The conclusive picture*

that has emerged from these studies is that while nitrided SiO_2/4H-SiC interface are quite robust against electron injection, they are significantly more susceptible to positive charge buildup when subjected to hole injection.

(A) Effect of ionizing radiation: Please refer to Appendix A.

(B) Photo-injection of electrons and Fowler-Nordheim tunneling of holes.

For these experiments, dry oxidation was performed at 1150 °C with n-4H-SiC (0001) epi-layers doped at $5x10^{15}$ cm^{-3}. Post-oxidation passivation was performed at 1150 °C for 30 min in Ar for some samples (as-oxidized) and for 2hr in NO at 1175 °C for other samples (nitrided). Capacitors were fabricated with thin, evaporated Al gate contacts of less than 35nm thickness to facilitate photo-injection. Injection of electrons from the metal was performed using a focused 100W Hg lamp at fields between -3 and -5 MV/cm, with an injection current of around 1μA/cm^2. A diagram of the experiment is shown in Fig. 1.23 (left). At these fields, we suspect that there might be a background inversion hole current flowing from the semiconductor towards the gate. However, this current is estimated to be no more than 10% of the total current.

For F-N hole tunneling, holes were injected from the valence band of the semiconductor as shown in Fig. 1.23 (right). In this case, the oxide electric field was between -4 and -6 MV/cm with an injection current of around 0.1 μA/cm^2. The system was kept in inversion using a low intensity handheld UV lamp. For both injection schemes, 'effective' charge buildup in the oxide was determined as a function of injected charge dose by monitoring flat-band voltage shifts. Results for the photo-injection experiments shown in Fig. 1.24 indicate a significantly higher amount of electron trapping in the as-oxidized samples compared to the nitrided samples. For the as-oxidized samples, rate equations and photo-CV results indicate that 90% of the injected charge is confined at the interface/near-interface region. The cross section related to these traps charge was estimated to be ~2.5 x 10^{-17} cm^2, in agreement with previous reports attributing this negative buildup to the formation of slow acceptor-like interface states. A markedly different behavior is observed for the nitrided samples where the negative charge buildup is significantly lower. Electron trapping occurs almost entirely in the bulk of the oxide with negligible buildup of the slow acceptor-like interface states observed for the as-oxidized sample. For a detailed discussion of these results please refer to Appendix B.

On the other hand, F-N tunneling of holes under inversion biasing in these devices shows a markedly different behavior as shown in Fig. 1.25. A significantly higher buildup of positive charge is observed for the nitrided samples. Unlike the results from the photo-injection experiments, these curves could not be analyzed with a rate equation because of both limited data and the apparent absence of saturation of the positive charge in the nitrided sample at the injection levels investigated. Therefore, a clear separation between bulk and interface contributions could not be extracted. However, the evolution of the photo-CV hysteresis (not shown) reveals an increase of interface states during injection (similar to the effect of electron injection in as-oxidized samples). Also, a portion of the excess positive charge seemed to be removed by the tunneling of electrons

from the substrate which is a strong indication that this part of the charge resides in near-interface oxide traps.

We attribute the enhanced positive charge trapping at nitrided interfaces to the atomic scale configuration of N in the near-interfacial region of the oxide. Recent theoretical calculations suggest that it is energetically favorable for nitrogen atoms (incorporated via NO annealing) to replace threefold coordinated C or Si atoms (i.e., dangling bonds) and remove trap levels associated with these defects [S. Wang, et al., *Phys. Rev. Lett.* **98**(2) (2007) 026101]. As a result, nitrogen is effective for passivation of C and Si dangling bonds with a variety of back-bond configurations. However, the threefold coordinated N formed as a result of such passivation reactions induces an energy level in the gap about 0.5 eV above the valence band edge due to its lone pair state when N has Si-N or C-N back-bonds. When N has O-N backbonds, there are no states in the gap. The N lone pair state predicted by theory is a hole trapping center which could account for the severe hole trapping observed in our charge injection experiments. (For a more detailed discussion, please refer to Appendix A.).

In conclusion, these charge injection experiments strongly indicate that as far as charge trapping in the near-interfacial region and interface trap creation is concerned, as-oxidized samples are more sensitive to electron injection whereas nitrided oxides are more sensitive to hole injection. It is important to evaluate the impact of the enhanced hole trapping effect in nitrided oxides from the point of view of power device operation.

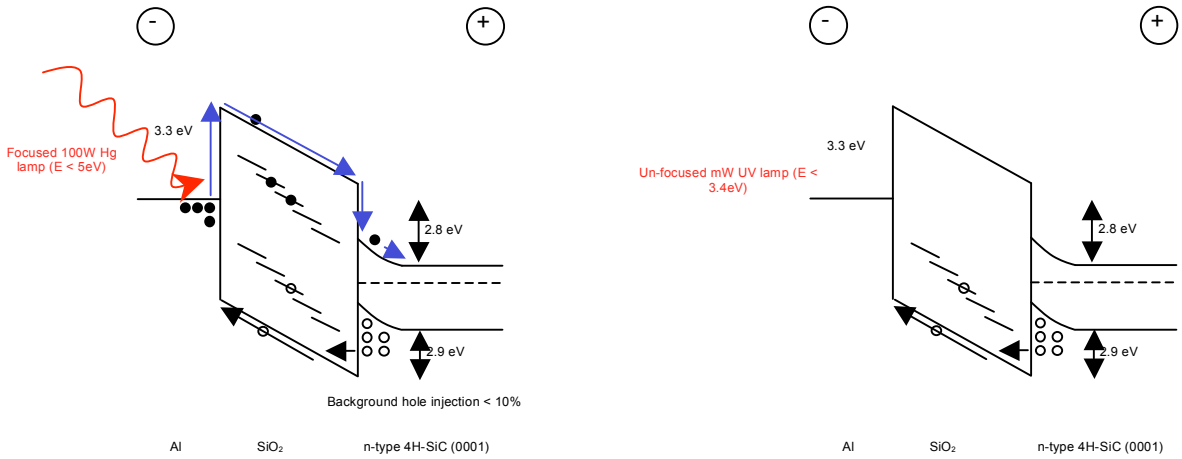


Fig. 1.23. Diagrams for (left) Photo-injection of electrons and (right) F-N tunneling of holes into the oxide layer of SiO_2/n-4H-SiC MOS structures.

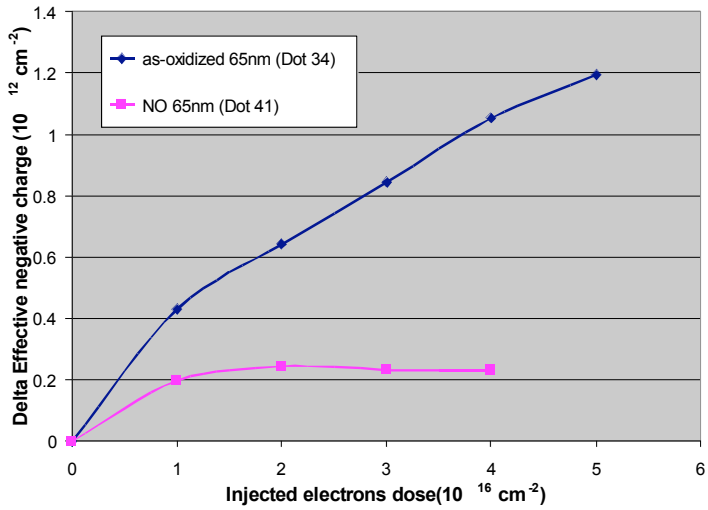


Fig. 1.24. Electron photo-injection results showing the buildup of effective negative charge as a function of photo injected electron dose in as-oxidized and nitrided SiO_2/n-4H MOS capacitors.

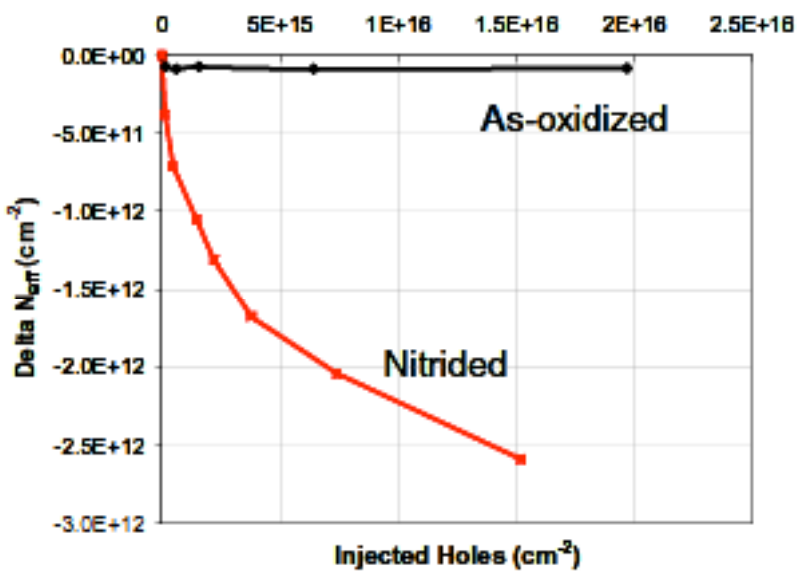


Fig. 1.25. Buildup of effective positive charge by F-N hole tunneling in as-oxidized and nitrided SiO_2/n-type 4H-SiC MOS capacitors under inversion.

1.6. Temperature and bias instability

The effects of temperature and bias are shown in Figs. 1.26 and 1.27 for n-4H MOS capacitors passivated with NO. In accumulation (positive gate bias), field stressing alone (~ 4 MV/cm) does not produce much of an instability in the flatband voltage (Fig. 1.26). However, positive bias stress at temperature does produce a significant threshold voltage shift that is consistent with the injection of negative charge into the oxide. The flatband

voltage shift of approximately 0.8 V that is observed in Fig. 1.26 is significantly larger than the 0.1 V set initially as goal in our program. However, the shift appears to saturate for a given field strength and temperature, although testing for longer times should be carried out to demonstrate conclusively that this is the case. Nevertheless, the shift is less than value of 1 V that is allowed for power devices that frequently tested under the following conditions: V_g = 20 V, T = 150 °C, Time = 10^3 hr.

Figure 1.27 shows results for the MOS capacitors from Fig.1. 26 subjected to depletion biasing (without inversion). Little effect is observed for field stressing only. Field plus temperature stressing appears to remove injected electrons; however, the process is slow.

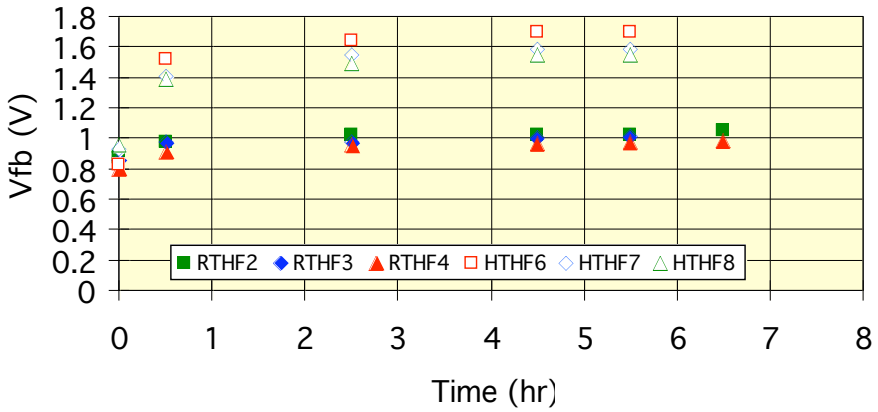


Fig. 1.26. Positive bias-temperature stress for n-4H MOS capacitors passivated with NO. t_{ox} ~ 60nm. RT = room temperature, HT = high temperature (250C), HF = high field (4 MV/cm).

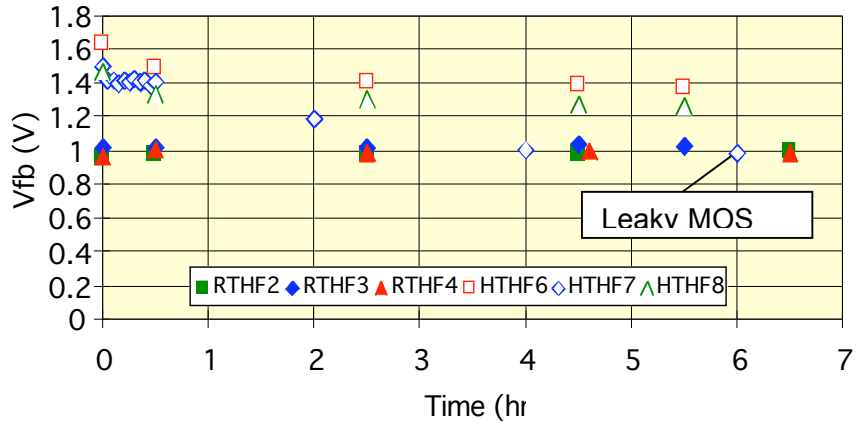


Fig. 1.27. Negative bias-temperature stress for n-4H MOS capacitors passivated with NO. t_{ox} ~ 60nm. RT = room temperature, HT = high temperature (250 °C), HF = high field (-1.25 x accumulation bias).

1.7. Summary of Task I

The main findings from the work carried out as a part of Task I are listed below:

(i) Devices on (000-1) C-face of 4H-SiC:

- C-face MOSFETs present a unique advantage over conventional Si-face MOSFETs with respect to channel mobility and threshold voltage. After nitridation effective mobility of C-face MOSFETS is comparable to the Si-face, but the threshold voltage (V_{TH}) is substantially higher (~ +3V for ~ 60 nm nitrided oxides).

(ii) Oxide reliability (breakdown and stability)

- Oxides grown on C-face have poor reliability compared to oxides on the Si-face. After nitridation, reliability improves, but breakdown strength and lifetime are still much inferior compared to the Si-face. This seriously limits the application of C-face 4H-SiC to power MOSFETs and IGBTs in spite of the advantage with regards to threshold voltage.
- Projected oxide lifetime on the Si-face was found to be acceptable for power device application.
- For implanted SiC, improving surface morphology by employing graphitic caps or post-implantation polishing improves the reliability of oxides grown on the implanted layer.
- Charge injection and trapping studies indicate that nitrided SiO_2/4H-SiC interface are quite robust against electron injection but they are significantly more susceptible to positive charge buildup when subjected to hole injection.
- Flatband voltage shifts introduced by bias/temperature stressing were found to be substantially higher than the shifts set initially in the program goals. These instabilities, in part, may be associated with mobile ion contamination and therefore, not 'intrinsic' to the oxide. Although the instabilities are large, they are within the limits of the values allowed for commercial power devices (delta V_{th} < 1V after 1000 hr with V_g = 20 V and T = 150 ^oC).

2: Growth of Thick Blocking Layers with Long Lifetime and No V_F Drift

M. A. Capano, Purdue University
M. Skowronski, Carnegie Mellon University

2.1 Activities at Purdue University (M. A. Capano)

2.1.1 Epitaxial Growth of SiC by Chemical Vapor Deposition (CVD)

In this section, a detailed discussion of SiC epitaxial growth by CVD technique will be given. First, different SiC CVD reactor designs will be reviewed followed by a general discussion of SiC CVD growth process. Then, the theory of widely-used step-controlled epitaxy technique will be presented.

2.1.1.1 CVD reactors

Several different types of CVD reactors are available for the epitaxial growth of SiC. The cold-wall design, which used to the most common type of reactor, is now less frequently used and is replaced by the hot-wall reactor. Both types of reactors often have horizontal system configuration. Recently, vertical hot-wall reactor concept for the SiC epitaxial growth is introduced by Ellison et al. [52], and is also called the "chimney reactor". Some basic concepts for each type of CVD reactors will be presented next.

*Horizontal cold-wall reactor*s are the first kind of CVD reactors for SiC epitaxial growth, which were originally converted from conventional CVD reactors. The schematic drawing of this kind of reactor is shown in Fig. 2.1. High purity graphite susceptors are heated up to the growth temperature of about 1500°C by surrounding RF-coils. The source gases are introduced from one side and are heated in a stagnant layer above the graphite susceptor; thus the temperature gradient around SiC substrates becomes significantly large in the cold-wall reactor design [4]. Because of the high growth temperature, special care has to be taken to protect the quartz tube from overheating, especially on the bottom side. The thermal insulation of the susceptor is provided by graphite felt or high reflective graphite layers deposited on additional quartz tubes. The reactor quartz tube is cooled by either water or air. Therefore, the surrounding quartz tube walls are several hundred degrees cooler than substrate and susceptor, which prevent

coating on the walls of the system. Cold wall reactors have the advantages of less maintenance due to less deposition on chamber walls and lower thermal loads on substrates because of a faster heat-up and cool-down times. The major drawback of cold-wall reactors is the lack of temperature homogeneity, which becomes more important when growth on the large diameter wafers is needed. Also, a SiC-coated graphite susceptor easily sublimes owing to the large temperature gradient between the susceptor and the cold wall, which impedes long growth run. Thus, the thickness of epitaxial layer has been limited below 10 μm with a relatively low growth rate.

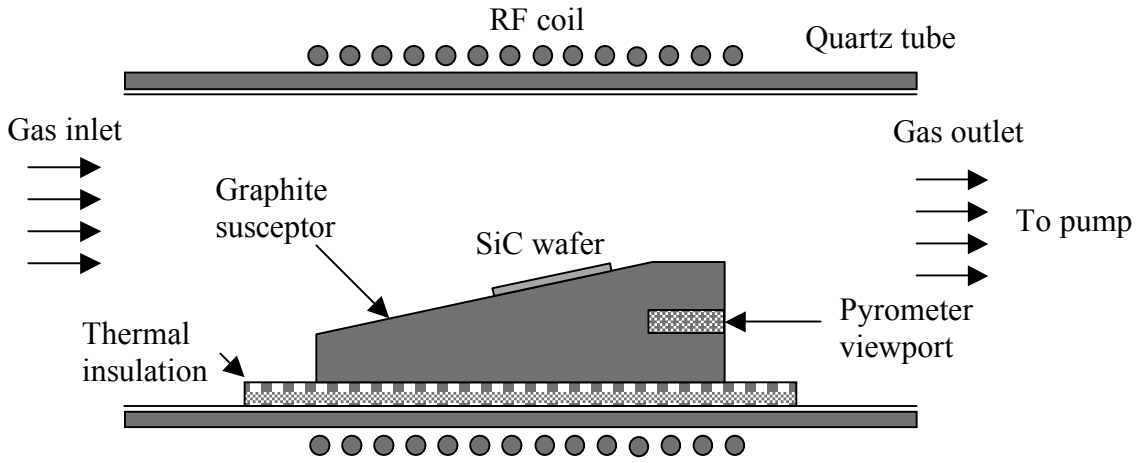


Fig. 2.1 Schematic of the horizontal cold-wall SiC CVD system

Horizontal hot-wall reactors have become increasingly popular due to the ease of obtaining high-quality epilayers. Today, the horizontal hot-wall reactor is the most advanced and developed equipment for homoepitaxial growth of SiC [23]. The schematic drawing of a horizontal hot-wall reactor is shown in Fig. 2.2. The susceptor made of high purity graphite forms an inner cell with rectangular cross section for placing the substrate wafer. The susceptor is surrounded by graphite felt for thermal insulation and placed inside an air-cooled quartz tube. The hot-wall reactor design limits the heat radiation to the entrance and exit parts of the reactor inner cell, and hence minimizes the radiation losses. It provides a large region of high temperature uniformity inside the susceptor. During the growth, source gas temperature starts to increase at the inlet of inner cell, and the gas is heated almost uniformly inside of the tunnel formed by susceptor. Therefore,

hot-wall reactors can achieve a remarkably high uniformity in both thickness and doping. Even without rotation, thickness uniformity of 1% and doping uniformity of 6% has been reported [1]. More recently, multi-wafer systems with planetary wafer rotation are introduced to produce SiC epitaxy in higher volume, and superior thickness and doping uniformity [2].

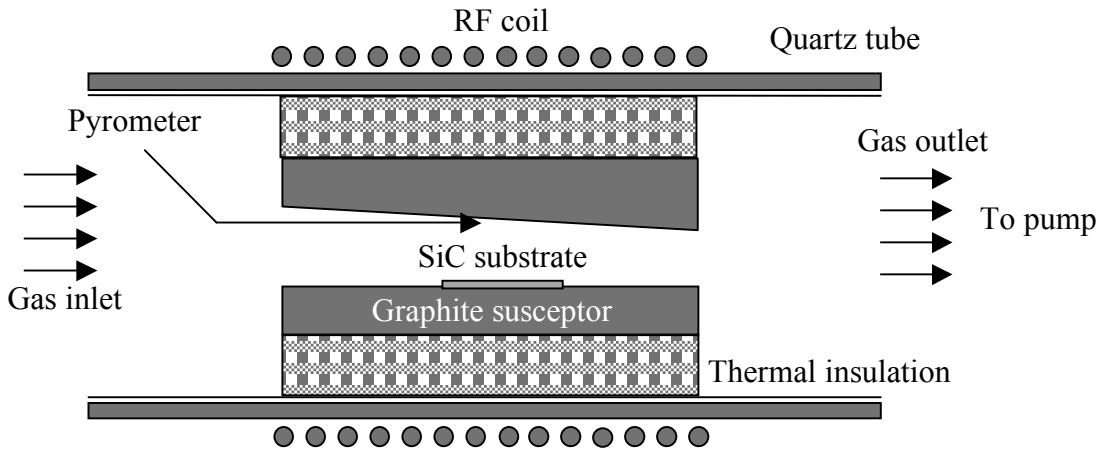


Fig. 2.2 Schematic of the horizontal hot-wall SiC CVD system

For both types of horizontal reactor configurations, the concentration of precursor gases will decrease along the flow direction due to the consumption of growth species, which is referred to as depletion. This will result in a change in growth rate and thickness non-uniformity along flow direction. To compensate for the depletion it is common to increase the flow speed along the flow direction and thus the boundary layer will be pushed downward, resulting in a shorter diffusion distance for the active species to reach the substrate [7]. In cold-wall reactors, this is achieved by tapering the graphite susceptor underneath the substrate as shown in Fig. 2.1. In hot-wall reactor, this is achieved by designing an inclined ceiling for upper piece of susceptor as shown in Fig. 2.2.

Vertical hot-wall reactor, also called chimney reactor, is a relatively new reactor design concept. Simply described, the chimney reactor is a vertical hot-wall system, where the process gases flow upwards through a hollow-shaped susceptor with internal rectangular cross-section as shown in Fig. 2.3 [53]. The symmetric temperature and gas flow distributions can be established in this reactor configuration. The vertical geometry

allows mounting the substrates along both inner walls of the channel, while minimizing thermal gradients in the vicinity of the growth region. In this configuration, the gas flow is aided by the tendency of a hot gas to rise (like in a chimney), which makes it suitable for a high temperature process (from 1650°C to 1850°C) [53]. Material transport is achieved by allowing large clusters of Si to form in the inlet region at relatively low temperatures. As the temperature increases along the flow direction, the Si clusters will thermally re-evaporate and be available for growth. Very high growth rate and outstanding purity has been achieved using this technique. Growth rate between 15-50 μm/hr and background doping in the low 10^{13} cm^{-3} have been reported [53].

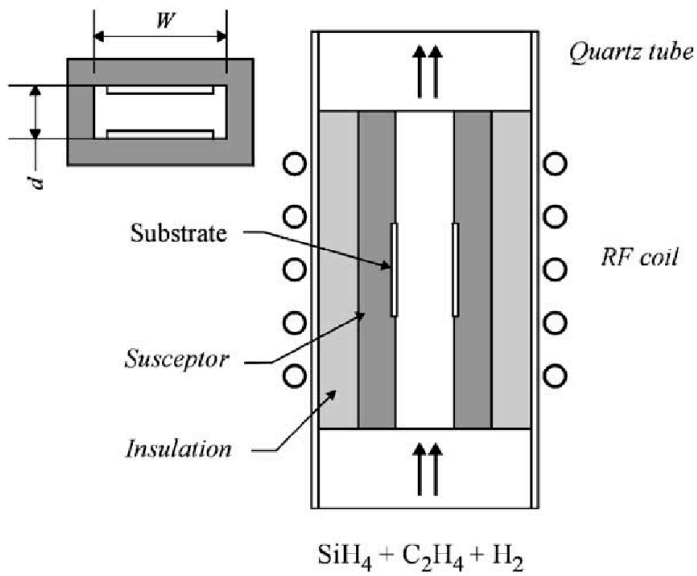


Fig. 2.3 Schematic view of the chimney CVD reactor configuration [53].

Another issue which is common for all SiC CVD reactors is the susceptor coatings. Because of the reaction between hydrogen and graphite at temperatures greater than 1300°C, susceptor coating is often used. Etching of a graphite susceptor can release B, Al and other impurities that can be incorporated into the epilayers during the growth. The release of carbon from graphite also changes the carbon to silicon ratio in the reaction environment. Besides, a bare graphite susceptor is porous and can trap dopants during a growth run, then release the dopant during a subsequent run. Thermally stable polycrystalline SiC coating is a popular solution and is still used in many reactor designs. However, SiC coating is also vulnerable to hydrogen etching at the growth temperature, which results in the shortened susceptor lifetime. Tantalum carbide (TaC) and other

carbon base coating are being investigated as an alternative to the SiC coating. More precise doping control and longer susceptor lifetime has been demonstrated by using those types of coatings [54].

2.1.1.2 SiC CVD growth in general

In SiC CVD the most common precursor gases are silane (SiH_4) and propane (C_3H_8). Hydrocarbon such as methane (CH_4) and ethane (C_2H_6) are also investigated as alternative carbon precursors. The precursor gases are diluted in a massive flow of carrier gas, which normally is hydrogen. During the growth, the precursors decompose within the hot zone of the reactor with a temperature in the range of 1550 to 1800°C and the epitaxial growth takes place on the heated substrate. The growth of SiC consists of the following basic processes [23]:

(1) Transport of the reactive gases from the inlet to the inner cell
(2) Cracking of the precursor gas molecules
(3) Diffusion of silicon and carbon containing species to the surface
(4) Adsorption of silicon and carbon containing species at the surface
(5) Desorption and evaporation of silicon and carbon from the surface
(6) Surface diffusion of adsorbed species
(7) Incorporation of adsorbed species into the growing crystal, preferably at steps or defect sites

Inside the reactor cell, the velocity of the gases is high but flow is always laminar. There will be a boundary layer (or stagnant layer) over the susceptor where the velocity gradient decreases to zero. During the growth, silane and propane will decompose and the decomposed species will diffuse through the boundary layer to grow on the substrates. The process (4), (6) and (7) are the primary SiC deposition processes, while process (5) can be considered as etching. When the deposition process dominates over the etching process, SiC epitaxial layer is grown on the substrate. The growth rate of the epilayer depends on which of the above listed processes is the limiting one, and also on the ratio of deposition rate to etch rate [23]. Both of factors are strongly dependent on the growth temperature and the supplied gas flows.

Studies on gas-phase and surface reactions of CVD process is extremely difficult to perform experimentally considering the temperature and speed of the reactions involved. Computational models have been established to facilitate both process development and reactor design [55-57]. For the SiH_4-C_3H_8-H_2 system, it has been shown

that the dominant species contributing to SiC growth were Si, SiH_2 and Si_2H_2 from SiH_4 and CH_4, C_2H_2 and C_2H_4 from C_3H_8 [56]. During the growth, Si-containing species may be preferentially absorbed and make chemical bonds with SiC substrates. Then, C-related chemical species in growth environment incorporate into the attached Si to form SiC. Therefore, no deposition will happen without the SiH_4 supply. Detailed discussion of gas-phase and surface chemistry can be found in literature and will not be discussed here.

2.1.1.3 Step-controlled epitaxy

Step-controlled epitaxy is the key technology for development of high-performance SiC devices. In this section, the growth mechanisms of step-controlled epitaxy will be presented and conditions to achieve step-flow growth will be discussed.

There are two possible growth modes in the epitaxial growth of 4H-SiC. One is two-dimensional growth, which will result in heteroepitaxy of poor-quality 3C-SiC crystal; the other is the step-flow growth, which will result in the homoepitaxy of 4H-SiC. These two growth modes compete with each other, and one of them will be favored depending on the substrate and growth conditions.

During the growth, the precursors will be decomposed and diffuse to the substrate surface. On well-oriented or small off-cut angle substrates, terrace length is long and step density is low, as shown in Fig. 2.4 (a). Crystal growth may initially occur on terraces through two-dimensional nucleation if there is a high superstauration on the surface. The (0001) crystal planes of hexagonal SiC are crystallographically equivalent to the (111) plane of 3C-SiC, and therefore the two-dimensional nucleation of 3C on those planes are perfectly lattice matched to the substrate. Also, it is believed that certain metastable phase of 3C-SiC has a lower surface energy and therefore a higher probability of spontaneous nucleation, especially at low growth temperature [58]. This is why a temperature as high as 1800°C is often required for on-axis growth of hexagonal SiC polytype, such as 6H-SiC, otherwise twinned crystalline 3C-SiC will grow [6].

On the contrary, the surface on off-axis substrates has a high step density and a narrower terrace length, as illustrated in Fig. 2.4(b). Hence, the absorbed chemical species have diffusion length long enough to reach steps and incorporate into crystal at steps. Since the incorporation sites at the steps are uniquely determined by the stacking sequence of the substrate, the same polytype as that of the substrate can be grown through the step-flow growth. By introducing steps on substrates, the polytypes of SiC epilayers can be controlled and the vertical growth of the epilayer is achieved by the horizontal

flow of the steps. This is why it is called “step-controlled epitaxy”. Although the technique of epitaxial growth on off-axial substrates also has been used for many other materials, the application of this technique on SiC has some special significance in that the high quality epilayer with stable polytype can be grown at reduced temperature.

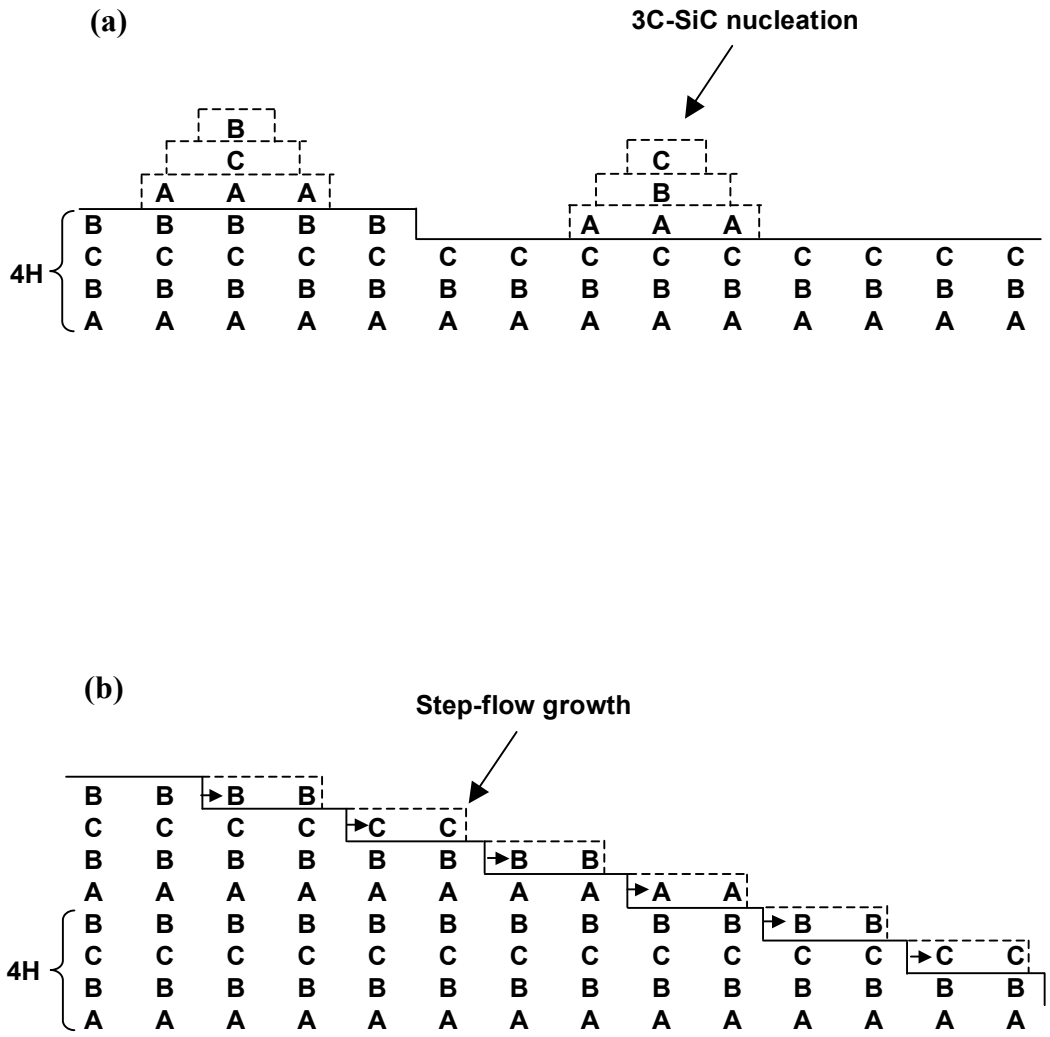


Fig. 2.4 Growth modes for 4H-SiC epitaxial growth. (a) 3C-SiC formation by two-dimensional nucleation, and (b) homoepitaxial growth of 4H-SiC by step-controlled epitaxy.

Step-flow growth can happen on an off-axis substrate, and there are still other conditions that are needed to achieve the step-flow growth. In order to predict the required conditions and elucidate the mechanism for step-controlled epitaxy, a surface diffusion model is considered based on the BCF (Burton, Cabrera, and Frank) theory by Matsunami, et al. [6]. Schematic of the model is shown in Fig. 2.5 assuming steps with a height of h are equally spaced with equal separation distance λ_o. During the growth, the adsorbed species diffuse on terraces and some of them are incorporated into the crystal at steps, and others re-evaporate (desorb). Assuming 2-dimensional nucleation does not occur on terraces, the continuity equation for the adsorbed species is expressed by [6]:

$$-D_s \frac{d^2 n_s(y)}{dy^2} = J_s - \frac{n_s}{\tau_s} \qquad (2.1)$$

where $n_s(y)$ is the number of adsorbed species per unit area on the surface (adatom concentration), J_s is the flux of reactants arriving at the surface, τ_s is the mean residence time of adsorbed species, and D_s is the surface diffusion coefficient. Here, steps are assumed as uniform and perfect sinks for approaching chemical species.

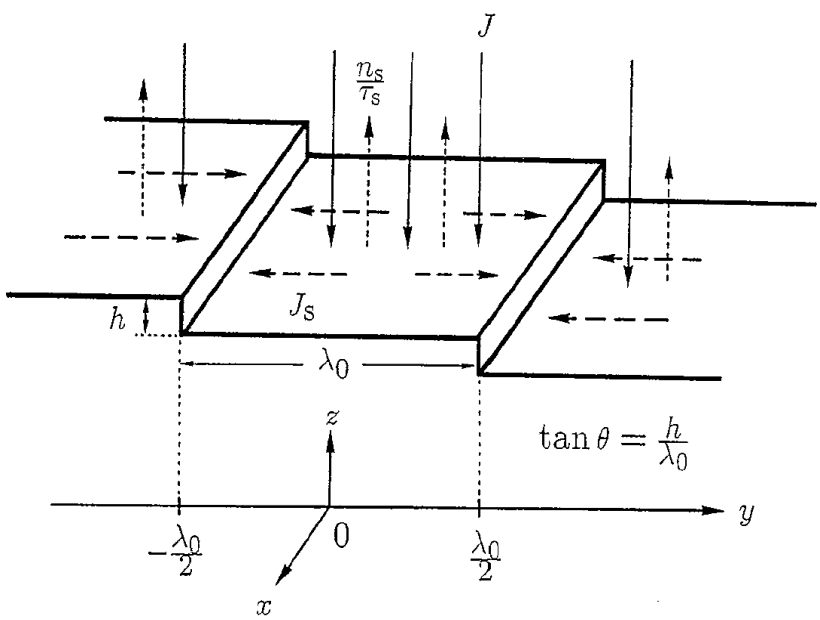


Fig. 2.5 Schematic of simple surface diffusion model, where steps are equally spaced with equal separation distance [6].

The continuity equation for the chemical species can be solved under the boundary condition that the supersaturation ratio α equals unity at the steps, where α is defined as $n_s(y)/n_{s0}$, the ratio of the adatom density at certain position y and its equilibrium value n_{s0}. The solution gives the adatom concentration on the terrace, which can be expressed as [6]:

$$n_s(y) = J\tau_s + (n_{s0} - J\tau_s)\frac{\cosh(y/\lambda_s)}{\cosh(\lambda_0/2\lambda_s)} \qquad (2.2)$$

where λ_s is the surface diffusion length of adsorbed species, the average distance that chemical species travel on a step-free surface before desorption. Then, the distribution of adatom concentration and supersaturation ratio on the surface is calculated based on the Eq. 2.2 and is plotted in Fig. 2.6 [6]. It is clear that α has a maximum value α_{max} at the center of the terrace, which implies an easy nucleation at the center. The value of α_{max} strongly depends on growth conditions, such as growth temperature, growth rate, and terrace length. It is also an essential parameter in determining the growth modes. Assuming a critical supersaturation ratio α_c, the conditions for step-flow growth and two-dimensional nucleation can be expressed as:

$$\begin{cases} \alpha_{max} < \alpha_c, \text{: Step-flow growth,} \\ \alpha_{max} > \alpha_c \text{ : two-dimensional nucleation.} \end{cases}$$

Under the critical conditions when α_{max} is equal to α_c, we can establish the following equation [6]:

$$\frac{\lambda_0}{4\lambda_s}\tanh\left(\frac{\lambda_0}{4\lambda_s}\right) = \frac{(\alpha_c - 1)}{2n_0 R}\frac{n_{s0}}{\tau_s} \qquad (2.3)$$

where n_0 is the density of available adatom sites on the surface and R is the growth rate. This is the basic equation which describes the growth modes. In Eq. (2.3), n_0 and h are inherent SiC material parameters, and λ_0 and R are determined by growth conditions. From Eq. (2.3), the critical growth conditions can be predicted under various conditions using the temperature dependencies of n_{s0}/τ_s, α_c, and λ_s. One example of the calculated critical growth conditions as a function of growth temperature, growth rate, and off-cut angles is shown in Fig. 2.7 [6]. The lower-right and upper-left regions of individual curves correspond to step-flow growth and two-dimensional nucleation mode,

respectively. It is obvious from the figure that higher temperatures, larger off-cut angles, and lower growth rates are preferable to step-flow growth.

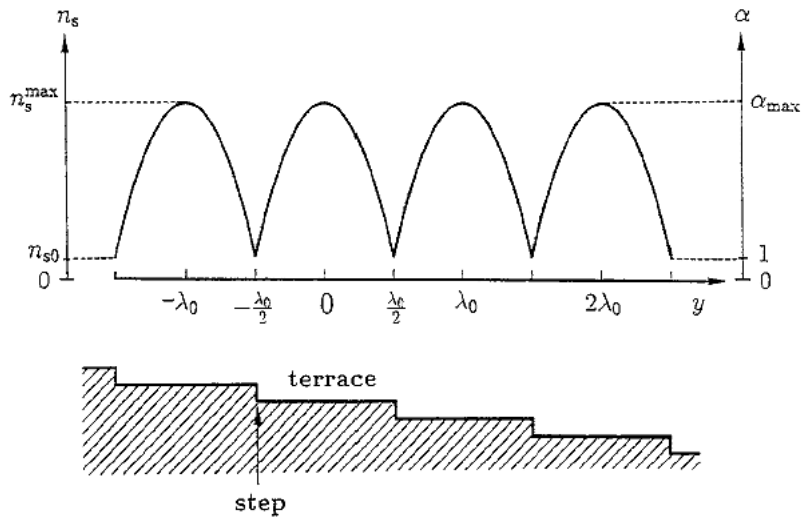


Fig. 2.6. Distribution of adatom concentration and supersaturation ratio α on an off-axis *substrate [6].*

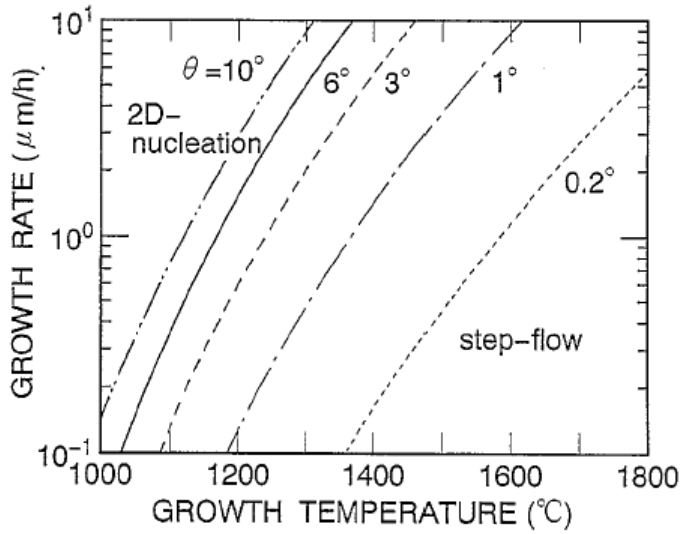


Fig. 2.7. Critical growth conditions as a function of growth temperatures, growth rates, and off-cut angles. The lower-right and upper-left regions of individual curves correspond to step-flow growth and tow-dimensional nucleation, respectively [6].

2.1.1.4. Doping control during epitaxial growth

In order to build operational devices on SiC, the controlled doping must be achieved. There are several factors which make the doping SiC different from traditional semiconductors. First, since SiC is a compound semiconductor, dopants can choose to reside on either of two sublattices, which can result in different ionization levels. Second, the strong bonds of SiC crystal structure make effective doping by diffusion impractical. Therefore, doping of SiC epitaxial layer is achieved either during epitaxial growth or by ion implantation. The former procedure introduces hydrogen impurities, the latter causes intrinsic point defects [59]. The doping during the epitaxial growth is achieved by flowing a specific dopant source into the CVD reactor. The most common n-type and p-type dopants are Nitrogen and Aluminum, which is accomplished through the introduction of N_2 and trimethylaluminum (TMA) respectively into the reactor during the growth. Phosphorus-doping (using PH_3) for n-type and Boron-doping (using B_2H_6) for p-type are also used, but they are less common.

Doping concentration can be adjusted by changing the dopant source flow during the growth. However, doping control in this way is limited both in reproducibility and in attainable doping range [22]. This situation has been greatly improved by the discovery of “site-competition” epitaxy [22]. The site-competition dopant control technique is based on the fact that many dopants of SiC have preferences to incorporate into Si lattice sites or C lattice sites. By varying the C-source to Si-source ratio (C/Si ratio) during epitaxial growth, the doping of the epitaxial layer can be controlled by prohibiting or enhancing the incorporation of certain dopant atoms into their preferred lattice sites. For example, Nitrogen atoms have been known to occupy the C-sites. By growing in a carbon-rich environment, the incorporation of nitrogen can be prohibited to form lightly-doped epilayer for drifty region in high power devices. Aluminum atoms, which are opposite to nitrogen, have known to occupy Si-sites in the SiC sublattices. The Al doping concentration can be increased by growing in the C-rich environment to achieve degenerate P-type doped epilayer for good ohmic contacts. For n-type doping with phosphorus, the site competition effect is shown consistently with phosphorous competing with Si for the Si-sites [60]. Boron has been reported to occupy both the Si and C sites, with preference of the Si-sites. It has been shown that the boron

incorporation in the Si-rich condition is significantly lower than in the C-rich condition, which is consistent with the preferential occupation of B on the Si-sites [22].

The phenomenon of site preference for some dopant atoms can be understood by considering the size of the dopant atom as compared to the size of the Si or C atom. The non-polar covalent radii of the elements of interest are: Si (1.17 Å); C (0.77 Å); N (0.74 Å); Al (1.26 Å); P (1.10 Å); B (0.82 Å) [22]. Using the atomic size as a first order approximation, we can find out that N should substitute for C in the C-site and Al and P should substitute Si in the Si-site, which is consistent with the experimental results. However, B should mainly occupy C-site if only considering the atomic size and this is not consistent with the experimental observations. This discrepancy has been explained based on the fact that considerable amount of hydrogen is also incorporated into the Boron-doped epitaxial layer during the CVD growth. According to the experiments, B-doped samples contain hydrogen in the same order of magnitude as boron, and the B-H complexes are incorporated in the SiC crystal. Therefore, the actual specie that participates in the doping process is "B-H" complex, which has a size of 1.10 Å [22]. Based on this information, B-H complex has a size which is closely matched with Si atom and should occupy the Si-site, in agreement with the experiment results.

Besides C/Si ratio, dopant incorporation can also depend on substrate polarity and off-cut angle, growth rate, growth temperature, and growth pressure. Different doping behaviors have been observed on Si-face and C-face substrates. The site-competition effect is less effective on C-face than on Si-face. For nitrogen doping, C-face epilayers exhibit higher doping concentration than Si-face ones under the same growth conditions. The lowest controlled nitrogen doping on C-face is usually in the range of $1\bullet10^{15}$~$1\bullet10^{16}$ cm^{-3}, although the lowest background doping has been dropped into low 10^{14} according to some reports [20, 61]. For p-type doping, both Al and B incorporation on C-face were less efficient than Si-face under the same condition, which makes the growth of p^+ layer difficult on C-face [22]. The dependence of doping incorporation on temperature is somehow complicated. For n-type doping, the temperature dependence of N incorporation depends on both substrate polarity and C/Si ratio [62, 63]. Under high C/Si ratio, the N incorporation shows different temperature dependence on Si-face and C-face. Under low C/Si ratio, the temperature dependence of N incorporation is the same for both faces. It is believed due to the competing effects of the desorption process and thermally activated process during the growth [63]. Nitrogen doping is found to decrease with increasing growth rate on Si-face, but this trend is reversed on C-face [64]. By decreasing

growth pressure, nitrogen incorporation can be reduced on both Si-face and C-face, which provides an efficient way to achieve low-doped n-type epilayers [64].

Another important aspect of doping incorporation is the control of doping transitions between opposite conductivity. This problem is of special importance for "continuous growth" process, which is believed to help to reduce the forward-voltage instability in SiC bipolar devices [2, 3, 31, 65]. In the continuous growth, the entire active device structure consisting of a thick, low doped n-type drift layer and thinner, heavily doped p-type emitter layer is grown without interruption. It is pointed out that a sharp transition can be achieved by stopping the growth for some minutes at the growth temperature and etching the wafer during the stop time slightly by the hydrogen carrier gas [23]. A challenge with the continuous growth process is the so-called "memory effect". It is found that areas of lower temperature in the growth cell, such as reactor walls, can serve as sinks for intentional impurities [1]. These impurities can re-evaporate and incorporate unintentionally during the subsequent growth runs. The memory effect is an especially severe problem for aluminum due to the easy deposition of aluminum species in the growth environment. Future research effort is needed to explore reproducible continuous growth technique.

2.1.1.5. Defect control during the epitaxial growth

The performance of SiC-based devices can be limited by the defects in epilayers. Defects can either propagate from the substrate into the epilayer or generate during the growth. Defects commonly seen on the epilayer are micropipes, dislocations, growth pits, polytype inclusions, carrot defects, and step bunching. The presence of some defects, such as micropipe and triangular inclusion, severely limits the yield of larger area SiC power devices, while other defects also impact device performance in one or other way. Therefore, control of various defects during epitaxial growth is extremely important for SiC power device development.

Although the quality of substrates has been improved greatly in recent years, there are still a relatively large number of defects in commercial SiC substrates, which may propagate into the epilayer during the CVD growth process. Figure 2.10 illustrates the propagations of major substrate defects into the epilayer. The micropipe defect is an open-core threading screw dislocation (TSD) with a burger vector several times of the c-axis lattice parameter. They can induce device failure or cause reliability issues [48]. During the epitaxial growth, micropipe defects can propagate directly into the epilayer

(labeled as “A” in Fig. 2.10) or dissociate at the substrate/epi interface into multiple closed-core TSDs (labeled as “B” in Fig. 2.10). Micropipe closing in SiC is first reported in liquid phase eptiaxy (LPE) [66]. Recently, it is found that the closing of micropipes can also be achieved during the CVD growth. The probability of micropipe dissociation can be enhanced under Si-rich or low C/Si ratio condition [48, 67]. More than 99% of micropipes can be closed under optimized conditions during the CVD growth. Additionally, a two–epilayer growth scheme has been designed to grow device structures with low micropipe density, which consists of a high-doped micropipe stopping layer and a low-doped active layer [67]. For micropipe stopping layers, a high probability of micropipe dissociation is maintained at a relatively low C/Si ratio; while growth of a low-doped active layer on a micropipe stopping layer is possible at a relatively high C/Si ratio for high power device structure.

Closed-core TSDs (labeled as “C” in Fig. 2.10) are less harmful than micropipe defects, and may contribute to premature breakdown in some device structures. They can either propagate directly into epilayer as TSDs or act as a source of other epitaxial defect, such as carrot defects (labeled as “D” in Fig. 2.10) [68]. Threading edge dislocations (TEDs) are another class of defects in SiC substrates that may propagate into the epilayers. Although TEDs are not desirable, they are considered to be the least harmful dislocation among others. Densities of both types of threading dislocations in epilayers generally depend on the quality of substrates. Commercially SiC wafers typically have a density of about 10^3~10^4 cm^{-2} for both types of dislocations.

Basal plane dislocations (BPDs) are defects that exist in the basal plane of the SiC crystal that may propagate into epilayers. Much research has been made to reduce BPD density because they are believed to cause forward voltage instability in SiC bipolar devices. Research has found that BPDs propagating from substrates can either still propagate as BPDs (“E” in Fig. 2.10) or can be converted to threading edge dislocations (TEDs) (“F” in Fig. 2.10) during epitaxial growth [24]. Recent studies have found this conversion can be promoted by proper pre-growth treatment or optimization of growth process. Sumakeris, et al., have reported that reactive ion etching (RIE) and KOH etching prior to growth help to reduce the BPD density significantly [2]. Tsuchida, et al., found that re-polishing of the substrate surface, in-situ H_2 etching also influence the propagation of BPDs into the epilayers [10]. Ohno, et al., investigated the effect of growth conditions on the BPD density, and found out the correlation between the BPD propagation and growth condition, such as C/Si ratio and growth rate [25]. Researcher also found that BPD density can be reduced by growing on substrates with C-face polarity or with low

off-cut angles [8, 10, 14, 15]. While the density of BPDs in commercial substrates ranges from 10^3 cm^{-2} to 10^4 cm^{-2}, this number can be reduced to several hundreds in epilayers after standard CVD growth process. The BPD density of less than 10 cm^{-2} has been obtained by using certain low BPD process [2]. There are two major pre-growth treatment techniques that have been developed to enhance the BPD conversion. One of the techniques is selective KOH etching and regrowth. In this technique, the SiC substrate is selectively etched by molten KOH before the epitaxial growth. When the epilayer is grown on the etched substrate, BPD density is found to be greatly reduced. One explanation is that the growth pit helps to locally reduce the off-axis angle in the vicinity of a BPD, which in turn help the BPD to convert into a TED [2]. Another explanation is that lateral growth perpendicular to the step-flow direction will take place in the pit during the growth, which blocks the path for the BPD propagation, and thus promote the conversion of BPDs to TEDs [69]. The other technique is so-called lithographic patterning. In this technique, surface patterns are created by reactive ion etching with a photolithography-defined mask. Those patterns are believed to promote the BPD conversion and decrease the BPD density. In this study, BPD density of 2.6 cm^{-2} has been achieved by using substrate with low off-cut angle and optimized growth conditions, which will be discussed in chapter 4.

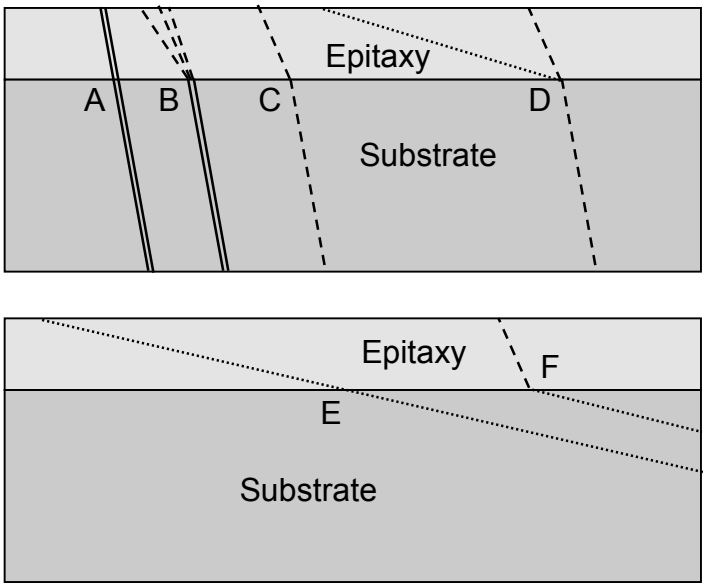


Fig. 2.10. Propagation of substrate defects into epilayers. A: micropipe; B: multiple closed-core threading screw dislocation; C: closed-core threading screw dislocation and

threading edge dislocation; D: carrot defect; E: basal plane dislocation; F: BPD converted into threading edge dislocation during epilayer growth. (modified from reference [2])

Besides micropipes and elementary dislocations, surface defects are often found on epilayers grown by CVD, including growth pits, polytype inclusions and carrot defects. Figure 2.9 summarizes the shapes, origins and possible impacts on device performance for some major surface defects on SiC epilayers along with micropipe defects. Growth pits are a common morphological defect present on SiC epilayers. The origin of growth pits has been studied by Powell, et al., [70]. It is believed that growth pits can be caused by different sources, such as polishing damage, substrate imperfections and bulk defects. It seems that the polishing and preparation of the substrate play a bigger role in the formation of growth pits than bulk defects such as micropipes and dislocations. It has been shown that chemical mechanical polishing (CMP) and proper pre-growth H_2 or HCl etching have helped to reduce the growth pit density significantly [70].

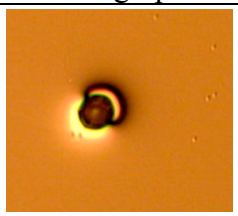
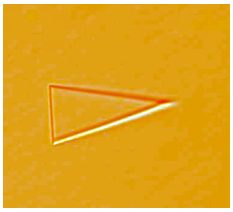
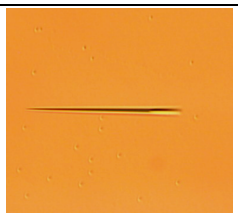
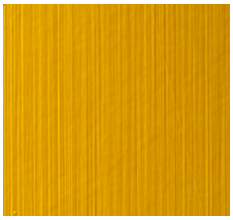
Polytype inclusion is also a common type of surface defect in 4H-SiC epilayers grown by CVD. These polytype inclusions are usually found to 3C-SiC, and have a triangular shape (often called triangular defects) as shown in Table 2.1. The presence of these triangular defects can significantly reduce the device breakdown voltage. The mechanism of 3C inclusion has been studied by Konstantinov, et al., [58]. It is believed that 3C-SiC nucleation occurs via the formation of triangular stacking faults at substrate imperfections. For 4H-SiC, 3C inclusions are more often to be found on epilayers grown on low off-cut angle substrates. By growing on 8° off-angle substrates, the 3C-SiC inclusions can be almost eliminated.

Carrot defects are also common on epilayers, which are defined as carrot-like features on the surface parallel to off-cut direction. Density of these defects is usually less than 5 cm^{-2}. They also have negative impact on the reverse characteristic of the device by increasing the leakage current. Recently, the origin of the carrot defects has been pointed out to be the threading screw dislocations from substrates, which expand as planar fault in both the prismatic plane and basal plane [68]. Sumakeris, et al., also reported that carrot defect density can be reduced by the judicious selection of substrates and optimized epilayer growth techniques [2].

Step bunching is multiple-height steps formed during the epitaxial growth. It is observed that epitaxial layers grown on (0001) Si face exhibits macrostep bunching, where three bilayer-height steps are dominant on 6H-SiC epilayers and four-bilayer-height steps on 4H-SiC epilayers. On the (000-1) C face, the surface is relatively flat and

no macrosteps are observed. Also, the tendency of step bunching increases as the substrate off-cut angle decreases as reported by Powell, et al., [11]. It is not yet clear what effect step bunching has on device performance. However, it is obvious that rough surface from severe step bunching will have negative impact on Schottky contact and metal-oxide-semiconductor (MOS) interface properties.

Table 2.1 Nomarski micrographs, origins and possible impacts on device performance of major SiC epilayer defects (not all images are in the same scale and part of materials listed in this table are modified from reference [44]).

Defect types	Nomarski micrographs	Possible origin of defects	Impacts on device performance
Micropipes		Substrate micropipes that propagate into epilayer.	>50% breakdown voltage reduction and increased leakage current
Growth pits		polishing damage, substrate imperfections and bulk defects	Harmless in general. Non-smooth surface seems likely to impact Schottky rectifying properties
Triangular defects		3C-SiC nucleation at substrate imperfections or defects	>50% breakdown voltage reduction and increased leakage current
Carrot defect		Nucleate at substrate TSDs, and expand through epilayer structure	Increase in reverse leakage current.
Step bunching		Coalescence of steps from substrate off-cut	Rough surface, effect on device are not confirmed.

There is much research needed to understand factors that influence the generation and densities of surface defects in SiC epilayers. These factors can be roughly divided into the following categories: (1) substrate characteristics: polytype, off-cut angle, off-cut direction, face polarity, and surface orientation; (2) mechanical and chemical treatment of the substrate before the growth, such as polishing and cleaning of substrates; (3) in-situ pre-growth substrate treatment inside the reactor, such as H_2 etching; (4) growth conditions: growth temperature, pressure, C/Si ratio, and growth rate. For example, epilayers grow on 4H-SiC substrates with off-cut angle of 3.5^o or less have more tendencies of forming triangular defects and step bunching. Increasing the off-cut angle from 3.5^o to 8° reduces the density of these defects and also helps to obtain smooth surface for 4H-SiC [70]. The relative content of C and Si (C/Si ratio) in the growth environment also has a great impact on the surface morphology of final epilayer. With C/Si ratio higher than certain value, occurrence of 3C inclusion happens more often. Growth with a low C/Si ratio gives rise to Si droplets on or imbedded within the epitaxial layer [5].

Defect reduction will continue to be a subject of active study in the filed of SiC epitaxial growth, and will be one of major research topics in this proposal. Also, it must be pointed out that the optimal growth conditions are strongly dependent on many variables, especially reactor configuration and susceptor type. The growth process must be optimized for specific reactor setup and care must be taken to adopt any existing results from literature.

2.1.1.6 Lifetime control and measurement for SiC epilayers

Carrier lifetime is one of the important parameters giving information about the epilayer quality, since deep levels or crystal imperfections usually affect the carrier lifetime. Moreover, minority carrier lifetime plays a key role in determining bipolar device performance, as forward voltage drop, bipolar gain, maximum current rating and maximum operating frequency are inherent functions of minority carrier lifetime [71]. Therefore, it is critical to investigate the lifetime limiting factors and explore possible ways to control the lifetime in SiC epilayers.

Lifetimes fall into two primary categories: recombination lifetimes and generation lifetimes. The concept of recombination lifetime τ_r holds when there are excess carriers, and is interpreted as the average time for an electron-hole pair (ehp) to recombine. By analogy, the concept of generation lifetime τ_g holds when there is a paucity of carriers,

and is interpreted as the average time to generate an ehp. These recombination and generation events occur not only in the bulk, but also on the surface. When they occur on the surface, they are characterized by the surface recombination velocity s_r and the surface generation velocity s_g. Both bulk and surface recombination (generation) occur simultaneously and their separation is sometimes quite difficult. Some methods allow this separation while others do not. The measured lifetimes are always effective lifetimes consisting of bulk and surface components [72]. Detailed discussion of carrier lifetime theory will not be given here, and can be found in many semiconductor textbooks, such as reference [73].

Although studies on growth and characterization of 4H-SiC epilayers has been carried out intensively, systematic studies on carrier lifetime in SiC epilayers are limited in literature [74-78]. Deep levels in the bandgap are believed to severely limit the carrier lifetime of SiC epilayers by acting as recombination centers. Those deep level traps could either come from intrinsic defects, such as point defects in SiC crystal, or come from impurities introduced during the epitaxial growth. Electrical properties of major defects observed in 4H-SiC have been summarized in Table 2.2. The most common intrinsic defects found in SiC epilayer are $Z_{1/2}$ center and $EH_{6/7}$ center. Although the exact origins of those defects have not been identified, they are found to degrade lifetime [77]. Impurities, such as Ti and B, are also been studied for possible lifetime limiting factors. Ti is believed to substitute for the Si lattice site (both the cubic and the hexagonal sites), and is identified as an acceptor-like electron trap [79]. Boron is believed to create at least two electrically active levels in SiC: one shallow acceptor level and one deeper level. The shallow B center is believed to reside on Si lattice site. The deep B-related level, know as the D center, has been suggested to be complexes of boron and intrinsic defects [77].

Table 2.2 Summary of electrical properties of major defects observed in 4H-SiC [77].

Defect	Position in the band gap	Capture cross section (cm^2)
$Z_{1/2}$	E_C-(0.63-0.68) (eV)	$3\cdot10^{-15}$-$2\cdot10^{-14}$ (for electron)
$EH_{6/7}$	E_C-(1.60-1.65) (eV)	$2\cdot10^{-13}$-$9\cdot10^{-12}$ (for electron)
Titanium (h)	E_C-(0.11-0.13) (eV)	$2\cdot10^{-15}$-$1\cdot10^{-14}$ (for electron)
Titanium (k)	E_C-(0.15-0.17) (eV)	$3\cdot10^{-15}$-$2\cdot10^{-14}$ (for electron)
Shallow Boron	E_v+(0.23-0.28) (eV)	$2\cdot10^{-14}$-$3\cdot10^{-134}$ (for hole)
D-center	E_{V+}(0.58-0.63) (eV)	N/A (hole trap)

In order to control the deep trap densities during the growth process, correlation between certain growth parameters and deep trap densities has been identified [77, 80, 81]. Those parameters include, but do not limit to, growth temperature, C/Si ratio and graphite susceptor purity. It has been shown consistently that epilayers grown at relatively low temperature exhibit lower deep trap densities (such as $EH_{6/7}$, $Z_{1/2}$). From a thermodynamic perspective, point defects such as vacancies and interstitials increase with increasing growth temperature [80]. A high dc current gain has been achieved in 4H-SiC BJT by growing emitter and base layers at lower temperature, which is believed due to improved carrier lifetime [33]. Studies on effects of C/Si ratio on deep trap densities are not conclusive at this point. Some studies show that high C/Si ratio reduces the $EH_{6/7}$ and $Z_{1/2}$ trap densities [77, 81, 82], while other study indicates the other way[83]. The incorporation of the shallow B and Ti has shown to increase with increasing C/Si ratio, which has been explained in terms of site-competition principle sine both types of impurities are believed to occupy Si site [77]. It is also observed that D-center concentration is reduced under C-rich condition for 6H-SiC, which implies the association of a carbon vacancy complex with the D-center [84]. Studies on the microscopic and electronic structure of those defects are still needed to provide further guidance for growth process optimization. Graphite susceptor purity also has a great impact on impurities concentration in the epilayers. Reduction in epilayer lifetime has been directly correlated to the degradation of SiC coating on graphite susceptor [85]. High-purity graphite and alternative susceptor coating are being investigated for growing high purity SiC epilayers with longer carrier lifetime [54].

Data on SiC lifetime are very limited in literature. This is, to some extent, due to the difficulties in measuring and interpreting lifetimes in SiC materials. Both electrical and optical techniques have been used to measure carrier lifetime in SiC. Electrical techniques include reverse recovery, electron beam induced current (EBIC), pulsed MOS capacitor (Capacitance-transient) and open circuit voltage decay (OCVD). Optical techniques include time-resolved photoluminescence, microwave-detected photoconductance decay (μ-PCD) and optical free carrier absorption. Different measurement methods can give widely differing values for the material with similar qualities. In most cases, the reasons for these discrepancies are fundamental and are not due to a deficiency of the measurement [72]. Several commonly used techniques for lifetime measurement will be discussed briefly next.

Reverse Recovery (RR) technique is based on the measurement of transient response of a pn junction diode. When a pn diode is rapidly switched from forward into

reverse bias, there are excess minority carriers remaining in the device from forward bias injection. Some carriers are swept out of the device by reverse current and some carriers recombine. The reserve current will remain constant for a period of t_s, also called the storage time, which is directly related to the minority carrier lifetime of the base region. This method has been widely used in Si-based diode characterization. However, a fast response circuitry has to be used for SiC due to the relatively short recovery time in SiC pn diode, which makes this measurement somewhat difficult. It has been reported that the effective minority carrier lifetime measured by this technique is very short compared with the results from other techniques [71, 86]. The author in reference [71] believed that this is due to perimeter surface recombination effect, and a technique is proposed to further separate the surface effect from the bulk. However, the validity of this analysis is still in debate and further studies are needed [87]. Ramungul, et al., studied the ramp recovery of SiC pin diodes under high-level injection [86]. They found a reduction of effective carrier lifetime with injection level, which is believed due to the dominance of Auger recombination process at high current injection level (>100 A/cm^2). In addition, the emitter lifetime is generally much lower than the base lifetime in pn diode. Emitter recombination also has a significant influence on the RR transient, which leads to reduced effective lifetimes [72]. Therefore, reverse recovery is not widely used as a lifetime characterization tool in SiC materials due to the difficulties in both measurements and interpretations.

Pulsed MOS capacitor (C-t) technique is usually used to measure the generation lifetime τ_g. The generation lifetime is related to carrier recombination lifetimes through $\tau_g = \tau_n + \tau_p$, when assuming n and p are much smaller than n_i in a depleted region and trap levels E_T are close to E_i. This is exactly the ambipolar lifetime, which is often used to characterize the bipolar devices in high-injection level. In this technique, the MOS capacitors are pulsed into deep depletion region, and recover to the equilibrium state through bulk and surface generation. Capacitance-time response of the MOS capacitors is recorded in this process, which is then converted to Zerbst plot to extract both bulk generation lifetime τ_g and effective surface generation velocity S_{eff}. Because of the extremely long generation lifetime of SiC at room temperature due to its wide band gap, the measurement has to be performed at elevated temperature. The measured C-t transient are usually quite long (usually several hours for SiC), hence no fast response circuitry is required. Also, this technique enables the separation of surface generation component from the bulk generation lifetime, which makes it suitable for consistent material characterization. Characterization of both n-type and p-type doped 4H-SiC epilayer (in

the doping range of $10^{16}cm^{-3}$) by C-t technique has been reported in an effort to achieve long charge retention time for non-volatile memory elements [88, 89]. In our lab, C-t technique has been used to characterize p-type epilayers for base region in the 4H-SiC BJT [90]. Measurement problems are encountered when we try to extend this method to lightly doped n-type epilayer characterizations. Studies are still needed to further explore the capabilities of this technique.

EBIC is used to measure minority carrier diffusion length, minority carrier lifetime, and defect distribution. In this technique, a semiconductor with some type of electrical junction (either p-n or Schottky) is bombarded by an electron beam inside a scanning electron microscope (SEM). Electron hole pairs (ehp) are generated inside the bulk semiconductor. These excess minority carriers diffuse toward the device junction where they are collected by the built-in electrical field. The device is usually connected to a current meter which the EBIC current (I_{EBIC}) is collected. During the measurement, I_{EBIC} decrease as the beam is scanned away from the contact due to bulk and surface recombination. This decay can be used to determine the diffusion length, from which minority carrier lifetime can be deduced. It is also possible to extract the minority carrier lifetime directly from the transient analysis by using a stationary pulsed beam [72]. Surface recombination effects can be significantly reduced if the beam penetration is increased. This can be directly tested by plotting $\ln(I_{EBIC})$ versus *d* (distance between beam and edge of space charge region) for various beam energies. The plot should approach a straight line for higher energies [72]. EBIC has been used to measure minority carrier diffusion length in both 4H- and 6H-SiC [91, 92]. It also has been used to characterize electrical active surface defect in 4H-SiC diodes [93, 94].

Time-resolved photoluminescence (PL decay) is an optical method to measure minority recombination lifetime. Excess carriers are generated by a short pulse of incident photons with energy $h\nu > E_g$. The excess carrier density is monitored by detecting the time dependence of the light emitted by the recombining electron-hole pairs. The PL decay signal can then be used to extract lifetime information. Due to the indirect nature of SiC, the dominating recombination mechanism is assumed to be non-radiative recombination of carriers by mid-gap traps. A minor part of recombination is radiative and can be detected as PL signal. Time-resolved photoluminescence has been used to generate a map of the minority carrier lifetime for a 4H-SiC epilayer on a 30 mm diameter wafer [76]. This technique is attractive in that it is non-destructive and no special sample preparation is needed.

2.1.2 SiC PiN Diode Device Physics

In this section, the physics of pin diodes is discussed for both forward and reverse operation modes. The pin diode structure consists of an n^+ substrate, an n^- low-doped drift layer and a p^+ emitter layer. Pin diodes can carry a very high current density during forward conduction due to the effect of conductivity modulation, which makes it possible to develop rectifiers with high breakdown voltage.

2.1.2.1 Forward conduction

At low injection levels, current flow is dominated by recombination occurring within the space charge region and drift-diffusion in the neutral region. By ignoring the series resistance, high level injection, and short base effects, the theoretical forward current-voltage equation of a pn diode can be written as

$$I_F = I_1(e^{qV/kT} - 1) + I_2(e^{qV/2kT} - 1) \tag{2.4}$$

$$I_1 = qA(D_n n_i^2 / L_n N_A + D_p n_i^2 / L_p N_D) \tag{2.5}$$

$$I_2 = qAWn_i / \tau_r \tag{2.6}$$

Here, N_D and N_A are the doping concentrations in the n and p regions, respectively. L_n and L_p are the diffusion lengths. D_n and D_p are the diffusion coefficients. n_i is the intrinsic carrier concentration. W is the depletion width in the junction and A is area of active device region. τ_r is the effective carrier recombination lifetime. The first term represents the diffusion current, and the second term is the recombination current. The typical I-V curves for a SiC pin diode and a Si pn diode are shown in Fig. 2.11. One striking difference between Si pn diode and SiC pin diode is the different threshold voltage V_T. Recombination current dominates if $V<V_T$, and diffusion current will dominate if $V>V_T$. For Si, the value of V_T is around 10kT/q. For 4H-SiC, V_T is estimated to be around 100kT/q due to its much smaller n_i at room temperature (assuming other parameters in the ideal diode equation are kept the same as Si). Therefore, the forward current in SiC diodes is dominated by the recombination current in most voltage range of low current level until series resistance or high-level injection effects come into play. It should be pointed out that Eq. (2.4) is only valid for low-level injection condition, where the minority carrier density injected into the neutral regions has a concentration well below that of the majority carrier density.

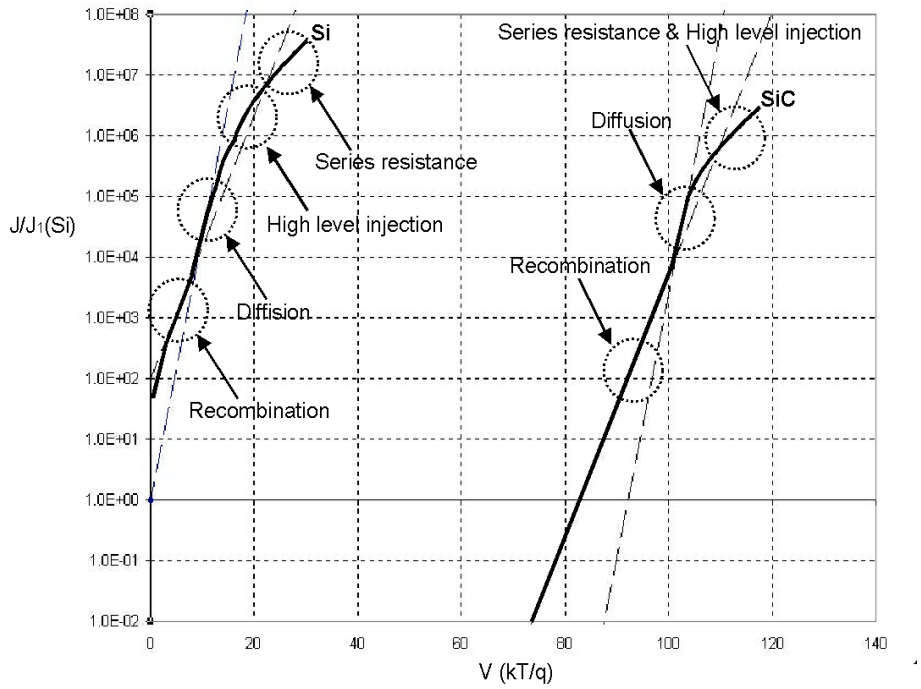


Fig. 2.11. Forward I-V curves of Si and SiC PN diodes [90].

At a certain forward current level the minority carriers injected into the low doped region of a pin diode will outnumber the majority carrier concentration of this region. This mode of operation is called high-level injection (Fig. 2.12). Carriers of opposite polarity are injected from both highly doped regions adjacent to the drift layer, and the concentrations of electrons and holes become equal throughout the drift layer due to charge neutrality. The carrier concentrations are given by [95]:

$$n(x) = p(x) = \frac{\tau_{HL} J}{2qL_a}\left[\frac{\cosh(x/L_a)}{\sinh(w/L_a)} - \frac{\sinh(x/L_a)}{2\cosh(w/L_a)}\right] \qquad (2.7)$$

where w is the width of the low doped region, τ_{HL} is the effective carrier lifetime under high-level injection and L_a is the ambipolar diffusion length. High level lifetime τ_{HL} can be expressed as $\tau_{HL}=\tau_n+\tau_p$. L_a is a function of τ_{HL} and ambipolar diffusion coefficient D_a [95, 96]:

$$L_a = \sqrt{D_a \tau_{HL}} \qquad (2.8)$$

$$D_a = \frac{2D_n}{1 + \mu_n / \mu_p} \qquad (2.9)$$

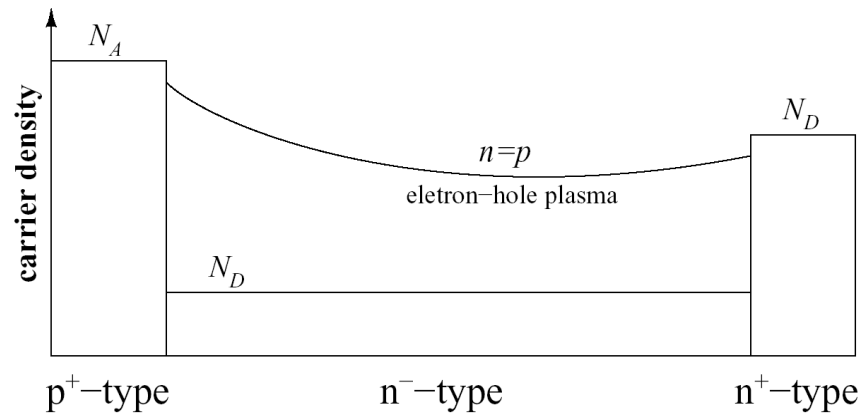


Fig. 2.12. Carrier concentration in a pin diode at high-level injection. The concentration of electrons and holes in the low-doped drift region are equal to each other leading to a decreased series resistance.

Under the assumption of a constant lifetime and diffusion length, the carrier concentration is directly proportional to the current density J through the drift region. Since the resistivity ρ of a semiconductor is inversely proportional to the free carrier concentrations, the voltage drop $V_m=\rho J$ over the drift region becomes constant under high-level injection. This voltage drop can be calculated by using the following approximate expressions

$$V_m = \frac{3k_B T}{q}\left(\frac{w}{2L_a}\right)^2 \quad \text{for } w \le 2L_a \qquad (2.10)$$

$$V_m = \frac{3\pi k_B T}{8q} e^{w/L_a} \quad \text{for } w \ge 2L_a \qquad (2.11)$$

A normalized voltage drop V_m over the middle region of a pin diode as a function of the normalized diffusion length L_a/w for carriers in the low-doped region is shown in Fig. 2.13 based on Eq. (2.10) and (2.11). The voltage drop V_m increases with decreasing L_a/w. As the half-base width (w/2) becomes longer than the diffusion length, the voltage drop across the middle region causes an appreciable increase in the forward voltage drop due to a reduction in the conductivity modulation. Therefore, the diffusion length L_a, and thus the carrier lifetime τ_{HL}, in the drift region is important for achieving high current

densities in pin diode. For 4H-SiC, carrier lifetimes of epilayers are still needed to be improved for better diode performance.

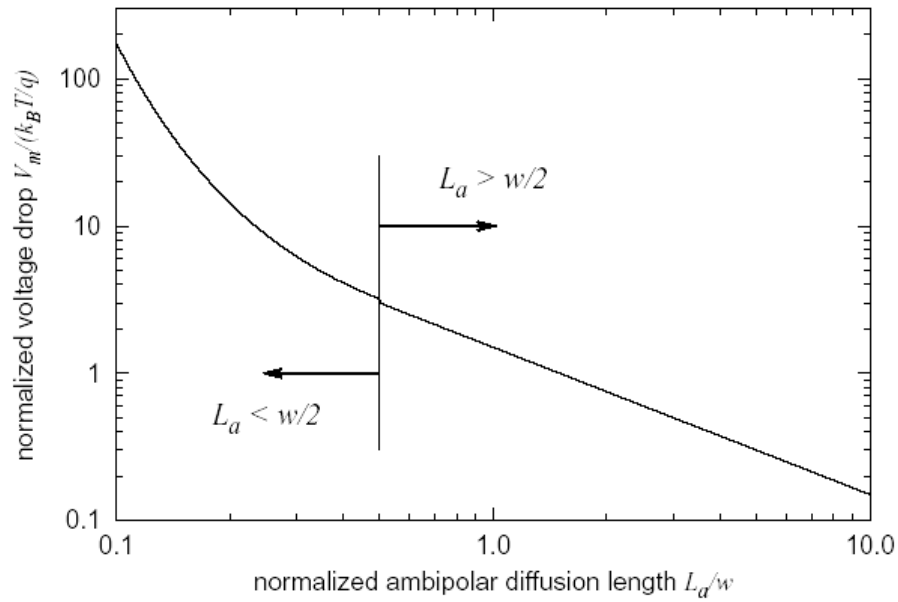


Fig. 2.13. Voltage drop V_m over the middle region of a pin diode as a function of the normalized diffusion length L_a/w for carriers in the low-doped region.

2.1.2.2 Static reverse operations

There are two basic mechanisms responsible for current flow under reverse bias conditions. The first is associated with the generation of electron-hole pairs within the depletion region, referred to as space-charge-generation, and the other is associated with the generation of ehp in the neutral regions that then diffuse to the junction, referred to as diffusion leakage current. Total leakage current of a reverse-biased pn junction can be written as

$$I_R = M(I_1 + I_3) \qquad (2.12)$$

where

$$I_3 = qAWn_i / \tau_g$$

where I_1 is the diffusion leakage current part as shown in Eq. (2.5) and I_3 is the space-charge-generation leakage current. M is the avalanche multiplication factor, which is

assumed to be unity unless the reverse voltage is close to the breakdown voltage. τ_g is the carrier generation time in the depletion region. Because of the small n_i, the leakage current density I_R of SiC diodes is mainly due to generation and is much smaller than Si diodes.

The reverse blocking voltage is determined by the impact ionization process in the depleted layer, which makes M approach infinity. Because impact ionization coefficients depend exponentially on the electric field, avalanche breakdown occurs when the peak electric field reaches the critical field. Assuming the base region is thick enough, the depletion width (W_d) at the point of breakdown can be expressed as:

$$W_d = \varepsilon_S E_C / qN_D \qquad (2.13)$$

If the thickness of the base layer w is larger than W_d, this is considered to be non-punchthrough design. If w if smaller than W_d, it is considered to be a punchthrough design. The reverse blocking voltage V_{br} can be obtained by integrating the electric field distribution.

$$V_{br} = E_C W_d - \frac{qN_D W_d^2}{2\varepsilon_s} = \frac{\varepsilon_s E_C^2}{2qN_D}, \qquad \text{if } w \geq W_d \qquad (2.14)$$

$$V_{br} = E_C w - \frac{qN_D w^2}{2\varepsilon_s}, \qquad \text{if } w < W_d \qquad (2.15)$$

Under reverse bias, if there is a sharp corner in the voltage supporting depletion layer, there will be severe electric field crowding at this corner. To achieve a blocking voltage close to its theoretical one-dimensional value, appropriate edge termination is required. Several edge termination techniques such as field plates, floating guarding rings and junction termination extensions have been successfully applied to reduce the field crowding effect on SiC power devices [97, 98].

2.1.3 Hot-wall CVD Rector and Growth Process

CVD system used in this work is EPIGRESS VP508 SiC CVD reactor built by EPIGRESS (Sweden). The high purity condition in this system is achieved by a high-integrity vacuum system employing a turbo-molecular pump and a dry backing pump. Heating is performed with RF induction in combination with a hot wall design. This contributes to good temperature homogeneity and long-term stability of the system. Epitaxial growth takes place in a SiC-coated graphite susceptor. The temperature is measured with a 2-color pyrometer at the ceiling of the susceptor. The pyrometer is adjusted to the temperature maximum above the substrate and is calibrated by melting silicon on the wafer carrier plate. A photo of the CVD system inner cell is shown in Fig. 2.14. The growth cell consists of a single-walled quartz tube, a dense graphite susceptor, and Rigid Graphite Insulation (RGI) to thermally insulate the susceptor from its surroundings. Hydrogen is used as carrier gas, which is purified by a palladium membrane purifier. Silane (5% diluted in H_2) and pure propane are used as process gases. Argon is available as a purge gas during loading and unloading the cell. Gas flow rates are controlled with analog Mass Flow Controllers (MFC). A dry process pump allows accurate pressure adjustment in the cells. The operation of the system is achieved by using a control software package with a Graphical User Interface (GUI). The growth process is done in step-by-step mode for an active operator interaction. The substrate is placed in a recess of the wafer carrier plate. The carrier plate is loaded from the downstream side into the reactor. A stop in the end of the susceptor makes sure that 2 inch substrates are always placed at the same position in the inner cell. The double chamber system allows the deposition of n-type and p-type material in separate cells. The doping species available in the system are nitrogen, aluminum and boron. Nitrogen is introduced into the reactor either directly into the reactor though a MFC or after diluting with hydrogen through a double dilution line. Aluminum is introduced by vaporization of trimethylaluminum (TMA) through a bubbler system.

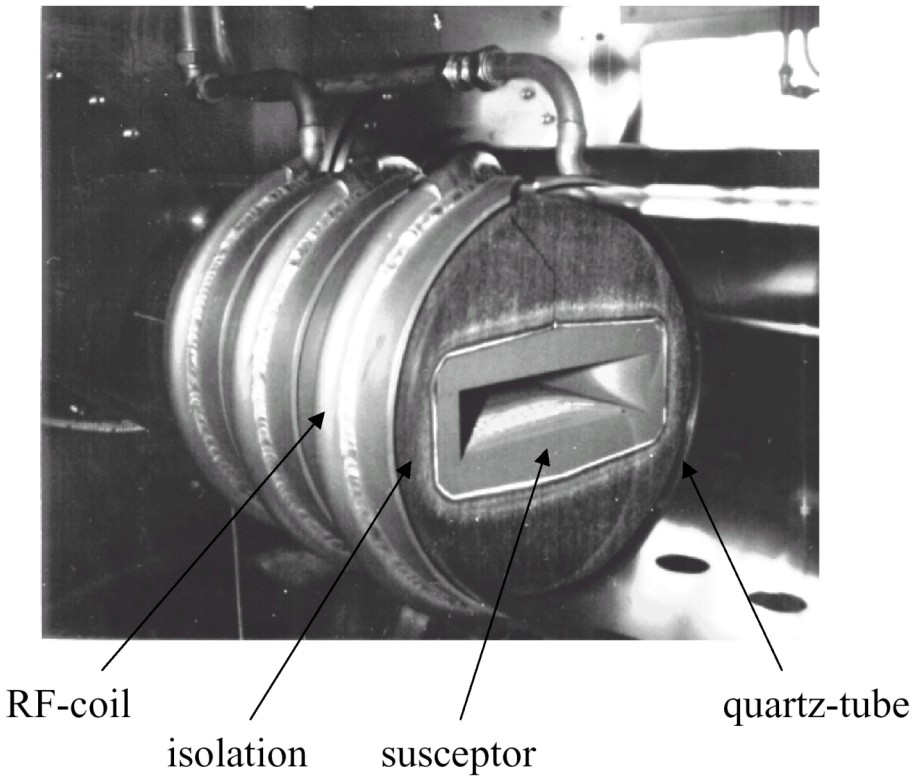


Fig. 2.14 Photo of the Epigress VP508 CVD system inner cell

The actual growth process used in this study is schematically shown in Fig. 2.15. Before growth, samples are first cleaned by standard solvent cleaning procedures, and then are soaked in a mixture of H_2SO_4 and H_2O_2 for 15 minutes, followed by a 2 minutes BHF etch. The growth starts with a flow of H_2 carrier gas, and temperature is ramped up to 1100°C and held at that temperature for about 5 minutes. This procedure allows the reactor chamber to be cleaned and residual gases or moisture to be purged out. After that, the temperature is ramped up to growth temperature (usually 1600°C). During this ramp, 3 sccm of C_3H_8 is flowed into the reactor chamber at temperature of 1400°C. The sample is etched at this step in the mixture of H_2 and C_3H_8 at growth temperature for a period of 5 minutes. Pre-growth in-situ etching is found to be very effective in removing the subsurface damage and creating a smooth surface without scratches [70, 99, 100]. C_3H_8 is added to prevent the Si droplet formation during the pure H_2 etching at high temperature as reported by several groups [99, 101, 102]. After the H_2/C_3H_8 etching, the flow setting of C_3H_8 is changed to the desired value and doping specie, if needed, is flowed into the growth cell. After 30 second for gas mixture to stabilize, SiH_4 is flowed into the growth

environment to start the growth. For thick epilayer growth, a heavily n-type doped buffer layer is usually grown first to isolate the active device region from the substrates with poor quality, and this buffer layer has also been found to help to reduce the forward voltage instability in the bipolar devices [65]. At the end of growth run, RF heating and SiH_4 flow are stopped first to terminate the growth. H_2 and C_3H_8 will be flowed during the cooling phase to purge the reactor cell.

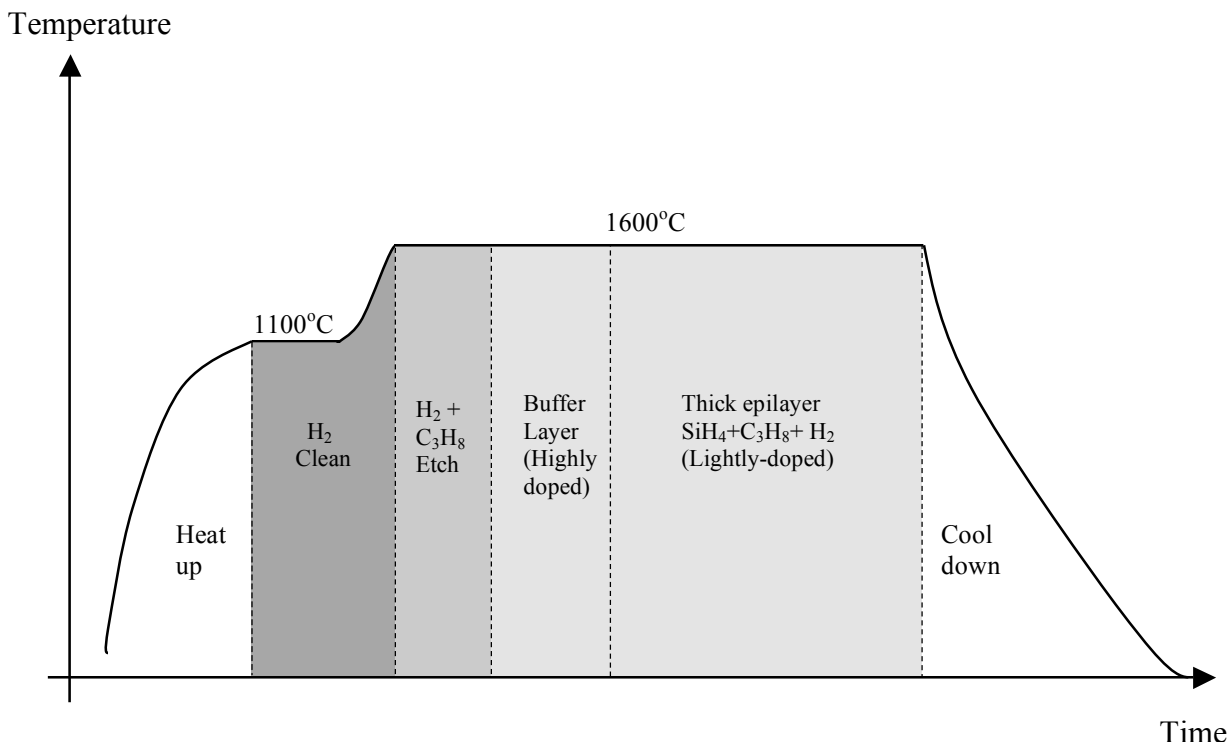


Fig. 2.15 4H-SiC CVD growth process for thick epilayer growth

2.1.4 Epilayer Characterization

Various characterization techniques have been used to determine the different material and electrical properties of the 4H-SiC epilayers. This section will discuss those techniques and their application in this dissertation.

2.1.4.1 Thickness measurement

Thickness of the epilayer is measured using Fourier transform infrared spectroscopy (FTIR). The interferogram is collected by the FTIR and transformed to get reflectance spectrum as shown in Fig. 2.16. The thickness of the epilayer d is given by [72]:

$$d = \frac{i}{2\sqrt{n^2 - \sin^2\theta}} \frac{1}{(1/\lambda_i - 1/\lambda_0)} \qquad (3.1)$$

where i is the number of complete cycles from λ_0 to λ_i, the two wavelength peaks that bracket the i cycles. n is the refractive index of the SiC (□ 2.6), and θ is the angle between the incident beam and sample surface normal . In our current FTIR system, θ is set up to be 0°. Therefore, the Eq. (3.1) can be simplified into:

$$d = \frac{i}{2n(1/\lambda_i - 1/\lambda_0)} \qquad (3.2)$$

For example, the epilayer thickness for the spectrum as shown in Fig. 2.16 is calculated to be 18 μm.

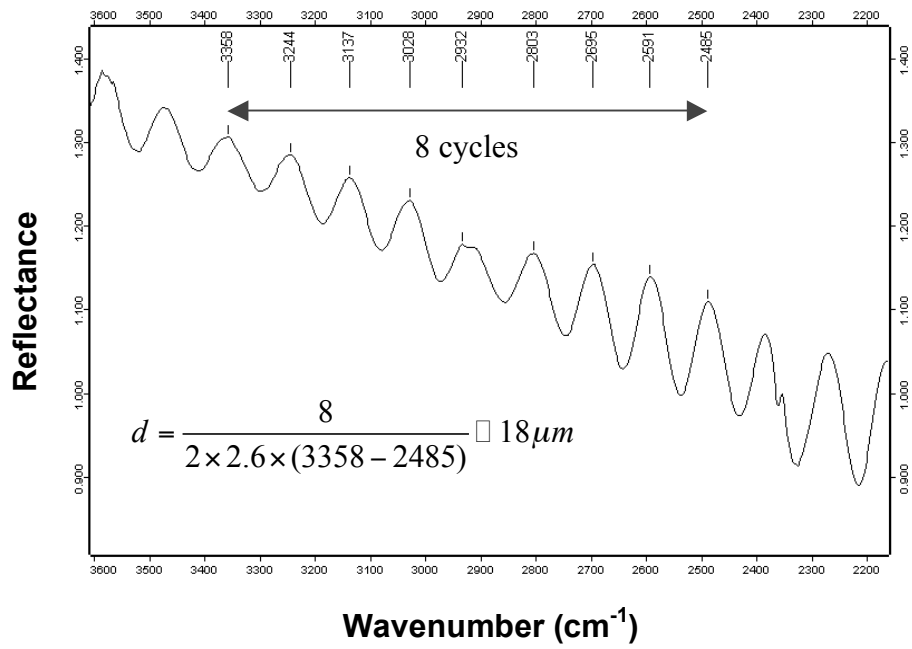


Fig. 2.16 FTIR reflectance spectrum of 4H-SiC epilayer

2.1.4.2 Doping measurement

The net donor concentration is determined by the capacitance-voltage measurement on a Mercury probe. In the measurement, a temporary Schottky contact is formed by mercury contacting the sample through two well-defined orifices. One of orifices is a small hole and the other is a circular ring with larger area, and the area of the small hole is calibrated by standard samples with known doping concentrations. Then C-V measurements are done by connecting the two mercury contacts to a LCR meter. The C-V curves will exhibit different shapes depending on the doping types, and the doping concentration can be calculated from the part of curve when the semiconductor under the small hole is depleted by using the following equation [72]:

$$N(W) = \frac{2}{qK_S \varepsilon_0 A^2 \, d(1/C^2)/dV} \qquad (3.3)$$

$$W = \frac{K_S \varepsilon_0 A}{C} \qquad (3.4)$$

where W is the width of space-charge region. K_S and ε_0 are the dielectric constant of SiC and permittivity in vacuum, respectively. A is the area of the small hole. By plotting $N(W)$ versus W, the doping profile of the epilayer can be obtained.

For heavily-doped sample (>10^{19} cm^{-3}), the doping concentrations are measured using secondary ion mass spectroscopy (SIMS). In this work, samples are sent out to Evans Analytical Group to perform SIMS measurement.

2.1.4.3 Surface morphology characterization

Surface morphology is characterized by an optical microscopy in differential interference contrast mode (Nomarski microscopy) and an atomic force microscopy (AFM). By using Nomarski microscopy, the topographical features on the epilayer surface can be easily observed, such as growth pits and surface defects. AFM is used to characterize the epilayer surface in a smaller scale. For example, step bunching behaviors on the epilayer can be observed by using AFM. In this work, all the AFM measurements are made in the tapping mode by using etched silicon tips.

2.1.4.4 Defect etches

Molten KOH has been shown to etch Si-face of SiC preferentially, but etch C-face of SiC isotropically [103]. Therefore, molten KOH etching technique is used to reveal structural defects for the epilayers grown on Si-face substrates. In this work, etching is performed in molten KOH inside a nickel crucible at a temperature of 520°C for a period of 5-10 minutes. A typical KOH etched sample surface micrograph is shown in Fig. 2.17. There are fours types of etch pits that have been reported on Si-face off-cut surfaces of SiC. The oval-shaped etch pits correspond to basal plane dislocations (BPD), while large, medium, and small hexagonal pits correspond to micropipes, threading screw dislocations (TSD), and threading edge dislocations (TED) [24]. In Fig. 2.17, only three types of etch pits are shown and marked with white arrows. Since low BPD density is especially important for SiC bipolar devices, the BPD etch pit densities are calculated based on the observation under a Nomarski microscope.

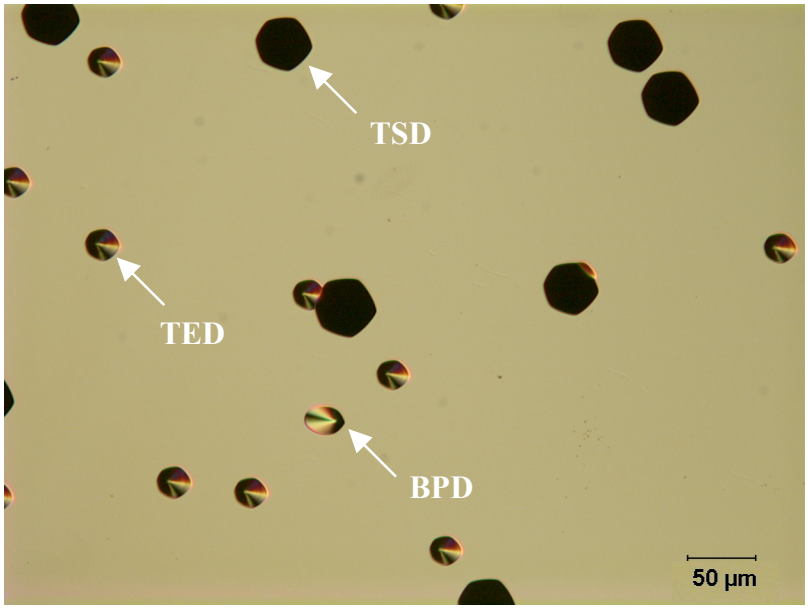


Fig. 2.17 Defect etch pits on Si-face 4H-SiC epilayer after etching in molten KOH.

2.1.4.5 Carrier lifetime measurement

Pulsed MOS capacitor and reverse recovery techniques have been used for characterization of epilayer lifetimes for 4H-SiC epilayers in our lab. Lifetimes of n-type epilayers are also measured by EBIC and PL decay technique through the collaboration with other laboratory.

2.1.4.5.1 Pulsed MOS capacitor (C-t)

In this method，fabrication of a MOS capacitor is needed on epilayers. First, a gate-quality oxide is grown on the epilayer after RCA clean. Different oxidation time and temperature will be selected for Si-face and C-face 4H-SiC due to different oxidation rate. The gate layer is then deposited and patterned on the oxide, along with a large pad forming the virtual ground in the measurement. For the gate material, the phosphorus-doped polysilicon is preferred over aluminum because it gives more stable results during high-temperature measurements.

Because of the extremely long generation lifetime of SiC at room temperature, the measurement is performed with samples heated above 250°C on a hot chuck. During the

measurement, the MOS capacitors are pulsed into deep depletion region, and recover to the equilibrium state through bulk and surface generation. Provided that the size of capacitor is large, lateral surface generation around the perimeter can be neglected compared with bulk generation. The capacitance transient relation can be expressed as [72]:

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2n_i}{\tau_g N_A}\frac{C_{ox}}{C_{inv}}\left(\frac{C_{inv}}{C}-1\right)+\frac{2K_{ox}n_i s_{eff}}{K_s t_{ox} N_A} \qquad (3.5)$$

C_{ox} is the oxide capacitance. C_{inv} is the capacitance when the MOS structure is in equilibrium and the inversion layer is formed. S_{eff} is an effective surface recombination velocity. From the slope of a $-d(C_{ox}/C)^2/dt$ versus $(C_{inv}/C-1)$ plot (as known as Zerbst plot), τ_g can be calculated, and S_{eff} can extracted from the intercept.

2.1.4.5.2 Reverse recovery

Effective minority carrier lifetimes are characterized by measuring the reverse recovery switching transient of SiC pin diodes. The reverse recovery testing is carried out using a fast-risetime pulse-test circuit as shown in Fig. 2.18 [71]. This circuit can stress the diode by using manually triggered single-shot rectangular shaped pulse of 200 ns width. The pulse voltage amplitude is controlled by adjusting the high-voltage DC (HVDC) supply, which charges a 1/2 inch diameter 150 ft semi-rigid coax transmission line. The fast-risetime pulse is formed by the discharge of the semi-rigid coax when the mercury vapor switch is triggered. The diode is initially forward biased by the DC supply through the 200Ω resistor. A 10 μF high-voltage capacitor isolates the initial DC bias from the transmission line circuit, but permits the pulse to rapidly switch the diode from forward bias into reverse bias. The Tektronix CT2/P6041 current probe monitors the transient reverse recovery current of the diode. The transient response of the diode is collected by digital oscilloscope.

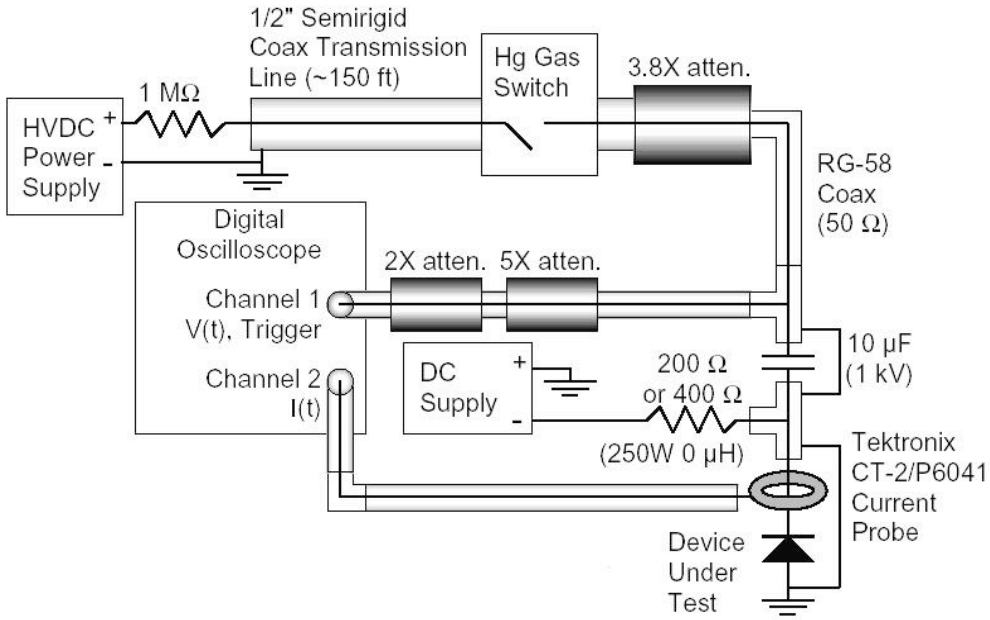


Fig. 2.18 Fast-risetime pulse-test circuit employed to measure pin diode reverses recovery [71].

In the ideal case, the reverse recovery curve of the pn diode will show a constant reverse current during a time of t_s, the storage time. The effective minority carrier lifetime can then be expressed as [72]:

$$\tau_p = \frac{t_s}{\left(erf^{-1}\left[\frac{1}{1 + I_R / I_F} \right] \right)^2} \qquad (3.6)$$

As we discussed in Section 2.3.6, the lifetime measured from this method can be influenced by surface recombination, emitter lifetime and high-level injection, which makes result interpretation difficult.

2.1.5 Device Fabrication

In this work, 4H-SiC pin diodes for both electrical test and light-emission microscopy (LEM) studies have been fabricated on n-type epilayers. MOS capacitors are fabricated on p-type epilayers to be used in C-t transient analysis. This section will discuss the fabrication details for those devices.

2.1.5.1 Fabrication of 4H-SiC pin diodes

4H-SiC pin diodes are fabricated on the epilayers grown as described previously. Thick n^- drift layers with doping below $1 \cdot 10^{15} cm^{-3}$ and thin p+ anode cap layers with doping more than $5 \cdot 10^{18} cm^{-3}$ are grown in separate runs in our CVD system. There are two sets of pin diode masks are used in this work. One set consists of circular patterns of different diameters (100 μm ~ 2 mm), which is used to fabricate pin diodes for electrical tests. The other set consists of rectangular patterns with wide open contact areas for LEM experiments. The cross-section of 4H-SiC pin diodes built in this study are shown Fig. 2.19. The mask set for electrical test consists of two levels named p^+ contact and top metal, and the mask set for LEM consists of three levels named mesa, p^+ contact and top metal.

For fabrication of pin diodes used in electrical tests, liftoff lithography is first done using the p^+ contact mask and Ti/Al (100Å/4000Å) anode contact metal is evaporated on the wafer. Thick AZ4620 photoresist is deposited on the wafer surface and patterned to suppress micro-masking. Reactive Ion Etch (RIE) in SF_6 is used to form the mesa structures with a depth of 2 μm. Ni (4000Å) is then deposited on the backside of the sample, which is then annealed in vacuum at temperature of 950^oC for 2 minutes to achieve ohmic contacts on both sides. Finally, Au top layer (4000Å) is evaporated and patterned by liftoff using top metal mask. For fabrication of pin diodes for LEM, fabrication processes are same as described above, except that the mesa structure are formed by using an additional mesa mask and Ti/Ni (100Å/2000Å) is deposited as the RIE masking material.

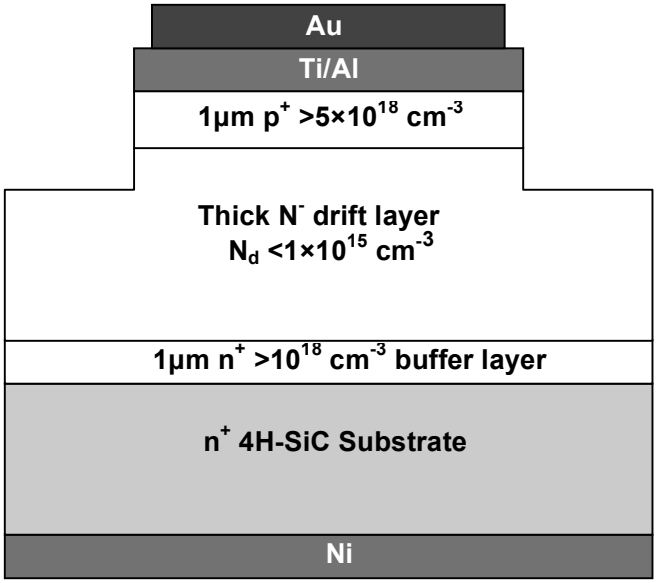


Fig. 2.19. Cross-section structure of 4H-SiC pin diode.

2.1.5.2. Fabrication of 4H-SiC MOS capacitors

4H-SiC MOS capacitors are fabricated on p-type epilayers. A gate-quality oxide is grown by in a pyrogenic system at 1150°C for 120 minutes after RCA clean. The gate material is phosphorus-doped polysilicon. Polysilicon are deposited by LPCVD system using SiH_4 as precursor gas at a temperature of 555 ^{o}C. Phosphorus dopant is introduced by spin-on dopant followed by a drive-in at 900 ^{o}C for 1 hour. After that, the gate and field region are patterned by photolithography and wet etching.

2.1.6. Experimental Results

In this section, experimental results on epitaxial growth of 4H-SiC will be presented first with an emphasis on growth of low-doped epilayers having low BPD densities and high minority carrier lifetimes. Epitaxial growth on both Si-face and C-face will be discussed. Then, results on the fabricated PiN diodes will be presented.

2.1.6.1 Epitaxial Growth of Si-face 4H-SiC

Homoepitaxial growth of 4H-SiC is performed in the Epigress SiC CVD reactor as described in section 3.1. The n-type epilayers used in section 4.1 are 20 μm thick grown on a 5 μm thick highly-doped n-type buffer layer. Substrates used in this study are commercial 2" or 3" Si-face wafers with off-cut angles of 4° or 8° toward the <11-20> direction. Some substrates are re-polished using a chemical mechanical polishing (CMP) technique by NOVASiC.

2.1.6.1.1 Growth rate

The growth rate is investigated as a function of growth parameters, including silane flow and C/Si ratio, and its dependence on substrate off-cut angle is also studied. As discussed earlier, no deposition occurs without silane flow during the growth. We studied the dependence of growth rate on silane flow with a fixed C/Si ratio of 1.5 on Si-face substrates with 8° off-cut angle. The growth rate is plotted as a function of SiH_4 (5% in H_2) mass flow controller (MFC) setting, as shown in Fig. 2.20. The growth rate linearly increases with SiH_4 gas flow in the plotted range. This result is consistent with reports on a similar system by an other group [104]. One advantage of hot-wall CVD reactor is the larger growth rate compared with its cold-wall counterpart (usually with growth rate less than 5 μm/h). The maximum growth rate obtained on our current system is 15 μm/h with a SiH_4 flow of 500 sccm, which is limited by the capacity of the SiH_4 MFC.

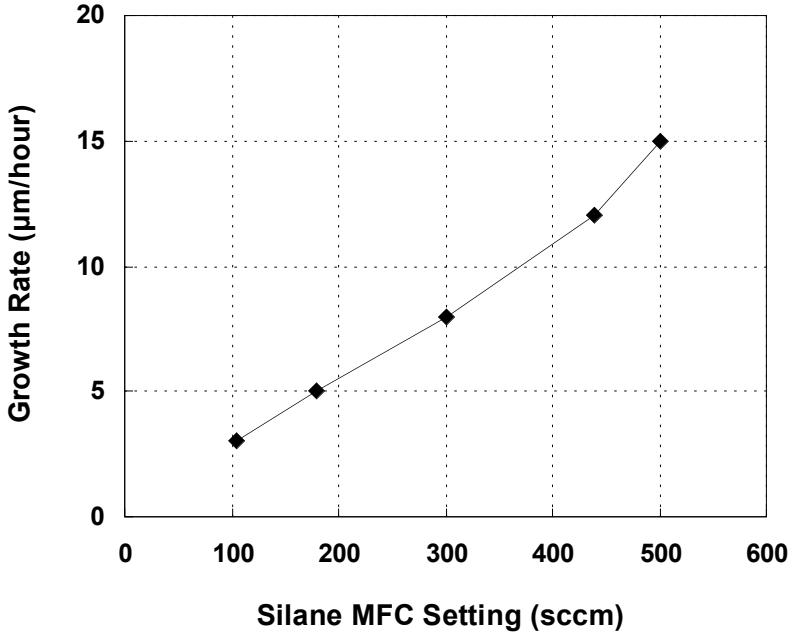


Fig. 2.20. Dependence of growth rate on the silane flow (5% SiH_4 in H_2)

The growth rate dependence on C/Si ratio for both 4° and 8° off-angle Si-face substrates is investigated. The flow rate of C_3H_8 is varied to obtain different C/Si ratios by keePiNg the SiH_4 MFC setting fixed at 360 sccm for all growth runs. Results are shown in Fig. 2.21, where the open and closed diamonds correspond to 4° and 8° substrates, respectively. When C/Si is larger than 1.0, both orientations show constant growth rate, while the growth rate drops substantially between C/Si ratio of 0.5 and 1. This is due to the lack of carbon for C/Si of 0.5, which limits the growth rate. The growth rates on 8° samples are higher than those on 4° samples at various C/Si ratios and under fixed SiH_4 flow. Larger off-cut angles will result in shorter terrace width and higher step density per unit area, which increases the chance of adatom incorporation and promotes step-flow growth. Therefore, an increase in growth rate with increasing off-cut angle is expected. Matsunami and Kimoto studied the growth rate dependence on off-cut angle for 6H-SiC ranging from 0.2° to 10° [6]. They found that the growth rates increase with off-cut angle in the range of 1° to 3.5°, and they believed this is due to the effects of two-dimensional nucleation on terraces even when step-flow growth is the dominant mode. Growth rates become almost constant for off-angles from 4° to 10° in their study. The terrace width can be calculated from $h/tan\theta$, where h is step height and θ is off-cut angle. Assuming step height of two Si-C bilayers (h=0.504 nm) when no macrostep bunching

occurs, the terrace width should be 7.2 nm and 3.9 nm for 4° and 8° substrates, respectively. Based on AFM observations, the actual epilayer surface on 4° substrates has a terrace width of 150-200 nm and a step height of 10-15 nm with severe macrostep bunching, while the epilayer surface on 8° substrates has a terrace width of 10-20 nm and a step height of about 0.5 nm. The terrace width on 4° substrates is nearly ten times longer than that on 8° substrates in this study. Also step flow is slowed down as step height increases with step bunching. All these factors contribute to the larger growth rate difference for the two substrate orientations observed in this work.

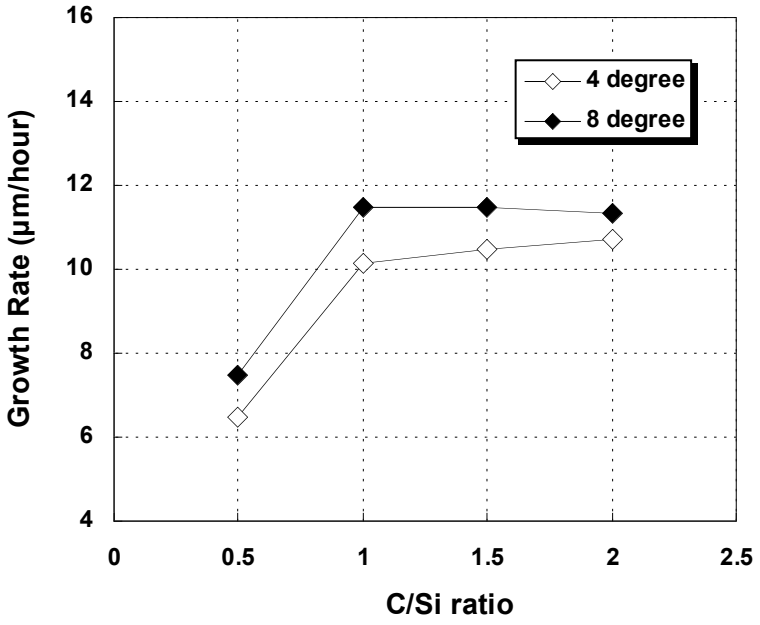


Fig.2.21. Growth rate dependence on the C/Si ratio for both 4° and 8° off-angle substrates.

2.1.6.1.2 Nitrogen doping characteristics

The nitrogen doping is examined in an effort to achieve low-doped epilayers for high power devices. The dependence of net doping concentration on C/Si ratio with a fixed N_2 flow ($7.3 \cdot 10^{-2}$ sccm) and system pressure (150 mbar) is shown in Fig. 2.22, where the open and closed diamonds correspond to 4° and 8° off-angle Si-face substrates, respectively. Doping during SiC epitaxial growth can be controlled by the well-known site-competition technique [22]. Since nitrogen occupies the carbon lattice site, nitrogen doping of the epitaxial layer can be controlled by prohibiting the incorporation of

nitrogen atom under a C-rich condition. The site-competition effect is observed on both substrate orientations. A wide range of doping concentrations have been achieved by adjusting C/Si ratio from 0.5 to 2.0. The lowest controlled doping achieved with a N_2 flow rate of $7.3 \cdot 10^{-2}$ sccm is $1.75 \cdot 10^{-14}$ cm^{-3} for 8° samples and $1.4 \cdot 10^{-14}$ cm^{-3} for 4° samples both at C/Si ratio of 2.0. A background doping of $1 \cdot 10^{-13}$ cm^{-3} has also been obtained on 8° substrates.

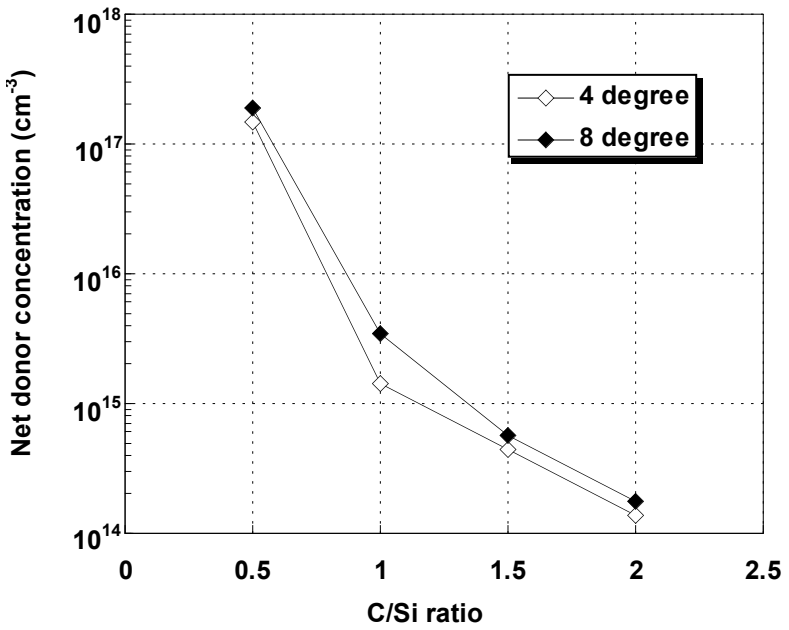


Fig. 2.22. Net donor concentration dependence on C/Si ratios for both 4° and 8° off-angle substrates.

Comparing the net doping concentration for two different substrate orientations, we found that the net doping concentrations on 4° samples are consistently lower than that on 8° samples at various C/Si ratios as shown in Fig. 2.22. This result is consistent with previous studies on doping incorporation as a function of off-cut angles [64, 105]. Yamamoto, et al., reported that nitrogen doping concentrations in 4H-SiC epilayers become higher on both (0001) Si-face and (000-1) C-face substrates as off-cut angles increase from 4° to 8°. Forsberg, et al., studied nitrogen doping behavior on 3.5^o off-angle 6H-SiC and 8° off-angle 4H-SiC, and found the doping on the 4H polytype is about 60% higher than that on the 6H material [64]. It is believed that nitrogen is incorporated at steps in step-controlled epitaxy with a sticking coefficient of almost unity [106]. For large off-angle samples, there are more steps per unit area and more available incorporation

sites for nitrogen atoms. This explains the larger net doping concentrations on 8° samples. Therefore, growth on low off-angle substrates is beneficial in terms of obtaining low-doped epilayers for power device applications.

The dependence of net doping concentration on growth pressure with a fixed N_2 flow ($7.3 \cdot 10^{-2}$ sccm) is shown in Fig. 2.23, where the closed and open diamonds correspond to C/Si ratio of 1.5 and 1.75, respectively. For both C/Si ratios, the nitrogen doping concentration decreases as the growth pressure decreases. Similar observations have been reported by Forsberg, et al., [64]. The decrease of nitrogen doping is attributed to two changes that happen when the pressure in the growth chamber is reduced. First, the partial pressure of nitrogen-containing species is reduced as the total system pressure is reduced. Secondly, the effective C/Si ratio (or carbon coverage on the surface) is increased as the total pressure is reduced. Both phenomena contribute to the reduction of nitrogen doping concentrations. Therefore, reduced growth pressure is very efficient in decreasing the nitrogen incorporation in the grown epilayers. However, the capacity of process pump limits the low pressure that can be achieved. The lowest pressure of 50 mbar has been used in our current CVD system with moderate system performance stability.

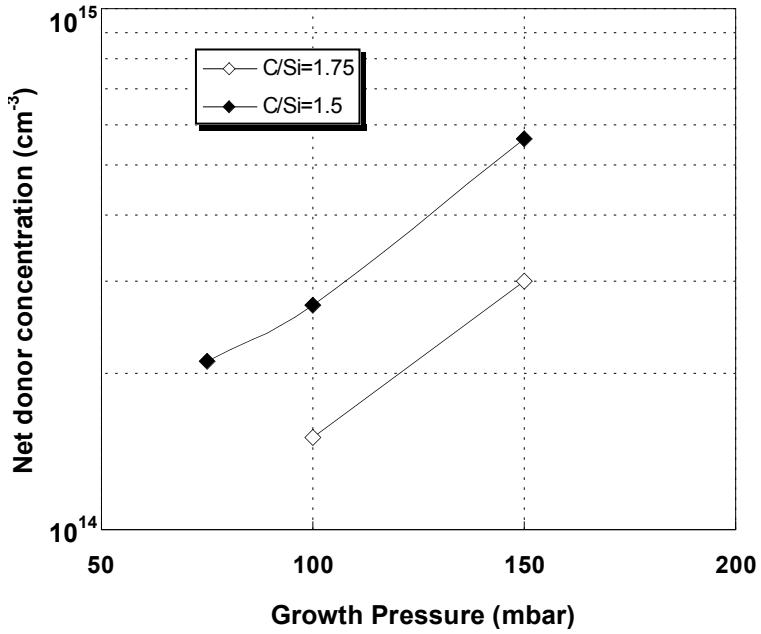


Fig. 2.23. Net donor concentration dependence on growth pressure for two different C/Si ratios.

2.1.6.1.3 Surface morphology

Surface morphology of the epilayers is characterized by both Nomarski microscopy and AFM. Different morphologies of the epilayers grown on Si-face substrates with different off-cut angles are studied. Effects of growth parameters on surface morphology are also investigated.

Figure 2.24 shows Nomarski micrographs for epilayers grown on 4° and 8° off-angle Si-face substrates at various C/Si ratios. Smooth surfaces have been obtained on all 8° samples, while extensive macrostep bunching can be seen on the 4° samples. For 8° samples, the total density of large surface defects (e.g. carrots, comet tails and triangular defects) is usually less than 10 cm^{-2} for various C/Si ratios, while the total density of large surface defects on 4° samples is usually less than 1 cm^{-2}. It was reported that triangular-shaped 3C inclusions were often found on 4H-SiC epilayers grown on substrates with low off-cut angles [11, 107]. However, the epilayers grown on 4° substrates in this study have extremely low surface defect densities, which is not consistent with some earlier reports. The formation mechanism of 3C-SiC inclusion has been studied by several groups [58, 108-110]. Some authors believed 3C inclusions result from step bunching which promoted 3C nucleation by generating longer terraces; others believed that 3C nucleation originated from substrate imperfections or bulk defects. Based on our results, there is no direct correlation between the 3C-inclusion and step bunching. The reduced density of 3C defects on the low off-angle samples in this study compared with earlier reports may be simply due to the improved substrate quality. Micropipes with clear hollow cores (white arrow “A” in Fig. 2.24) can be observed on the 8° sample when C/Si ratio reaches 2.0. As C/Si ratio is reduced to 0.5, there are no micropipes observed on the epilayer. It has been shown that the dissociation of micropipes into elementary screw dislocations can be promoted by growth under low C/Si ratio conditions [48, 67]. Therefore, it is believed that the micropipe shown in Fig. 2.24 is the unfilled micropipe penetrating from the substrate under the relatively high C/Si ratio growth condition.

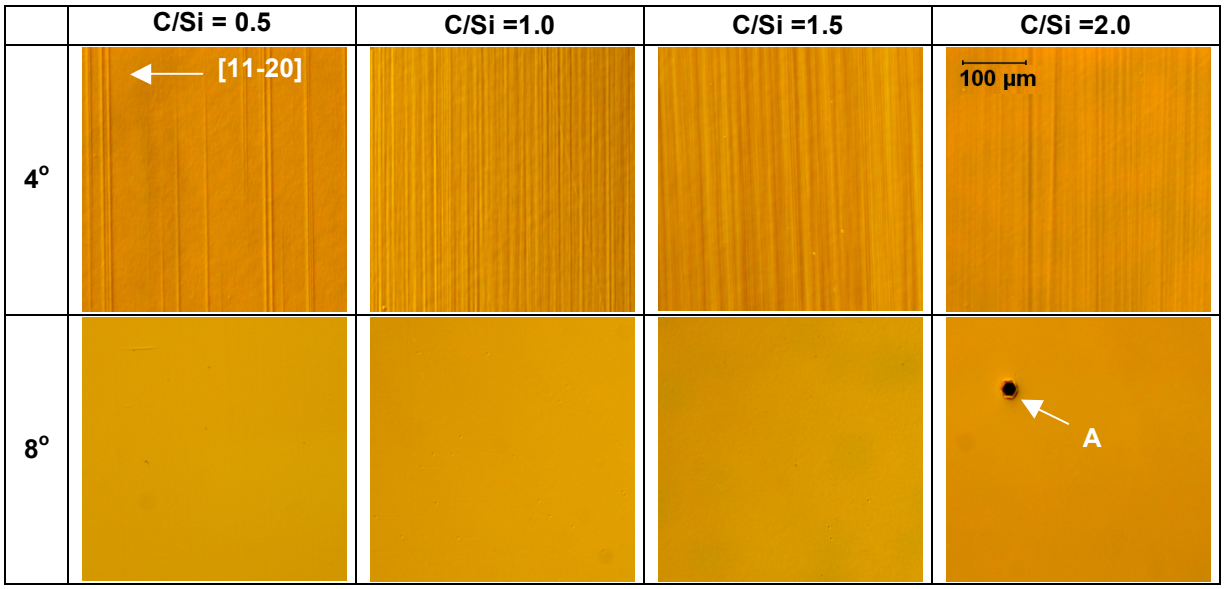


Fig. 2.24. Nomarski micrographs of epilayers grown at various C/Si ratios on substrates with different off-cut angles. Arrow "A" is the unfilled micropipe propagating from the substrate.

A detailed investigation of surface morphology is carried out by AFM in tapping mode. Figure 2.25 is the corresponding AFM images of the samples shown in Fig. 2.24. Surface roughness defined as the root mean square (RMS) for each sample is measured on more than 5 images, and minimum and maximum RMS values are listed in Table 2.3. For 4° off-angle samples, macrosteps with height of 10-15 nm are characteristic of all surfaces. These macrosteps are perpendicular to the [11-20] off-cut direction. Step crossover (white arrow "B" in Fig. 2.26) has been observed on the sample grown at C/Si ratio of 2.0. The distribution of the macrosteps also changes with the C/Si ratio. At relatively high C/Si ratio (larger than 1.5), macrosteps are periodic almost all over the sample with step spacing of about 0.2-0.4 µm. At the C/Si ratio of 1.0, the spacings between macrosteps increase and become irregularly distributed ranging from 0.5 µm to over 3 µm, and the region between the macrosteps is very smooth consisting of steps with single-bilayer height. When C/Si ratio is reduced to 0.5, macrosteps are further separated from each other with spacings up to 100 µm. The area between the macrosteps has relatively flat surface as shown in the corresponding AFM image, which consists of steps with about 2-nm height. As indicated in Table 2.3, the change in the distribution of the macrosteps results in an increase of RMS roughness with increasing C/Si ratio. No

macrostep is observed on the surface of 8° samples, which is evident on both Nomarski micrographs and AFM images. Steps with height of less than 0.5 nm (one or two bilayers) can be seen on the AFM images for all the 8° samples. The spacing between steps does not show significant change with C/Si ratio. As C/Si ratio goes up, the percentage of steps with single bilayer height increases. This leads to a decrease in RMS roughness as indicated in Table 2.3, with an exception of the sample grown at C/Si ratio of 2.0. Hillocks with height of 2-3 nm (white arrow "C" in Fig. 2.25) have been observed on the sample grown at C/Si of 2.0. The presence of hillocks increases the RMS roughness for the sample grown under this condition.

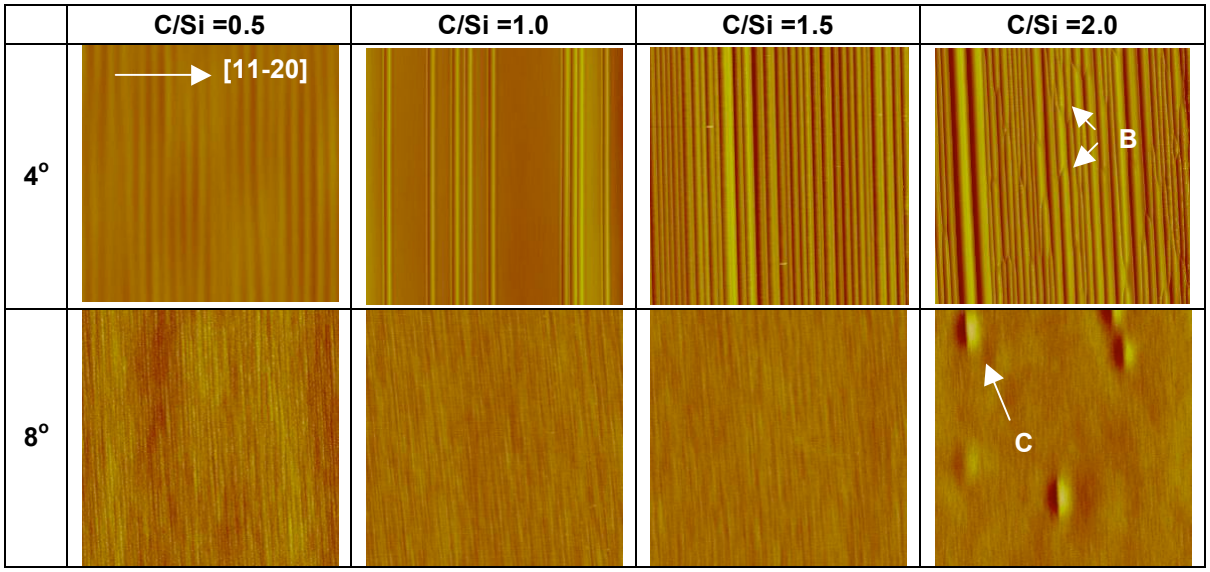


Fig. 2.25 AFM images of epilayers grown on 4° and 8° off-angle Si-face substrates at various C/Si ratios. For 4° samples, scan size and color scale are 10×10 μm and 50 nm, respectively; for 8° samples, they are 2×2 μm and 10 nm respectively, except that the image for C/Si =2.0 has a scan size of 5×5 μm. Arrow "B" is the step crossover and arrow "C" is the hillock found on the epilayers grown at C/Si ratio of 2.0.

Table 2.3 RMS roughness for epilayers grown on 4° and 8° substrates with various C/Si ratios.

Substrate types	RMS_{min} / RMS_{max} (nm) at various C/Si ratios			
	C/Si=0.5	C/Si=1.0	C/Si=1.5	C/Si=2.0
4° off-cut angle	0.8 / 3.5	1.4 / 3.2	4.0 / 5.5	4.5 / 6.4
8° off-cut angle	0.25 / 0.33	0.18 / 0.25	0.17 / 0.18	0.3 / 0.45

Powell, et al., reported the surface morphologies on epilayers grown on 4H-SiC substrates with off-angles from 0.1^o to 3.5^o [11]. Macrostep bunching with variable separations was observed in epilayers grown on 3.5^o off-angle substrates in their study. Saitoh and Kimoto studied the epitaxial growth on 4H-SiC substrates with off-angles from 1° to 45° [12]. Deteriorated surfaces have been reported on substrates with off-angle smaller than 4°. Current data show that a tendency for macrostep bunching is greater at smaller tilt angles and step separation depends on C/Si ratio. The step bunching mechanism in SiC has been studied by several groups [111-114]. Kimoto, et al., investigated step bunching behavior on 6H- and 4H-SiC epilayers grown by CVD on 5° off-angle substrate using AFM and transmission electron microscopy (TEM) [114]. They found that three bilayer height steps predominate on 6H-SiC epilayer and four bilayer height steps on 4H-SiC epilayer. They discussed step bunching behavior in terms of surface equilibrium process, in which the surface free energy is minimized during growth. The different step velocities for each Si-C bilayer promote the formation of the half-unit-cell steps. Periodically changing bond configuration at step edges may further induce these steps to bunch into unit-cell height steps. However, this mechanism does not explain continued coalescence of the unit-cell size steps into macrosteps with multiple unit-cell height. Also, it does not explain different step bunching behaviors observed on different off-angle substrates. Ohtani, et al., studied step bunching behavior on the 6H- and 4H-SiC crystal grown by physical vapor transport (PVT) method [112]. They discussed the mechanism of macrostep formation by considering the interplay between step energetics (repulsive step interaction) and asymmetric step dynamics on the growing crystal surface.

A complete explanation of the differences in macrostep formation observed on 4° and 8° substrates is still not in hand. One note of comparison between 4° and 8° substrates is the resolved component of the surface along the c-axis of 4H-SiC. This component is

approximately two times greater for 8° samples than it is for 4° samples. Nakagawa, et al., have pointed out that atomic planes of the form (11-2n) have a local minimum in surface free energy [115]. The larger (11-2n) component of surfaces on 8° substrates may help to stabilize the morphology. Enhanced macrostep formation on 4° substrates may be driven by the surface attempting to lower its overall surface energy by forming large-area facets with (0001) and (11-2n) orientations. Regular spacing of macrostep edges has been observed in this study, which implies there is a strong repulsive step interaction on the surface [112]. Marchenko and Parshin derived an analytical expression for the elastic potential between two identical steps at the surface of an isotropic solid [116]:

$$U(x) = \frac{2(1-\sigma^2)}{\pi E}(f^2 + \beta a)^2 \frac{1}{x^2} \qquad \textbf{(4.1)}$$

Here, E and σ are Young's modulus and Poisson's ratio, respectively; f and β are the surface force and surface tension at steps, respectively; a is the step height and x is the distance from the step. While a repulsive force would lead to a regular spacing between macrosteps, Marchenko-Parshin (MP) model indicates a near infinite and unphysical repulsive interaction as steps merge, which would preclude the formation of macrosteps. Therefore, an attractive interaction of steps is missing in the treatment of Marchenko and Parshin [117, 118]. Kukta, et al., proposed a new model for the interaction energy on a stepped surface by introducing a roughness correction to MP model [118]. They found that step interactions between a bunched step and a single step switch from repulsive to attractive as separation distance decreases, and this happens only when the bunched steps exceed a certain height. Based on this model, it is reasonable to believe that the short-range attractive step interactions facilitate the formation of macrosteps, while the regular step structure is maintained by the long-range repulsive step interaction. In addition, step bunching is also influenced by kinetic factors, as the dependence of macrostep formation on step flow, which is dependent on C/Si ratio, has been identified.

Step crossover was observed on the 4° sample grown under a C/Si ratio of 2.0. Similar phenomenon, which is referred to as anisotropic step-bunching, has been reported on the 4H- and 6H-SiC epilayers grown by liquid phase epitaxy (LPE) [113]. It is believed that step crossover is a competition effect of different temperature-dependent lateral growth velocities in <1100> and <1120> directions. Data from this study suggest the C/Si ratio also has an impact on the growth velocities in different directions. Nakamura, et al., also found that a high C/Si ratio enhances spiral growth and a low C/Si ratio enhances step flow growth [9, 119]. Therefore, it is believed that the occurrence of step crossover is due to the enhanced lateral growth along <1100> direction under a high

C/Si ratio. This also provides a possible explanation of the hillock formation on the 8° off-angle substrates under high C/Si ratio, which is the result of inhibited step flow growth with respect to lateral spiral growth.

It is reported that step bunching is enhanced under C-rich condition [111]. This is consistent with the current study on 4° samples, but not on 8° samples. Based on the discussion in the preceding paragraph, step flow is promoted at low C/Si ratio. Under the same condition, fast-moving steps will have less chance to come together forming macrosteps, which is consistent with our observation that the area with macrostep bunching decreases with decreasing C/Si ratio for 4° substrates. However, this cannot explain the slight increase in the degree of step bunching with decreasing C/Si ratio for 8° substrates. This implies different mechanisms may dominate step bunching of different height.

Based on the discussion above, surface morphologies for epilayers grown on 4° off-angle substrates need to be improved in terms of step bunching. The macrostep bunching is greatly suppressed in the current investigation by reducing the growth rate from the usual 10 μm/hour to 3 μm/hour. A relatively flat surface with RMS roughness of 0.35 nm has been achieved, and the percentage of flat region on the surface is over 90%.

Degree of step bunching has also been studied as a function of epilayer thickness. Epilayers with different thickness has been grown under the same growth conditions. The averaged RMS roughness of the epilayers as a function of thickness is shown in Fig. 2.26. Surface roughness increases from 4.3 nm to 5 nm when epilayer thickness increases from 10 μm to 60 μm. Although this increase is not desirable for thick epilayer growth, our current results indicate that the increase of roughness with thickness is not dramatic. For critical device applications, the epilayers can be polished using CMP to remove the nanometer scale steps. Additional device layers, for example p-type anode layer in the PiN diode structure, can be grown with slower growth rate and lower C/Si ratio to minimize the step bunching on 4° off-angle substrates.

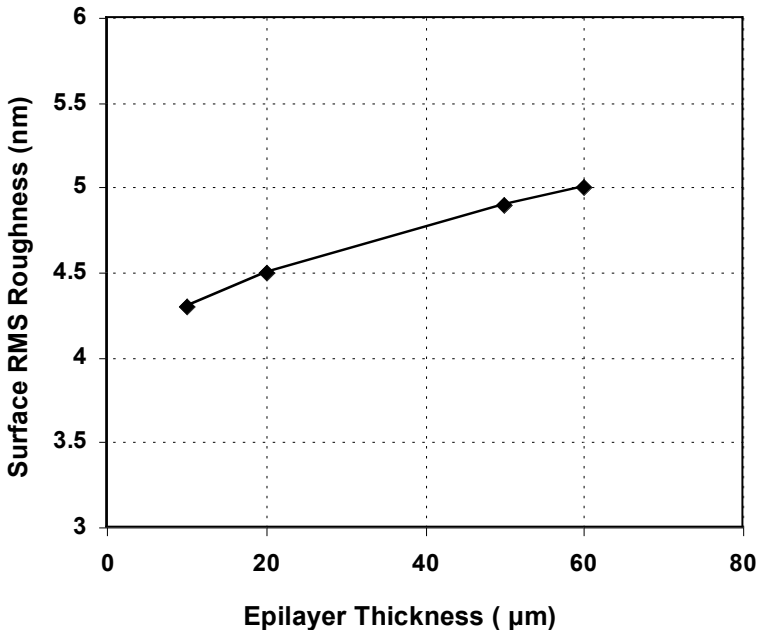


Fig. 2.26. The averaged RMS roughness of the epilayers as a function of thickness

2.1.6.1.4 Basal plane dislocation density

Basal plane dislocations (BPDs) have been found to be the root cause of the forward voltage degradation in 4H-SiC bipolar devices. Most of the BPDs are propagated from substrate into epilayers during epitaxial growth. Therefore, it is very important to study the effects of growth parameters and substrate off-cut angle on BPD density. Several techniques have been developed to enhance the conversion of BPDs into threading edge dislocations during the growth, such as KOH etching and lithographic patterning. In this section, experimental results on BPD reduction will be discussed.

Basal plane dislocation density is evaluated by examining and counting etch pits following KOH etching, as discussed earlier. The BPD etch pit densities on epilayer grown on both 4° and 8° Si-face substrates as a function of C/Si ratio are summarized in Fig. 2.27. In general, the BPD densities decrease with increasing C/Si ratio on both orientations. The lowest BPD density on 8° sample is 175 cm^{-2} at C/Si ratio of 1.5, while the lowest BPD density on 4° off-angle sample is 2.6 cm^{-2} at C/Si of 2.0. No pretreatment, such as KOH etching, was performed prior to epigrowth so the intrinsic characteristics of BPD behavior could be observed on 4° and 8° substrates. Comparing two different off-

angle samples, we found that the BPD density has been greatly reduced by growing on low off-angle substrates, especially under optimized growth conditions. The Nomarski micrographs of typical KOH etched sample surfaces are shown in Fig. 2.28. The different shapes for BPD etch pits are the result of the different distances between the dislocation lines and the surfaces for different off- angles. Only one oval shaped etch pit is identified on the Fig. 4.9(a) for the 4° off-angle sample grown under C/Si ratio of 1.5, and BDP-free areas exceeding 2 cm^2 are also observed on the sample grown under C/Si ratio of 2.0. Epilayers grown on 8° substrate under the C/Si ratio of 1.5 still have a relatively high BPD density, as shown in Fig. 2.28(b).

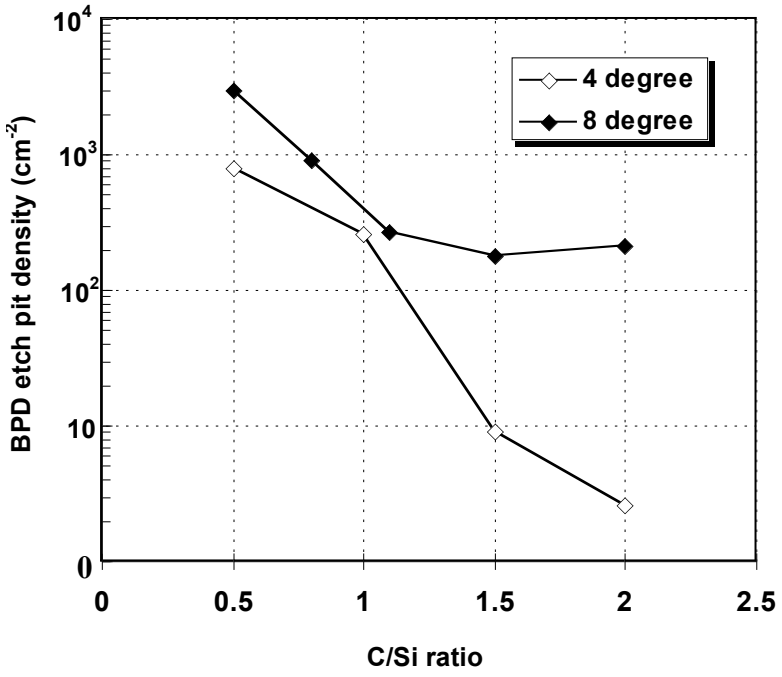


Fig. 2.27. BPD etch pit densities for epilayers on both 4° and 8° off-angle Si-face substrates grown under various C/Si ratios.

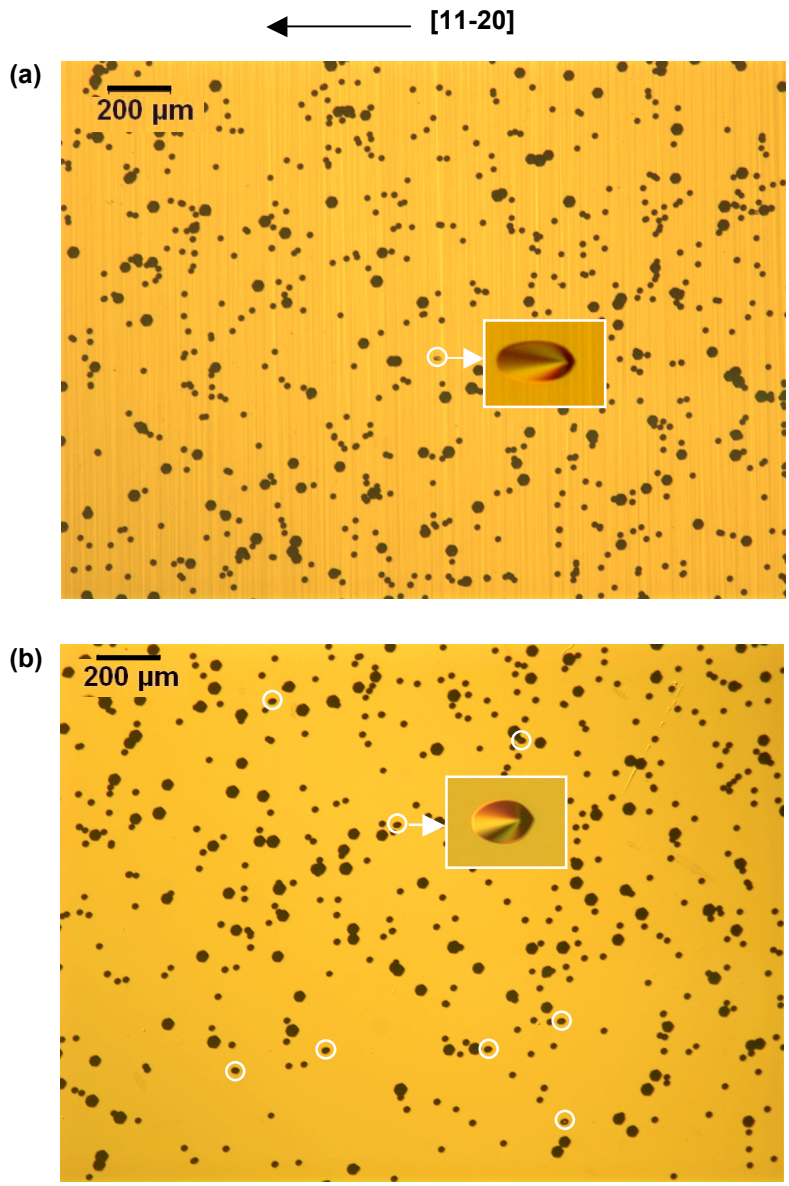


Fig. 2.28. Nomarski micrographs of molten KOH etched surface for (a) epilayer grown on 4° off-angle substrate with C/Si of 1.5, (b) epilayer grown on 8° off-angle substrate with C/Si of 1.5. The white circle are marked for the etch pits corresponding to BPDs. The small insets are large magnification view of BPD etch pits.

The reduction of BPD density on 4° samples is due to the enhanced conversion of basal plane dislocations to threading edge dislocations. Ha, et al., postulated that the image force between the off-axis surface and the basal plane dislocation is the driving

force for dislocation conversion [24]. The image force acting on a dislocation line can be estimated by the equation derived in the conventional isotropic elastic theory:

$$\sigma = \frac{Gb}{4\pi d} \qquad (4.2)$$

Where σ is the shear stress; d is the distance of straight dislocation line from a free surface; G and b are the shear modulus of the materials and the Burgers vector, respectively. Equation (4.2) clearly shows that the shear stress or the resulting image force is inversely proportional to the separation between the dislocation line and free surface. Lower off-angles will result in a smaller separation between the basal plane and the substrate surface, which enhances the image force on the dislocation line. This explains the reduced BPD density on 4° samples.

For both types of substrate orientations, BPD density decreases with increasing C/Si ratio. Ohno, et al., studied the effect of C/Si ratio on the BPD density in the epilayer grown on 8° off-angle 4H-SiC substrates by hot-wall CVD technique [25]. Their results show that BPD density increases for C/Si ratio less than 1.0 and remains almost constant as C/Si ratio exceeds 1.0. This is consistent with our experimental data shown in Fig. 2.26. As discussed in the last section, the relative speed of flowing step to spiral step changes with C/Si ratio. It is possible the reduced BPD densities at high C/Si ratio are the results of reduced step flow speed under the C-rich growth environment, which in turn increases the possibility of BPD conversion into threading edge dislocation.

In the previous section, it is shown that BPD density can be reduced by growing on low off-cut angle substrates under optimized conditions. However, BPD density on 8° off-angle substrates is still high (> 200 cm^{-2}). Recently, some pre-growth treatment techniques have been developed to enhance the BPD conversion to TED [65, 120]. One of the techniques is to subject the SiC substrates to a molten KOH defect etching before the epitaxial growth. Because of the preferential etching of defects by molten KOH, etch pits will be produced on the substrates. When a standard epitaxial growth is performed on the etched substrates, BPD density is found to be dramatically reduced.

Based on the above idea, a series of growth experiments has been performed to evaluate this technique. 4H-SiC substrates with 8° off-cut angle were etched in molten KOH at a set temperature of 520^oC for different time, followed by standard epitaxial growth. In the first set of samples, the KOH etching time is 1 minute and 3 minutes, followed by a 100-μm epitaxial growth. Fig. 2.29 is the Nomarski micrographs of samples before and after growth under different etching conditions. It is observed that the

etch pit size increases with increasing KOH etching time. Beside the etch pits, polishing scratches also become more pronounced after KOH etching. After growth, surface defect densities on KOH etched samples are much higher than the un-treated sample. It has been found that the conversion efficiency of BPDs increases with the size of etch pits [120]. In the second set of samples, the KOH etching time is 2 minutes, 5minutes and 8 minutes, followed by a 30-μm epitaxial growth. BPD densities as function of etching time are plotted in Fig. 2.30. It is found that BPD density decreases dramatically with KOH etching up to 5 minutes. The lowest BPD density obtained using this technique is around 40 cm^{-2} with KOH etching time of 3 and 5 minutes. This number is still higher compared with the reported low BPD densities (<10 cm^{-2}) using the similar technique [2, 121]. This may be due to the high BPD density in the substrates used in this study or non-optimized KOH etching process. The BPD etch pit density for the sample etched for 8 min before growth is very high, and only part of bar is shown in the Fig. 2.30.

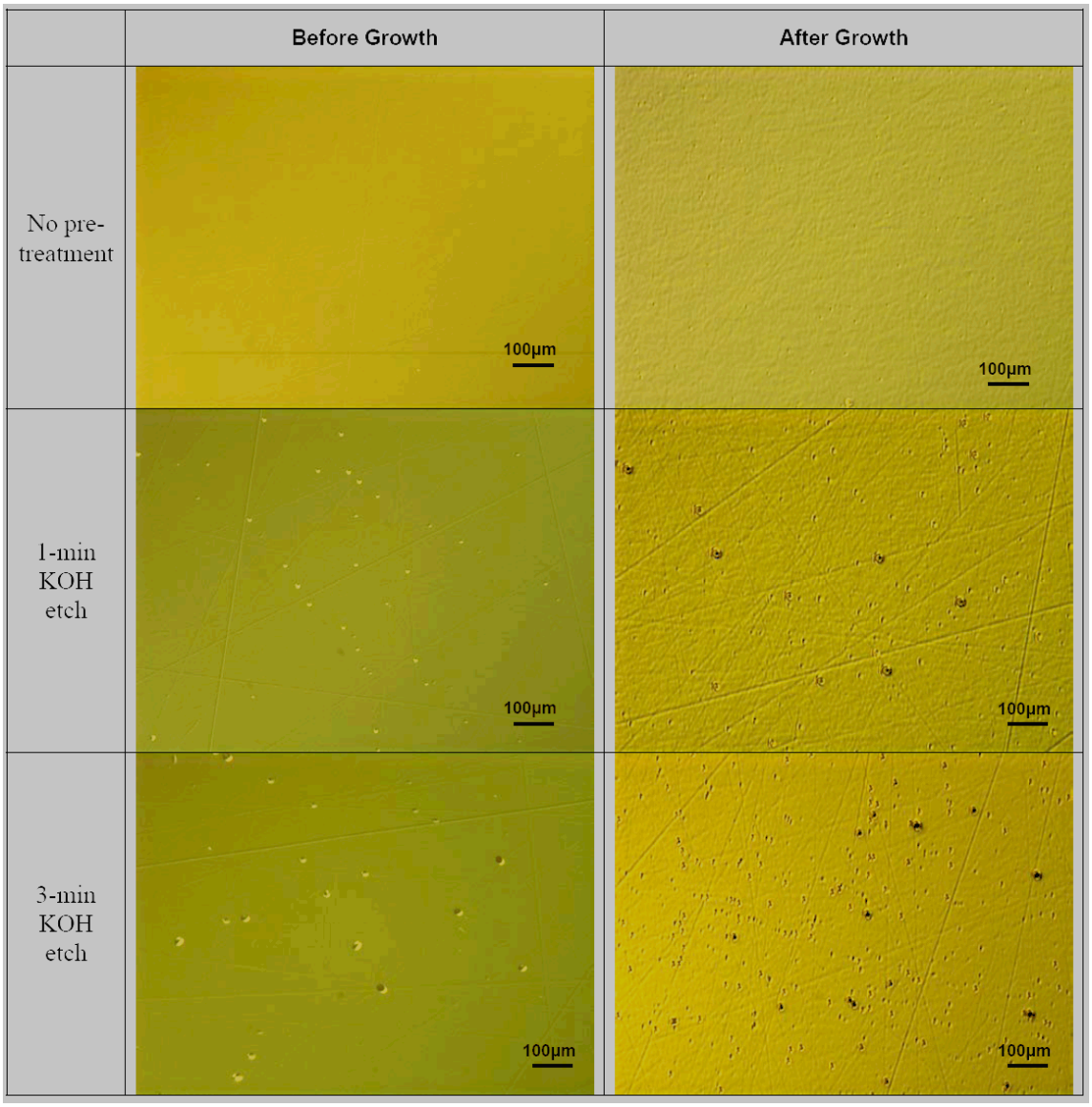


Fig. 2.29. Nomarski micrographs of samples before and after growth under different etching conditions.

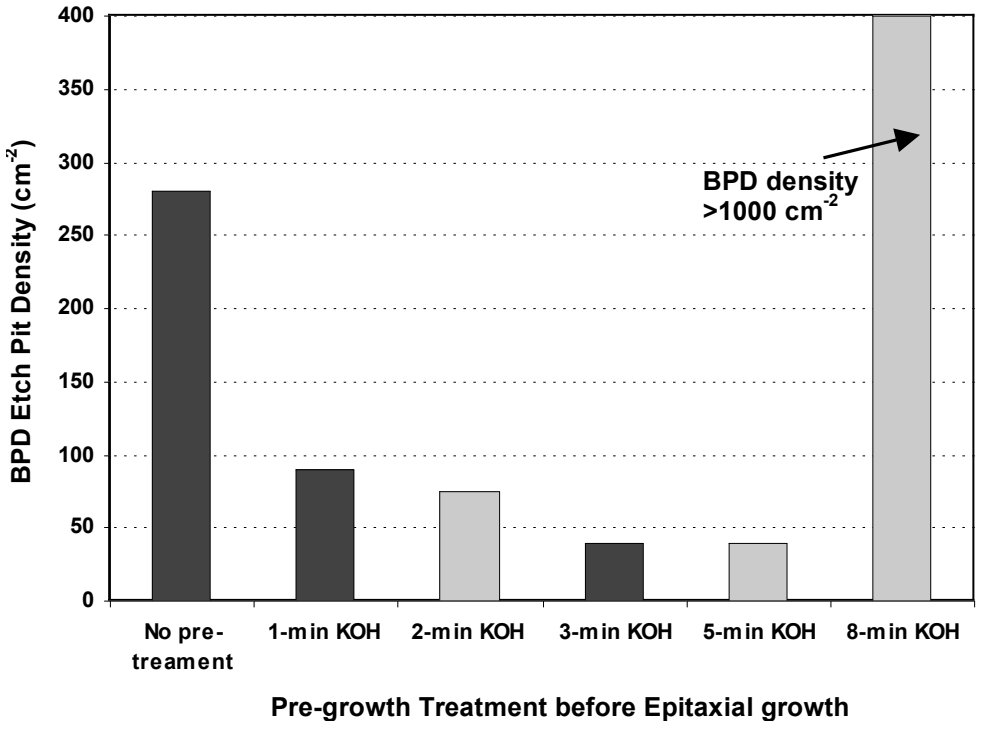


Fig. 2.30. BPD etch pit densities under different pre-growth treatments. The dark gray bars are results from first set of samples, and the light gray bars are from second set of samples.

When excessive pre-growth KOH etching is performed (8 minutes), BPD density increases sharply to over 1000 cm^{-2}. Figure 2.31 is the Nomarski micrograph of KOH etched epilayer with 8 minutes pre-growth KOH etching. Stacking faults which show as vertical lines are identified in the micrograph, and BPD etch pits are found to be aligned along the stacking faults. Moreover, BPD etch pits which have different orientation are also observed on the surface, as indicated in Fig. 2.31 as white circles. It is believed that the high BPD density under excessive KOH etching condition comes from the generation of new BPD during the epitaxial growth. Although most BPDs from substrates are converted into TEDs during the initial state of growth, new BPDs generated during the subsequent growth account for the increased BPD density in the epilayer. Therefore, the KOH etching process has to be carefully designed to minimize this effect.

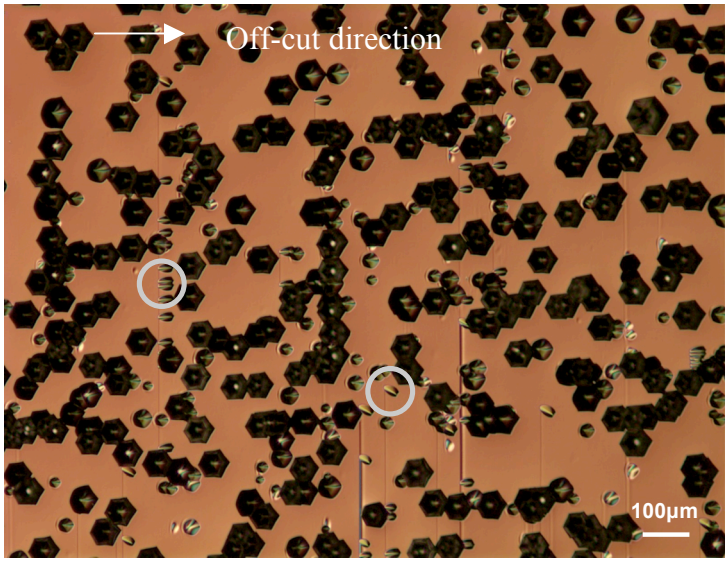


Fig. 2.31 Nomarski micrograph of KOH etched epilayer with 8-min pre-growth KOH etching. The BPD etch pits inside two white circles are BPDs with different orientations.

The mechanisms of enhanced BPD conversion by KOH etching has been discussed in terms of etch pit geometry by Sumakeris [2, 122]. As we discussed earlier, the driving force of BPD conversion is the image force on BPDs near a surface. Selective etching of SiC by KOH creates etch pits around BPDs with a cross-section as shown in Fig. 2.32. The bottom of the etch pit roughly parallels the basal plane of the crystal, which locally reduces the off-axis angle close to a BPD. The image force which promotes the BPD conversion is inversely proportional to the distance between the dislocation and the surface, as described in Equation (4.2). So if the BPD shown as dotted line in Fig. 2.32 propagates into the epilayer as a BPD, it would experience a large image force that promotes a conversion into TED.

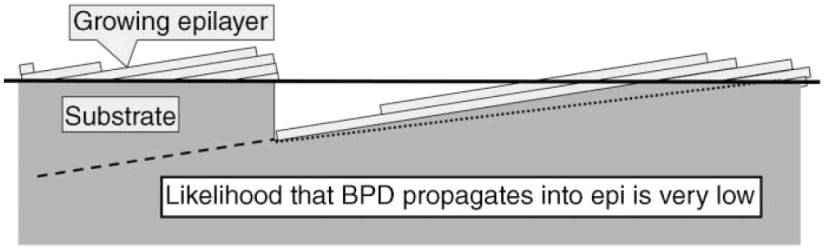


Fig. 2.32. SiC epilayer growth within a KOH etch pit associated with a basal plane dislocation [2].

We can also reduce the BPD by lithographic patterning of the growth substrate. In this technique, SiC substrate surface is patterned by using photolithography method. Hexagonal patterns are etched by reactive ion etching (RIE) to a depth of ~0.3 μm using photoresist as mask. The substrate surface after etching is shown in Fig. 2.33. After patterning, the standard epitaxial growth is performed on the patterned substrates. The BPD density is calculated using molten KOH etching method. The lowest BPD density obtained from this technique is around 50 cm^{-2} in our experiments. This is close to the BPD density we have obtained by using KOH etching technique as discussed in previous section. The exact mechanism behind this technique is still not clear. The BPD conversion may be enhanced through the interaction of BPDs with the sidewalls of the hexagonal patterns.

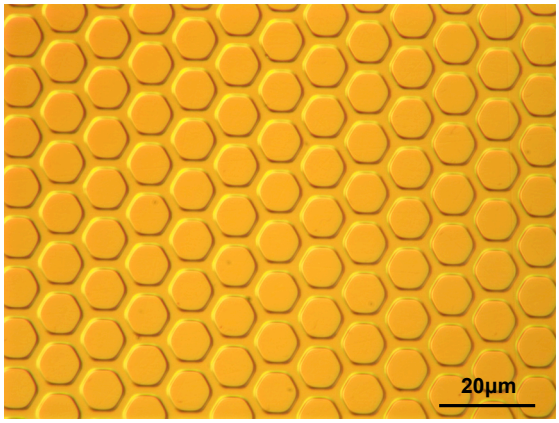


Fig. 2.33. Nomarski micrograph of substrate surface after lithographic patterning.

AFM is used in this case to study how the surface morphology evolves during the growth on the patterned substrates. Figure 2.34 is the AFM images before and after the epitaxial growth. After 7 μm of growth, a flat edge is observed at the up-step direction of the hexagonal pattern (marked as "A" in Fig. 2.34). After 100 μm of growth, the flat regions are connected with each other to form big steps (marked as "B" in Fig. 2.34). The height of the step is more than 1 μm as shown on the height profile on the left side of Fig. 2.34. Formation of huge steps during thick epitaxial growth makes this technique undesirable for high power device applications. In order to solve this problem, a post-growth CMP process is needed to planarize the surface.

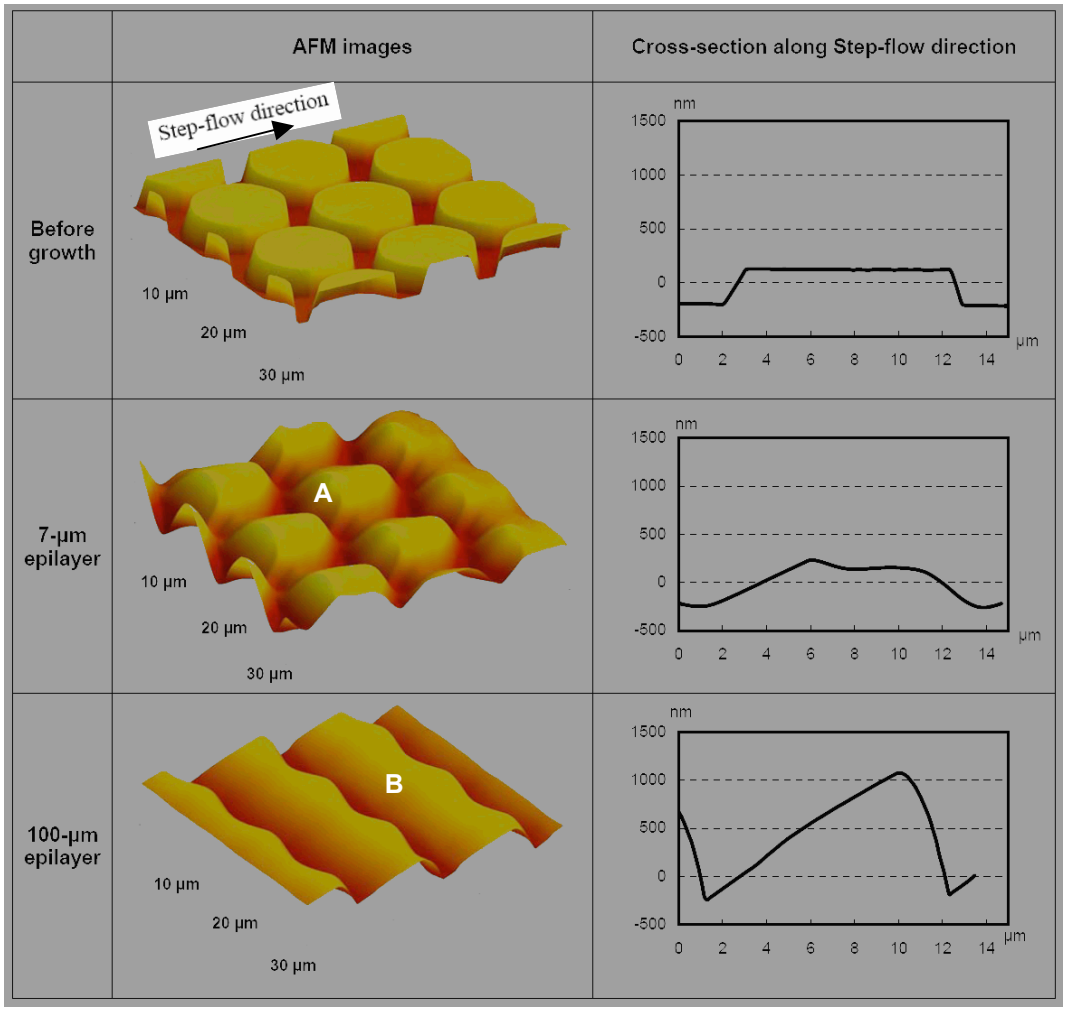


Fig. 2.34. AFM images before and after the epitaxial growth on the substrate with *lithographic patterning. Letter "A" is labeled where the flat edge happened after 7 µm of growth. Letter "B" is labeled where the big step happened after 100 µm of growth.*

In summary, both KOH etching and lithographic patterning techniques has been shown to reduce BPD densities to relatively low level. Further process optimization is needed to achieve very low BPD densities reported in literatures or claimed by other groups. In both techniques, epilayer surface morphology becomes undesirable after growth. CMP process is usually needed to smooth or planarize the epilayer surface for subsequent device fabrication. This means the epitaxial process become more complicated. In comparison, reduction of BPDs by growing on 4° off-axis substrates has the advantages of no added process steps. The disadvantage of growth on 4° off-axis substrates is the increase of surface roughness by step-bunching. However, the step

height from step bunching is the range of several nanometers and can also be removed by subsequent CMP process. Therefore, growth on low-angle substrates is a viable technique to obtain epilayers with low BPD density. We will shown later in that 4H-SiC PiN diodes built on epilayers with 4° off-cut angle exhibit good performance and minimal forward voltage drifts.

2.1.6.2 Epitaxial Growth of Epilayers on C-face 4H-SiC

Up to now, most studies are performed on 8° off-axis Si-face 4H-SiC substrate due to the ease of obtaining good surface morphology and low nitrogen doping concentration. Recently, $(000\bar{1})$ C-face 4H-SiC epitaxial growth has gained some attention due to a few advantages over Si-face. Low basal plane dislocation (BPD) densities are reported on epilayers grown on C-face 4H-SiC substrate [10, 14]. As a result, high-voltage PiN diodes fabricated on C-face show superior forward voltage stability compared with those on Si-face [15, 16]. C-face has also shown to be more suitable for epitaxial growth on low off-cut angle or on-axis substrates [17, 18]. The reduction of off-angle is beneficial in both reducing the substrate price and promoting the conversion of BPDs into threading edge dislocations (TEDs) [17-19]. Additional studies have shown C-face growth is less susceptible to step bunching during epitaxial growth [6, 18, 20, 21]. In view of above advantages, epitaxial growth on 4° off-axis C-face 4H-SiC substrates has been investigated.

2.1.6.2.1 Surface morphology

Figure 2.35 shows Nomarski micrographs for nitrogen-doped epilayers grown under two different N_2 flow conditions with various C/Si ratios. Under high N_2 flow condition (1800 sccm), surface morphology starts to deteriorate at high C/Si ratios. Triangular-shaped defects, which are aligned perpendicular to the off-cut direction, begin to appear on the surface when the C/Si ratio equals 2.0. Further AFM analysis shows the triangular-shaped defects are pits with a typical depth of about 0.8 μm. This type of defect will be referred to later as triangular pit. At C/Si ratio of 3.0, the sample surface is full of wave-like surface defects, which also exhibit triangular-shaped features and alignment perpendicular to the off-cut direction. Under low N_2 flow condition (0.037 sccm), triangular pits are observed on the surface when the C/Si ratio is greater than 2.0, but the densities are much lower than those for high N_2 flow conditions. Triangular pit

densities increase from 10 cm^{-2} to 17 cm^{-2} when C/Si ratio changed from 2.0 to 3.0. The formation mechanism for these defects is still not clear at this time. Since defect densities are higher on the samples grown under high N_2 flow and high C/Si ratio, the presence of excessive N_2 and C promote the formation of those defects.

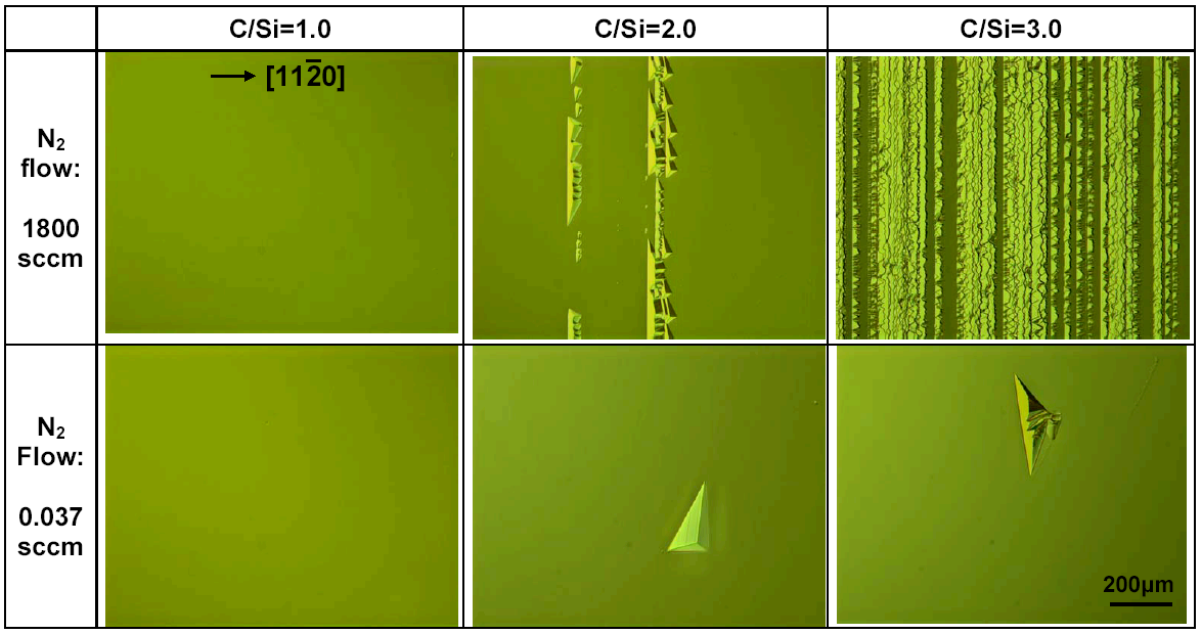


Fig. 2.35. Nomarski micrographs for nitrogen-doped epilayers grown at two different N_2 flow conditions under various C/Si ratios.

Kojima, et al., reported similar surface defects on the 8° off-axis C-face 4H-SiC epilayers [20]. These defects have been identified to be 4H-SiC polytype by micro-Raman analysis. Our AFM analysis indicates the shapes of these defects are similar to an inverted pyramid with well-defined sidewalls. This is quite different from the triangular defects observed on the Si-face 4H-SiC epilayers, which usually show a relatively planar region surrounded by triangular edges [58]. AFM scans on the sidewall of the pits reveal step-bunching behavior, which is often observed during 4H-SiC step flow growth. Therefore, triangular pits observed in this study are believed to be a new type of surface defect only observed on C-face epilayers. Since the surface of the C-face is terminated with C atoms, the formation of C-C bonds is favored under C-rich growth environment [20]. This bond may interrupt step-flow and cause the formation of defects. Under high

N_2 flow conditions, the accumulation of N_2 on the growth surface may also alter the normal step-flow and cause the formation of defects. In fact, nitrogen-induced macrostep bunching has been observed on epilayers grown under high N_2 flow conditions in this study, which will be discussed in a later section.

Considering the large dimensions of triangular pits, their density has to be reduced in order to achieve high-quality C-face epilayers. Based on the results shown in Fig. 2.35, growth under low C/Si ratio is very effective in reducing the density of triangular pits. Although low C/Si ratios can be used to grow the heavily doped C-face epilayers, higher C/Si ratios are usually needed to achieve low doping concentration for power device applications. In order to strike a compromise between these mutually exclusive conditions another parameter, growth temperature, is investigated. Figure 2.36 shows the surface morphology of an epilayer grown at temperatures of 1640 ^{o}C and C/Si ratio of 2.0. Triangular pits are not observed on this sample. However, shallow growth pit density increases dramatically as the growth temperature increases. It is found that surface defect densities are strongly dependent on growth temperature, as summarized in Table 2.4. The triangular pit density decreases with increasing growth temperature, and is completely eliminated at temperature of 1640 ^{o}C. On the other hand shallow growth pit density increases as growth temperature goes up. Based on the data presented in Table 2.4, the optimum growth temperature is believed to be around 1620 ^{o}C, when the densities for both types of defects are reasonably low. Similar trends have been reported on 8° off-cut C-face 4H-SiC epilayers [20]. As discussed previously, the origin of the triangular pit is believed to be due to interrupted step-flow growth. Higher growth temperature will increase the surface mobility of the adatoms and also help to disassociate the C-C bond on the growth surface, which will reduce the triangular pit density. At the same time, the excessive H_2 etching at higher growth temperature may cause the formation of shallow growth pits on the epilayers.

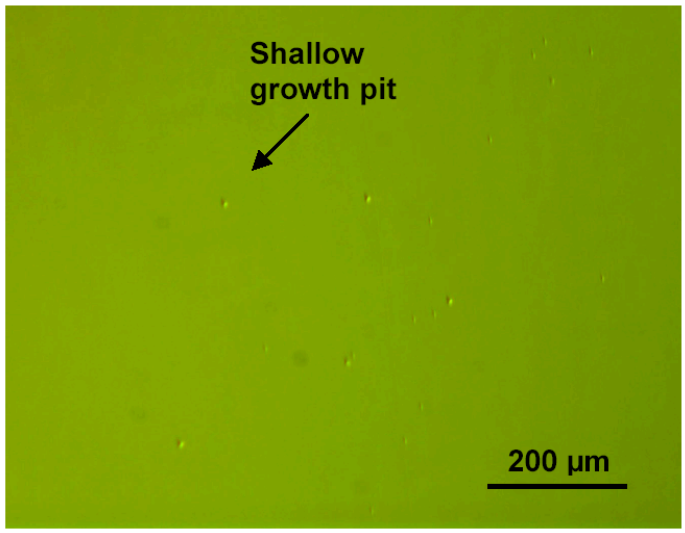


Fig. 2.36. Nomarski micrograph of the epilayer grown at temperatures of 1640 °C and C/Si ratio of 2.0. Black arrow is the shallow growth pit observed on the sample.

Table 2.4 Defect densities on C-face 4H-SiC epilayers grown at different temperatures

Defect types	Growth Temperature		
	T=1600 °C	T=1620 °C	T=1640 °C
Triangular pits (cm^{-2})	10	0.7	0
Shallow pits (cm^{-2})	50	580	3017

2.1.6.2.2 Nitrogen-induced step bunching

In order to study surface features on a smaller scale, tapping-mode AFM is performed on areas of the surface away from surface defects. As shown in Fig. 2.37, macrostep bunching has been observed on the samples grown under high N_2 flow conditions at various C/Si ratios. Step-heights measured fall into a range between 5~15 nm and increase slightly with increasing C/Si ratio. At C/Si ratio of 1.0, equidistant steps are observed on most of the scanned areas with average terrace widths of about 100 nm. As C/Si ratio increases, more step crossovers on the surface are found and terrace widths also become wider in some regions. Surface features change from equidistant steps to meandering steps with increasing C/Si ratios. Under low N_2 flow conditions, surfaces are

very flat without step bunching, and step-heights are about 0.25~0.5 nm (1~2 bilayers). Surface roughness, defined as the root mean square (RMS) displacement from a perfectly flat surface, is measured for each sample and plotted in Fig. 2.38 (a). Surface roughness of the heavily-doped samples is about one order of magnitude higher than that of the lightly doped ones. RMS roughness values increase with C/Si ratio for the heavily doped samples due to the increasing step heights. Roughness remains almost constant with C/Si ratio for the lightly doped samples.

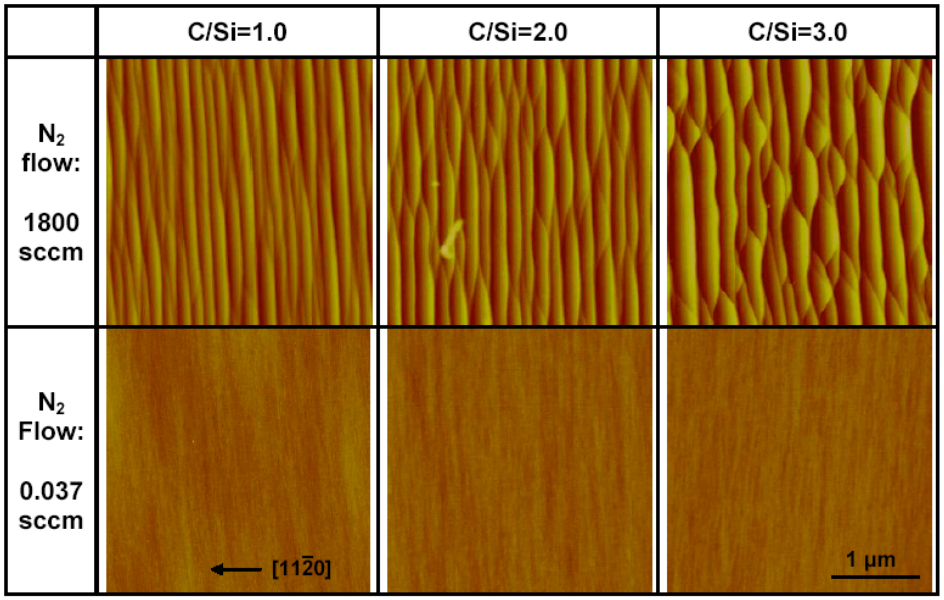


Fig. 2.37. AFM images for nitrogen-doped epilayers grown at two different N_2 flow conditions under various C/Si ratios. Scan size is 3×3 µm for all the images. Color scale is 30 nm and 10 nm for high and low N_2 flow conditions, respectively.

Heavily doped n-type buffer layers are often needed in standard 4H-SiC epitaxial growth, especially for bipolar device applications. The macrostep bunching observed is certainly not desirable. In order to reduce macrostep bunching, the effect of nitrogen flow on step bunching is studied. By reducing the N_2 flow, macrostep bunching is greatly attenuated as observed by AFM (not shown in the paper). RMS roughness measured by AFM as a function of N_2 flow is plotted in Fig. 2.38(b). As N_2 flow is reduced from 1800 sccm to 500 sccm, step height decreases from 5 nm to 0.5 nm and RMS roughness drops from 1.9 nm to 0.3 nm. The dependence of macrostep bunching on nitrogen flow condition indicates that nitrogen plays an important role in promoting step bunching.

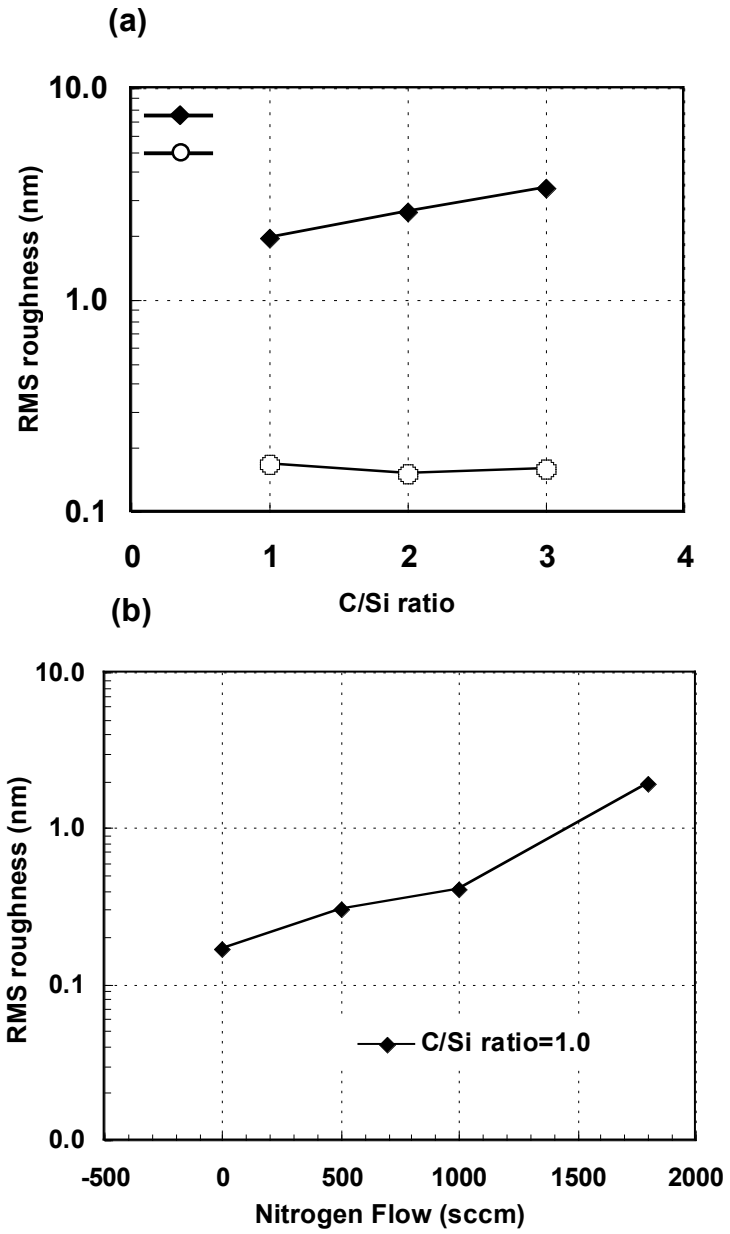


Fig. 2.38. Surface roughness RMS roughness for C-face 4H-SiC epilayers (a) as a function of C/Si ratio under two N_2 flow conditions and (b) as a function of N_2 flow setting.

Nitrogen-induced macrostep bunching has been observed on C-face crystal grown by physical vapor transport (PVT) method [112]. Mechanism of macrostep bunching was discussed through the consideration of the interplay between step energetics (repulsive step interaction) and kinetics (asymmetric step kinetics). However, the strong

dependence of step bunching on nitrogen flow condition indicates that an impurity-related model is more appropriate in our case. It has been realized for a long time that impurities may cause step bunching during growth. A number of models have been proposed to explain this phenomenon. The most widely cited one is proposed by Frank and further developed in several other papers [123-125]. The two-dimensional model proposed by Kandel and Weeks is considered here to explain the experimental data [125]. In this model, a step velocity $f(W)$ is defined as a function of the terrace width (W) located underneath the step. This function behaves differently depending whether impurities are present, as detailed in Kandel's paper. In the absence of the impurities, the velocity function $f(W)$ is an increasing function of the terrace width, and saturates for terraces wider than a characteristic surface diffusion length. Therefore, the step velocity is higher when terraces are wide and small otherwise. This establishes a negative feedback against step bunching, which makes wide terraces shrink and narrow ones grow. With the presence of impurities, the velocity function $f(W)$ is an increasing function of the terrace width W for small terrace width, has a maximum value $V^m=f(W^m)$ at $W=W^m$, and decreases with increasing W for $W>W^m$. If the surface starts with the uniform step train with step spacing $W>W^m$, a perturbation that makes a terrace become wider will reduce the step velocity above that terrace and increase terrace width even further. As a result, the perturbation is amplified and the surface is unstable with respect to step bunching. Although this model can explain impurity-induced step bunching, it does not consider the effect of overall impurity density. In our experimental data, macrostep bunching only happens when nitrogen flow exceeds a certain value as shown in Fig. 2.38(b). Therefore, there must exist a critical impurity density beyond which Kandel's model can be applied.

Different step features are also observed for different C/Si ratios under high N_2 flow condition. As C/Si ratio increases, more step crossovers are observed, and surfaces change from equidistant steps to meandering steps with wider terraces. This phenomenon has been reported as "step bunching anisotropy" on Si-face 6H- and 4H-SiC epilayers grown by liquid phase epitaxy (LPE) [113]. Effects of C/Si ratio on the step bunching anisotropy have also been studied on 4° off-cut Si-face 4H-SiC epilayers in our earlier paper [19]. It is believed that the occurrence of step crossover is due to the enhanced lateral growth along <1100> direction under a high C/Si ratio. The terrace width also increases with anisotropic step bunching, which may be the result of coalescence of the bunched steps. In general, the formation of wavy steps should cost more energy than the straight steps, and this energy is outweighed by the decrease in step repulsion energy as

the separations between the steps increase. Therefore, the total energy is minimized by step coarsening as observed under high C/Si ratios.

2.1.6.2.3 Nitrogen doping characteristics

The dependence of nitrogen doping concentrations on growth parameters is also investigated on C-face 4H-SiC epilayers. Figure 2.39(a) shows the doping concentration as a function of C/Si ratio under both high and low N_2 flow conditions. Under low N_2 flow conditions, the net donor concentrations measured by C-V technique decrease with increasing C/Si ratio. Since the background doping under the similar growth conditions exhibits n-type characteristic, the effect of p-type compensation on the doping can be eliminated. The decrease of doping concentration with C/Si ratio can be explained by the site-competition effect. Similar results have been reported on 8° off-cut C-face 4H-SiC epilayers in some recent papers [17, 126]. However, earlier reports have shown that the doping incorporations on C-face 4H-SiC are independent of C/Si ratio [6, 64]. This discrepancy can be explained by considering the different growth pressures used in different reports. When the growth pressure is low, the carbon coverage on the sample surface is expected to be lower than under atmospheric pressure. Low-pressure conditions promote the site-competition effect on the C-face 4H-SiC observed in this study. On the other hand, the doping concentrations show different C/Si ratio dependence for samples grown under high N_2 flow condition as measured by SIMS technique. The doping concentrations are almost constant when C/Si ratio changes from 1.0 to 2.0, and increase when C/Si ratio changes from 2.0 to 3.0.

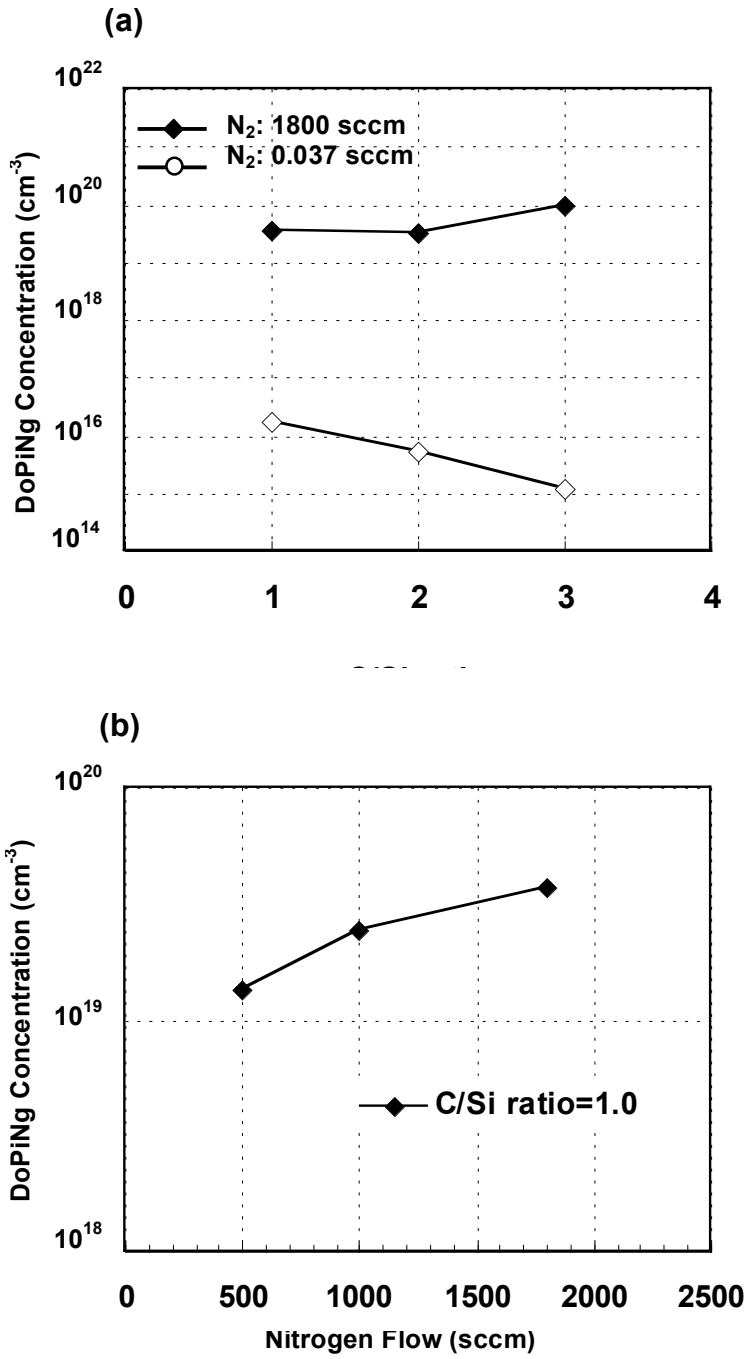


Fig. 2.39. Nitrogen doping concentrations for C-face 4H-SiC epilayers (a) as a function of C/Si ratio under two N_2 flow conditions and (b) as a function of N_2 flow setting. Heavily doped samples (greater than $1 \cdot 10^{-19}$ cm^{-3}) are measured by SIMS. Lightly doped samples are measured by mercury C-V.

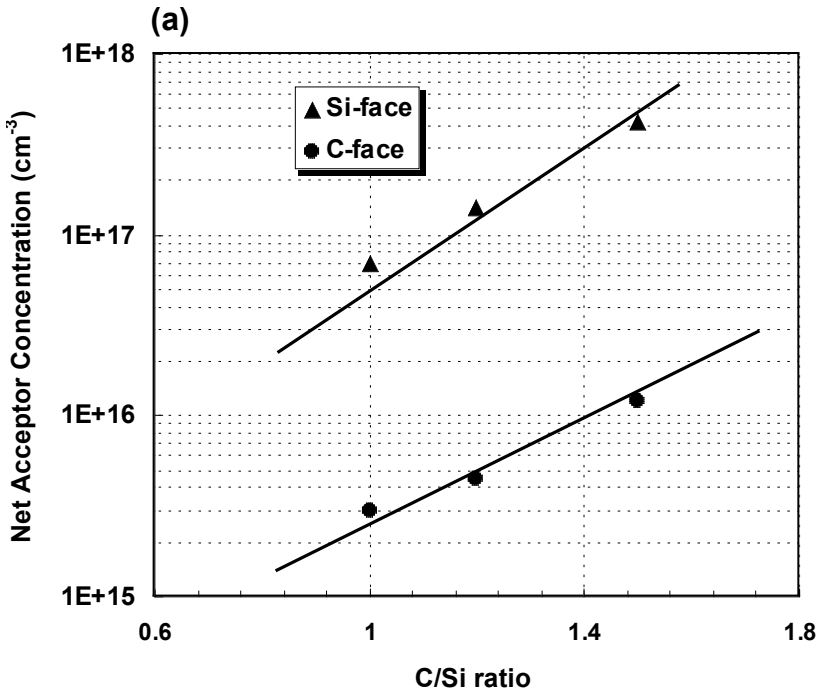
The different doping behaviors under high and low N_2 flow conditions can be explained by considering the nitrogen incorporation process during growth. Based on thermodynamic calculations, it is believed that HNC and HCN molecules are the primary species that contribute to nitrogen doping during growth [64]. The HNC and HCN species will increase when either C_3H_8 or N_2 concentrations increase in the growth environment. When the C/Si ratio (C_3H_8 flow) is increased, two possible mechanisms that compete with each other will determine the dopant incorporation. First the HNC and HCN concentration will increase with C/Si ratio, which will enhance nitrogen incorporation. Second the carbon coverage will increase with C/Si ratio, which reduces the amount of available sites for dopant species. Under low N_2 flow condition, the second process dominates over the first one due to the limited amount of N_2 flow, and this leads to the observed site-competition effect. Under high N_2 flow condition, the first process could balance or even dominate over the second one, which explains the opposite doping dependence on C/Si ratio.

Figure 2.39(b) shows the nitrogen doping concentration as a function of the N_2 flow rate at fixed C/Si ratio of 1.0. Doping concentration increases with increasing N_2 flow. Doping concentrations greater than $1 \cdot 10^{-19}$ cm^{-3} can be obtained when N_2 flow rate is above 500 sccm. As discussed already, surface roughness and step bunching is a function of N_2 flow rate. When nitrogen flow rate is too high, macrostep bunching will happen and results in a large surface roughness. At N_2 flow rate of 500 sccm, the RMS roughness of the epilayer is measured to be 0.3 nm without macrostep bunching. Therefore, both high doping concentration and smooth surface can be achieved by proper selection of N_2 flow condition.

2.1.6.2.4 P-type doping characteristics

P-type doping in the epilayers are achieved by flowing trimethylaluminum (TMA) into the reactor through a bubbler configuration. The TMA source is maintained at a temperature of 19 ^{o}C. The dependence of Al doping concentrations on growth parameters is investigated on both 4° C-face and 8° Si-face 4H-SiC epilayers. Figure 2.40(a) shows the net acceptor concentration as a function of C/Si ratio under fixed TMA flow of 0.83 sccm. On both faces, acceptor concentrations from Al doping increase with C/Si ratio. These results can be well explained by the site-competition theory [22]. Al dopant atoms are incorporated into SiC epilayer by occupying the Si lattice site. Therefore, the incorporation will be enhanced by growing under C-rich environment. These results are

consistent with similar study performed on 8° C-face 4H-SiC epilayers [20]. However, some earlier study has shown that the C/Si ratio did not influence the Al incorporation on C face [106]. The reason for this discrepancy is considered to be related to the growth pressure, similar to the case of nitrogen doping. Under low-pressure condition, site competition effect of Al doping has been observed on both C-face and Si-face. Fig. 2.40 (b) shows the acceptor concentration plotted as a function of the input dopant gas flow rate under fixed C/Si ratio of 1.5. It is clear that Al incorporation is higher on Si-face than that of the C-face under same conditions. Therefore, low C/Si ratio and high Al flow are needed to achieve high p-type doping on C-face.



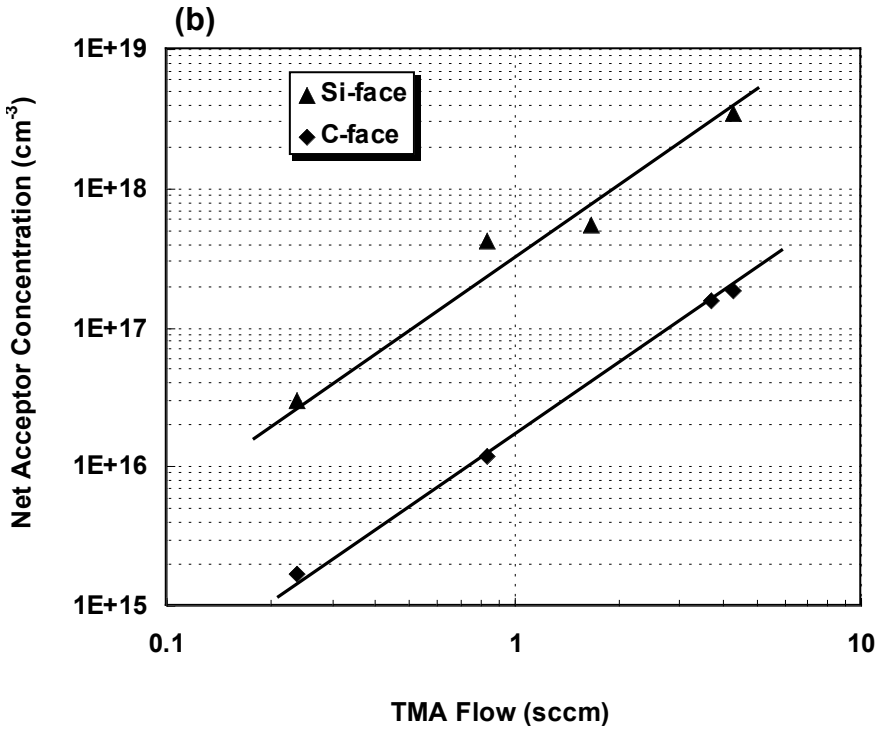


Figure 2.40. (a) Net acceptor concentrations as a function of C/Si ratio under fixed TMA flow of 0.83 sccm; (b) net acceptor concentrations as a function of the input TMA flow rate under fixed C/Si ratio of 1.5.

2.1.6.3 Characterization and Control of Minority Carrier Lifetimes

In this section, carrier lifetimes of n-type epilayers are characterized using EBIC and time-resolved photoluminescence techniques, and that of p-type epilayers are characterized by pulsed MOS capacitor technique. Deep level trap densities in the epilayers are measured using deep level transient spectroscopy (DLTS) technique to identify the lifetime-limiting defects. Purpose of this study is to establish a relationship between deep level trap densities, carrier lifetime and growth parameters. Effective carrier lifetime measured from PiN diode reverse recovery technique will be discussed in a later section.

2.1.6.3.1 Carrier lifetimes in n-type epilayers

Lifetime and deep level concentration on our low-doped n-type epilayer are characterized by using EBIC, photoluminescence and DLTS techniques through the collaboration with Prof. Skowronski group at Carnegie Mellon University. Epilayers used in this study are grown on 8° off-angle Si-face 4H-SiC substrate at various C/Si ratios. Before sending out for measurements, Schottky diodes are fabricated on some of the epilayers. A 3000Å Ni is first deposited on the backside and annealed for backside ohmic contact, and then 500Å thick Ni is deposited and patterned on the sample surface by using liftoff process.

In DLTS, an excitation pulse is applied to the Schottky junction to fill all the traps and then the pulse is removed. The next step is to detect the resulting capacitance relaxation signal from the sample due to the charge emission from the traps at different temperature. From these recorded capacitance transients at different temperatures, a spectrum generated using selected time windows (τ) will exhibit peaks, each one being associated with a deep level. To determine the energy levels of the trap level, the time window is changed. In this case, different DLTS spectra are obtained with the peaks at different temperatures. From the time window and the temperature at which the peak occur, Arrhenius plots are made to determine the defect energy level. Fig. 2.41 is the DLTS spectrum of an n-type epilayer from the measurement. The epilayer used in this measurement is 20 μm thick with nitrogen doping of $2 \cdot 10^{14}$ cm^{-3} grown at C/Si ratio of 1.5. There are three peaks in the spectrum corresponding to traps at different energy levels. The activation energy or E_c-E_T of each trap can be determined by plotting Arrhenius plot as shown in Fig. 2.42. The deep trap energy levels are determined to be 0.16 eV, 0.65 eV and 1.6 eV. They are identified to be Ti shallow donor level, Z_1/Z_2 center and EH_6/EH_7 center respectively according to the data listed in Table 2.2.

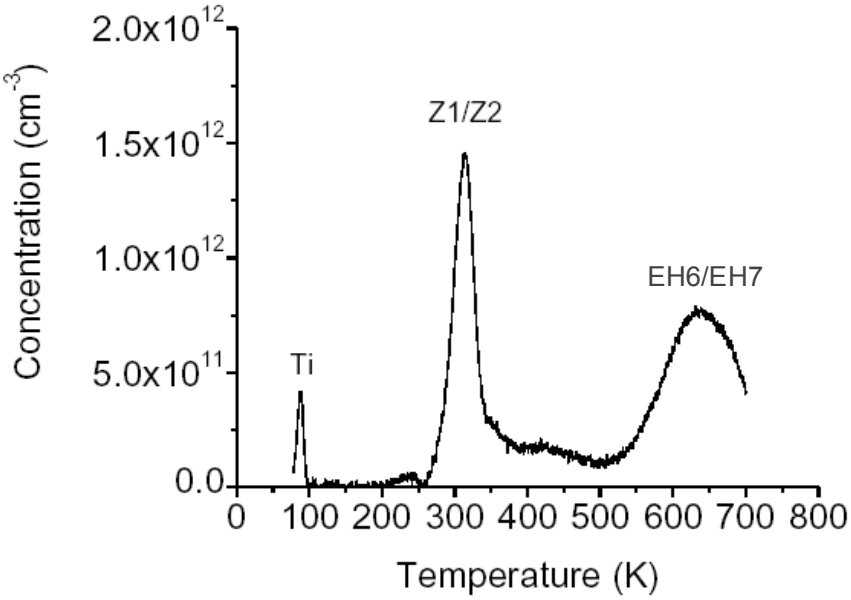


Fig. 2.41. DLTS spectrum from a 20 µm lightly-doped n-type epilayer

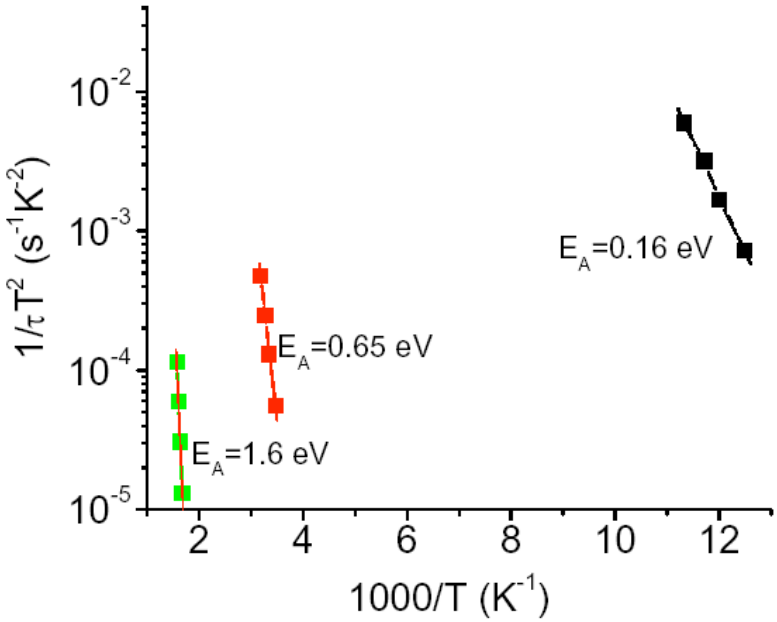


Fig. 2.42. Arrhenius plot of three trap levels observed in DLTS spectrum.

The concentration of Z_1/Z_2 center is the highest among three trap levels, and is estimated to be around $1.4 \cdot 10^{12}$ cm^{-3}. The concentration of EH_6/EH_7 is estimated to be $8 \cdot 10^{11}$ cm^{-3}. Concentrations for both types of deep trap levels are relatively low compared with the results from literature [77, 80, 82], which indicates the high-purity of the epilayer. The low concentration of EH_6/EH_7 centers is especially important to achieve long carrier lifetime since they have a large capture cross-section, and are believed to be the major lifetime killer [127].

The diffusion length of minority carriers is measured using EBIC technique. The electron beam of the scanning electron microscope (SEM) scans along the surface of the Schottky diode that is not covered with metal toward the edge of the Schottky contact. The diffusion length was deduced from the slope of the logarithmic plot of the EBIC signal as a function of the distance from the edge of the Schottky diode. The minority carrier lifetime of the epilayer is then deduced from the diffusion length. The EBIC result for the epilayer grown in this study is shown Fig. 2.43. The curve shows multiple slopes instead of single one as in an ideal case. The relatively sharp slope at small distance gives a short lifetime of 0.12 μs, which is believed to be an effect of surface recombination. The minority carrier lifetime of 1.45 μs is obtained when the beam is some distance away from the contact, which is believed to be close to the bulk minority carrier lifetime of the epilayer.

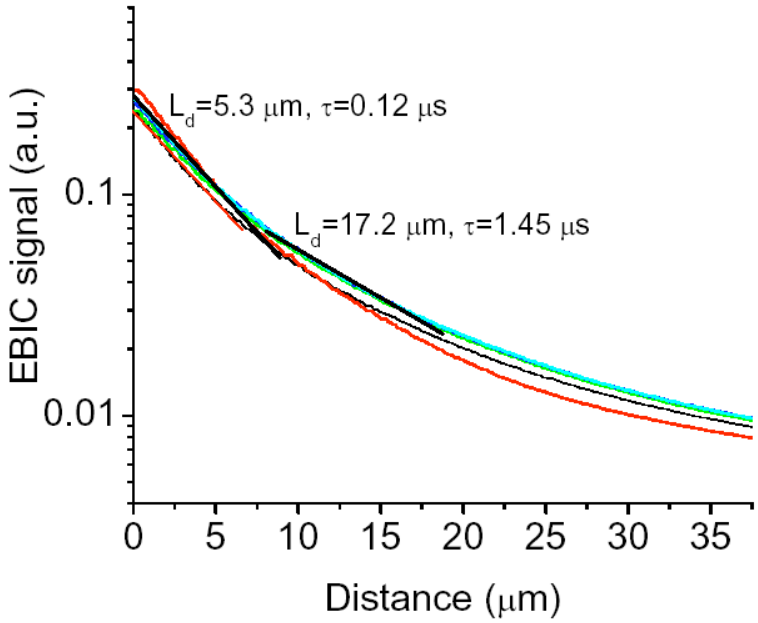


Fig. 2.43. EBIC signal as a function of distance between e-beam and Schottky contact.

Minority carrier lifetime of the epilayers is also characterized by time-resolved photoluminescence technique through collaboration with Naval Research Lab. The sample used in this study is part of wafer used for fabrication of n-channel IGBTs. The epilayer has a thickness of 182 μm and doping concentration of $1 \cdot 10^{14}$ cm^{-3} grown at C/Si ratio of 1.5. The substrate of this sample is removed by CMP to expose both Si-face and C-face before the measurement. Therefore, the minority carrier lifetime can be measured on both faces. In the time-resolved PL measurement, the sample is excited by a laser pulse with an optical injection level of around $1 \cdot 10^{14} cm^{-3}$. The collected light is then focused into a double spectrometer and detected by a photomultiplier using time-correlated photon counting. In this case, carrier lifetimes were measured at room temperature from the decay of the band edge photoluminescence peak at 391 nm. The PL decay curve is shown in Fig. 2.44 (a), which shows a complex, multi-component decay. Low-resolution time-resolved spectra shown in Fig. 2.44 (b) indicate three overlapping decay components at 391nm: 1) fast initial decay component peaking at 415nm due to shallow impurities, 2) band edge PL with roughly 1μsec decay and τ =1-2 μsec, reflecting carrier lifetime and 3) deep defect level PL peaking at larger than 500 nm with roughly 6 μsec decay and $\tau > 5$ μsec. Carrier lifetimes measured from PL decay in the 1-2 μsec range (after subtracting off the 6 μsec decay component) are 1.07μsec for the C face and 0.72 μsec for the Si face. Due to the low injection level in this measurement, the carrier lifetime is believed to be the minority carrier lifetime in the epilayer. The value of around 1 μsec is consistent with the lifetime measured by EBIC technique on the epilayers grown under similar conditions.

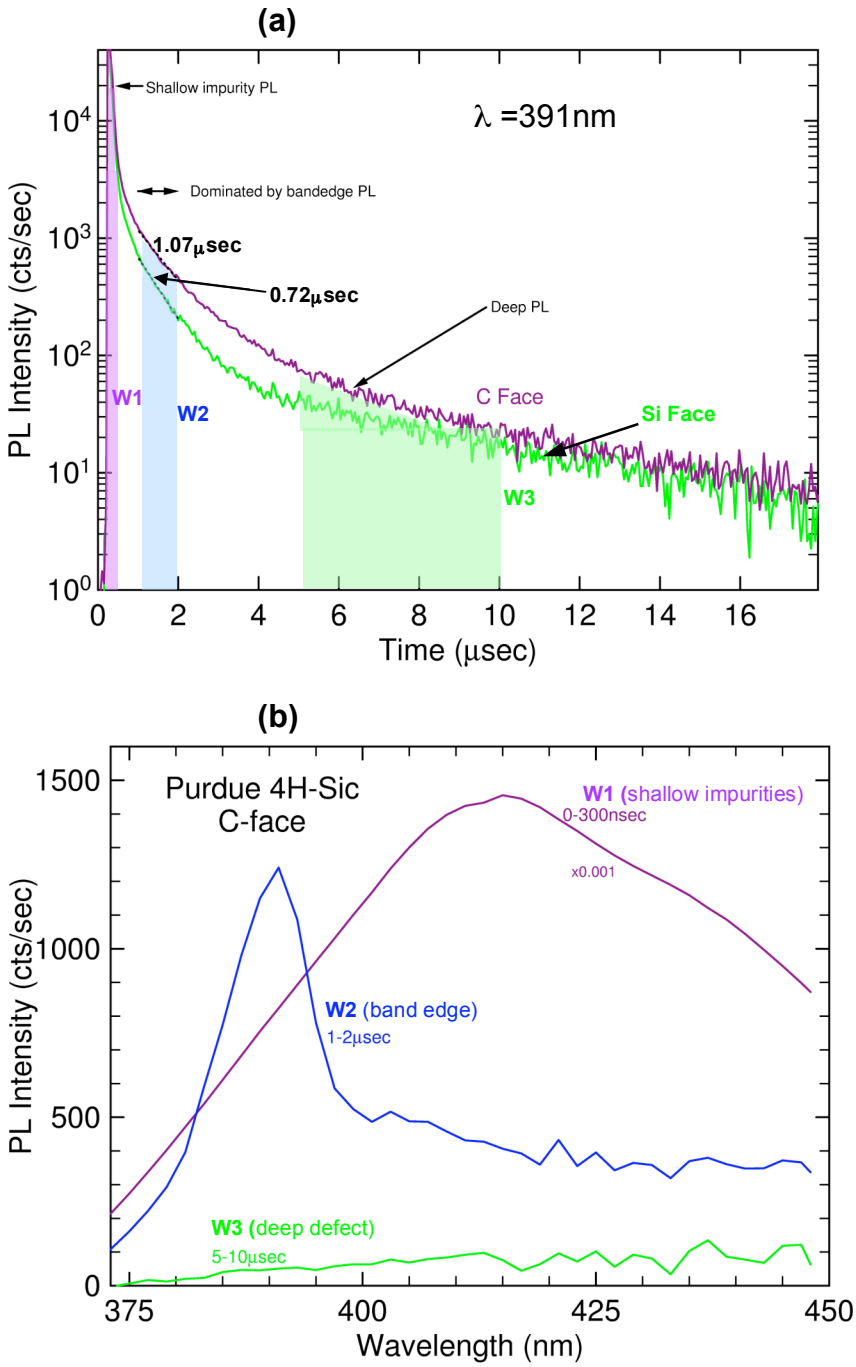


Fig. 2.44. (a) PL decay curve measurement on Si-face and C-face of a free-standing 182 μm epilayer. (b) Low-resolution time-resolved PL spectra measured on the C-face of the same sample.

Although the high minority carrier lifetime has been achieved in the epilayers grown in our lab, there is still a need to study the relationship between carrier lifetime, deep level trap densities and growth parameters. After the key parameters in determining the carrier lifetime are identified, we can consistently grow epilayers with desired carrier lifetimes. As discussed earlier, C/Si ratio is one of the most important growth parameters that impact the deep level trap densities. Therefore, effects of C/Si ratio on deep level trap densities and minority carrier lifetimes were investigated. Table 2.5 is a summary of the experimental results from four different batches of samples. Each batch of samples are grown in consecutive runs and measured at the same time. The doping concentrations of the epilayers were measured by CV technique on the Schottky contact. For the first three batches, the nitrogen flow rate was held constant at 0.073 sccm. For the forth batch, the nitrogen flow is adjusted to make the doping concentration almost constant at different C/Si ratios. The Z1/Z2 and EH6/EH7 trap densities were measured by DLTS, and carrier lifetime of the epilayers were measured using both EBIC an PL techniques.

Table 2.5 Summary of the carrier lifetime study results from four different batches of samples.

Batch #	Run #	C/Si ratio	Thickness of epilayer (μm)	Nitrogen Doping ($10^{15}cm^{-3}$)	Z1/Z2 ($10^{12}cm^{-3}$)	EH6/EH7 ($10^{12}cm^{-3}$)	EBIC Lifetime (nsec)	PL Lifetime (nsec)
First batch	619	1	~20	6.0	0.95	1.75	111	60
	629	1.2	~20	2.0	4	1.05	132	112
	617	1.5	~20	0.87	0.8	0.45	195	71
	626	1.75	~20	0.458	1.75	0.57	295	65
Second batch	695	1	~20	2.55	0	0	1420	1560
	697	1.2	~20	1.22	0.93	0	998	905
Third batch	752	1	~40	3.35	2.07	1.66	197	229
	750	2	~40	0.065	0.254	0.367	667	678
Forth batch	771	1.2	~7.5	2.5	2.5	1.74	96.4	N/A
	769	2.5	~7.5	2.0	1.79	0.86	197	N/A
	770	3	~7.5	1.9	1.68	0.78	436	N/A

Figure 2.45 (a) shows the concentration of Z1/Z2 centers as a function of C/Si ratio for the first, the third, and the forth batch of samples. For the second batch, the samples showed an anomalously low concentration of Z1/Z2 centers and therefore excluded from this comparison. As we can see from the figure, the concentrations of Z1/Z2 centers in the samples show a deceasing trend with increasing C/Si ratio except the first batch. However, the concentrations of Z1/Z2 centers from the fourth batch are an order of magnitude higher than that of the third batch with comparable C/Si ratios. This implies that the concentration of Z1/Z2 centers might be affected by other unknown factors. One thing to note is that the carrier concentrations in the forth batch are higher than the third batch. The high concentrations of Z1/Z2 centers may be a result of the higher carrier concentrations.

Fig. 2.45 (b) shows the concentrations of EH6/EH7 centers as a function of C/Si ratio for the first, third and forth batch of samples. The second batch of samples did not show an EH6/EH7 peak in DLTS spectrum. In general, the EH6/EH7 concentrations follow a similar decreasing trend with increasing C/Si ratios. Similar to the Z1/Z2 centers, the EH6/EH7 center concentrations in the forth batch seems to be higher compared with the first and third batch of samples with similar C/Si ratios. Minority carrier lifetimes measured from EBIC technique match well with those measured from PL technique in most cases. The long carrier lifetimes also correspond to the samples with low concentrations of both Z1/Z2 and EH6/EH7 centers. The longest minority carrier lifetimes and the lowest deep trap concentrations are observed in second batch of samples. However, those samples are grown at relatively lower C/Si ratios as compared with other batch of samples.

From the data above, it appears that there is large inconsistency in measured lifetimes for samples grown nominally under identical growth conditions. This suggests there are some unknown variables that control lifetimes other than C/Si ratio. Possible controlling variables not usually specified for growth include susceptor coating integrity, chamber base vacuum and doping memory effects. Future studies are needed to isolate one variable from the other in order to find out the effects of each parameter on carrier lifetimes.

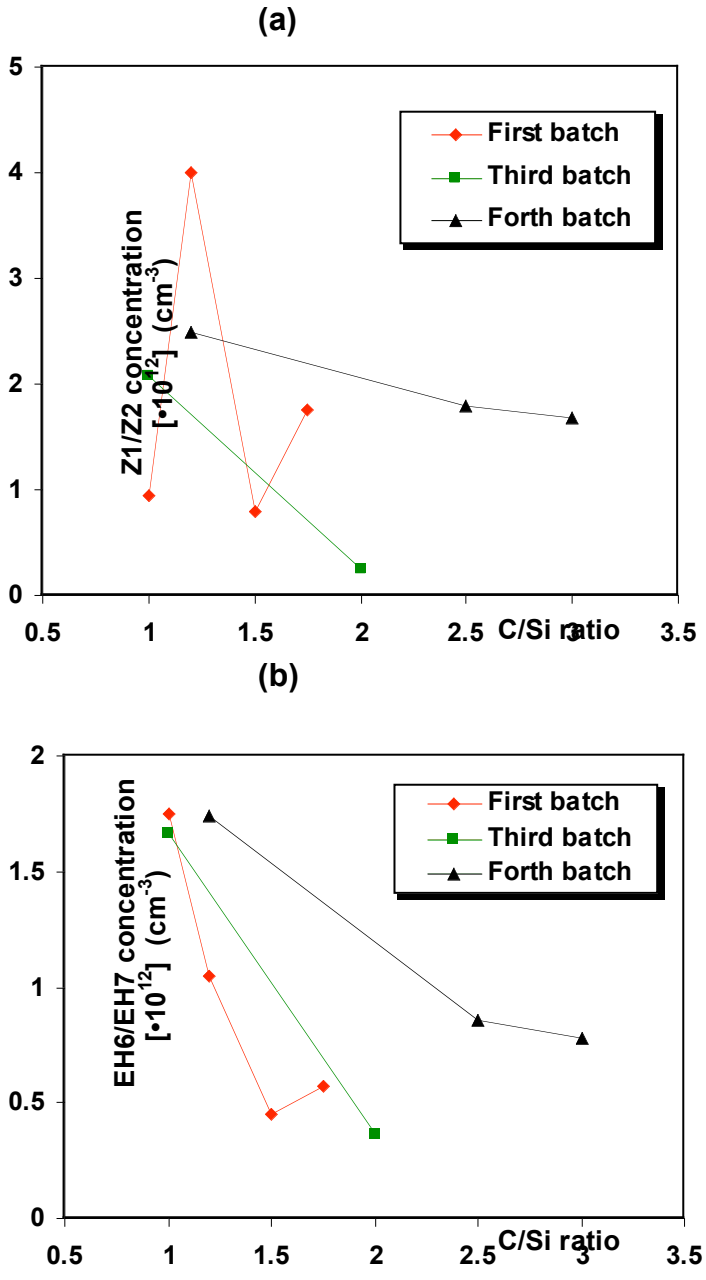


Fig. 2.45. (a) Concentrations of Z1/Z2 centers as a function of C/Si ratio for the first, the third, and the forth batch of samples; (b) concentrations of EH6/EH7 centers as a function of C/Si ratio for the first, third and forth batch of samples.

2.1.6.3.2 Carrier lifetimes in p-type epilayers

Generation lifetimes of the p-type epilayer are characterized by pulsed MOS capacitor technique as described earlier. The epilayer used in this study are aluminum doped and has a thickness of around 3 μm. After the fabrication of MOS capacitors on the epilayer, capacitance-voltage (C-V) measurement is performed to determine the aluminum doping concentration and oxide capacitance. A C-V plot of the sample at 348 ^{o}C and 320 ^{o}C is shown in Fig. 2.46. Doping concentration N_A is extracted to be around $1.5x10^{17}cm^3$ from the deep depletion region of the C-V plot. C_{ox} is extracted from the accumulation region of the C-V plot. The C-V curves do not match each other when it is biased from deep depletion to accumulation, which is believed due to the emission from interface traps. C-t plots at different temperatures are shown in Fig 2.47. Notice that light is shined on the sample at the end of the recovery, and then turned off. The excess carriers generated by light recombine, and the capacitance then gradually reduces to its equilibrium value. This step is to make sure that C_{inv} with reasonable accuracy can be obtained. The data from the C-t plots is then converted into Zerbst plots as shown in in Fig. 2.48, from which the generation lifetime τ_g can be extracted according to Eq. (3.5).

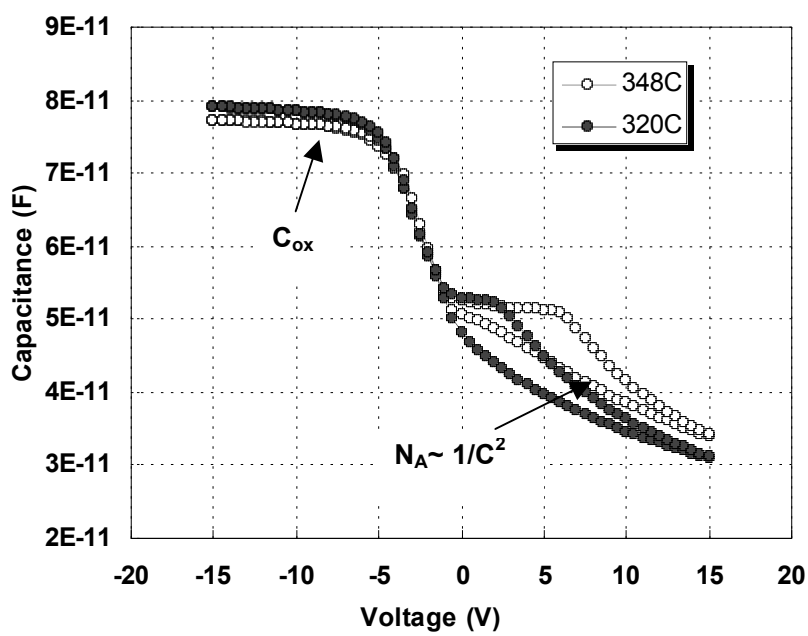


Fig. 2.46. C-V plot of the p-type sample at two different temperatures

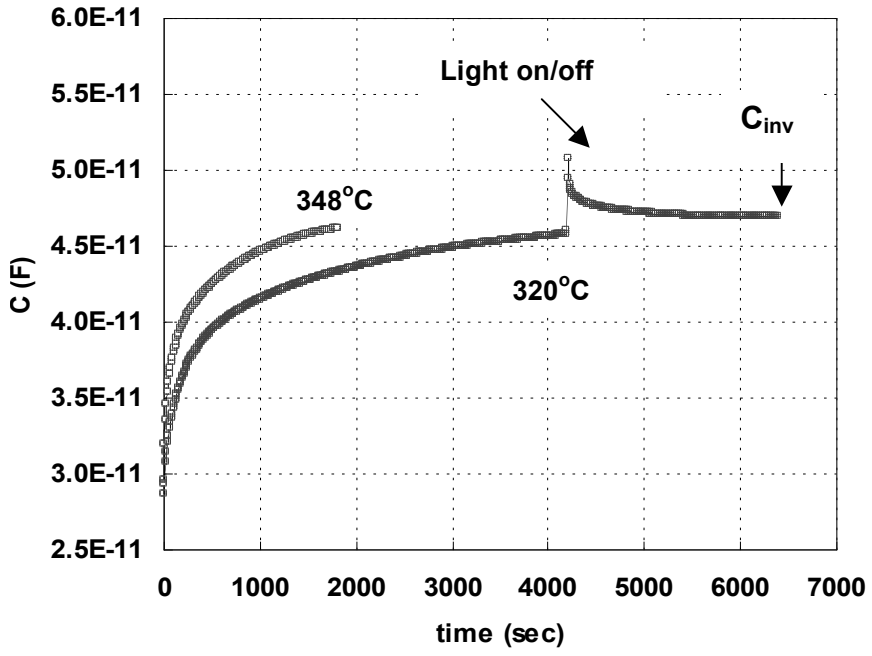


Fig. 2.47. C-t plot of the p-type sample at two different temperatures

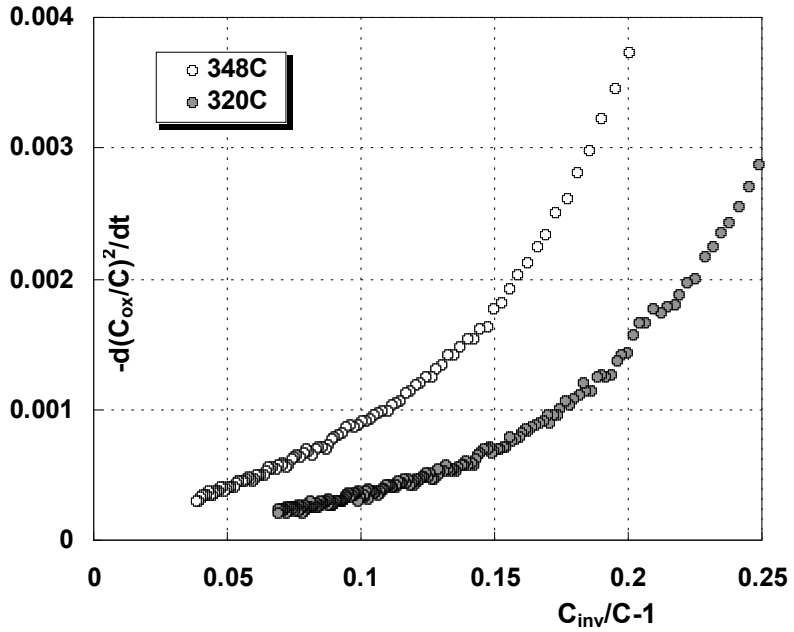


Fig. 2.48. Zerbst plot of the p-type sample at two different temperatures.

As shown in Fig. 4.28, the Zerbst plot is not a straight line in the whole range. The curved upper part is due to the field-emission from interface and/or bulk traps, which happens at the beginning of the C-t transient [72]. The generation lifetimes extracted are 38 ns for 348 ^{o}C, and 20 ns for 320 ^{o}C. The lifetime of the p-type layer is relatively short compared with that of the n-type epilayer. This may be related to the relatively higher doping of those epilayers.

2.1.6.4 Issues with Thick Epilayer Growth

Thick lightly doped 4H-SiC drift layers are needed for multikilovolt power devices. The hot-wall CVD reactor enables the growth of these layers. However, there are still outstanding issues concerning thick epilayer growth.

An epilayer with a thickness of 182 μm has been grown and relatively good morphology has been obtained. The nitrogen doping concentration is determined to be around $1 \cdot 10^{14}$ cm^{-3}. The Nomarski micrograph of the sample is shown in Fig. 2.49. The large surface defect density (including carrot, comet tail and triangular defects) is less than 10 cm^{-2}. The growth pit density is around $6 \cdot 10^{4}$ cm^{-2}, which is relatively high. However, they are considered to have small impact on device performance. From our previous thick epilayer run, the most severe problem is the particle formation. These particles are believed to be Si droplets formed during the prolonged growth process. For this sample, less than 5 particles are observed on the whole 2-inch surface.

The surface morphology of the thick epilayer is also characterized with AFM, as shown in Fig. 2.50. Surface roughness is determined to be 0.2 nm averaged from six scan areas of size 5 μm×5μm. Also, the surface is found to be uneven as indicated by the different colors on the surface in Fig. 2.50, which has been observed on most of the AFM images from this sample. The uneven surfaces are not found on the thinner epilayers used in the doping studies. Therefore, it is considered to be unique to the thick epigrowth and is apparently undesirable for device fabrications.

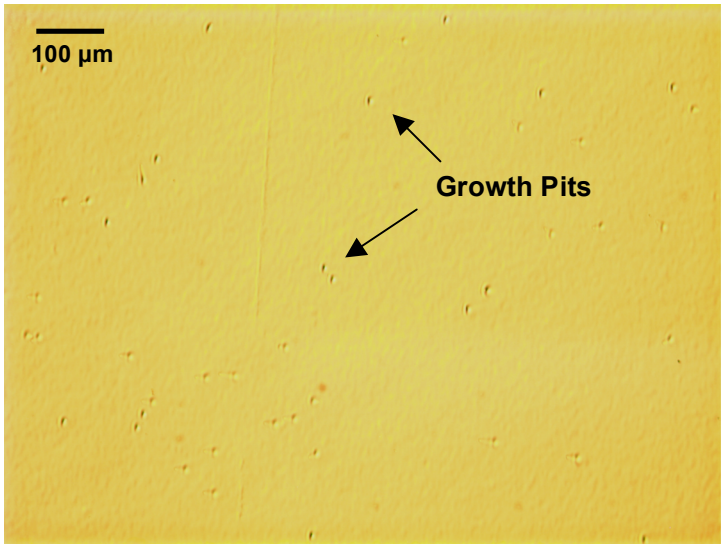


Fig. 2.49. Nomarski micrograph of the 182-µm thick epilayer with doping of $1 \cdot 10^{14}$ cm^{-3}

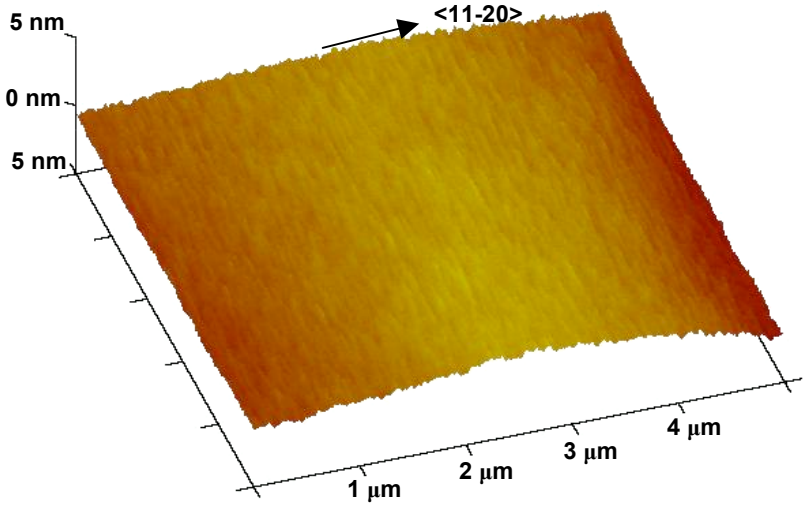


Fig. 2.50. AFM image of the 182-µm thick epilayer with doping of $1 \cdot 10^{14}$ cm^{-3}

Another issue with thick epilayer growth we have identified recently is the "growth rate creep" during the long growth run. It is found that average growth rate from the thick epigrowth run is about 1 μm slower per hour than the averaged growth rate from the short runs. For this particular run, a 17-hour-long growth is projected to give 200 μm thick epilayer, which ends up being 182 μm. This is believed due to the depletion of SiH_4 by accumulation on the susceptor walls, which becomes more severe with growth.

2.1.6.5 4H-SiC PiN Diodes

4H-SiC PiN diodes are fabricated on both 8° and 4° off-angle epilayers as described earlier. The cross-section structure of the PiN diode is shown in Fig. 2.51. No surface passivation and edge termination structures are used in those devices. For the 8° PiN diode sample, both forward and reverse I-V characteristics of the diodes will be presented, and studies on forward voltage instability will be discussed in a separated subsection. Results on reverse recovery transient analysis of the fabricated PiN diodes will also be presented. For the 4° PiN diode sample, the forward characteristics of the diodes will be discussed with an emphasis on the forward voltage drift issues.

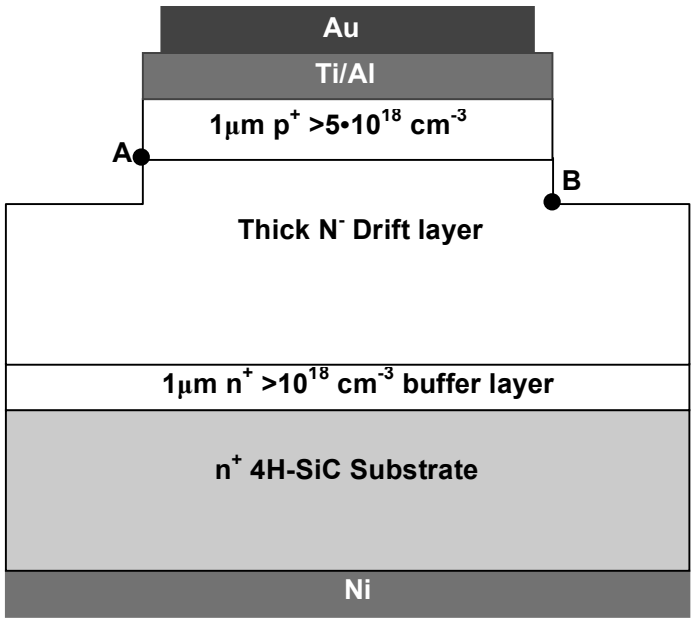


Fig. 2.51. Cross-section structure of the 4H-SiC PiN diodes.

2.1.6.5.1 4H-SiC PiN diodes on 8° off-axis epilayers

Epilayers used in this study consist of a 100-μm thick n^- drift layers with doping of $4.4 \cdot 10^{14} cm^{-3}$ and a 1-μm thick p+ anode layer with doping more than $5 \cdot 10^{18} cm^{-3}$. They are grown in separate runs in our CVD system. The PiN diodes were fabricated as described in an earlier section.

Forward I-V curves for the devices are extracted by using an HP-4156 semiconductor parameter analyzer. Figure 2.52 is the linear forward J-V characteristics of the 4H-SiC PiN diodes with different diameters, and the corresponding semi-logarithmic plot of forward J-V curves is shown in Fig. 2.53. The forward voltage drop at a current density of $100 A/cm^2$ is 4.1 V for the 100-μm diameter diode shown in Fig. 2.53. At high current region, the forward conduction is governed by a series resistance as low as 4.4 $m\Omega cm^2$ for the 100 μm-diameter diode extracted by fitting the straight portion of J-V curve. The low on-resistance indicates that the conductivity of n- layer is significantly modulated by minority carrier injections. In the low current region, ideality factors of 2 have been obtained in part of the J-V curves, as shown in Fig. 2.53. The J-V curves deviate from the recombination current slope for forward bias smaller than 2 V. The extra leakage current in the low current region is believed to come from the incomplete passivation at mesa edge, which is shown as point A in Fig. 2.51.

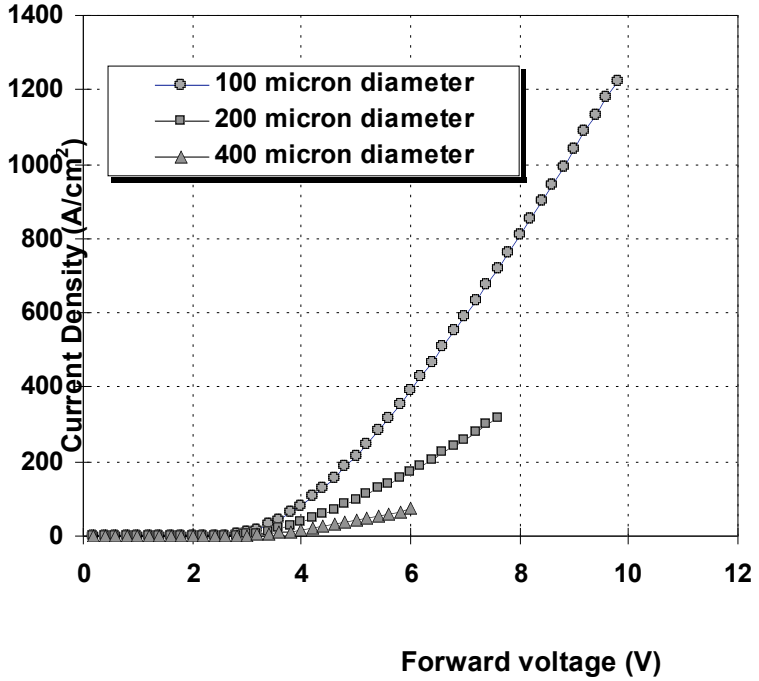


Fig. 2.52. Linear plot of forward J-V characteristics of 4H-SiC PiN diodes with different diameters fabricated on 8° off-angle epilayer.

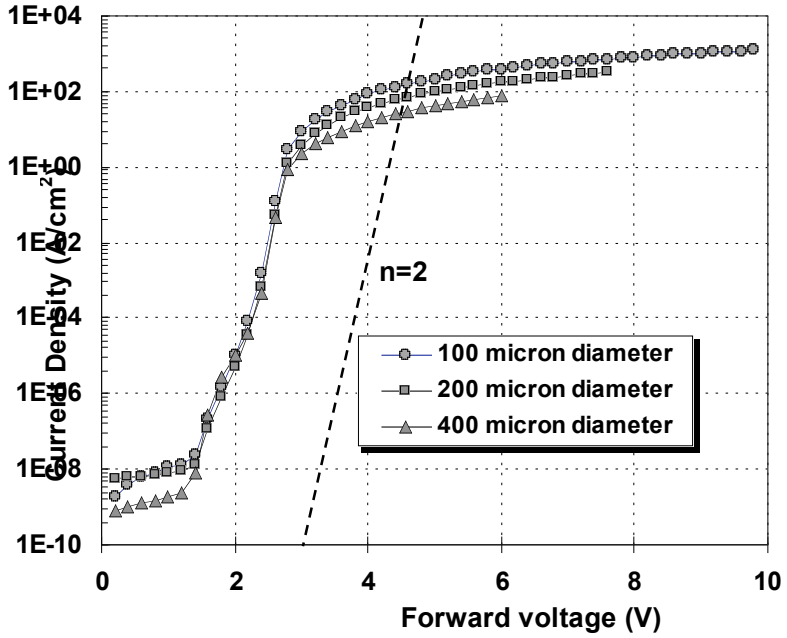


Fig. 2.53. Semi-logarithmic plot of forward J-V curves of 4H-SiC PiN diodes with different diameters fabricated on 8° off-angle epilayer. The dotted line is fitted with ideality factor of 2.0.

The on-resistance of the PiN diodes increases with increasing diode sizes as shown in Fig. 2.52, which results in an increase in forward voltage drops. The forward voltage drop (V_F) at 100 A/cm^2 is measured for diodes with different sizes on over twelve dies, and results are summarized in Fig. 2.54. The averaged forward voltage drop increases from 4.3 V for 100-µm diameter diodes to 8.3 V for 1000-µm diameter diodes, as shown in Fig. 2.54. Fujihira, et al., also reported similar results on the 6H-SiC PiN diodes with different sizes [128]. They attributed this to the anisotropy in electron mobility in 6H-SiC, which will influence the current spreading in the devices. However, this explanation cannot be applied here since the anisotropy in electron mobility for 4H-SiC is small. In our study, larger diameter diodes may include more defects in their active areas, which will reduce forward current conduction and even cause more V_F drift during measurements.

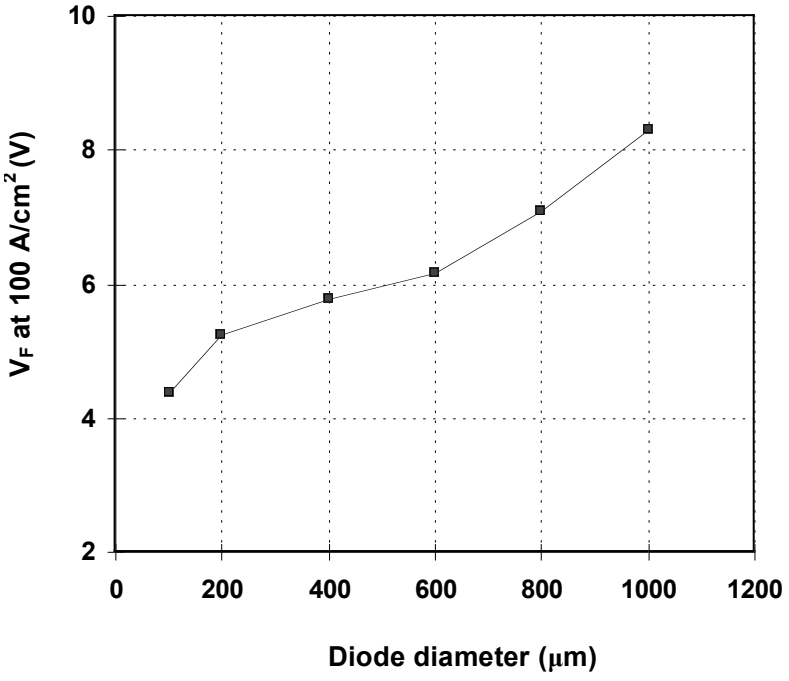


Fig. 2.54. Forward voltage drops (V_F) at 100 A/cm^2 as a function of PiN diode diameters fabricated on 8° off-angle epilayer.

Reverse I-V curves are extracted from a 10 kV measurement setup, consisting of a digital multimeter and a Bertan high-voltage source. During the measurements, the devices are immersed in Fluorient to prevent sparking in air. The reverse J-V curves of two diodes are shown in Fig. 2.55. The 400-μm diameter diode in Fig. 2.55 does not show destructive breakdown up to 4.7 kV with leakage current density as low as $2 \cdot 10^{-5}$ A/cm^{-2}. The 1000-μm diameter diode has higher leakage current and exhibits a microplasma breakdown at 2.5 kV. In general, the smaller diodes tend to achieve a higher breakdown voltage, probably due to the lower possibility of containing defects. During electrical measurements on reverse biased diodes, microplasma breakdown is observed as a sudden, step-like increase in the leakage current within a narrow bias range of a few tenths of a volt, as shown in Fig. 2.55. A large fraction of diodes including almost all larger diodes (larger than1000-μm diameter) show early microplasma breakdown. The microplasma is believed to come from the localized breakdown, which creates confined electron-hole plasma short-circuiting the depletion region. Zimmermann, et al., have studied the microplasma breakdown in 4H-SiC diodes, and found that the appearance of microplasma spots are related to extended crystal defects, mainly closed-core screw dislocations and micropipes [129]. Therefore, the occurrences of microplasma breakdown in current study indicate a high screw dislocation or micropipe densities. For smaller diodes, the highest breakdown voltage achieved is about 4.9 kV, which is about 40% of the theoretical value. This low breakdown voltage may be attributed to the lack of proper junction termination, resulting in the electrical field crowding at the corners of the mesa structure (point B in Fig. 2.51). In order to achieve high breakdown voltage, edge termination techniques such as junction extension termination (JTE) are needed.

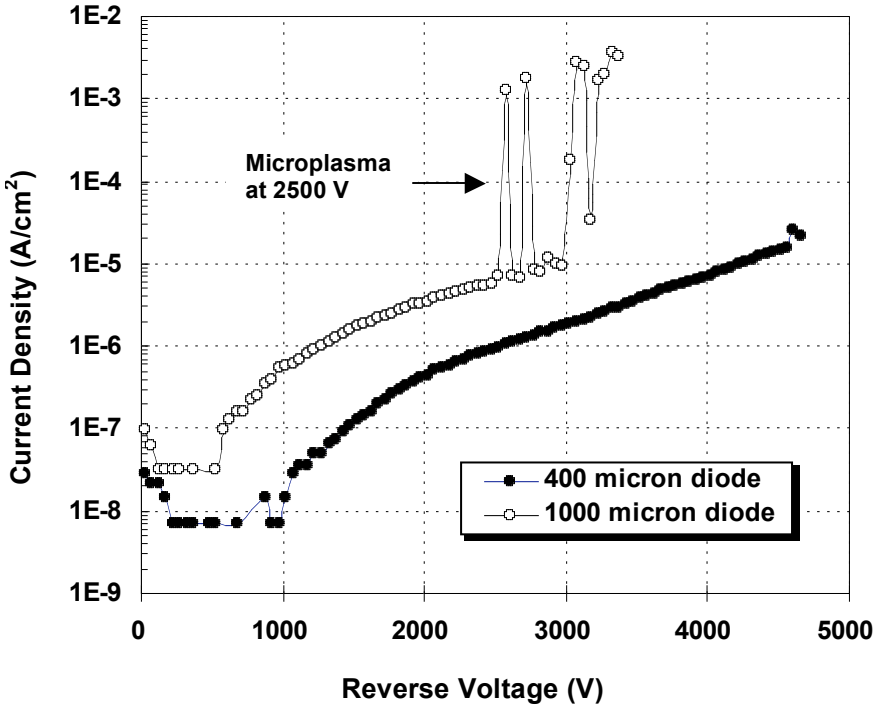


Fig. 2.55. Reverse current J-V characteristics of 4H-SiC PiN diodes with different diameters fabricated on 8° off-angle epilayer.

Forward voltage instability is characterized on the fabricated 4H-SiC diodes with both electrical stressing and light emission microscopy technique. In the electrical stressing test, the diodes are stressed with constant current density (100A/cm^2), and the forward voltage drop over the diodes is monitored using the HP-4156 semiconductor parameter analyzer. Figure 2.56 is the forward J-V curves for the same 100-μm diameter diode measured before and after 34 hours of stressing at constant current density of 100 A/cm^2. The on-resistance of the diode increases from 3.5 mΩcm^2 to 10.7 mΩcm^2, and V_F at 100 A/cm^2 increases from 4.1 V to 5.8 V. The forward voltage drift as a function of time for two diodes is shown in Fig. 2.57. For both diodes, V_F increases rapidly at the beginning of the stressing, stabilizes over a period of less than 2 hours, and remains almost constant throughout the rest of the test.

The phenomenon of forward degradation in SiC bipolar devices has been reported and studied for several years. It is well accepted that V_F drift is caused by the formation of single-layer Shockley-type stacking faults (SFs) in the basal plane of the drift layer [130]. The nucleation sources of SFs are believed to be pre-existing basal plane dislocations in SiC epilayers [131]. During forward conduction, stacking faults expand

and form regions with low minority carrier lifetime, which degrades the current-handling capability and increase the on-state resistance of the devices [130]. The stability of V_F after a period of stressing in this study is believed due to the pinning of SFs at bulk defects or interfaces, which leaves the areas with SFs unchanged in the device.

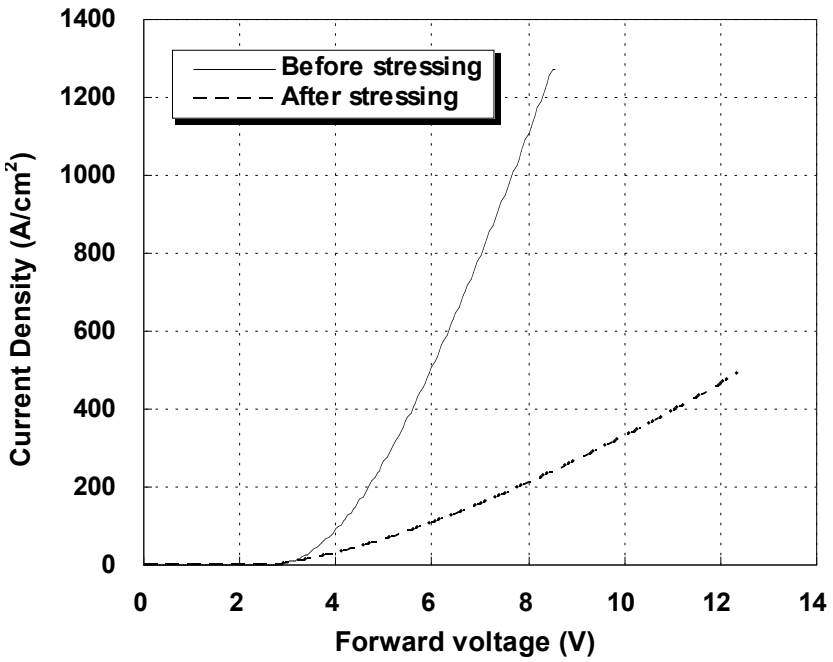


Fig. 2.56. Forward J-V curves for a 100-µm diode measured before and after electrical stressing.

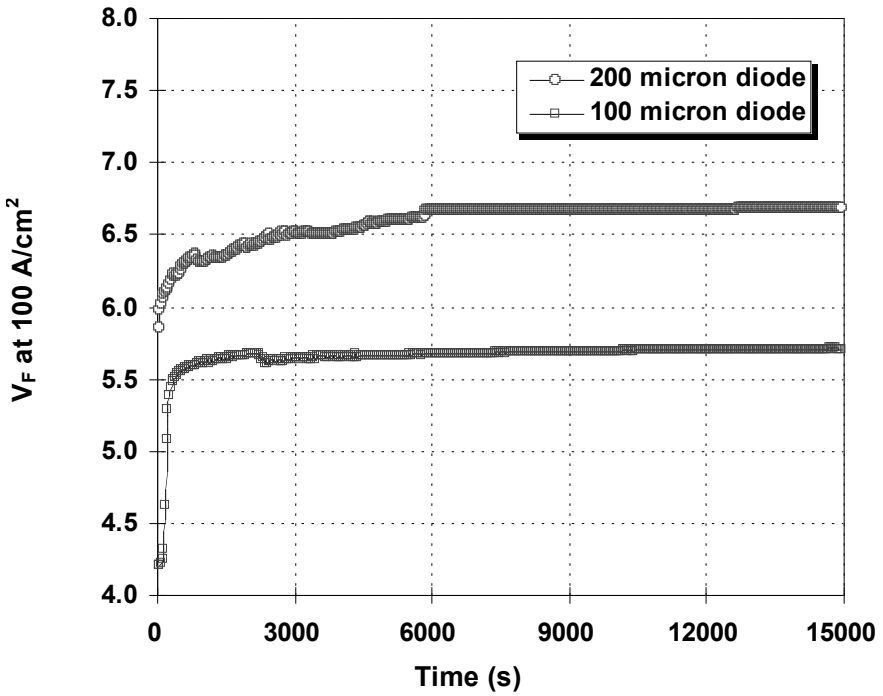


Fig. 2.57. Forward voltage drop at as a function of stressing time during forward electrical stressing of 34 hours at current density of 100 A/cm^2 (only portion of curves is shown in the figure).

The forward stability is also tested on large size devices. Since most of the forward voltage drift happens during the first two hour of stressing, the PiN diodes with active area of 0.5 mm^2 (800-µm diameter) has been stressed at 100 A/cm^2 for over 2 hour. Forward voltage drops are measured before and after the stressing, and results are shown Fig. 2.58. The blue bars correspond to the initial forward voltage drops before the stressing test, and the orange bars correspond to the amount of drift happened after 2 hour of stressing. The averaged V_F drifts over ten diodes is about 4 V. The largest drift measured is about 12 V, which is about two times of the original forward voltage drop.

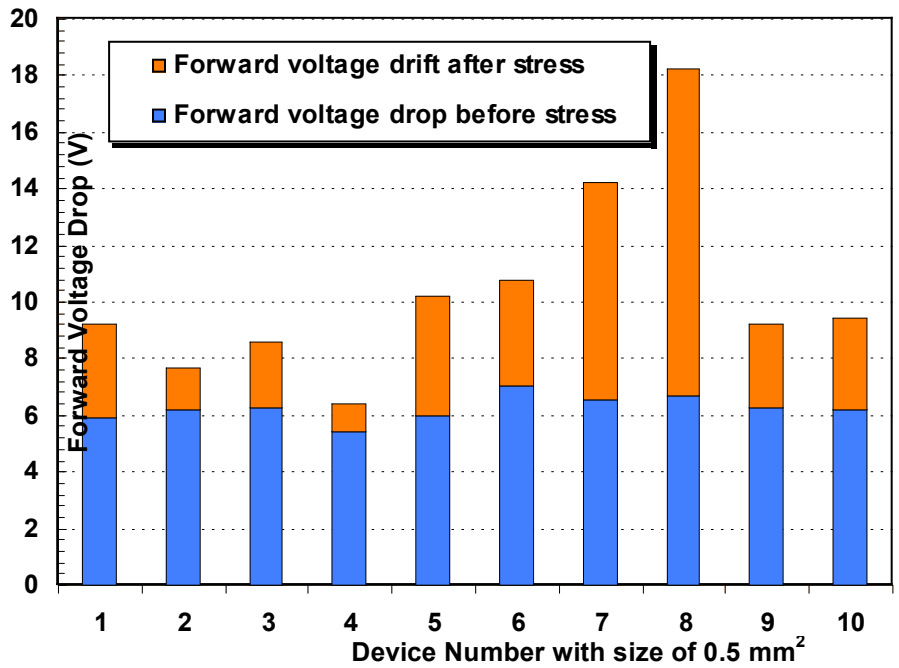


Fig. 2.58. Forward voltage drops measured before and after 2 hour of stressing on large size 4H-SiC PiN diodes fabricated on 8° off-angle epilayer.

To track stacking fault growth, in-situ light emission microscopy (LEM) is used to monitor the device degradation. PiN diodes with wide open anode contact area are built as described earlier, and LEM experiments are done at Naval Research Laboratory (NRL) in collaboration with Dr. Robert Stahlbush. The light-emission images are collected with a sensitive charge-couple device (CCD) mounted to a microscope in a probe station. The CCD is cooled to -100 ^{o}C, which strongly suppresses dark current and makes it possible to collect images at low-light level [132]. During the measurement, a series of high-current level stressing is performed, and low-current images are collected during each stressing interval. Figure 2.59 is the light-emission images from a series of current stressing. After low current level stressing at 1 mA for 2 second, there are no stacking faults observed in the active device region, as shown in Fig. 2.59(a). The horizontal bright lines in the upper part of the images are believed not to be SFs because they remain stable throughout the stressing test. With increasing stressing current, well-defined bright-line emission can be observed, and they are distributed over the sample at the end of the stressing, as shown in Fig. 2.59 (d). Those sharp bright lines correspond to the partial dislocations which bound the areas with SFs. Planar structures of rectangular, rhombic, and triangular stacking faults are reported, and their origins and movements

have been studied [130, 133]. One example of rhombic-shaped stacking faults has been identified in Fig. 2.59(d), which is shown in circle A.

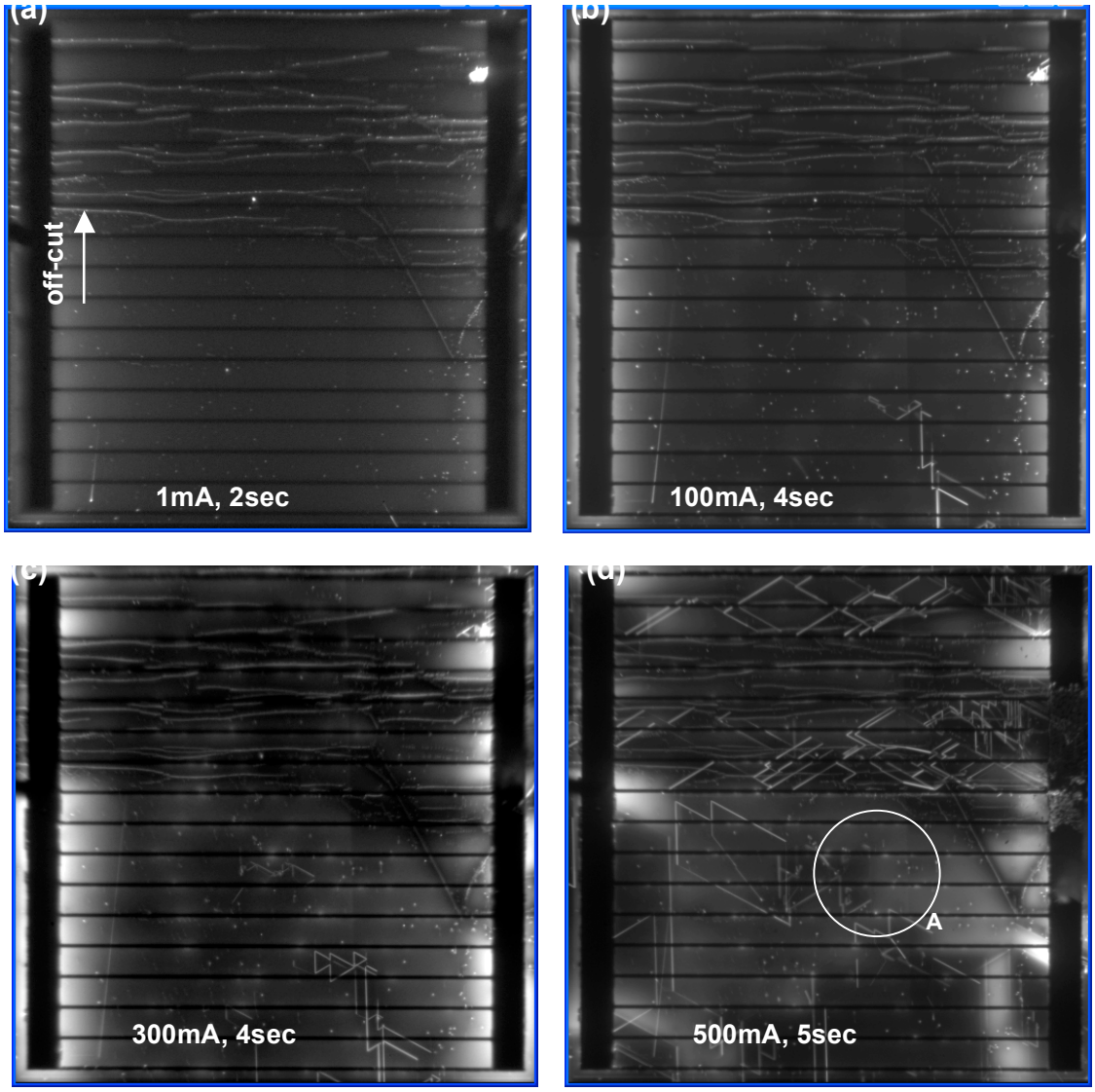


Fig. 2.59 Light-emission microscopy images of 4H-SiC PiN diodes fabricated on 8° off-angle epilayer under a series of forward current stressing.

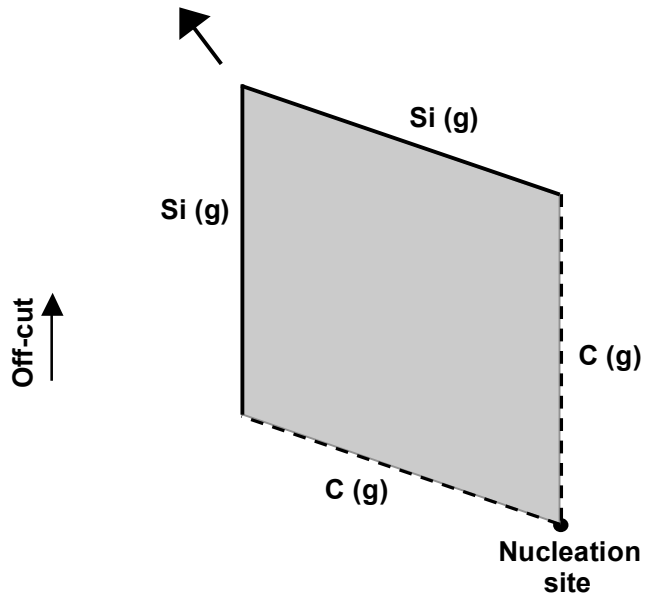


Fig. 2.60 Schematic diagram of the rhombic stacking fault development.

Schematic diagram of the rhombic stacking faults development during the forward degradation is shown in Fig. 2.60. It has been shown that the bounding partial dislocations have Burgers vector of the 1/3<1-100> type and their lines are aligned along <11-20> directions. Four partial dislocation segments that surround the stacking fault area can be divided into two types, referring to silicon-core Si(g) and carbon-core C(g) partial dislocations, respectively. The letter "g" denotes a glide-set dislocation, which can form a Shockley-type stacking fault by glide. The Si (g) partial dislocations are believed to be mobile and are brightly luminescent in LEM images, while the C (g) partial dislocations are immobile and invisible under LEM. The activation energy for the partial dislocation glide is believed to come from the recombination in the electron-hole plasma under forward conduction. As the mobile partial dislocations move, the areas with SFs expand and forward conduction of the devices degrades.

Reverse recovery transient analysis is performed on the fabricated 4H-SiC PiN diodes in a fast-risetime pulse-test circuit as described earlier. During the measurement, the diode under test is initially forward biased, and then switched into reverse bias by a single pulse. Effective carrier lifetimes of the drift layer are extracted from the current recovery waveform. Figure 2.61 is the reverse recovery current transient recorded on a 1000-μm diameter diode, which is switched from forward current of 0.3 A by a reverse pulse with voltage amplitude of 150 V. The reverse recovery time t_{rr} is approximately

80ns, and the peak reverse current is about 90% of the forward current. For comparison, an idealized current response of Si p^+n diode is also shown in the inset. Circuit parasitics (such as stray inductance, transmission-line delay and reflection, etc.) are believed responsible for some non-idealities in the recovery current waveform, such as several nanosecond risetime and slightly non-constant I_R during the storage state [71]. However, a relatively constant current storage phase can still be distinguished from a strong decaying recovery phase portion. The extracted storage time t_s is then used to calculate effective carrier lifetime τ_p by using Eq. (3.6). The effective carrier lifetime extracted from the waveform in Fig. 2.61 is about 210 ns, which is considerably lower than the lifetime measured from EBIC and PL techniques.

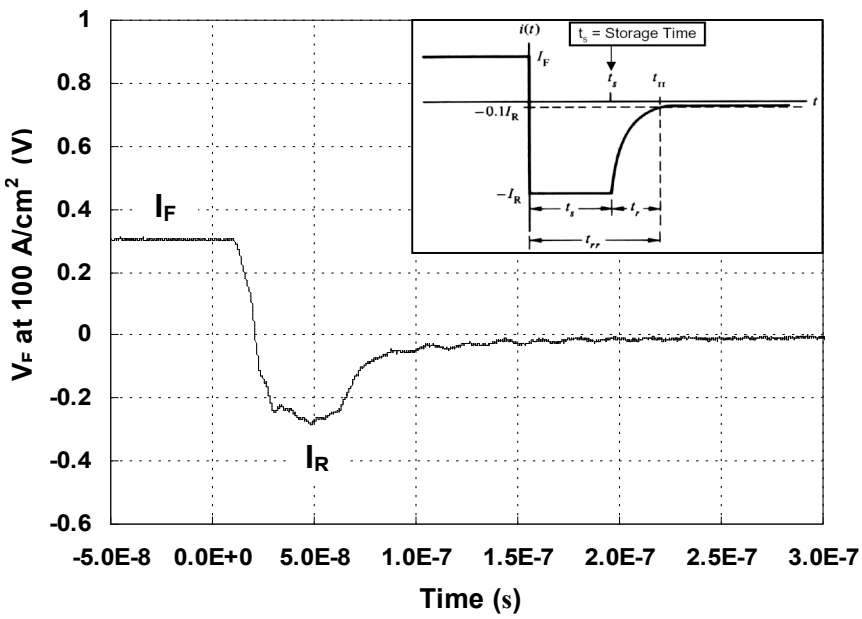


Fig. 2.61 Reverse recovery current transient recorded on a 1000-μm diameter diode. Inset is idealized reverse recovery current waveform of Si p^+n diodes.

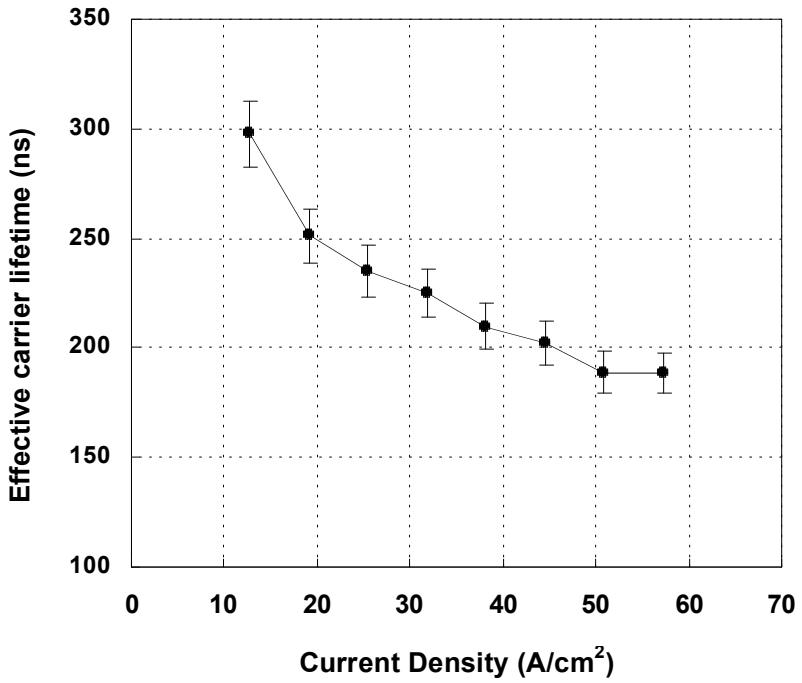


Fig. 2.62 The effective minority carrier lifetimes as a function of forward current densities as extracted from reverse recovery current waveform. About 5% errors are introduced by taking the mean value for the non-constant I_R in the charge storage region.

In order to study the current level dependence of the effective carrier lifetime, forward currents of the diodes were varied from 12A/cm^2 to 57 A/cm^2 before the turn-off transient. The effective carrier lifetimes are plotted as a function of current density in Fig. 2.62. An error of about 5% was introduced by taking the mean value for the non-constant I_R in the charge storage region. It is shown that the effective carrier lifetimes decrease with increasing current densities in the measured range. Since different forward current densities imply different injection levels, the observed trend indicates that the effective carrier lifetimes decrease with increasing injection level. It was reported that effective carrier lifetimes of 6H-SiC PiN diodes decrease with injection levels at very high current densities (>100 A/cm^2) due to the effect of bulk Auger recombination [86]. However, Auger recombination is not believed to be responsible for the decrease in the carrier lifetime here due to the relatively low current densities in this study. Samples used in this work were also subjected to measurement of the bulk carrier lifetime by optical techniques where lifetimes were determined to be in the range of 1.0-2.0 μs, which is much longer than the effective carrier lifetime shown in Fig. 2.62. Therefore, other

components instead of bulk recombination must be dominating the effective carrier lifetimes in this case.

Neudeck reported that perimeter recombination may be responsible for poor effective minority carrier lifetime in 4H-SiC p^+n diodes [71]. A study by Grivickas, et al., also indicated that a large recombination rate on the surface and at the n^-/n^+ interface of 4H-SiC epilayers is the limiting factor for the measured carrier lifetime under high-level injection conditions [134]. Including surface and interface effects, measured effective carrier lifetimes τ_{eff} can be expressed in terms of the bulk minority carrier lifetime τ_b and average recombination velocity S that accounts for recombination at the surface and n^-/n^+ interface [135]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \left(\frac{d}{2S} + \frac{d^2}{D\pi^2} \right)^{-1} \qquad (2)$$

where D is the ambipolar diffusion coefficient and d is the sample thickness. Equation (2) indicates that the effective carrier lifetime will decrease with increasing effective recombination velocity.

In order to understand the excessive carrier distribution inside the diodes, a 2D device simulation was carried out to study the electron and hole concentration in the forward biased 4H-SiC PiN diode. The electron and hole concentrations are plotted as a function of distance from p^+ emitter layer for the drift region, as shown in Fig. 2.63. It is clear that a high level injection condition exists in most of the drift region at a current density of 12 A/cm^2, and through the entire drift layer at a current density of 57 A/cm^2. The excessive carrier concentrations are the highest at p^+/n^- and n^-/n^+ interfaces. The high carrier concentration at the p^+/n^- interface will facilitate the perimeter surface recombination at the diode mesa sidewall and trench bottom, where the recombination velocity is believed to be high due to the un-passivated surface after the RIE [136]. The high carrier concentration at the n^-/n^+ interface will promote recombination at the epilayer and substrate interface, where a high recombination velocity is also expected due to high defect densities. Furthermore, the surface and interface recombination velocities are found to be injection-dependent, showing increasing trend with higher injection levels [134]. This could be responsible for the decrease in the effective carrier lifetime with increasing current levels observed in this study. Therefore, the experimental results in this study can be understood by considering the effect of the surface and interface recombination in the 4H-SiC PiN diodes.

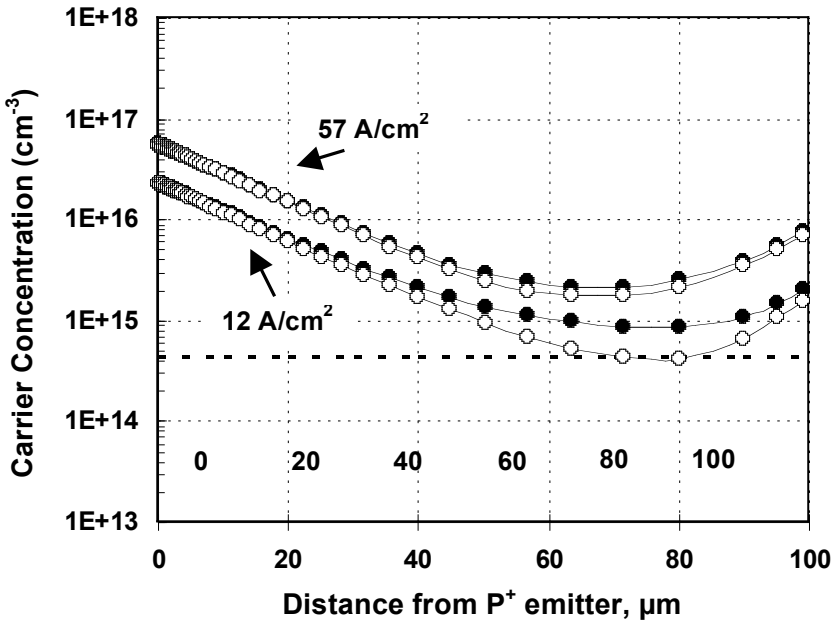


Fig. 2.63 Electron (●) and hole (○) concentrations in the drift region of a simulated 4H-SiC PiN diode forward biased at current densities of 12A/cm^2 and 57A/cm^2. The drift region doping is 4.4x10^{14} cm^{-3} as marked by the dotted line

2.1.6.5.2 4H-SiC PiN diodes on 4° off-angle epilayers

4H-SiC PiN diodes are built on 50 µm thick epilayer with doping of $6.0 \bullet 10^{14}$ cm^{-3} grown on 4° off-axis Si-face 4H-SiC substrate. Figure 2.64 is the linear forward J-V characteristics of the 4H-SiC PiN diodes with different diameters. The forward voltage drop at a current density of 100A/cm^2 is 3.3 V for the 100-µm diameter diode shown in Fig. 2.64. At high current region, the forward conduction is governed by a series resistance as low as 1.8 mΩcm^2 for the 100 µm-diameter diode extracted by fitting the straight portion of linear J-V curve. The low on-resistance indicates that the conductivity of n- layer is significantly modulated by minority carrier injections. In the low current region, ideality factors of 1.7 have been obtained in part of the semi-logarithmic J-V curves, as shown in Fig. 2.65.

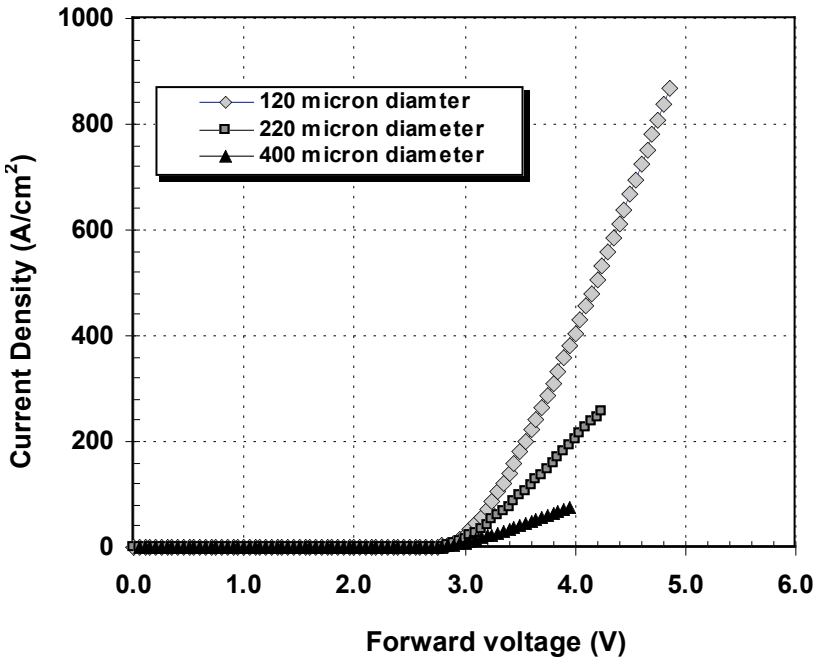


Fig. 2.64. Linear plot of forward J-V characteristics of 4H-SiC PiN diodes with different diameters fabricated on 4° off-angle epilayer.

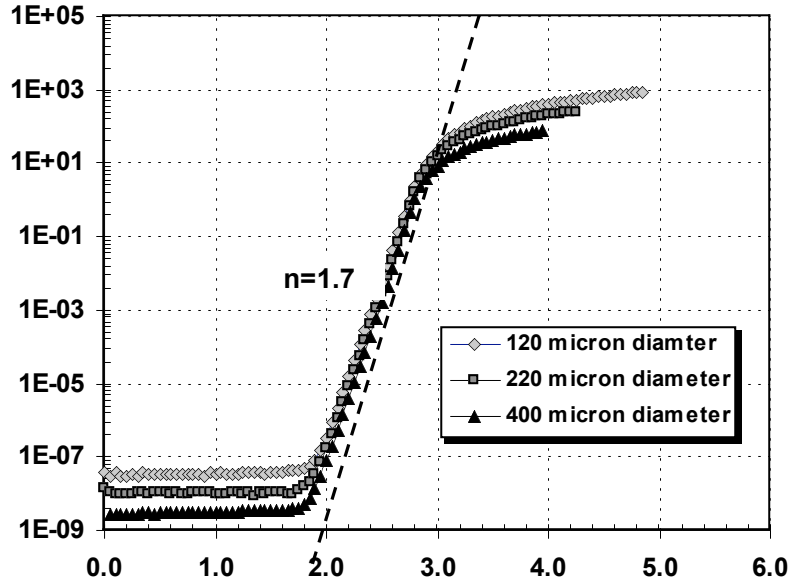


Fig. 2.65. Semi-logarithmic plot of forward J-V curves of 4H-SiC PiN diodes with different diameters fabricated on 4° off-angle epilayer. The dotted line is fitted with ideality factor of 1.7.

Figure 2.66 shows the forward voltage drop as a function of time for 200 μm-diameter device under the stress of 100 A/cm^2 for 22 hour. The forward voltage drop decreases slowly with time in the first 5 hour, and remain constant for the rest of the test.

The decrease in V_F within the first five hours is believed to be related to a slight decrease in the contact resistance as the sample temperature increases during testing. The forward J-V curves of the PiN diodes before and after the stress are shown in Fig. 2.67. The device has been tested immediately after the stress test and after 20 min cooling. It can be seen that the forward voltage drop decreases when the device is tested immediately after the stress, and increases after 20 min cooling. The V_F drift for the device is around 50 mV after 22 hours of stressing. The stable forward operation of 4H-SiC PiN diodes built on 4° off-axis is the result of low basal plane dislocation density as discussed in an earlier section.

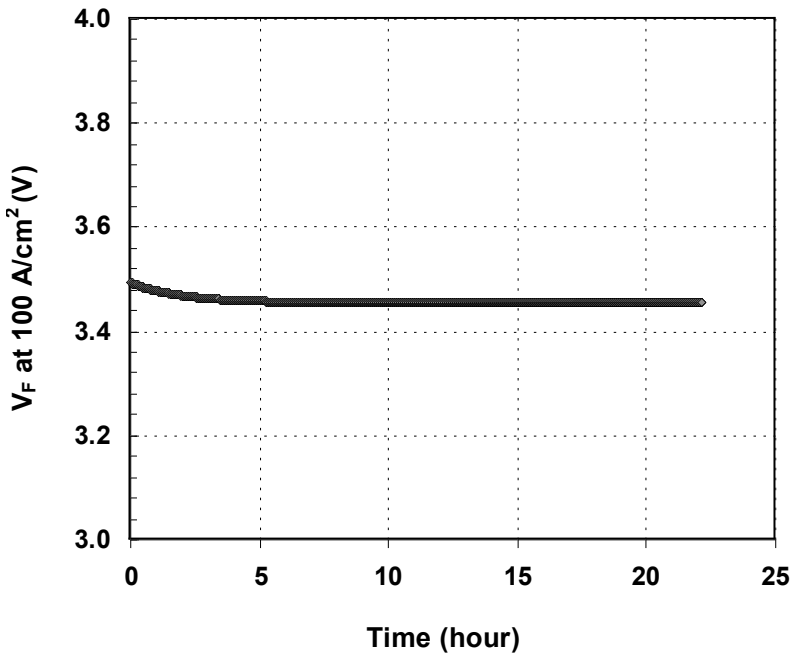


Fig. 2.66 Forward voltage drop at as a function of stressing time during forward electrical stressing of 22 hours at current density of 100 A/cm^2 on 4H-SiC PiN diodes fabricated on 4° off-angle epilayer.

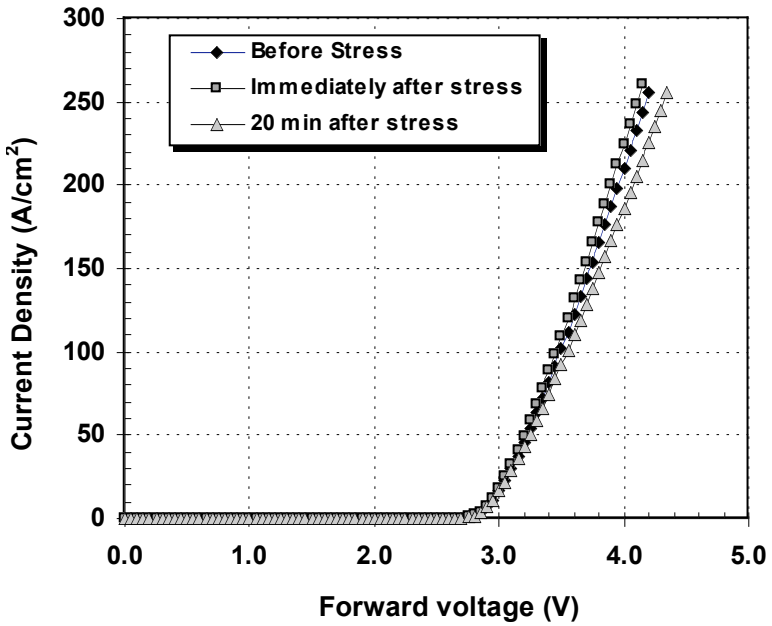


Fig. 2.67 Forward J-V curves measured before electrical stressing, immediately after stressing and after 20 min of cooling on a 4H-SiC PiN diode fabricated on 4° off-angle epilayer.

The forward stability is also tested on large size devices. As shown in Fig. 2.57, most of the forward voltage drift happened during the first two hours of stressing. Therefore, the PiN diodes with active area of 0.5 mm^2 (800 μm diameter) has been stressed at 100 A/cm^2 for over 2 hour, and left cooled for 20 minutes. Forward voltage drops are measured before and after the stressing, and results are shown Fig. 2.68. The blue bars correspond to the initial forward voltage drops before the stressing test, and the orange bars correspond to the amount of drift happened after 2 hour of stressing. Out of 10 devices tested across the test wafer, only one device has a forward voltage drift larger than 100 mV. If we define a device with forward voltage drift less than 100 mV as good device, the forward voltage drift yield for this sample will be around 90%.

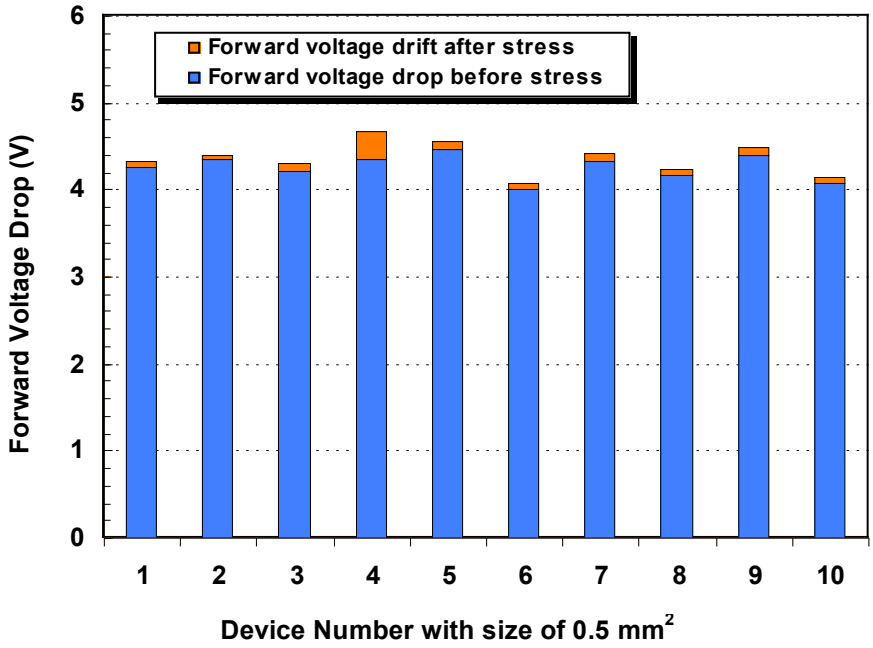


Fig. 2.68. Forward voltage drops measured before and after 2 hour of stressing on large size 4H-SiC PiN diodes fabricated on 4° off-angle epilayer.

In summary, 4H-SiC PiN diodes built on 8° off-angle substrates show good forward and reverse performance. However, the forward voltage drift is very severe due to the relatively high BPD density in those epilayers. On the other hand, 4H-SiC PiN diodes fabricated on 4° off-angle substrates show very good forward characteristics and minimal forward voltage drift due to the low BPD density. Therefore, epitaxial growth on low off-angle substrate is a very promising solution to forward degradation problem in SiC bipolar devices.

2.1.7 Summary of Task 2 Activities at Purdue University

The following results have been achieved:

1. Epitaxial growth on 4H-SiC (0001) Si-face substrates with 4° and 8° off-angles by hot-wall CVD is investigated. Epilayers grown on 8° substrates exhibit slightly larger growth rates and higher nitrogen doping concentrations compared with those on 4° substrates. Smooth surfaces have been obtained on 8° samples at various C/Si ratios, while surfaces with macrosteps are found on 4° samples. Step bunching behavior is found to be dependant on C/Si ratio for both substrate orientations. An epilayer as thick as 182 μm with low surface defect densities and n-type doping of $1 \cdot 10^{14}$ cm^{-3} has been grown on 8° substrate in this work for n-channel IGBT device fabrication at Purdue.

2. Basal plane dislocation densities are greatly reduced on 4° substrates grown under proper growth conditions. The BPD conversion is found to be dependent on C/Si ratio. The lowest BPD density is 2.6 cm^{-2} on 4° samples at C/Si ratio of 2.0. This study shows that growth on low off-angle substrates provides a possible route to obtain thick, low-doped SiC epilayers with low BPD densities for bipolar device applications.

3. 4H-SiC epilayers are grown on 4° off-axis $(000\bar{1})$ C-face substrates under various growth conditions. Surface morphology of the epilayers shows a strong dependence on C/Si ratio, N_2 flow and growth temperature. Surface defect densities are higher for samples grown under high C/Si ratio and high N_2 flow condition. Triangular-shaped defect density decreases and the shallow growth pit density increases with increasing growth temperature. Lightly doped C-face epilayers with low defect densities have been achieved by growing under optimized conditions.

4. AFM analysis indicates that macrostep bunching happens on the samples grown under high N_2 flow condition on 4° off-axis $(000\bar{1})$ C-face substrates. Step bunching anisotropy is also observed under high C/Si ratio. The degree of step bunching shows dependence on the N_2 flow settings. Macrostep bunching can be

greatly suppressed on heavily doped samples by proper selection of N_2 flow conditions. Different doping characteristics have been observed for samples grown under different N_2 flow conditions. Under low N_2 flow conditions, doping concentrations on C-face epilayers decrease with increasing C/Si ratio, exhibiting the site-competition effect. However, similar effect has not been observed on the heavily doped epilayers.

5. Minority carrier lifetimes of epilayers grown on Si-face 4H-SiC substrates are characterized using EBIC and time-resolved PL techniques. Minority carrier lifetimes between 1~2 μsec have been achieved. The correlation between deep level trap densities and C/Si ratios has been established. It is found that both Z1/Z2 and EH6/EH7 trap densities decrease with increasing C/Si ratios under most growth conditions.

6. High-voltage 4H-SiC PiN diodes are fabricated on both 8° and 4° off-axis epilayers. Forward, reverse, and reverse recovery characteristics of the devices are investigated. The forward voltage degradation is studied using electrical stressing and light emission microscopy techniques. 4H-SiC PiN diodes fabricated 8° epilayers show an averaged forward voltage drift of 4 V after 2 hour stressing. However, 4H-SiC PiN diodes fabricated 4° epilayers exhibit very stable forward operation with minimal forward voltage drift (less than 100 mV) after electrical stressing. This is attributed to the low BPD densities on those epilayers.

BIBLIOGRAPHY FOR SECTION 2.1

[1] A. R. Powell and L. B. Rowland, "SiC materials - Progress, status, and potential roadblocks," *Proceedings of the IEEE*, vol. 90, pp. 942-955, 2002.

[2] J. J. Sumakeris, J. R. Jenny, and A. R. Powell, "Bulk crystal growth, epitaxy, and defect reduction in silicon carbide materials for microwave and power devices," *MRS Bulletin*, vol. 30, pp. 280-286, 2005.

[3] S. G. Muller, J. J. Sumakeris, M. F. Brady, R. C. Glass, H. M. Hobgood, J. R. Jenny, R. Leonard, D. P. Malta, M. J. Paisley, A. R. Powell, V. F. Tsvetkov, S. T. Allen, M. K. Das, J. W. Palmour, and C. H. Carter, "Defects in SiC substrates and epitaxial layers affecting semiconductor device performance," *European Physical Journal-Applied Physics*, vol. 27, pp. 29-35, 2004.

[4] H. Matsunami, "Technological breakthroughs in growth control of silicon carbide for high power electronic devices," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers*, vol. 43, pp. 6835-6847, 2004.

[5] M. G. Spencer, J. Palmour, and C. Carter, "Substrate and epitaxial issues for SiC power devices," *IEEE Transactions on Electron Devices*, vol. 49, pp. 940-945, 2002.

[6] H. Matsunami and T. Kimoto, "Step-controlled epitaxial growth of SiC: high quality homoepitaxy," *Materials Science & Engineering R-Reports*, vol. 20, pp. 125-166, 1997.

[7] S. E. Saddow and A. Agarwal, *Advances in silicon carbide processing and applications*. Boston: Artech House, 2004.

[8] K. Kojima, H. Okumura, S. Kuroda, D. Arai, A. Ohi, and H. Akinaga, "2-inch 4H-SIC homoepitaxial layer grown on on-axis C-face substrate by CVD method," *Silicon Carbide and Related Materials 2004*, vol. 483, pp. 93-96, 2005.

[9] S. Nakamura, T. Kimoto, and H. Matsunami, "Surface mechanisms in homoepitaxial growth on alpha-SiC {0001}-vicinal faces," *Silicon Carbide and Related Materials 2003, Pts 1 and 2*, vol. 457-460, pp. 163-168, 2004.

[10] A. Tsuchida, T. Miyanagi, I. Kamata, T. Nakamura, K. Izumi, K. Nakayama, R. Ishii, K. Asano, and Y. Sugawara, "Investigation of basal plane dislocations in the 4H-SiC epilayers grown on {0001} substrates," *Silicon Carbide and Related Materials 2004*, vol. 483, pp. 97-100, 2005.

[11] J. A. Powell, D. J. Larkin, P. B. Abel, L. Zhou, and P. Pirouz, "Effect of tilt angle on the morphology of SiC epitaxial films grown on vicinal (0001)SiC substrates," *Silicon Carbide and Related Materials 1995*, vol. 142, pp. 77-80, 1996.

[12] H. Saitoh and T. Kimoto, "4H-SiC epitaxial growth on SiC substrates with various off-angles," *Silicon Carbide and Related Materials 2004*, vol. 483, pp. 89-92, 2005.

[13] K. Masahara, M. Kushibe, H. Ohno, K. Kojima, T. Takahashi, Y. Ishida, T. Suzuki, T. Tanaka, S. Yoshida, and K. Arai, "Control of surface morphologies for epitaxial growth on low off-anglie 4H-SiC (0001) substrates," *Silicon Carbide and Related Materials, Ecscrm2000*, vol. 353-3, pp. 135-138, 2000.

[14] H. Tsuchida, I. Kamata, T. Miyanagi, T. Nakamura, K. Nakayama, R. Ishii, and Y. Sugawara, "Growth of thick 4H-SiC(0001) epilayers and reduction of basal plane dislocations," *Japanese Journal of Applied Physics Part 2-Letters & Express Letters*, vol. 44, pp. L806-L808, 2005.

[15] K. Nakayama, Y. Sugawara, H. Tsuchida, T. Miyanagi, I. Kamata, T. Nakamura, K. Asano, and R. Ishii, "8.3 kV 4H-SiC pin diode on (000-1) C-face with small forward voltage degradation," *Silicon Carbide and Related Materials 2004*, vol. 483, pp. 969-972, 2005.

[16] Y. Tanaka, K. Fukuda, K. Arai, K. Kojima, T. Suzuki, and T. Yatsuo, "Reverse characteristics of pn diodes on 4H-SiC(000-1) C and (11-20) face," *Applied Physics Letters*, vol. 84, pp. 1774-1776, 2004.

[17] K. Wada, T. Kimoto, K. Nishikawa, and H. Matsunami, "Epitaxial growth of 4H-SIC on 4 degrees off-axis (0001) and (0001) substrates by hot-wall chemical vapor deposition," *Journal of Crystal Growth*, vol. 291, pp. 370-374, 2006.

[18] K. Kojima, H. Okumura, S. Kuroda, and K. Arai, "Homoepitaxial growth of 4H-SiC on on-axis (0001(-)) C-face substrates by chemical vapor depositon," *Journal of Crystal Growth*, vol. 269, pp. 367-376, 2004.

[19] W. Chen and M. A. Capano, "Growth and characterization of 4H-SiC epilayers on substrates with different off-cut angles," *Journal of Applied Physics*, vol. 98, pp. 114907, 2005.

[20] K. Kojima, T. Suzuki, S. Kuroda, J. Nishio, and K. Arai, "Epitaxial growth of high-quality 4H-SiC carbon-face by low-pressure hot-wall chemical vapor deposition," *Japanese Journal of Applied Physics Part 2-Letters*, vol. 42, pp. L637-L639, 2003.

[21] K. S. Ramaiah, I. Bhat, T. P. Chow, J. K. Kim, E. F. Schubert, D. Johnstone, and S. Akarca-Biyikli, "Growth and characterization of SiC epitaxial layers on Si- and

C-face 4H SiC substrates by chemical-vapor deposition," *Journal of Applied Physics*, vol. 98, pp. 106108, 2005.

[22] D. J. Larkin, "SiC dopant incorporation control using site-competition CVD," *Physica Status Solidi B-Basic Research*, vol. 202, pp. 305-320, 1997.

[23] W. J. Choyke, H. Matsunami, and G. Pensl, *Silicon carbide : recent major advances*. Berlin ; New York: Springer, 2004.

[24] S. Ha, P. Mieszkowski, M. Skowronski, and L. B. Rowland, "Dislocation conversion in 4H silicon carbide epitaxy," *Journal of Crystal Growth*, vol. 244, pp. 257-266, 2002.

[25] T. Ohno, H. Yamaguchi, S. Kuroda, K. Kojima, T. Suzuki, and K. Arai, "Influence of growth conditions on basal plane dislocation in 4H-SiC epitaxial layer," *Journal of Crystal Growth*, vol. 271, pp. 1-7, 2004.

[26] J. A. Cooper and A. Agarwal, "SiC power-switching devices - The second electronics revolution?," *Proceedings of the IEEE*, vol. 90, pp. 956-968, 2002.

[27] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE*, vol. 90, pp. 969-986, 2002.

[28] R. Singh, J. A. Cooper, M. R. Melloch, T. P. Chow, and J. W. Palmour, "SiC power Schottky and PiN diodes," *IEEE Transactions on Electron Devices*, vol. 49, pp. 665-672, 2002.

[29] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, and T. Hayashi, "12-19KV 4H-SiC pin diodes with low power loss," *Proceedings of 2001 International Symposium on Power Semiconductor Devices & ICs, Osaka*, pp. 27-30, 2001.

[30] R. Singh, K. G. Irvine, D. C. Capell, J. T. Richmond, D. Berning, A. R. Hefner, and J. W. Palmour, "Large area, ultra-high voltage 4H-SiC p-i-n rectifiers," *IEEE Transactions on Electron Devices*, vol. 49, pp. 2308-2316, 2002.

[31] J. J. Sumakeris, M. Das, H. M. Hobgood, S. G. Muller, M. J. Paisley, S. Ha, M. Skowronski, J. W. Palmour, and C. H. Carter, "Approaches to stabilizing the forward voltage of bipolar SiC devices," *Silicon Carbide and Related Materials 2003, Pts 1 and 2*, vol. 457-460, pp. 1113-1116, 2004.

[32] B. A. Hull, M. K. Das, J. J. Sumakeris, J. T. Richmond, and S. Krishnaswami, "Drift-free 10-kV, 20-A 4H-SiC PiN diodes," *Journal of Electronic Materials*, vol. 34, pp. 341-344, 2005.

[33] S. Krishnaswami, A. Agarwal, S. H. Ryu, C. Capell, J. Richmond, J. Palmour, S. Balachandran, T. P. Chow, S. Bayne, B. Geil, K. Jones, and C. Scozzie, "1000-V, 30-A 4H-SiC BJTs with high current gain," *Ieee Electron Device Letters*, vol. 26, pp. 175-177, 2005.

[34] A. Q. Huang and B. Zhang, "Comparing SiC switching power devices: MOSFET, NPN transistor and GTO thyristor," *Solid-State Electronics*, vol. 44, pp. 325-340, 2000.

[35] T. P. Chow, "SiC bipolar power devices," *MRS Bulletin*, vol. 30, pp. 299-304, 2005.

[36] J. Zhang, J. H. Zhao, P. Alexandrov, and T. Burke, "Demonstration of first 9.2 kV 4H-SiC bipolar junction transistor," *Electronics Letters*, vol. 40, pp. 1381-1383, 2004.

[37] A. K. Agarwal, S. Krishnaswami, J. Richmond, C. Capell, S.-H. Ryu, J. Palmour, B. Geil, D. Katsis, and C. Scozzie, "Influence of Basal Plane Dislocation Induced Stacking Faults on the Current Gain in SiC BJTs," *Final Technical Program, ICSCRM 2005*, pp. 69.

[38] S.-H. Ryu, R. Singh, and J. W. Palmour, "High-power p-channel UMOS IGBT's in 6H-SiC for high temperature operation," *Materials Science Forum*, vol. 338-342, pp. 1427-1430, 2000.

[39] R. Singh, S. H. Ryu, D. C. Capell, and J. W. Palmour, "High temperature SiC trench gate p-IGBTs," *Ieee Transactions on Electron Devices*, vol. 50, pp. 774-784, 2003.

[40] Q. Zhang, H.-R. Chang, M. Gomez, C. Bui, E. Hanna, J. A. Higgins, T. Isaacs-Smith, and J. R. Williams, "10kV trench gate IGBTs on 4H-SiC," *Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs, ISPSD'05, 2005*, pp. 303-306.

[41] M. Iwami, "Silicon carbide: fundamentals," *Nuclear Instruments & Methods in Physics Research Section a-Accelerators Spectrometers Detectors and Associated Equipment*, vol. 466, pp. 406-411, 2001.

[42] W. J. Choyke and G. Pensl, "Physical properties of SiC," *MRS Bulletin*, vol. 22, pp. 25-29, 1997.

[43] M. Lades, W. Kaindl, N. Kaminski, E. Niemann, and G. Wachutka, "Dynamics of incomplete ionized dopants and their impact on 4H/6H-SiC devices," *IEEE Transactions on Electron Devices*, vol. 46, pp. 598-604, 1999.

[44] P. G. Neudeck, "SiC Technology," in *The VLSI Handbook, The Electrical Engineering Handbook Series*. Boca Raton, Florida: CRC Press and IEEE Press, 2000.

[45] Z. C. Feng and J. H. Zhao, *Silicon carbide : materials, processing, and devices*. New York: Taylor & Francis, 2004.

[46] Y. M. Tairov and V. F. Tsvetkov, "General-Principles of Growing Large-Size Single-Crystals of Various Silicon-Carbide Polytypes," *Journal of Crystal Growth*, vol. 52, pp. 146-150, 1981.

[47] S. G. Muller, R. C. Glass, H. M. Hobgood, V. F. Tsvetkov, M. Brady, D. Henshall, J. R. Jenny, D. Malta, and C. H. Carter, "The status of SiC bulk growth from an industrial point of view," *Journal of Crystal Growth*, vol. 211, pp. 325-332, 2000.

[48] K. Kojima, S. Nishizawa, S. Kuroda, H. Okumura, and K. Arai, "Effect of growth condition on micropipe filling of 4H-SiC epitaxial layer," *Journal of Crystal Growth*, vol. 275, pp. e549-e554, 2005.

[49] D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, and K. Takatori, "Ultrahigh-quality silicon carbide single crystals," *Nature*, vol. 430, pp. 1009-1012, 2004.

[50] M. Syvajarvi, R. Yakimova, R. R. Ciechonski, A. Kakanakova-Georgieva, L. Storasta, and E. Janzen, "Deep levels in 4H-SiC layers grown by sublimation epitaxy," *Optical Materials*, vol. 23, pp. 61-64, 2003.

[51] S. V. Rendakova, I. P. Nikitina, A. S. Tregubova, and V. A. Dmitriev, "Micropipe and dislocation density reduction in 6H-SiC and 4H-SiC structures grown by liquid phase epitaxy," *Journal of Electronic Materials*, vol. 27, pp. 292-295, 1998.

[52] A. Ellison, J. Zhang, W. Magnusson, A. Henry, Q. Wahab, J. P. Bergman, C. Hemmingsson, N. T. Son, and E. Janzen, "Fast SiC epitaxial growth in a chimney CVD reactor and HTCVD crystal growth developments," *Silicon Carbide and Related Materials - 1999 Pts, 1 & 2*, vol. 338-3, pp. 131-136, 2000.

[53] A. Ellison, J. Zhang, A. Henry, and E. Janzen, "Epitaxial growth of SiC in a chimney CVD reactor," *Journal of Crystal Growth*, vol. 236, pp. 225-238, 2002.

[54] B. E. Landini, "Susceptor effects on the morphological and impurity properties of 4H-SiC epilayers," *Journal of Electronic Materials*, vol. 29, pp. 384-390, 2000.

[55] A. Veneroni, F. Omarini, D. Moscatelli, M. Masi, S. Leone, M. Mauceri, G. Pistone, and G. Abbondanza, "Modeling of epitaxial silicon carbide deposition," *Journal of Crystal Growth*, vol. 275, pp. e295-e300, 2005.

[56] M. D. Allendorf and R. J. Kee, "A Model of Silicon-Carbide Chemical Vapor-Deposition," *Journal of the Electrochemical Society*, vol. 138, pp. 841-852, 1991.

[57] J. Meziere, M. Ucar, E. Blanquet, M. Pons, P. Ferret, and L. Di Cioccio, "Modeling and simulation of SiC CVD in the horizontal hot-wall reactor concept," *Journal of Crystal Growth*, vol. 267, pp. 436-451, 2004.

[58] A. O. Konstantinov, C. Hallin, B. Pecz, O. Kordina, and E. Janzen, "The mechanism for cubic SiC formation on off-oriented substrates," *Journal of Crystal Growth*, vol. 178, pp. 495-504, 1997.

[59] P. Deak, B. Aradi, A. Gali, and U. Gerstmann, ""Some like it shallower" - p-type doping in SiC," *Physica Status Solidi B-Basic Research*, vol. 235, pp. 139-145, 2003.

[60] D. J. Larkin, "An overview of SiC epitaxial growth," *MRS Bulletin*, vol. 22, pp. 36-41, 1997.

[61] K. Danno, T. Kimoto, K. Asano, Y. Sugawara, and H. Matsunami, "Fast epitaxial growth of high-purity 4H-SiC(000(1)over-bar) in a vertical hot-wall chemical vapor deposition," *Journal of Electronic Materials*, vol. 34, pp. 324-329, 2005.

[62] K. Kojima, S. Kuroda, H. Okumura, and K. Arai, "Influence of lattice polarity of nitrogen and aluminum doping on 4H-SiC epitaxial layer," *Microelectronic Engineering*, vol. 83, pp. 79-81, 2006.

[63] K. Kojima, S. Kuroda, H. Okumura, and K. Arai, "Nitrogen incorporation characteristics on a 4H-SiC epitaxial layer," *Applied Physics Letters*, vol. 88, pp. -, 2006.

[64] U. Forsberg, O. Danielsson, A. Henry, M. K. Linnarsson, and E. Janzen, "Nitrogen doping of epitaxial silicon carbide," *Journal of Crystal Growth*, vol. 236, pp. 101-112, 2002.

[65] J. J. Sumakeris, M. K. Das, S. Ha, E. Hurt, K. Irvine, M. J. Paisley, M. J. O'Loughlin, J. W. Palmour, M. Skowronski, H. M. Hobgood, and C. H. Carter, "Development of epitaxial SiC processes suitable for bipolar power devices," *Silicon Carbide and Related Materials 2004*, vol. 483, pp. 155-158, 2005.

[66] I. Kamata, H. Tsuchida, T. Jikimoto, and K. Izumi, "Influence of 4H-SiC growth conditions on micropipe dissociation," *Japanese Journal of Applied Physics Part 2-Letters*, vol. 41, pp. L1137-L1139, 2002.

[67] H. Tsuchida, I. Kamata, and K. Izumi, "Epitaxial growth of a low-doped 4H-SiC layer on a micropipe stop layer," *Japanese Journal of Applied Physics Part 2-Letters*, vol. 41, pp. L1300-L1302, 2002.

[68] M. Benamara, X. Zhang, M. Skowronski, P. Ruterana, G. Nouet, J. J. Sumakeris, M. J. Paisley, and M. J. O'Loughlin, "Structure of the carrot defect in 4H-SiC epitaxial layers," *Applied Physics Letters*, vol. 86, pp. -, 2005.

[69] Z. Zhang, E. Moulton, and T. S. Sudarshan, "Mechanism of eliminating basal plane dislocations in SiC thin films by epitaxy on an etched substrate," *Applied Physics Letters*, vol. 89, pp. -, 2006.

[70] J. A. Powell and D. J. Larkin, "Process-induced morphological defects in epitaxial CVD silicon carbide," *Physica Status Solidi B-Basic Research*, vol. 202, pp. 529-548, 1997.

[71] P. G. Neudeck, "Perimeter governed minority carrier lifetimes in 4H-SiC p(+)n diodes measured by reverse recovery switching transient analysis," *Journal of Electronic Materials*, vol. 27, pp. 317-323, 1998.

[72] D. K. Schroder, *Semiconductor material and device characterization*, 2nd ed. New York: Wiley, 1998.

[73] R. F. Pierret, *Advanced semiconductor fundamentals*, 2nd ed. Upper Saddle River, N.J.: Prentice Hall, 2003.

[74] A. Galeckas, J. Linnros, M. Frischholz, K. Rottner, N. Nordell, S. Karlsson, and V. Grivickas, "Investigation of surface recombination and carrier lifetime in 4H/6H-SiC," *Materials Science and Engineering B-Solid State Materials for Advanced Technology*, vol. 61-2, pp. 239-243, 1999.

[75] J. P. Bergman, O. Kordina, and E. Janzen, "Time resolved spectroscopy of defects in SiC," *Physica Status Solidi a-Applied Research*, vol. 162, pp. 65-77, 1997.

[76] O. Kordina, J. P. Bergman, C. Hallin, and E. Janzen, "The minority carrier lifetime of n-type 4H- and 6H-SiC epitaxial layers," *Applied Physics Letters*, vol. 69, pp. 679-681, 1996.

[77] J. Zhang, L. Storasta, J. P. Bergman, N. T. Son, and E. Janzen, "Electrically active defects in n-type 4H-silicon carbide grown in a vertical hot-wall reactor," *Journal of Applied Physics*, vol. 93, pp. 4708-4714, 2003.

[78] T. Tawara, H. Tsuchida, S. Izumi, I. Kamata, and K. Izumi, "Evaluation of free carrier lifetime and deep levels of the thick 4H-SiC epilayers," *Silicon Carbide and Related Materials 2003, Pts 1 and 2*, vol. 457-460, pp. 565-568, 2004.

[79] T. Dalibor, G. Pensl, N. Nordell, and A. Schoner, "Electrical properties of the titanium acceptor in silicon carbide," *Physical Review B*, vol. 55, pp. 13618-13624, 1997.

[80] K. Danno, K. Hashimoto, H. Saitoh, T. Kimoto, and H. Matsunami, "Low-concentration deep traps in 4H-SiC grown with high growth rate by chemical vapor deposition," *Japanese Journal of Applied Physics Part 2-Letters & Express Letters*, vol. 43, pp. L969-L971, 2004.

[81] T. Kimoto, S. Nakazawa, K. Hashimoto, and H. Matsunami, "Reduction of doping and trap concentrations in 4H-SiC epitaxial layers grown by chemical vapor deposition," *Applied Physics Letters*, vol. 79, pp. 2761-2763, 2001.

[82] K. Fujihira, T. Kimoto, and H. Matsunami, "Growth and characterization of 4H-SiC in vertical hot-wall chemical vapor deposition," *Journal of Crystal Growth*, vol. 255, pp. 136-144, 2003.

[83] I. Pintilie, L. Pintilie, K. Irmscher, and B. Thomas, "Formation of the Z(1,2) deep-level defects in 4H-SiC epitaxial layers: Evidence for nitrogen participation," *Applied Physics Letters*, vol. 81, pp. 4841-4843, 2002.

[84] M. S. Mazzola, S. E. Saddow, P. G. Neudeck, V. K. Lakdawala, and S. We, "Observation of the D-Center in 6h-Sic P-N Diodes Grown by Chemical-Vapor-Deposition," *Applied Physics Letters*, vol. 64, pp. 2730-2732, 1994.

[85] J. Nishio, M. Kushibe, K. Masahara, K. Kojima, T. Ohno, Y. Ishida, T. Takahashi, T. Suzuki, T. Tanaka, S. Yoshida, and K. Arai, "Investigation of residual impurities in 4H-SiC epitaxial layers grown by hot-wall chemical vapor deposition," *Silicon Carbide and Related Materials 2001, Pts 1 and 2, Proceedings*, vol. 389-3, pp. 215-218, 2002.

[86] N. Ramungul, V. Khemka, T. P. Chow, M. Ghezzo, and J. Kretchmer, "Carrier lifetime extraction from a 6H-SiC high voltage p-i-n rectifier reverse recovery waveform," *Silicon Carbide, III-Nitrides and Related Materials, Pts 1 and 2*, vol. 264-2, pp. 1065-1068, 1998.

[87] A. Udal and E. Velmre, "Measurement of charge carrier lifetime temperature-dependence in 4H-SiC power diodes," *Silicon Carbide and Related Materials - 1999 Pts, 1 & 2*, vol. 338-3, pp. 781-784, 2000.

[88] K. Y. Cheong, S. Dimitrijev, and J. Han, "Comparison of charge-retention times in n- and p-type 4H-SiC MOS capacitors as non-volatile memory elements," *Journal of Crystal Growth*, vol. 268, pp. 547-553, 2004.

[89] K. Y. Cheong, S. Dimitrijev, and J. S. Han, "Investigation of electron-hole generation in MOS capacitors on 4H SiC," *IEEE Transactions on Electron Devices*, vol. 50, pp. 1433-1439, 2003.

[90] C.-F. Huang, "Development of 4H-SIC BJTS for power electronics applications," Purdue University, 2003.

[91] M. Tabib-Azar, S. M. Hubbard, C. M. Schnabel, and S. Bailey, "Mapping of crystal defects and the minority carrier diffusion length in 6H-SiC using a novel electron beam induced current technique," *Journal of Applied Physics*, vol. 84, pp. 3986-3992, 1998.

[92] C. Diaz-Guerra and J. Piqueras, "Electron-beam-induced current study of electrically active defects in 4H-SiC," *Journal of Physics-Condensed Matter*, vol. 16, pp. S217-S223, 2004.

[93] Y. Wang, G. N. Ali, M. K. Mikhov, V. Vaidyanathan, B. J. Skromme, B. Raghothamachar, and M. Dudley, "Correlation between morphological defects, electron beam-induced current imaging, and the electrical properties of 4H-SiC Schottky diodes," *Journal of Applied Physics*, vol. 97, pp. -, 2005.

[94] S. Maximenko, S. Soloviev, D. Cherednichenko, and T. Sudarshan, "Observation of dislocations in diffused 4H-SiC p-i-n diodes by electron-beam induced current," *Journal of Applied Physics*, vol. 97, pp. -, 2005.

[95] B. J. Baliga, *Power semiconductor devices*. Boston: PWS Publishing Co., 1996.

[96] S. M. Sze, *Physics of semiconductor devices*, 2nd ed. New York: Wiley, 1981.

[97] D. C. Sheridan, G. F. Niu, J. N. Merrett, J. D. Cressler, C. Ellis, and C. C. Tin, "Design and fabrication of planar guard ring termination for high-voltage SiC diodes," *Solid-State Electronics*, vol. 44, pp. 1367-1372, 2000.

[98] D. C. Sheridan, G. F. Niu, and J. D. Cressler, "Design of single and multiple zone junction termination extension structures for SiC power devices," *Solid-State Electronics*, vol. 45, pp. 1659-1664, 2001.

[99] G. Wagner, J. Doerschel, and A. Gerlitzke, "Surface preparation of 4H-SiC substrates for hot-wall CVD of SiC layers," *Applied Surface Science*, vol. 184, pp. 55-59, 2001.

[100] C. Hallin, F. Owman, P. Martensson, A. Ellison, A. Konstantinov, O. Kordina, and E. Janzen, "In situ substrate preparation for high-quality SiC chemical vapour deposition," *Journal of Crystal Growth*, vol. 181, pp. 241-253, 1997.

[101] E. Neyret, L. Di Cioccio, E. Blanquet, C. Raffy, C. Pudda, T. Billon, and J. Camassel, "SiC in-situ pre-growth etching: A thermodynamic study," *Silicon Carbide and Related Materials - 1999 Pts, 1 & 2*, vol. 338-3, pp. 1041-1044, 2000.

[102] A. A. Burk and L. B. Rowland, "The role of excess silicon and in situ etching on 4H-SiC and 6H-SiC epitaxial layer morphology," *Journal of Crystal Growth*, vol. 167, pp. 586-595, 1996.

[103] M. Syvajarvi, R. Yakimova, A. L. Hylen, and E. Janzen, "Anisotropy of dissolution and defect revealing on SiC surfaces," *Journal of Physics-Condensed Matter*, vol. 11, pp. 10041-10046, 1999.

[104] G. Wagner, B. Thomas, J. Doerschel, J. Dolle, and K. Irmscher, "Structural and electrical properties of unintentionally doped 4H-SiC epitaxial layers - Grown by hot-wall CVD," *Journal of Electronic Materials*, vol. 30, pp. 207-211, 2001.

[105] T. Yamamoto, T. Kimoto, and H. Matsunami, "Impurity incorporation mechanism in step-controlled epitaxy growth temperature and substrate off-angle dependence," *Silicon Carbide, III-Nitrides and Related Materials, Pts 1 and 2*, vol. 264-2, pp. 111-114, 1998.

[106] T. Kimoto, A. Itoh, and H. Matsunami, "Incorporation Mechanism of N, Al, and B Impurities in Chemical-Vapor-Deposition of Sic," *Applied Physics Letters*, vol. 67, pp. 2385-2387, 1995.

[107] J. A. Powell, D. J. Larkin, and P. B. Abel, "Surface-Morphology of Silicon-Carbide Epitaxial-Films," *Journal of Electronic Materials*, vol. 24, pp. 295-301, 1995.

[108] M. Syvajarvi, R. Yakimova, A. Henry, and E. Janzen, "Polytype inclusions and triangular stacking faults in 4H-SiC layers grown by sublimation epitaxy," *Physica Scripta*, vol. T79, pp. 64-66, 1999.

[109] C. Hallin, A. O. Konstantinov, B. Pecz, O. Kordina, and E. Janzen, "The origin of 3C polytype inclusions in epitaxial layers of silicon carbide grown by chemical vapour deposition," *Diamond and Related Materials*, vol. 6, pp. 1297-1300, 1997.

[110] W. L. Zhou, P. Pirouz, and J. A. Powell, "The origin of triangular surface defects in 4H-SiC CVD epilayers," *Silicon Carbide, III-Nitrides and Related Materials, Pts 1 and 2*, vol. 264-2, pp. 417-420, 1998.

[111] T. Kimoto, A. Itoh, H. Matsunami, and T. Okano, "Step bunching mechanism in chemical vapor deposition of 6H- and 4H-SiC{0001}," *Journal of Applied Physics*, vol. 81, pp. 3494-3500, 1997.

[112] N. Ohtani, M. Katsuno, T. Aigo, T. Fujimoto, H. Tsuge, H. Yashiro, and M. Kanaya, "Step bunching behaviour on the {0001} surface of hexagonal SiC," *Journal of Crystal Growth*, vol. 210, pp. 613-622, 2000.

[113] M. Syvajarvi, R. Yakimova, and E. Janzen, "Step-bunching in SiC epitaxy: anisotropy and influence of growth temperature," *Journal of Crystal Growth*, vol. 236, pp. 297-304, 2002.

[114] T. Kimoto, A. Itoh, and H. Matsunami, "Step Bunching in Chemical-Vapor-Deposition of 6h-Sic and 4h-Sic on Vicinal Sic(0001) Faces," *Applied Physics Letters*, vol. 66, pp. 3645-3647, 1995.

[115] H. Nakagawa, S. Tanaka, and I. Suemune, "Self-ordering of nanofacets on vicinal SiC surfaces," *Physical Review Letters*, vol. 91, pp. 226107/1-226107/4, 2003.

[116] V. I. Marchenko and A. Y. Parshin, "On the Elastic Properties of Crystal-Surfaces," *Zhurnal Eksperimentalnoi I Teoreticheskoi Fiziki*, vol. 79, pp. 257-260, 1980.

[117] P. Hecquet, "Surface stress stabilizes vicinal surfaces," *Surface Science*, vol. 561, pp. 127-146, 2004.

[118] R. V. Kukta, A. Peralta, and D. Kouris, "Elastic interaction of surface steps: Effect of atomic-scale roughness," *Physical Review Letters*, vol. 88, pp. 186102/1-186102/4, 2002.

[119] S. Nakamura, T. Kimoto, and H. Matsunami, "Effect of C/Si ratio on spiral growth on 6H-SiC (0001)," *Japanese Journal of Applied Physics Part 2-Letters*, vol. 42, pp. L846-L848, 2003.

[120] Z. Zhang and T. S. Sudarshan, "Basal plane dislocation-free epitaxy of silicon carbide," *Applied Physics Letters*, vol. 87, pp. -, 2005.

[121] M. Skowronski and S. Ha, "Degradation of hexagonal silicon-carbide-based bipolar devices," *Journal of Applied Physics*, vol. 99, pp. -, 2006.

[122] J. Sumakeris, B. Hull, and D. Grider, "Etching and regrowth technique increases bipolar diode stability," *Compound Semiconductor*, vol. 12, pp. 25-28, 2006.

[123] R. H. Doremus, *Growth and perfection of crystals; proceedings*. New York,: Wiley, 1958.

[124] J. P. Vandereerden and H. Mullerkrumbhaar, "Dynamic Coarsening of Crystal-Surfaces by Formation of Macrosteps," *Physical Review Letters*, vol. 57, pp. 2431-2433, 1986.

[125] D. Kandel and J. D. Weeks, "Theory of Impurity-Induced Step Bunching," *Physical Review B*, vol. 49, pp. 5554-5564, 1994.

[126] K. Kojima, S. Kuroda, H. Okumura, and K. Arai, "Nitrogen incorporation characteristics on a 4H-SiC epitaxial layer," *Applied Physics Letters*, vol. 88, pp. 021907, 2006.

[127] Y. Negoro, T. Kimoto, and H. Matsunami, "Stability of deep centers in 4H-SiC epitaxial layers during thermal annealing," *Applied Physics Letters*, vol. 85, pp. 1716-1718, 2004.

[128] K. Fujihira, S. Tamura, T. Kimoto, and H. Matsunami, "Low-loss, high-voltage 6H-SiC epitaxial p-i-n diode," *IEEE Transactions on Electron Devices*, vol. 49, pp. 150-154, 2002.

[129] U. Zimmermann, J. Osterman, D. Kuylenstierna, A. Hallen, A. O. Konstantinov, W. M. Vetter, and M. Dudley, "Material defects in 4H-silicon carbide diodes," *Journal of Applied Physics*, vol. 93, pp. 611-618, 2003.

[130] S. Y. Ha and J. P. Bergman, "Degradation of SiC high-voltage pin diodes," *MRS Bulletin*, vol. 30, pp. 305-307, 2005.

[131] S. Ha, M. Skowronski, and H. Lendenmann, "Nucleation sites of recombination-enhanced stacking fault formation in silicon carbide p-i-n diodes," *Journal of Applied Physics*, vol. 96, pp. 393-398, 2004.

[132] R. E. Stahlbush, M. Fatemi, J. B. Fedison, S. D. Arthur, L. B. Rowland, and S. Wang, "Stacking-fault formation and propagation in 4H-SiC PiN diodes," *Journal of Electronic Materials*, vol. 31, pp. 370-375, 2002.

[133] M. Skowronski, J. Q. Liu, W. M. Vetter, M. Dudley, C. Hallin, and H. Lendenmann, "Recombination-enhanced defect motion in forward-biased 4H-SiC p-n diodes," *Journal of Applied Physics*, vol. 92, pp. 4699-4704, 2002.

[134] V. Grivickas, J. Linnros, and A. Galeckas, "Depth- and time-resolved free carrier absorption in 4H SiC epilayers: A study of carrier recombination and transport parameters," *Materials Science Forum*, vol. 264-268, pp. 529-532, 1998.

[135] A. B. Sproul, "Dimensionless Solution of the Equation Describing the Effect of Surface Recombination on Carrier Decay in Semiconductors," *Journal of Applied Physics*, vol. 76, pp. 2851-2854, 1994.

[136] A. Galeckas, J. Linnros, M. Frischholz, and V. Grivickas, "Optical characterization of excess carrier lifetime and surface recombination in 4H/6H-SiC," *Applied Physics Letters*, vol. 79, pp. 365-367, 2001.

[137] F. La Via, G. Galvagno, G. Foti, M. Mauceri, S. Leone, G. Pistone, G. Abbondanza, A. Veneroni, M. Masi, G. L. Valente, and D. Crippa, "4H SiC epitaxial growth with chlorine addition," *Chemical Vapor Deposition*, vol. 12, pp. 509-515, 2006.

[138] R. Myers, O. Kordina, Z. Shishkin, S. Rao, R. Everly, and S. E. Saddow, "Increased growth rate in a SiCCVD reactor using HCl as a growth additive," *Silicon Carbide and Related Materials 2004*, vol. 483, pp. 73-76, 2005.

2.2 Activities at Carnegie Mellon University (M. Skowronski)

2.2 Activities at Carnegie Mellon University (M. Skowronski)

2.2.1 Characterization of deep traps and carrier lifetimes in 4H-SiC epilayers

Some of the characteristic of materials grown as part of this effort are included as part of the previous section. This one focuses only on measurements of deep trap concentrations in the 4H-SiC bandgap and their effect on minority carrier lifetimes.

2.2.1.1 Background: deep traps in silicon carbide

Figure 2.69 shows the schematic diagram with 4H-SiC bandgap and positions of deep levels detected in Deep Level Transient Spectroscopy experiments. Although many of deep centers in 4H-SiC have been reported in as-deposited and irradiated samples, in high-quality of SiH_4-based CVD-grown 4H-SiC epilayers typically only three deep electron traps are observed. Those centers are Ti (0.14 eV) center, Z center (0.65 eV) and EH6/EH7 (1.5 eV) centers below conduction band.

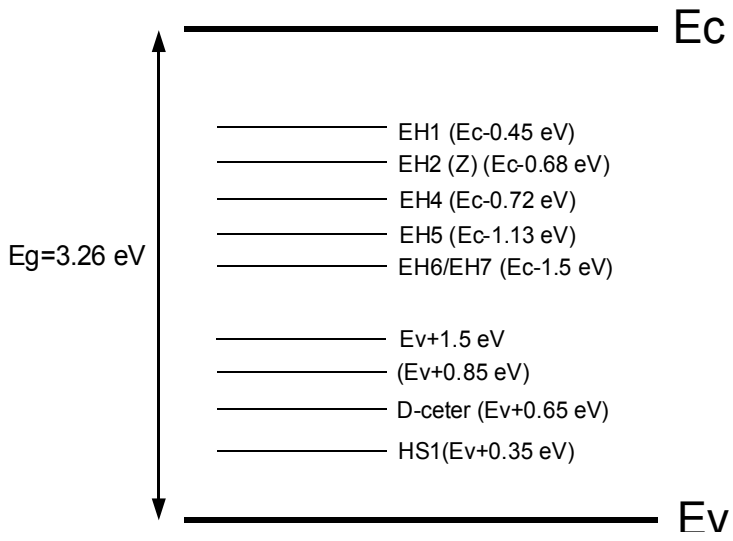


Fig. 2.69 Schematic diagram of deep levels in 4H-SiC determined by DLTS measurements.

Ti-related centers were identified by implanting the SiC crystals with the radioactive isotope ^{48}V which decays to the stable ^{48}Ti. [1] These authors investigated change of DLTS spectra with time corresponding to the decau of 48V and concluded that Ti-related levels were located 0.14 eV and 0.17 eV from conduction band edge. The two

DLTS peaks being were interpreted as due to substitutional vanadium occupying hexagonal and cubic silicon sites. Ti-related centers have not been reported in 6H-SiC. This was due to the fact that the ground state of Ti in 6H-SiC is degenerate with the conduction band of 6H-SiC.

Most thoroughly studied centers in 4H-SiC are EH2 (also referred to as the Z or Z1/Z2 center) and EH6/EH7 because they are the dominant centers in high quality crystals and suspected to be the recombination centers in 4H-SiC. Z centers in 4H-SiC were demonstrated to have negative-U properties with the acceptor -/+ state near E_c-0.7 eV and the donor 0/+ state near E_c-0.4 eV. Since negative-U centers are quite rare, it is expected that the Z center in 4H-SiC has the same origin as that of Z center in 6H-SiC. This is further supported by the center activation energy. The valence-band edge of all SiC polytypes (4H, 6H, 15R, and 3C) is at the same distance from the vacuum level as determined by experimental and theoretical studies [2]. Using this as a reference, the energy level of Z center is aligned in 4H and 6H polytypes. The origin of Z centers in either polytype, was not identified and remains a matter of controversy. Different authors suggested isolated carbon vacancies V_c [3], V_{si} [4] and V_c-V_{si} vacancy complexes [5] have been suggested as possible atomic structure of this defect. Most of recent results on high quality of epilayers show that the Z center concentration increases with Si/C ratio suggesting that the center is related to silicon excess. Possible candidates are Si_C, V_C, and I_{Si}. Zhang *et. al.* [6], Fujihira *et. al.* [7] and Kimoto *et. al.* [3], reported the identical trend in the range of C/Si = 0.3 ~ 0.45, 0.6 ~ 0.8, and 1.0 ~1.5, respectively that the concentrations of all the deep centers in 4H-SiC epilayers grown by SiH_4 CVD process decrease with increasing C/Si ratio. On the other hand, Pintilie *et. al.* [4] argued that in the intentionally nitrogen-doped samples with the range of C/Si = 1.2 ~ 3.0, the Z center concentration increases with increasing C/Si ratio in samples with the same carrier concentration (N_d-N_a) for each C/Si ratio. However, due to site-competition effect, if the samples were grown at same growth condition (specifically, nitrogen doping flow condition), the samples grown at various C/Si ratios can not have the same doping concentration. Hence, their interpretation is questionable.

EH6/EH7 centers were first reported by Hemmingsson in the irradiated sample. [8] Later, the same centers were also observed in as-grown material. [3] Based on the EH6/EH7 concentrations change with C/Si ratio in CVD-grown samples, Danno *et. al.* suggested that the center is V_c-related center. The calculated band-gap position of positively charged carbon vacancy [9] is 1.5 eV from the conduction band which is very close to activation energy of EH6/EH7. The centers were claimed as acceptor-like trap

based on the fact that the activation energy of EH6/EH7 center is unchanged with changing applied electric field in the depletion region of the Schottky barrier.

Three hole traps are also commonly detected in the lower half of 4H-SiC band gap. HS1 center has the level located 0.35 eV above the valence band. The center was observed by MCTS technique in n-type as grown samples. Later, the center concentration was correlated with a photoluminescence band referred to as D1 Storasta *et. al.* [10] demonstrated that HS1 center concentration changes in the same way as D1 PL center intensity changes with various annealing temperatures. Recent model of pseudodonor also predicts that D1 center is associated with a hole trap with energy level of 0.35 eV from valence band edge. The energy level frequently seen in in DLTS spectra on p-type material located at 0.3 eV is due to boron was determined by Hall effect measurement as 300 meV from valence band in 4H and 6H SiC. [11] [12] Since boron is closer in size to C than Si, it is expected that boron replaces C. However, boron is reported to be incorporated into both C-site and Si-site. Matsumoto *et. al.* reported that shallow boron acceptor center has been identified to occupy Si-site (B_{Si}). On the other hand, experimental result in the samples grown by CVD method [13] showed that boron concentration increases with increasing C/Si ratio. This was explained by the fact that boron is incorporated into crystal together with hydrogen. In such a case, size of boron-hydrogen complex is comparable to Si size so that boron with hydrogen can take the place of Si site instead of C site. Larkin *et. al.* [13] demonstrated that in boron-doped p-type epilayers hydrogen concentration determined by photoluminescence and SIMS analysis increased with increasing boron concentration which was varied by C/Si ratio. It was also shown that after annealing at 1700 ^{o}C carrier concentration increased and hydrogen concentration by SIMS decreased which was explained by hydrogen depassivation from B-H complex. The above Larkin's experiments clearly show that boron is incorporated with hydrogen together in Si-site and electrical activity of boron atoms is passivated by hydrogen and is reactivated by annealing-out of hydrogen. Boron is also suspected to form a complex with unidentified intrinsic defects and form a complex D-center located 0.65 eV above the valence band edge. [14]

The hole trap with the activation energy of 0.65 eV (called D-center) was observed by several groups in PVT-grown bulk p-crystals or in CVD-grown epilayers. [15] [16] The structure of D-center was associated with donor-like complexes of boron with native defects such as $B_{si}^{-}+V_{c}^{+}$ or $B_{c}^{-}+V_{si}^{+}$. This association is based on Electron Paramagnetic Resonance (EPR) [17] [18] [19] Recently a deep hole trap which is located 1.55 eV above the valence band was reported in as-grown 4H-SiC epilayers. The center

was argued to act as donor-like trap because its emission rate did not change with the applied electric field .

2.2.1.2 Background: Carrier lifetimes in SiC

Carrier lifetime studies in SiC material have so far focused on qualitative correlations between dominant electron (Z-defect and EH6/7) [6, 20] and hole traps (D-center) with observed lifetimes. Zhang *et al*. [6] reported that the minority carrier lifetime was dependent on the flow direction and growth temperature of the epitaxial layers grown by CVD. The first of these effects was indirect: the origin of the change was due to the change of the C/Si ratio with position on the SiC substrate along the flow direction. These authors also observed that the minority carrier lifetimes increased as the concentrations of two dominant electron traps $Z_{1/2}$ and $EH_{6/7}$ decreased. The concentration of shallow B acceptors did not show any correlation with the minority carrier lifetimes. Similar results were reported by Tawara *et al.* [20], on CVD grown samples, which showed inverse correlation between carrier lifetimes with Z-defect and $EH_{6/7}$ defects concentration. However, these observations were qualitative and the dependences of both the carrier lifetimes and trap densities on growth conditions were rather weak. The lack of data on hole traps and extended defect densities further questioned the interpretations. In another study, Polyakov *et al*. [21] have shown the variation of the diffusion length of minority carriers along the growth axis of bulk SiC crystals grown by the Physical Vapor Transport method. The results showed that diffusion length of holes in lightly nitrogen doped 6H-SiC grown boule increased from the seed portion towards the tail. This result correlated well with electron trap densities that fell along the boule growth direction. It was interpreted as the effect f changing stoichiometry of the growth ambient. As the silicon-rich vapor leaks out of the quasi-closed crucible, the vapor becomes progressively carbon-rich decreasing the densities of silicon-excess related point defects. As the deep center concentration fall, the lifetimes increase.

During the course of this project, a group at Kyoto University reported that the carrier lifetimes are controlled by Z-defect in agreement with the findings described in this report. [22] Whenever the Z-defect concentration exceeds 10^{13} cm^{-3} in lightly doped n-type 4H-SiC epilayers, it typically acts as the dominant recombination center. In epilayers with Z-defect concentration less than that, other recombination processes such

as surface or extended defect-induced recombination are responsible for limiting carrier lifetimes. These conclusions were drawn based on injection level dependence of carrier lifetimes which show an increase in carrier lifetime with injection level for Z-defect limited carrier lifetimes and a decrease in carrier lifetime with injection level for 'other' processes controlling carrier lifetimes. This observation strengthens the conclusion but is not without its weaknesses. The only approach to identification of dominant recombination center is to determine both the minority and majority carrier capture cross sections. This would allow to construct the quantitative equation for carrier lifetime and to calculate the limit of the lifetime for a given sample with known trap concentration.

The following studies had a two-fold aim - (1) correlation of growth conditions with types and concentration of impurities and native point defects (for both Si- and C-face grown epilayers), and subsequent correlation of deep traps with carrier lifetimes, and (2) extensive measurements of capture cross sections of concerned traps in order to provide quantitative estimate of carrier lifetimes using Shockley-Read-Hall (SRH) recombination model.

2.2.1.3 Experimental

The characterization methods used in this work included Deep Level transient Spectroscopy, Minority Carrier Transient Spectroscopy, Electron Beam Induced Current, and Photo-Induced Free Carrier Absorption. While most of these methods have been described in detail, a description of experimental approach and analysis of EBIC method are included here for readers convenience.

In EBIC, a focused electron beam from SEM is employed to excite electron-hole pairs in the semiconductor material. The schematic of EBIC planar scanning setup is shown in Fig. 2.70. The electron beam is incident perpendicular to the semiconductor surface. The range of electrons, R_e, denotes the penetration depth of the incident electron beam inside the semiconductor. The generated carriers diffuse randomly inside the material. The random diffusion of carriers is accompanied by trapping and recombination, in similar fashion as the optically excited excess carriers. The diffusion of generated holes in n-type material can be described by steady state continuity equation as follows:

$$g - \frac{1}{q}\nabla J_h - \frac{\Delta p}{\tau} = \frac{d\Delta p}{dt} = 0$$

where g is the generation rate, q is electronic charge, J_h is the hole diffusion flux, Dp is the excess hole concentration, and t is the minority carrier lifetime. The diffusion flux of holes can be written as:

$$J_h = \frac{-qD_p \partial \Delta p}{\partial x}$$

here D_p is the hole diffusion coefficient and x is parallel to the surface of semiconductor. The holes which diffuse to the boundary of space charge region of the Schottky diode are collected at the junction due to the built-in electric field. This collected charge constitutes the EBIC current. The solution of the above the equations is of the form:

$$\Delta p = const \times \exp\left(-\frac{x}{L_h}\right)$$

Here L_h is the hole diffusion length. In other words, the EBIC current decreases exponentially as the electron beam is scanned away from the edge of Schottky diode. Fitting the resulting EBIC profile as a function of scan distance, x, with theoretical curves yield surface recombination velocity and diffusion length of carriers.

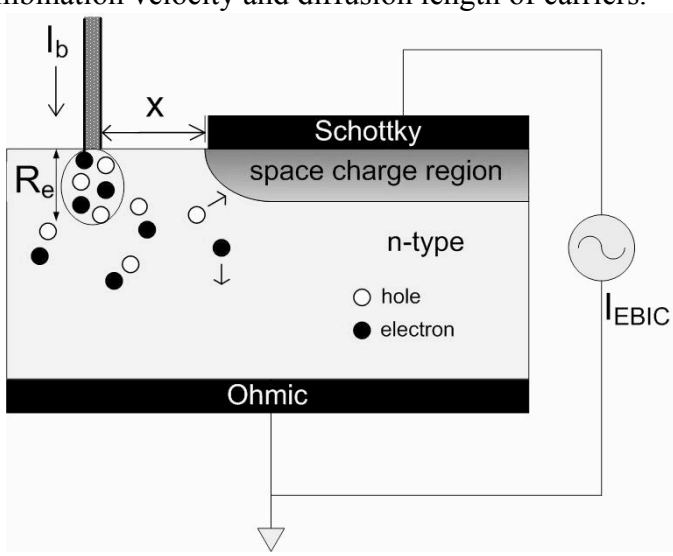


Fig. 2.70 Schematic of electron beam induced current (EBIC) technique. In the planar junction shown here, electron beam is incident perpendicular to the Schottky junction.

The theoretical modeling of EBIC profile is performed by estimating the collection efficiency of charge carriers at the Schottky junction. The energy of focused electron beam is typically in several keV range which is few orders of magnitude higher

than the energy required to excite single electron – hole pair. The energy of the incident electron beam required to ionize an electron from the valence band, *e*, is given by:

$$\varepsilon = 2.1E_g + 1.3$$

Here E_g, is the bandgap of material in eV ($E_g^{4H\text{-}SiC}$ = 3.2 eV; $E_g^{6H\text{-}SiC}$ = 3 eV). Thus, single electron is capable of producing several electron-hole pairs in the material. The range of incident electrons, R_e (cm), is given by the following expression:

$$R_e = \frac{2.56\times10^{-3}}{\rho}\left(\frac{V}{30}\right)^{1.7}$$

V is the incident electron beam accelerating voltage in kV, and r is the density of SiC (= 3.21 g/cm^3). Fig. 2.71 shows the dependence of R_e on incident electron beam accelerating voltage. As can be seen from the figure, the penetration depth of the incident electron beam varies from zero (at the surface) to 8 mm deeper from the surface for beam accelerating voltage of zero to 30 kV, respectively. Diffusion length measurements in the planar geometry configuration were typically performed at 25 kV which would correspond to the penetration depth of ~ 6 mm.

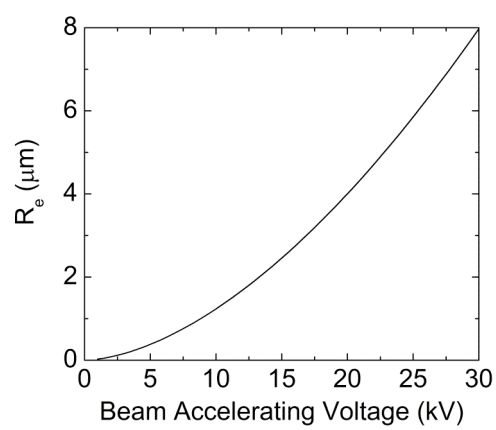


Fig. 2.71 Dependence of R_e on the incident electron beam accelerating voltage.

Therefore, the influence of trapping and recombination of free carriers at the surface states is expected to be more pronounced in the case of EBIC than the optical techniques. Latter techniques employ an excitation beam with photon energy corresponding to the bandgap of SiC (λ~355 nm) with penetration depth of ~50 mm.

The recombination at the surface is described in analogous terms to the bulk of the material as a product of trap density per unit area, capture cross section per trap, and the thermal velocity. The product has dimensions of cm/s and is consequently referred as surface recombination velocity, S. For the case of n-type material, the diffusion of holes to the surface can be mathematically written as:

$$S\Delta p = D_h \frac{\partial \Delta p}{\partial z}|_{z=0}$$

where D_h is the diffusion coefficient of holes, Δp is the excess hole density, z denotes the position coordinate normal to the surface of semiconductor. The above equation describe the boundary condition such that under the steady state, the minority carrier flux that recombines at the surface (left hand side) is equal to the minority carrier flux diffusing to the surface. Therefore, higher the surface recombination velocity, higher is the density of surface defects which leads to higher recombination rate at the surface.

The theoretical calculation of EBIC profiles for the planar geometry case has been extensively preformed by Kuiken and van Opdorp [23]. Although, complete details of the Kuiken and van Opdorp's model would consume considerable space, the main equations describing the EBIC profile are illustrated here for the sake of completeness:

$$Q \equiv \frac{I_{EBIC}}{qG} \approx \frac{(1/S'+Y_S)f(S')e^{-X_S}}{[X_S + g(S')]^{3/2}}$$

$$f(S') = \frac{(S'+1)^{1/2}}{\pi^{1/2}S'}\exp\left(\frac{1}{\pi}\int_0^{\pi/2}\ln(1+S'\sin\theta)d\theta\right)$$

$$g(S') = \frac{3}{4} + \frac{1}{\pi S'} + \frac{3}{2S'^2} - \frac{\sigma(S')}{\pi S'^2}$$

$$\sigma(S') = \sqrt{S'^2-1}\ln(S'+\sqrt{S'^2-1})$$

where Q is the charge collection efficiency defined as the ratio of collected I_{EBIC} current and generation rate, G. The above equations are written in terms of dimensionless variable:

S'= St/L_d: ratio of recombination velocity and diffusion velocity.

$X_s = x/L_d$; $Y_s = y/L_d$: denotes the dimensionless coordinates of the point source. Y_s is assumed to lie $1/3R_e$ below the surface [24] . The generation rate is given by [25]:

$$G = \langle g \rangle \frac{EJ_b(1-f)}{\varepsilon q}$$

In this expression, <g> is the normalized distribution, E is the incident electron beam energy in kV, J_b is the incident electron current density (measured experimentally), f is the fraction of electron beam energy that is reflected by the sample (f~0.07 for SiC), e is the energy required to produce single electron hole pair.

The line scans were collected from five different locations per Schottky diode and two diodes from each sample. The values of L_d and S are therefore, an average of ten values for each sample. The experimental linear scan was then fitted using the theoretical curves using L_d and S as the fitting parameters. An indigenously written Maple™ code with Levenberg-Marquardt fitting routine was employed for this purpose. Fig. 2.3 shows

an example of fitting the experimental data with the theoretical profiles developed by Kuiken and van Opdorp [23]. The experimental data was taken at a beam accelerating voltage of 25 kV. The empty circles (o) denote the experimental EBIC profile and the solid line represents the theoretical fit of the data. As can be seen from the data, the theoretical curve fits the experimental data satisfactorily. For this sample, the fitting of experimental data yielded L_d and S as 5.1 mm and 6.7×10^3 cm/s, respectively.

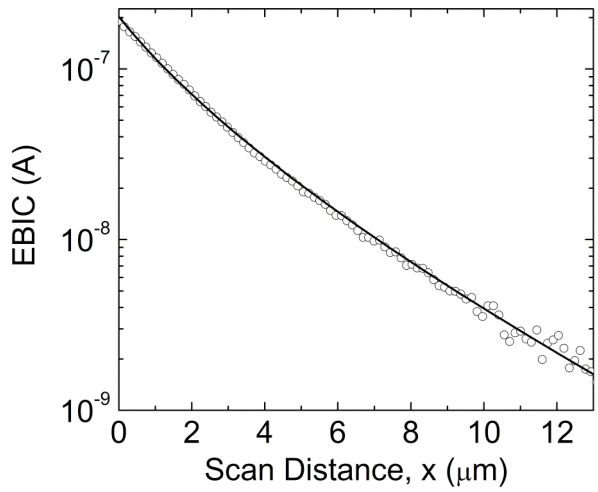


Fig. 2.72 Fitting of theoretical EBIC profile to the experimental data. The open circles (o) denote experimental data points and the solid line represents the theoretical fit.

In order to verify the minority carrier regime, it is instructive to estimate the injection level during the EBIC measurements. The injection level depends on L_d and S, and can be calculated using van Roosbroeck's model [26]. The values of L_d and S evaluated from the linear scan, as described in the previous paragraph, can be substituted in van Roosbroeck's model. The results are shown in Fig. 2.73.

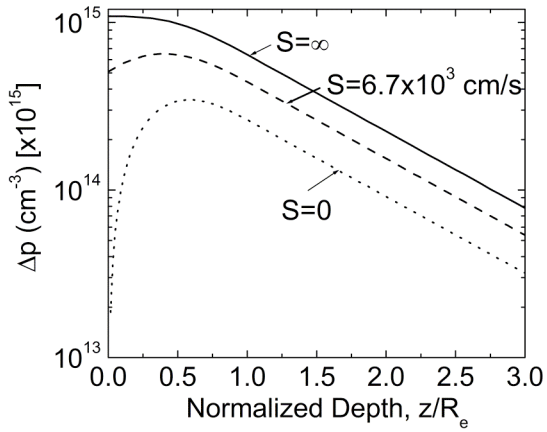
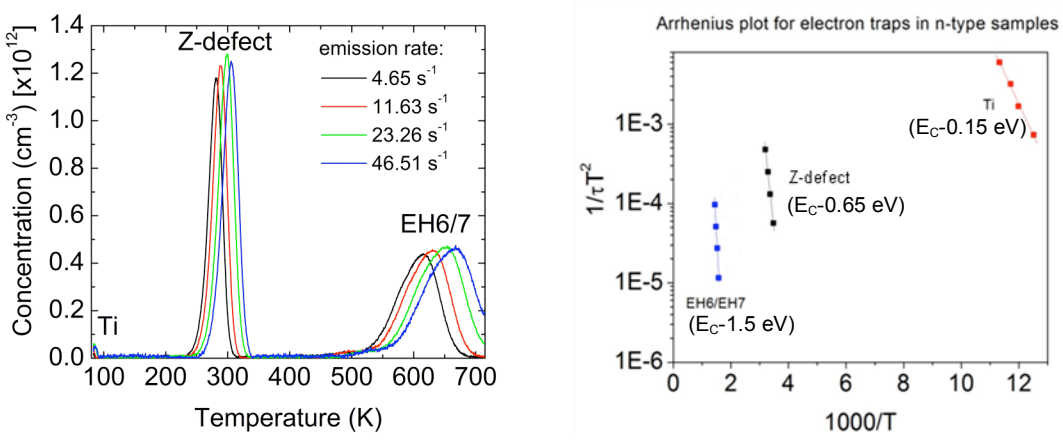


Fig. 2.73 The injection rate is a function of the depth and surface recombination velocity (S).

2.2.1.4 Results and Discussion

2.2.1.4.1 DLTS and MCTS measurements in 4H-SiC epilayers

High quality 4H-SiC epitaxial layers with controlled stoichiometry for this effort were grown at Purdue University using silane-based chemical vapor deposition [20] [6]. Fig. 2.74 shows characteristic DLTS spectrum for Si-face grown 4H-SiC epilayer. Commonly observed electron traps in undoped epitaxial 4H-SiC are Ti (E_C- 0.15 eV) [6], Z-defect (E_C-0.65 eV) [6] [27], and EH6/7 centers (E_C-1.5 eV) [8]. Microscopic identification of Z-defect is still under debate. It has been associated with isolated V_C [28], V_C-V_{Si} divacancies [5], V_{Si} [29] and complex of N impurity with interstitial carbon atom (N+C_i) or silicon vacancy (N+V_{Si}) [4]. Recently it was shown that the Z-defect can be produced in high concentrations after low energy electron irradiation which is just sufficient to displace C atom but not the Si atom in SiC lattice [30]. Based on these arguments Z-defect has been associated with either V_C, C_i, Si_C, or C_{Si}.



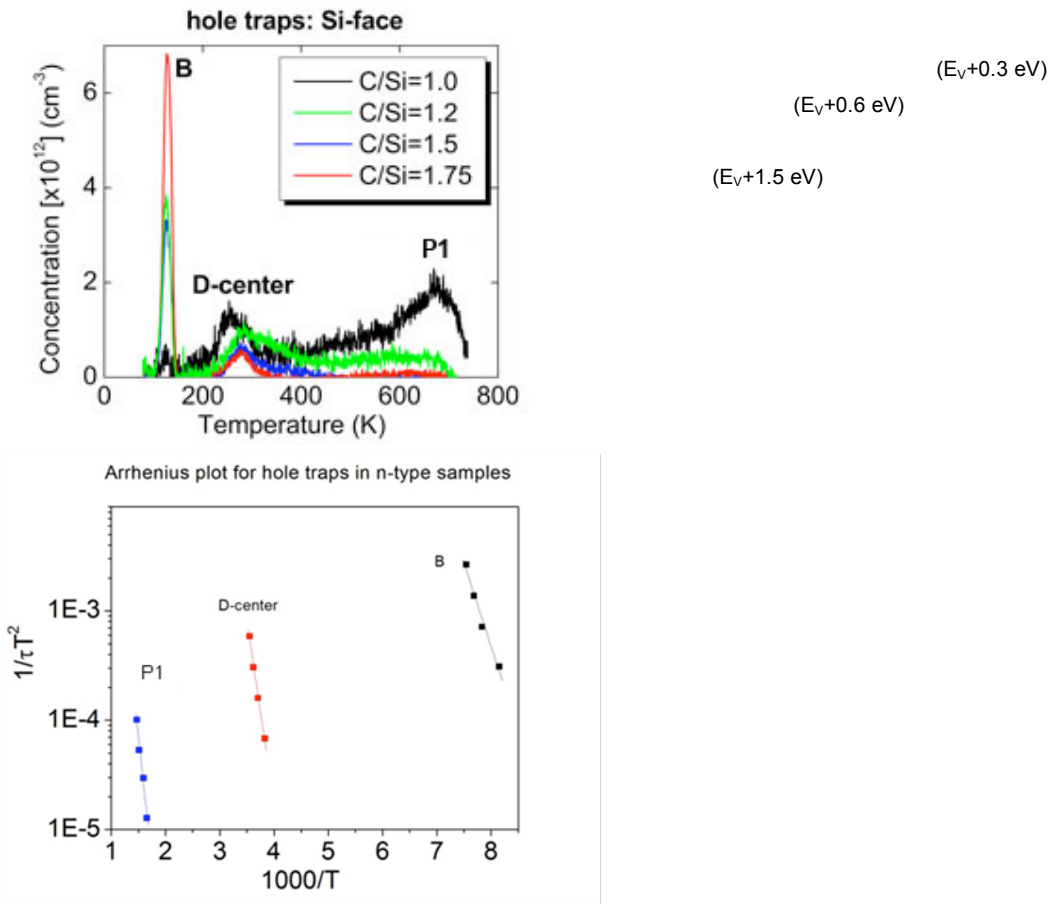
(a) (b)

Fig. 2.74 (a) DLTS spectrum of electron traps in n⁻-4H-SiC epilayers. (b) Arrhenius plot for estimation of apparent activation energies of electron traps.

Only limited data is available for EH6/7 traps partially due to high temperatures (>650 K) required during DLTS measurements in order to observe these traps. EH6/7 has been associated with V_C based on similarity of the activation energy observed in photo-EPR [31].

Hole traps have been observed in n-type layers using Minority Carrier Transient Spectroscopy MCTS using optical injection. Figure 2.75 shows typical MCTS spectrums on n^- 4H-SiC epilayers grown on Si-face with C/Si ratio in 1-1.75 range. As can be observed from the figure, there are three dominant hole traps visible in MCTS spectrum. These are boron shallow-acceptors (E_V+0.3 eV) [6, 20], D-centers (E_V+0.6 eV), and P1 hole traps (E_V+1.5 eV). The D-centers are B-related defects and have been associated with $B_{Si}^-+Si_C^+$ or $B_{Si}^-+V_C^+$ donor-like deep centers [15, 17]. P1 hole traps have been associated with an isolated V_C [32] based on the photo-EPR measurements of V_C (EI-5 center in EPR) state which lie 1.47 eV above the valence band and is donor-like (+/0).

The latter was also speculated as a different charge state of EH6/7 electron trap [32]. Figure 2.75 summarizes the dominant electron and hole traps observed in n^--4H-SiC epilayers and their relative positions in the band-gap.



(a) (b)

Fig. 2.75 (a) MCTS spectrum for n^--4H-SiC grown epilayers on Si-face. MCTS spectrums for four different samples grown with C/Si ration of 1, 1.2, 1.5, and 1.75 have been shown. (b) Arrhenius plot for estimation of apparent activation energies of hole traps.

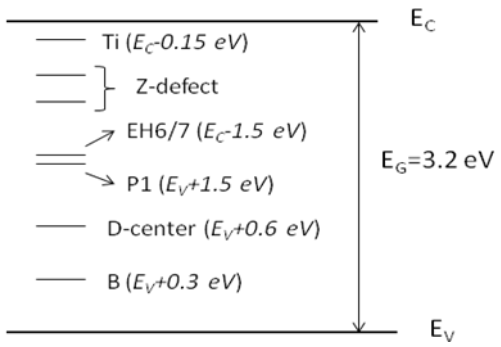
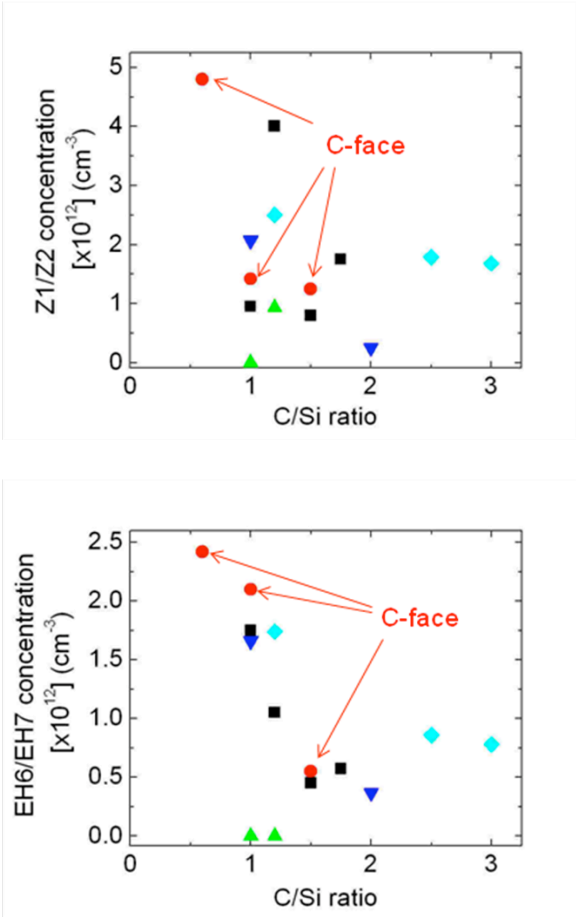


Fig. 2.76 Energy band diagram for 4H-SiC with relative positions of dominant defects in the band-gap.

2.2.1.4.2 Dependence of trap concentration on growth stoichiometry

Figure 2.77 shows the variation of (a) Z-defect and (b) EH6/7 trap concentrations with C/Si ratio for Si-face and C-face grown samples. All the samples were lightly doped n-type with free carrier concentration in 0.5-5x10^{15} cm^{-3} range for Si-face samples, and 1-7x10^{16} cm^{-3} for C-face samples. The free carrier concentration decreases with increase in C/Si ratio for both Si- and C-face samples. This set of samples will be referred as 'growth stoichiometry set'. The general trend in Fig. 2.77 shows that the concentration of Z-defect and EH6/7 decrease with an increase in C/Si. Data points with same symbol represent the samples grown as one batch. The growth conditions change over a period of time due to degradation of the reactor parts such as susceptor, insulations, etc. Therefore, dataset produced under similar set of growth conditions should be best for direct assessment of trends. As can be seen from Fig. 2.77 (a) and 2.77 (b), scatter from run-to-run at nominally the same growth conditions is by up to an order of magnitude. Also, the main electron traps trace each other better then they trace nominal growth conditions. Our results are consistent conclusions that Z-defect and EH6/7 traps are related to Si-rich conditions such as V_C- or Si_C-related traps.

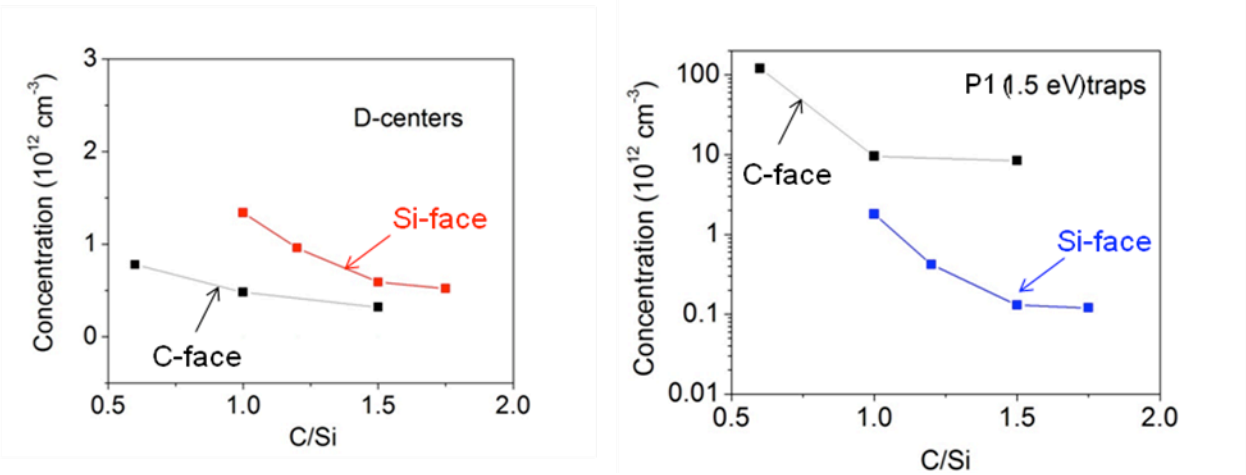


(a) (b)

Fig. 2.77 (a) Z-defect and (b) EH6/7 trap concentration vs. C/Si ratio for Si- and C-face grown samples. Data points with same symbol denote the batch of samples grown in one set of experiments.

Figure 2.78 shows the dependence of (a) D-center and (b) P1 hole trap concentration on C/Si ratio. The data for C-face grown samples is shown with black data points whereas the Si-face grown samples are represented in red and blue data points in left and right figures, respectively. As can be observed from the figure, the concentration of D-centers and P1-hole traps decrease with increase in C/Si ratio for both Si-and C-face grown samples, although, the decrease in concentration for former is not strong. The D-

center concentrations in both the Si- and C-face grown samples are similar (0.5-1.5x10^{12} cm^{-3}). The decrease in D-center concentration with increasing C/Si is contradictory to the site competition model [33] since B is known to incorporate on Si-site as a complex with hydrogen. Therefore, the concentration of D center should increase with C/Si ratio as observed for shallow B. On the other hand, if D-center is related to B_{Si}-V_C or B_{Si}+Si_C complex, there is a trade-off between the B_{Si} and V_C/Si_C concentration as the C/Si varies. This would result in weak dependence of D-center on C/Si ratio.



(a) (b)

Fig. 2.78 (a) D-center and (b) P1 hole trap concentration vs. nominal C/Si ratio. The symbols in black denote data on C-face grown epilayers. Note the vertical scale on right figure is logarithmic.

The vertical scale on the right figure is logarithmic, thus, the P1 hole trap concentration is at least an order of magnitude higher in C-face samples than the corresponding Si-face grown epilayers. The decrease in P1 trap concentration with C/Si ratio is in agreement with Danno *et al*. who have associated P1 traps with isolated V_C [32].

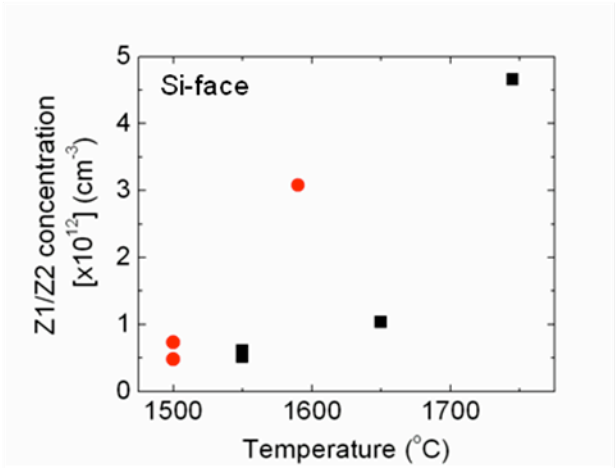
2.2.1.4.3 Dependence of trap concentrations on growth temperature

Table 1 shows the growth conditions for temperature dependent series. The first series (samples 1 through 4) covered a temperature range from 1550 - 1745 ^{o}C. The aim of second series of samples (samples 5 through 7) was to study the effect of epilayer thickness on the type and concentration of defects. Samples #5 and 6 were grown at the same temperature (1500 ^{o}C) under identical conditions but with different epilayer thickness. The epilayer thickness for first series of samples was approximately constant. Figure 2.79 compares (a) Z-defect and (b) EH6/7 trap concentrations as a function of growth temperature on 4H-SiC epilayers. These set of samples (henceforward referred as 'temperature dependent set') were grown on Si-face. The free carrier concentration in these samples varies in $3x10^{14}$ - $1.5x10^{15}$ cm^{-3}, range with a monotonically decreasing trend with increase in growth temperature. As can be observed from Fig. 2.79, the general trend shows an increase in Z-defect and EH6/7 trap concentrations with growth temperature. The concentration of Z-defect increases by an order of magnitude on increasing the growth temperature from 1550 ^{o}C to 1745 ^{o}C. A similar increase in the Z-defect concentration is observed for second series of samples but within a much narrow temperature range (1500 ^{o}C to 1590 ^{o}C). The concentration of EH6/7 traps also increases by ~ order of magnitude with an increase in growth temperature from 1550 ^{o}C to 1745 ^{o}C. The concentration of EH6/7 traps on the two samples grown at 1500 ^{o}C (samples 5 and 6) was below the detection limit. It can be observed from Fig. 2.79 that the thickness of the epilayer does not have any significant impact on the concentration of Z-defect or EH6/7

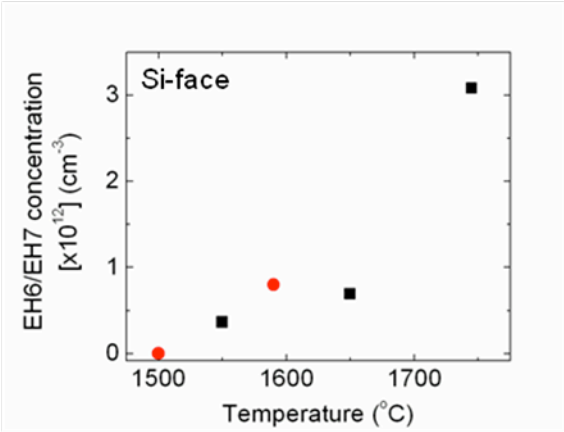
traps. The increase in Z-defect and EH6/7 trap concentration with temperature was also observed by Zhang *et al*. [6]

Table 1. Growth conditions for temperature dependent series of samples.

Sample#	Growth Face	Growth Temp. (^{o}C)	Epilayer Thickness (μm)	Doping (10^{15}cm^{-3})
1	Si	1745/1745	127.04	0.349
2	Si	1745/1650	125.61	0.76
3	Si	1745/1550	115.71	1.2
4	Si	1550/1550	128	1.0
5	Si	1500	54.7	0.105
6	Si	1500	123.6	1.15
7	Si	1590	114.4	0.397



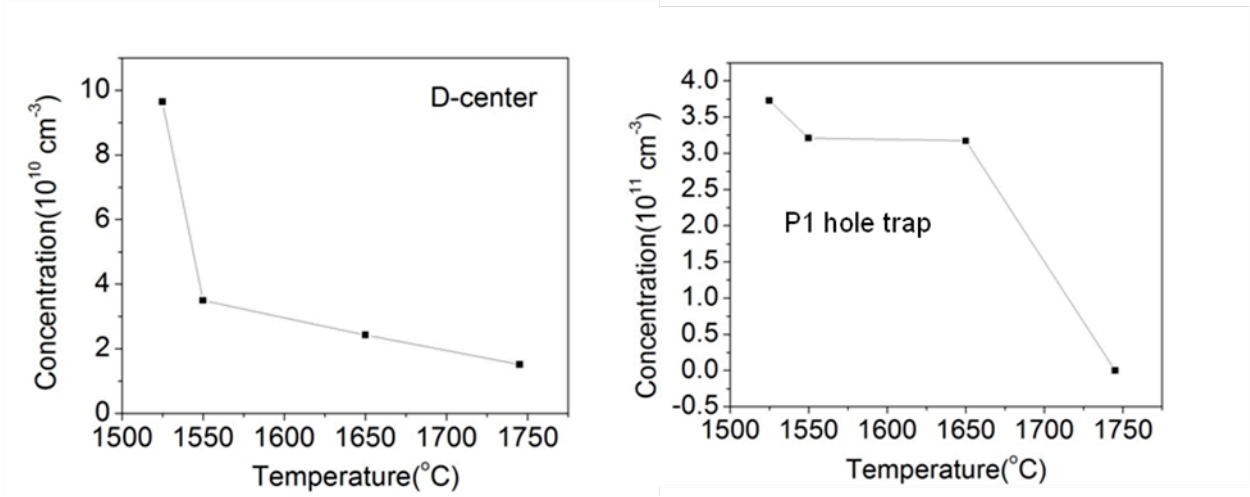
(a)



(b)

Fig. 2.79 (a) Z-defect and (b) EH6/7 trap concentration vs. growth temperature on Si-face grown 4H-SiC epilayers.

The variation in D-center and P1 hole trap concentration with temperature is shown in Fig. 2.80. The data set corresponds to first set of samples (sample # 1 through 4) from the temperature dependent series. Comparison between Fig. 2.79 and 2.80 shows that the concentration of hole traps is at least an order of magnitude lower than the electron traps in the first set of temperature dependent samples. The concentration of both hole traps decreased by a factor of ten with an increase in growth temperature from 1500 ^{o}C to 1745 ^{o}C. This trend is opposite to that observed for electron traps. Zhang *et al*. [6] reported a decrease in shallow B concentration with increase in growth temperature and explained their results based on enhanced desorption rate for B-related species from the growing surface at elevated temperatures. The same reasoning can be applied to the decrease in D-center concentration observed with increase in temperature since D-center is related to boron. The observed decrease in P1 hole traps with growth temperature is not clear at present.



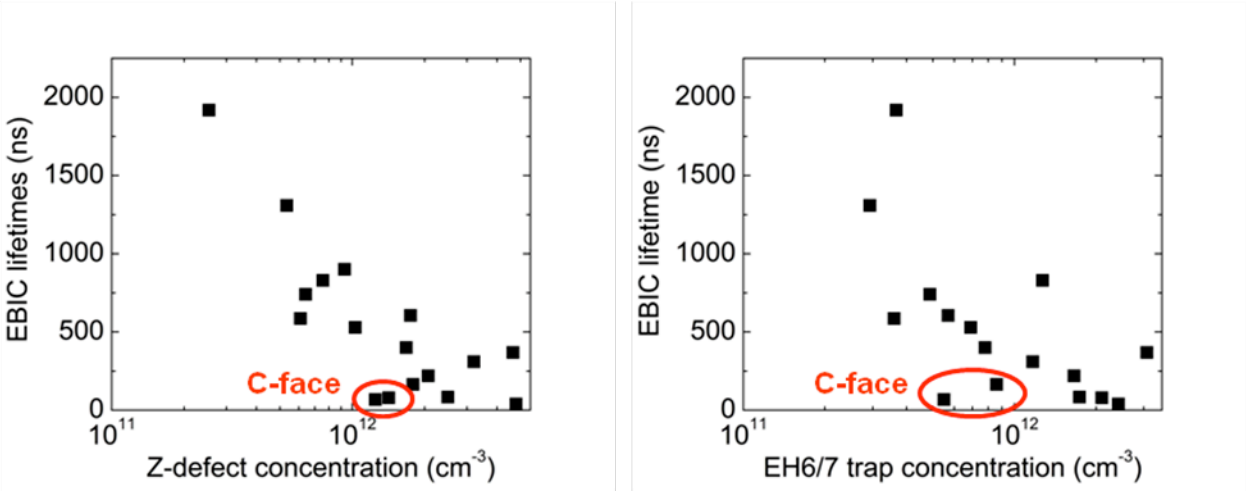
(a) (b)

Fig. 2.80 Variation of (a) D-center and (b) P1 hole traps with growth temperature. The dataset corresponds to first batch of samples (samples 1 through 4) of the temperature dependent series (Table 1).

2.2.1.4.4 Correlation between trap concentration and carrier lifetimes

Diffusion length measurements were done on 'growth stoichiometry series' and 'temperature dependent series' samples in order to examine qualitative correlations between observed traps and carrier lifetimes. Figure 2.81 shows correlation between dominant electron traps (Z-defect and EH6/7 traps) and carrier lifetimes. The general trend denotes anti-correlation between carrier lifetimes and two electron traps with wide scatter. Similar trend in electron traps concentration vs. carrier lifetimes in 4H-SiC epilayers was reported by Zhang *et al*. [6] and Tawara *et al*. [20]. The maximum carrier lifetime measured was ~ 1.9 μs corresponding to Z-defect and EH6/7 trap concentration of 2.5×10^{11} cm^{-3} and 3.67×10^{11} cm^{-3}, respectively. The sample with maximum carrier lifetime was a 40 μm thick Si-face grown epilayer at nominal C/Si ratio of 2.0. The outlier samples in Fig. 2.81 (encircled data points) showed anomalously low carrier lifetimes and corresponded to C-face grown epilayers. It was shown above that the

concentration of P1 hole traps were at least an order of magnitude higher than the corresponding Si-face samples. The P1 hole trap concentration was also significantly higher (approximately an order of magnitude) than the Z-defect and EH6/7 trap concentrations in the C-face grown samples. Therefore, carrier lifetimes in C-face samples could be limited by P1 hole traps. However, this is a purely qualitative estimate and further investigation is needed to prove this hypothesis.



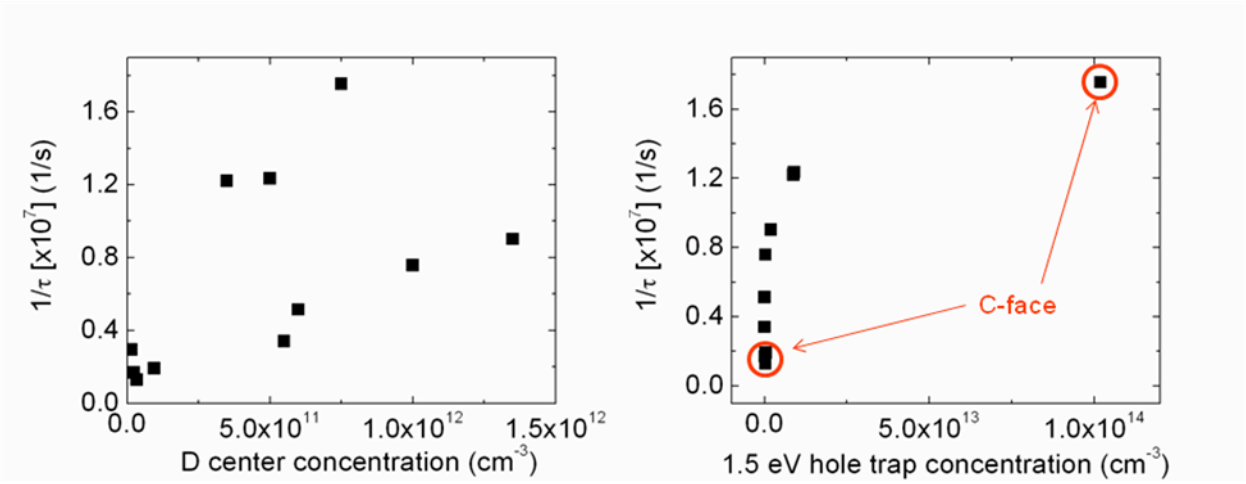
(a) (b)

Fig. 2.81 Correlation between (a) Z-defect and (b) EH6/7 trap concentrations and carrier lifetimes measured by EBIC on 4H-SiC epilayers. The encircled data points correspond to outlier samples grown on C-face and show anomalously low carrier lifetimes.

Figure 2.82 shows correlation between (a) D-center and (b) P1 hole trap (E_V+1.5 eV) concentration and inverse of carrier lifetimes. As can be seen in Fig. 1.3.4.2 (a), there is a large scatter in data points resulting in poor correlation between carrier lifetimes and D-center concentration. The dependence of carrier lifetimes on D-center concentration is in contradiction to that reported by Storasta *et al*. It should be noted that the concentration of D-centers in the samples investigated by Storasta *et al*. was much higher (>10^{13} cm^{-3})

than observed in our case (<1.5x10^{12} cm^{-3}) and at the same time the concentration of Z-defect and EH6/7 concentration were reported in 10^{11} cm^{-3} range. The D-center was shown to have a hole capture cross section of 3x10^{-14} cm^{2} but very low electron capture cross section, therefore, only the low level lifetimes in n-type epilayers should be affected by D-center concentration. The results of Storasta *et al*. are inconclusive by the authors since there was no variation observed in the low and high injection lifetimes in the studies samples.

Similar to the D-center concentration dependence on carrier lifetimes, there was a weak correlation observed between carrier lifetimes and P1 hole traps (Fig. 2.82 (b)), except for the C-face samples (encircled). As mentioned earlier, the P1 hole traps could act as lifetime limiting defects in C-face grown samples. The data on C-face samples is very limited at present to draw a strong conclusion on the role of P1 hole traps as recombination centers. More samples grown on the C-face would be studied in future to ascertain the dependence of carrier lifetimes on P1 hole traps.



(b)

Fig. 2.82 Correlation between (a) D-center and (b) P1 hole trap concentrations and inverse of carrier lifetimes measured by EBIC on 4H-SiC epilayers. The encircled data points correspond to samples grown on C-face.

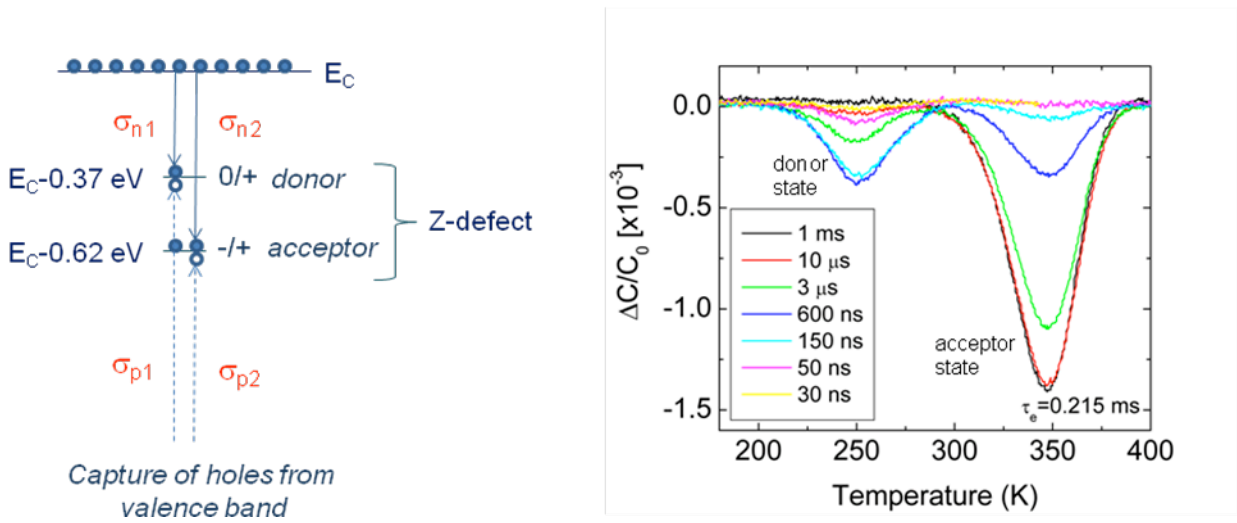
2.2.1.4.5 Capture cross section measurements

Since the concentration of all the dominant electron and hole traps decrease with increase in C/Si and is accompanied with corresponding increase in carrier lifetimes, it is difficult to identify single recombination center that limits the carrier lifetimes based on qualitative correlations presented above. It is also evident from the above discussion that for the Si-face grown samples, only Z-defect and/or EH6/7 traps are of interest as lifetime limiting defects. Therefore, an extensive measurement of capture cross sections of these two traps should be performed in order to provide quantitative estimate of carrier lifetimes using Shockley-Read-Hall (SRH) recombination model. This will also ascertain the role of these defects as recombination centers in the studied samples.

2.2.1.4.6 Z-defect

It was shown by Hemmingsson *et al*. [8] that Z-defect possess a negative-U behavior with the acceptor state (-/+) near E_C-0.62 eV and the donor state (0/+) near E_C-0.37 eV. In other words, an empty Z-center has an attractive (positive) columbic potential for the capture of electron. Capture of second electron to the center results in a net negative charge on the Z-defect and an attractive potential for the capture of holes. Fig. 2.83 (a) shows schematically the capture of free carriers (electrons from the conduction band and holes from the valence band) by Z-defect. As can be seen in this figure, there are four characteristic capture cross sections associated with Z-defect. $\sigma_{n1}(\sigma_{p1})$ and $\sigma_{n2}(\sigma_{p2})$ denotes the capture cross sections for electron (hole) to the donor and acceptor states, respectively. Since the acceptor state with two electrons has lower energy than the donor state with single electron (metastable state), it is difficult to

observe the donor state in regular DLTS experiments. In order to observe the donor state of Z-defect, photo-ionization of the Z-center preceding each filling pulse and using short filling pulses is required so as to avoid capture of two electrons to the center. Fig. 2.83 (b) shows set of DLTS spectrum with different filling pulse widths ranging from 30 ns to 1 ms. A n-type 4H-SiC epilayer with relatively high concentration of Z-defect was selected for these measurements. DLTS spectrums were taken on semi-transparent Ni-Schottky diodes. An optical pulse from 100 mW AlGaN/GaN light emitting diode with above bandgap energy (λ = 365nm) was employed for optically emptying the traps before each filling pulse. As can be seen from the Fig. 2.83 (b), the DLTS peak corresponding to acceptor state decreases and another peak at 245 K emerge as the pulse width is decreased. The peak at 245 K corresponds to emission of single electron from the donor state of Z-defect. The DLTS peak corresponding to emission of two electrons from acceptor state completely vanishes as the filling pulse width is decreased to 100 ns. Since the height of the DLTS peak is proportional to the population of the given state, the decrease in acceptor state peak height with filling pulse width implies kinetic limitation for the capture of second electron to the Z-defect. The peak height for the donor state peak did not decrease for filling pulse width less than 100 ns implying that the decrease in acceptor state peak is due to capture of second electron only. The capture cross section for the capture of second electron to the Z-defect can be estimated using pulse width dependence of acceptor state peak [34]. The donor state peak starts to decline as the filling pulse width was decreased to less than 30 ns. This was due to the kinetic limitation to the capture of first electron to the donor state.



(a) (b)

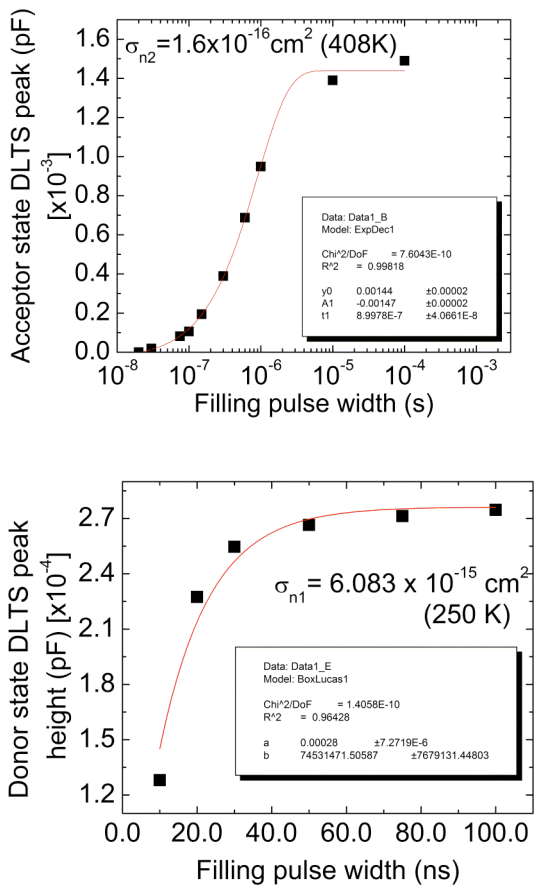
Fig. 2.83 (a) Schematic of electron and hole capture at Z-defect, (b) DLTS spectrum for donor and acceptor state of the Z-defect as a function of filling pulse width. An optical injection from 100 mW AlGaN/GaN light emitting diode (λ~365 nm) was used for optically emptying the centers prior to the filling pulse width.

The variation in DLTS peak height (ΔC_{peak}) as a function of filling pulse width can be expressed as:

$$\Delta C_{peak}(t_p) = \Delta C_{peak}(t_p \rightarrow \infty)[1 - e^{(-\sigma_n n v_{th} t_p)}]$$

where $\Delta C_{peak}(t_p \rightarrow \infty)$ is the peak amplitude when all the traps are saturated with electrons, σ_n is the majority carrier capture cross section, n is the free carrier concentration, and v_{th} is the average thermal velocity of the majority carriers. Figure 2.84 shows the variation of DLTS peak amplitude for (a) acceptor state and (b) donor state, with filling pulse width. The red solid curve denotes the fitting of experimental data points (black squares) according to the equation above. The dataset for acceptor state peak corresponds to DLTS peak temperature 408 K and that for donor state peak to 250 K. Fitting the DLTS peak amplitude data yields electron capture cross sections for

acceptor and donor states as $1.6x10^{-16}$ cm^2 and $6.08x10^{15}$ cm^2, respectively. The capture cross section values determined from pulse width experiments are considered more accurate than from the Arrhenius plot since the former are extracted from capture processes and latter from emission.



(a) (b)

Fig. 2.84 DLTS peak amplitude for (a) acceptor state and (b) donor state as a function of filling pulse width on n-type 4H-SiC epilayer. The fitting of experimental data yields the majority capture cross section for acceptor and donor state as $1.6x10^{-16}$ cm^2 and $6.083x10^{-15}$ cm^2 at respective peak temperatures of 408 K and 250 K.

These capture cross section values are valid for the respective peak temperatures. In order to measure the temperature dependence of the capture cross-section, the method developed by Criado *et al*. [34] was employed. In this method, series of DLTS spectrums at different emission rate windows are measured with filling pulse width such that only a fraction of defect charge state is populated during the filling process. Calculating the difference in DLTS peak amplitude for individual rate windows (different temperature) yields the temperature dependence of capture cross section. The temperature dependence of the capture cross section, σ can be described by:

$$\sigma = \sigma^{\infty} \times \exp(-E_B / kT)$$

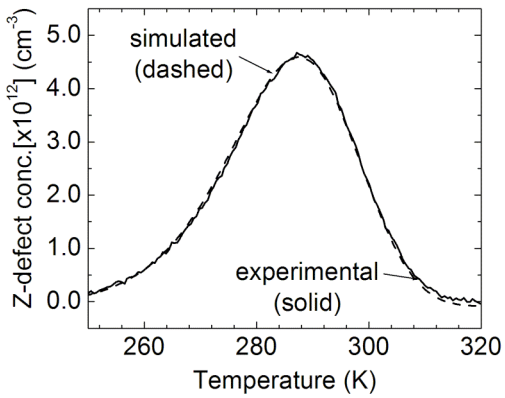
where E_B is the thermal energy barrier for capture process, the pre-exponential factor σ^{∞} is the capture cross section when $T \rightarrow \infty$. The values of pre-exponential factor and energy barrier for the acceptor state and donor state were found to be:

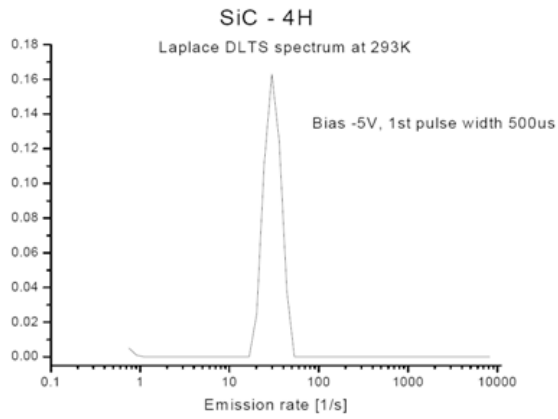
(acceptor state): $\sigma_{n2} = 6.8 \times 10^{-16} \times \exp(-0.0513 / kT)\,\mathrm{cm}^2$

(donor state): $\sigma_{n1} = 6.083 \times 10^{-15} \times \exp(-0.006 / kT)\,\mathrm{cm}^2$

Therefore, the capture of second electron to the acceptor state was found to be thermally activated with activation energy of 51.3 meV. This value of E_B is close to that reported by Weidner *et al*. [35] and Hemmingsson [27] for the acceptor state of Z center. The latter authors reported two overlying acceptor state peaks and two distinct donor state peaks due to negative-U centers, Z1 and Z2 in 4H-SiC epilayers. The two centers (Z1 and Z2) were argued to be associated to a defect occupying the two crystallographically inequivalent lattice sites in 4H-SiC. However, this interpretation has recently come into debate [35]. In the samples used in our studies, we have observed only

single DLTS peaks for the acceptor and donor states. We have confirmed the occurrence of single DLTS peak by fitting the experimental peak with theoretically simulated peak due to single emission transient as shown in Fig. 2.85 (a). The experimental DLTS peak corresponds to the rate emission window of 4.65 s^{-1}. As can be seen from the figure, there is a close agreement between the experimental and the simulated peak implying that the DLTS peak is due to emission from single defect. This was further confirmed by the Laplace DLTS spectrum on the same sample at 293 K. Hemmingsson *et al*. [27] reported a difference in Z1 and Z2 acceptor state activation energies of 0.04 eV. Since the resolution of the Laplace DLTS is orders of magnitude higher than the conventional DLTS, a difference in emission rates for two defects separated by 40 meV should be resolvable in Laplace-DLTS spectrum [36]. However, as can be seen from Fig. 2.85 (b), the Laplace DLTS spectrum shows one single emission rate peak which implies that the emission at 293 K is due to single defect.





(b)

Fig. 2.85 (a) DLTS peak simulation for acceptor state of Z-defect using single emission transient. The solid curve denotes experimental DLTS peak and the dashed curve is for simulated peak. An exact fit of the experimental peak at 293 K with simulated peak implies single trap. (b) Laplace DLTS spectrum for the acceptor state peak of Z-defect at 293 K. The single emission rate peak in Laplace DLTS signifies emission from one single trap at 293 K.

Comparing the capture cross section and its temperature dependence together with activation energy, the Z-defect in our studied samples resemble the Z1 defect reported by Hemmingsson *et al*. [27]. Also, the temperature dependence of capture cross section for acceptor state suggests capture by multiphonon capture process. On the other hand,

negligible thermal barrier for capture of electron by donor state suggest cascade capture process by electron attractive center.

It would have been most straight forward to measure the hole capture cross sections for the acceptor and donor states using p-type samples in a similar way as the electron carrier capture cross sections were measured on n-type samples (pulse width dependence). However, DLTS experiments in p-type samples would require very high temperatures to probe the Z-center since they lie in the upper half of the bandgap and hole capture-emission requires interaction with the valence band. This is also the primary reason for unavailability of hole capture cross sections for Z-defect even after their first detection in irradiated 4H-SiC material, back in 1997 [5]. Therefore, we have followed the approach by Henry *et al.* who measured the capture cross sections of oxygen donor in GaP which also exhibits negative-U behavior. The technique makes use of pn diodes for injection of minority carriers in n^- base. The capture kinetics equations for the population of two levels (acceptor and donor states) were described in terms of electron and hole capture cross section and free carrier concentration of electrons, n, and holes, p (during forward injection). The schematic representation for the population of three charge states of Z-defect coupled by electron and hole capture is shown in Fig. 2.86.

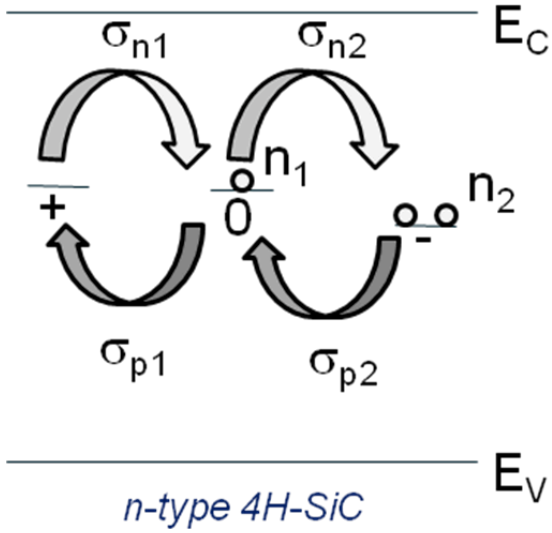


Fig. 2.86 Schematic diagram showing the populations of three charge states of Z-defect coupled by electron and hole capture.

The donor state can exist in two charge states, positive and neutral, when empty or occupied with single electron, respectively. The acceptor state can be neutral or negatively charged when occupied with single or two electrons, respectively. In Fig. 2.86, n_1 and n_2 represent population of filled donor and acceptor states, respectively. The capture rates for electrons and holes can be defined as:

$$c_{ni} = \sigma_{ni} v_{th} n \qquad c_{pi} = \sigma_{pi} v_{th} p \qquad i = 1, 2$$

These equations relate capture rates c_{ni} and c_{pi}, with capture cross sections for electron, σ_{ni}, and holes, σ_{pi}. v_{th} is the thermal velocity. If the rate of thermal emission of electrons and holes from the Z-defect during the filling pulse is assumed much smaller than the rate of capture of free carriers, two coupled equations for densities n_1 and n_2 can be written as:

$$\dot{n}_1 + (c_{n1} + c_{p1} + c_{n2})n_1 + (c_{n1} - c_{p2})n_2 = c_{n1}N$$

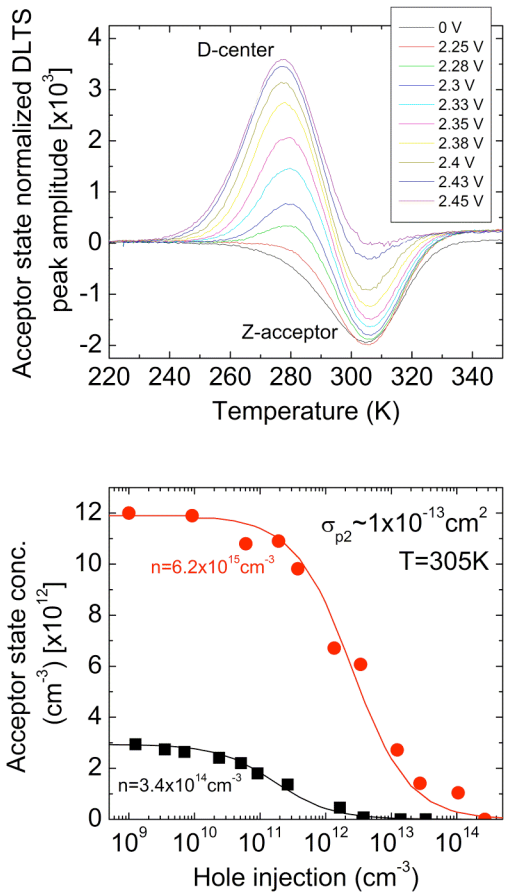
$$-c_{n2}n_1 + \dot{n}_2 + c_{p2}n_2 = 0$$

where, N is the total Z-defect concentration. Instead of performing the transient analysis of the above equations , the experiments can be performed under pseudo-steady state in which case the densities of donor and acceptor state can be expressed as:

$$n_1 = \frac{1}{\left(1 + \frac{\sigma_{p1} p}{\sigma_{n1} n} + \frac{\sigma_{n2} n}{\sigma_{p2} p}\right)} N$$

$$n_2 = \frac{\frac{\sigma_{n2} n}{\sigma_{p2} p}}{\left(1 + \frac{\sigma_{p1} p}{\sigma_{n1} n} + \frac{\sigma_{n2} n}{\sigma_{p2} p}\right)} N$$

σ_{n1} and σ_{n2} are known from experiments performed on Schottky diode with the dependence of majority carrier DLTS peak amplitude on filling pulse width. Here, n_1 and n_2 are proportional to DLTS peak height for donor and acceptor states, respectively. Selecting pn diodes with different values of n^- concentration, and measuring the changes in DLTS peak height for donor and acceptor state peaks as a function of injected minority carrier (p) yields the hole capture cross sections σ_{p1} and σ_{p2}. The variation in acceptor state peak with minority carrier injection is presented in Fig. 2.87.

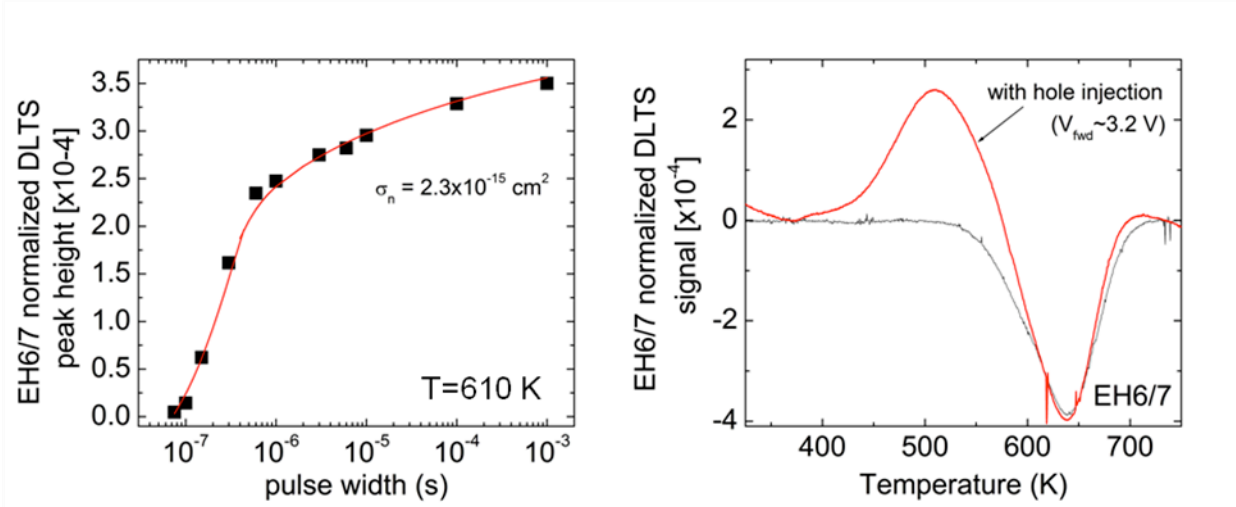


(a) (b)

Fig. 2.87 (a) DLTS spectrum for acceptor state of Z-defect as a function of applied forward bias during the filling pulse. The spectrum also shows the D-center peak which lies close to the Z-defect peak, (b) Variation of acceptor state population as a function of injected hole concentration on samples with background doping concentration of $6.2x10^{15}cm^{-3}$ (filled circles) and $3.4x10^{14}$ cm^{-3} (filled squares). The solid lines represent theoretical fit of the data .

The p^+ doping was $5x10^{18}$ cm^{-3} in the pn diodes studied. The filling pulse width was 100 ms to ensure steady state occupancy of Z-traps. The acceptor state peak amplitude decreases as the applied forward bias is increased during the filling pulse. This is due to capture of injected holes by part of Z-center (acceptor state). As the forward bias is increased, the injected hole concentration increases which results in further decrease of

acceptor state peak height. As can be seen from Fig. 2.87 (a), another peak corresponding to D-center starts to emerge as the hole injection is increased. The D-center peak is a positive peak since it results from emission of minority carriers (holes) in n-type sample. The acceptor state peak completely vanished for applied forward bias of 2.45 V. Fig. 2.87 (b) shows the variation in acceptor state peak as a function of injected hole density. The calculation for trap concentration from DLTS peak height incorporates the so-called 'λ-correction' factor and the term which accounts for the free carrier tail in the space charge region (Debye tail). The I-V characteristics of the pn diode showed that the forward current was dominated by recombination in the space charge region (ideality factor ~ 2). Therefore, the hole injection density was estimated using the Sah-Noyce-Shockley model. There was no appreciable decrease observed in the donor state peak height for forward voltages of 2.84 V which suggests that the upper limit for hole capture cross section, σ_{p1}, is 10^{-18} cm^2. Substituting the maximum value of σ_{p1}, and values of electron capture cross sections for acceptor and donor states estimated from pulse width method on n-type Schottky diodes, yields the hole capture cross section at the acceptor state, σ_{p2} as ~ 10^{-13} cm^2. As can be seen from the Fig. 2.87 (b), the fit of experimental data for the two samples with different background n-type doping is self-consistent i.e. the decrease in DLTS peak height for sample with n-type doping of 6.2 x 10^{15} cm^{-3} occurs at hole injection density of ~10^{11} cm^{-3} which is an order of magnitude higher than for the sample with n-type doping of 3.4 x 10^{14} cm^{-3}. Therefore, now all the four capture cross sections associated with Z-defect are known.



(a) (b)

Fig. 2.88 (a) DLTS peak amplitude as a function of filling pulse width for EH6/7 trap on n-type Schottky diode, (b) DLTS spectrum for EH6/7 trap on p^+n diode with filling pulse bias of 0V (black curve) and 3.2 V (red curve).

The electron capture cross section for EH6/7 can be found in a similar way as described for electron capture cross sections for Z-defect, i.e. by pulse width method. Figure 2.88 (a) shows the dependence of DLTS peak amplitude on filling pulse width in n-type Schottky diode. It can be noticed that there is no clear saturation observed in the DLTS peak amplitude at longer pulse width as was seen for the case of Z-defect (Fig. 2.84). This is because of the longer extension Debye tail of free carriers into the space charge region higher temperature. The Debye length scales as $(T)^{1/2}$, therefore, the contribution from slow capture of carriers in the Debye tail (due to the low concentration of free carriers in the Debye tail) is more significant at higher temperatures. This leads to incomplete filling of traps in the Debye tail during the filling pulse resulting in slow rate of saturation of the DLTS peak height with increasing pulse width. The electron capture cross section for EH6/7 trap was estimated at 2.3 x 10^{-15} cm^2. These are the first known

measurements of electron capture cross section for EH6/7 traps using the pulse width method. The value of electron capture cross section derived from arrhenius plot is ~10^{-13} cm^2 which is similar to those reported in literature [6]. As discussed earlier in reference to electron capture cross section measurements in Z-defect, the value of capture cross section deduced from Arrhenius plot can have significant error.

The measurement of hole capture cross section for EH6/7 trap was performed on a p^+n-diode in a similar way as described for the Z-defect. However, unlike Z-defect there is only one level associated with EH6/7 trap, therefore, rate equation can be rewritten for a single level trap as:

$$\dot{n}_1 = c_{n1}(N - n_1) - c_{p1}n_1$$

where n_1 denotes the population of filled traps, N is the total trap concentration, c_{n1} and c_{p1} are the electron and hole captures rates. As shown in Fig. 2.88 (b), there was no significant change observed in the DLTS peak height of EH6/7 trap for applied forward bias of 3.2 V. However, another peak corresponding to unknown hole trap emerged (positive-going peak) at the low temperature side of the EH6/7 peak on application of forward bias during the DLTS measurement. A forward bias of 3.2 V correspond to flat band conditions (band gap of 4H-SiC ~ 3.2 eV at 300 K), therefore, the hole injection level can be assumed equal to the p^+ doping level ($5x10^{18}$ cm^{-3}) which would yield an upper limit for hole capture cross section of $8.9x10^{-19}$ cm^2.

In order to assess the roles of Z-defect and EH6/7 traps in limiting the carrier lifetimes on Si-face grown 4H-SiC, lifetimes were calculated based on the Shockley-Read-Hall (SRH) recombination model using the capture cross sections for respective centers. In the event of parallel recombination channels present, the carrier lifetimes are

limited by the trap resulting in shortest lifetimes. For example, considering recombination through Z-defect and EH6/7 traps to occur in parallel, the trap resulting in shorter lifetime would effectively act as lifetime limiting defect in the material. The carrier lifetime according to the SRH recombination model can be expressed as:

$$\tau = \tau_p \frac{n_0 + n'_1 + \Delta n}{n_0 + p_0 + \Delta n} + \tau_n \frac{p_0 + p'_1 + \Delta p}{n_0 + p_0 + \Delta n}$$

$$\tau_p = \frac{1}{\sigma_p v_{th} N_T} \qquad \tau_n = \frac{1}{\sigma_n v_{th} N_T}$$

$$n'_1 = n_i \exp(\frac{(E_T - E_i)}{kT}) \qquad p'_1 = n_i \exp(\frac{-(E_T - E_i)}{kT})$$

where n_0 and p_0 are equilibrium electron and hole concentrations, respectively, $\Delta n = n - n_0$ and $\Delta p = p - p_0$ are excess carrier densities ($\Delta n = \Delta p$, assuming negligible trapping); σ_n and σ_p are electron and hole capture cross-sections for the lifetime limiting defect; and N_T is the concentration of lifetime limiting defect.

However, in most of the cases one can simplify equation (1) by making certain assumptions:

(i) for the n-type samples $n_0 >> p_0$,

(ii) in the minority carrier regime, $\Delta n < n_0$.

(iii) for traps lying in the upper half of the band gap, i.e. $E_T > E_i$, $n'_1 > n_i > p_1$

Under the above mentioned assumptions, the minority carrier lifetime can be written as

$$\tau = \tau_p (1 + \frac{n'_1}{n_0}) = \tau_p (1 + \exp\frac{(E_T - E_F)}{kT})$$

If $E_T - E_F >> kT$, then equation (4) can be simplified to:

$$\tau = \tau_p = \frac{1}{\sigma_p v_{th} N_T}$$

Diffusion lengths were experimentally measured using electron beam induced current (EBIC) technique. Diffusion length can be converted to lifetime using the relation $L_d=\sqrt{D\tau}$ where L_d is the diffusion length, D is the diffusion coefficient of minority carrier and τ is the minority carrier lifet. Assuming that the Z-defect controls the carrier lifetimes in the studied samples, theoretical estimates for carrier lifetime can be made using the above equation and hole capture cross section of 10^{13} cm^2. The thermal velocity can be assumed as 10^7 cm/s and N_T is the Z-defect concentration. Comparison of theoretically estimated lifetimes and experimental lifetimes measured from EBIC are compared in Fig. 2.88. The dashed line denotes perfect correlation between theoretical and experimental lifetimes. The error in theoretically estimating the carrier lifetimes stems from variation in the trap concentration measured from DLTS that can vary by a factor of two over the sample. Close correlation between the experimental and theoretical lifetimes calculated for Z-defect proves these defects as lifetime killer defects in Si-face grown 4H-SiC epilayers.

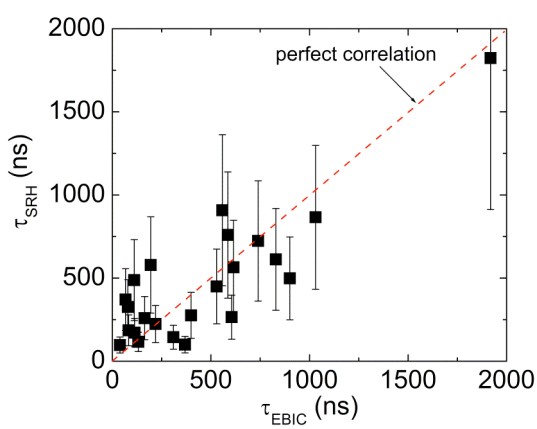


Fig. 2.89 Comparison of theoretically calculated (from SRH model) and experimentally observed carrier minority carrier lifetimes for Z-defect. In theoretical calculation, a hole capture cross section of 10^{-13} cm^2 was used for Z-defect. The diffusion length values measured from EBIC were converted to lifetimes using the relation $L_d=\sqrt{Dt}$.

Similar analysis for EH6/7 traps gives theoretical lifetime values three to four orders of magnitude higher than experimental lifetimes suggesting that EH6/7 traps do not act as lifetime limiting defects in the studied samples. This represents the conclusive proof that the carrier lifetimes in our set of samples were controlled by Z1/Z2 defect and that all capture cross ections (and the model itself) are correctly determined.

2.2.2. Observation of 3*C*-SiC inclusion nucleation in 4*H*-SiC epilayers

One of the unusual characteristics of silicon carbide is polytypism i.e. existence of multiple different stacking sequences of closely packed layers [37]. The hexagonal polytypes are stable at high temperatures typical of bulk crystal growth temperatures. On the other hand, the cubic form of SiC appears to be stable at temperatures typically employed for epitaxy. He experimental manifestation of this is the fact that 2D nucleation at temperatures below 1800 ^{o}C invariably results in deposition of the 3C polytype. This, in turn, typically leads to deposition of mixed polytypes during epi growth, polytype boundaries, and double positioning boundaries. Such defects are well known to cause premature breakdown in pin diodes and Schottky barriers. The approach used to avoid formation of such defects relies on 'step-controlled epitaxy' technique [38]. The epilayers are grown on off cut the surface of substrates that are intentionally misoriented from (0001) creating high density of atomic steps along the off-cut direction. The layer grows by the motion of steps while avoiding the 2D nucleation. It is quite

obvious that any defect on the substrate surface that impedes the step flow can lead to a formation of a wide terrace and nucleation of cubic polytype inclusions. One example of such defects are triangular defects observed frequently on the surface of 4*H*-SiC epilayers grown on 3.5° off-cut substrates. The defects can be either depression or hillocks on the epilayer surface with a triangular shape. Their structures were determined to include twinned 3*C* crystals [39] [40] [41].

Two mechanisms have been mechanisms proposed to explain the formation of 3*C* polytype during the step-controlled epitaxy of hexagonal SiC [41] [39]. One argued that 3*C* is formed due to 2D nucleation on the terraces between surface steps. Any conditions that make it difficult for adatoms to diffuse to the step edges would promote 3*C* formation. Based on this argument, one way to suppress the 2D nucleation of 3*C* polytype is to reduce the width of the terraces. Growth experiments have proved that by increasing the off-cut angle from 3.5° to 8°, the triangular defects can be largely eliminated from the 4*H*-SiC epilayers [39]. The second mechanism related the nucleation of 3*C* polytype to substrate imperfections, such as dislocations, polishing scratches, and surface contamination. Although no consensus has been reached on the correlation between triangular defects and dislocations in the substrates, triangular defects decorated along the intended polishing scratches were observed [41]. Instead of the step edges, adatoms can be incorporated by the dangling bonds along the scratches to form 3*C* nuclei.

In he course of this project, another form of 3*C* inclusions was observed and documented in 4*H*-SiC epilayers grown on Si face with 8° off-cut by silane-based CVD. They produced surface features that have an arrow-like morphology. The defect structure was characterized by optical microscopy, molten KOH etching and transmission electron

microscopy (TEM) and its characteristics and origin are described below.

2.2.2.1 Experiment

The samples examined in this study were grown by a silane-based CVD method on Si face of 4*H*-SiC *n*-type conducting substrates (n=8×10^{18} cm^{-3}). The substrates were off cut by 8° from [0001] towards [11-20] direction. The off-cut direction defined here is opposite to the step-flow direction. The epilayers were doped with nitrogen in the 10^{14}-10^{15} cm^{-3} range and the thickness of 22-108 μm.

The morphology of the surface features was monitored using a Nikon ME600L optical microscope fitted with Nomarski differential interference contrast optics. The defects in the volume of the epilayer were observed in a cross-section view. The cross-section samples were cut from the selected areas of the epi-wafers with each containing at least one defect of interest. The length of the samples was about 5 mm along the direction of the off-cut. The two side faces of the samples were lapped down with boron carbide abrasives to reach a width in the range of 350-500 μm. Both faces were then polished with 1 μm diamond paste so that the defects inside the samples can be clearly observed by optical microscope. Complementary data were obtained by molten KOH etching at 500°C for 5-10 minutes.

Both plan-view and cross-section TEM were applied to study the microstructures of the defects. The TEM samples were cut from the selected areas of the epi-wafers that contain the defects of interest. They were lapped down to a thickness of about 100 μm followed by dimpling to a thickness of about 20 μm. In the final step, the electron transparency was obtained by sputtering the samples with argon ion beams in a Gatan

Precision Ion Polishing System. The TEM observations were carried out on a JEOL 4000 EX-TEM, operated at 200 kV.

2.2.2.2 Results and discussion

Fig. 2.90 shows the optical micrographs of the features of interest on 4*H*-SiC epilayer surface. Fig. 2.90 (a) and (c) were taken in reflection while images in Fig. 2.90 (b) and (d) were taken under transmission light at the same regions as (a) and (c), respectively. The images show defects with an arrow-like morphology. The long axes of the arrows are along the step-flow direction with the arrowheads pointing towards the down-step direction. The two examples shown in Fig. 2.90 (a) are from an epilayer with a thickness of 108 μm. The one shown in Fig. 2.90 (c) is from an epilayer with a thickness of 44 μm. By using atomic force microscopy (AFM), the region around the axes of the arrows was determined to be depression on the epilayer surface. For the two arrows in Fig. 2.90 (a), close to their arrowheads the surface corrugates in waves. It is easy to notice that the arrow feature on the right has more pronounced morphology than the one on the left. In addition, it has a dark contrast at its tail. The dark contrast was produced by a deep polygon-shaped depression on the epilayer surface. No such depression hole was detected at the tail of the other arrow feature in Fig. 2.90 (a). However under transmission light, both arrows were detected to be exhibit dark contrasts at their tails, as shown in Fig. 2.90 (b). The triangle marked the dark spot at the tail of the smaller arrow feature. It should also be noted that for the larger arrow feature, the dark contrast at its tail under transmission light does not have as clear-cut boundaries as in Fig. 2.90 (a). Fig. 2.90 (b) was focused around the epilayer/substrate interface, indicating that the dark spot for the

smaller arrow feature and the difference in the dark contrast at the tail of the larger one occurred close to the interface. Such observations imply that the cause for the arrow-like surface features comes from defects located under the epilayer surface.

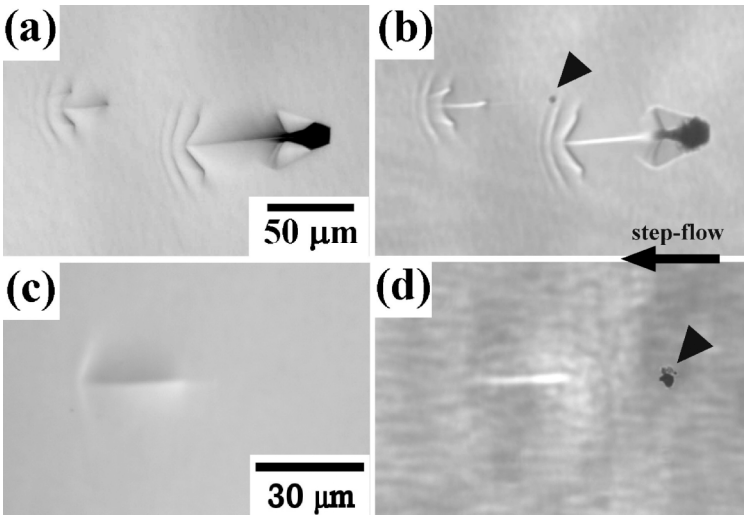


Fig. 2.90 Optical micrographs showing the morphologies of arrow-like features on 4H-SiC epilayer surface. (a) and (c) are under reflection light; (b) and (d) are under transmission light taken from the same regions as (a) and (c), respectively.

The morphology of the arrow feature could vary slightly with different growth conditions, as the one shown in Fig. 2.90 (c) from a different epilayer. Using transmitted light, similar dark contrast was revealed at its up-step side, as marked with a triangle in Fig. 2.90 (d). The dark spot was in focus at the position close to the epilayer/substrate interface. The observations described above imply that the arrow features on the 4H-SiC epilayer surface could be produced by defects nucleated close to the interface. They disturb the advancing steps during growth and induce the surface corrugation along the step-flow direction. It has to be pointed out that for some arrow features that are much smaller and shallower than those shown in Fig. 2.90, no dark contrasts were identified at their tails close to the interface by transmission light. Two possibilities exist: either there

is no corresponding defect located at the interface, or the size of the defect is too small for the optical microscopy to resolve.

Cross-sectional samples were made for optical microscopy observation of the defect structures underneath the arrow features. Fig. 2.91 shows the micrograph obtained from one of such defects [41]. The sample was from the same epilayer as the one in Fig. 2.90 (a). The arrow feature in this sample was very similar to the one on the right shown in Fig. 2.90 (a), which also had a depression at its tail. The side face of the sample is (-1100) and the step-flow direction is from right to the left. Different nitrogen doping concentrations in the epilayer and the substrate produced different colors under optical microscope, which clearly indicate the position of the interface. The heavily doped substrate had a darker color as compared with the lightly doped epilayer. The positions of the interface and the epilayer surface are labeled in Fig. 2.91. The defect underneath the surface arrow feature is clearly visible. It appears to be an inclusion with an ellipsoidal shape extending from the interface to the middle of the epilayer thickness. On top of the inclusion was a tubular void that reached the epilayer surface and produced the depression at the tail of the arrow. Interestingly, dark contrast appeared close to the interface, as compared with the lighter contrast from the other part of the inclusion. As mentioned in the description of Fig. 2.90 (b) and (d), the dark contrasts at the tails of the arrow features were observed to come into focus close to interface. Based on what have been observed in cross-sectional micrographs, they should correspond to the dark contrasts underneath the inclusions. Such a defect structure with essentially three components including the hollow pipe, the ellipsoidal inclusion, and the dark contrast underneath the inclusion, has been observed repeatedly for multiple arrow features from

different epilayers. The size of the inclusion varies for arrow features in different epilayers. It is not uniform even in one epilayer. Obviously, the one that produced the arrow feature on the left in Fig. 2.90 (a) was smaller than that for the arrow feature on the right. In addition, the hollow pipes above the inclusions in some cases closed of. This occurs more readily for small size of the dark feature and inclusion

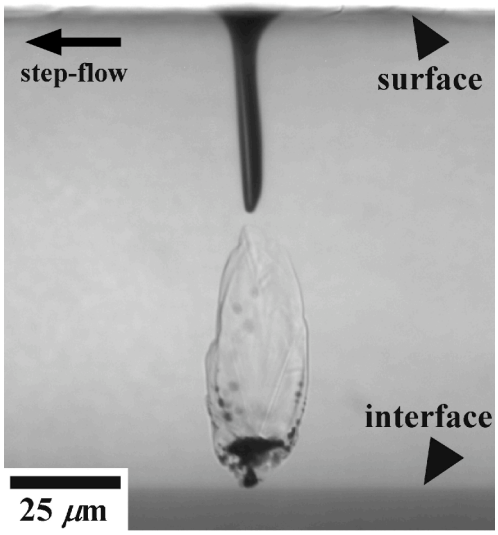


Fig. 2.91 Optical micrograph of the defect in a cross-section view.

The observed defect structure suggests that it nucleated during the epitaxial growth. The inclusion located close to the interface disturbs the step flow and induces the arrow-like surface corrugation. In order to determine the microstructures of the inclusions and their nucleation sites, the side faces of cross-sectional samples were lapped down in order to intersect the inclusions. Fig. 2.92 (a) shows one defect before exposed on the side face of the sample. The image was produced in transmitted light. The position of the interface is labeled with a triangle. The three components of the defect are clearly visible. The part of the defect underneath the inclusion got exposed on the side surface of the

sample, as shown in Fig. 2.92 (b). The inset shows the magnified image of the region obtained by secondary electron microscopy (SEM). This part of the defect appears to be a void. Considering that the refractive index of SiC is about 2.5, incident light from SiC can be easily totally refracted at the SiC/air interface. This explains the dark contrasts produced by both the voids underneath the inclusions and the hollow pipes on top of them in the transmission optical micrographs. The image of the same inclusion after etching in molten KOH for 5 minutes is shown in Fig. 2.92 (c). The etched lines on the cross section of the inclusion indicate that it has a polycrystalline structure.

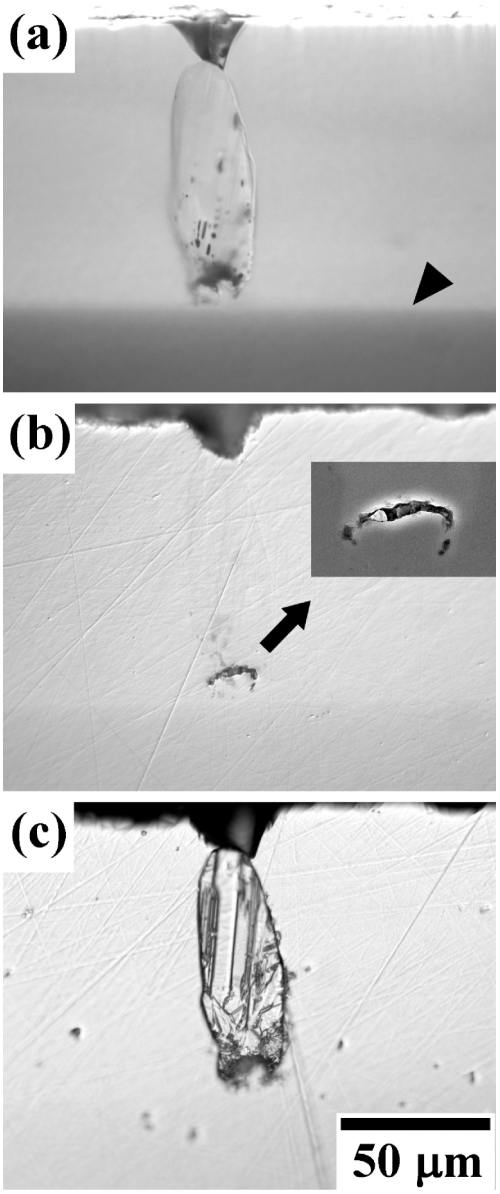


Fig. 2.92 (a) Optical micrograph of an inclusion in a cross-section view; (b) The same defect after it was exposed on the side surface by mechanical polishing. The inset shows a magnified image by SEM at the position underneath the inclusion; (c) The etch pattern of the defect.

The microstructure of the inclusion was examined by transmission electron microscopy (TEM) in both plan-view and cross-section geometry. The plan-view samples were made first by lapping down both the epilayer and the substrate thicknesses until the

inclusions were reached. The cross-sectional samples were made with the surface facing the electron beam perpendicular to the off-cut direction of [11-20]. Fig. 2.93 (a) shows the cross-section bright field image taken at the boundary between the inclusion and the 4H-SiC epilayer. The inclusion was in one zone axis orientation. The boundary could be clearly seen and shows fringe contrast. The upper bright region was identified as 4H-SiC and its (11-20) zone axis diffraction pattern (Fig. 2.93 (b)) was acquired by tilting the sample. Similarly, the zone axis shown in Fig. 2.93 (c) was acquired for the inclusion. It was identified to be one from the {110} group, which are characteristic of the cubic polytype of SiC. Thus the inclusion has been determined to be 3C-SiC. The polycrystalline nature of the inclusion has been determined by KOH etching, as shown in Fig. 2.92 (c). It was also supported by the TEM observation. Fig. 2.93 (d) shows the bright field image of 4H-SiC and two grains of the 3C-SiC inclusion (I and II), which had distinct contrasts under the same imaging condition. In addition, even inside one grain the 3C-SiC crystal was highly defected, as can be seen from the multiple defect contrasts inside grain I.

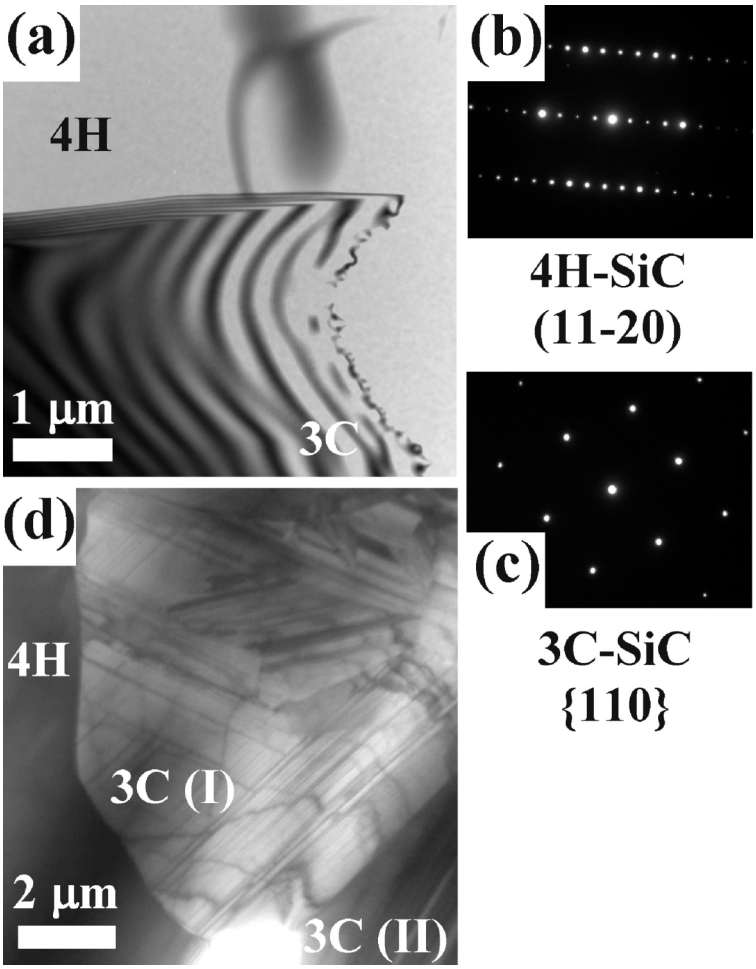


Fig. 2.93 (a) Cross-section bright field TEM image showing the boundary between 4H-SiC and the inclusion. The inclusion is on zone axis; (b) (11-20) zone axis diffraction pattern obtained from 4H-SiC; (c) {110} zone axis diffraction pattern obtained from the 3C inclusion; (d) Plan-view bright field TEM image showing the 4H-SiC and two grains of the 3C inclusion.

The conclusion of the above analysis is that the inclusions at the epilayer/substrate interface consisted of polycrystalline 3C-SiC and nucleated during the early stage of the epitaxial growth.

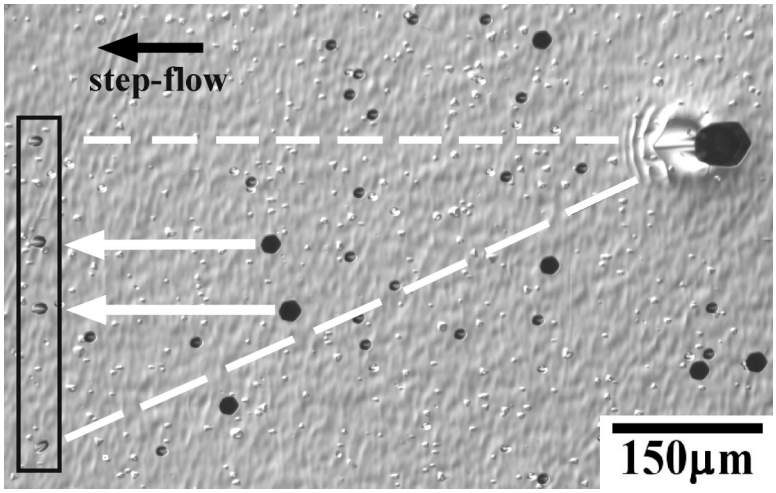


Fig. 2.94 Etch pattern of the in-grown stacking fault associated with an arrow defect.

One of the frequent characteristic features of 3C inclusions 3C inclusions is that some of them were associated with in-grown stacking faults. One example is shown in Fig. 2.94. The epilayer was etched by molten KOH. Etch pits produced by threading screw dislocations, threading edge dislocations, and basal plane dislocations (BPD) were observed in the micrograph. One arrow defect was at the right side of the figure. To its down-step direction, an array of oval shape BPD etch pits was enclosed in a rectangle. The distance between the array and the arrow defect corresponded well to the projection length on the epilayer surface of a BPD defect nucleated at the interface and propagating to the surface. Upon close inspection, the axis of the BPD etch pit at the bottom end of the array was tilted off the step-flow direction. Thus the arrow defect and the two BPD etch pits at the ends of the array formed the three apexes of a right angle triangle. For each of the two etch pits in the middle of the array, a threading screw dislocation can be found to its up-step direction inside the triangle, as labeled by two white arrows in Fig. 2.94. Such an etch pattern is characteristic of in-grown stacking fault that has been

detected in 4H-SiC epilayers. The two BPD etch pits in the middle correspond to two partial dislocations which were formed due to the intersection of threading screw dislocations with the in-grown stacking faults. Surprisingly, both the 3C inclusions that can extend to 100 μm and the in-grown stacking faults that are only of several Si-C bilayers thickness could nucleate at the same site at the interface.

References Cited in Section 2.2

[1] N. Achtziger and W. Witthuhn, "Band-gap states of Ti, V, Cr in 4H-SiC: Identification and characterization by elemental transmutation of radioactive isotopes," *Phys. Rev. B,* vol. 57, pp. 12181-12196, 1998.

[2] P. Kackell, B. Wenzein, and F. Brechstedt, *Phys. Rev. B,* vol. 50, p. 10761, 1994.

[3] T. Kimoto, S. Nakazawa, K. Hashimoto, and H. Matsunami, "Reduction od doping and trap concentrations in 4H-SiC epitaxial layers grown by chemical vapor deposition," *Appl. Phys. Lett.,* vol. 79, pp. 2761-2763, 2001.

[4] I. Pintilie, L. Pintilie, K. Irmscherb, and B. Thomas, "Formation of the Z1,2 deep-level defects in 4H-SiC epitaxial layers: Evidence for nitrogen participation," *Appl. Phys. Lett.,* vol. 81, p. 4841, 2002.

[5] T. Dalibor, G. Pensl, H. Matsunami, T. Kimoto, W. J. Choyke, A. Schoner, and N. Nordell, "Deep defect centers in silicon carbide monitored with Deep Level transient Spectroscopy," *phys. stat. solidi (a),* vol. 162, 1997.

[6] J. Zhang, L. Storasta, J. P. Bergman, N. T. Son, and E. Janzen, "Electrically active defects in n-type 4H-silicon carbide grown in a vertical hot-wall reactor," *J. Appl. Phys.,* vol. 93, pp. 4708-4714, APR 15 2003.

[7] K. Fujihira, T. Kimoto, and H. Matsunami, "High-purity and high-quality 4H-SiC grown at high speed by chimney-type vertical hot-wall chemical vapor deposition," *Applied Physics Letters,* vol. 80, pp. 1586-1588, MAR 4 2002.

[8] C. Hemmingsson, N. T. Son, O. Kordina, J. P. Bergman, E. Janzen, J. L. Lindstrom, S. Savage, and N. Nordell, "Deep level defects in electron-irradiated 4H SiC epitaxial layers," *Journal of Applied Physics,* vol. 81, pp. 6155-6159, MAY 1 1997.

[9] L. Torpo, M. Marlo, T. E. M. Staab, and R. M. Nieminen, "Comprehensive ab initio study of properties of monovacancies and antisites in 4H-SiC," *Journal of Physics-Condensed Matter,* vol. 13, pp. 6203-6231, JUL 16 2001.

[10] L. Storasta, F. H. C. Carlsson, S. G. Sridhara, J. P. Bergman, A. Henry, T. Egilsson, A. Hallen, and E. Janzen, "Pseudodonor nature of the D-I defect in 4H-SiC," *Applied Physics Letters,* vol. 78, pp. 46-48, JAN 1 2001.

[11] W. Suttrop, G. Pensl, and P. Lanig, "Boron-related deep centers in 6H-SiC," *Appl. Phys. A,* vol. 51, pp. 231-237, 1990.

[12] A. Evwaraye, S. R. Smith, W. C. Mitchel, and H. M. Hobgood, "Boron acceptor levels in 6H-SiC bulk samples," *Appl. Phys. Lett.,* vol. 71, pp. 1186-1188, 1997.

[13] D. J. Larkin, S. G. Sridhara, D. R. P., and C. W. J., "Hydrogen incorporation in boron-doped 6H-SiC CVD epilayers produced using site-competition epitaxy," *J. Electron. Materials,* vol. 24, p. 289, 1995.

[14] A. Kakanakova-Georgieva, R. Yakimova, M. K. Linnarsson, and E. Janzen, "Site-occupying behavior of boron in compensated p-type 4H–SiC grown by sublimation epitaxy," *J. Appl. Phys.,* vol. 91, p. 3471, 2002.

[15] B. Aradi, A. Gali, P. Deak, E. Rauls, T. Frauenheim, and N. T. Son, "Boron centers in 4H-SiC," *Mat. Sci. Forum,* vol. 353-356, pp. 455-458, 2001.

[16] H. Itoh, T. Troffer, and G. Pensl, "Coimplantation effects on the electrical properties of boron and aluminum acceptors in 4H-SiC," *Silicon Carbide, Iii-Nitrides and Related Materials, Pts 1 and 2,* vol. 264-2, pp. 685-688, 1998.

[17] R. Muller, M. Feege, S. Gruelich-Weber, and J.-M. Spaeth, *Semicond. Sci. Technol.,* vol. 8, p. 1377, 1993.

[18] P. G. Baranov and N. G. Romanov, "Acceptors in silicon carbide: ODMR data," *Materials Science Forum,* vol. 83-87, pp. 1207-1212, 1992.

[19] P. Deak, B. Aradi, and A. Gali, "Boron and aluminium doping in SiC and its passivation by hydrogen," *Journal of Physics-Condensed Matter,* vol. 13, pp. 9019-9026, Oct 8 2001.

[20] T. Tawara, H. Tsuchida, S. Izumi, I. Kamata, and K. Izumi, "Evaluation of free carrier lifetime and deep levels of the thick 4H-SiC epilayers," *Mater. Sci. Forum,* vol. 457-460, pp. 565-568, 2004.

[21] A. Y. Polyakov, Q. Li, S. W. Huh, M. Skowronski, O. Lopatiuk, L. Chernyak, and E. Sanchez, "Minority carrier diffusion length measurements in 6H-SiC," *Journal of Applied Physics,* vol. 97, p. 053703, Mar 1 2005.

[22] K. Danno and e. al., *Appl.Phys. Lett.,* vol. 90, p. 202109, 2007.

[23] H. K. Kuiken and C. v. Opdorp, "Evaluatin of diffusion length and srface recombination velocity from a planar collector geometry electron beam induced curent scan," *J. Appl.Phys.,* vol. 57, pp. 2077-2090, 1985.

[24] F. Berz and H. K. Kuiken, "Theory of life time measurements with the scannig electron microscope: steady state," *Solid-State Electron.,* vol. 19, pp. 437-445, 1976.

[25] H. J. Leamy, "Charge collection scanning electron microscopy," *J. Appl. Phys.,* vol. 53, pp. R51-R80, 1982.

[26] W. Van Roosbroeck, "Injected Current Carrier Transport in a Semi-Infinite Semiconductor and the Determination of Lifetimes and Surface Recombination Velocities," *Journal of Applied Physics,* vol. 26, pp. 380-391, 1955.

[27] C. G. Hemmingsson, N. T. Son, A. Ellison, J. Zhang, and E. Janzen, "Negative-U centers in 4H silicon carbide," *Physical Review B,* vol. 58, pp. 10119-10122, Oct 15 1998.

[28] T. Kimoto, S. Nakazawa, K. Hashimoto, and H. Matsunami, "Reduction of doping and trap concentrations in 4H-SiC epitaxial layers grown by chemical vapor deposition," *Applied Physics Letters,* vol. 79, pp. 2761-2763, OCT 22 2001.

[29] A. Kawasuso, F. Redmann, R. Krause-Rehberg, T. Frank, M. Weidner, G. Pensl, P. Sperr, and H. Itoh, "Vacancies and deep levels in electron-irradiated 6 HSiC

epilayers studied by positron annihilation and deep level transient spectroscopy," *Appl. Phys. Lett.,* vol. 90, p. 3377, 2001.

[30] L. Storasta, J. P. Bergman, E. Janzen, A. Henry, and J. Lu, "Deep levels creted by low energy electron irradiation in 4H-SiC," *J. Appl.Phys.,* vol. 96, p. 4909, 2004.

[31] S. G. Mueller, M. F. Brady, W. H. Brixius, R. C. Glass, H. M. Hobgood, J. R. Jenny, R. T. Leonard, D. P. Malta, A. R. Powell, V. F. Tsvetkov, S. T. Allen, J. W. Palmour, and C. H. Carter, "Sublimation-grown semi-insulating SIC for high frequency devices," *Silicon Carbide and Related Materials - 2002,* vol. 433-4, pp. 39-44, 2003.

[32] K. Danno, T. Kimoto, and H. Matsunami, "Midgap levels in both n- and p-type 4H-SiC epilayers investigatd by deep level transient spectroscopy," *Appl. Phys. Lett.,* vol. 86, p. 122104, 2005.

[33] D. J. Larkin, "SiC dopant incorporation control using site-competition CVD," *phys. stat. sol. (b),* vol. 202, p. 305, 1997.

[34] J. Criado, A. Gomez, E. Calleja, and E. Munoz, "Novel method to determine capture cross secion activation energies by deep level transient spectroscopy techniques," *Appl. Phys. Lett.,* vol. 52, p. 660, 1988.

[35] M. Weidner, G. Pensl, H. Nagasawa, A. Schoner, and T. Ohishima, "Negative U cwnters in 4H- and 6H-SiC detected by spectral light detection," *Mater. Sci. Forum,* vol. 457-460, p. 485, 2004.

[36] L. Dobaczewski, P. Kaczor, L. D. Hawkins, and A. R. Peaker, "Laplace transform deep level transient spectroscopic studies of defects in semiconductors," *J. Appl. Phys.,* vol. 76, p. 194, 1994.

[37] P. Pirouz and J. W. Yang, "Polytypic transformations in SiC: the role of TEM," *Ultramicroscopy,* vol. 51, pp. 189-214, 1993.

[38] H. Matsunami and T. Kimoto, *Mater. Sci. and Eng.,* vol. 20, p. 125, 1997.

[39] W. Si, M. Dudley, H. Kong, J. J. Sumakeris, and C. H. Carter, *J. Electron. Mater.,* vol. 26, p. 151, 1997.

[40] W. L. Zhou, P. Pirouz, and J. A. Powell, "The origin of triangular surface defects in 4H-SiC CVD epilayers," *Mater. Sci. Forum,* vol. 264-268, pp. 417-420, 1998.

[41] A. O. Konstantinov, C. Hallin, P. Pecz, O. Kordina, and E. Janzen, "The mechanism for cubic SiC formation on off-oriented substrates," *J. Crystal Growth,* vol. 178, pp. 495-504, 1997.

3. Process Integration and Device Development

J. A. Cooper, Purdue University

3.1 p-Channel IGBTs

Although SiC power MOSFETs have fast switching speed and low input-gate current drive requirement, their on-state conduction loss is large, especially for those designed for high blocking voltages. The need for a controllable switch that combines the advantages of power MOSFETs and power BJTs has led to the development of the insulated gate bipolar transistors (IGBTs) [1-3]. IGBTs combine the high input gate impedance of power MOSFETs with the low on-state loss of bipolar transistor. Another new feature of the IGBTs is their ability to block high voltage on both forward and reverse directions. All these features make the IGBTs superior power devices in many applications.

3.1.1 Introduction to SiC Power IGBTs

3.1.1.1 Device structure

A p-channel DMOS-IGBT (as shown in Fig. 3.1) is similar to a p-channel DMOSFET, except that instead of having a p+ substrate, the IGBT has an n+ substrate as the cathode. A pn junction is formed between the n+ substrate and the lightly doped p-type drift layer. In high voltage DMOSFETs, the drift region resistance is high due to the lightly doped, thick drift region. IGBTs reduce the drift region resistance by injecting a large number of electrons from the n+ substrate to the p- drift region. Typically, the minority carrier concentration in the drift region can be hundreds of times higher than the background doping level. Therefore, the resistivity of the drift region is reduced by conductivity modulation.

The following pn junctions are named J1, J2, and J3, respectively: p+ source/n-well junction, n-well/p- drift region junction, and p- drift region/n+ substrate junction.

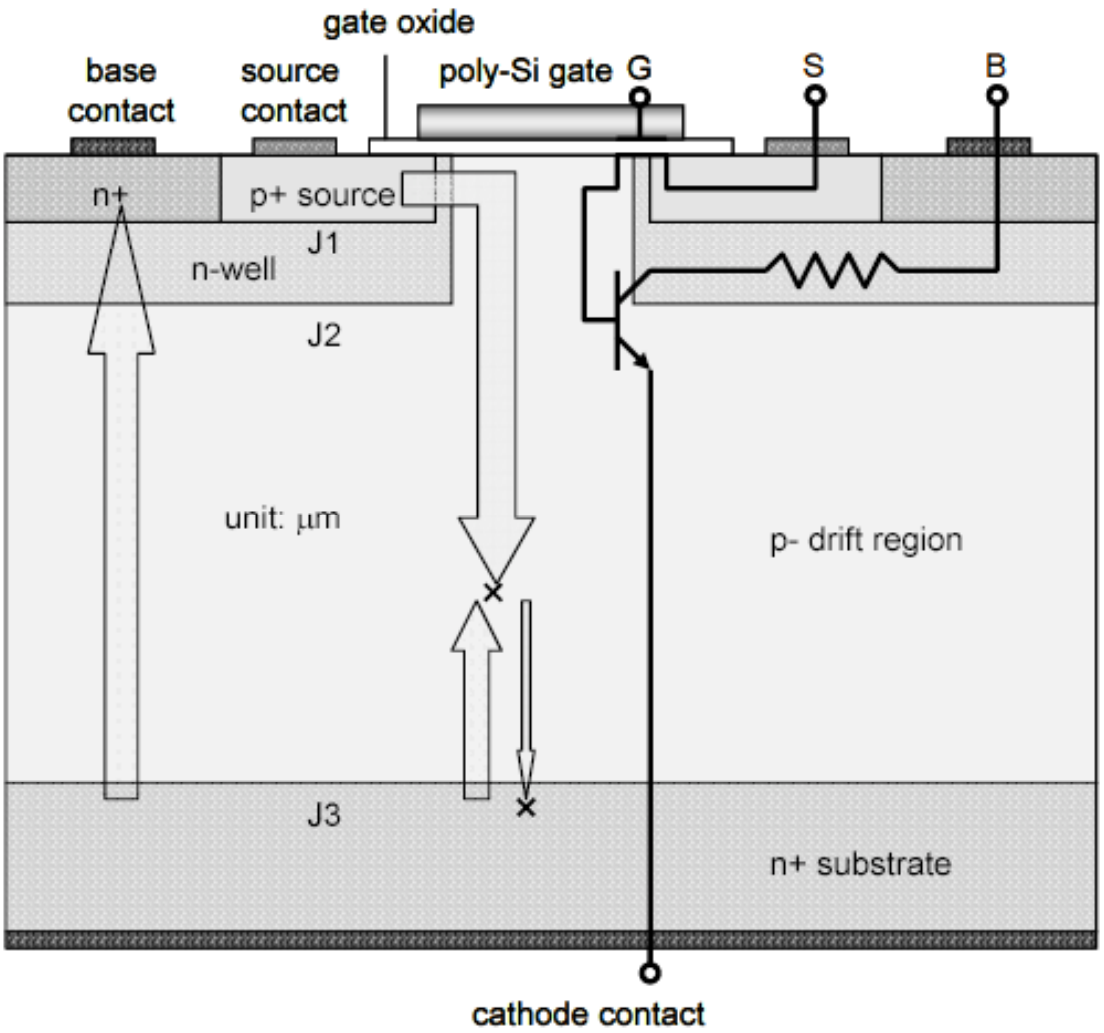


Fig. 3.1 Cross section of a p-channel DMOS-IGBT. The dark arrows indicates electron flow and the light arrows indicates hole flow.

The p- drift region is epitaxially grown on top of the n+ substrate. Thickness of the drift layer depends on the blocking voltage design. For blocking voltage over 10 kV, the drift layer has to be over 85 μm thick with doping of 10^{14}-10^{15} cm^{-3}. The doping of the drift layer has to be carefully chosen, such that the drift layer is close to punch-through as the peak electrical field in the semiconductor reaches the critical field of the material. High doping of the drift region compromises the blocking voltage and causes degradation of the injection efficiency across J3. The n-well and p+ source are formed by aluminum and nitrogen ion implantations. The doping of the n-well region has to be high enough that the base is not punched-through in the forward blocking state and low enough that the MOS inversion channel can be formed with a reasonably low gate bias. Usually, the n-well has a retrograde doping profile.

Vertically along the p+ source, the IGBT resembles a PNPN device, or thyristor. The turn-on of the parasitic thyristor (latch-up) will cause lose of current control and destroy the device. However, the IGBT is designed to suppress the turn-on of the parasitic thyristor by shorting the p+ source with the n-well.

3.1.1.2 Operation of SiC power IGBTs

There are three operation modes for the IGBTs: forward blocking, reverse blocking and forward conducting mode. Figure 3.2 shows the electric field in a P-IGBT for the blocking modes.

Unlike MOSFETs, IGBTs are capable of blocking high voltages in the reverse direction. In the reverse blocking mode, source and base are grounded and cathode is taken to a positive voltage. Junction J3 is reverse biased. Since the doping of the p- drift region is 3 to 4 orders of magnitude lower than the doping of the n+ substrate, the depletion region almost solely extends into the drift region. The doping level and thickness of the drift region are crucial for achieving a high blocking voltage. Too light drift region doping will cause punch-through before the peak field at J3 reaches the critical field of the semiconductor. Too heavy doping will lower the blocking voltage of the IGBT.

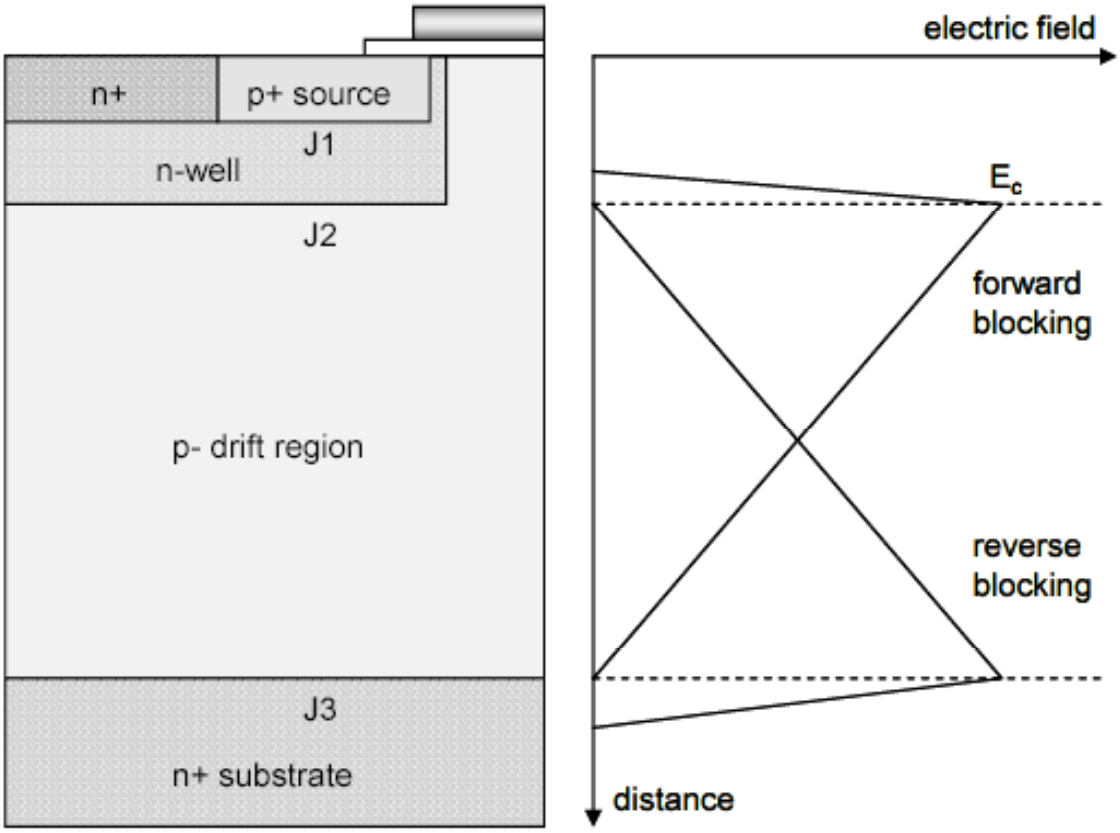


Fig. 3.2 Electric field in a P-IGBT for forward blocking and reverse blocking mode. E_c is the critical electric field of the semiconductor.

The thickness of the drift region is designed to be as small as possible to support the desired blocking voltage, because the on-state forward voltage drop increases with increasing drift region thickness. Equation (2.1) shows the relationship between the drift region thickness and blocking voltage:

$$W_{drift} = \sqrt{\frac{2\varepsilon_{SiC} V_B}{qN_d}} \tag{2.1}$$

where W_{drift} is the drift region thickness, V_B is the desired blocking voltage, and N_d is the drift region doping.

In the forward blocking mode, the source and gate are grounded, and the inversion channel is turned off. A negative bias on the cathode does not stimulate current flow because there is no current path between p+ source and p- drift region. J2 is reverse biased since the p- drift layer potential is lower than the n-well. Higher negative bias on the cathode only leads to wider depletion region in the drift layer. The n-well usually has a retrograde doping profile, such that the surface channel layer can be inverted at a reasonably low gate bias, while the depletion region in the n-well does not punch through to the p+ source. Like the reverse blocking, the forward blocking capability depends on the thickness and doping of the drift layer, and the critical electric field of the material. In Fig. 3.2, the area inside the triangles indicates the blocking voltage.

In the forward conducting mode, the equivalent circuit of the IGBT is a wide base NPN BJT with the base driven by a p-channel MOSFET, as shown in Fig. 3.1. The collector of the BJT is connected with the base contact through a lateral series resistor. The thick drift region functions as the wide base of the BJT and the n+ substrate works as the emitter.

The source and base contacts are grounded together. As the negative bias on the gate contact exceeds the threshold voltage, the channel is turned on, which allows holes in the p+ source to flow into the p- drift region. The bottom junction J3 is forward biased as a negative bias is applied to the cathode of the IGBT. Electrons are injected across J3 into the p- drift region. Some electrons travel across the drift region without recombination and get collected by the n-well. Some electrons recombine with the holes

from the source in the drift region. A small portion of holes make it through the drift region without recombination and recombine with electrons in the n+ substrate.
As the cathode voltage is increased, more electrons are injected from the n+ substrate, and correspondingly more holes flow through the MOS channel to keep charge neutrality in the drift layer. The electron and hole concentration in the drift region continues to increase until they both exceed the background doping concentration. This state, $\Delta n \cong \Delta p >> N_d$, is called "high-level injection". The resistivity of the thick drift layer is significantly reduced. The forward current saturates when the MOS channel is pinched off. Therefore, we can get a family of on-current by applying different gate voltages. With conductivity modulation in the drift region, the IGBTs can support very high blocking voltages in the off state and still operate at high on-state current density. Figure 2.3 shows the I-V characteristics of an IGBT for the three operation modes.

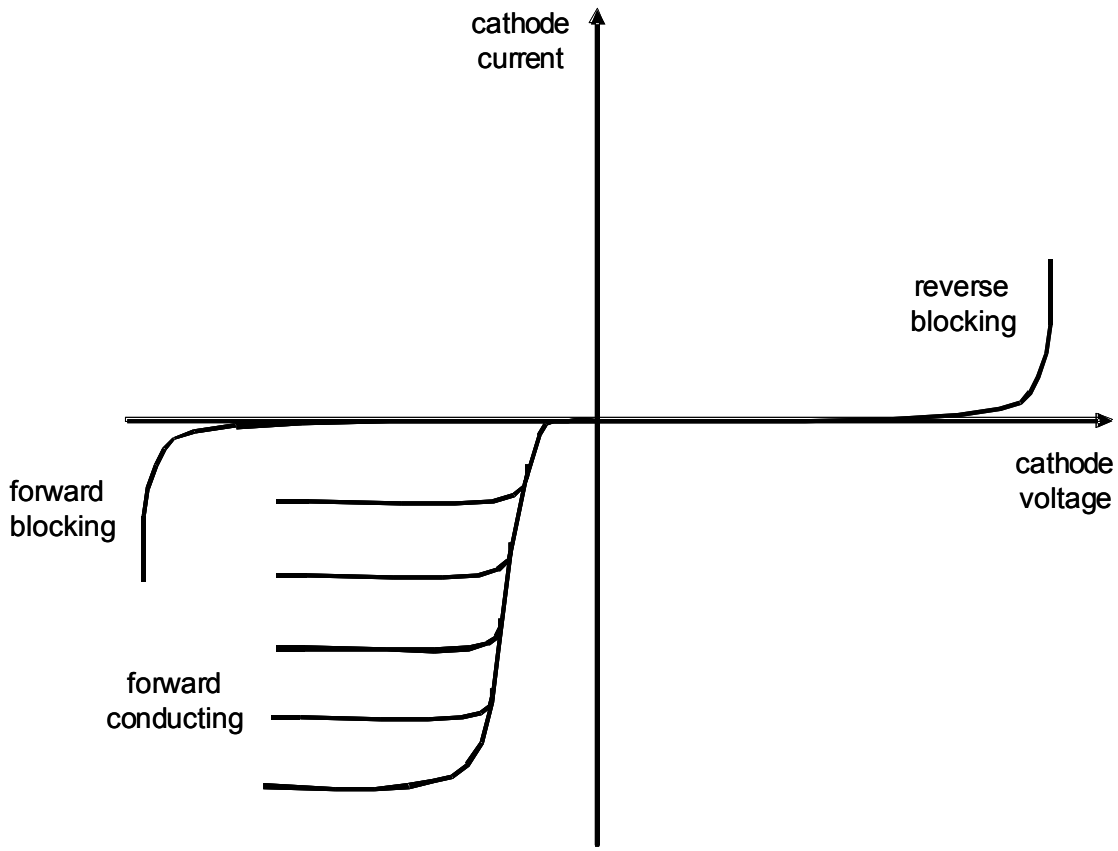


Fig. 3.3 Current-voltage characteristics of a P-IGBT.

3.1.1.3 Advantages of SiC IGBTs over MOSFETs for 10-20 kV application

10 kV SiC power MOSFETs with low on-resistance have been reported [12, 22]. The performance of these devices is approaching the theoretical limits of SiC unipolar devices. However, the demand for high blocking voltage does not stop at 10 kV. It may not be feasible to fabricate SiC MOSFETs that block over 10 kV, because the drift layer resistance is proportional to the square of the blocking voltage for a unipolar device. IGBTs, on the other hand, do not obey the R_{on}-V_B relationship of unipolar devices. Figure 3.4 show the I-V characteristics of a 20 kV p-channel IGBT and a 20 kV DMOSFET at room temperature and 225°C.

In the forward conducting mode, the DMOSFET behaves as an intrinsic MOSFET with a series resistor. The total on-resistance includes contact resistance, channel resistance, JFET resistance, and the most dominant drift region resistance. The resistances related to the intrinsic MOSFET (contact, channel and JFET resistance) can be minimized below 10 mΩ-cm^2 using several processing techniques [17]. However, the drift region resistance cannot be reduced. The on-state current increases linearly with the drain voltage as a result of the large drift region resistance. On the other hand, for the DMOS-IGBT with identical intrinsic MOSFET and drift layer, conductivity modulation takes place and the current increases very rapidly with cathode voltage. The voltage drop across the drift region, V_M, is nearly independent of current density at full conductivity modulation.

To mathematically compare the on-state performances of DMOSFETs and p-channel DMOS-IGBTs, we examine the voltage drop at fixed power dissipation. Assume the voltage drop across the devices to be V_{MOS} and V_{IGBT} for the DMOSFET and the IGBT, respectively. We have,

$$V_{MOS} = J_{on}\left(R_{ch,sp} + R_{c,sp} + R_{JFET,sp} + R_{d,sp}\right) \tag{2.2}$$

$$V_{IGBT} = \frac{J_{on}}{\beta + 1}(R_{ch,sp} + R_{c,sp} + R_{JFET,sp}) + V_M + V_J \tag{2.3}$$

where $R_{ch,sp}$, $R_{c,sp}$, $R_{JFET,sp}$, $R_{d,sp}$ are the specific channel resistance, specific contact resistance, specific JFET resistance, and specific drift region resistance, respectively. β is

the ratio of the current through the BJT to the current through the MOS channel of the IGBT. Only 1/(β+1) of the total current flows through the MOSFET part for the p-channel IGBT. The voltage drop across the drift layer V_M is a function of drift layer thickness, mobility, doping concentration, and ambipolar lifetime. Assuming 1 μs ambipolar lifetime on a 20-kV blocking epilayer (T_{epi} = 150 μm, $N_{epi} = 1x10^{14}cm^{-3}$), V_M is about 5 V. V_J is the voltage across a forward biased SiC pn junction, typically about 3 V at room temperature.

As we can see in Fig. 3.4, the current increases linearly with the applied drain voltage for the N-MOSFET with a 200 μm thick drift layer, while the current increases much more rapidly for the P-IGBT. Both devices must operate below 300 W/cm^2 package power dissipation limit. The P-IGBT carries 1.41x and 3.75x more current than the N-MOSFET at room temperature and 225°C, respectively. The greater advantage of the P-IGBT at elevated temperature is important because the device will be heated up if it continuously operates at the package power limit.

As shown in Fig. 3.4, the P-IGBT performance is almost independent of temperature. This is because of the competing temperature dependence of carrier mobility and ambipolar lifetime. As temperature is increased, mobility decreases due to phonon scattering ($\mu \sim (T/300)^{-2.8}$ [41]), while lifetime increases in a power law form ($\tau_A \sim (T/300)^{3.2}$ [42]). Consequently, the ambipolar diffusion length is almost independent of temperature. Ambipolar diffusion length is the determining factor for the voltage drop across the drift region of an IGBT.

On the other hand, the reduction of mobility with temperature leads to the increased resistance in MOSFETs at high temperatures [41].

In terms of power dissipation, the on-state power dissipation of an IGBT increases almost linearly with current density. This is because the voltage drop across the blocking layer of the IGBT is nearly independent of the current, as illustrated in equation (2.3).

$$P_{on,IGBT} = J_{on}\left[\frac{J_{on}}{\beta+1}\left(R_{ch,sp} + R_{c,sp} + R_{JFET,sp}\right) + V_M + V_J\right] \le J_{on}\left(1+5+3\right) \qquad (2.4)$$

We have set $J_{on}(R_{ch,sp} + R_{c,sp} + R_{JFET,sp}) \le (100\ A/cm^2)(10\ m\Omega\text{-}cm^2) = 1$ V, since $R_{ch,sp} + R_{c,sp} + R_{JFET,sp} \le 10\ m\Omega\text{-}cm^2$ has been demonstrated in SiC power DMOSFET in Purdue

University by using a self-aligned process and NO post-oxidation annealing [20]. The power dissipation of an on-state MOSFET is given by

$$P_{on,MOSFET} \geq J_{on}^{2}\left(R_{ch,sp} + R_{c,sp} + R_{JFET,sp} + \frac{4V_B^{2}}{\mu\varepsilon_{SiC}E_c^{3}}\right) \tag{2.5}$$

The first three terms are the intrinsic MOSFET resistance, and the fourth term is blocking layer resistance. Obviously the power dissipation of a MOSFET increases quadratically with the blocking voltage, whereas the power dissipation of an IGBT is not directly related with the blocking voltage, although there may be second-order effect of the blocking layer thickness and doping on V_M of IGBT. Therefore, the power dissipation of the IGBTs is much lower than that of the MOSFETs for devices blocking over 20 kV.

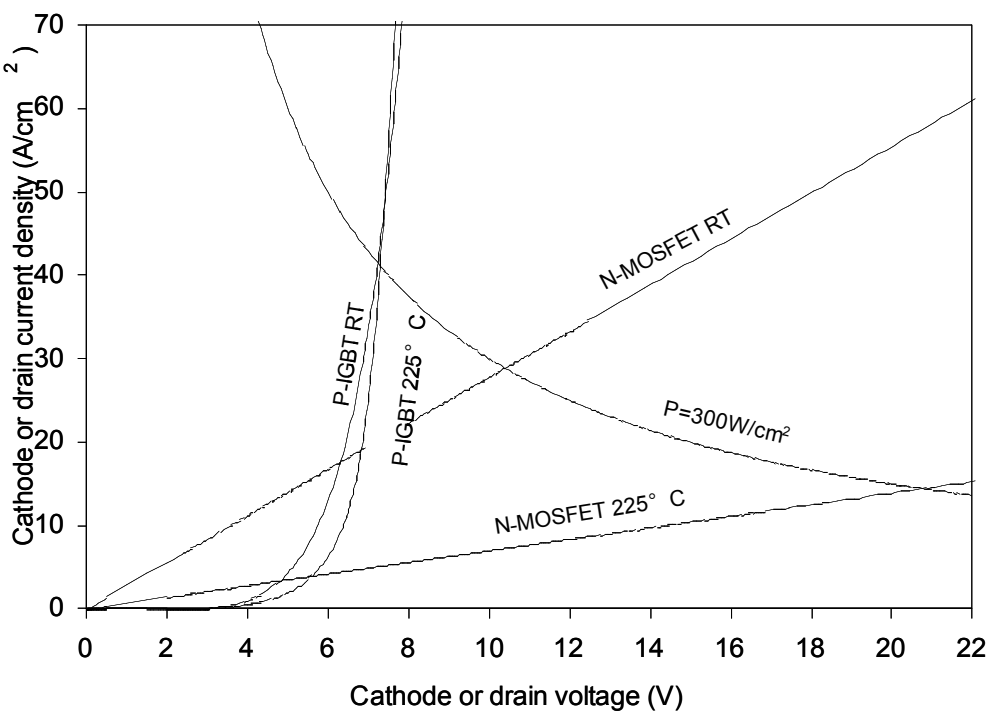


Fig. 3.4 On-state current-voltage characteristics of a P-IGBT and an N-MOSFET at room temperature and 225°C. Assume mobility and ambipolar lifetime both have power law temperature dependence [41, 42]. Both devices are designed to block 20 kV. The intrinsic MOSFET parts of the two devices are identical. N-MOSFET: T_{epi} = 200 μm, N_{epi} = 3.3x10^{14} cm^{-3}, μ_{ch} = 30 cm^2/Vs; P-IGBT: T_{epi} = 150 μm, N_{epi} = 1.0x10^{14} cm^{-3}, μ_{ch} = 7.5 cm^2/Vs, τ_A(RT) = 1 μs, τ_A(225°C) = 4 μs. The curves are generated using MEDICI^{TM} numerical simulator.

Another advantage of IGBTs over MOSFETs is that IGBTs relax the requirements on the doping accuracy of the drift layer. Figure 3.5 shows the dependence of MOSFETs figure of merit (FOM = $V_B^2/R_{on,sp}$) on drift layer doping concentration. In a unipolar power device such as a MOSFET, the drift region doping has to be precisely controlled to produce the highest figure of merit. For a given blocking voltage, there is only one pair of optimum drift layer thickness and doping. If the doping is too high, the blocking voltage is reduced. If the doping is too low, the on-resistance of the device increases. However, current epigrowth technology can only control doping within ±50% of the target value. This implies that the device performance is limited to about 75% of the theoretical value, as shown in Fig. 3.5, assuming all the fabrication processes are perfectly carried out. It is a serious issue for the yield of devices in production environment.

For IGBTs, however, $R_{on,sp}$ is not a critical parameter for device performance, and it is independent of drift layer doping on the first order. This means that we can choose the doping to maximize V_B alone, without regard to $R_{on,sp}$. The drift region on-state voltage drop V_M is not a strong function of doping. It mainly depends on drift layer thickness and ambipolar lifetime. This greatly relaxes the requirements for a precise drift layer doping. For instance, consider designing a SiC power transistor blocking 25 kV theoretically. Figure 3.6 shows the V_B dependence on the epilayer doping N_d. Point A is the optimum doping for a MOSFET with 220 μm thick epilayer. In the IGBT, we only need to optimize for V_B. It means that we can stay with 220 μm epilayer and go to point B for a higher blocking voltage. Or, we can keep the desired blocking voltage of 25 kV and go to a thinner epilayer point C. Thinner epilayer is easier to conductivity modulate and costs much less than the thick epilayer. In either case, point B or C, the blocking voltage sensitivity to doping variation is greatly reduced compared to the MOSFET, or point A. This is a significant advantage in production environment.

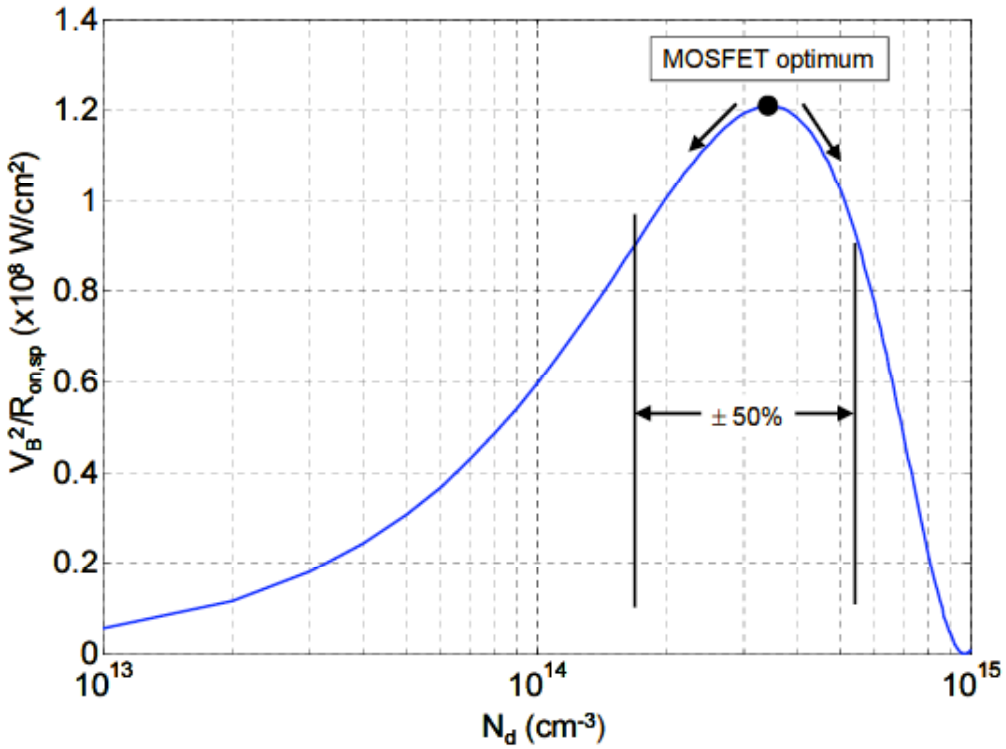


Fig. 3.5 Dependence of MOSFETs figure of merit on drift layer doping concentration. The drift layer thickness is 220 μm.

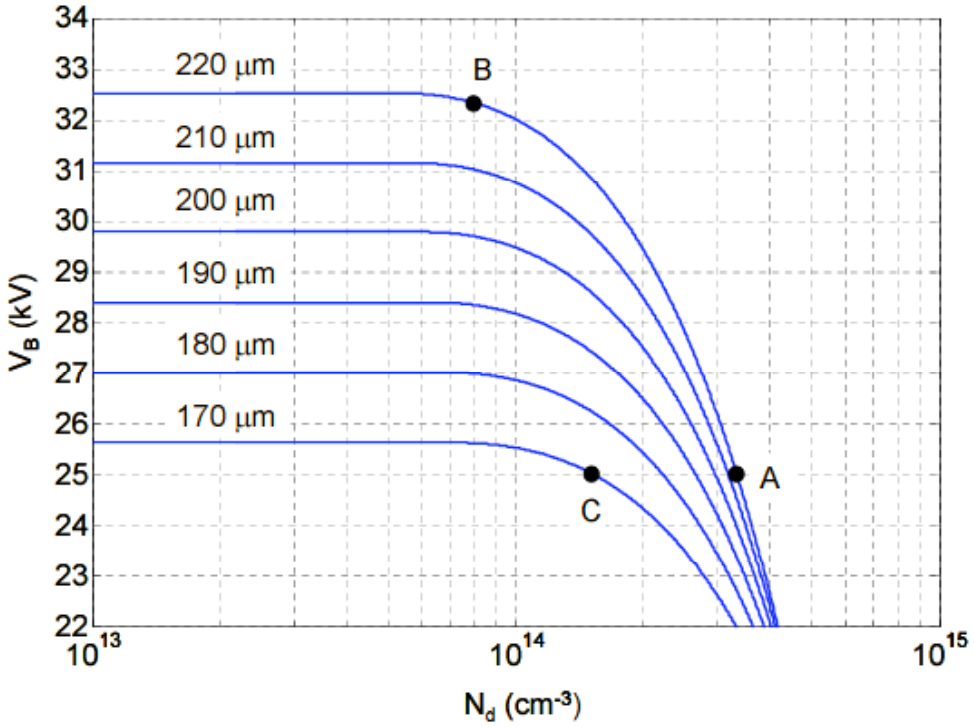


Fig. 3.6 Dependence of IGBTs blocking voltage on drift layer thickness and doping. Point A is the optimum design point for a 25 kV MOSFET.

3.1.1.4 Existing issues of SiC power IGBTs

3.1.1.4.1 P+ substrate resistance for n-channel IGBTs

We have demonstrated the superior performance of the power IGBTs compared to unipolar power devices, such as MOSFETs, in the previous secsion. From Fig. 3.1 we see that the IGBT is simply a DMOSFET with a pn junction on the bottom. There are two options to design this device: n-channel IGBT and p-channel IGBT.

N-channel devices benefit from the higher electron inversion channel mobility and the lower n-type source contact resistance compared with p-channel devices. However, the n-channel IGBT requires a low resistance p+ substrate. Unfortunately, the fraction of ionized Al dopants at a high doping level is very low (as shown in Fig. 3.7) [43]. Moreover, the ionization percentage decreases with the increase of doping concentration. Only 0.37% of Al dopants are ionized at the doping level of 10^{20} cm^{-3}. Therefore, it is difficult for the free carrier concentration in the p-type SiC to exceed $5x10^{17}$ cm^{-3}. Although increasing doping slightly helps increase the absolute number of ionized Al, the added charged centers cause more ionized impurity scattering, which results in the decrease in mobility. Therefore, it is hard to obtain a low resistive p+ substrate. Regular 300-μm p+ substrates usually have a specific resistance of 0.8-1.0 Ω-cm^2. The voltage drop across the p+ substrate will kill the on-state performance of the device. By chemical mechanical polishing (CMP), the substrate can be thinned to about 100 μm and the substrate resistance is reduced to about 250 mΩ-cm^2, which is still too high for a high performance power switch. This is why the n-channel SiC IGBTs are generally not attractive up till now. Recently, Prof. Cooper's group at Purdue University are developing a new process to reduce the p+ substrate resistance to about 2.5 mΩ-cm^2 by removing the n+ substrate and growing a thin p+ anode [44], which makes it possible to build high performance 20 kV SiC n-channel IGBTs. The process will not be discussed in detail here. But this substrate removal is difficult and the thin stand-alone epilayer is subjected to breakage during processing.

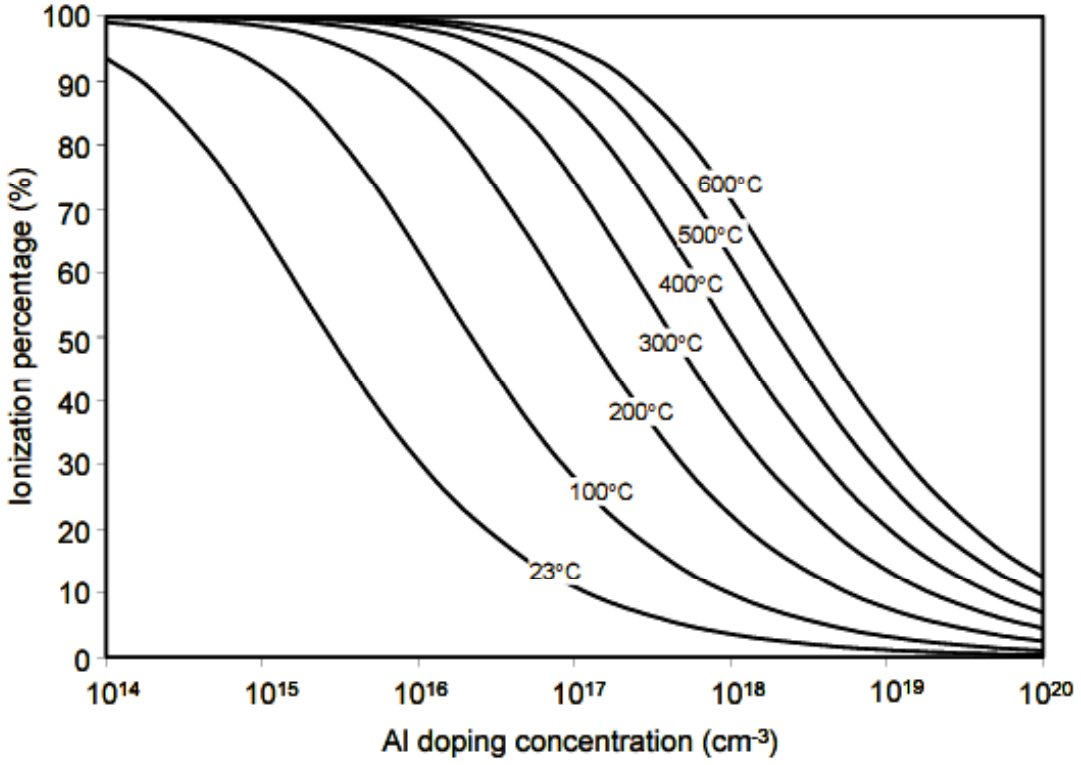


Fig. 3.7 Aluminum ionization percentage in 4H-SiC at different temperatures [43].

Another approach is to make a p-channel IGBT by switching all the doping polarities. Cree Inc. built the first p-channel 6H-SiC UMOS-IGBT in 1999 [45]. The device was built on a 15 μm 6H-SiC epilayer. It had a specific on-resistance of 431 mΩ-cm^2 and blocked 400 V. The high on-resistance is due to low vertical (along c-axis) mobility of the 6H-polytype, high contact resistance, and poor conductivity modulation. Another 10 kV p-channel 4H-SiC UMOS-IGBT was reported by Zhang et al. in 2004 [46]. The device performance was improved in terms of specific on-resistance and blocking voltage. A specific on-resistance of 175 mΩ-cm^2 was achieved at a gate voltage of -66 V at room temperature. Measurement shows much higher level of conductivity modulation in the drift layer at elevated temperatures.

The known disadvantages of the p-channel IGBTs are low inversion channel mobility, high source ohmic contact resistivity, high sheet resistance, and lack of experiences of

processing a p-channel device. The p-channel devices use n-type base and n+ substrate. The ionization ratio for n-type dopants is usually over 90% [43]. Therefore, the substrate resistance can be easily minimized and the lateral base resistance, which is related to latch-up, is also not of great concern.

In this thesis, we focus on building and characterizing p-channel 4H-SiC DMOS-IGBTs designed for blocking 20 kV.

3.1.1.4.2 Channel mobility for P-IGBTs

For a p-channel IGBT, the forward conduction operation mode is initiated by holes flowing from the p+ source to the p- drift region through the inversion channel. Since the current is the base current for the NPN BJT, the inversion channel hole mobility plays an important role on the on-state performance of p-channel IGBTs.

However, little is known about the inversion channel hole mobility in 4H-SiC. The only related information we have is that MOSFET I_d-V_{ds} measurement shows that the saturation current of an n-channel device is approximately four times greater than the saturation current of a p-channel device in 6H-SiC [47] for the same $|V_{gs}-V_t|$. The saturation current equations of n-channel and p-channel MOSFETs are:

$$I_{d,sat}^{n-mos} = \mu_{n,eff} C_{ox} \bullet \frac{W}{2L}\left(V_{gs} - V_t\right)^2 \tag{2.6}$$

$$I_{d,sat}^{p-mos} = \mu_{p,eff} C_{ox} \bullet \frac{W}{2L}\left(V_{gs} - V_t\right)^2 \tag{2.7}$$

where $\mu_{n,eff}$ and $\mu_{p,eff}$ are the effective channel mobility for electrons and holes, C_{ox} is the oxide capacitance, W and L are the width and length of the channel. By making the n-channel and p-channel MOSFETs identical dimensions and same gate oxide thickness, the ratio of the two saturation current at same $|V_{gs}-V_t|$ equals to $\mu_{n,eff}/\mu_{p,eff}$. Therefore, we can deduce the effective channel hole mobility from the effective channel electron mobility. In our work, we will directly measure the MOS hole mobility using the constant current technique, which does not require ohmic contacts [33].

3.1.1.4.3 P-type ohmic contact resistance

The p-channel UMOS-IGBTs reported by Ryu et al. [45] and Zhang et al. [46] both suffer from poor p-type ohmic contacts. Since p-channel devices require a p-type source

region, the ohmic contact to the source is crucial for the on-state performance of the devices. For instance, supposing the p-type contact resistivity $\rho_c = 5x10^{-2}$ Ω-cm^2, the voltage across the p-type contact at 100 A/cm^2 is 5 V! It has been discovered that the p-type contact resistance is influenced by the composition of contact metal alloys, the annealing condition, and the cleaning procedures [48].

Aluminum is an excellent choice for p-type ohmic metal. However, it is reported that spiking of Al causes premature junction breakdown if pure Al is used. It can be prevented by replacing pure aluminum with 25 wt% Ti / 75 wt% Al as contact metals [48]. The two metals form alloys at the annealing temperature. The ratio of the metals is important because the Ti/Al alloy is in liquid phase for 0 ~ 30 wt % of Ti at our annealing temperature. The alloy is not a liquid if Ti is over 30wt%, and contacts are not ohmic. High purity metals should be used for best results.

The wafer has to be properly cleaned before the contact metals are evaporated. Lift-off lithography is used for patterning the contact metals. It is possible that some residual photoresist is left on the wafer areas where metals will be deposited. RIE in SF_6 for 1 minute at 100 Watt is used to remove the residual photoresist. Then O_2 plasma etching for 1 minute at 100 Watt is used to clean the fluorine compound residue that RIE left. Finally, dipping the wafer in BHF for 10 seconds removes any oxide that is grown during the O_2 plasma etch. Ti/Al is then deposited on the wafer using an e-beam evaporator. The vacuum during the evaporation has to be lower than $5x10^{-7}$ torr, since Ti and Al are subjected to oxidation in the presence of oxygen [48].

The wafer lies on a piece of SiC susceptor in the contact annealer. The susceptor needs to be cleaned with the following procedure each time before annealing: Aqua-regia 1 hr, HF: HNO_3 (1:1) 1 hr, Piranha 10 min, BHF 3 min, and sacrificial oxidation 3 hrs. A dummy annealing will be conducted in vacuum condition before the run with the real sample to drive off and pump out all the contamination from the previous annealing [48]. We discover that there is always a fluctuation of contact resistivity across the wafer after annealing. It is possibly caused by the non-uniform temperature distribution of the heater and/or the non-flat susceptor or wafer.

The most significant parameters for contact annealing are atmosphere and temperature [48]. Annealing in vacuum has the advantage over annealing in argon because the contaminating substance driven off is likely to be pumped out of the chamber rather than being re-deposited on the wafer surface. This explains the lower leakage current for the vacuum annealed samples than the Ar annealed samples. O_2 plasma etching after annealing reduces the leakage current by several orders of magnitude. Top metal can slightly improve the contact resistivity. Annealing at higher temperature results in much lower contact resistivity because metals alloy faster with SiC due to the kinetics of the reaction. However, MOS devices are not suitable for annealing over 1000 °C because the MOS interface tends to be damaged at high temperature. Therefore, we will limit the annealing temperature to 1000°C for the p-channel IGBT fabrication.

Table 3.1 P-type contact resistivity after contact annealing under different conditions [48]

Contact anneal condition	After contact anneal (before top metal)		After O_2 plasma etch and top metal	
	Contact resistivity ρ_c (Ω-cm^2)	Leakage current I_j (A) @ 40V	Contact resistivity ρ_c (Ω-cm^2)	Leakage current I_j (A) @ 40V
1000°C, 2 min, vacuum	$8x10^{-6}$ ~ $5x10^{-4}$	$5x10^{-8}$ ~ $5x10^{-7}$	$6x10^{-6}$ ~ $4x10^{-5}$	~$5x10^{-11}$
950°C, 2 min, vacuum	$6x10^{-5}$ ~ $3x10^{-4}$	$2x10^{-9}$ ~ $1x10^{-8}$	$1x10^{-4}$ ~ $5x10^{-4}$	~$5x10^{-11}$
900°C, 4 min, vacuum	$2x10^{-2}$ ~ $1x10^{-1}$	$5x10^{-9}$ ~ $2x10^{-8}$	$4x10^{-3}$ ~ $3x10^{-2}$	~$5x10^{-11}$
1000°C, 2 min, argon	$2x10^{-4}$ ~ $6x10^{-4}$	$5x10^{-6}$ ~ $5x10^{-5}$	$1x10^{-4}$ ~ $6x10^{-4}$	$1x10^{-6}$ ~ $2x10^{-5}$

3.1.1.4.4 Ambipolar lifetime in the drift region

The most attractive property of high voltage IGBTs is the low on-state power loss. High conductivity modulation in the drift region is essential for the low on-resistance of the IGBTs. Ambipolar diffusion length (L_A) is the determining factor for conductivity modulation.

$$L_A = \sqrt{D_A \tau_A} \tag{2.8}$$

where D_A is the ambipolar diffusion coefficient, and τ_A is the ambipolar lifetime.

$$D_A = \frac{2D_n D_p}{D_n + D_p} \tag{2.9}$$

where D_n and D_p are related to μ_n and μ_p by the Einstein relation:

$$D_{n,p} = \frac{kT}{q}\mu_{n,p} \tag{2.10}$$

The ambipolar lifetime is the sum of the electron lifetime and the hole lifetime:

$$\tau_A = \tau_n + \tau_p \tag{2.11}$$

Therefore, in order to achieve high conductivity modulation, the ambipolar lifetime in the drift epilayer is a key material parameter.

Figure 3.8 shows the simulated on-state I-V characteristics of a 20-kV p-channel IGBT at room temperature with different ambipolar lifetime. Long ambipolar lifetime is desired because it significantly reduces the voltage across the drift region. The I-V characteristics of a 20-kV n-channel DMOSFET is also shown in the figure for comparison. Since the devices must operate under 300 W/cm^2 package power dissipation limit, the ambipolar lifetime needs to be at least 0.5 μs for the IGBT to have an advantage over the MOSFET at room temperature.

Ambipolar lifetime basically depends on temperature, impurity and trap density in the semiconductor. Kordina et al. has reported that by using the “Hot-Wall” CVD technique for growing 4H-SiC, room temperature minority carrier lifetime is in the microsecond range [49].

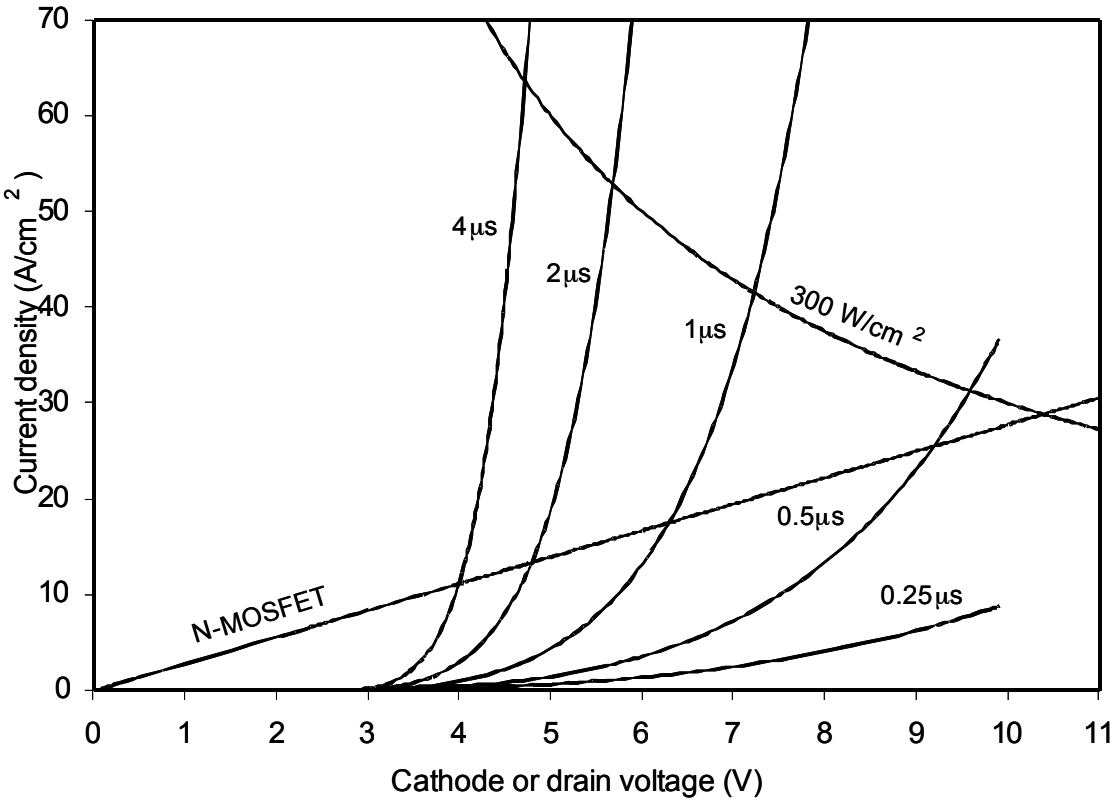


Fig. 3.8 Simulated I-V characteristics of an N-MOSFET and P-IGBTs with different ambipolar lifetime. All devices are designed to block 20 kV. P-IGBTs: T_{epi} = 150 μm, N_{epi} = $1x10^{14}cm^{-3}$; N-MOSFET: T_{epi} = 200 μm, N_{epi} = $3x10^{14}cm^{-3}$.

The temperature dependence of minority lifetime has been reported by several groups and the results are shown in Fig. 3.9. Although different parts of different devices are subjected to lifetime measurement, all the results agree well on the temperature dependence. Lifetime is plotted against 1000/T and the linear trendlines are added to the data. The slopes of the trendlines are almost identical for different devices. The temperature dependence is extracted from the lines to be:

$$\tau(T) = \tau(T_0)\left(\frac{T}{T_0}\right)^{3.2} \quad [42] \qquad (2.12)$$

Since mobility decreases with temperature in a power law form [50], and lifetime increases with temperature according to equation (2.12), the ambipolar diffusion length is nearly independent of temperature in the regime of room temperature to 200°C.

Figure 3.8 indicates that lifetime is the single most important material parameter for IGBTs on-state performance. The materials used for the P-IGBT fabrication is provided by Cree Inc. The lifetime of the materials is around 0.5 μs at room temperature. Therefore, we expect the P-IGBTs to have a small advantage over N-MOSFETs at room temperature, and much more pronounced advantages at high temperature.

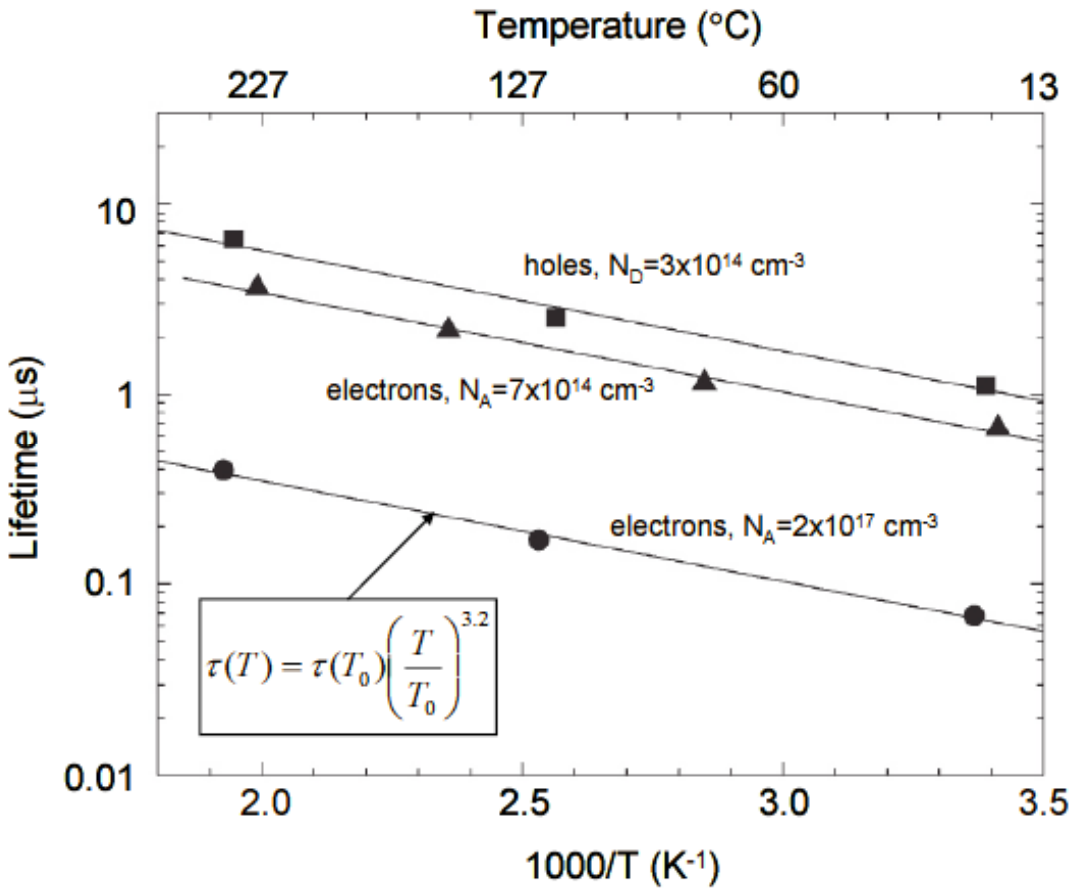


Fig. 3.9 Temperature dependences of minority lifetime in 4H-SiC bipolar devices. Circles, electron lifetime in the p-base of a 1 kV BJT [42]; squares, hole lifetime in the n-base of a 10 kV pn diode [51]; triangles, electron lifetime in the p-base of a 2.6 kV GTO [52].

3.1.1.4.5 Latch-up under high current condition

Latch-up is the turn on of the parasitic PNPN thyristors present in the IGBT. Once the device is in the latch-up mode, gate control of the current flow is lost and the IGBT will be destroyed due to excessive power dissipation.

The mechanism of latch-up is explained in Fig. 3.10. A PNP bipolar transistor is connected with an NPN bipolar transistor in the way that they feed each other's base currents with their collector currents. In forward conducting mode, a negative bias is applied to the cathode and the bottom pn junction is forward biased. Electrons are injected into the drift layer. The MOS gate turns on to supply hole current through the inversion channel to the base of the NPN bipolar transistor. The base/collector junction of the NPN bipolar transistor is reverse biased and most of the injected electrons are swept into the n-well. These electrons flow out of the device through the n+ contact. Numerical simulation shows that the majority of electron current enters the n-well from the right edge of n-well. Therefore, these electrons laterally traverse the n-well. The lateral resistance of the n-well creates a voltage drop from the n+ contact to the right edge of n-well under high base current conditions. If this voltage drop is close to 3 V, the p+ source/n-well junction is forward biased and holes are injected from the p+ source into the n-well. This leads to the formation of a PNP bipolar transistor with p+ source (emitter), n-well (base), and p- drift region (collector), as shown in the circuit in Fig. 3.10.

The PNP and NPN bipolar transistors are connected in such a way that any increase in the base current of one transistor causes β times base current increase for the other one, and vise versa. It is a positive feedback circuit as long as $\beta 1 \bullet \beta 2 > 1$. This condition is satisfied if the emitter to base doping ratios for the two BJTs are both large. Even if the MOS gate is turned off, the two transistors can still feed base current to each other and keep increasing the current. The device will eventually be destroyed by excessive power dissipation.

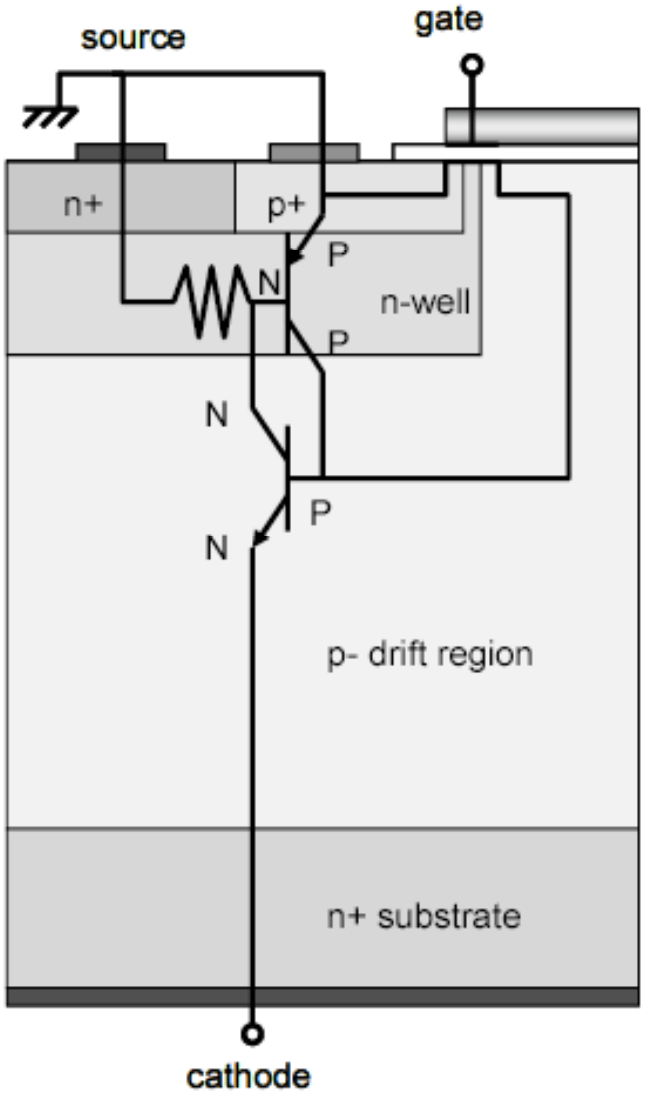


Fig. 3.10 Circuit diagram for a p-channel DMOS-IGBT under latch-up condition.

Several techniques have been employed to prevent latch-up of IGBTs. Most approaches attempt to reduce the resistivity of the n-well such that the lateral voltage drop is less than the amount needed to turn on the PNP bipolar transistor. Goodman et al. indicate that a buffer layer between drift region and cathode contact not only improves the forward blocking performance of IGBTs, but also increases the latch-up current capability by suppressing the electron injection from the cathode contact [53].

After all, latch-up is unlikely to occur for the p-channel SiC IGBT. The voltage required to turn on a SiC PN junction is close to 3 V, which is hard to achieve under normal operation conditions. Moreover, it is easy to make the n-type base less resistive because of the high ionization ratio of n-type dopants at room temperature [43]. Our numerical simulation indicates that latch-up does not occur for current up to 1760 A/cm^2, as shown in Fig. 3.11.

3.1.1.4.6 Open base BJT effect in blocking state

In the punch-through IGBT design, a p+ buffer layer is inserted between the p- drift layer and the n+ substrate to improve the blocking voltage. The p+ buffer layer also helps prevent electrons in the n+ substrate to be injected into the p- drift layer and cause current flow.

Figure 3.12 shows the band diagram of the P-IGBT in the blocking state. The n+ substrate, p- drift layer & p+ buffer layer, and the n-well are the emitter, base and collector of an NPN bipolar transistor. In the blocking state, the collector is grounded, the base is open, and the emitter is taken to a negative high voltage. Therefore, the EB junction is forward biased and the BC junction is reverse biased. This is equivalent to a BJT in forward active mode. If the current gain β is high, any small current fluctuation in the base will cause β times higher current in the collector. This premature breakdown prior to the junction breakdown due to avalanche is called the open base BJT effect. Simulation of a 25 kV P-IGBT with p+ buffer layer is carried out to verify the open base BJT effect. The device blocks 25,037 V before avalanche breakdown starts. Obviously, no premature breakdown occurs. The explanation will be given with the aid of the band diagram and the minority carrier density diagram as shown in Fig. 3.12.

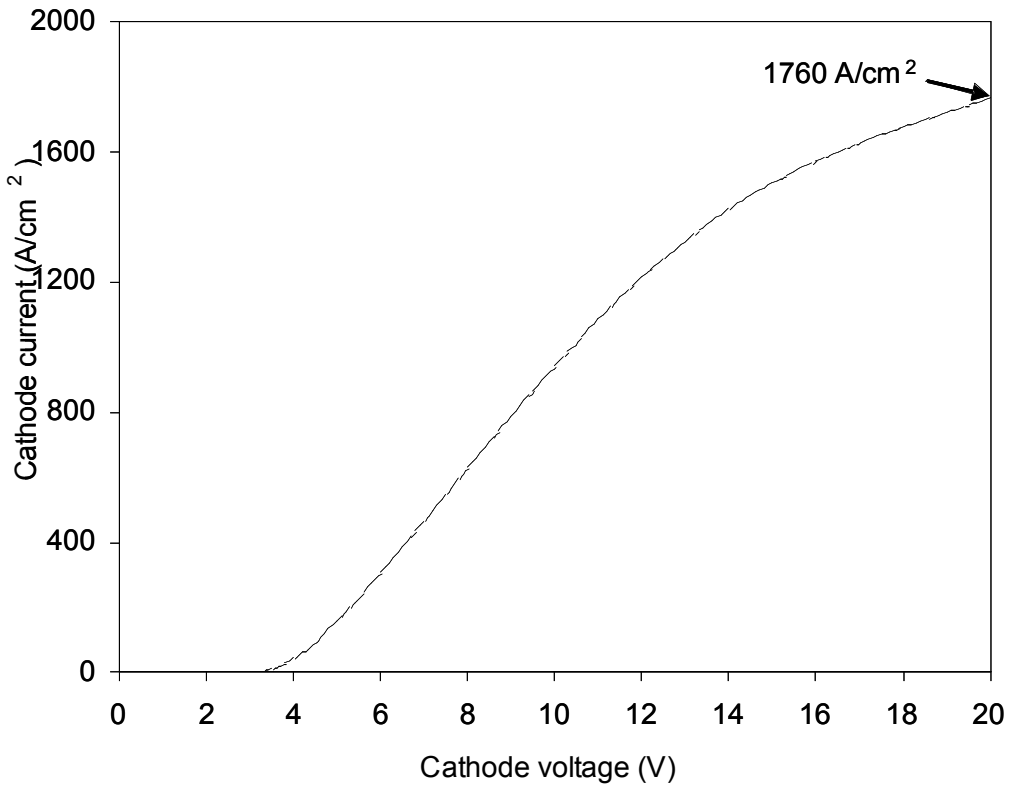


Fig. 3.11 I-V characteristics of a p-channel IGBT under high current condition.

The p- drift region is completely depleted as well as part of the p+ buffer layer as the n+ substrate is taken to a negative high voltage. The effective base width is the remaining undepleted p+ layer, which is smaller than the minority carrier diffusion length in the p+ region. The hole current and the electron current in the emitter are given by:

$$I_{EP} = qA\frac{n_i^2}{N_{DE}}\frac{D_{PE}}{L_{PE}}e^{qV_{EB}/kT} \tag{2.13}$$

$$I_{EP} = qA\frac{n_i^2}{N_{AB}}\frac{D_{NB}}{W_B}e^{qV_{EB}/kT} \tag{2.14}$$

where N_{DE} and N_{AB} are the doping in the emitter and the base, D_{PE} and D_{NB} are the diffusion coefficient in the emitter and the base, W_B is the effective base width, and L_{PE} is the diffusion length in the emitter. Therefore, the emitter efficiency is

$$\gamma = \frac{I_{En}}{I_{En} + I_{Ep}} = \frac{1}{1 + \left(\frac{N_{AB}}{N_{DE}}\frac{W_B}{L_{PE}}\frac{D_{PE}}{D_{NB}}\right)} \tag{2.15}$$

Since both the emitter and the base are heavily doped to the same level, we can assume that value of the terms in the parenthesis in equation (2.15) is ~ 1. Therefore, $\gamma = 1/2$. Since the base is open, all the emitter electron current flows across the base into the collector. Therefore, the base transport factor $\alpha_T = I_{Cn}/I_{En} = 1$. The current gain is

$$\beta = \frac{\gamma\alpha_T}{1 - \gamma\alpha_T} = 1 \tag{2.16}$$

As long as the doping concentration of the p+ layer is comparable to the n+ substrate, the current gain will be low and the open base BJT effect is not going to be a big issue for the blocking voltage of the P-IGBT.

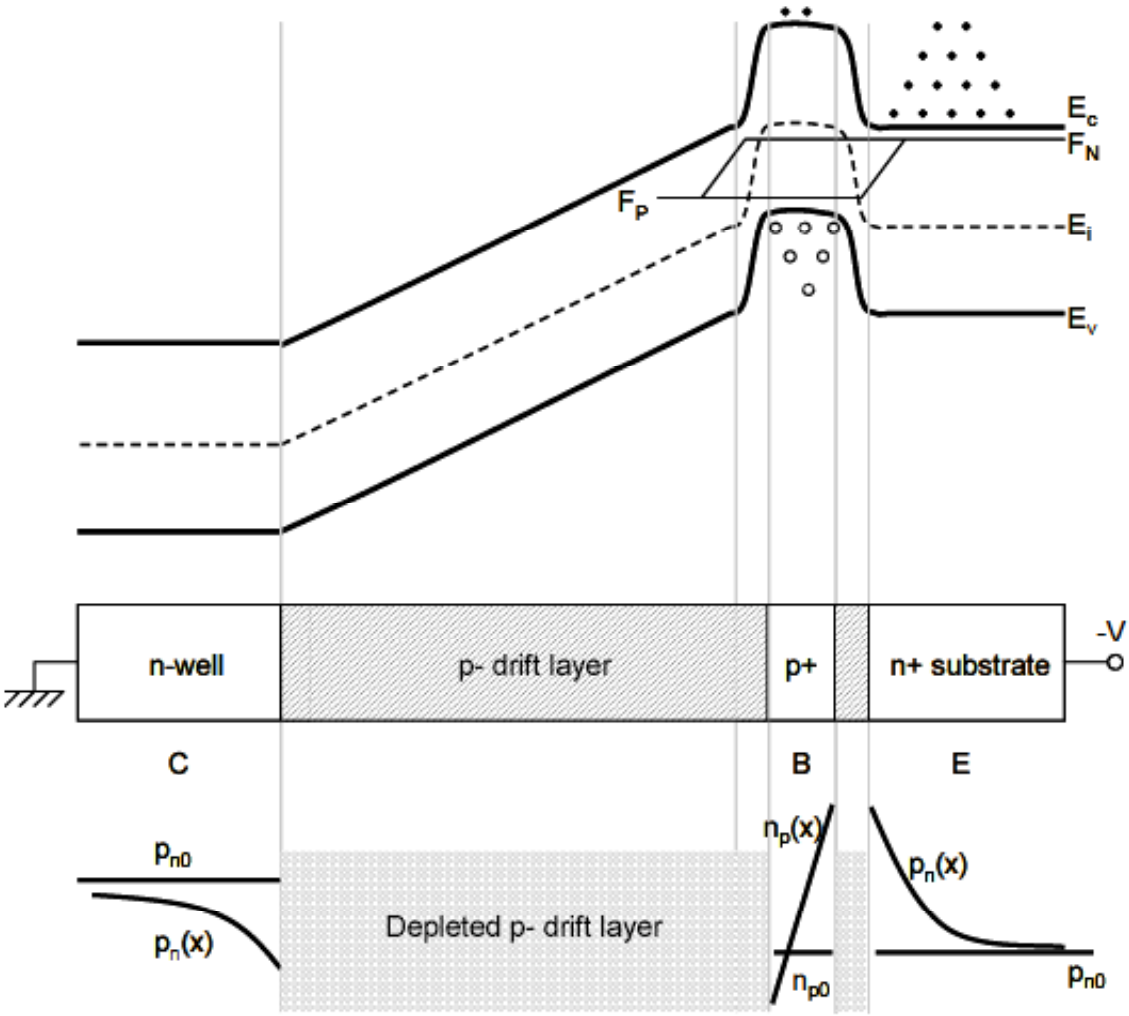


Fig. 3.12 Band diagram and minority carrier concentration of the P-IGBT in blocking state.

3.1.2 Design and Optimization of the SiC P-Channel DMOS IGBT

3.1.2.1 Figure of merit for IGBTs

Figure of merit (FOM) is used to evaluate device performance. For unipolar power devices such as MOSFETs, FOM is defined as $V_B^2/R_{on,sp}$. This definition is not suitable for evaluating the performance of IGBTs because IGBTs do not have a constant specific

on-resistance due to conductivity modulation. Therefore, we need a new definition of figure of merit that can evaluate both unipolar devices and bipolar devices. For power switching devices, the product of blocking voltage (V_B) and maximum allowed on-state current (I_{on}) represents the power capability of the device. Define the figure of merit:

$$FOM \equiv P = V_B I_{on} = V_B J_{on} A \tag{3.1}$$

The limitation for J_{on} is the on-state power dissipation per unit area

$$P_D \equiv V_{on} J_{on} \tag{3.2}$$

where V_{on} is the on-state voltage drop across the device.

For MOSFETs, the on-state specific resistance ($R_{on,sp}$) is a constant in the linear region, and $V_{on,MOSFET}$ is given as

$$V_{on,MOSFET} = J_{on} R_{on,sp} \tag{3.3}$$

Therefore, the figure of merit for a MOSFET is:

$$FOM_{MOSFET} = A V_B \sqrt{\frac{P_D}{R_{on,sp}}} = A \sqrt{P_D \left(\frac{V_B^{\ 2}}{R_{on,sp}} \right)} \tag{3.4}$$

This is consistent with the conventional definition of FOM ≡ $V_B^2/R_{on,sp}$ for MOSFETs.

For IGBTs, the I-V relationship is not linear, but

$$V_{on,IGBT} = V_J + V_M + J_{on} R_{intr,sp} \tag{3.5}$$

where V_J is the voltage across the forward biased pn junction, V_M is the voltage across the drift region, and $R_{intr,sp}$ includes specific channel, contact, and JFET resistance. Note that equation (3.5) is slightly different from equation (2.3) because β is usually much smaller than 1 for very wide p- base and is ignored here.

$$J_{on} = P_D / V_{on,IGBT} = \frac{P_D}{V_J + V_M + J_{on} R_{intr,sp}} \tag{3.6}$$

V_M actually increases slowly with J_{on}. But if we assume that J_{on} does not exceed 100 A/cm^2 due to the power dissipation limit, we can use the V_M value at 100 A/cm^2 as an upper limit for V_M. It is a pessimistic approximation. Solving for J_{on}, we have

$$J_{on} \geq \frac{1}{2R_{intr,sp}} \left[\sqrt{(V_J + V_M)^2 + 4R_{intr,sp} P_D} - (V_J + V_M) \right] \tag{3.7}$$

Therefore,

$$FOM_{IGBT} = AV_B J_{on} \geq A\frac{V_B}{2R_{intr,sp}}\left[\sqrt{(V_J + V_M)^2 + 4R_{intr,sp}P_D} - (V_J + V_M)\right] \quad (3.8)$$

Note that $R_{intr,sp}$, V_J and P_D are constants. Mathematically, FOM approaches zero if (V_J + V_M) >> $4R_{intr,sp}P_D$. To maximize the FOM for IGBTs, we need to maximize V_B and minimize V_M. This is the design criterion for the P-IGBTs.

3.1.2.2 Analytical models for blocking mode and conducting mode

3.1.2.2.1 Blocking voltage

In the blocking state, the voltage across the drift region can be increased until impact ionization starts. The rate at which carriers are generated by impact ionization is a strong function of electric field. The critical electric field is a fundamental material parameter. Generally speaking, breakdown occurs as the electric field in the semiconductor reaches the critical field. However, more careful study suggests that it is the ionization integral approaching 1 that initiate the avalanche process [5]. For electron initiated impact ionization, the ionization integral is given by:

$$\int_0^W \alpha_n \exp\left[-\int_x^W (\alpha_n - \alpha_p)dx'\right]dx = 1 \quad (3.9)$$

If avalanche is initiated by holes, switch the subscripts n and p and obtain an equivalent integral. The electron and hole impact ionization coefficients (α_n, α_p) are highly sensitive to local electric field [54]. α is given by an empirical model in the following form:

$$\alpha = \alpha_0 \exp\left[-\left(\frac{E_c}{E}\right)^m\right] \quad (3.10)$$

For 4H-SiC, $\alpha_{p0} = 3.32\text{x}10^6$ cm^{-1}, $E_{cp} = 1.07$ x 10^7 V/cm, $m_p = 1.1$; $\alpha_{n0} = 1.69\text{x}10^6$ cm^{-1}, $E_{cn} = 9.69\text{x}10^6$ V/cm, $m_n = 1.6$ [3].

One way of determining the avalanche breakdown voltage is to decouple the electron and hole continuity equations from the impact ionization integral calculation. In this method, the electric field is calculated by solving Poisson's equation and then the ionization integral is evaluated until the condition in (3.9) is met. It is relatively simple,

but it assumes that the avalanche process does not significantly alter the electrostatics of the device. This method is inaccurate if multiplication becomes significant or two-dimensional field crowding is included [54]. Another method is to solve the Poisson's equation and the electron and hole continuity equations self-consistently using numerical simulators such as Medici™. The second method can give accurate results for complicated device structures, although it takes more time and computing resources.
It has been shown that the decoupled method is sufficiently accurate for developing design guidelines for simple device structures. Figure 3.13 shows the electric field in the lightly doped drift layer as a function of position. The blocking voltage is the shaded area. If the drift layer is not punched-through, the blocking voltage is

$$V_B = \frac{\varepsilon_{SiC} E_c^{\,2}}{2qN_{epi}} \tag{3.11}$$

If the drift layer is punched-through and the electric field is terminated in the n+ layer, the blocking voltage is given by

$$V_B = E_c T_{epi} - \frac{qN_{epi}}{2\varepsilon_{SiC}} T_{epi}^{\,2} \tag{3.12}$$

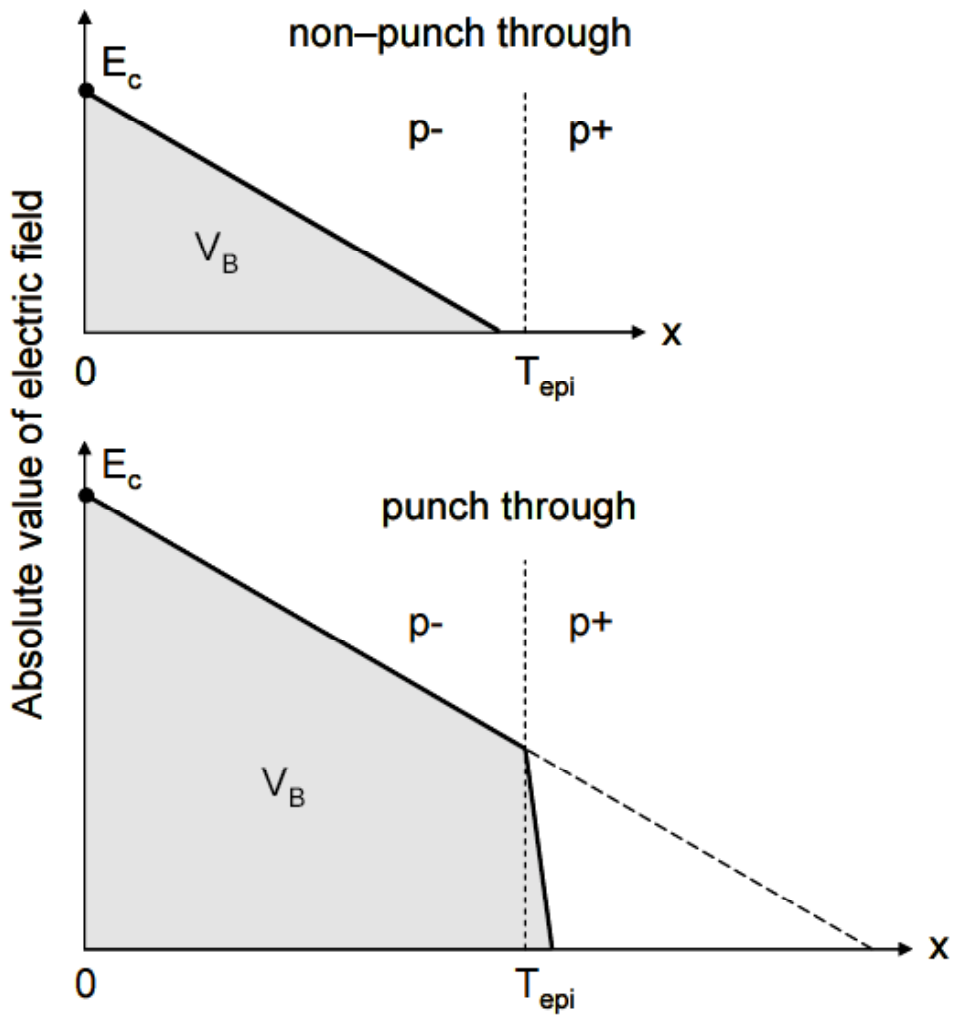


Fig. 3.13 Electric field in the drift layer of a non-punch-through P-IGBT and a punch-through P-IGBT. The shaded area indicates blocking voltage. The p- region is drift layer.

Konstantinov, et al., indicates that the critical electric field is a function of epilayer doping by the following relation [3]:

$$E_c = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log_{10}\left(\frac{N_{epi}}{10^{16}\,cm^{-3}}\right)} \quad \text{(V/cm)} \qquad (3.13)$$

Equation (3.13) is plotted in Fig. 3.1. It shows a descending trend of critical field as doping level decreases. However, careful study of the ionization integral by Morisette

[54] indicates that in punch-through devices, the correct critical field to use in (3.12) is given by (3.13) at moderate doping concentration. At very low doping, the critical field becomes independent of doping, and instead depends on the drift layer thickness according to the empirical relationship:

$$E_{cr,\min} = 274 - 88.5 T_{epi}^{-0.1} \log_{10}(T_{epi}) \ \ (\text{V/}\mu\text{m}) \tag{3.14}$$

Combining (3.12), (3.13) and (3.14), the V_B-N_{epi} relationship is plotted in Fig 3.14. Note that the blocking voltage approaches a constant as the doping becomes lower than 10^{14} cm^{-3} [54].

When we design a device, several (N_{epi}, T_{epi}) pairs can be selected to achieve the same blocking voltage. For instance, we can choose either (140 μm, $3x10^{14}$ cm^{-3}), or (160 μm, $4x10^{14}$ cm^{-3}) epilayers to block 20 kV. The criterion is to select the epilayers that have the lowest on-state voltage drop at the power dissipation limit.

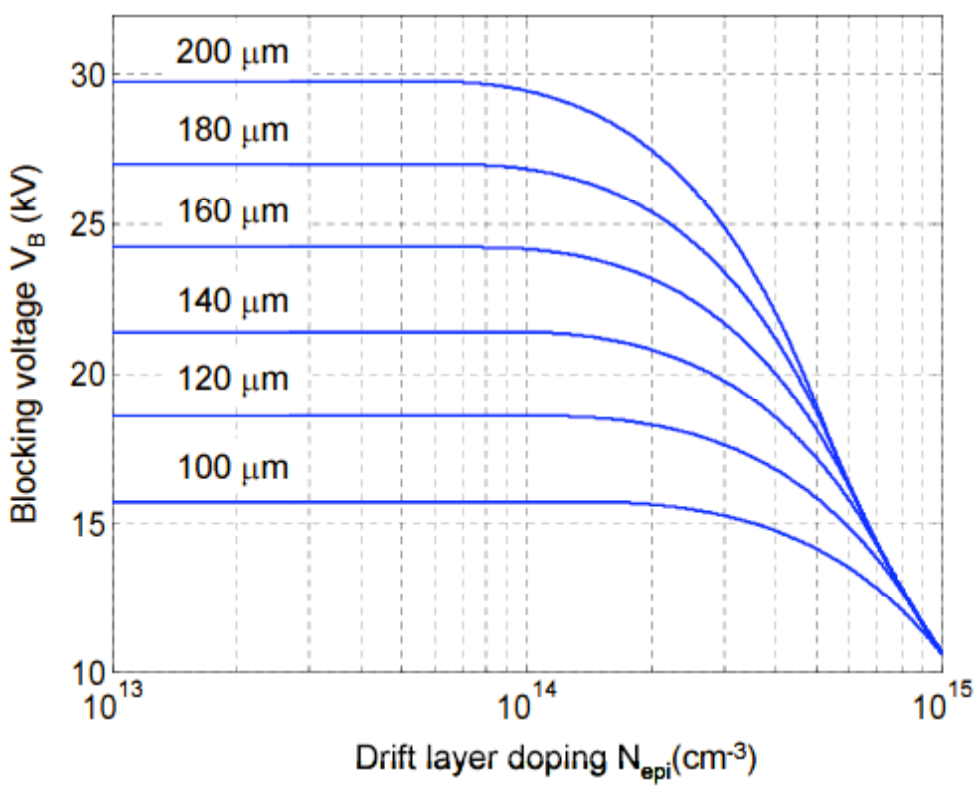


Fig. 3.14 4H-SiC IGBTs blocking voltage vs. drift layer doping

3.1.2.2.2 Forward voltage drop

As stated in the introduction of the IGBTs, the forward voltage drop across the device includes the voltage across the forward biased pn junction (V_J), voltage across the intrinsic MOSFET, and voltage across the drift region (V_M). The first two terms are constant or small. The third term, V_M, is a variable of drift layer specifications. We developed the following one-dimensional analytical model to describe the current and voltage in the drift region of IGBTs.

Let's take the p-channel IGBT for example. Consider that the n+ substrate, p-drift region and the n-well form the emitter, base and collector of a wide-base BJT, as shown in Fig. 3.15. Set the origin at the EB junction, and W is the base width minus the depletion region width at BC junction. The material parameters in the drift region are defined in Table 3.2.

Table 3.2 Parameters in the drift layer of the P-IGBT

Symbol	Unit	Value
μ_N	cm^2/Vs	943
D_N	cm^2/s	24.4
τ_N	μs	0.5
L_N	cm	$3.49x10^{-3}$
μ_P	cm^2/Vs	106
D_P	cm^2/s	2.75
τ_P	μs	0.5
L_P	cm	$1.17x10^{-3}$
b	-	8.9
D_A	cm^2/s	4.94
τ_A	cm	$1x10^{-6}$
L_A	cm	$2.22x10^{-3}$

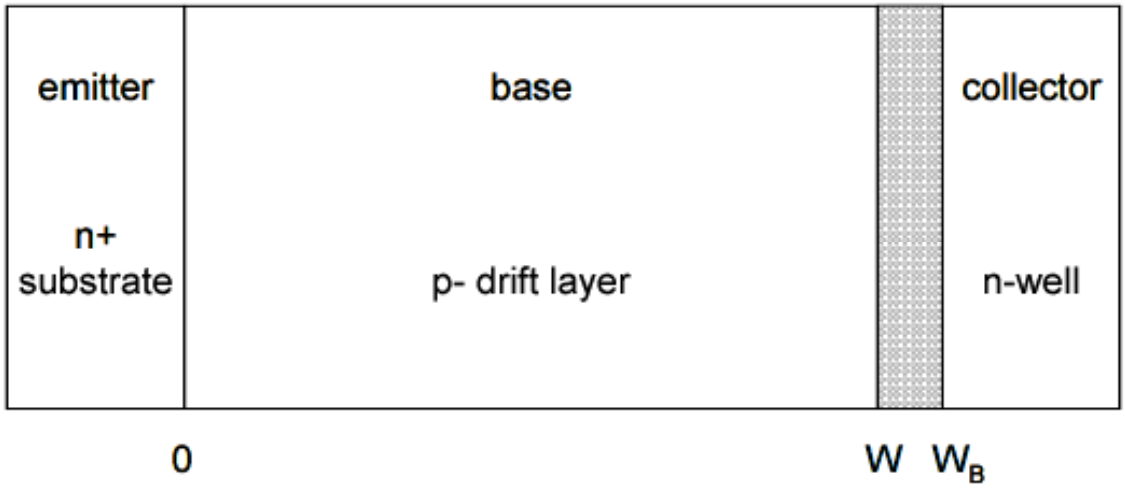


Fig. 3.15 Schematic for the BJT part of a P-IGBT. The shaded region is the depletion region at the reverse biased BC junction.

In the lightly doped drift region, we assume high-level injection and quasi-neutrality. Therefore, in the base of the BJT shown in Fig. 3.15:

$$n = n_0 + \Delta n \approx \Delta n \tag{3.15}$$

$$p = p_0 + \Delta p \approx \Delta p \tag{3.16}$$

$$n = p \tag{3.17}$$

Ambipolar lifetime, ambipolar diffusion coefficient, and ambipolar diffusion length are defined in equation (2.11), (2.9), and (2.8), respectively. b is the ratio of electron mobility to hole mobility.

$$b = \frac{\mu_N}{\mu_P} \tag{3.18}$$

The ambipolar diffusion equation in the wide base region is:

$$\frac{\partial \Delta n}{\partial t} = D_A \frac{\partial^2 \Delta n}{\partial x^2} - \frac{\Delta n}{\tau_A} \tag{3.19}$$

Under steady-state conditions,

$$\frac{\partial^2 \Delta n}{\partial x^2} = \frac{\Delta n}{L_A{}^2} \tag{3.20}$$

The general solution to the above equation is

$$\Delta n(x) = Ae^{-x/L_A} + Be^{x/L_A} \tag{3.21}$$

Set boundary conditions at x = 0 and x = W,

$$\Delta n(0) = A + B \tag{3.22}$$

$$\Delta n(W) = Ae^{-W/L_A} + Be^{W/L_A} \tag{3.23}$$

Δn(0) is determined by the total current injection from the cathode, and Δn(W) is essentially zero because the BC junction is reverse biased. After applying the boundary conditions to the general solution, we have:

$$\Delta n(x) = \left[\frac{\Delta n(0)e^{W/L_A} - \Delta n(W)}{e^{W/L_A} - e^{-W/L_A}}\right]e^{-x/L_A} + \left[\frac{\Delta n(W) - \Delta n(0)e^{-W/L_A}}{e^{W/L_A} - e^{-W/L_A}}\right]e^{x/L_A} \tag{3.24}$$

Electron and hole currents in the drift region are generally described by the drift-diffusion equations [43]:

$$J_N = nq\mu_N\varepsilon + qD_N\frac{\partial n}{\partial x} \tag{3.25}$$

$$J_P = pq\mu_P\varepsilon - qD_P\frac{\partial p}{\partial x} \tag{3.26}$$

The electric field can be expressed in terms of J_P from equation (3.26). Then substitute ε into (3.25), and the electron current density is written as

$$J_N = bJ_P + bqD_P\frac{\partial p}{\partial x} + qD_N\frac{\partial n}{\partial x} \tag{3.27}$$

Define total current $J_T \equiv J_N + J_P$, then

$$J_N - bJ_P = J_N - bJ_P - bJ_N + bJ_N = bqD_P\frac{\partial p}{\partial x} + qD_N\frac{\partial n}{\partial x} \tag{3.28}$$

$$J_N(x) = \frac{b}{1+b}J_T + \frac{2bD_P}{1+b}q\frac{\partial n}{\partial x} = \frac{b}{1+b}J_T + qD_A\frac{\partial n}{\partial x} \tag{3.29}$$

where $D_A = \dfrac{2D_N D_P}{D_N + D_P}$, and $\dfrac{D_N}{D_P} = \dfrac{\mu_N}{\mu_P} = b$.

$$J_N(x) = \frac{b}{1+b}J_N(x) + \frac{b}{1+b}J_P(x) + qD_A\frac{\partial n}{\partial x} \tag{3.30}$$

At x = 0,

$$J_N(0) = bJ_P(0) - (1+b)\frac{qD_A}{L_A}\Delta n(0)\coth\left(\frac{W}{L_A}\right) \tag{3.31}$$

Substituting (3.31) into (3.29) yields:

$$J_N(x) = J_N(0) + \frac{qD_A\Delta n(0)}{L_A}\left[\coth\left(\frac{W}{L_A}\right) - \frac{\cosh\left(\frac{W-x}{L_A}\right)}{\sinh\left(\frac{W}{L_A}\right)}\right] \tag{3.32}$$

Similarly, we have the following expression for hole current density as a function of distance:

$$J_P(x) = \frac{J_N(0)}{b} + \frac{qD_A\Delta n(0)}{L_A}\left[\frac{\coth\left(\frac{W}{L_A}\right)}{b} + \frac{\cosh\left(\frac{W-x}{L_A}\right)}{\sinh\left(\frac{W}{L_A}\right)}\right] \tag{3.33}$$

Define $J_{N0} \equiv q\frac{n_i^2}{N_{AB}}\frac{D_{NB}}{L_{NB}}$, where N_{AB}, D_{NB}, L_{NB} are the doping concentration, diffusion coefficient and diffusion length in the base. Considering the electron current at the forward biased EB junction to be

$$J_N(0) = J_{N0}\exp\left(\frac{qV_A}{kT}\right) = J_{N0}\exp\left(\frac{F_N - F_P}{kT}\right) = J_{N0}\exp\left(\frac{F_N - E_i}{kT}\right)\exp\left(\frac{E_i - F_P}{kT}\right) \tag{3.34}$$

$$J_N(0) = J_{N0}\frac{n}{n_i}\frac{p}{n_i} \approx J_{N0}\frac{\Delta n\Delta p}{n_i^2} = J_{N0}\frac{\Delta n(0)^2}{n_i^2} = \frac{qD_{NB}}{N_{AB}L_{NB}}\Delta n(0)^2 \tag{3.35}$$

Finally, we can express $J_N(x)$ and $J_P(x)$ by $\Delta n(0)$ as in equation (3.36) and (3.37). If we fix the total current density $J_T = J_N(x) + J_P(x)$, we can solve for $\Delta n(0)$.

$$J_N(x) = \frac{qD_{NB}}{N_{AB}L_{NB}}\Delta n(0)^2 + \frac{qD_A}{L_A}\left[\coth\left(\frac{W}{L_A}\right) - \frac{\cosh\left(\frac{W-x}{L_A}\right)}{\sinh\left(\frac{W}{L_A}\right)}\right]\Delta n(0) \tag{3.36}$$

$$J_P(x) = \frac{qD_{NB}}{bN_{AB}L_{NB}}\Delta n(0)^2 + \frac{qD_A}{L_A}\left[\frac{\coth\left(\frac{W}{L_A}\right)}{b} + \frac{\cosh\left(\frac{W-x}{L_A}\right)}{\sinh\left(\frac{W}{L_A}\right)}\right]\Delta n(0) \tag{3.37}$$

From equation (3.24), we know that

$$\Delta n(x) = \Delta n(0)\frac{\sinh\left[\frac{W-x}{L_A}\right]}{\sinh\left(\frac{W}{L_A}\right)} \tag{3.38}$$

Hefner et al. have developed an analytical solution for the voltage drop across the drift region of an IGBT [55]:

$$V_M = \frac{J_T W}{(1+b)\mu_P q n_{eff}} - \frac{D_A}{\mu_P}\ln\left[\frac{\Delta n(0) + N_{epi}}{N_{epi}}\right] \tag{3.39}$$

where N_{epi} is the doping of the drift region and n_{eff} is defined as [55]:

$$\frac{1}{n_{eff}} \equiv \frac{1}{W}\int_0^W \frac{dx}{N_{epi} + \Delta n(x)} \tag{3.40}$$

Therefore, by knowing the total current, we can solve Δn(0), and eventually solve the voltage across the drift region V_M analytically. This analytically solution is entirely one-dimensional. It can be used as a guideline for device design and optimization. For more accurate solutions, two-dimensional numerical simulation is used.

3.1.2.3 Optimizing the P-IGBT design using numerical simulation

3.1.2.3.1 Device structure and physical models in the simulation

Medici™ numerical simulation is used extensively for optimizing the device design. The device structure in the simulation is shown in Fig. 3.16. The algorithm used by Medici™ is to solve the Poisson's equation and continuity equations for electrons and holes self-consistently for the electrostatic potential (ψ), and electron (n) and hole (p) concentrations.

Poisson's equation: $$\varepsilon\nabla^2\Psi = -q\left(p - n + N_D^+ - N_A^-\right) - \rho_S \quad (3.41)$$

Electron continuity equation: $$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - U_n \quad (3.42)$$

Hole continuity equation: $$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \bullet J_p - U_p \quad (3.43)$$

where n, p are electron, hole concentrations; N_D^+, N_A^- are ionized impurity concentrations; Un, Up are net electron and hole recombination rate; ψ is the intrinsic Fermi potential; ρ_S is the surface charge density, and ε is the dielectric constant of the semiconductor.

The following physical models [56] are employed in solving the above three equations self-consistently.

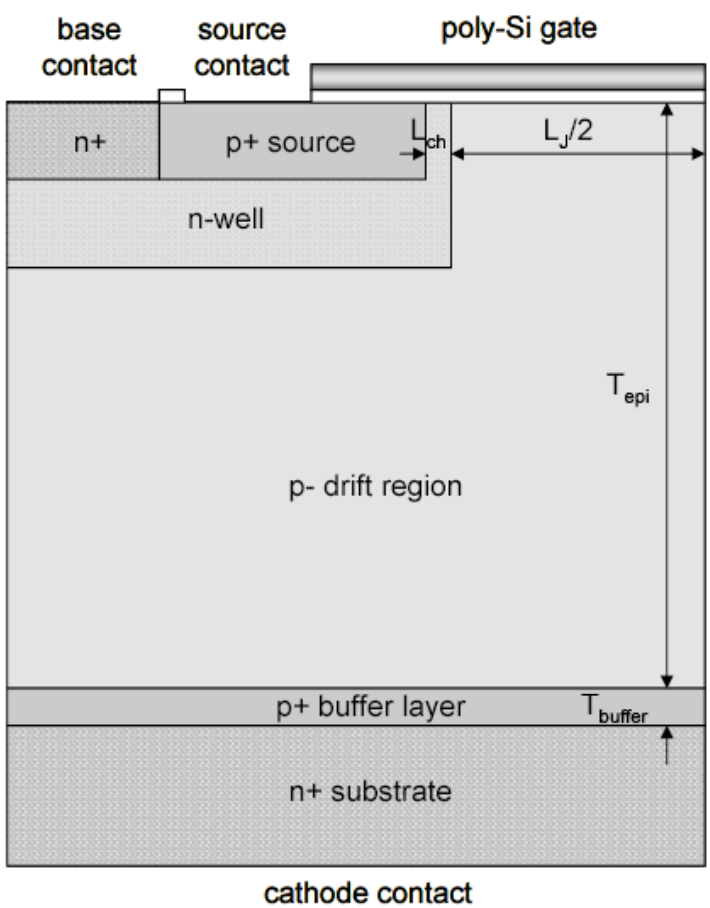


Fig. 3.16 Structure of the P-IGBT in Medici™ simulation.

For electron-hole recombination, there are three kinds of recombination supported by Medici™: Shockley-Read-Hall (SRH), Auger, and direct recombination. Note that all the parameters in bold capital letters are quantities specified by input statement.

$$U_{SRH} = \frac{pn - n_{ie}^{2}}{\tau_p \left[n + n_{ie} \exp\left(\frac{ETRAP}{kT} \right) \right] + \tau_n \left[p + n_{ie} \exp\left(\frac{-ETRAP}{kT} \right) \right]} \tag{3.44}$$

$$U_{dir} = C.DIRECT(np - n_{ie}^{2}) \tag{3.45}$$

$$U_{Auger} = AUGN(pn^2 - nn_{ie}^{2}) + AUGP(np^2 - pn_{ie}^{2}) \tag{3.46}$$

where **ETRAP** is the difference between trap energy and intrinsic Fermi energy, **C.DIRECT** is the band-to-band recombination coefficient, and **AUGN**, **AUGP** are Auger recombination constants. n_{ie} is the effective intrinsic concentration, and τ_n, τ_p are the electron, hole lifetimes.

An analytic mobility model is specified for the mobility dependence on doping concentrations and temperature. These are given by

$$\mu_{n0} = MUN.MIN + \frac{MUN.MAX \left(\frac{T}{300} \right)^{NUN} - MUN.MIN}{1 + \left(\frac{T}{300} \right)^{XIN} \left(\frac{N_{total}(x,y)}{NREFN} \right)^{ALPHAN}} \tag{3.47}$$

$N_{total}(x,y)$ is the local net impurity concentration; **MUN.MIN** and **MUN.MAX** are the minimum and maximum electron mobilities; **NUN** and **XIN** are the temperature dependent exponents for the semiconductor; **ALPHAN** is the doping dependent exponent; and **NREFN** is the reference electron concentration. A similar equation is used for holes.

For MOS devices, the inversion channel mobility is different from the bulk mobility. The following enhanced surface mobility model is specified for electron surface mobility.

$$\frac{1}{\mu_{eff,n}} = \frac{1}{MUN1.SM}\left(\frac{E_{eff\perp}}{10^6}\right)^{EXN1.SM} + \frac{1}{MUN2.SM}\left(\frac{E_{eff\perp}}{10^6}\right)^{EXN2.SM} + \frac{1}{MUN3.SM}\left(\frac{N_B}{10^{18}}\right)\left(\frac{10^{12}}{N_{inv}}\right)^{EXN3.SM} \tag{3.48}$$

$E_{eff\perp}$ is the field perpendicular to the (0001) surface. In our simulation, we specify the parameters as follows to match the surface mobility with the reported experimental results [30]. **EXN1.SM** = 1; **EXN2.SM** = 0; **EXN3.SM** = 0; **MUN1.SM** = 30; **MUN2.SM** = 10^{20}; **MUN3.SM** = 10^{20}. The effective electron surface mobility becomes

$$\mu_{eff,n} = MUN1.SM\left(\frac{10^6}{E_{eff\perp}}\right) = 30\left(\frac{10^6}{E_{eff\perp}}\right) cm^2/Vs \tag{3.49}$$

The effective electron surface mobility is 30 cm^2/Vs at a semiconductor surface field (perpendicular to surface) of 10^6 V/cm, and decreases with the field. Similarly, the hole surface mobility is given by

$$\mu_{eff,p} = MUP1.SM\left(\frac{10^6}{E_{eff\perp}}\right) = 7.5\left(\frac{10^6}{E_{eff\perp}}\right) cm^2/Vs \tag{3.50}$$

The effective hole mobility at 10^6 V/cm surface field is assumed to be 7.5 cm^2/V-s. This assumption is based on the report that 6H-SiC n-channel and p-channel MOSFETs with the same structure built on the same wafer have approximately 4:1 current ratio at same (V_g-V_{th}) [47]. We will experimentally measure the inversion channel hole mobility to verify this assumption.

In the bulk semiconductor under high field, the Caughey-Thomas expression [57] is used for high field mobility.

$$\mu_n = \frac{\mu_{S,n}}{\left[1 + \left(\frac{\mu_{S,n} E_{\parallel}}{v_n^{sat}}\right)^{BETAN}\right]^{1/BETAN}} \tag{3.51}$$

where $\mu_{S,n}$ is the low field mobility given by (3.47) and v_n^{sat} is the saturation velocity for electrons. v_n^{sat} at room temperature is 2.2×10^7 cm/s for 4H-SiC [58]. $E_{||}$ is the field in the direction of current flow. Holes have a similar field-dependent mobility expression. The saturation velocity for holes at room temperature is 9.5×10^6 cm/s [59].

Fermi-Dirac statistics are used for the distribution of electrons and holes. Incomplete ionization of dopants and impact ionization under high field is included in the simulation. Minority carrier lifetime is a constant and can be specified by users. Anisotropy of electron mobility is also included.

3.1.2.3.2 Optimizing the drift layer for 20 kV P-IGBT

The drift layer is used to block the high voltage in the off-state, and the voltage across the drift layer is dominant for the on-state. Therefore, optimizing the drift layer is critical for the performance of IGBTs. We will discuss the influence of drift layer ambipolar lifetime (τ_A), thickness (T_{epi}), and doping (N_{epi}) on the performance of P-IGBTs.

As discussed earlier, the blocking voltage depends on drift layer doping and thickness. To design a 20 kV P-IGBT, we set theoretical blocking voltage of 25 kV and assume 80% of the theoretical blocking voltage can be achieved. Figure 3.17 shows the blocking voltage vs. drift layer doping for different drift layer thickness. The thinnest drift layer to block 25 kV is 166 μm. Anything thinner than 166 μm cannot block 25 kV no matter what doping concentration it has. Of course, drift layers thicker than 166 μm can block 25 kV.

We know from the figure of merit of IGBTs that high V_B and low V_{on} are desired for maximum FOM. The on-state voltage drop (V_{on}) is the sum of voltage across the intrinsic MOSFET part (V_{intr}), voltage across the forward biased junction ($V_J \approx 3$ V), and the voltage across the drift region (V_M). The task is to minimize V_M by optimizing τ_A, T_{epi}, and N_{epi} of the drift layer.

Figure 3.18 shows the voltage across the drift layer of a P-IGBT with different ambipolar lifetime and drift layer thickness. The drift layer doping is 2×10^{14} cm^{-3} and the total current density is fixed at 30 A/cm^2. As shown in the figure, ambipolar lifetime is

indeed a very important parameter determining the voltage across the drift region. This is because the ambipolar diffusion length (L_A), which indicates the extent of conductivity modulation, is directly related to ambipolar lifetime ($L_A = \sqrt{D_A \tau_A}$). For thicker drift layers, the dependence on lifetime is stronger. Therefore, it is more important to have long lifetime for IGBTs blocking 10 kV and above. For the 20 kV P-IGBTs, the minimum requirement on ambipolar lifetime is 0.5 μs. Otherwise, the P-IGBTs will lose the advantage over MOSFETs. Fortunately, it has been reported that 4H-SiC ambipolar lifetime can reach 1μs on 80% of wafer area by using "hot-wall" CVD technique during wafer growth [49].

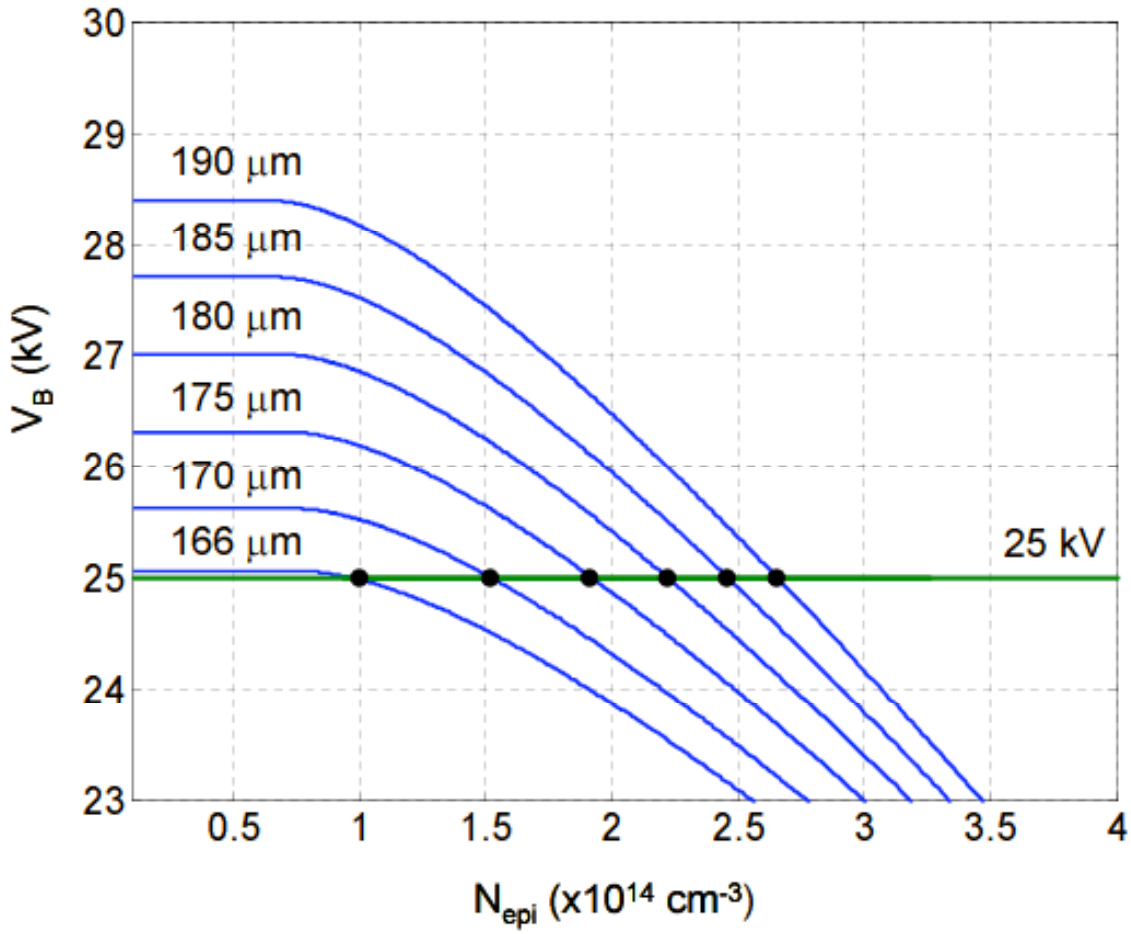


Fig. 3.17 Drift layer blocking voltage vs. drift layer doping of a P-IGBT. The result is given by Matlab calculation. The intersection points of the curves on 25 kV line are chosen for numerical simulation to determine the optimum design.

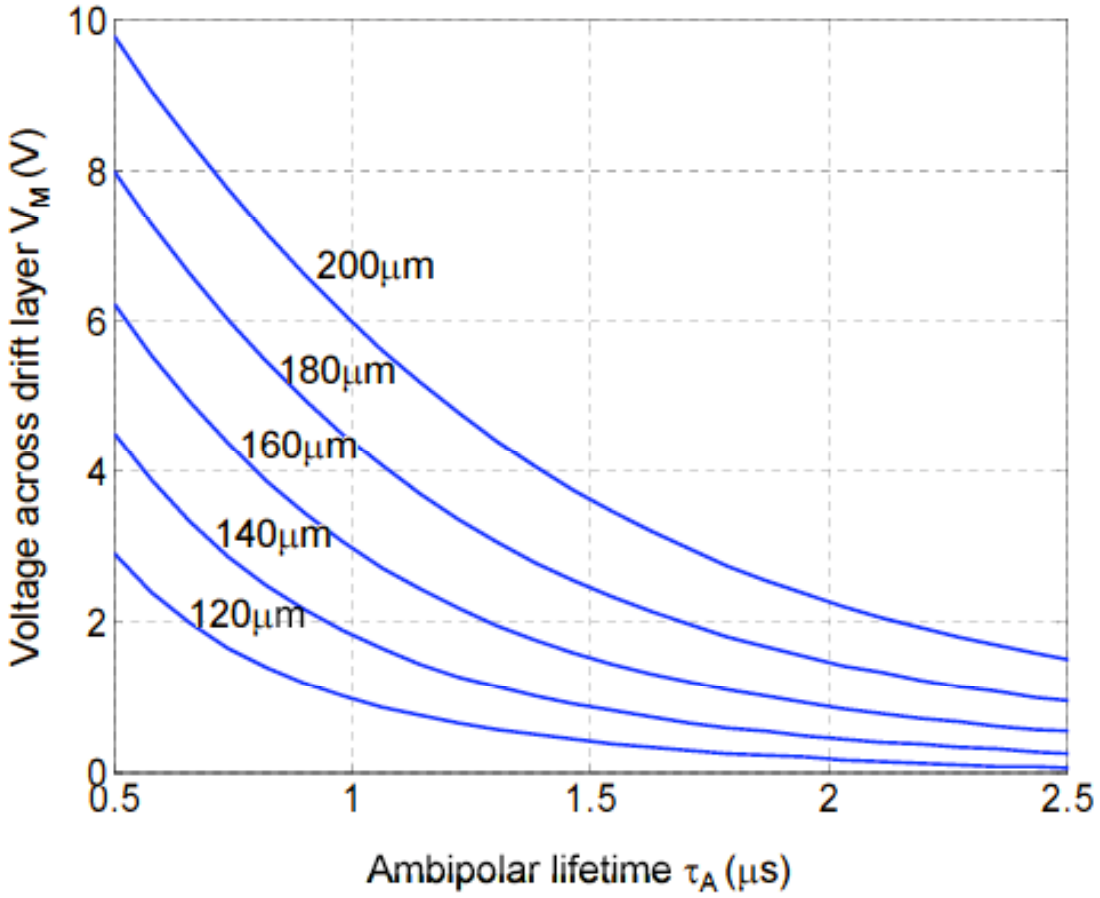


Fig. 3.18 On-state voltage drop across the drift layer vs. ambipolar lifetime of a P-IGBT. J_{total} = 30 A/cm^2, and N_{epi} = 2x10^{14} cm^{-3}. The result is given by Matlab calculation [55].

Another factor on V_M is the drift layer thickness (T_{epi}). The reason is obvious that the thicker the drift layer is, the harder it is for the injected carriers to diffuse through the entire drift layer. Figure 3.19 shows V_M as a function of T_{epi} at a total current of 30 A/cm^2. Given the blocking voltage, the drift layer should be as thin as possible to keep a low on-state voltage drop.

Figure 3.19 shows that V_M of a P-IGBT is different for different drift layer doping. Intuitively, the drift layer resistance should be independent of the background doping, because the drift layer should be flooded with excess carriers. This is true for PiN diodes, since electrons and holes are injected from both ends [60]. A more careful examination of the P-IGBT drift layer under on-state operation reveals that the n-well/p- junction is reverse biased, which lowers the excess carrier concentration essentially to zero in the top part of the drift region, as illustrated in Fig. 3.20. The top part of the drift layer becomes much more resistive than the rest of the drift layer and most of the voltage drop occurs in this region [55]. Consequently, the background doping provides a significant portion of free carriers in this region. Figure 3.21 show V_M as a function of drift layer doping. In order to achieve a low on-state voltage drop, the drift layer doping should be as high as possible, given the desired blocking voltage is satisfied.

Among the variables of the drift layer, ambipolar lifetime is determined by crystal growth technology and cannot be changed in the process. Therefore, τ_A is more of a parameter than a variable. However, T_{epi} and N_{epi} are very much controllable. We will run numerical simulation to find the most suitable (T_{epi}, N_{epi}) pairs for maximizing the FOM of 20 kV P-IGBTs.

As mentioned previously, the target theoretical blocking voltage is 25 kV for a 20 kV P-IGBT design. As shown in Fig. 3.17, the drift layer has to be at least 166 μm to block 25 kV. In order to achieve the lowest V_M, a low T_{epi} and a high N_{epi} are favorable. Therefore, only the intersection points on the 25 kV horizontal line should be considered for optimum design. Since these intersection points have competing T_{epi} and N_{epi}, it is necessary to use numerical simulation to find the (T_{epi}, N_{epi}) pair that provides the lowest on-state voltage drop. The simulation results for the total on-state voltage drop across the

device for these design points are listed in Table 3.3. The optimum drift layer thickness and doping for a 25 kV P-IGBT are 175 μm, $2x10^{14}$ cm^{-3}.

Table 3.3 On-state voltage drop for 25 kV P-IGBTs with different (T_{epi}, N_{epi}) at τ_A = 0.5 μs

T_{epi} (μm)	N_{epi} (cm^{-3})	V_{on} (V)
166	$1.0x10^{14}$	10.6
170	$1.5x10^{14}$	10.0
175	$2.0x10^{14}$	9.7
180	$2.2x10^{14}$	9.8
185	$2.5x10^{14}$	9.8
190	$2.7x10^{14}$	9.9

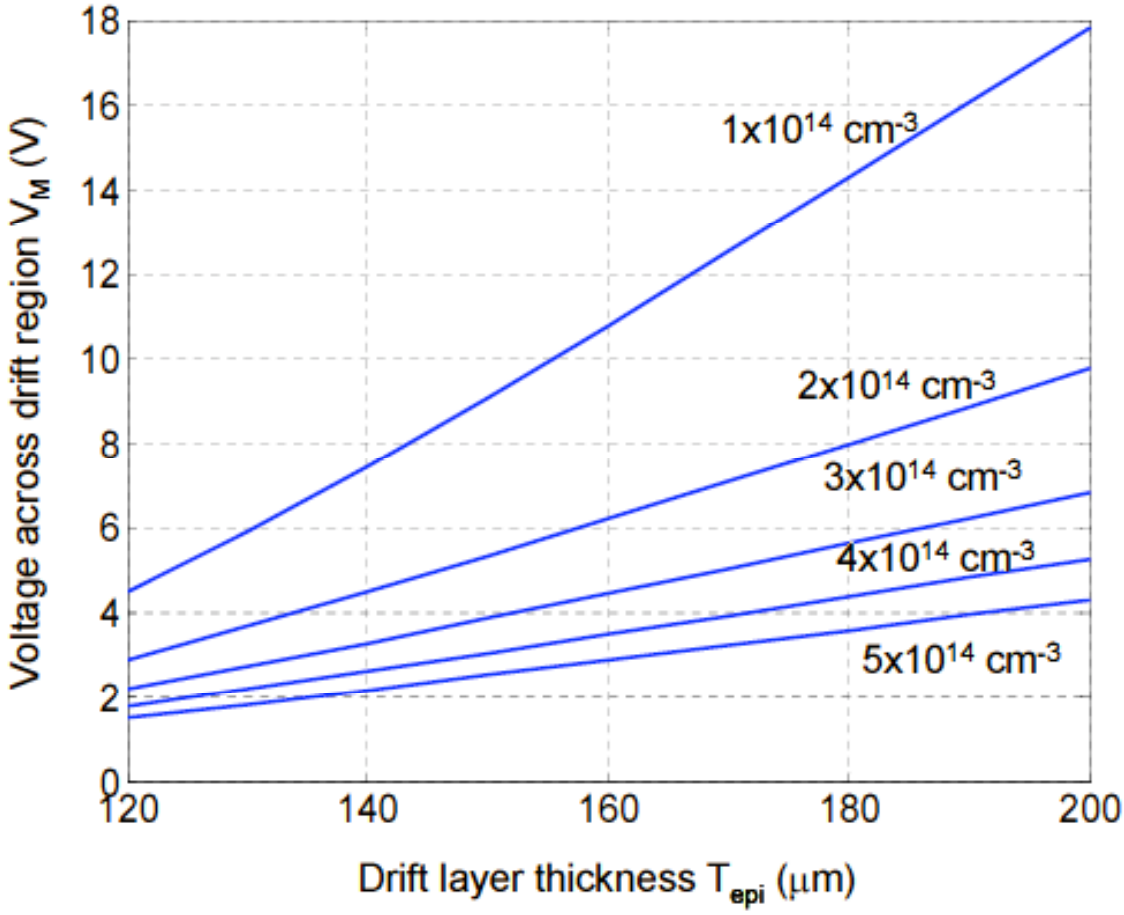


Fig. 3.19 On-state voltage drop across the drift region vs. drift layer thickness of a P-IGBT. J_{total} = 30 A/cm^2, and τ_A = 0.5 μs. The result is given by Matlab calculation [55].

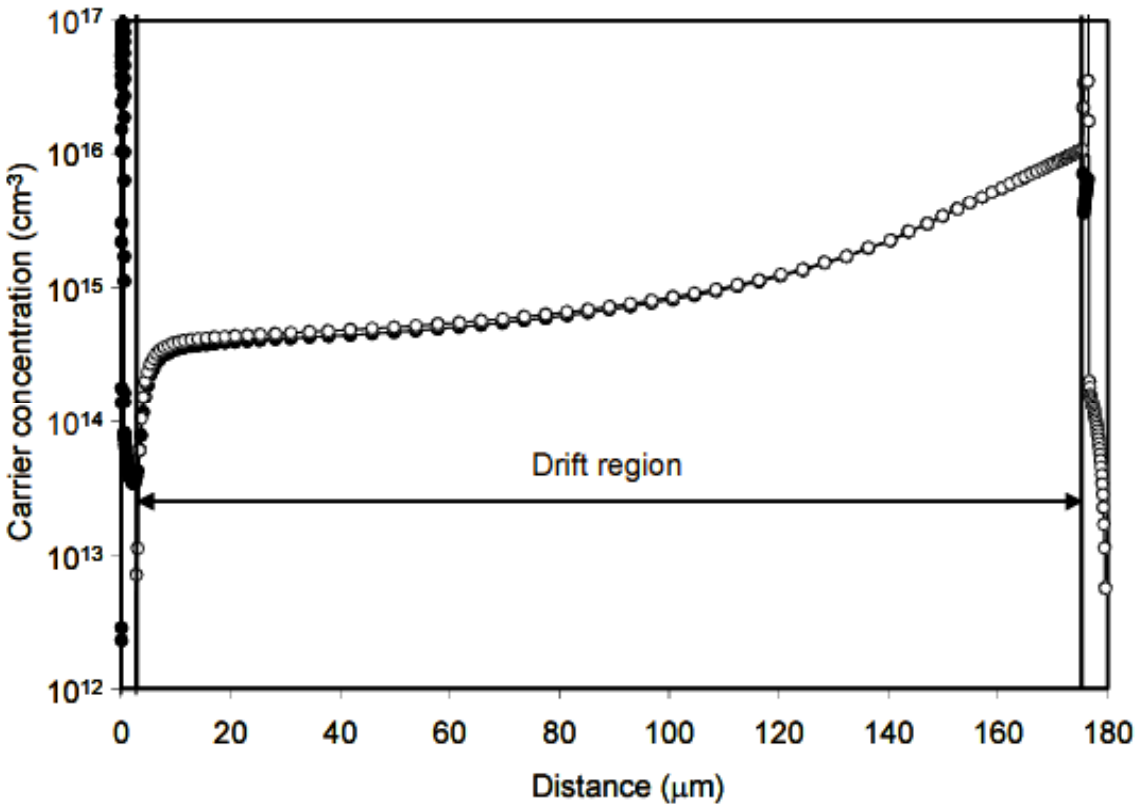


Fig. 3.20 Electron and hole concentration across a 20 kV P-IGBT under on-state operation. Solid circles and open circles represent electron and hole concentration, respectively. The drift region is between the vertical lines. The region to the left side of the drift region is n-well, and the region to the right side of the drift region is p+ buffer and n+ substrate. $N_{epi} = 2x10^{14}$ cm^{-3}, τ_A = *0.5 μs, and* J_{total} = *30 A/cm*^{2}. *The result is given by Medici*^{TM} *numerical simulation.*

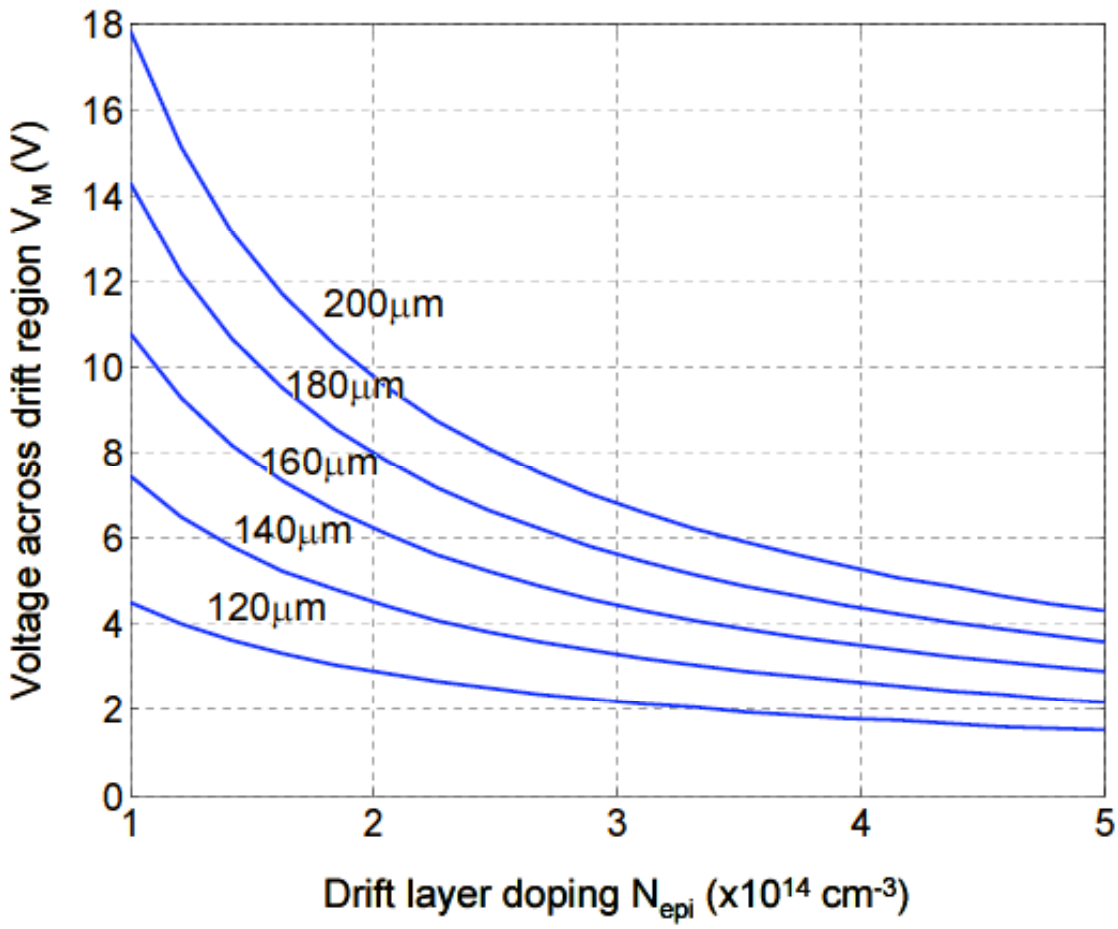


Fig. 3.21 On-state voltage drop across the drift region vs. drift layer doping of a P-IGBT. J_{total} = 30 A/cm^2, and τ_A = 0.5 μs. The result is given by Matlab calculation [55].

3.1.2.4 Temperature dependence of SiC MOSFETs and IGBTs

The temperature dependence is important for power devices because these devices carry high voltage and high current, therefore, high power dissipation. The wide bandgap and high intrinsic temperature of SiC allow SiC power transistors to operate at a much high temperature than Si power transistors. However, for SiC power MOSFETs, bulk mobility decreases with temperature in power law form [41, 61], which causes degradation of the high temperature performances.

For IGBTs, the critical material parameter is the ambipolar diffusion length (L_A), which depends on both bulk mobility and ambipolar lifetime as follows.

$$L_A = \sqrt{D_A \tau_A} = \sqrt{\frac{kT}{q} \frac{2\mu_N \mu_P}{\mu_N + \mu_P} \tau_A} \tag{3.52}$$

According to the latest reports on 4H-SiC mobility and lifetime [41, 42, 61], L_A is plotted against temperature in Fig. 3.22. According to the plot, the ambipolar diffusion length increases with temperature, which indicates that the on-state performance of the IGBTs should be better at high temperature than room temperature.

Figure 3.23 shows the simulated 20 kV P-IGBT and 20 kV MOSFET on-state I-V characteristics at room temperature and 177°C. The MOSFET shows significant increase in resistance as predicted. The intersection point of the P-IGBT's I-V curve with the 300 W/cm^2 power limit line does not change much at high temperature. But for a higher cathode voltage, the P-IGBT does show higher current density at 177°C than at room temperature. Above all, the maximum current density under the 300 W/cm^2 limit of the 20 kV P-IGBT is 1.24x and 2x higher than that of the 20 kV MOSFET at room temperature and 177°C, respectively. This superior high temperature performance of IGBTs is particularly significant because power devices will heat up if they continuously operate under the package power dissipation limit.

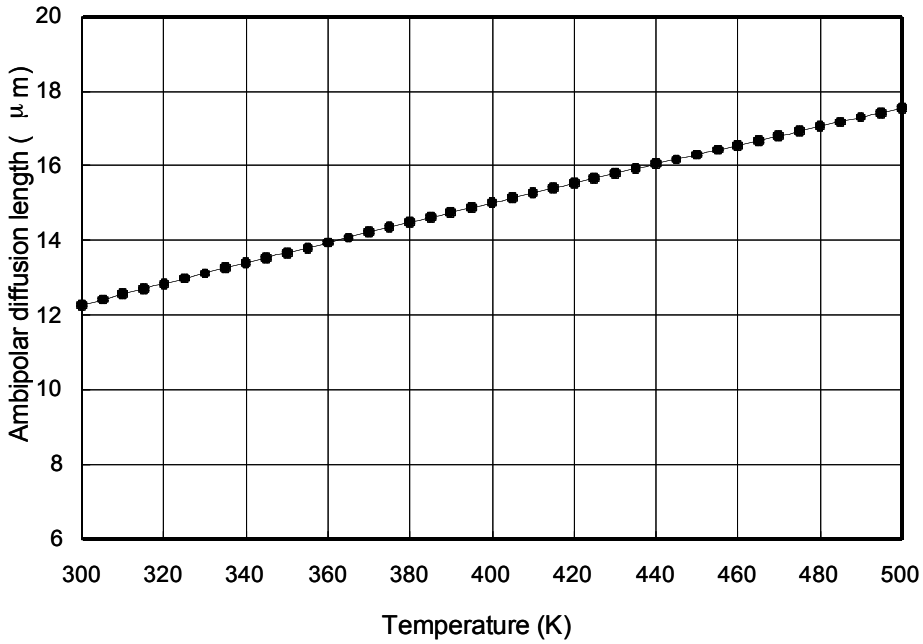


Fig. 3.22 Temperature dependence of 4H-SiC ambipolar lifetime [41, 42, 61].

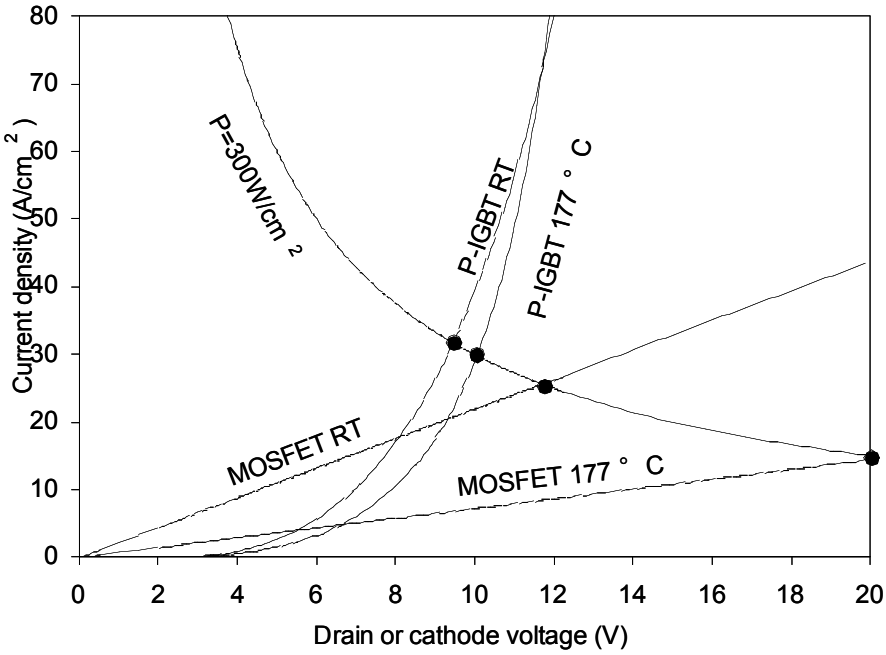


Fig. 3.23 Current-voltage characteristics of a theoretical 20 kV p-IGBT and a 20 kV n-MOSFET at room temperature and 177 °C. V_g = 20 V (E_{ox} = 4 MV/cm). The room temperature ambipolar lifetime is assumed to be 458 ns. Temperature dependent mobility and lifetime models refer to [41, 42, 61].

3.1.2.3.3 JFET length and p+ buffer layer

JFET length is the length between two adjacent implanted n-wells indicated by L_J in Fig. 3.16. The JFET region is depleted from the n-wells when the n-well/p- junction is reverse biased as the drain voltage becomes negative. This leads to a narrower current path for holes to flow from the MOS channel to the drift layer, and consequently, a higher JFET resistance. Numerical simulations of P-IGBTs with different L_J show that the on-voltage starts to increase rapidly when L_J is less than 10 μm as shown in Fig 3.24. A wider JFET region leads to a lower JFET resistance. But it increases the total device area, which lowers the on-state current density of the device. A wider L_J also results in a higher field in the oxide in the blocking state, and this can limit the maximum blocking voltage. Considering all the above conditions, we choose the optimum JFET length to be 12 μm.

Inserting a p+ buffer layer between the p- drift layer and the n+ substrate allows the drift region to be punched through in the blocking state. This punch-through design effectively improves the blocking voltage of the IGBT by nearly two times and helps prevent the open base BJT effect. In order to prevent the depletion region to reach n+ substrate in the off state, the following condition has to be met for the p+ buffer layer:

$$N_{buffer} t_{buffer} \geq \frac{\varepsilon_S E_{cr}}{q} = 1.34 \times 10^{13}\, cm^{-2} \tag{3.53}$$

where N_{buffer} is the buffer layer doping, t_{buffer} is the buffer layer thickness.

The p+ buffer slightly lowers the electron injection into the drift layer for on-state, because the ambipolar diffusion length in the buffer layer is much shorter than in the drift layer. If the buffer layer is too thick, the electron recombination in the buffer layer will be too strong, such that the conductivity modulation in the drift layer cannot be achieved. The estimated $L_{A,buffer}$ is at least 1.7 μm (assuming $\tau_{A,buffer} \geq 10$ ns).

Simulations are carried out to optimize the buffer layer thickness and doping. The results show that for $N_{buffer} = 10^{18}$ cm^{-3} and $t_{buffer} = 0.2$ μm, the extra on-voltage drop due to the buffer layer is small and almost constant for $\tau_{A,buffer}$ 10 ns ~ 200 ns. Therefore, we can choose this p+ buffer specification without compromising the on-state performance.

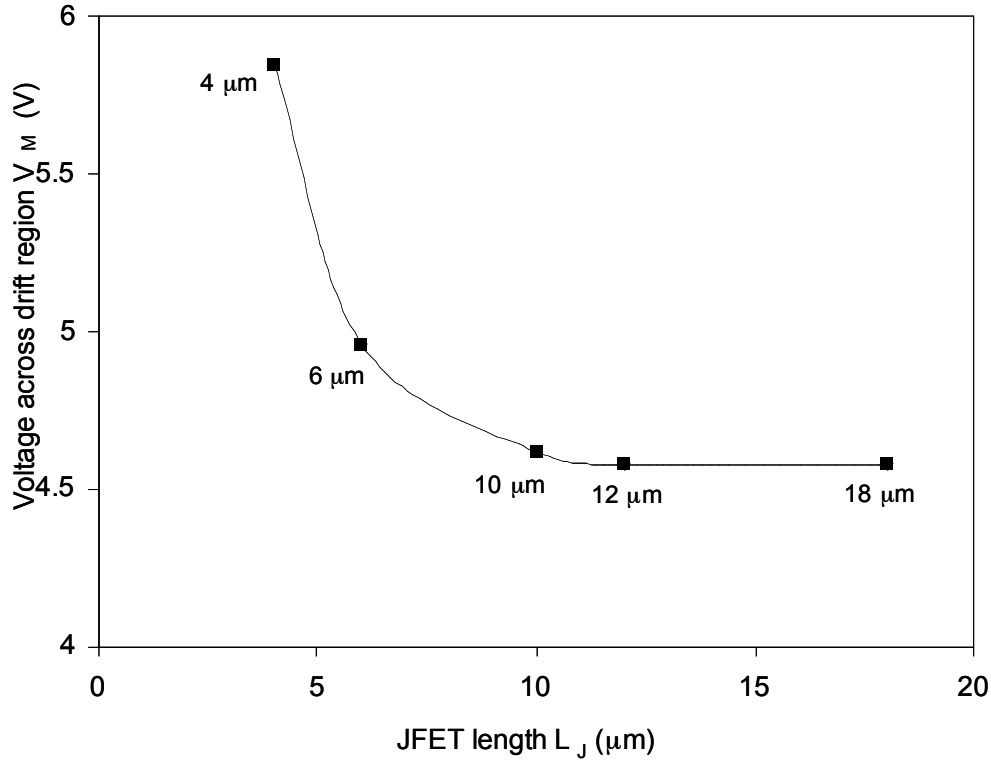


Fig. 3.24 On-state voltage drop across the drift region of a P-IGBT for different JFET length. J_{total} = 100 A/cm^2, T_{epi} = 85 μm, N_{epi} = 8x10^{14} cm^{-3}, τ_A = 1 μs.

3.1.3 Fabrication of Self-Aligned P-Channel IGBTS

3.1.3.1 Structure of the experimental devices

In the previous section, we discuss optimization of the 20 kV p-channel IGBTs. The summary of the optimum device is the following: T_{epi} = 175 μm, N_{epi} = 2x10^{14} cm^{-3}, $\tau_{A,epi} \approx$ 0.5 μs; T_{buffer} = 0.2 μm, N_{buffer} = 1x10^{18} cm^{-3}; L_J = 12 μm, $L_{ch} \approx$ 0.5 μm. We use these parameters for the experimental P-IGBTs.

Figure 3.25 shows the structure and dimensions of the experimental P-IGBTs. The minimum feature size is 4 μm and the alignment tolerance is 2 μm. The p+ source mask is the reference layer. All the other layers align to p+ source. The poly-Si gate overlaps 2 μm with the edge of p+ source, such that if the poly-Si gate is 2 μm misaligned to the left, the gate still has control over the channel. 4 μm spacing is left between the gate and source contact, such that for the worst case scenario, the gate does not short to

the source. The source contact and n-well contact are made 6 μm wide, so that at least 2 μm contact metals are left for the worst misalignment. The 0.5 μm short MOS channel is to be fabricated using a self-aligned short channel process [20]. The JFET length is 12 μm, as discussed in the previous chapter.

There are three types of P-IGBT designs as shown in Fig. 3.25. Type A is the one discussed above. It has a pitch size of 21.5 μm. Type B is similar to type A, except that the metal contacts are reduced to 4 μm wide, so that the pitch size is 18.5 μm. If the top MOSFET/JFET part limits the current, a smaller pitch size can provide higher current density. If the current is limited by the drift region, the effect of the pitch size is minimal. Type C P-IGBTs have separate source and n-well contacts. This design allows us to measure the source and base current separately. The pitch size of type C is 27.5 μm.

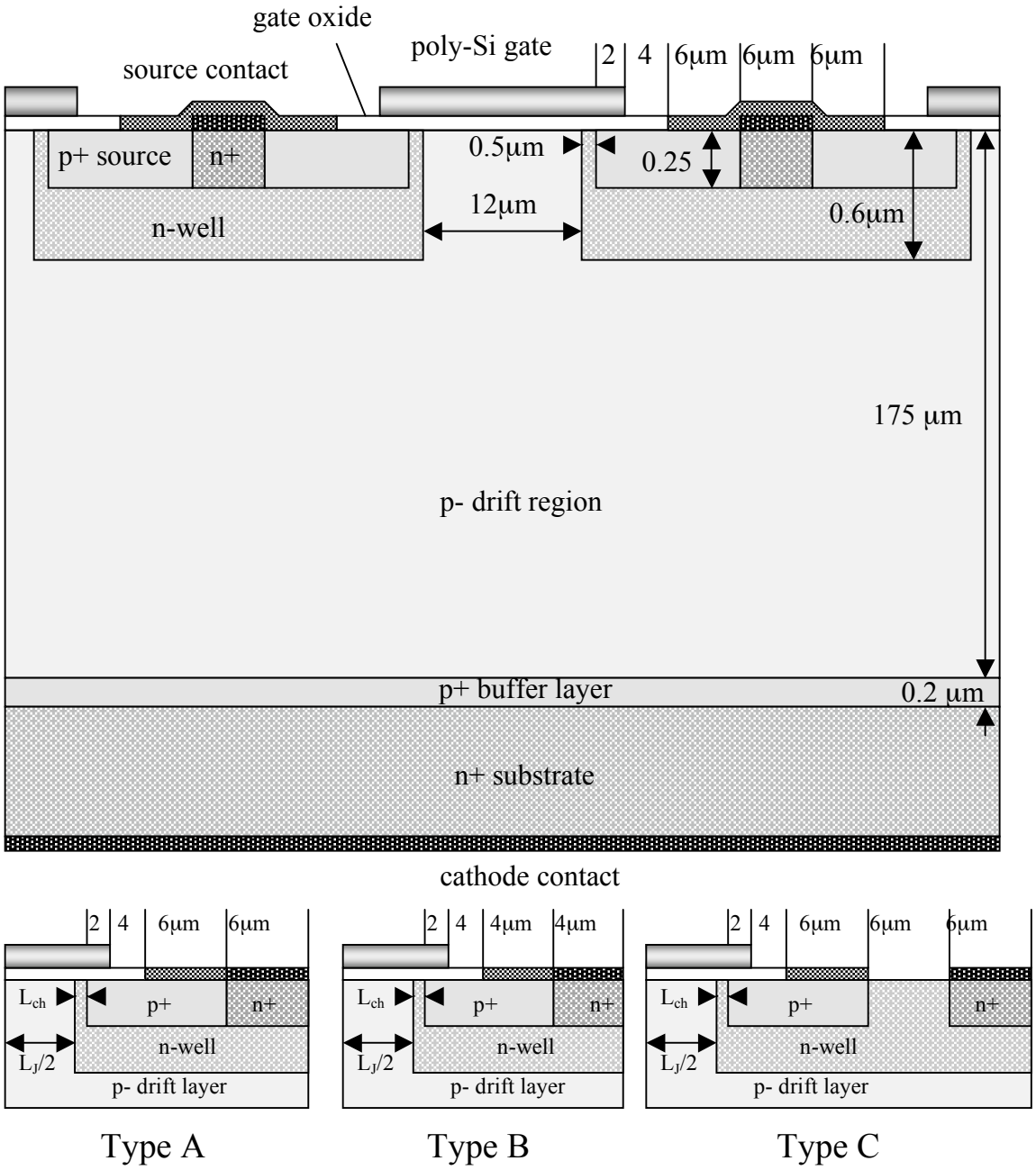


Fig. 3.25 Structure of the experimental P-IGBTs. All dimensions are in microns. The small schematics show three types of P-IGBT design. Pitch size for type A, B, and C are 21.5 μm, 18.5 μm, and 27.5 μm, respectively. L_J *= 12 μm and* $L_{ch} \approx 0.5$ *μm for all three types of P-IGBTs.*

The mask layout is designed using IC Station™ CAD software, by Mentor Graphics, Inc., 8005 SW Boeckman Rd, Wilsonville, OR 97070, USA. Figure 3.26 shows a die layout. The die is divided into 4 quadrants. Quadrant 1 has 1 mm x 1 mm IGBTs in type A and type B. Quadrant 2 has 1.5 mm x 1.5 mm IGBTs in type A and type B. Quadrant 3 has 0.5 mm x 0.5 mm IGBTs in type A and type B, three type C IGBTs, and testers (MOS capacitors, mobility MOSFETs). Quadrant 4 has one type A IGBT with floating field rings (FFRs) edge termination, one PiN diode with FFRs, and two type B IGBTs. There are a total of 66 rings around a device, and each ring is 3 μm wide with 3 μm spacing. All the IGBTs without FFRs have rounded corners to reduce the field crowding at the corners in the blocking state. We include MOS capacitors and mobility MOSFETs to study the gate oxide reliability and p-type inversion channel mobility.

Figure 3.27 shows the layout of a type C IGBT. Notice that the source contact and base contact fingers are separated, as well as the source and base contact pads. This allows us to measure the source and base current separately.

The masks are made on 0.09-inch thick quartz plates with chromium as reflective layers by Photronics, Inc., 15 Secor Rd / P.O. Box 5226, Brookfield, CT 06804, USA. The patterns are written by e-beam lithography with 0.25 μm addressing accuracy. There are a total of ten layers of masks.

1. N-well - liftoff mask
2. Registration - etch mask
3. P+ block - liftoff mask
4. N+ contact implant -liftoff mask
5. Micromasking - etch mask
6. Gate - etch mask
7. N+ contact - liftoff mask
8. P+ contact - liftoff mask
9. SOG window - etch mask
10. Top metal - liftoff mask

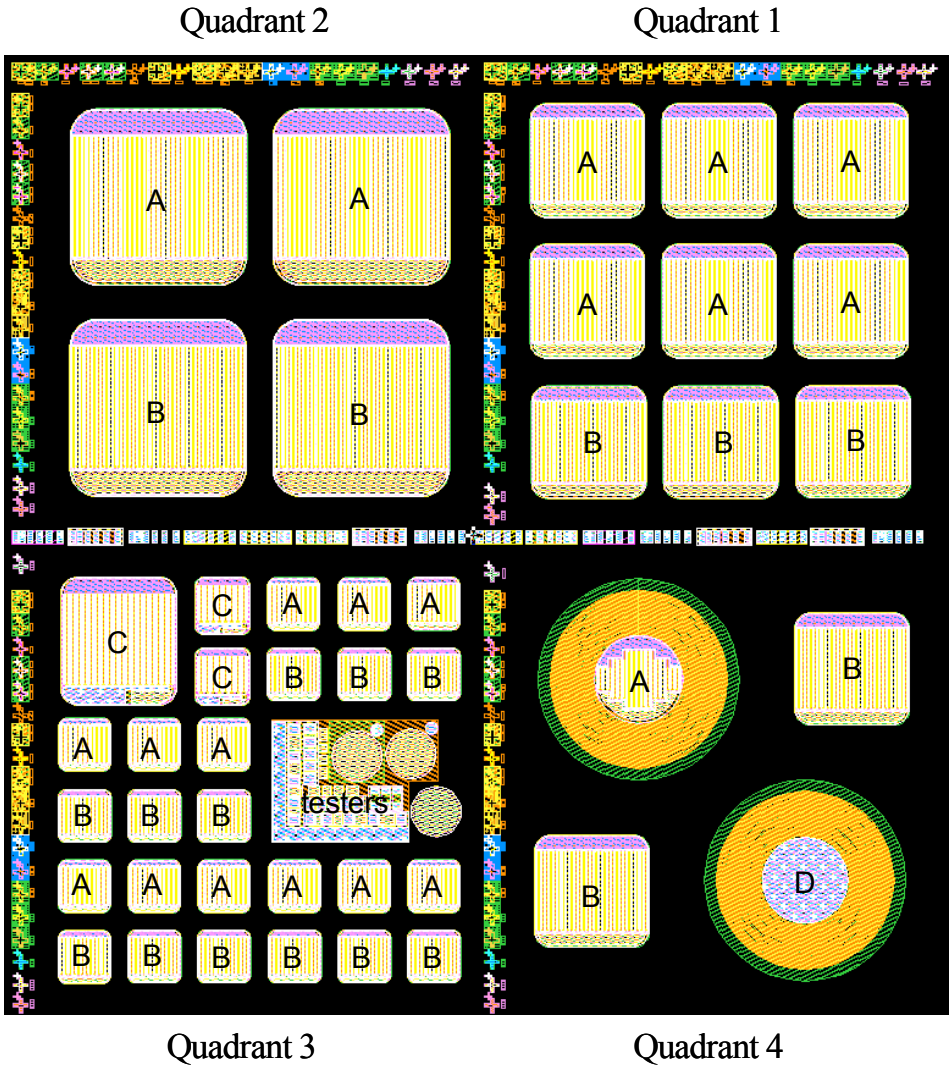


Fig. 3.26 The P-IGBT die layout. Devices are defined as following: A - IGBT type A, B - IGBT type B, C - IGBT type C; D - PiN diode. The TLMs are along the horizontal line. The rest of the long bars are alignment marks.

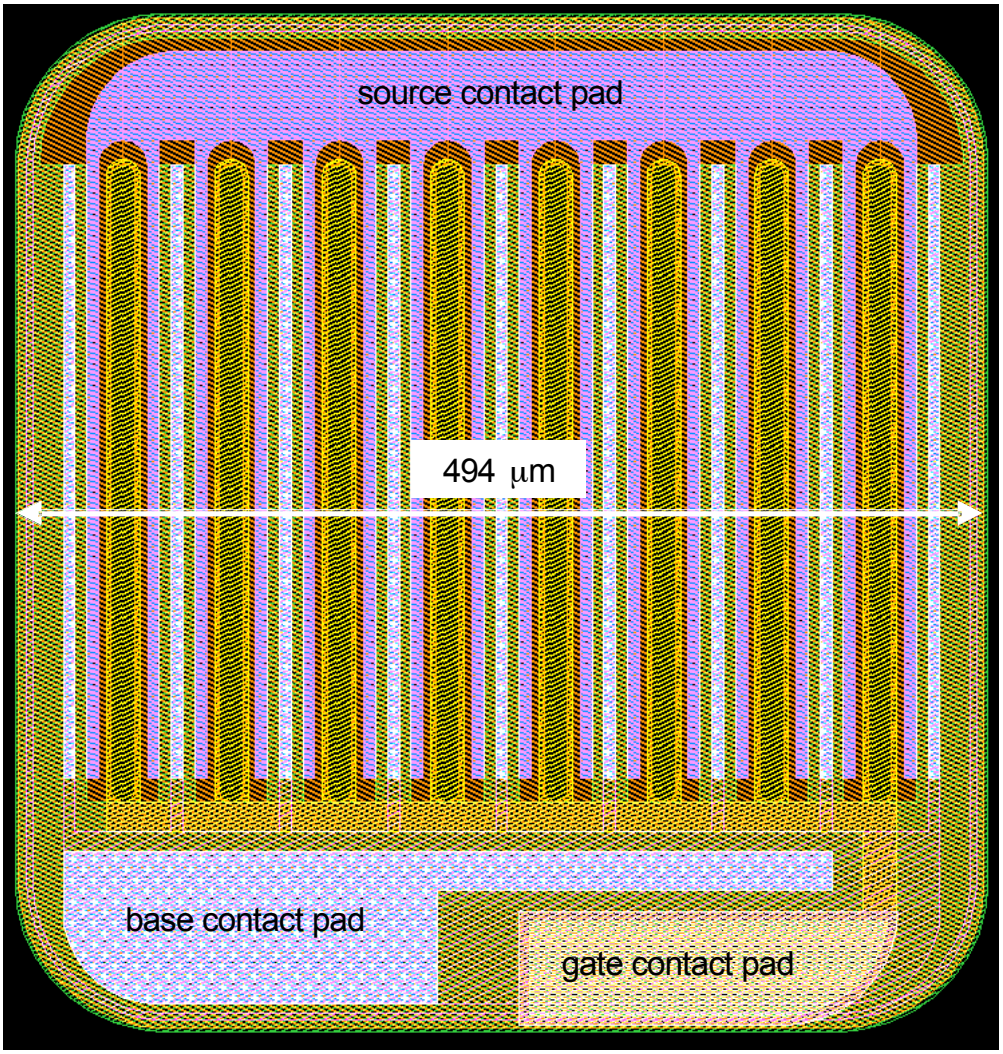


Fig. 3.27 Mask layout of a small type C IGBT.

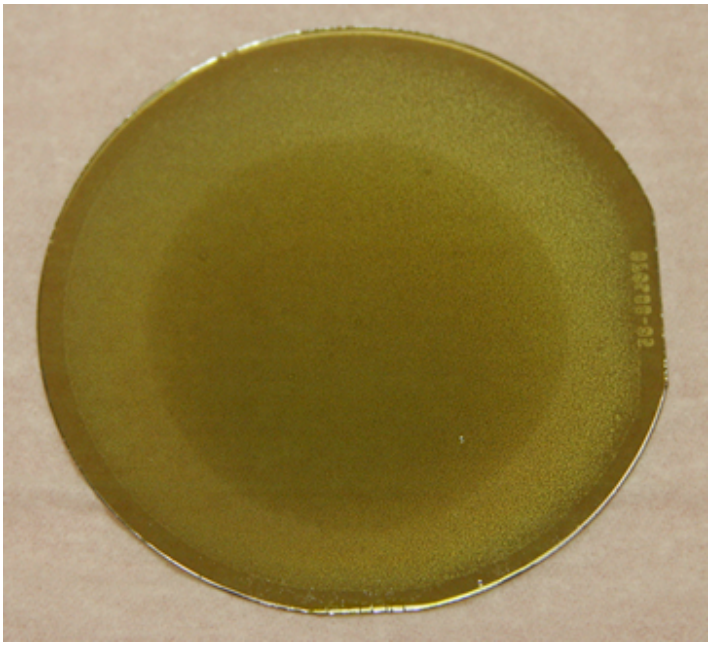
3.1.3.2 Fabrication process

3.1.3.2.1 Wafer specifications

The photo and schematic cross section of the starting wafer is shown in Fig. 3.28. Two epilayers (0.2 μm, $1x10^{18}$ cm^{-3} and 175 μm, $2x10^{14}cm^{-3}$) are grown on low basal plane dislocation (BPD) 3" n+ substrate, cut 8° off axis. The micropipe density is lower than 3 micropipes/cm^2. Fourier transform infrared (FTIR) measurement is performed to map the thickness of the epilayer. The drift layer thickness is within 175 ± 4 μm. The ambipolar lifetime across the wafer is measured by photoluminescence of the free-exciton emission. The RMS average of τ_A is 458 ns, with the maximum of 510 ns and minimum of 380 ns. The wafer specification is basically in good agreement with the optimum design.

3.1.3.2.2 N-well implantation

The 3" wafer is first cut into 4 quarters. These 4 quarters are processed separately to improve the chance of success. After the initial wafer cleaning, the wafer undergoes sacrificial oxidation at 1150°C for 1.5 hours in wet oxygen. A thin layer (~ 40 nm) of thermal oxide is grown on the top surface (Si-face) of the wafer. Then a uniform layer of 1.5 μm thick poly-Si is deposited on the wafer by low pressure chemical vapor deposition (LPCVD) at 600°C for 4 hours. The smoothness of the poly-Si is critical because it determines the smoothness of the channel region surface. A rough channel surface leads to lower channel mobility due to surface roughness scattering [16]. The wafer is then oxidized at 900°C in wet oxygen to form a thin layer of sacrificial oxide on top of the poly-Si. Liftoff lithography is performed using the n-well mask with AZ1518 positive photoresist. Ti (20 nm) and Ni (200 nm) are evaporated by e-beam evaporation and lifted off using airbrush or ultrasonic cleaner. A thick layer of AZ4620 photoresist is spun on, patterned, and hardbaked using the micro masking mask. This thick photoresist prevent micro masking (sputtering of Ni during the long RIE).



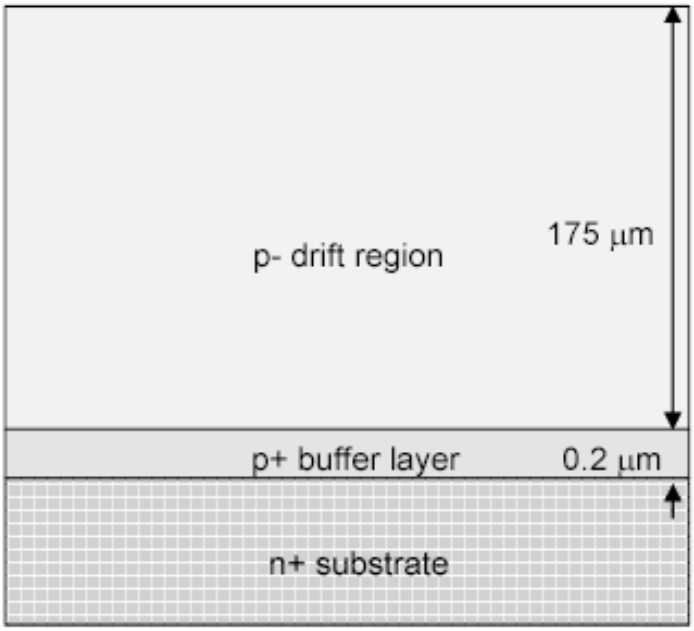


Fig. 3.28 Photo and schematic cross section of the initial 4H-SiC wafer.

The 1.5 μm poly-Si is patterned by RIE. It is crucial to do the RIE etching in several steps. After each step, the wafer is inspected under microscope to estimate the remaining etching time. After all the poly-Si is removed, the wafer should have a dark green color, as opposed to the gray or rainbow color the poly-Si has. AZ4620 photoresist is then removed by acetone soak and O_2 plasma etching at 200 W in Ar/O_2. Figure 3.29 shows the photos of the wafer from sacrificial oxidization to removing the AZ4620. The wafer is then sent out for n-well implantation. According the previous experiences on N-MOSFETs, the n-well doping profile requires a moderate doping ($2x10^{17}$ cm^{-3}) near the surface and a higher doping ($2x10^{18}$ cm^{-3}) at the bottom of the n-well. As shown in Fig. 3.30, this retrograde doping profile can be achieved using several different energy and dose combinations. SRIM/TRIM is used to determine the energy and dose of the implantations.

Due to the lack of experience for p-channel MOS devices, we have to guess the dose of the threshold adjustment implant to achieve a proper threshold voltage. The three samples have slightly different n-well profiles for better chance of hitting the target. Tables 3.4, 3.5 and 3.6 show the n-well implantation conditions of sample #1, #2, and #3.

Sample #1 does not have any threshold adjustment implant. Sample #2 and #3 have different dose of Al ions to adjust the threshold voltage. Considering the thickness of the gate oxide (50 nm) and assuming 50% Al activation ratio, the Al implantation should be able to shift the threshold voltage of the P-IGBT by about 11.6 V and 5.8 V toward the origin for sample #2 and #3, respectively. The threshold voltage of the experimental devices with the above n-well profiles will be measured and discussed in a later section.

Table 3.4 N-well implantation conditions for sample #1

Temperature = 650°C	
Tilt angel = 0°	
Nitrogen	
Energy (keV)	Dose (cm^{-2})
40	$8.5x10^{11}$
80	$1.3x10^{12}$
200	$1.3x10^{13}$
300	$2.4x10^{13}$

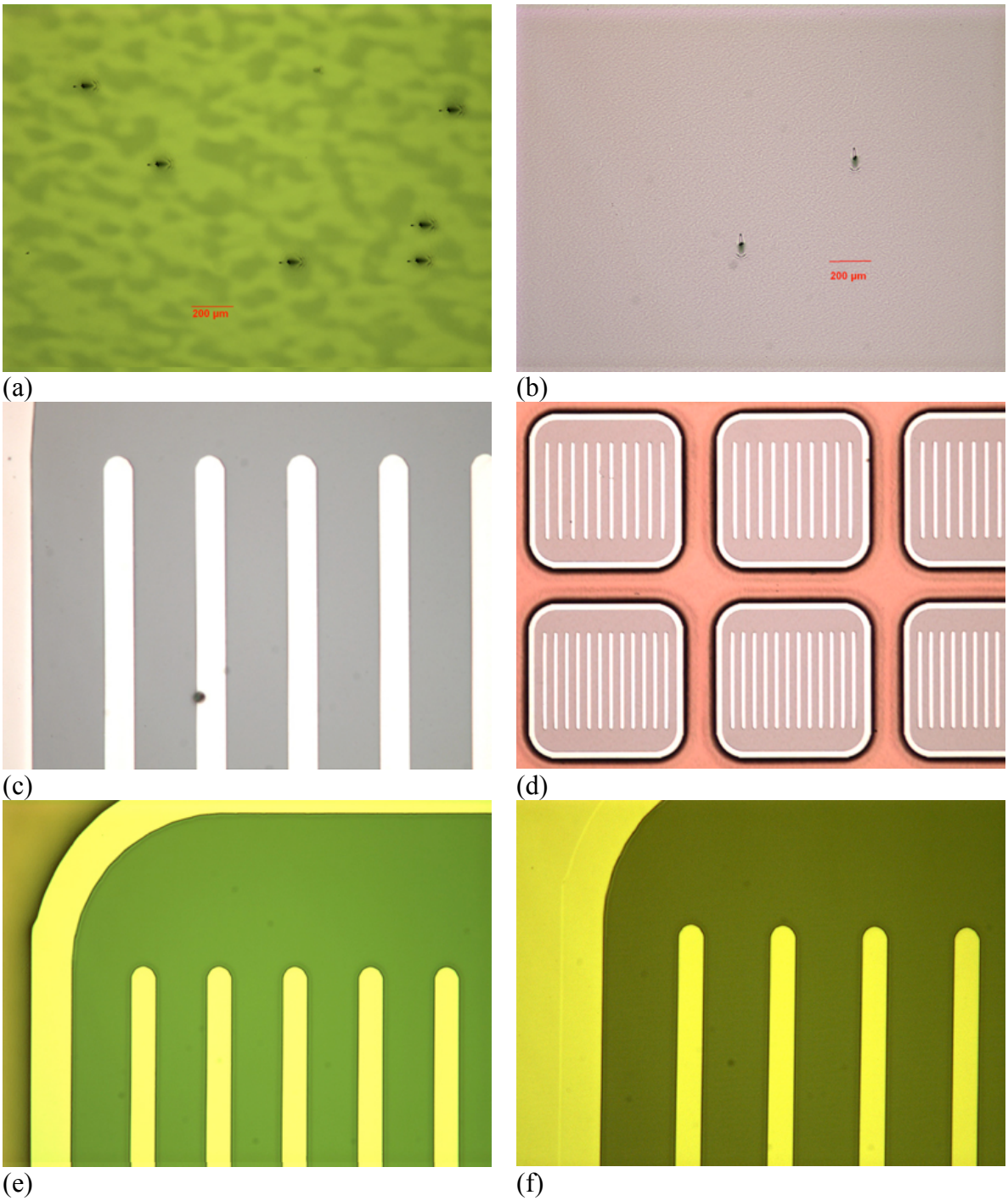


Fig. 3.30 (a) wafer after initial sacrificial oxidation; (b) 1.5 µm poly-Si; (c) Ni fingers after liftoff; (d) AZ4620 photoresist patterned to prevent micro masking; (e) after RIE removing poly-Si; (f) after removing AZ4620 photoresist

Table 3.5 N-well implantation conditions for sample #2

Temperature = 650°C			
Tilt angel = 0°			
Nitrogen		Aluminum	
Energy (keV)	Dose (cm^{-2})	Energy (keV)	Dose (cm^{-2})
40	$8.5x10^{11}$	40	$1x10^{13}$
80	$1.3x10^{12}$		
200	$1.3x10^{13}$		
300	$2.4x10^{13}$		

Table 3.6 N-well implantation conditions for sample #3

Temperature = 650°C			
Tilt angel = 0°			
Nitrogen		Aluminum	
Energy (keV)	Dose (cm^{-2})	Energy (keV)	Dose (cm^{-2})
40	$8.5x10^{11}$	40	$5x10^{12}$
80	$1.3x10^{12}$		
200	$1.3x10^{13}$		
300	$2.4x10^{13}$		

3.1.3.2.3 The self-aligned source process

After n-well implantation, Ti/Ni is removed using piranha. Step height measurement is performed to measure the thickness of the poly-Si using α-step. The minimum poly-Si thickness is about 1.3 μm. If the poly-Si is too thin, it will be difficult to obtain sufficient poly-Si lateral expansion by wet oxidation. The poly-Si thickness on sample #1 is 2.07 μm.

The self-aligned source process is developed by the Wide Bandgap Group at Purdue University [20]. The idea is to use the expanded poly-Si as the source implant mask, so that the channel length is the lateral expansion. The wafer is oxidized in wet oxygen for 9 hours at 1000°C. α-step measures that the vertical growth of the poly-Si is 0.63 μm. The lateral growth of the poly-Si fingers is measured to be 0.84 μm using scanning electron microscope (Hitachi, s4800), as shown in Fig. 3.31 (a), (b). Considering the symmetry of the design, the inversion channel length is about 0.42 μm.

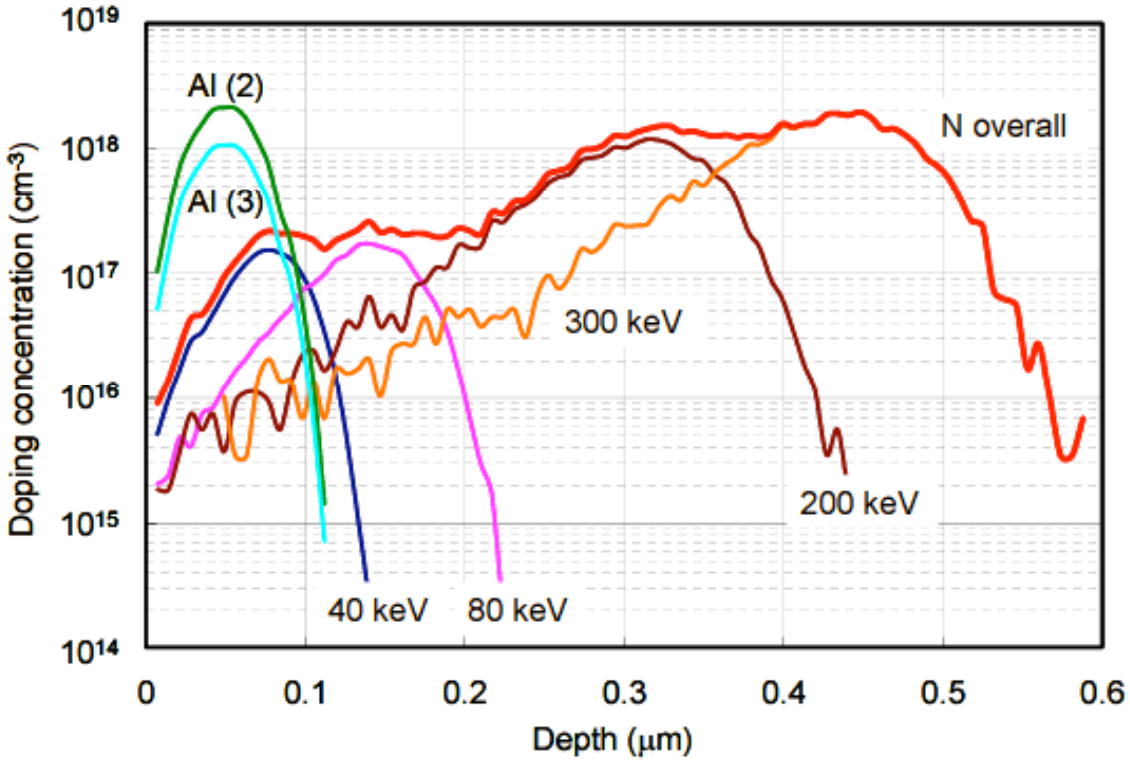


Fig. 3.30 N-well implantation profile for sample #1, #2 and #3. Energy and dose refer to Table 3.4, 3.5, and 3.6.

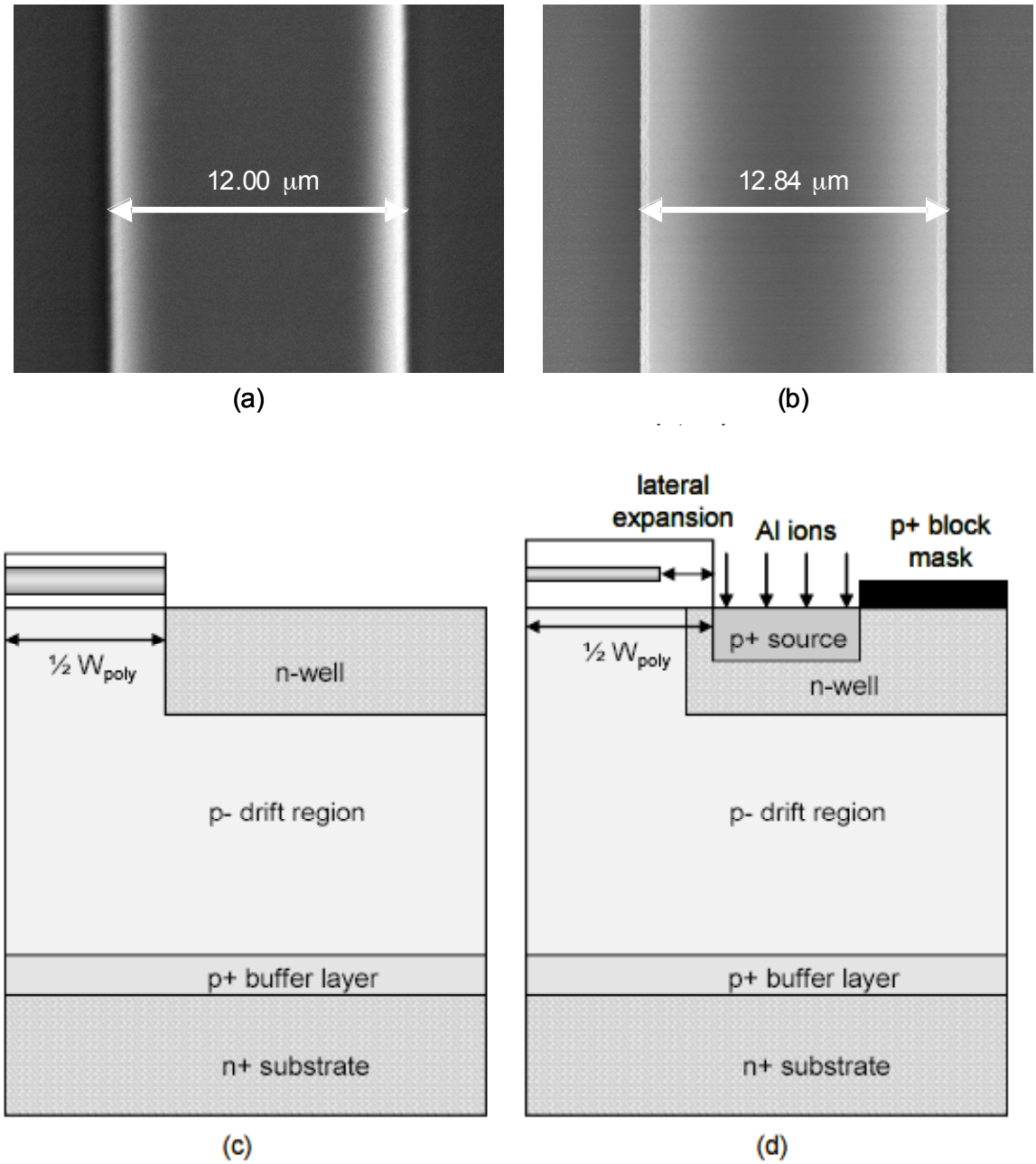


Fig. 3.31 (a), (b) SEM photos of poly-Si finger before and after the self-align oxidation; (c), (d) schematics of the self-aligned source process

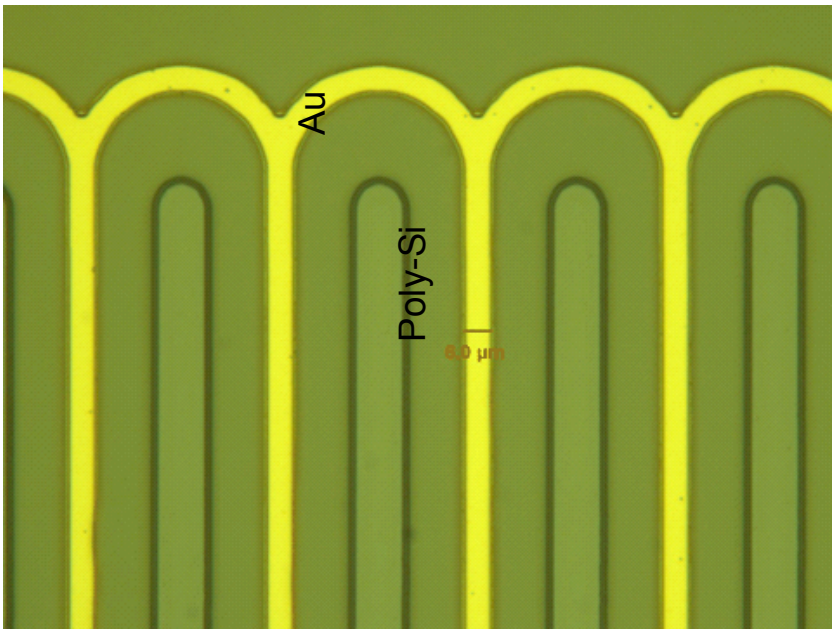
Liftoff lithography is performed with the p+ block mask, and Ti (20 nm)/Au (450 nm) are evaporated and patterned. Then Al ions are implanted with the mask of expanded poly-Si and Ti/Au. This implantation forms the p+ source region. The implantation conditions are listed in Table 3.7. The photo of the wafer before source implantation and the implant profile are shown in Fig. 3.32. In speaking of the doping concentration in the p+ source region, a higher doping is not always better. This is because of the p-type dopants (Al) have low ionization percentage at room temperature in 4H-SiC. In fact, the activated Al ions cannot exceed middle 10^{17} cm^{-3} even at the highest possible implantation dose [43]. Heavy Al implant dose severely damages the SiC lattice and causes step-bunching during the implant activation anneal. Therefore, the implanted Al concentration should not exceed the low 10^{19} cm^{-3} ranges.

Table 3.7 P+ source implantation conditions

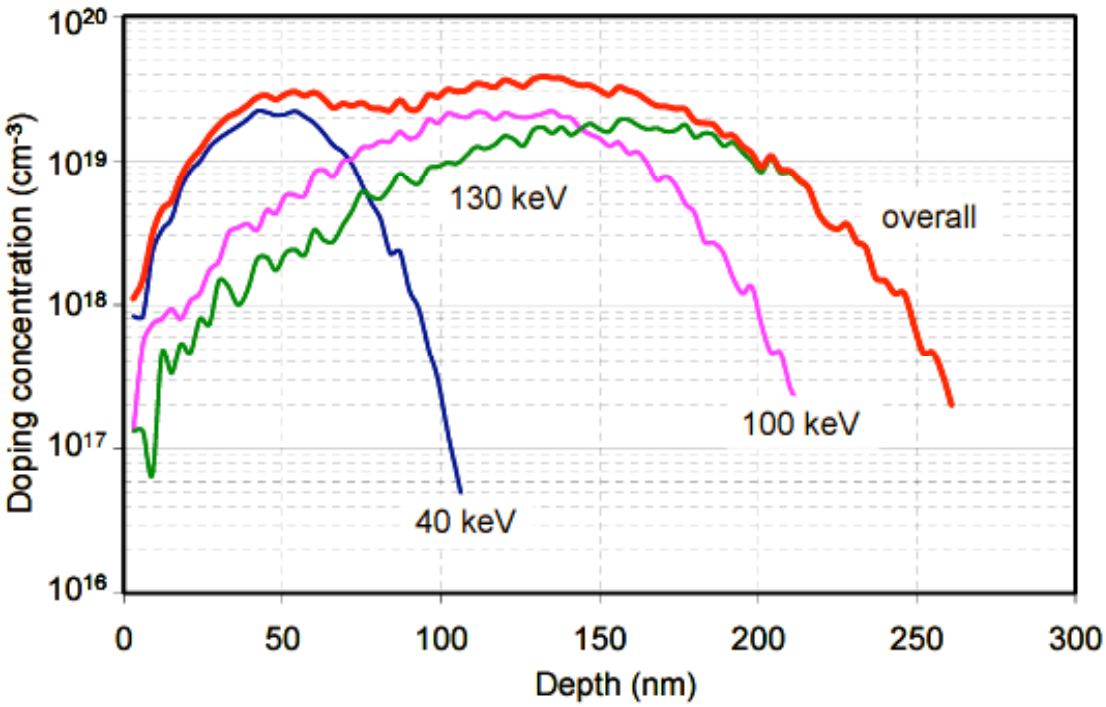
Temperature = 650°C	
Tilt angel = 0°	
Aluminum	
Energy (keV)	Dose (cm^{-2})
40	$1.0x10^{14}$
100	$2.0x10^{14}$
130	$2.0x10^{14}$

3.1.3.2.4 N+ implantation

After the p+ source implantation, the Ti/Au mask, SiO2, and un-oxidized poly-Si are removed by subsequently soaking in Aqua Regia ($HCl:HNO_3$ = 3:1), and poly-Si etchant ($HF:HNO_3:DI$ = 30:55:300). A thermal oxidation is performed at 1150°C for 40 minutes in wet oxygen. The oxide thickness is around 20 nm. This oxide prevents metals to be in direct contact with SiC. Ti (20 nm)/Au (450 nm) are evaporated and patterned by liftoff lithography using the n+ contact implant mask. Figure 3.33 (a) shows the photo of the wafer before n+ implantation. A nitrogen implantation is then performed to form the n+ base contact. The energy and dose of the implantation are listed in Table 3.8. The implantation doping vs. depth profile is shown in Fig. 3.33 (b).

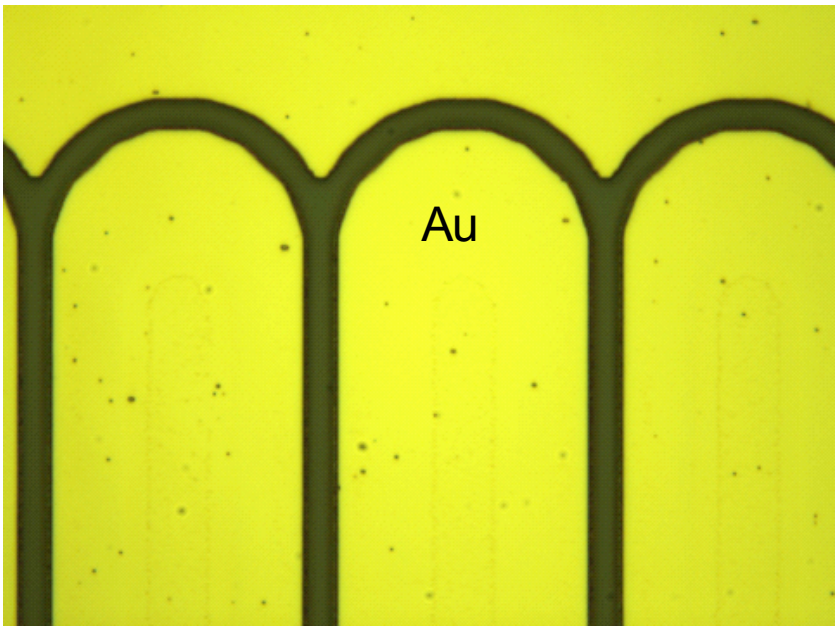


(a)

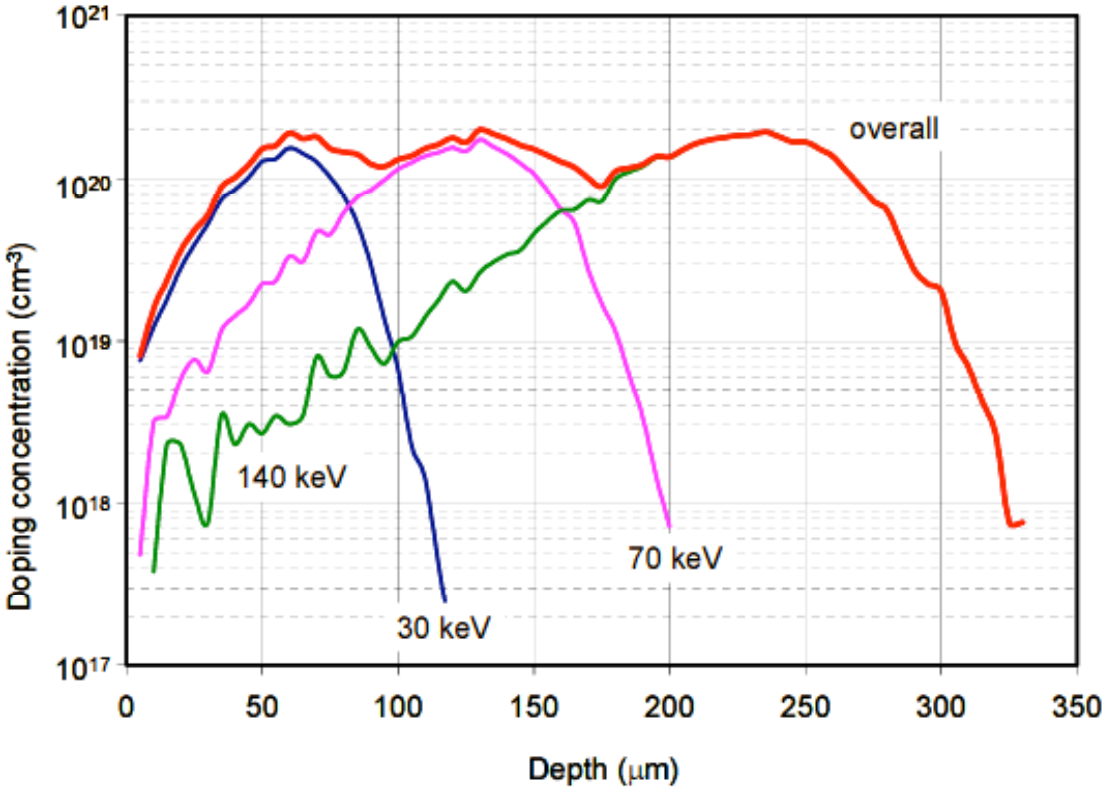


(b)

Fig. 3.32(a) Photo of the sample before p+ source implantation; (b) p+ source implantation profile



(a)



(b)

Fig. 3.33(a) Photo of the sample before n+ implantation; (b) n+ implantation profile.

Table 3.8 N+ implantation conditions

Temperature = 650°C	
Tilt angel = 0°	
Nitrogen	
Energy (keV)	Dose (cm^{-2})
30	$7.0x10^{14}$
70	$1.2x10^{15}$
140	$1.9x10^{15}$

3.1.3.2.5 Implant activation anneal

The n+ implantation is the last ion implantation step. All metals are removed and a high temperature anneal must be done to activate the implanted nitrogen and aluminum ions. It has been reported that nitrogen ions can be activated nearly 100% at a temperature lower than 1500°C [62]. The p-type aluminum dopants require 1600°C anneal to achieve over 50% activation [63]. The sublimation of Si from SiC surface at high temperature causes increased surface roughness, a phenomenon called "step-bunching". It has been observed that small surface steps coalesce into higher and wider steps during the implant activation anneal [15]. The result is a rough SiC surface with step height in nanometers range. MOS channels formed on the step-bunching region can suffer from very low inversion channel mobility. Since the degree of step-bunching is directly related to SiC surface damage, the p+ source and n+ regions are most likely to have the worst surface roughness. For the DMOS-IGBT structure, the source is insulated from the poly-Si gate by the oxide over the source region. We have observed high gate leakage current on IGBTs with very rough source region (RMS roughness = 17 nm). This gate leakage current is fatal to the MOS devices. Therefore, we have to find a good way to suppress step-bunching during the implant activation anneal.

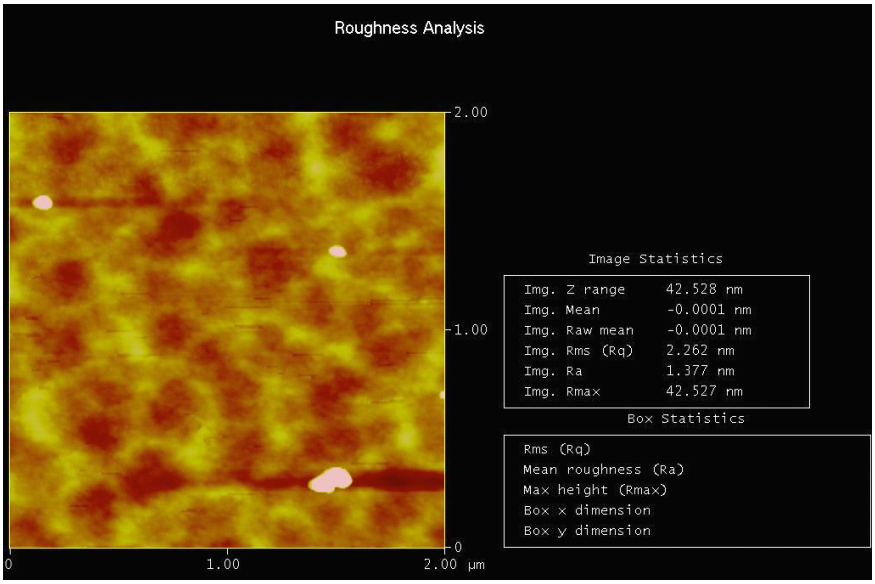
It has been reported that annealing in a Si-rich atmosphere (such as silane) can help minimize the surface roughness [64]. But the operation window for silane anneal is proved to be narrow, and therefore the yield of silane anneal is relatively low [65]. A recent approach for implant activation is to use a graphite cap to cover the wafer during annealing [66]. The graphite cap is made by spinning photoresist on the wafer surface

and then driving off the organic content in a high temperature furnace. The graphite cap effectively prevents surface Si atoms from sublimation at high temperature. It can be removed by a long O_2 plasma etching afterwards. According to our experiments on testing wafers, the graphite capped anneal is more consistent and yields lower surface roughness.

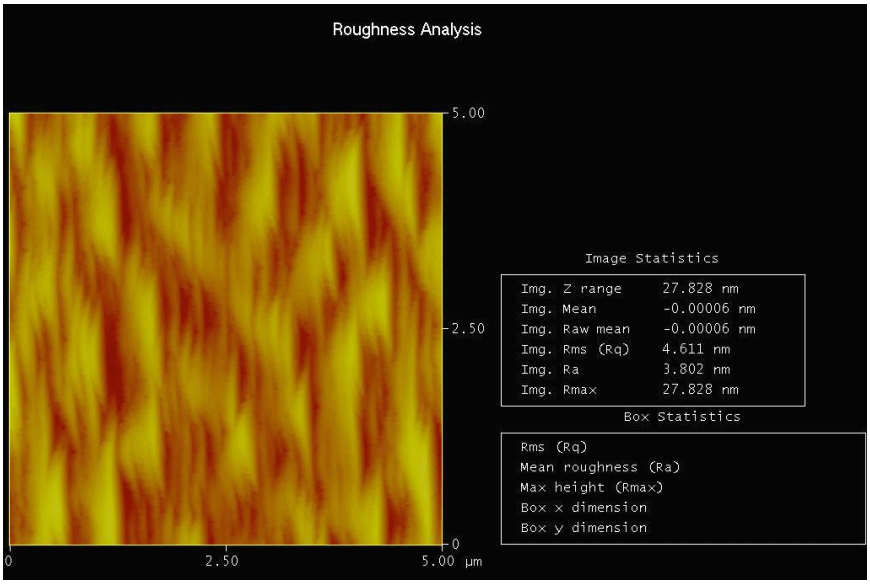
For the experimental p-channel IGBTs, silane anneal is performed at 1600°C for 20 minutes. The silane flow rate, timing for turning on and off silane are all critical for the surface roughness. Increased surface roughness in heavily doped regions is observed by atomic force microscope (AFM), as shown in Fig. 3.34. In future experiments, we suggest lower the implantation dose in p+ and n+ region, and using graphite capped anneal for better surface roughness.

3.1.3.2.6 Gate oxidation, post oxidation anneal, and poly-Si gate

One advantage of fabricating MOS devices on SiC is that high quality oxide can be achieved by thermal oxidation. It has been reported that the thermal oxide on 4H-SiC can withstand electric field in excess of 8 MV/cm [67]. As discussed earlier, the inversion channel mobility of 4H-SiC is in single digits if no post oxidation anneal is performed. It has been reported that nitric oxide (NO) anneal helps reduce the interface state density and improve the n-channel mobility to above 40 cm^2/Vs [68]. It is likely that NO anneal will also improve the p-channel mobility, considering the mechanism of NO anneal is to terminate excess carbon atoms and dangling bonds at the interface [69]. The experimental P-IGBTs are oxidized in a pyrogenic oxidation system for 150 minutes at 1150°C, followed by in-situ argon anneal at 1150 °C. The gate oxide thickness is then measured to be around 50 nm by an ellipsometer. The post oxidation anneal is carried out in nitric oxide at 1175°C for 2 hours. No significant change on the gate oxide thickness is observed.



(a)



(b)

Fig. 3.34 AFM picture of the p+ source region. (a) before implant activation, RMS roughness = 2.2 nm; (b) after implant activation, RMS roughness = 4.6 nm.

N-type poly-Si is used for gate material. Undoped poly-Si is deposited on the wafer by LPCVD at 600°C. The thickness of the poly-Si is 450 ~ 600 nm. If the poly-Si is too thick, it will be hard for the phosphorus dopants to diffuse through it. Phosphorus spin-on diffusant is spun on the wafer and driven in at 900 °C in oxygen for 1 hour. The surface oxide is then removed by a short BHF etch. The sheet resistance of the poly-Si gate is around 16 Ω/square, measured by four-point probe. The poly-Si gate is patterned by RIE etching through a photoresist mask. Figure 3.35 shows the P-IGBT after the poly-Si gate is patterned.

3.1.3.2.7 Ohmic contacts and top metal

Making good ohmic contacts to the semiconductor is one of the most important steps in device fabrication. It is particularly important for SiC power devices because high on-state current flows through the ohmic contacts. If the contacts are poor, the voltage drop will be significant on the contacts.

Nickel (100 nm) is deposited by e-beam evaporation and patterned by liftoff lithography on the wafer as n-type contact metal. Ni fingers are aligned with the n+ implantation fingers to make contacts to the n-well. The device after Ni liftoff is shown in Fig. 3.36 (a). Ti (33 nm) and Al (167 nm) are deposited and patterned as p-type ohmic metals. The Ti/Al fingers are about 3 times wider than the Ni fingers and cover the Ni fingers, as shown in Fig. 3.36 (b). The p-type ohmic metals make contact to the p+ source. Since current flows through both source and n-well of P-IGBTs, both p-type and n-type ohmic contacts resistance need to be as low as possible.

In order to achieve low contact resistance, several criteria must be met when preparing the ohmic contacts. The purity of the source metals has to be 99.99% or higher. The wafer surface must be properly treated after the liftoff lithography and before the metal evaporation. The treatment includes RIE at 100 W in SF_6 for 1 minute, followed by O_2 plasma etch in Ar/O_2 at 100 W for 1 minute, and BHF dip for around 30 seconds right before the wafer enters the e-beam evaporator chamber. The treatment effectively removes photoresist residue, byproducts from the plasma etch, and remaining oxide on the area where contacts are to be made. The base pressure in the e-beam evaporator needs to be lower than $5x10^{-7}$ torr during the evaporation to prevent oxidation.

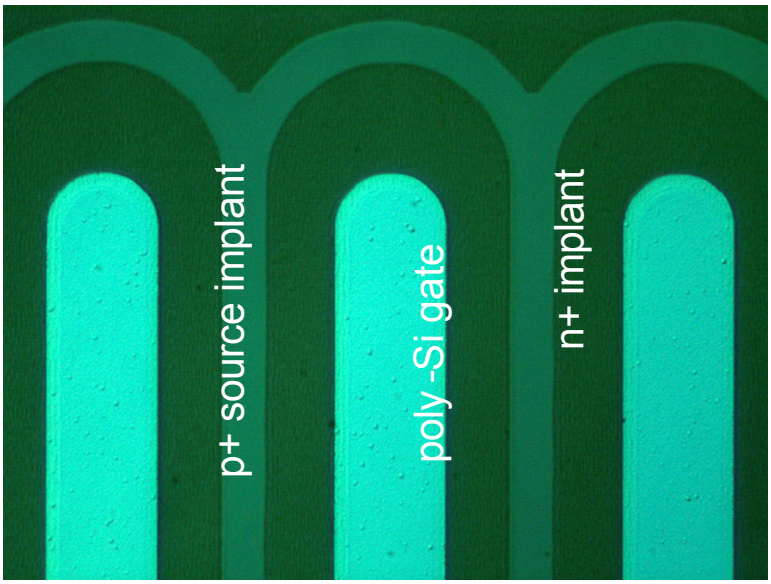
TLM testers prepared by the above protocol demonstrated 10^{-4} Ωcm^2 for p-type and 10^{-5} Ωcm^2 for n-type ohmic contacts.

All the contacts are annealed at 1000°C in vacuum for 2 minutes. The base pressure in the contact annealer is around $1x10^{-6}$ torr before annealing. The contact metals usually lose the shiny surface after the contact anneal. As shown in Fig. 3.36 (c), the ohmic metals become dark and have black dots on them after contact anneal. This discoloration usually indicates that the ohmic metals have alloyed with the semiconductor.

Electrical measurements are usually taken before and after the contact anneal. Sometimes there is surface leakage after contact anneal, which can be removed by O_2 plasma etching. The final step is to evaporate and pattern Ti (20 nm)/Au (500 nm) as top metal. The on-resistance of the device may further improve after the top metal because the top metal connects the discontinuous ohmic contacts and reduces the resistance of the long fingers. The device after top metal is shown in Fig. 3.36 (d).

Figure 3.37 shows the SEM photos of final type A, B, C P-IGBTs, and a P-IGBT with floating field rings edge termination. Type A and type B devices have similar structure, except that type B devices have narrower contact fingers. Therefore, type B devices have a higher channel density than type A devices. Type C devices have separate source and base contact fingers and contact pads, which allow us to measure the source and base current separately. The device with edge termination has a round shape, which effectively reduces local electric field crowding in the blocking state. There are sixty-six 3 μm wide floating field rings, with 3 μm spacing. Obviously, a device with edge termination takes up a lot of wafer area, which is the reason for only one P-IGBT with edge termination per die.

Figure 3.38 shows an overview of quadrant 3, a close-up look at the testers, and details of the P-IGBTs. The top metal covers the n-type and p-type contact metals, as shown in Fig 3.38 (c). Figure 3.38 (d) shows the separate source and base contact fingers of a type-C P-IGBT.



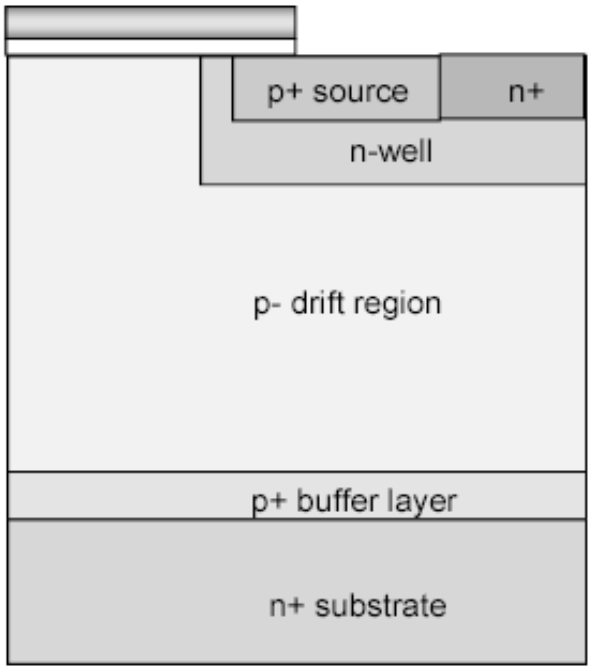


Fig. 3.35 P-IGBT after patterning the poly-Si gate. The photo is taken in Nomarski mode.

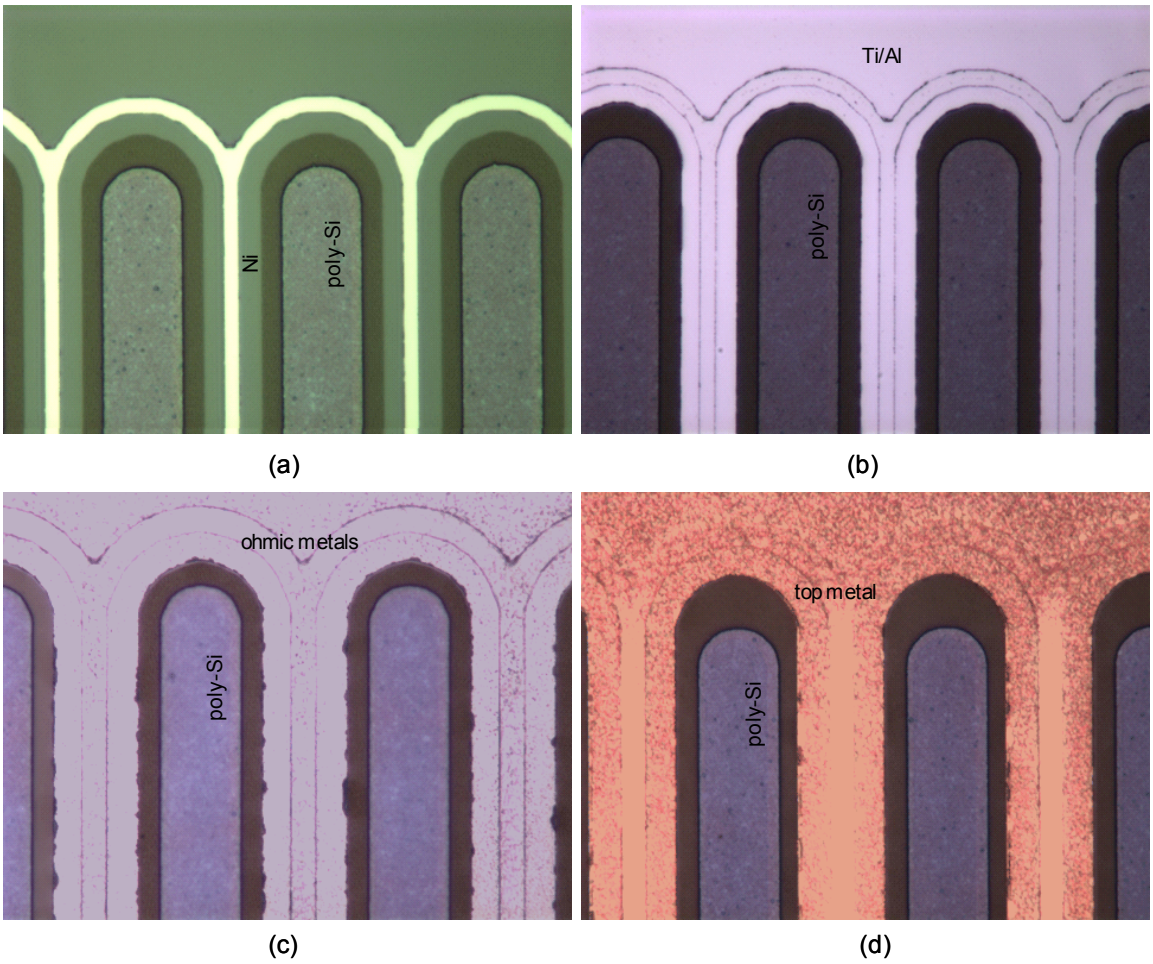


Fig. 3.36(a) P-IGBT after Ni liftoff; (b) P-IGBT after Ti/Al liftoff; (c) P-IGBT after contact anneal; (d) P-IGBT after top metal

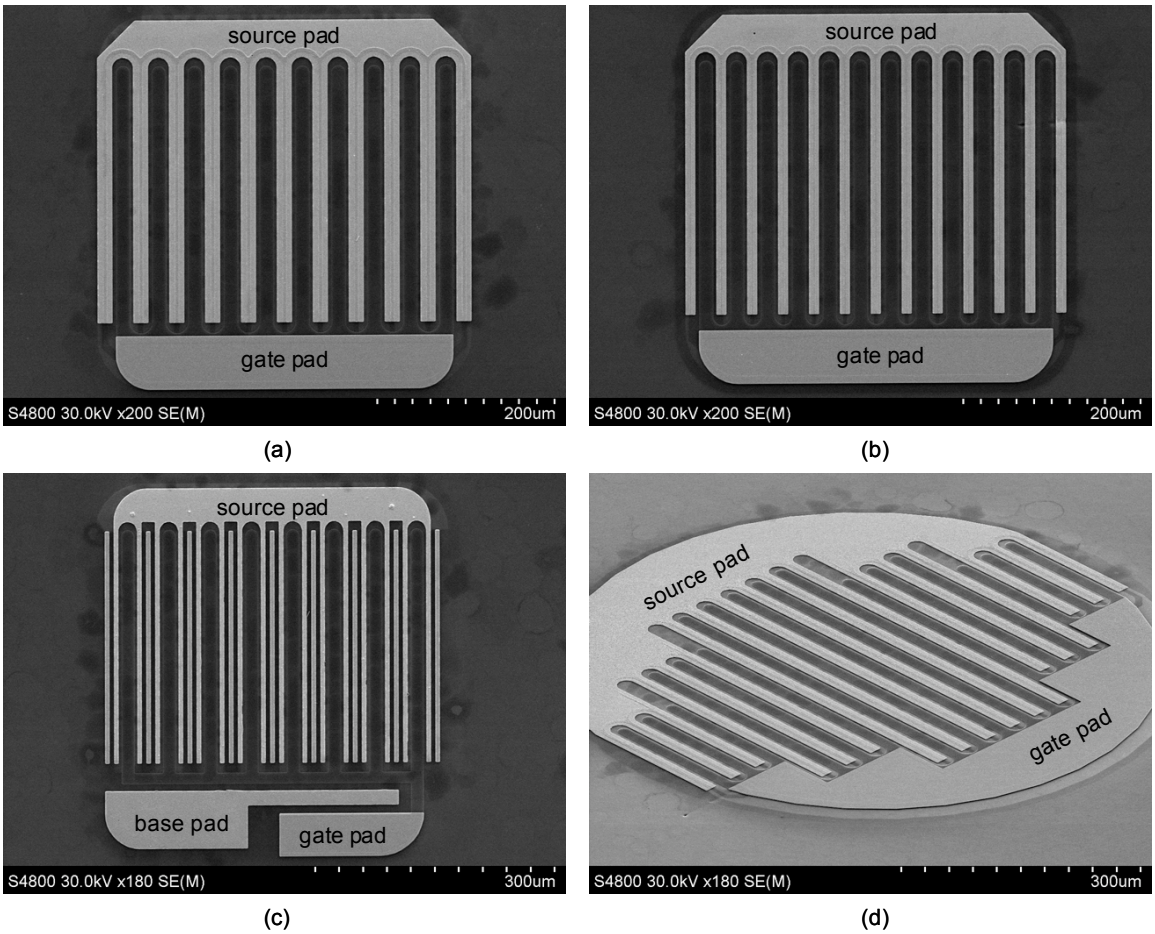


Fig. 3.37 SEM photos of the final P-IGBTs. (a) type A P-IGBT; (b) type B P-IGBT; (c) type C P-IGBT; (d) P-IGBT with edge termination

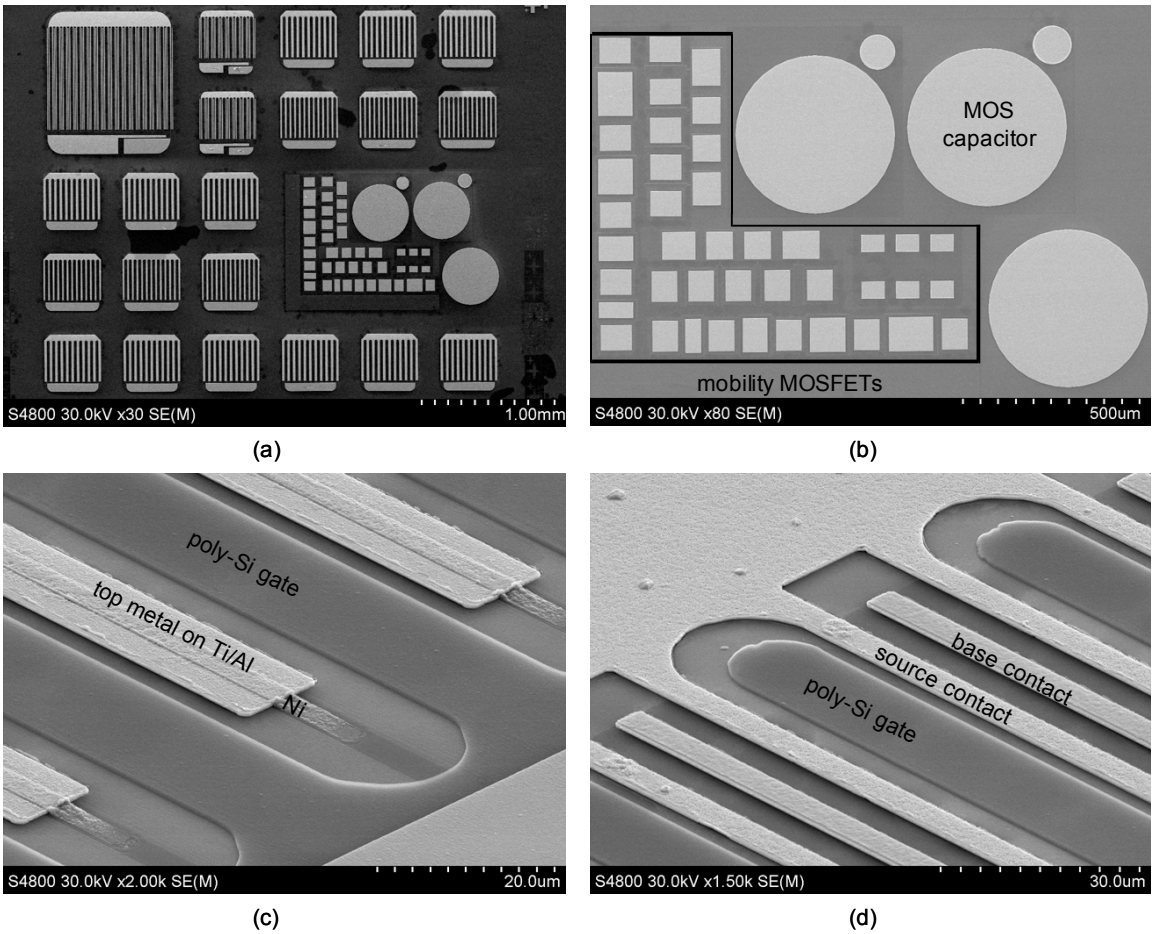


Fig. 3.38 SEM photos of the final devices. (a) quadrant 3 of the die; (b) mobility MOSFETs and MOS capacitors; (c) end of top metal fingers on a type A P-IGBT, tilt angle = 60°; (d) top metal fingers on a type C P-IGBT, tilt angle = 60°.

3.1.4 Experimental Results and Device Performance

3.1.4.1 I-V characteristics of the P-IGBTs

3.1.4.1.1 On-state performance of the P-IGBTs

The on-state I-V measurements of the P-IGBTs are performed using an HP-4156A semiconductor parameter analyzer and a Keithley-4200 semiconductor characterization system. During the measurements, the source and the n-well contacts are grounded, the gate is negatively biased, and the cathode voltage sweeps from zero to -20 V.

Figure 3.39 shows the on-state I-V characteristics of a typical type A P-IGBT before contact annealing (device area = 7.27×10^{-3} cm^2). The absolute value of the cathode voltage is plotted on the x-axis on all the I-V plots in this chapter. The on-state current is several orders of magnitude lower than the prediction from simulation, which is most likely caused by the unannealed ohmic contacts. The threshold voltage of the P-IGBT is high (-28V), which is caused by the high interface state density (D_{it}) and the lack of threshold adjustment implant. It shows gate modulation over the channel. Due to the high threshold voltage, the electric field in the gate oxide is around 6 MV/cm when the channel is turned on. Amazingly, the oxide does not show any signs of degradation or breakdown after prolonged measurements. This indicates that the protocol for gate oxidation and post-oxidation annealing is capable of providing reliable gate oxide that can withstand up to 8 MV/cm electric field.

Figure 3.40 shows the on-state performance of typical type A and type B P-IGBTs after contact annealing. Compared to the I-V curves before contact annealing, the on-state current density is increased by three to four orders of magnitude. This tremendous change in current indicates that significant voltage drop is on the contacts before the annealing. Contact annealing is one of the most crucial steps for SiC power IGBTs.

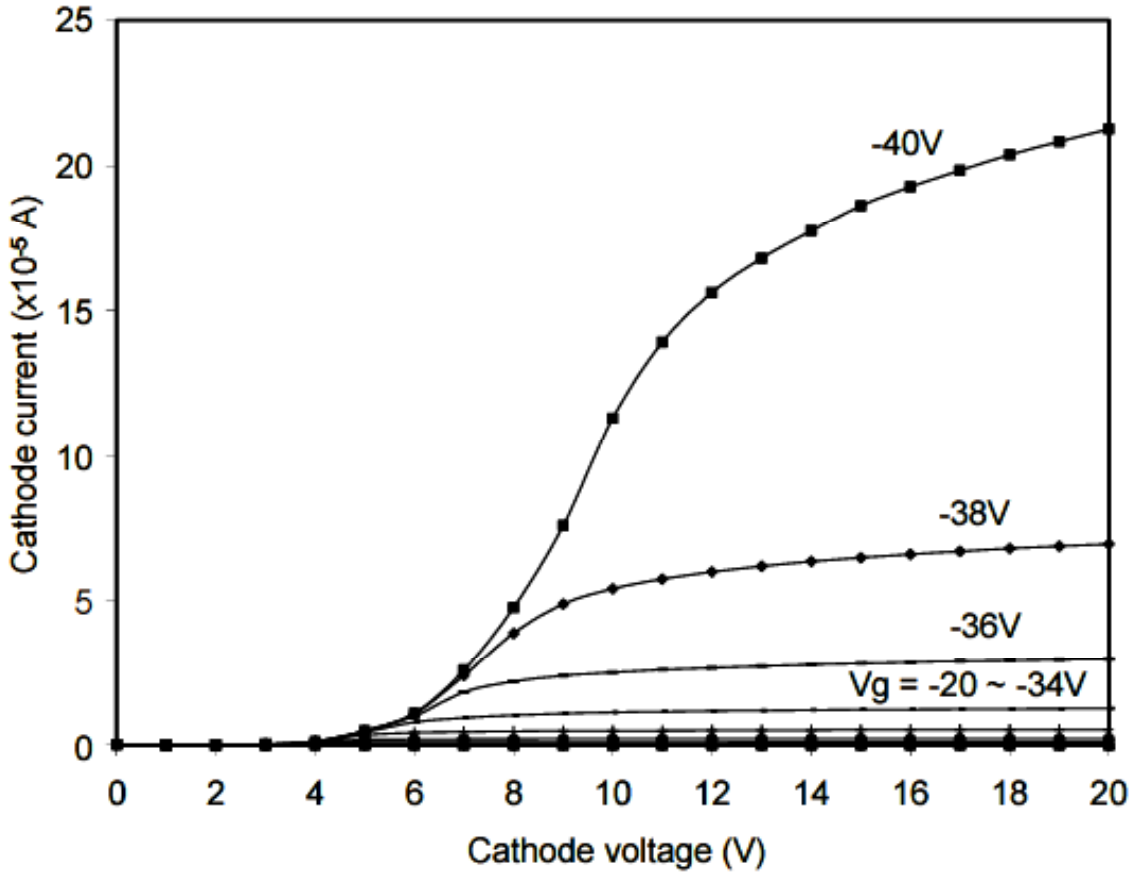


Fig. 3.39 On-state I-V characteristics of a typical type A P-IGBT before contact annealing. Device active area = $7.27x10^{-3}$ cm^2. T_{ox} = 50 nm.

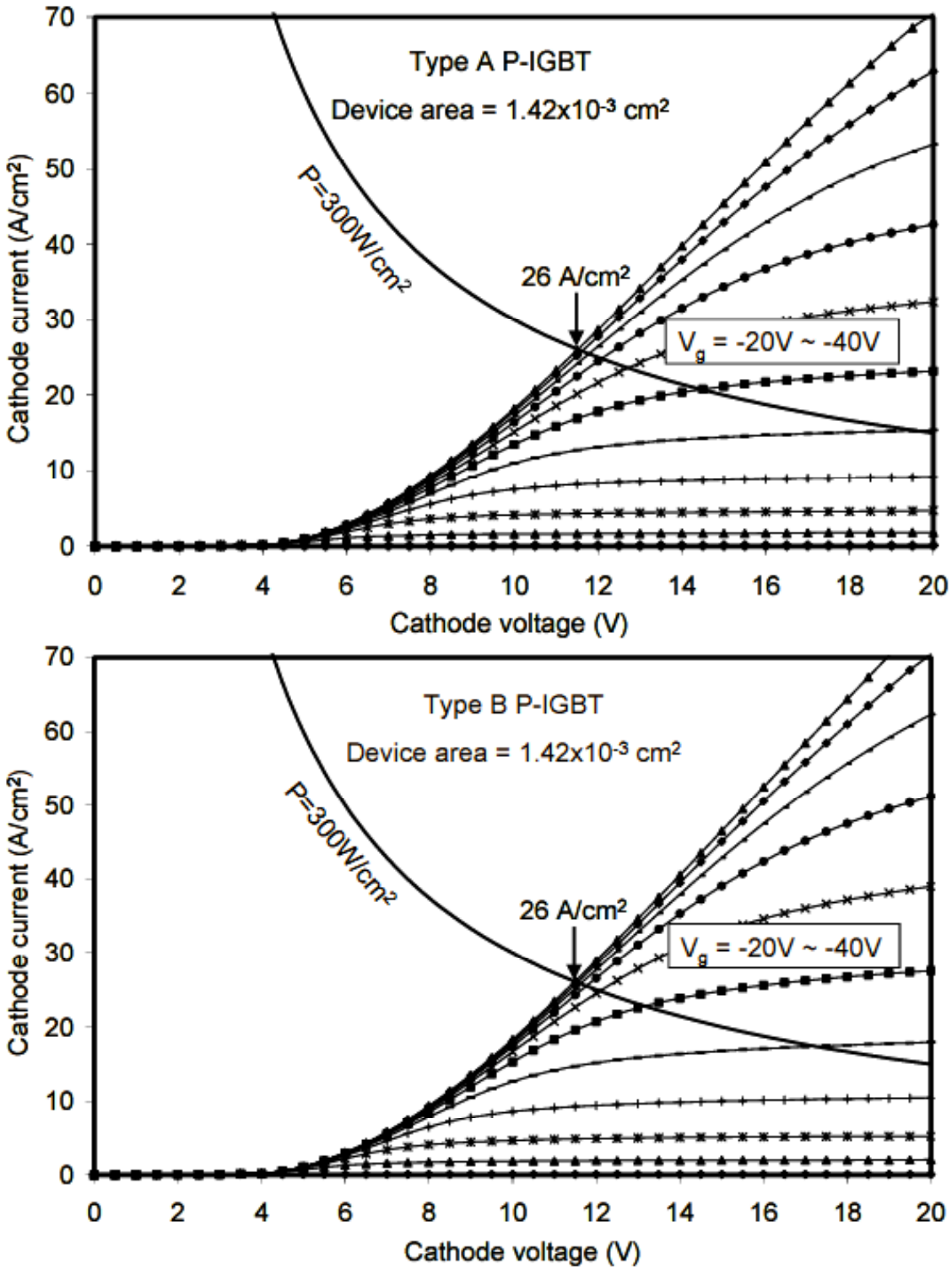


Fig. 3.40 On-state I-V characteristics of a type A and a type B P-IGBT after contact annealing. V_g = -20 V ~ -40 V in 2 V interval. T_{ox} = 50 nm.

The threshold voltage of the P-IGBTs after contact annealing is lowered to -20 V. Contact annealing itself does not change the MOS interface properties, but it changes the voltage across the contacts. The applied gate to source voltage (V_{gs}) is actually the sum of the source contact voltage and the real gate voltage. The source contact voltage is significantly reduced after contact annealing, which raises $|V_g|$. Another mechanism is the body effect that lowers $|V_t|$. Both mechanisms effectively increase $|V_g - V_t|$, and therefore increase the on-state current density at the same applied gate voltage.

The top areas of type A and type B P-IGBTs are the same, except that type B devices have narrower and two more fingers than type A devices. The on-state I-V characteristics of the two types of P-IGBTs are almost identical. It indicates that current spreads horizontally and becomes uniform under the device as flowing through the drift region. The channel density does not limit the total current. This speculation is confirmed by current flow charts in Fig. 3.45. In fact, the experimental P-IGBTs having the highest current density are type C devices with the largest pitch size.

Given the power dissipation limit of 300 W/cm^2, the current saturates at a gate voltage of -36 V. The highest current density under the power limit is around 26 A/cm^2 for both type A and type B device, which is ~81% of the theoretical value (32 A/cm^2). Figure 3.41 shows the type C P-IGBT with the best on-state performances. The current saturates at a gate voltage of -34 V. The maximum current density under the 300 W/cm^2 power limit is ~32 A/cm^2. It is very close to the theoretical value. This indicates that the physical models used in the simulation are quite accurate. The gate leakage current increases almost linearly with gate voltage, as the inset shows. The maximum gate leakage current at V_g = -40 V is still 5 to 6 orders of magnitude lower than the on-current. It's a good indication that the gate oxide is reliable even operating at an oxide field of 8 MV/cm.

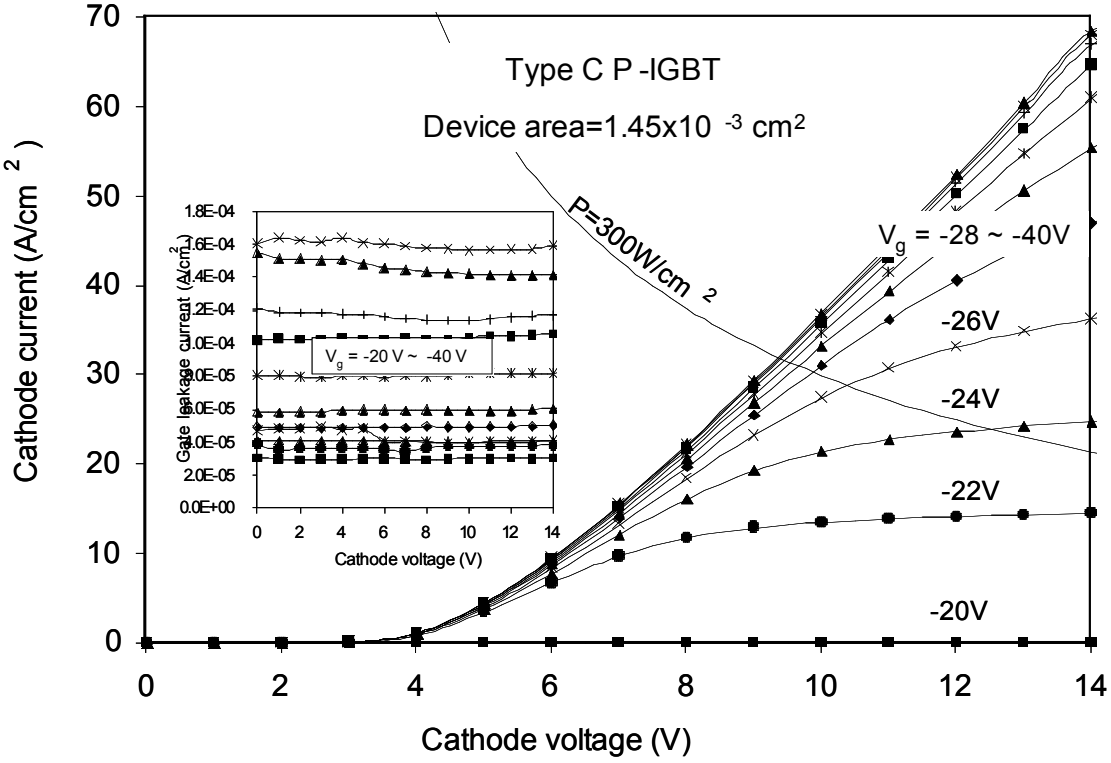


Fig. 3.41 On-state I-V characteristics of a type C P-IGBT after contact annealing. Vg = -20 ~ -40 V in 2 V interval. T_{ox} = 50 nm. The inset is the gate leakage current density vs. cathode voltage for different gate voltages.

3.1.4.1.2 Electron and hole current inside the P-IGBTs

As bipolar devices, P-IGBTs have both electron current and hole current inside the devices during on-state operation. The holes flow through the MOS channel into the drift region. The electrons are injected from the bottom of the device into the drift region. Some electrons and holes recombine in the drift region. Some electrons travel across the thick drift region and get swept out at the n-well/drift region junction. It is similar to a P-MOSFET driving the base of an npn BJT.

The ratio of electron current to hole current can be calculated from equation (3.36) and (3.37) by setting x = W. The result is that the electron current is about 9 times of the hole current. This current ratio agrees with the numerical simulation result. Type C P-IGBTs allow us to experimentally measure the source current (hole) and base current (electron) separately by having separate contact fingers and contact pads. However, as shown in Fig. 3.42, the experimental result is in conflict with the theoretical prediction. The electron current is only about 10% of the total current when the device is fully turned on.

We do not have a good explanation for this discrepancy yet. Our speculation is that the non-ohmic contacts and the high contact resistivity may have an influence on the current distribution. Another possible reason is the fact that the base contact pad is not in direct connection with the base contact fingers for type C devices, as shown in Fig. 3.41. This may hinder the current flow through the base contact. Further investigation is necessary to discover the true nature of the current distribution inside p-channel IGBTs.

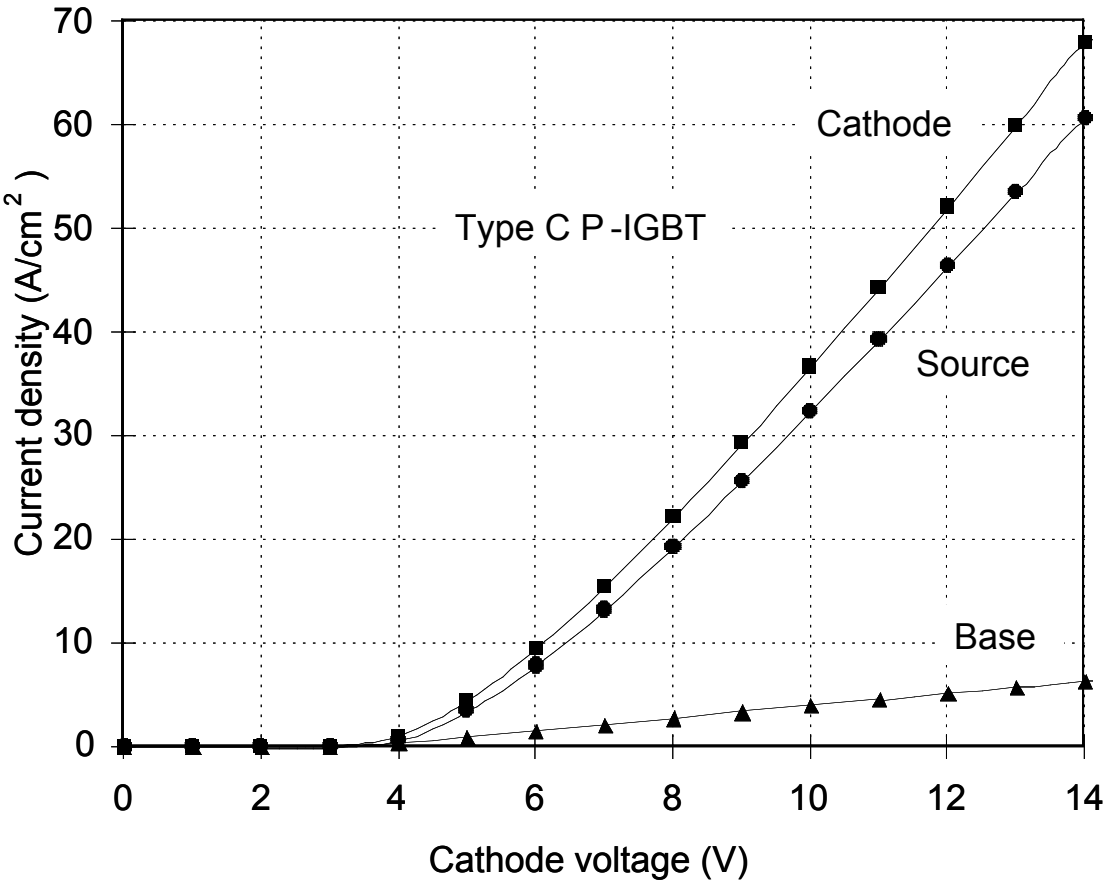


Fig. 3.42 Current distribution in a type C P-IGBT. Cathode indicates the total current; source indicates current through the MOS channel; base indicates current through the bipolar part of the device. V_g = -36 V.

3.1.4.1.3 Current spreading effect of IGBTs

For vertical power devices, the current usually spreads laterally as it flows through the drift region of the devices. Therefore, the current spreading effect cannot be overlooked when calculating the specific on-resistance or the on-state current density for SiC power transistors.

For unipolar power devices such as MOSFETs, the resistivity of the drift region is a constant. It only depends on the doping concentration in the drift region. A fixed spreading angle of 45° is assumed for 10 kV SiC power MOSFETs [12]. Using this model, the effective device area can be up to 2x larger than the device top area. We can convert the measured current density into the current density of an infinitely large device, where the current spreading effect can be neglected. For instance, Fig. 3.43 (a) shows the structure and current flow lines of a Schottky diode. The drift region is a lightly doped p-type SiC layer, which resembles the drift layer of a P-MOSFET. The top contact is grounded and the bottom contact is negatively biased. The current near the right edge of the top contact spreads horizontally as it flows through the drift region, as shown in the figure. Figure 3.43 (b) shows the current density along the bottom of the device. If we consider the average current density to be 27 A/cm^2, the effective device width is given by

$$W_{eff} = \frac{I}{J_{avg}} = 474\mu m \tag{5.1}$$

It is equivalent to moving the area under the curve into a rectangle indicated by the dashed lines. The current spreads horizontally by ΔW = 74 μm. Therefore, the effective area of this Schottky diode (rectangle top, 2W by 2L) should be

$$A_{eff} = 2(W + \Delta W) \bullet 2(L + \Delta W) \tag{5.2}$$

The correction factor for current spreading is

$$\frac{A_{eff}}{A} = \frac{(W + \Delta W)(L + \Delta W)}{WL} \tag{5.3}$$

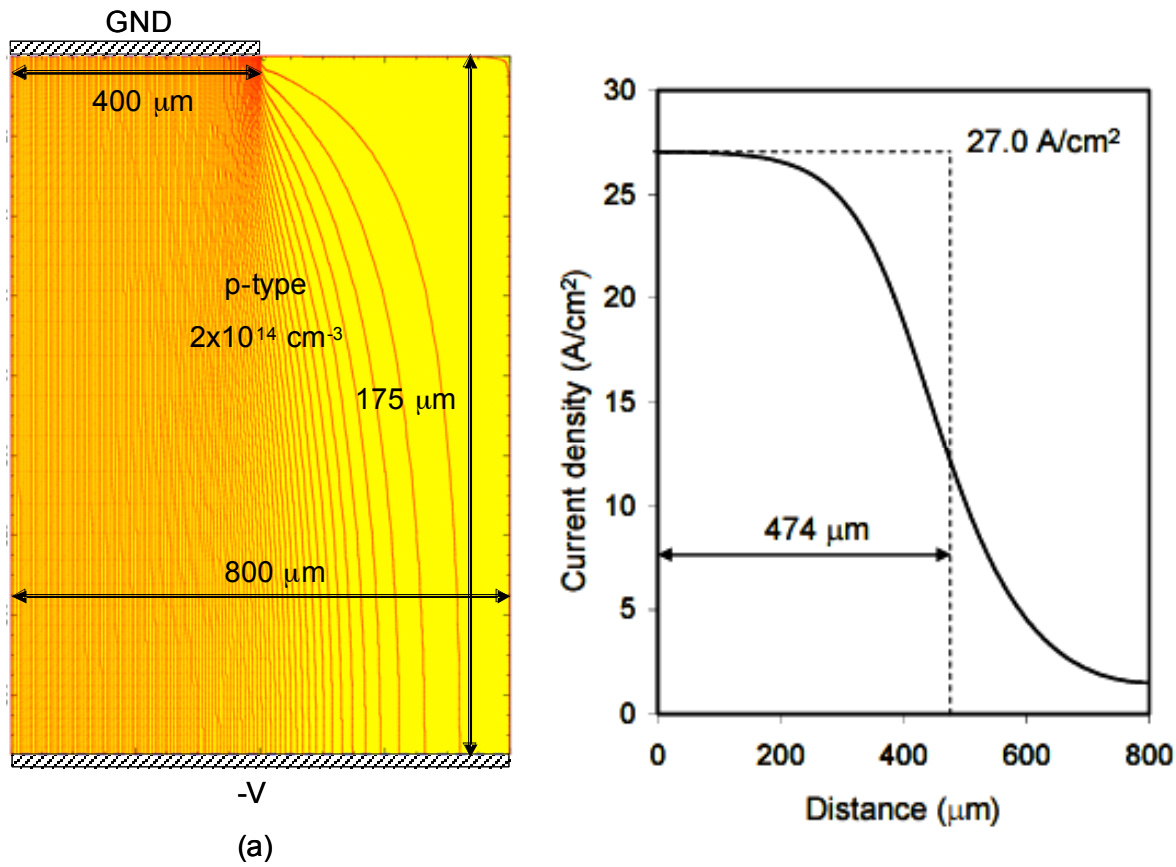


Fig. 3.43 Simulation of a Schottky diode current flow. Top contact width 400 μm, effective width of the device 474 μm.

For bipolar devices such as IGBTs, the resistivity of the drift region is a variable of conductivity modulation. The more current injection in the drift layer, the lower resistivity it has. Figure 3.44 (a) shows the structure and current flow of an infinite P^-N^+ diode. Apparently, the current flow should be uniform, which is exactly as shown in Fig. 3.44 (b). Figure 3.44 (c) shows the structure and current flow of a finite dimension P^-N^+ diode, allowing the current to spread. The current flow lines show that the current density drops rapidly with distance from the right edge of the top contact. The rectangle in dashed lines in Fig. 3.44 (d) has the same area (total current) as the area under the curve. Using equation (5.1), the effective width of the device can be calculated to be 160 μm, which is same as the width of the top contact. Therefore, the current density is not improved by allowing the current spreading.

Figure 3.45 shows the current flow of a P^-N^+ diode with separate top contacts. Similarly, the current flows uniformly for the infinitely large device, and current spreads horizontally for the finite dimension device. The effective width of the finite dimension device is calculated to be 220 μm, which is even smaller than the width of the top contact (228 μm).

In summary, unlike MOSFETs, allowing current spreading does not improve the current density for IGBTs. The reason lies in local conductivity modulation. For IGBTs, the current beyond the device top contact area has to go through a much more resistive region, because the region outside the top contact area has low conductivity modulation. The following example is a good explanation of current spreading for IGBTs. Infinitely large device: all current goes through low resistive regions, i.e., ten 10 Ω resistors in parallel, $R_{overall}$ = 1 Ω. Finite dimension device: a small portion of current goes through highly resistive regions, i.e., nine 10 Ω resistors and a 90 Ω resistor in parallel, $R_{overall}$ = 1.1 Ω.

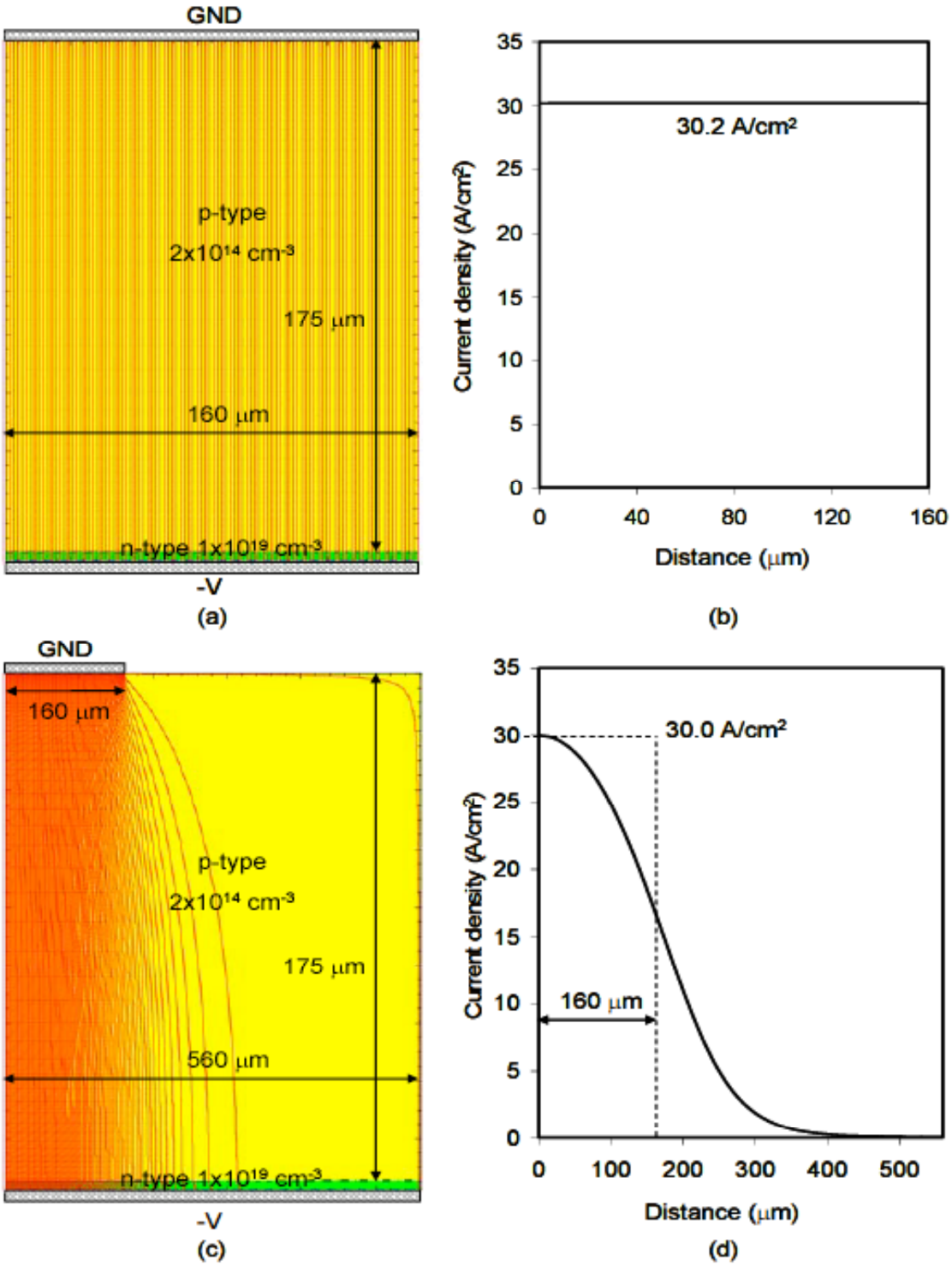


Fig. 3.44(a), (b) Simulation of an infinitely large diode current flow; (c), (d) simulation of a finite diode current flow, top contact width 160 μm, effective device width 160 μm.

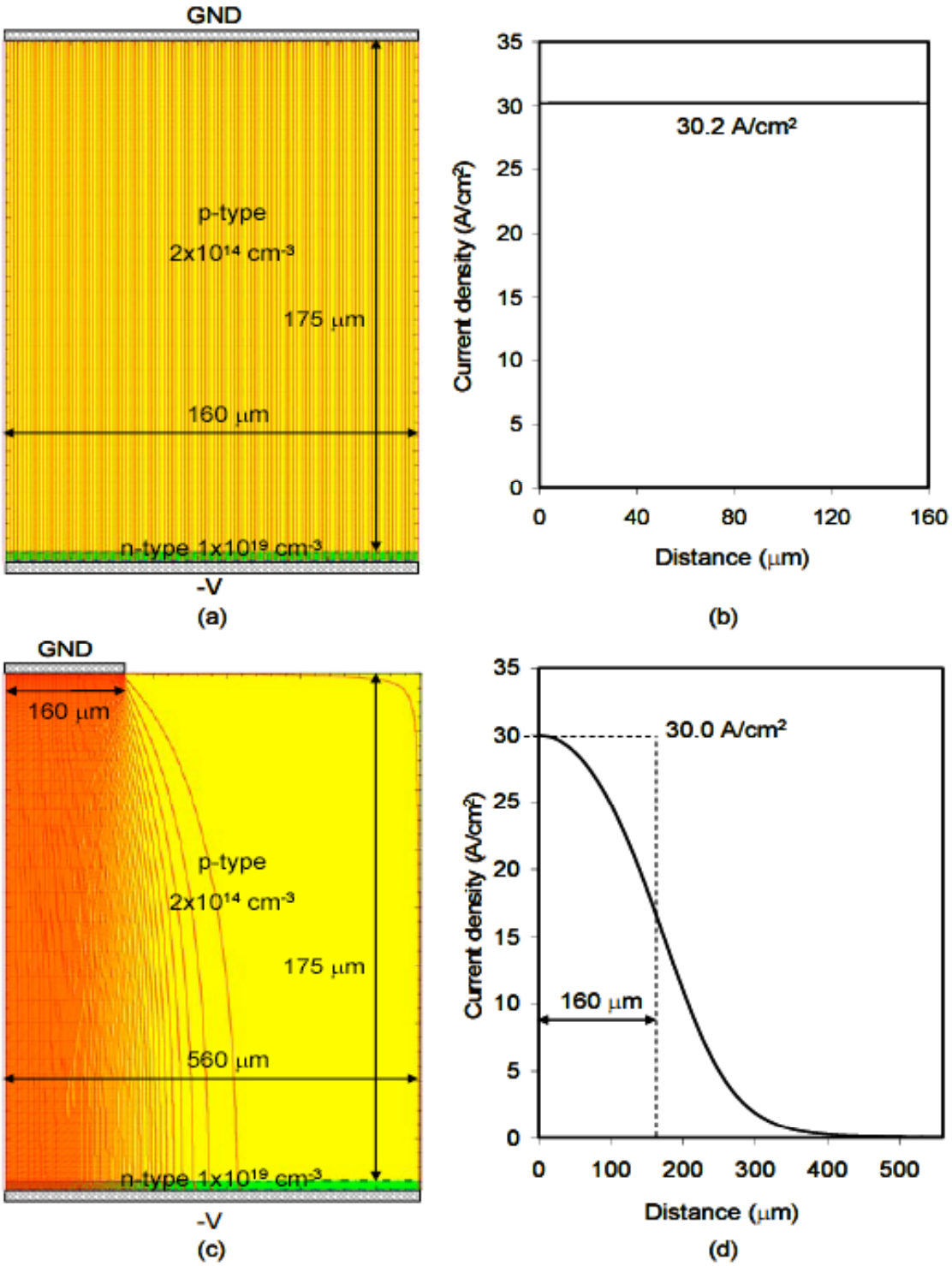


Fig. 3.45(a), (b) Simulation of an infinitely large diode current flow; (c), (d) simulation of a finite diode current flow, top contact width 228 μm, effective device width 220 μm.

3.1.4.1.4 High temperature performance of the P-IGBTs

Theoretically, SiC power IGBTs have excellent high temperature performance compared to power MOSFETs, as discussed earlier. We characterize the experimental P-IGBTs at room temperature and elevated temperature to verify our theory.

Figure 3.44 shows the I-V characteristics of an experimental P-IGBT at room temperature (circles) and 177°C (squares). Both curves intercept with the 300 W/cm^2 constant power line at around 28 A/cm^2. Beyond this point, the device carries higher current at 177°C than at room temperature. This is in good agreement with the simulation result, as shown in the inset of Fig. 3.44. The only difference is that the theoretical curves cross over at a higher current density. According to numerical simulation results, the optimized 20 kV SiC MOSFET carries a maximum of 15 A/cm^2 current at 177°C under the same power limit. Therefore, the experimental P-IGBTs outperform the theoretical MOSFETs by nearly 2x at elevated temperature. This is a major benefit for developing P-IGBTs because the junction temperature will be elevated during continual operation.

3.1.4.1.5 Reverse characteristics of the P-IGBTs

The p-channel IGBTs are designed to block 20 kV at their full capacity. According to Sze, the breakdown voltage of an unterminated junction can be as low as 5% of its full capacity depending on the shape and radius of the junction [5]. Due to the primary focus of this study, most of the P-IGBTs are designed without edge termination. It has been reported that the width of a full edge termination should be three times the drift layer thickness [70]. On the experimental samples, only a few P-IGBTs have partial edge terminations. Figure 3.45 shows the reverse characteristics of an unterminated P-IGBT and a partially terminated P-IGBT. The unterminated P-IGBT blocks around 1650 V, which is 6.6% of the theoretical blocking voltage. It agrees with Sze's theory. The P-IGBT with partial edge termination (400 μm wide) blocks around 4200 V. In order to achieve full blocking capacity, the edge termination for 20 kV P-IGBTs has to be over 1.7 mm wide [70], which costs significant amount of wafer area.

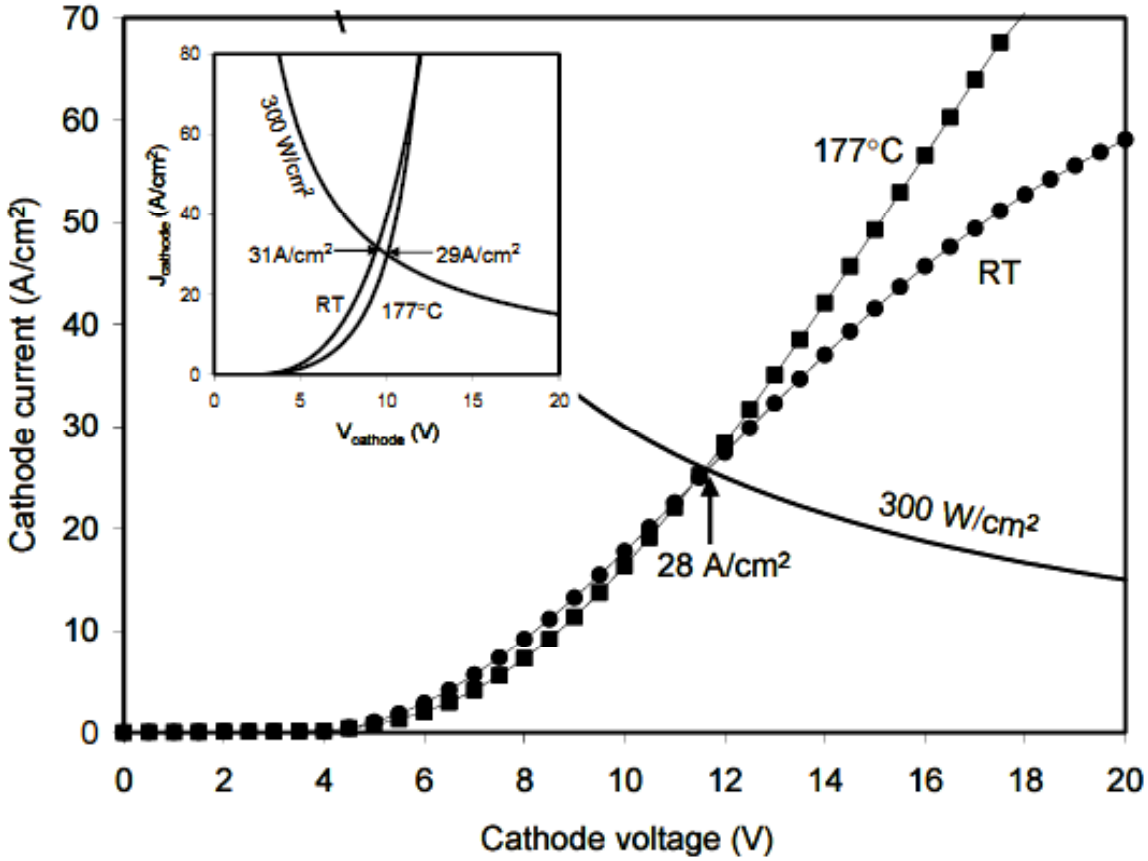


Fig. 3.44 I-V characteristics of an experimental P-IGBT at room temperature (circles) and 177°C (squares). The inset shows the simulation result of the P-IGBT's I-V at room temperature and 177°C.

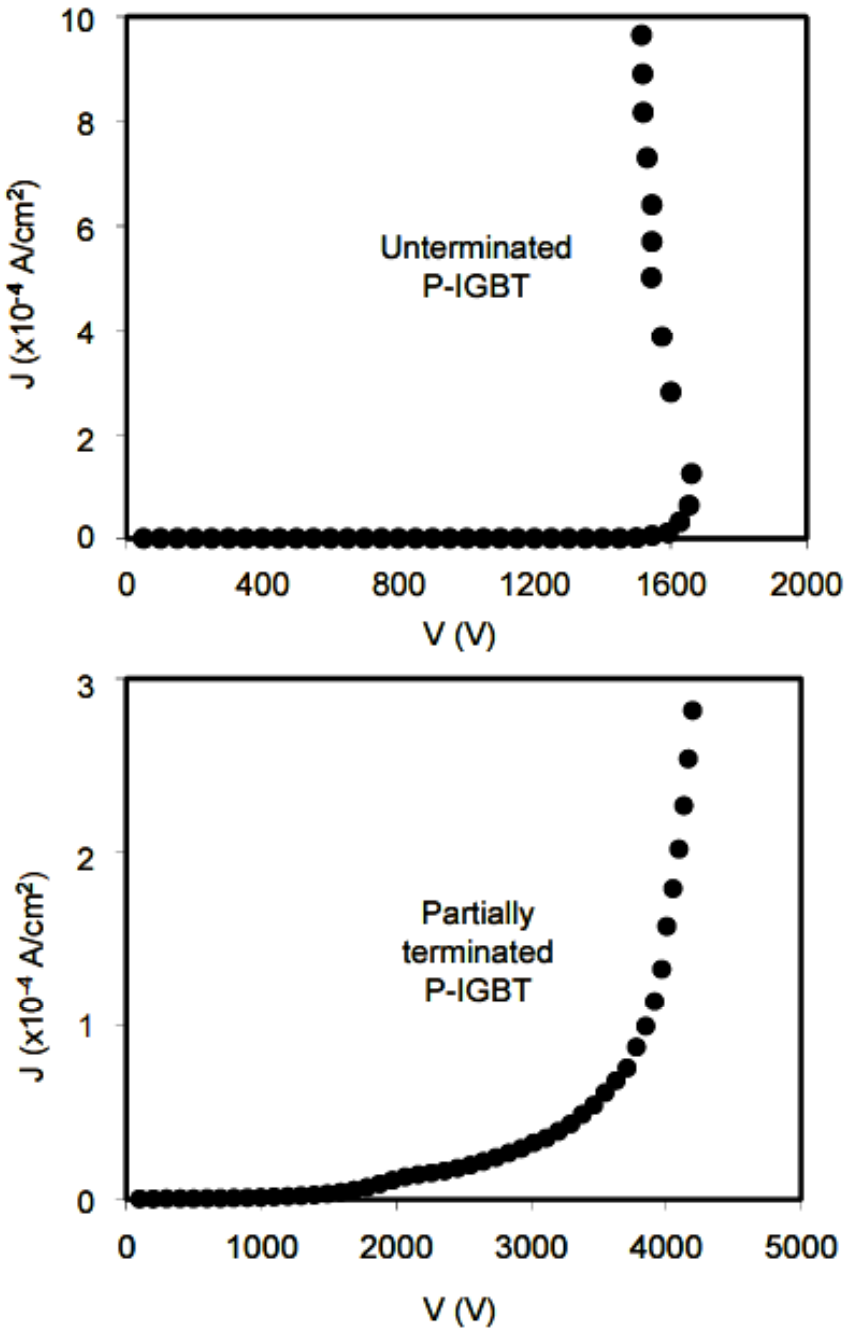


Fig. 3.45 Reverse characteristics of an unterminated P-IGBT and a partially terminated P-IGBT.

3.1.4.2 P-channel mobility measurement

The inversion channel mobility is one of the most important parameters for MOS transistors. P-IGBTs are no exception. The majority current of the device is hole current through the p-type MOS channel. Therefore, high channel mobility is essential for good on-state performance.

Due to the difficulty in making ohmic contacts to 4H-SiC material, the source and drain contact resistances may be nonlinear and may depend on gate voltage [33]. Lu et. al developed a constant current technique [71] to extract channel mobility from unannealed devices. Using this technique, the errors due to nonlinear source/drain contacts or gate voltage dependence can be eliminated [33].

Three mobility MOSFETs with different channel length (L) are investigated. The mobility MOSFETs have an n-well implantation profile as listed in Table 3.5. The source to drain voltage (V_{ds}) at a constant drain current (I_d) is measured under six different gate voltages (V_g).

The drain current for a MOSFET in the linear region (small V_{ds}) is given as

$$I_d = \mu_{eff} C_{ox} W (V_g - V_t) \frac{V_{ds}}{L} = \mu_{eff} C_{ox} W (V_g - V_t) E_{eff} \qquad (5.4)$$

where μ_{eff} is a function of V_g, and E_{eff} is the tangential electric field in the channel. By plotting V_{ds} versus L for a constant V_g and I_d, the slope of the trendline is E_{eff}. Six E_{eff} values can be obtained for six different V_g. All the V_{ds} - L lines should intercept approximately at the same point, which indicates the voltage drop across the source/drain contacts (at zero channel length). The sheet conductance of the channel is defined as

$$G_{ch}(V_g) = I_d / (W E_{eff}) = C_{ox} \mu_{eff} (V_g - V_t) \qquad (5.5)$$

The threshold voltage (V_t) is given by the intersection of the abscissa and the linear portion of the G_{ch} versus V_g curve. Finally, the effective mobility can be obtained from

$$\mu_{eff} = \frac{G_{ch}}{C_{ox}(V_g - V_t)} \qquad (5.6)$$

Figure 3.46 shows the plot of source to drain voltage vs. channel length at a gate voltage of -19 V to -24 V. A linear trendline can be extrapolated for each gate voltage. The slopes of each line indicate the electric field in the channel at the specific gate voltage,

which are listed in Table 3.9 as E_{eff}. The sheet conductance G_{ch} for each V_g can then be calculated from equation (5.5), given I_d = 10 nA and W = 110 μm. The inset of Fig. 3.46 shows the G_{ch} vs. V_g plot. The threshold voltage (V_t = -18 V) is indicated in the figure. The gate oxide capacitance can be easily calculated knowing the oxide thickness (T_{ox}).

$$C_{ox} = \frac{K_{ox}\varepsilon_0}{T_{ox}} = 6.903\times10^{-8}\,F/cm^2 \qquad (5.7)$$

Therefore, the field dependent effective channel mobility can be obtained from equation (5.6). The μ_{eff} values for different V_g are listed in Table 3.9. The peak mobility of 5.64 cm^2/Vs occurs at a gate voltage of -19 V. It is possible for the mobility to be higher at a lower gate voltage. But due to the high threshold voltage (-18 V), these data are not available at this time. The experimentally measured channel mobility is quite close to the assumption of 7.5 cm^2/Vs in the numerical simulations.

Obviously, high p-channel mobility is desired for P-IGBTs. Several new gate oxidation or post-oxidation annealing techniques have been developed to improve the n-channel mobility [72-74]. Whether these techniques are suitable for improving p-channel mobility has to be verified experimentally.

Table 3.9 Parameters for calculating p-channel mobility

V_g (V)	E_{eff} (V/cm)	G_{ch} (Ω^{-1})	μ_{eff} (cm^2/Vs)
-19	2.335	3.89×10^{-7}	5.64
-20	1.621	5.61×10^{-7}	4.06
-21	1.155	7.87×10^{-7}	3.80
-22	0.854	1.06×10^{-6}	3.86
-23	0.647	1.41×10^{-6}	4.07
-24	0.505	1.80×10^{-6}	4.35

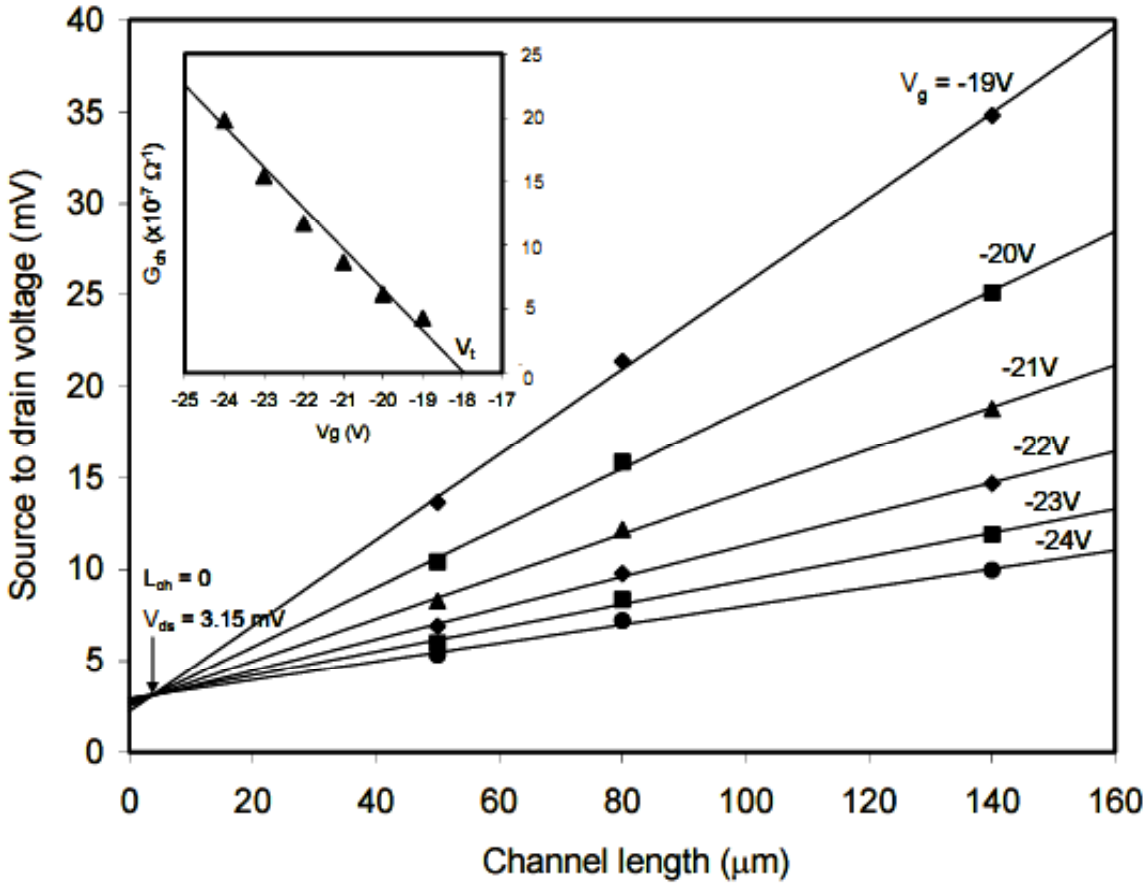


Fig. 3.46 Source to drain voltage vs. channel length for mobility MOSFETs. The channel lengths for the mobility MOSFETs are 50 μm, 80 μm, and 140 μm. The inset shows the channel sheet conductance vs. gate voltage. The threshold voltage is -18 V.

3.1.4.3 Threshold voltage

Due to the lack of literature for the p-type MOS channel properties, we design different threshold adjustment implants on several samples to maximize the chance of getting the right threshold voltage. The detailed implant profiles are listed in Table 3.4 to Table 3.6.

Figure 3.47 shows the threshold voltage measurement on a P-IGBT with no threshold adjustment implant and a P-IGBT with $1x10^{13}$ cm^{-2} Al implant. The shift in threshold voltage is $\Delta V_t = 4.1$ V. If we consider the implanted Al ions to behave like fixed charges, the threshold voltage shift is given by

$$\Delta V_t = \frac{Q_F}{C_{ox}} = \frac{qN}{C_{ox}} \tag{5.8}$$

Some of the implanted Al ions are consumed by oxidation during fabrication. The remaining activated Al ions are

$$N = \frac{C_{ox}\Delta V_t}{q} = 1.7 \times 10^{12}\, cm^{-2} \tag{5.9}$$

From the profile of the Al implantation (Fig. 3.30), we can assume that approximately 15% of the implanted Al ions are consumed during the gate oxidation (~ 25 nm of SiC consumed). Therefore, the activation percentage is approximately 20%.

Obviously, the threshold voltages on the samples are high. Providing the critical oxide field of 4 MV/cm, the amount of inversion charge is limited if the threshold voltage is too high. In order to have an appropriate threshold voltage (~ -3 V), we may use a heavier dose of Al ions as threshold adjustment implant. However, it is hard to have an accurate control of the activation percentage of implanted Al ions. The best control is only within ±50% [15]. Another way of adjusting V_t is to change the n-well surface doping level. It will be much easier to control the n-type doping level because the activation ratio of nitrogen ions is almost 100%. But we must make sure that the short channel does not get punched-through laterally from the p+ source due to the lower doping in surface region.

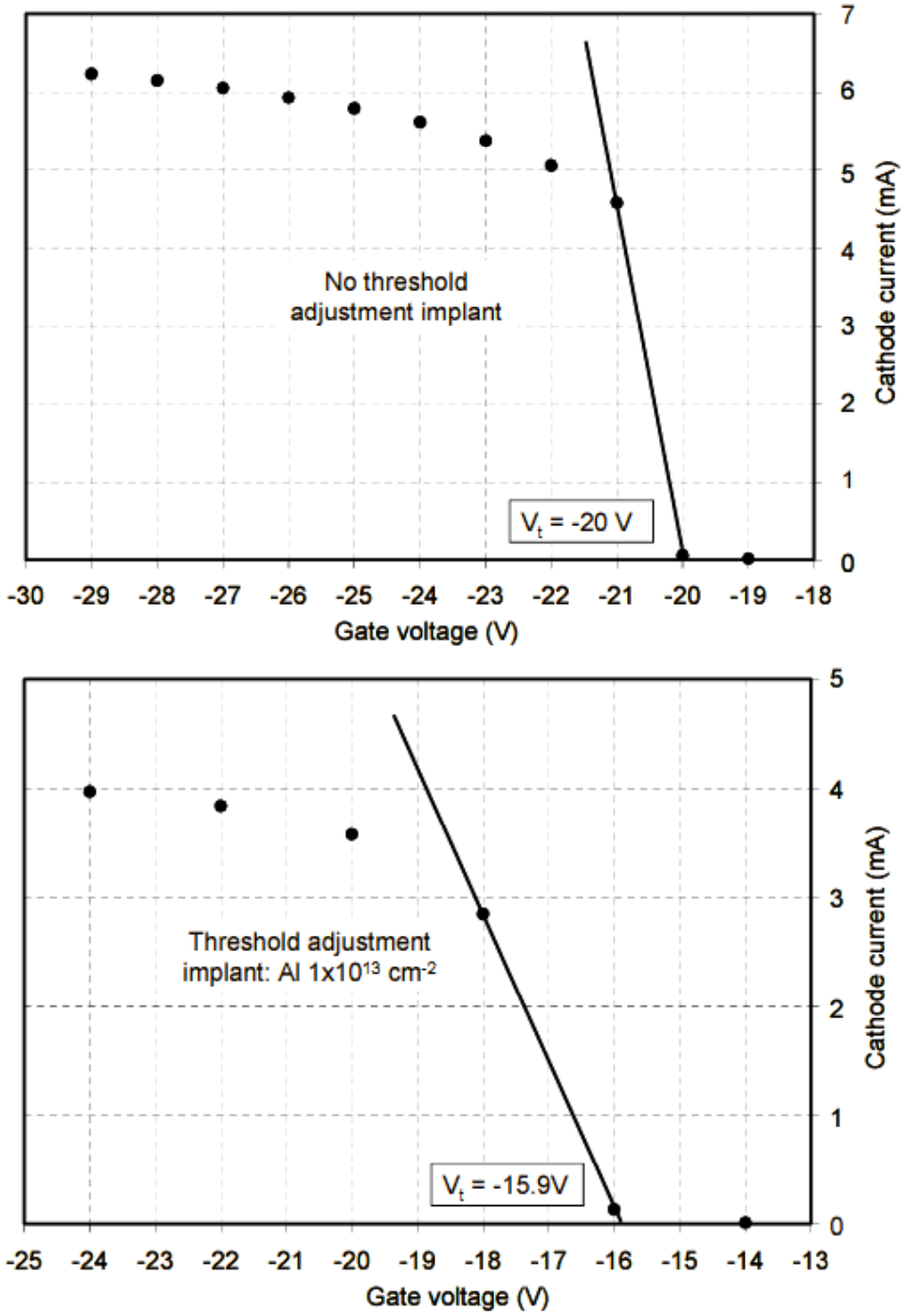


Fig. 3.47 P-IGBT threshold voltage measurement. Both samples have annealed contacts.

3.1.4.4 Contact resistivity

The contact resistivity for p-type and n-type ohmic contacts is measured using TLM testers. Figure 3.48 shows the photos of the n-type and p-type TLMs before and after contact annealing at 1000°C in vacuum for 2 minutes. The width of each rectangle is 110 μm, the length is 50 μm, and the spacing between contacts is 10 μm, 20 μm, 30 μm, 40 μm, and 50 μm.

The I-V curves of the N-TLM and P-TLM show nonlinear behavior. (Fig. 3.49 and Fig. 3.50). It indicates that neither contacts are exactly ohmic. In order to measure the contact resistivity from the nonlinear curves, we need to evaluate the total resistance (R_T = 1/slope) at the proper voltage, which is the voltage across the n-type contact of the P-IGBTs when operating at the power limit. At the 300 W/cm^2, we measure the source and base current density from type C devices to be 28.5 A/cm^2 and 3.5 A/cm^2.

Considering the base contact is 3 μm wide per half pitch (half pitch size for type C devices is 27.5 μm), the local current density through the n-type contact is

$$J_{n-contact} = 3.5 \bullet \frac{27.5}{3} = 32 A/cm^2 \tag{5.10}$$

Similarly, the source contact is 6 μm wide per half pitch, and the local current density through the p-type contact is

$$J_{p-contact} = 28.5 \bullet \frac{27.5}{6} = 131 A/cm^2 \tag{5.11}$$

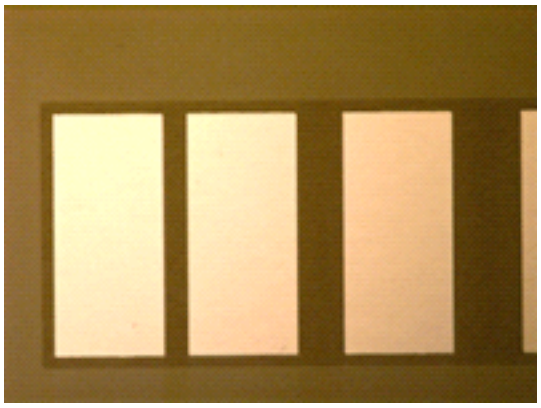
If we consider the same local current density through the TLMs (area = 5.5x10^{-5} cm^2), the current should be 1.76 mA and 7.21 mA through n-type and p-type TLMs, respectively.

For N-TLMs, the I-V curves intercept with V = 3 V line at a current of 1.5 ~ 3 mA, which is around the current level of 1.76 mA. We measure the slopes for difference spacing by connecting the origin and the points at 3 V with a straight line. The total resistance is plotted vs. spacing in the lower plot of Fig. 3.49. The sheet resistance (1606 Ω/square) and contact resistivity (0.015 Ωcm^2) are extracted from a linear fit to the points. The voltage drop across the n-type contact of a P-IGBT at 300 W/cm^2 is 32 x 0.015 = 0.48 V. It is a reasonably low voltage across the contact.

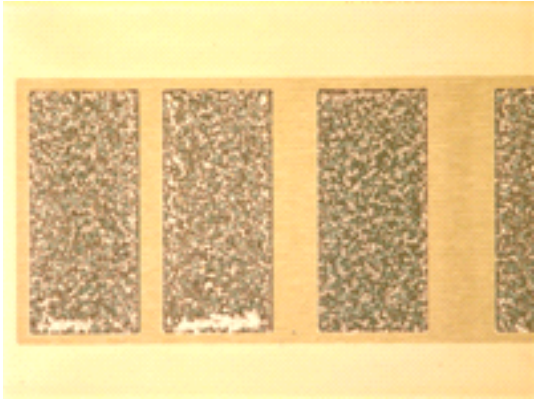
We can use the same method to calculate for the p-type contacts. The only difference is that the sheet resistance for the P-TLMs is very high, which leads to very low current. The current does not reach 7.21 mA until a very high voltage. Fortunately, the I-V curves of the P-TLM are much more linear than that of the N-TLM. We can use the points at 5 V to estimate the total resistance. According to Fig. 3.50, the sheet resistance and contact resistivity of the p-type contacts are 2.06×10^5 Ω/square and 0.038 Ωcm^2, respectively. Therefore, the voltage across the source contact of a P-IGBT at the power limit is131 x 0.038 = 4.98 V. This high source contact voltage contributes to the high threshold voltage of the P-IGBTs as well.

According to our previous successful experiences on ohmic contacts, the problem causing the high contact resistivity could be contaminations in the metal source, poor vacuum during metal evaporation and contact annealing, and temperature deviation during the annealing. Another possible reason for the Schottky behavior of the Ni contacts is that Ti/Al covers Ni on all n-type contacts, which may adversely affect the alloy composition and the reaction between Ni and SiC during the annealing.

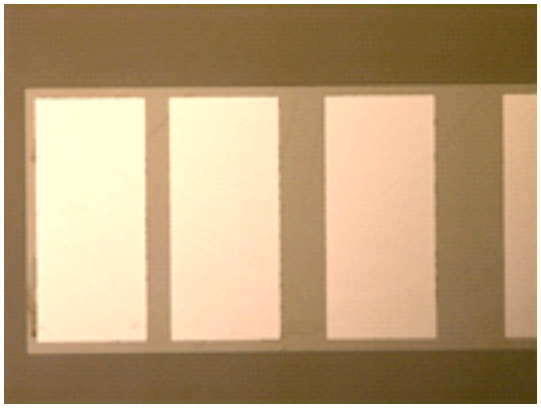
Once the problem is identified, we should be able to get both types of ohmic contacts in the range of 10^{-4} Ωcm^{-2}, which will further improve the device on-state performance.



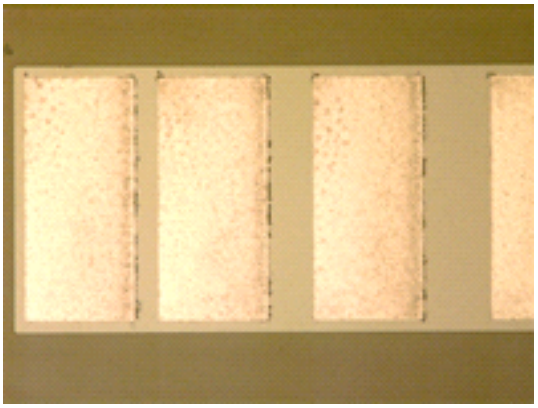
(a) N-TLM before contact annealing



(b) N-TLM before contact annealing



(c) P-TLM before contact annealing



(d) P-TLM before contact annealing

Fig. 3.48 Photos of n-type and p-type TLMs before and after contact annealing

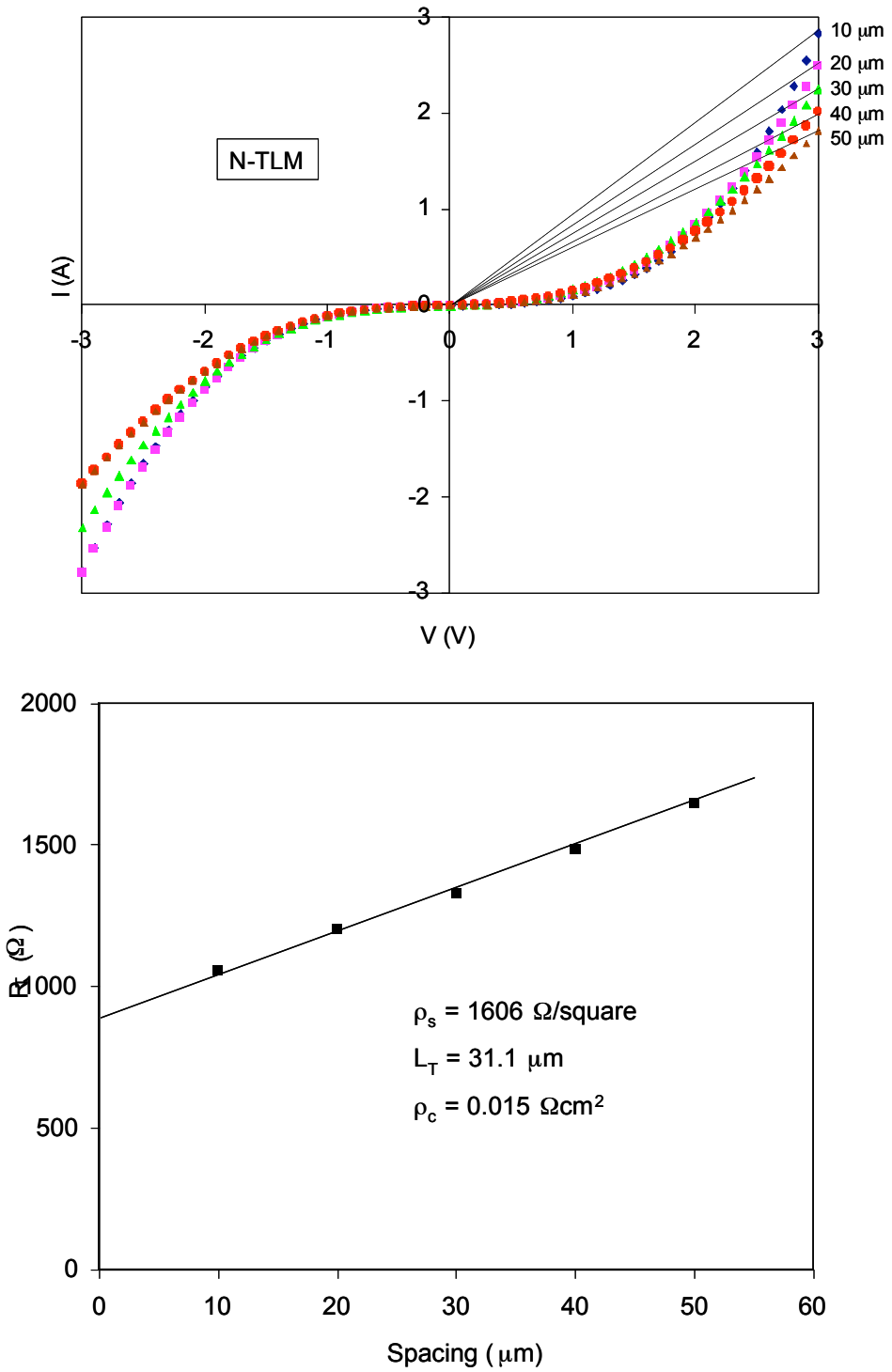
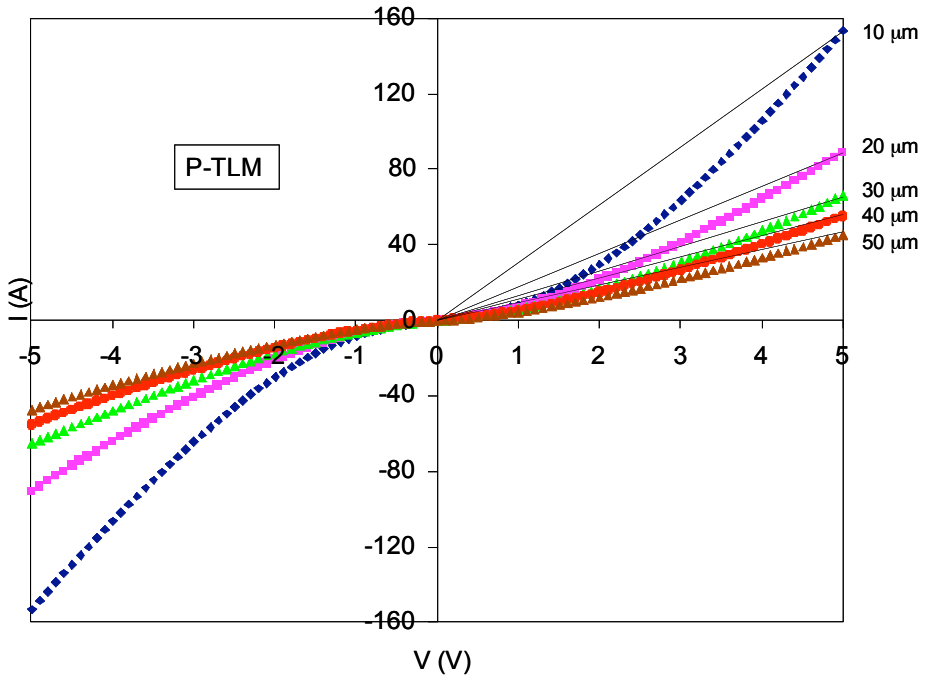


Fig. 3.49 I-V characteristics and contact resistivity extraction for n-type TLM



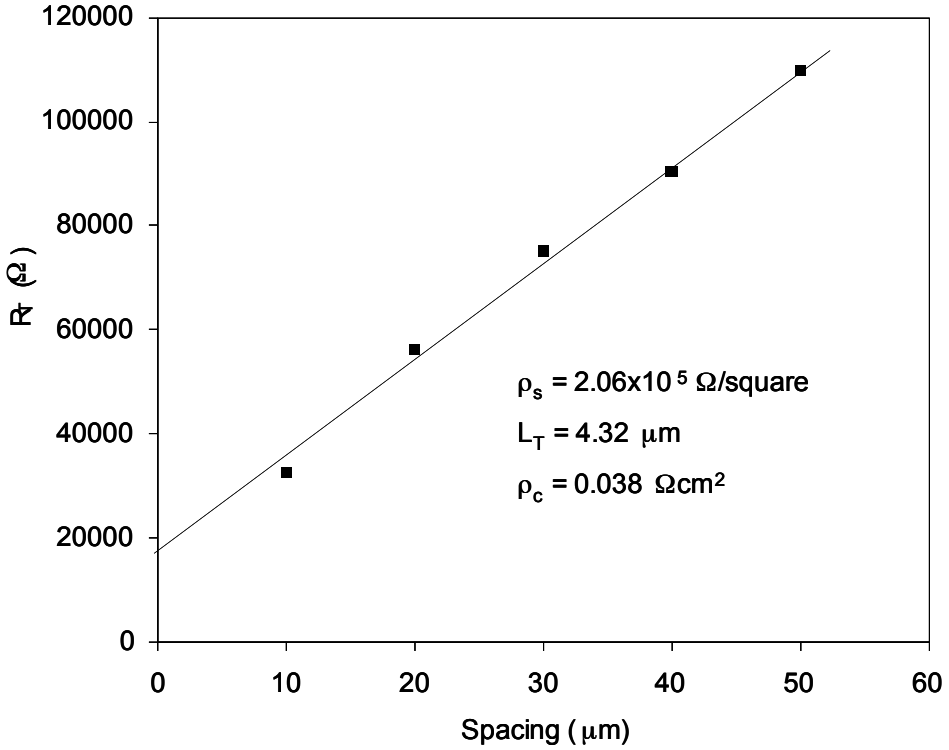


Fig. 3.50 I-V characteristics and contact resistivity extraction for p-type TLM

3.1.5 Summary of Results for the High-Voltage P-Channel IGBT

We have successfully achieved our primary goal of this project, designing and fabricating the first 4H-SiC P-channel IGBT on a drift layer capable of blocking 20 kV.

We extensively use Medici^{TM} numerical simulation for understanding the device performance and optimizing the device design. We compare the theoretical performance of 20 kV MOSFETs and 20 kV P-IGBTs side by side and conclude that the P-IGBTs have great advantages over the MOSFETs in terms of design/process window, on-state current density, and high temperature performance.

The processing steps of the P-IGBTs are almost identical to that of DMOSFETs, i.e., we get all the benefits of the IGBTs almost *for free*. Ambipolar lifetime in the drift region is a crucial material parameter for the on-state performances of IGBTs. Currently, the best lifetime in p-type epilayer is still under 0.5 μs. A lot of research in crystal growth technology has to be done to improve the ambipolar lifetime of 4H-SiC in the future.

We have successfully fabricated the first 4H-SiC short-channel P-IGBT on a drift layer capable of blocking 20 kV by adopting the process of short-channeled DMOSFETs. The on-state performances of the experimental P-IGBTs are very close to the simulation results. Almost 100% of the theoretical on-current has been achieved under the 300 W/cm^2 power dissipation limit. The experimental P-IGBTs do not show degradation at high temperatures. In fact, the experimental P-IGBTs outperform the theoretical MOSFETs by 2x at 177°C. This is a major advantage of SiC power IGBTs over MOSFETs.

SiC power MOSFETs blocking over 10 kV face the inevitable problem of high on-state drift layer resistance. They are not suitable for such high voltage applications. We believe that SiC p-channel IGBT is an excellent candidate for the next generation power switching device that blocks 10 kV and above.

There are still several process issues for the P-IGBTs. The p-type inversion channel mobility needs to be improved since the majority of current flows through the MOS channel. The channel current is also the base current of the npn bipolar transistor.

Research on gate oxidation and post-oxidation annealing specifically for improving the SiC p-channel mobility needs to be done.

Having longer ambipolar lifetime may be the most effective way to improve the on-state performance of IGBTs. It requires research in the field of CVD epitaxial growth technology.

We still do not repeatably get good results on n-type and p-type ohmic contacts. The contact alloy composition, the conditions for depositing the metals, and the conditions for contact annealing all need to be refined. Contact annealing is critical because it is almost the last process the device undergoes and it is irreversible. A failed contact anneal is going to lead to useless devices.

Another critical high temperature step is the implant activation annealing. It has been shown in the P-IGBTs that the rough surface in the p+ source region leads to premature oxide breakdown during on-state operation. This increased roughness is caused by the step-bunching during the contact annealing. We are considering lowering the source region implant dose to minimize the lattice damage from the implanted ions. A possible better way of solving this problem is to use the graphite capped anneal to prevent Si sublimation during the annealing.

Although we made efforts to optimize the P-IGBTs design, further design improvement is possible. It has been demonstrated by numerical simulation that making the JFET length narrow helps shield the gate oxide over the JFET region in the blocking state. The doping level in the JFET region has to be higher if a narrower JFET length is used. Introducing a current spreading layer under the n-well may help improve the overall on-state current density. Complete edge terminations are required for the P-IGBTs to exhibit the full blocking capacity. This requires over 1.7 mm wide float field rings for each 20 kV P-IGBT, which consumes a large area.

We are still not clear about the discrepancy between the P-IGBTs theoretical electron/hole current distribution and the experimental results. Further investigation and modeling for the on-state performance inside the device is necessary.

In this study, we focus mainly on the on-state performance of the P-IGBTs. The blocking state and the transient performances are equally important for power transistors. Further study in these areas needs to be done in the future.

3.1.6 Bibliography for Section 3.1

[1] J. Tan, "An optimized SiC power UMOSFET," Ph.D. thesis in School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 1998.

[2] J. B. Casady and R. W. Johnson, "Status of SiC as a wide-bandgap semiconductor for high temperature applications," *Solid State Electronics*, vol. 39, pp. 1409-1422, 1996.

[3] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindfelt, "Ionization rates and critical field in 4H silicon carbide," *Applied Physics Letters*, vol. 71, pp. 90-92, 1997.

[4] J. W. Palmour, S. T. Allen, R. Singh, L. A. Lipkin, and D. G. Waltz, "4H-silicon carbide power switching devices," presented at Proceedings of the Sixth International Conference IOP Publishing, Bristol, UK, 1995.

[5] S. M. Sze, *Physics of Semiconductor Devices*, Second ed. New York: John Wiley & Sons, Inc., 1981.

[6] Y. Goldberg, M. E. Levinshtein, and S. L. Rumyantsev, *Properties of Advanced Semiconductor Materials GaN, AlN, SiC, BN, SiC, SiGe*. New York: John Wiley & Sons, Inc., 2001.

[7] Y. S. Protasov and Y. V. Boyko, *Thermodynamic and optical properties of plasma, metals, and dielectrics*. New York: Hemisphere Pub. Corp., 1991.

[8] J. W. Palmour, J. A. Edmond, H. S. Kong, and C. H. Carter, Jr., "6H-Silicon Carbide Power Devices for Aerospace Applications," presented at Proceedings of 28th Intersociety Energy Conversion Energy Conference, 1993.

[9] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and Prospects for SiC Power MOSFETs," *IEEE Transactions on Electron Devices*, vol. 49, pp. 658-664, 2001.

[10] J. Tan, J. A. Cooper, Jr., and M. R. Melloch, "High Voltage Accumulation-Layer UMOSFETs in 4H-SiC," *IEEE Electron Device Letters*, vol. 19, pp. 487-489, 1998.

[11] K. Hara, "Vital issues for SiC power devices," *Materials Science Forum*, vol. 264-268, pp. 901-906, 1998.

[12] Y. Sui, T. Tsuji, and J. A. Cooper, Jr., "On-state Characteristics of SiC Power UMOSFETs on 115-μm Drift Layers," *IEEE Electron Device Letters*, vol. 26, pp. 255-257, 2005.

[13] J. N. Shenoy, J. A. Cooper, Jr., and M. R. Melloch, "High-voltage double implanted power MOSFETs in 6H-SiC," *IEEE Electron Device Letters*, vol. 18, pp. 93-95, 1997.

[14] M. A. Capano, S.-H. Ryu, J. A. Cooper, Jr., M. R. Melloch, K. Rottner, S. Karlsson, N. Nordell, A. Powell, and D. E. J. Walker, "Surface roughening in ion implanted 4H-silicon carbide," *Journal of Electronic Materials*, vol. 28, pp. 214-218, 1999.

[15] M. A. Capano, S.-H. Ryu, M. R. Melloch, and J. A. Cooper, Jr., "Dopant activation and surface morphology of ion implanted 4H and 6H-silicon carbide," *Journal of Electronic Materials*, vol. 27, pp. 370-376, 1998.

[16] M. K. Das, J. A. Cooper, Jr., M. R. Melloch, and M. A. Capano, "Inversion channel mobility in 4H and 6H-SiC MOSFETs," presented at Semiconductor Interface Specialists Conference, San Diego, CA, 1998.

[17] P. M. Shenoy and B. J. Baliga, "The planar 6H-SiC ACCUFET: A New High-Volgate Power MOSFET Structure," *IEEE Electron Device Letters*, vol. 18, pp. 589-591, 1997.

[18] D. Peters, R. Schorner, P. Friedrichs, J. Volkl, H. Mitlehner, and D. Stephani, "1800 V triple implanted vertical 6H-SiC MOSFET," *IEEE Transactions on Electron Devices*, vol. 46, pp. 542-545, 1999.

[19] D. Takayama, Y. Sugawara, T. Hayashi, R. Singh, J. W. Palmour, S.-H. Ryu, and K. Asano, "Static and dynamic characteristics of 4-6 kV 4H-SiC SIAFETs," presented at IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD), Osaka, Japan, 2001.

[20] M. Matin, A. Saha, and J. A. Cooper, Jr., "A self-aligned process for high-voltage, short-channel vertical DMOSFETs in 4H-SiC," *IEEE Transactions on Electron Devices*, vol. 51, pp. 1721-1725, 2004.

[21] A. Saha, "SiC Short Channel Power DMOSFET: An Optimized Design," Ph.D. thesis in School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 2006.

[22] S.-H. Ryu, S. Krishnaswami, M. O'Loughlin, J. Richmond, A. Agarwal, J. W. Palmour, and A. R. Hefner, "10-kV, 123-mW-cm^2 4H-SiC Power DMOSFETs," *IEEE Electron Device Letters*, vol. 25, pp. 556-558, 2004.

[23] C. E. Weitzel, J. W. Palmour, C. H. Carter, Jr., K. Moore, K. J. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, "Silicon carbide high-power devices," *IEEE Transactions on Electron Devices*, vol. 43, pp. 1732-1741, 1996.

[24] A. Agarwal, J. B. Casady, L. B. Rowland, W. F. Valek, M. H. White, and C. D. Brandt, "1.1 kV 4H-SiC power UMOSFET's," *IEEE Electron Device Letters*, vol. 18, pp. 586-588, 1997.

[25] A. Agarwal, J. B. Casady, L. B. Rowland, W. F. Valek, and C. D. Brandt, "1400 V 4H-SiC power MOSFETs," *Materials Science Forum*, vol. 264-268, pp. 989-992, 1998.

[26] Y. Li, J. A. Cooper, Jr., and M. A. Capano, "High-performance UMOSFETs in 4H-SiC," *Materials Science Forum*, vol. 389-393, pp. 1191-1194, 2002.

[27] I. Khan, J. A. Cooper, Jr., M. A. Capano, T. Isaacs-Smith, and J. R. Williams, "High-voltage UMOSFETs in 4H SiC," presented at IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2002.

[28] P. Friedrichs, H. Mitlehner, K. O. Dohnke, D. Peters, R. Schorner, U. Weinert, E. Baudelot, and D. Stephani, "SiC power devices with low on-resistance for fast switching applications," presented at IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2000.

[29] S.-H. Ryu, A. Agarwal, J. Richmond, J. W. Palmour, N. Saks, and J. R. Williams, "27 mOhm-cm^2, 1.6 kV power DiMOSFETs in 4H-SiC," presented at IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2002.

[30] A. Agarwal, S.-H. Ryu, and J. W. Palmour, Cree, Inc., private communication.

[31] http://www.ecn.purdue.edu/WBG

[32] M. K. Das, B. S. UM, and J. A. Cooper, Jr., "Anomalously high density of interface states near the conduction band in SiO_2/4H-SiC MOS devices," *Materials Science Forum*, vol. 338, pp. 1069-1072, 2000.

[33] C.-Y. Lu, "Design and fabrication of high performance UMOSFETs," Ph.D. thesis in School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 2003.

[34] P. Jamet and S. Dimitrijev, "Hysical properties of N_2O and NO-nitrided gate oxides grown on 4H SiC," *Applied Physics Letters*, vol. 79, pp. 323-325, 2001.

[35] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J. W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *IEEE Electron Device Letters*, vol. 22, pp. 176-178, 2001.

[36] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide," *Applied Physics Letters*, vol. 76, pp. 1713-1715, 2000.

[37] H.-F. Li, S. Dimitrijev, H. B. Harrison, and D. Sweatman, "Interfacial characteristics of N_2O and NO nitrided SiO_2 grown on SiC by rapid thermal processing," *Applied Physics Letters*, vol. 70, pp. 2028-2030, 1997.

[38] K. Fukuda, S. Suzuki, T. Tanaka, and K. Arai, "Reduction of interface-state density in 4H-SiC n-type metal-oxide-semiconductor structures using high-temperature hydrogen annealing," *Applied Physics Letters*, vol. 76, pp. 1585-1587, 2000.

[39] L. A. Lipkin, M. K. Das, and J. W. Palmour, "N_2O Processing Improves the 4H-SiC: SiO_2 Interface," *Materials Science Forum*, vol. 389-393, pp. 985-988, 2002.

[40] R. Kosugi, S. Suzuki, M. Okamoto, S. Harada, J. Senzaki, and K. Fukuda, "Strong dependence of the inversion mobility of 4H and 6H SiC (0001) MOSFETs on the water content in pyrogenic re-oxidation annealing," *IEEE Electron Device Letters*, vol. 23, pp. 136-138, 2002.

[41] M. Ruff, H. Mitlehner, and R. Helbig, "SiC Devices: Physics and Numerical Simulation," *IEEE Transactions on Electron Devices*, vol. 41, pp. 1040-1054, 1994.

[42] P. A. Ivanov, M. E. Levinshtein, A. K. Agarwal, S. Krishnaswami, and J. W. Palmour, "Temperature Dependence of Current Gain in Power 4H-SiC NPN BJTs," *IEEE Transaction on Electron Devices*, vol. 53, pp. 1245-1249, 2006.

[43] R. F. Pierret, *Advanced Semiconductor Fundamentals (Modular series on solid state devices, volume VI)*: Addison-Wesley Publishing Company, Inc, 1989.

[44] J. A. Cooper, Purdue University, private communication.

[45] S.-H. Ryu, R. Singh, and J. W. Palmour, "High-power p-channel UMOS IGBT's in 6H-SiC for high temperature operation," *Materials Science Forum*, vol. 338-342, pp. 1427-1430, 2000.

[46] Q. Zhang, M. Gomez, E. Hanna, B. Luo, K. Boutros, B. Pierce, T. Isaacs-Smith, and J. R. Williams, "10kV Trench Gate IGBTs on 4H-SiC," 2004, pp. Rockwell Scientific Company, private communication.

[47] S.-H. Ryu, "Development of CMOS technology for smart power applications in silicon carbide," Ph.D. thesis in School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 1997.

[48] J.-Y. Lee and C.-F. Huang, Purdue University, private communication.

[49] O. Kordina, C. Hallin, A. Henry, and J. P. Bergman, "Growth of SiC by "Hot-Wall" CVD and HTCVD," *Physica Status Solidi (B): Basic Research*, vol. 202, pp. 321-334, 1997.

[50] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC," *Ieee Transactions on Electron Devices*, vol. 48, pp. 1442-1447, 2001.

[51] M. E. Levinshtein, T. T. Mnatsakanov, P. A. Ivanov, R. Singh, J. W. Palmour, and S. N. Yurkov, "Steady-state and transient characteristics of 10 kV 4H-SiC diodes," *Solid-State Electronics*, vol. 48, pp. 807-811, 2004.

[52] A. K. Agarwal, P. A. Ivanov, M. E. Levinshtein, J. W. Palmour, S. L. Rumyantsev, and S. H. Ryu, "Turn-off performance of 2.6 kV 4H-SiC asymmetrical GTO thyristor," *Semiconductor Science and Technology*, vol. 16, pp. 260-262, 2001.

[53] A. M. Goodman, J. P. Russell, L. A. Goodman, C. J. Nuese, and J. M. Neilson, "Improved COMFETs with fast switching speed and high-current capability," presented at Technical Digest - International Electron Devices Meeting, 1983.

[54] D. T. Morisette, "Development of robust power schottky barrier diodes in silicon carbide," Ph.D. thesis in School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 2001.

[55] A. R. Hefner and D. L. Blackburn, "An Analytical Model for the Steady-State and Transient Characteristics of the Power Insulated-Gate Bipolar-Transistor," *Solid-State Electronics*, vol. 31, pp. 1513-1532, 1988.

[56] *Medici Two-Dimensional Device Simulation Program*. Sunnyvale, CA, 1997.

[57] S. Selberherr, *Analysis and simulation of semiconductor devices*. Wien, Austria ; New York: Springer-Verlag, 1984.

[58] I. Khan and J. A. Cooper, Jr., "Improved measurements of high-field drift velocity in silicon carbide," *Materials Science Forum*, vol. 338(1), pp. 761-764, 2000.

[59] H. E. Nilsson, E. Bellotti, M. Hjelm, and K. Brennan, "A comparison between different Monte Carlo models in simulation of hole transport in 4H-SiC," *Mathematics and Computers in Simulation*, vol. 55, pp. 199-208, 2001.

[60] S. K. Ghandhi, *Semiconductor power devices : physics of operation and fabrication technology*. New York: Wiley, 1977.

[61] W. J. Choyke and G. Pensl, "Physical properties of SiC," *MRS Bulletin*, vol. 22, pp. 25-29, 1997.

[62] J. N. Pan, J. A. Cooper, and M. R. Melloch, "Activation of nitrogen implants in 6H-SiC," *Journal of Electronic Materials*, vol. 26, pp. 208-211, 1997.

[63] N. S. Saks, A. K. Agarwal, S. H. Ryu, and J. W. Palmour, "Low-dose aluminum and boron implants in 4H and 6H silicon carbide," *Journal of Applied Physics*, vol. 90, pp. 2796-2805, 2001.

[64] S. E. Saddow, J. Williams, T. Isaacs-Smith, M. A. Capano, J. A. Cooper, M. S. Mazzola, A. J. Hsieh, and J. B. Casady, "High temperature implant activation in 4H and 6H-SiC in a silane ambient to reduce step bunching," *Materials Science Forum*, vol. 338, pp. 901-904, 2000.

[65] M. A. Capano, Purdue University, Private communication.

[66] K. A. Jones, M. A. Derenge, P. B. Shah, T. S. Zheleva, M. H. Ervin, K. W. Kirchner, M. C. Wood, C. Thomas, M. G. Spencer, O. W. Holland, and R. D. Vispute, "A comparison of graphite and AlN caps used for annealing ion-implanted SiC," *Journal of Electronic Materials*, vol. 31, pp. 568-575, 2002.

[67] S. Tanimoto, N. Kiritani, M. Hoshi, H. Okushi, and K. Arai, "Gate oxide with high dielectric breakdown strength after undergoing a typical power MOSFET fabrication process," *Materials Science Forum*, vol. 433, pp. 725-728, 2002.

[68] C.-Y. Lu, J. A. Cooper, T. Tsuji, G. Y. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, "Effect of process variations and ambient temperature on electron mobility at the SiO_2/4H-SiC interface," *IEEE Transaction on Electron Devices*, vol. 50, pp. 1582-1588, 2003.

[69] S. Dhar, Y. W. Song, L. C. Feldman, T. Isaacs-Smith, C. C. Tin, J. R. Williams, G. Y. Chung, T. Nishimura, D. Starodub, T. Gustafsson, and E. Garfunkel, "Effect of nitric oxide annealing on the interface trap density near the conduction bandedge of 4H-SiC at the oxide/(11-20) 4H-SiC interface," *Applied Physics Letter*, vol. 84, pp. 1498-1500, 2004.

[70] S.-H. Ryu, Cree Inc., private communication.

[71] C.-Y. Lu and J. A. Cooper, "A new constant-current technique for MOSFET parameter extraction," *Solid-State Electronics*, vol. 49, pp. 351-356, 2005.

[72] F. Allerstam, G. Gudjonsson, H. O. Olafsson, E. O. Sveinbjornsson, T. Rodle, and R. Jos, "High Field-Effect Mobility in 6H-SiC MOSFET with Gate Oxides Grown in Alumina Environment," vol. 483, pp. 837-840, 2005.

[73] G. Gudjonsson, H. O. Olafsson, F. Allerstam, P. A. Nilsson, E. O. Sveinbjornsson, H. Zirath, T. Rodle, and R. Jos, "High field-effect mobility in n-channel Si face 4H-SiC MOSFETs with gate oxide grown on aluminum ion-implanted material," *IEEE Electron Device Letters*, vol. 26, pp. 96-98, 2005.

[74] H. O. Olafsson, G. Gudjonsson, H. E. Nilsson, E. O. Sveinbjornsson, H. Zirath, T. Rodle, and R. Jos, "High field effect mobility in Si face 4H-SiC MOSFET transistors," *Electronics Letters*, vol. 40, pp. 508-510, 2004.

3.2 n-Channel IGBTs

3.2.1 Introduction and Background

In 1996, GE and RPI reported the first n-channel SiC IGBTs[5], but the device performance was unsatisfactory because of the high resistance of the SiC p+ substrate. Due to the incomplete ionization and low hole mobility, the resistance of SiC p+ substrate is typically as high as 0.8-1.0 Ω cm^2 and totally dominates all other resistances in the device. For this reason, SiC IGBTs on conventional p+ substrates are basically impractical.

In this project we employed a novel process, known as an *inverted growth* process to obtain the IGBT structure. This process is described in the following sections.

3.2.2 Design Considerations and Chip Layout

3.2.2.1 Reducing the Forward Voltage Drop V_F

3.2.2.1.1 Reducing the Thickness of the P+ Layer

The first attempts to produce a practical n-channel IGBT failed due to the highly resistive p+ SiC substrate, which serves as the p+ layer in the IGBT. Alternative ways to form the p+ layer are as follows.

1. After growing the n+ buffer layer and the n- blocking layer on the p+ substrate, reduce the substrate thickness to 3 μm by mechanical polishing (as shown in Fig. 3.51). However, the tolerance of current polishing technique is around 10 μm, which makes this approach infeasible.

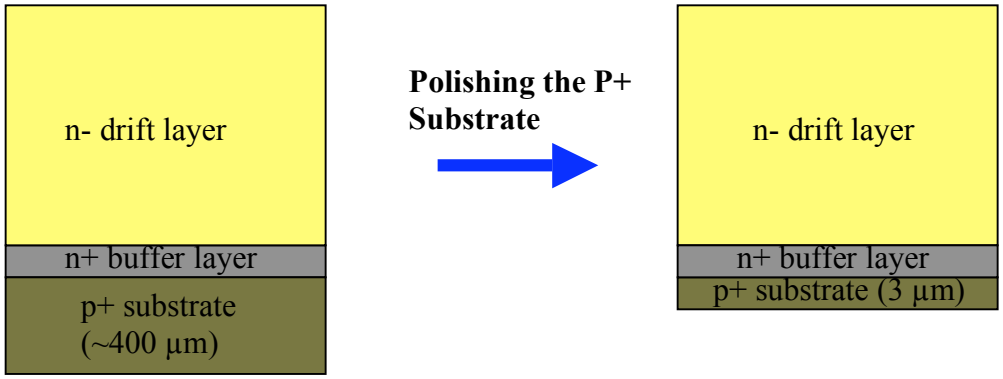


Figure 3.51 The first approach to reduce the p+ layer thickness.

2. First grow the n- blocking layer on a substrate and then remove the substrate by mechanical polishing, and form the n+ buffer and p+ anode layers on the back side of the n- layer (see Fig. 3.52). [1]

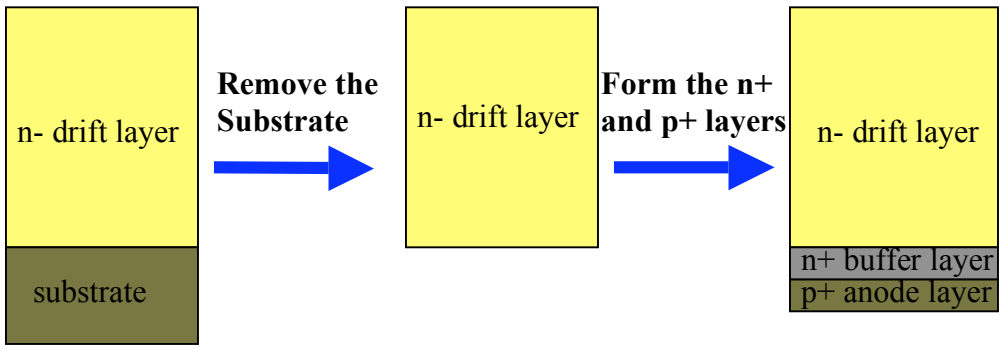


Figure 3.52 The second approach to reduce the p+ layer thickness.

[1] The n+ buffer layer and the p+ anode layer can also be grown on the top surface of the n- drift layer (See section 4.1.1.2 for detailed discussion on which surface to choose when growing these layers).

3. We could use a novel "inverted growth" process. As illustrated in Fig. 3.53, we first grow the n- blocking layer on a low BPD n+ substrate, followed by the epigrowth of a 0.2 μm n+ buffer layer and a 2-3 μm p+ anode layer. The n+ substrate is then removed and the wafer is flipped over. Now the p+ anode is on the bottom and n- blocking layer is on top. The devices will be fabricated on the top surface of the n- blocking layer.

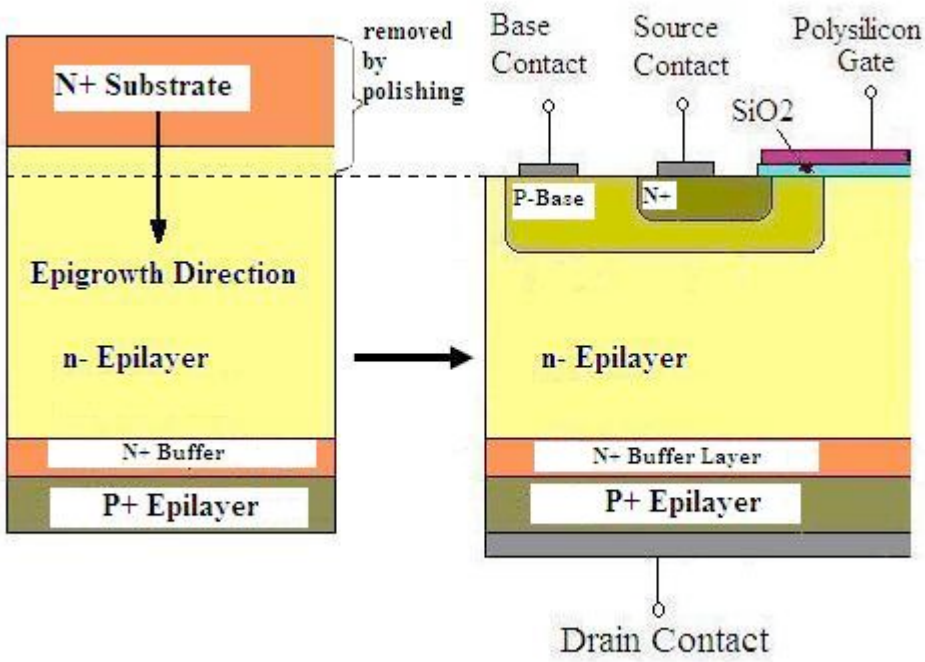


Figure 3.53 The "inverted growth" process employed in this project.

The "inverted growth" process is preferred over the second approach, because it allows *continuous* epigrowth of all critical layers in the IGBT on a low-BPD n+ substrate. The advantage of continuous epigrowth is reflected by a more stable forward voltage drop V_F. In the on-state, both electron and hole current flow into the drift region of a 4H SiC bipolar device, causing electron-hole recombination. The recombination provides energy to the lattice, allowing basal plane dislocations (BPDs) to generate stacking faults. A stacking fault becomes negatively charged by trapping electrons, and electron injection is attenuated at the cathode with a corresponding reduction of hole injection at the anode. The area under the fault becomes devoid of plasma, thereby reducing the effective current handling area. A larger forward bias is now needed to maintain the same forward current

level [7]. V_F may increase by several volts during operation [8]. Therefore, the key to stabilizing the forward voltage drop of 4H SiC bipolar devices is the reduction of BPDs. Figure 3.54 illustrates the V_F drift under constant current stress for both discontinuous epitaxy and continuous epitaxy [9]. The continuous growth helps reduce the defects at the metallurgical junction and therefore improves the stability of V_F.

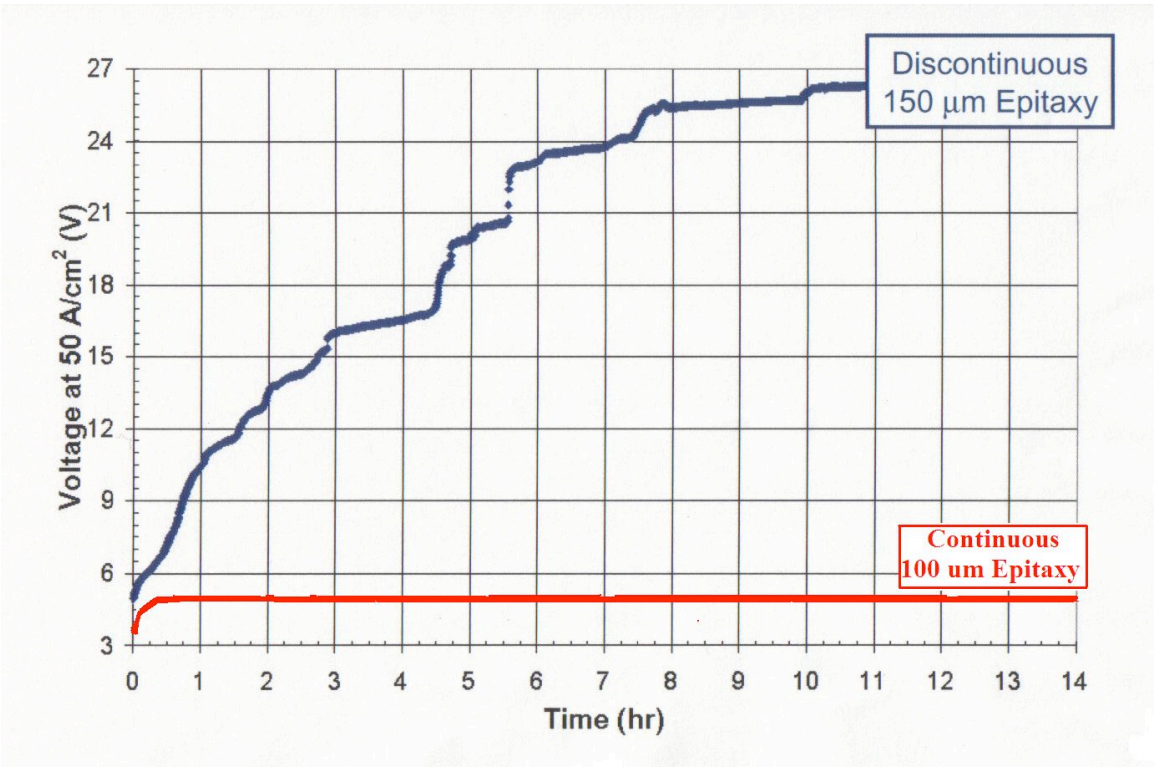


Figure 3.54 Stability of V_F for 4H-SiC PiN diodes. The critical layers of the diodes are grown by continuous epitaxy (red) and discontinuous epitaxy (blue).

The commercially available SiC wafers are usually grown on the Si-face of the substrate. The top surface of the grown epilayer is also Si-face. If the inverted growth sequence is used, devices will be fabricated on the backside of the n- epilayer, i.e. on the C-face. The oxidation rate on the C-face is considerably faster than Si-face and it was shown that the electrical quality of MOS interface on the C-face after NO annealing is comparable to that of Si-face [10]. Other processing steps on the C-face need to be studied during the fabrication.

No matter which approach is selected, the wafer would be about the same thickness as the original blocking layer alone. Then the question is whether or not the resulting wafer (150 µm -200 µm) is thick enough to survive the device processing.

Before committing to this process, we made two runs of simulated processing on thinned wafers. In the first run, two 50 mm Cree wafers with the thickness of 396 µm and 397 µm were thinned to around 218 µm by NovaSiC (Savoie Technolac, Arche Bat. 4, B.P.267, LE BOURGET DU LAC, 73370 France). Total thickness variation was 21 µm and 26 µm respectively. The first polished wafer had a bow of 40 µm and some scratches on the C-face. The second piece received a modified polishing procedure, and the bow was reduced to 6 µm. The first piece went through the optical lithography, e-beam evaporation of metal, lift-off and contact annealing without breaking. The condition for contact annealing is 950°C for 2 minutes and the ramping rate was about 15°C per second. Oxidation and implant annealing were performed on the other piece. During the pre-oxidation cleaning, a small piece was chipped off close to the flat of this wafer. During the subsequent dry oxidation, which is at 1150°C for 2 hours, a crack propagated from the broken area part-way across the wafer (see Fig. 3.55).

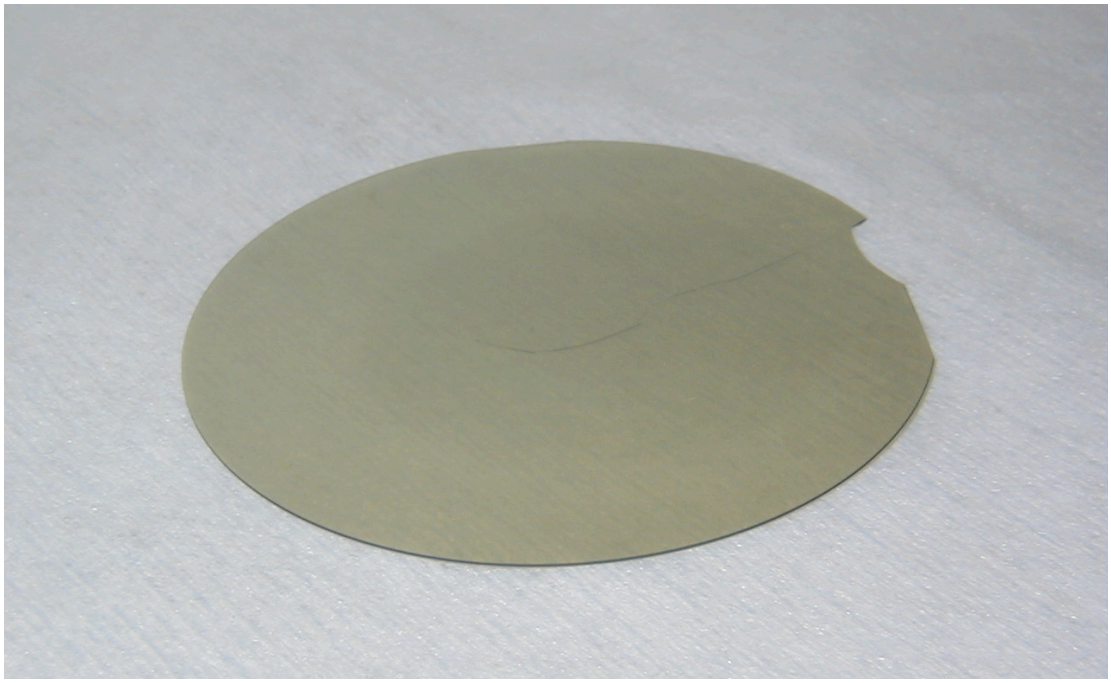


Figure 3.55 This 50 mm SiC wafer was thinned to 218 µm at NovaSiC. Then thermal oxidation at 1150 °C and simulated implant annealing at 1600 °C were performed on this wafer. During pre-oxidation clean, a small piece was broken near the edge, and a crack propagated from the broken area part way across the wafer. However, the crack did not propagate further during the second run of oxidation and implant annealing.

Later on, an operation flaw was found in this oxidation, that is, the wafer was loaded and unloaded at the oxidation temperature 1150 °C. A second run of oxidation was then performed on the same wafer under the same oxidation condition, except that the wafer was loaded at 450 °C and unloaded at 850 °C. The oxidation lasted for 1.5 hours. The crack didn't seem to propagate any further. Then, this wafer received a simulated implant annealing at 1600 °C. The crack didn't get bigger, either.

To test the sturdiness of even thinner wafers for device processing, another wafer of 397 µm thickness was sent to NovaSiC for thinning. The resulting thickness is 182 µm, with total thickness variation of 44 µm and a bow of 49 µm. There was a small piece missing at the edge when the wafer was received back from NovaSiC. Since the implant annealing gives the biggest thermal stress, a simulated implant annealing (at 1600 °C) was performed on this wafer to evaluate the high temperature processing steps. No change was observed on this wafer after the annealing (see Fig. 3.56). Since this thinned wafer has a 49 µm bow, the concern was whether or not it can survive the pressure in the exposure step of optical lithography, where it is sandwiched between a mask and a chuck. Therefore, a simulated optical lithography process was performed on this wafer. And it survived. Based on above results, we determined that it was feasible to fabricate devices on thinned wafers.

Figure 3.56 This 50 mm SiC wafer was thinned to 182 µm at NovaSiC. A small piece was broken at the edge as the wafer was received back from NovaSiC. It survived the simulated implant annealing at 1600 °C and the optical lithography process.

3.2.2.1.2 V_m and Ambipolar Lifetime

The voltage drop across the drift region, V_m, is a function of the ambipolar lifetime in the drift region. Figure 3.57 illustrates this dependence for different thicknesses of the drift region. The current density at which V_m is evaluated is 100A/cm^2. For each ambipolar lifetime, P_0 is first solved from equation (2.31). Then equation (2.28) is evaluated.

$$J_T = J_n + J_p = \frac{1+b}{b}\left\{\frac{P_0^2 J_{sne}}{n_i^2} + \frac{qD_a P_0}{L_a}\coth\left(\frac{w_d}{L_a}\right)\right\} \tag{2.31}$$

As shown, in order to keep V_m enough low, an ambipolar lifetime of 1.5 μsec or 2 μsec is required. O.Kordina et al reported lifetimes in this range in material grown by the hot-wall CVD process [11]. Figure 3.58 is the map of the minority carrier lifetime of a 30 mm diameter 4H-SiC epitaxial film. The temperature dependence of the minority carrier lifetime is also shown for two points of the wafer. The minority carrier lifetime is seen to increase with increasing temperature. During operation, the temperature in the device will rise, so lifetime increasing with temperature is a favorable property. The lifetimes of the materials used in this project will be discussed in section 3.2.3.

Another issue related to the lifetime is that in an ion implanted region of the semiconductor, lattice damaging exists, which could cause lifetime degradation. In the IGBT, the p-base region is ion implanted, which not only lowers the lifetime in the p-base region, but also the regions close to it. In order to evaluate how this degradation affects the on-state performance of the IGBT, the following simulation study was conducted. The simulated structure is a PiN diode, as shown in Fig. 3.59. Like the IGBT, the PiN diode is a bipolar device. In the on-state, the drift region of the PiN diode is conductivity modulated and the voltage drop across this region depends on the ambipolar lifetime. We assume that the p+ anode of the PiN diode is ion implanted, with an implantation depth of 0.5μm. We also assume that the implantation damage extends 0.5 μm further, i.e. the damaged region has a total depth of 1 μm. In the simulation, we manually set the lifetime in the damaged region to be 0.2 nsec, 2 nsec, 20 nsec, 200nsec and 2 μsec, with the lifetime in the rest of the device to be 2μsec, and observe the voltage drop in the on-state. Figure 3.60 shows the simulation results. As we can see, V_{on} is not affected prominently for a lifetime as low as 2 nsec. For the IGBT, the excess carrier density drops to zero at the junction of the p-well/n- drift region. This means there is not much conductivity modulation at that junction. The lowered lifetime will have an even

less effect on V_{on} of the IGBT than the PiN diode, so we think that the degradation of the carrier lifetime due to the implant damage may not seriously affect the on-state performance of the IGBT.

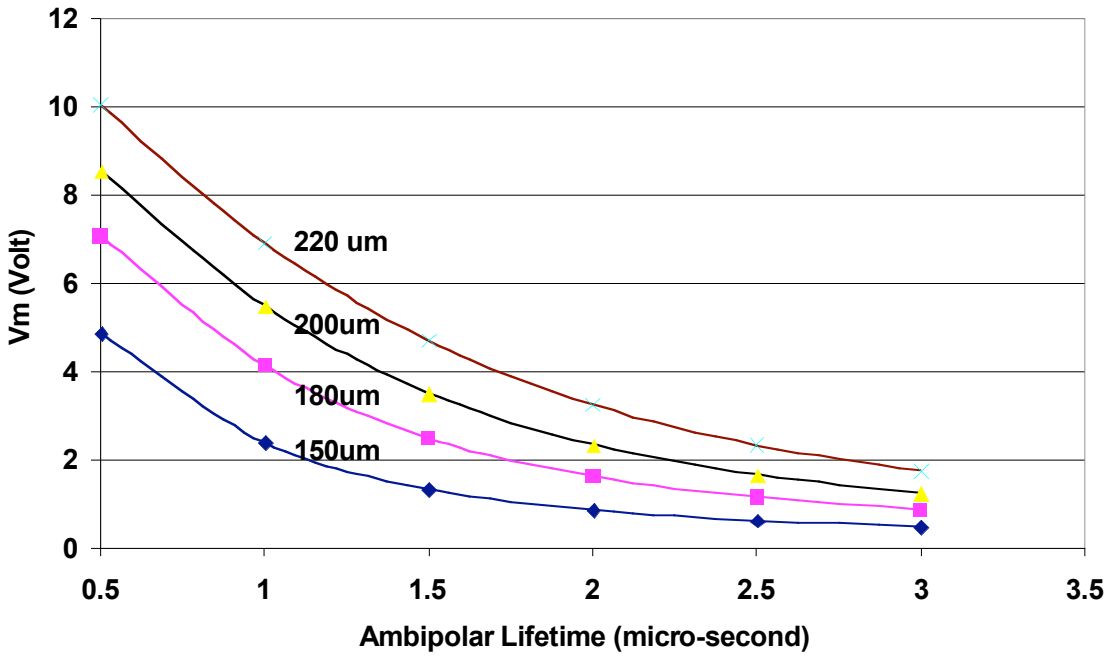


Figure 3.57 Voltage drop across the drift region vs ambipolar lifetime for different drift region thicknesses (150 µm, 180 µm, 200 µm and 220 µm). The doping level of the drift region is $2x10^{14}$ cm^{-3}, and the on-state current density is 25 A/cm^2. The data in this figure come from equation 2.28.

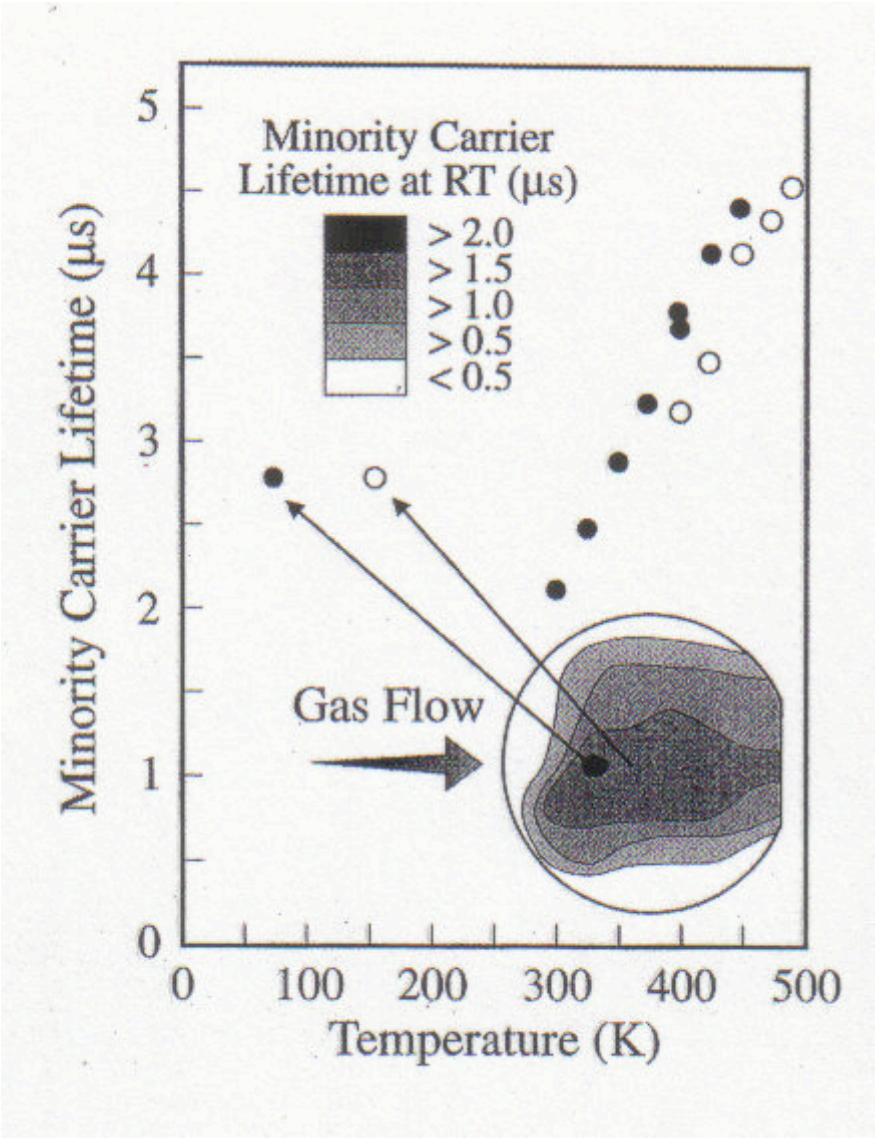


Figure 3.58 Minority carrier lifetime of a 30 mm diameter 4H-SiC epitaxial film grown by the hot-wall CVD process. The lifetime reaches its highest value close to the center of the wafer. The temperature dependence of the minority carrier lifetime for two points on the wafer is also demonstrated in the figure. It is shown that the minority carrier lifetime increases with increasing temperature. [12]

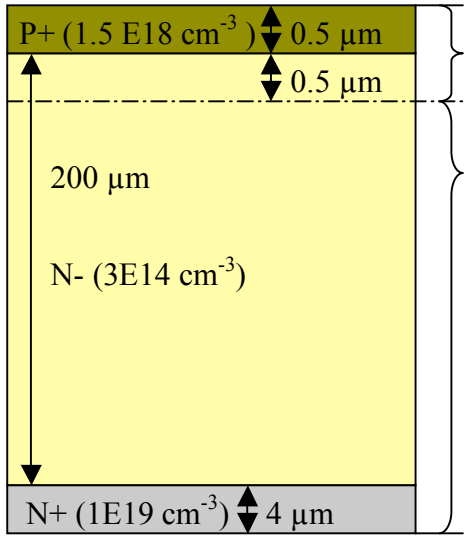


Figure 3.59 Parameters for the simulated PiN diode. This structure is used to study the effect of lifetime degradation in the implanted region on the on-state voltage drop.

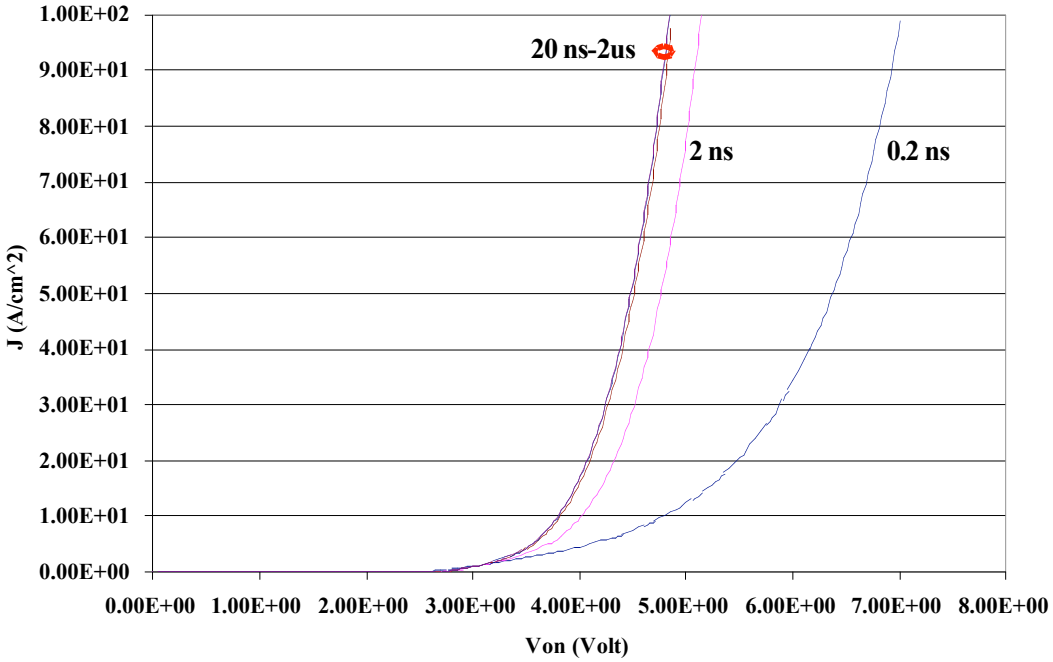


Figure 3.60 Simulation results for PiN diodes with lower lifetime in the region damaged by implant. As we can see, the forward voltage drop is not affected prominently for ambipolar lifetime of 2 ns and higher in the damaged region.

3.2.2.1.3 The Self-Aligned Short-Channel Process

To keep the voltage drop across the inherent MOSFET of the IGBT low, a small channel resistance is desired. There are two ways to reduce the channel resistance, increasing the inversion channel mobility and decreasing the length of the channel. At Purdue University, we use NO anneal after gate oxidation to reduce the density of the interface traps and therefore increase the inversion channel mobility. To realize the short channel, Pauline Matin et al developed a self-aligned process and achieved a 0.5 µm channel length. A self-aligned DMOSFET with 6µm epi-thickness was fabricated and has demonstrated an on-resistance as low as 6.95 mΩ cm^2 [13]. This means the voltage drop across the MOSFET portion of the IGBT could be less than (50 A/cm^2)(7 mΩ cm^2)=0.35 V, if the self-aligned process is adopted.

The self-aligned process is illustrated in Fig. 3.61. The processing steps are as follows. First, a patterned polysilicon layer is used as the mask for p-base implantation. Then, the polysilicon is oxidized and hence is expanded. This oxidized polysilicon serves as the mask for the n+ source implantation. The magnitude of the expansion determines the length of the channel (more details of the self-aligned process will be provided in a later section).

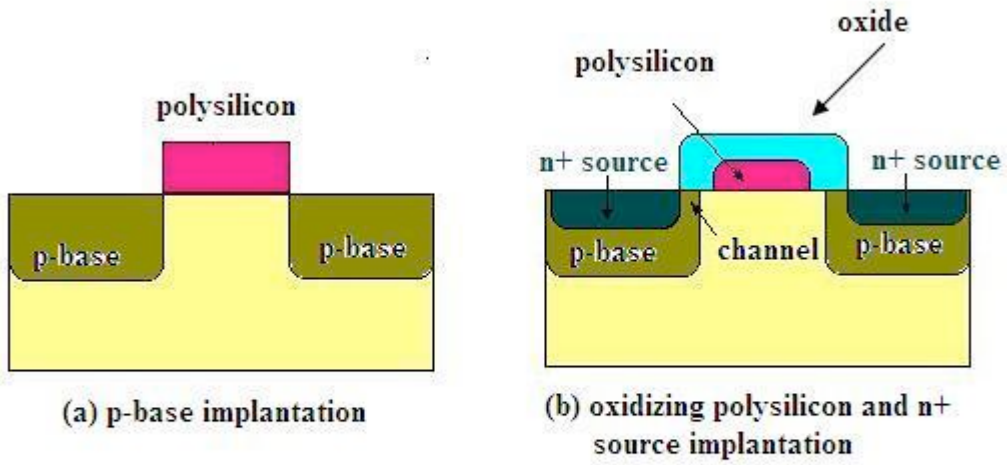


Figure 3.61 Overview of the self-aligned process.

3.2.2.1.4 Determination of JFET Width (L_J)

Due to the low doping concentration in the n- layer, the depletion region of the JFET in an IGBT is wider than a MOSFET. The depletion width can be evaluated by equation (2.32)

$$W_d = \left[\frac{2\varepsilon_{sic}}{q}\frac{N_A + N_D}{N_A N_D}V_{bi}\right]^{1/2} \approx \left[\frac{2\varepsilon_{sic}}{q}\frac{1}{N_D}V_{bi}\right]^{1/2} \tag{2.32}$$

where V_{bi} is the built-in potential, N_D is the doping concentration in the n- layer, and N_A is the doping concentration in the p-base. Assuming that $N_D \approx 3E14\ cm^{-3}$ and V_{bi} is about 3 V, then W_d is around 3.3 µm.

The width of the JFET region determines the magnitude of the JFET resistance and therefore affects V_F. In order to find a suitable JFET length, MEDICI simulations were conducted. The parameters used in the simulation are shown in Fig. 3.62. Notice that the width of the JFET region in Fig. 3.62 is one half of the real device. So the L_J simulated were actually 4, 6, 12 and 18 µm. The simulation results are shown in Fig. 3.63. L_J=12 µm is selected for this design.

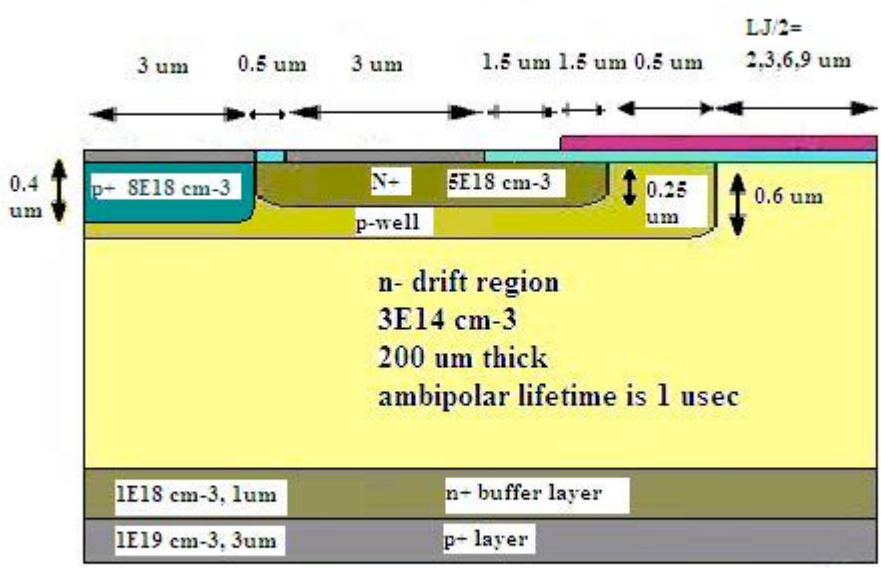


Figure 3.62 Structure simulated to determine L_J and parameters used in the simulation.

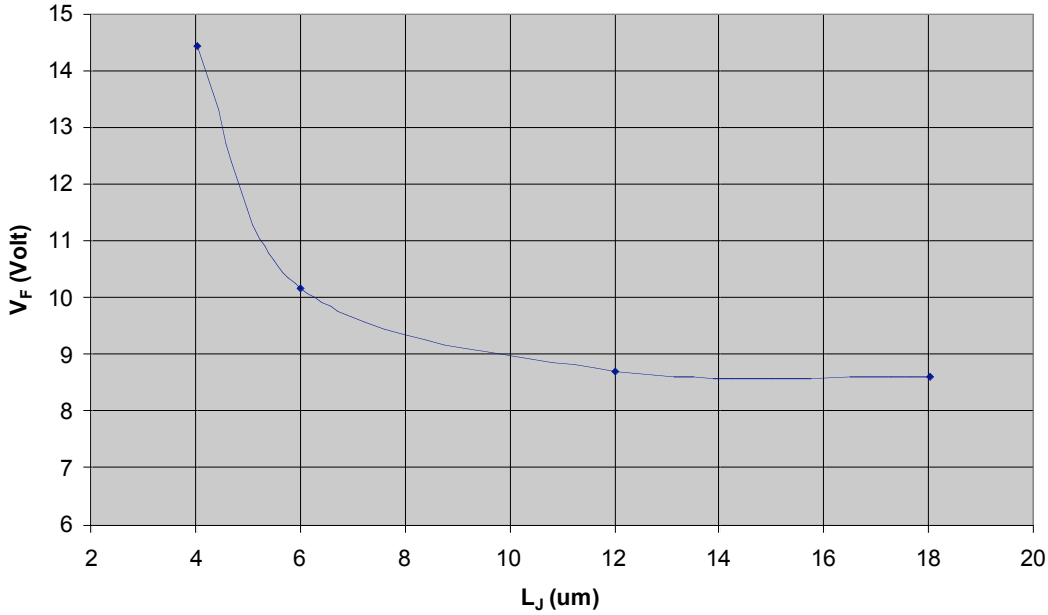


Figure 3.63 Forward voltage drop of the IGBT for L_J =4, 6, 12, 18 µm (MEDICI simulation).

3.2.2.2 Edge Terminations

The blocking voltage of a power transistor cannot reach the theoretical values due to field crowding at the edge of the device. In order to achieve a blocking voltage close to the theoretical value, optimized edge terminations are required to minimize the field crowding. Junction termination extension (JTE) [14] has emerged as a promising approach. In this thesis, numerical simulations were conducted for triple-zone JTE as edge terminations for n-type 4H-SiC epilayers designed to block 10 kV.

Figure 3.64 shows a schematic cross section of the triple-zone JTE edge termination. The n-type epilayer is 100 µm thick, doped $8x10^{14}$ cm^{-3}, and each JTE ring is 100 µm wide. The independent parameters for this investigation are the doses of each ring, designated $N_A(i)$ [cm^{-2}], and the depth Y_0 of the half-Gaussian implant profile shown in Fig. 3.65. For most simulations, the σ of the Gaussian tail is held at 0.5 µm. Blocking voltage (BV) is obtained from a solution of Poisson's equation on a two-dimensional grid using the MEDICI™ program. BV is defined as that voltage that results in an ionization integral of 0.9998 using the impact ionization coefficients of Konstaninov, et al. [15].

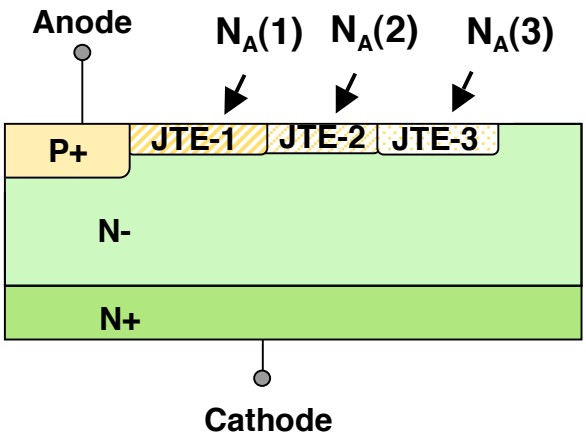


Figure 3.64 Schematic cross section of a PiN junction protected by triple-zone JTE.

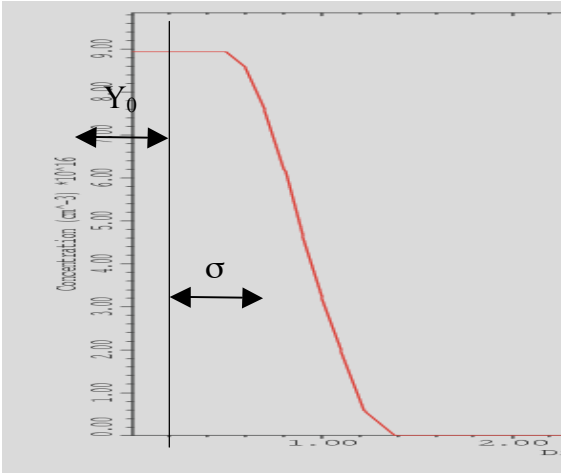


Figure 3.65 Half-Gaussian doping profile assumed for JTE regions.

Figure 3.66 shows BV as a function of outer ring dose $N_A(3)$ for four different doping ratios α, defined by $\alpha = N_A(i)/N_A(i+1)$. Unless otherwise specified, we employ a uniform α in all simulations. We note that the BV exhibits peaks as the dose is varied. Avalanche breakdown occurs either at the outer edge of one of the JTE rings or at the outer edge of the main junction. As dose is reduced, the breakdown point moves from the outer edge of the outer ring, to the outer edge of the middle ring, to the outer edge of the inner ring, and finally to the outer edge of the main junction. The peaks in BV correspond to doses where the breakdown is shared between two of these critical points.

The goal in selecting the dose ratio α is to achieve a BV > 10 kV over the widest possible range of doses. For this epilayer, the optimum α is 1.3.

Figure 3.67 shows BV using different α for the inner/middle and middle/outer rings. As seen, increasing α1 above 1.3 does not increase the range of doses where BV > 10 kV.

Figure 3.68 shows that the implant depth Y_0 has little effect for $Y_0 \leq 2$ μm, the largest value practical using modern implant technology.

As shown in Fig. 3.66, the doping levels of the JTE rings are critical for obtaining the target blocking voltage. If the doping concentration falls out of a certain range, blocking voltage drops quickly. This is a disadvantage for using JTE in a production environment. In addition, adding JTE brings extra processing complexity, because each ring of the JTE needs to be defined separately from all the other processing steps.

Compared to JTE, another kind of edge termination, called "floating field rings termination", has protecting capability less dependent on the doping and is easier to realize. As shown in Fig. 3.69, the idea of "floating field rings termination" is placing implanted rings surrounding the main junction ("floating" refers to the absence of electrical contacts to these rings). The rings have the same doping polarity as the main junction and can be fabricated simultaneously with the main junction. In the off-state, some of the electric field lines are terminated by the floating field rings, therefore, the electric field crowding at the corner of the main junction can be alleviated. By using floating field rings termination, Sei-Hyung Ryu, et al. achieved 89% of the theoretical blocking voltage in their fabrication of 10kV 4H-SiC Power DMOSFETs [16]. Fifty rings were used and the length of the termination structure is 400 μm. Due to its simplicity, we will use "floating field rings" as the edge termination for our IGBT device.

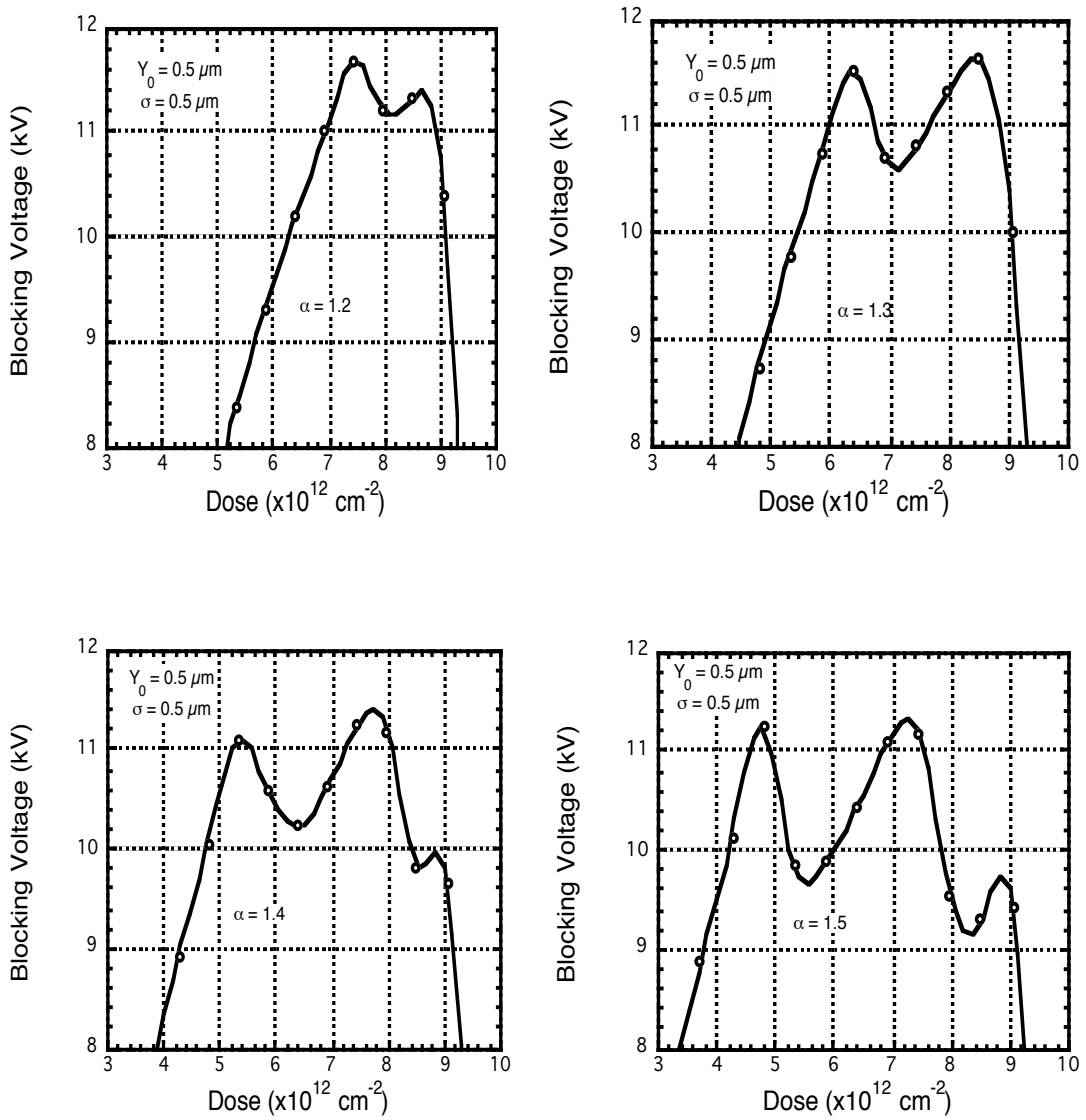


Figure 3.66 BV vs. dose for α = 1.2, 1.3, 1.4, and 1.5. For all plots, $Y_0 = \sigma = 0.5$ μm. The goal is to maximize the range of doses for which BV > 10 kV. This is obtained for α = 1.3.

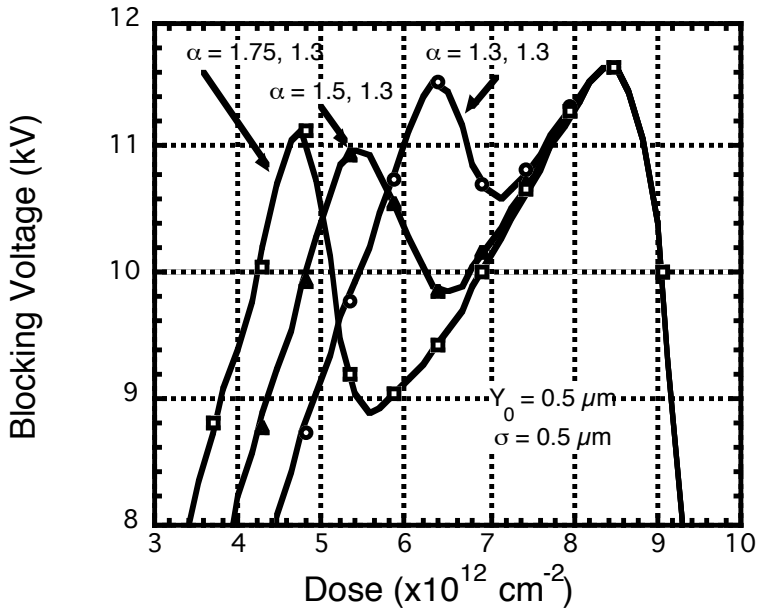


Figure 3.67 BV vs. dose with $\alpha 1 = N_A(1)/N_A(2)$ as a parameter. $\alpha 2 = N_A(2)/N_A(3) = 1.3$, and $Y_0 = \sigma = 0.5$.

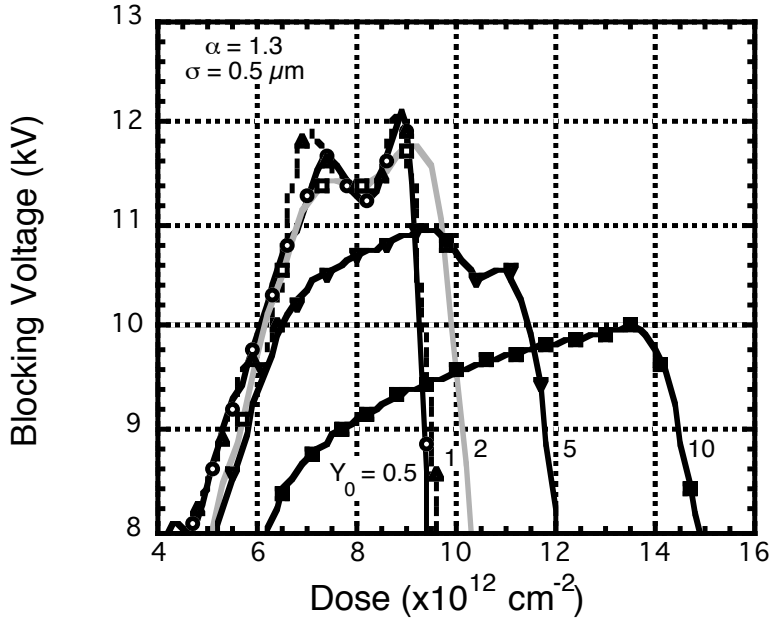


Figure 3.68 BV vs. dose with implant depth Y_0 as a parameter. $\alpha = 1.3$, and $Y_0 = \sigma = 0.5\ \mu m$.

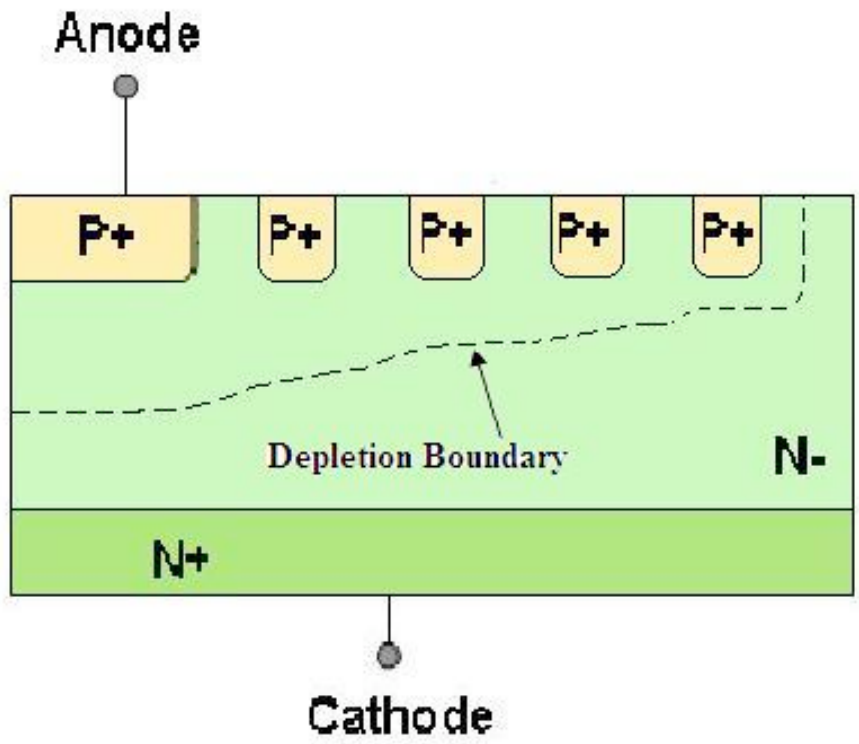


Figure 3.69 Schematic cross section of a PiN junction protected by floating field rings.

3.2.2.3 Design and Layout

3.2.2.3.1 Test Structures

Three kinds of IGBT structures were laid out on the mask. They are designated as device A, B and C. The schematic cross sections of these devices are illustrated in Fig. 3.70.

2μm misalignment is assumed when we determine the dimensions of the devices. In device A, the length of the base contact and source contact is 6 μm. In the worst case of misaligning, where the contact is reduced by 2 μm from both sides, we will still have 2 μm contacts. In device B, we reduce the length of the base contact and source contact to 4 μm, hoping that the worst misalignment wouldn't happen during the process. By reducing the area of the device, the channel density and the yield can be increased. In device C, the base contact and source contact are separated by 6 μm. Since electron current flows through the n+ source contact while the hole current through the p+ base contact, separate contacts allow us to measure the electron and hole currents and calculate the gain of the device.

Other test structures on the mask are shown in Fig. 3.71. The MOS-Capacitor in Fig. 3.71 (a) is used to measure the interface trap density at the n-/oxide interface, the maximum electric field in the oxide ($E_{ox,max}$) over n- drift region, the minority carrier lifetime and the doping concentration in the n- drift layer. The MOS-Capacitors in Fig. 3.71 (b) and (c) will be used to measure $E_{ox,max}$ over p-well and n+ source region respectively.

In each die, there are one IGBT and one diode with floating field rings. The width of the ring and the spacing between the rings are both 3 μm. There are 66 rings in total for each device.

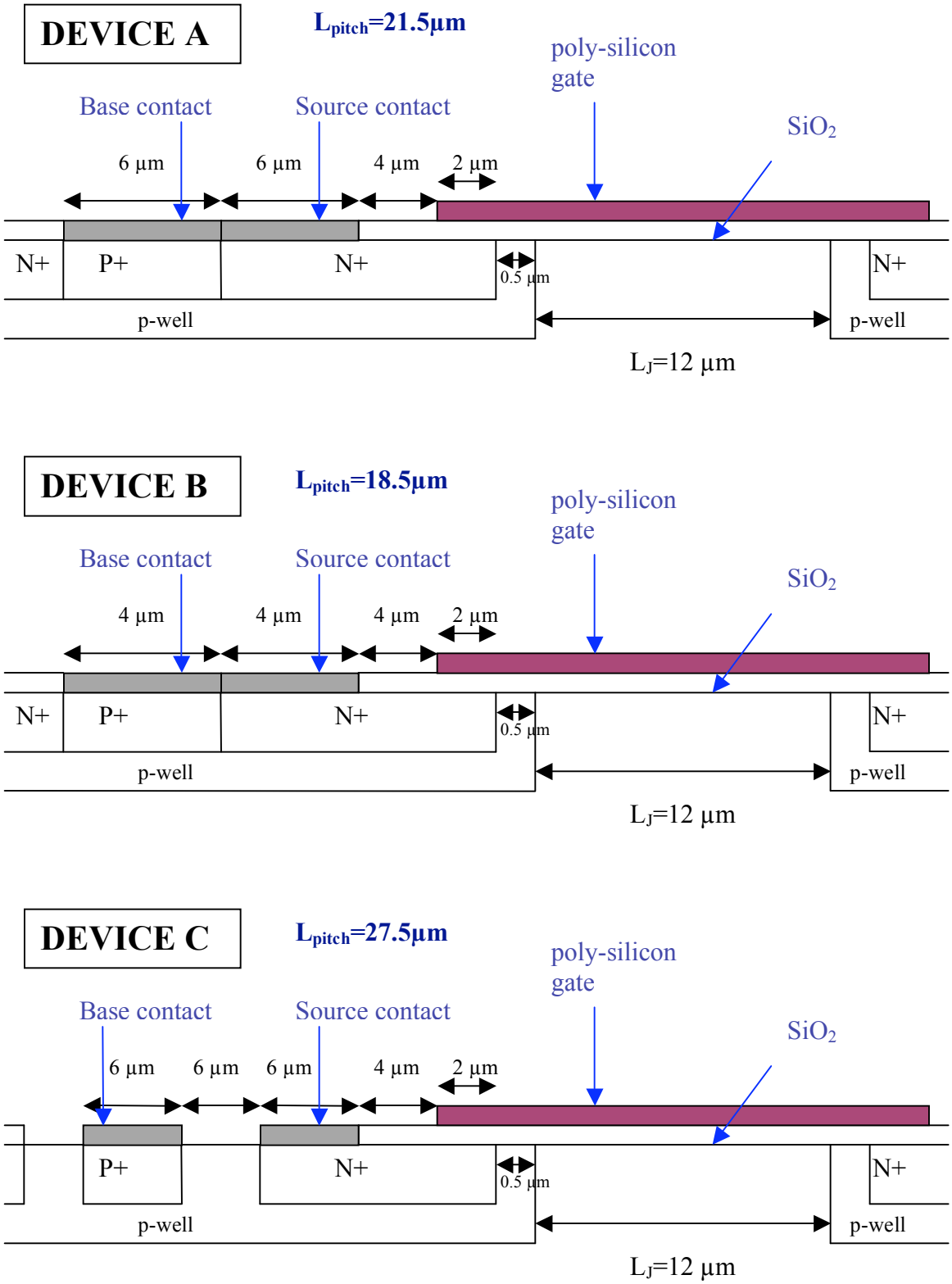


Figure 3.70 Schematic cross sections of IGBT structures on the mask.

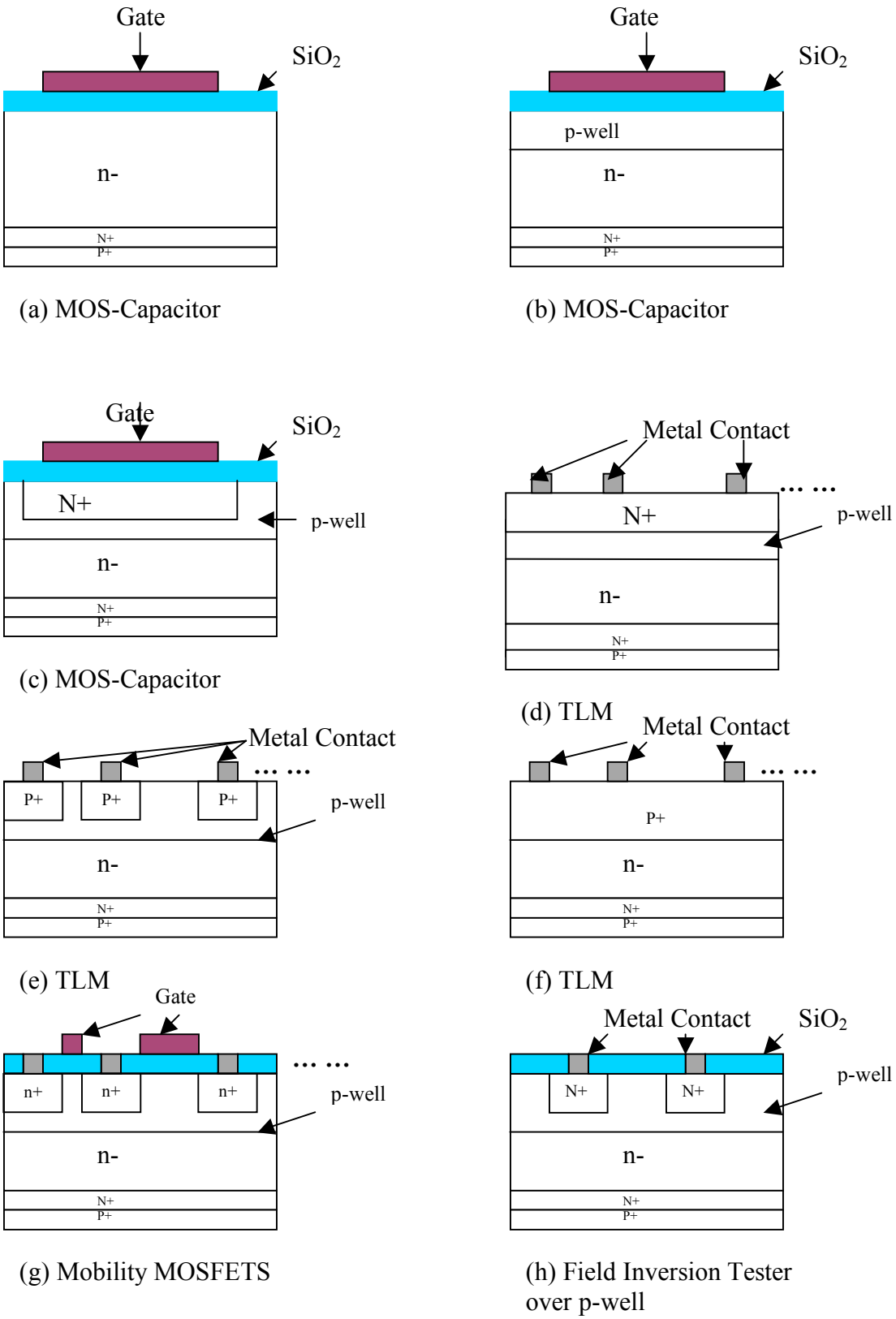


Figure 3.71 Other test structures on the mask.

Figure 3.71 (d), (e) and (f) are TLMs for evaluating the metal ohmic contacts. Figure (g) shows the n-channel mobility MOSFETs for measuring the inversion channel mobility of p-well.

3.2.2.3.2 Layout

The masks were designed using Mentor Graphics IC Station. The layout is shown in Fig. 3.72. The size of the die is about 8.5 mm x 8.5 mm. The size of the devices in quadrant II is about 1.5 mm x 1.5 mm. The size of the devices in quadrant I is about 1 mm x 1 mm. The smallest devices in quadrant III are about 0.5 mm x 0.5 mm. The IGBT in quadrant IV has 66 floating field rings. The ring width and spacing are 3 μm. The diode in quadrant IV has the same area and same FFRs as the IGBT. Since there is no concern about the oxide breakdown in a diode, this diode can be used to measure the avalanche breakdown voltage, while the IGBT with FFRs can be used to measure the blocking capability of a real device.

II **I**

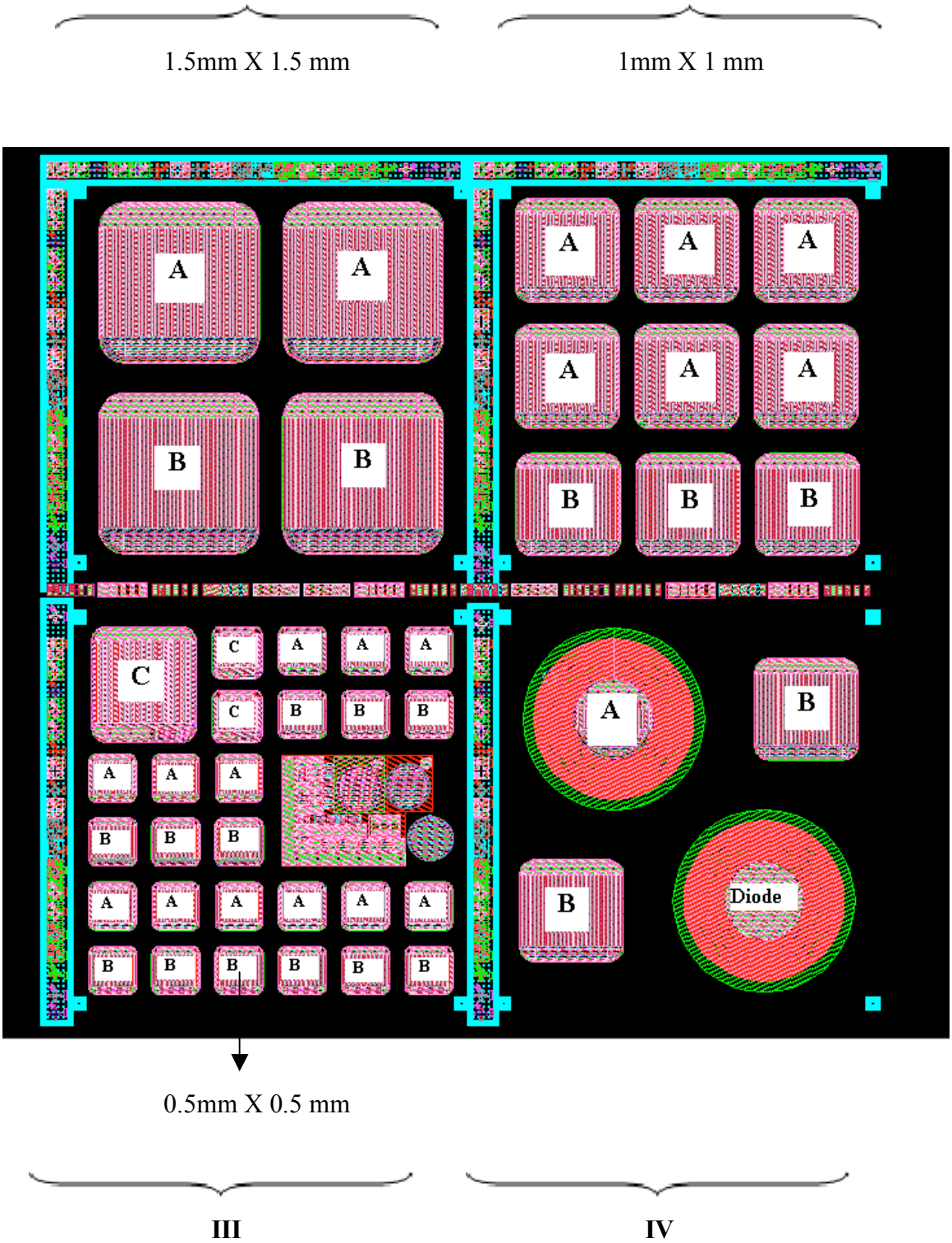


Figure 372 8.5 mm x 8.5 mm die layout.

3.2.3 Fabrication of High-Voltage N-Channel DMOS-IGBTs

Three wafers were processed for fabricating 20 kV n-channel DMOS IGBTs. The first wafer was grown at Purdue University and the other two were purchased at Cree, Inc. In this section, we will discuss the processing steps in detail.

3.2.3.1 Starting Wafers

3.2.3.1.1 The Wafer Grown at Purdue (Substrate CB0517-03)

The first wafer was grown in the Epigress VP508 SiC CVD reactor at Purdue University. A 182 µm n-type epilayer doped $2x10^{14}$ cm^{-3} was grown on the silicon face of a 50 mm n+ Cree substrate. The wafer was sent to NovaSiC for substrate removal, leaving a free-standing n-epilayer. Then the n+ buffer layer and p+ anode layer were grown on the silicon face by Cree. This process is illustrated in Fig. 3.73.

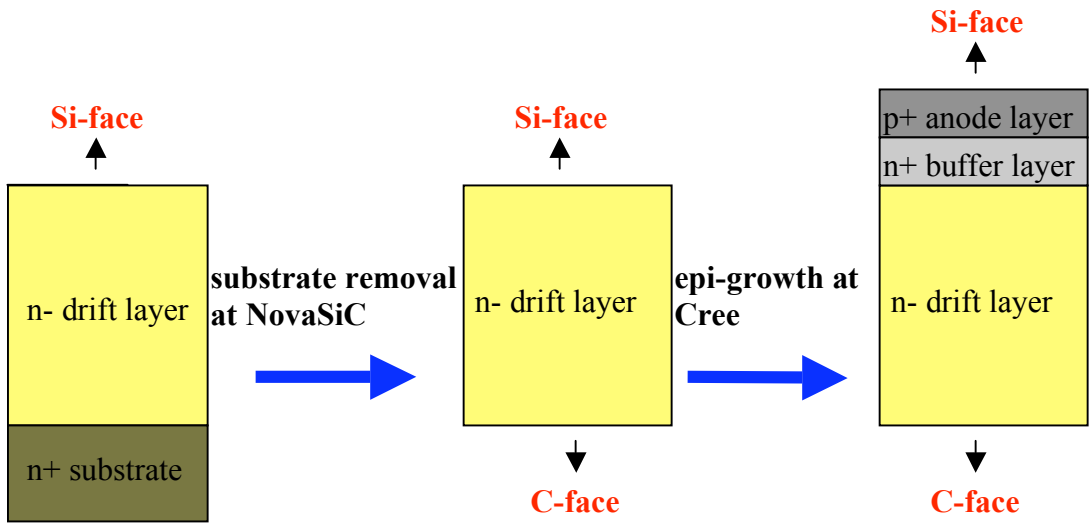


Figure 3.73 The first nIGBT wafer was grown at Purdue University. The substrate was removed at NovaSiC. Then the n+ buffer layer and p+ anode layer were grown on the Si-face at Cree

Substrate Removal

After removing the substrate, the thickness of the free-standing epilayer was measured by FTIR (Fourier Transform Infrared Spectroscopy, Bruker Vector 22 with the IR-1 Scope). As shown in Fig. 3.74, the thickness varied from 119.67 µm to 204.58 µm. Since the n- drift layer was only 182 µm thick, a portion of the wafer still had substrate left. RIE and a second polishing at NovaSiC were performed to remove the remaining substrate. The final thickness is below 176 µm everywhere on the wafer

.

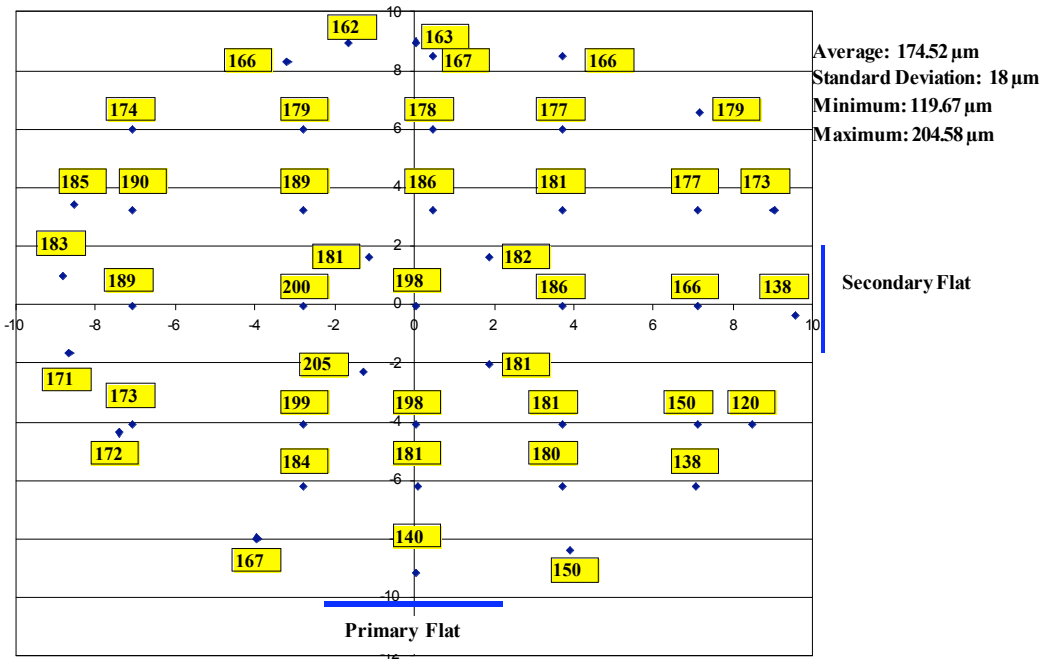


Figure 3.74 Thickness map of the Purdue grown wafer after the substrate removal.

Epigrowth of the N+ Buffer Layer and P+ Anode Layer

Since the n+ and p+ layers were not grown continuously with the n- layer, they could either be gown on the C-face or Si-face of the free-standing epilayer. Epigrowth on the C-face would give us the convenience of fabricating devices on the Si-face, of which we have many experiences. However, Cree could not guarantee a high doping in the p+ layer if it is grown on the C-face. Also, epilayers grown on the C-face have about 10 times higher deep-level trap densities than epilayers on the Si-face (2-5x10^{12} cm^{-3} as compared to 1-3x$10^{11}$$cm^{-3}$) [17]. This may result in a lower ambipolar lifetime.

Therefore, we decided to do the epigrowth on the Si-face and fabricate the devices on the C-face. This approach would also be consistent with continous epigrowth of the n- drift layer, n+ buffer layer, and p+ anode layer on the Si-face in future processing work.

The targeting thicknesses and doping concentrations of the n+ and p+ layers were 0.2 µm, $1x10^{18}cm^{-3}$ and 3 µm, $1x10^{19}cm^{-3}$ respectively. Because both layers were grown in the same run, the thickness and doping concentration of the n+ layer could not be measured after the growth. For the p+ layer, CV measurement showed the doping concentration to be about $8x10^{18}$ cm^{-3}. The total thickness of both epilayers on a companion 3-inch wafer was determined by its weight gain to be about 3.28 µm.

During the handling before the epigrowth at Cree, a portion of the lower-right quadrant was broken (see Fig. 3.75). The intact portion of the wafer was cut into four pieces for processing. Due to the breakage during cutting, polishing and processing, only about a quarter of this two inch wafer survived all the fabrication steps. It will be referred to as sample 1.

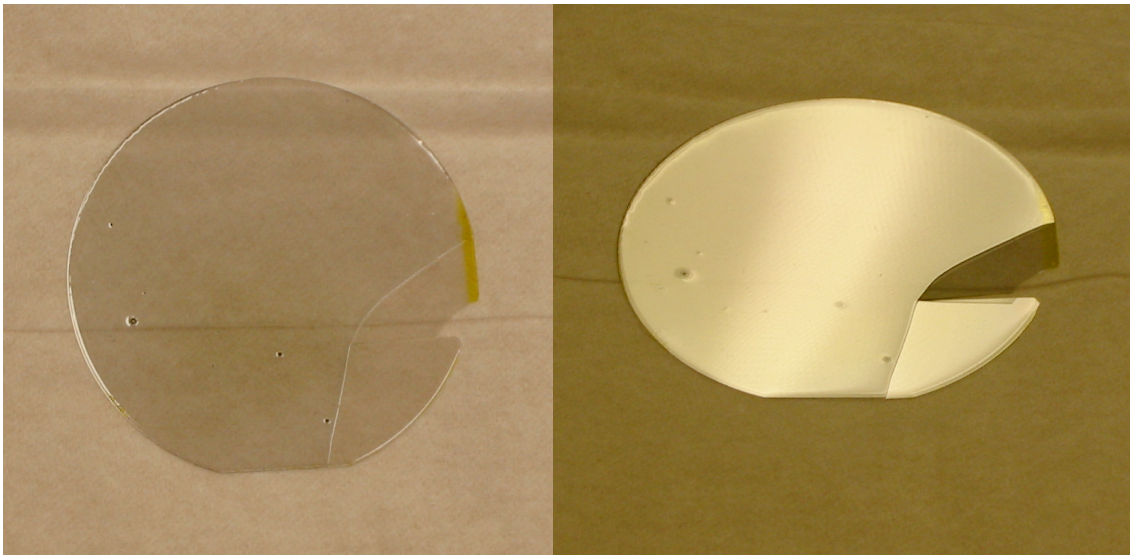


Figure 3.75 Purdue wafer after epigrowth at Cree. Two small pieces were broken off during the handling before epigrowth. The rest of the wafer remained intact.

Lifetime Measurements

Lifetime measurements were performed on the two small pieces by Semilab (Prielle Kornélia u. 2., 1117 Budapest, Hungary) using a microwave photoconductive decay (μ-PCD) technique. The ambipolar lifetimes were 1.11 μs and 1.27 μs on opposite sides of one piece, and 1.76 μs and 1.77 μs on opposite sides of the other piece (see FIg. 3.76). These pieces came from the periphery of the wafer and since lifetimes usually increase near the center of the wafer, it is likely that the remaining portion of the wafer has lifetimes no shorter than that measured.

Lifetime measurements were also performed using the time-resolved photoluminescence decay method. This is done by Dr. Paul B. Klein at Naval Research Laboratory. It showed that the carrier lifetimes were 1.07 μs for the C-face and 0.72 μs for the Si-face. The injection level was about $1x10^{14}$ cm^{-3}, which is considered as a low level injection. Therefore, the results should be interpreted as minority carrier (hole) lifetimes.

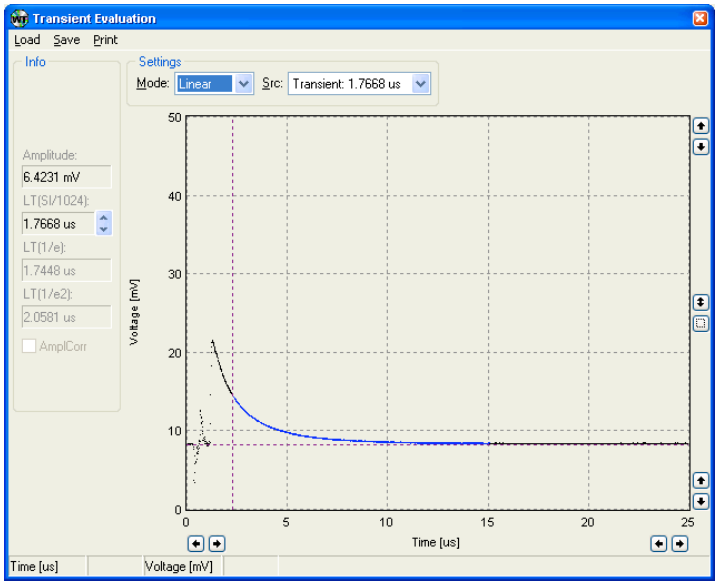


Figure 3.76 Microwave photoconductive decay measured by Semilab on the free-standing epilayer grown at Purdue University. Lifetime is 1.77 μs at room temperature.

3.2.3.1.2 Wafers Grown at Cree

Epigrowth

The cross-sectional view of the wafers ordered from Cree is shown in Fig. 3.77. The initial material is a 75 mm, 8º off-axis, n-type SiC substrate with low micropipe density. All the epilayers were grown on the Si-face. The LBPD template layer and the standard 1µm n+ buffer layer were for reducing the basal plane defects. They were removed in the subsequent polishing step. The doping concentrations and thicknesses of all the epilayers are listed in Table 3.10 and Table 3.11.

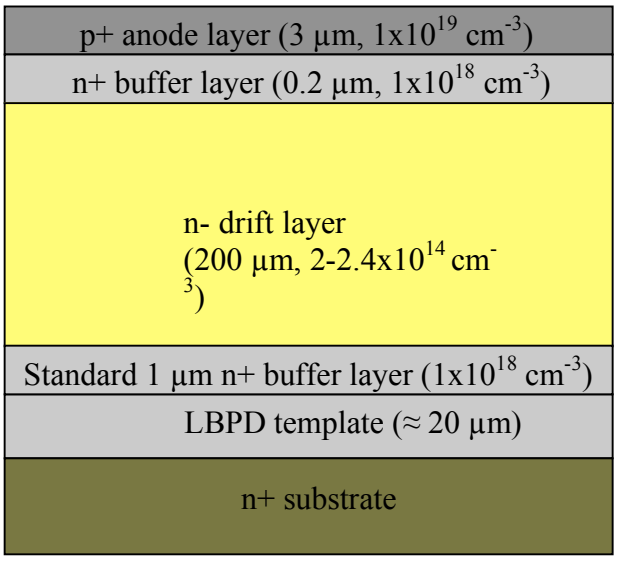


Figure 3.77 Cross-sectional view of the wafers ordered from Cree.

Table 3.10 Doping concentrations and thicknesses of the epilayers. Wafer HM0094-24

Epilayer	Thickness (µm)	Doping (cm^{-3})	
LBPD Template	21.8	N/A	
Standard 1 µm n+ buffer layer	1	$1x10^{18}$	Epi Run 1
n- drift layer	200	$2.4x10^{14}$	
n+ buffer layer	0.2	$1x10^{18}$	Epi Run 2
p+ anode layer	3	$1x10^{19}$	

Table 3.11 Doping concentrations and thicknesses of the epilayers. Wafer BZ0688-03

Epilayer	Thickness (μm)	Doping (cm^{-3})	
LBPD Template	19.6	N/A	
Standard 1 μm n+ buffer layer	1	$1x10^{18}$	Epi Run 1
n- drift layer	200	$2x10^{14}$	
n+ buffer layer	0.2	$1x10^{18}$	Epi Run 2
p+ anode layer	3	$1x10^{19}$	

As shown in Tables 3.10 and 3.11, the critical layers (the n- drift layer, the n+ buffer layer and the p+ anode layer) were not grown in the same run. This is due to the concern of hitting the doping target in a single continuous run. Therefore, even though the inverted growth process was employed, due to the limitations of the epigrowth techniques, the continuous epigrowth was not realized in this thesis.

Substrate Removal

After the epigrowth of the LBPD layer and again after the first epi run, the thicknesses of these epilayers were measured at Cree by FTIR (see Figs. 3.78 and 3.79). From these figures, we can estimate the thickness of the n- drift layer at each measured point. This gives us an idea of how thick the wafer should be after substrate removal. Take the circled numbers in Fig. 3.78(a) and Fig. 3.78(b) as an example.

$T_{LBPD\ template}$=22.837 μm

$T_{LBPD\ template}+T_{1\ \mu m\ n+\ buffer\ layer}+T_{n-\ drift\ layer}$=226.699 μm

where $T_{LBPD\ template}$, $T_{1\ \mu m\ n+\ buffer\ layer}$ and $T_{n-\ drift\ layer}$ are the thicknesses of the LBPD template, the 1 μm n+ buffer layer and the n- drift layer, respectively. Therefore, the thickness of the n- drift layer at that point should be 226.699 μm - 22.837 μm - 1 μm = 202.862 μm. Since the thicknesses of the second n+ buffer layer and the p+ layer are 0.2 μm and 3 μm respectively, after polishing, to ensure that there is no substrate left, the thickness of the wafer at that point should be no more than 202.862 μm + 3.2 μm = 206.062 μm. New maps were generated in this way (see Figs. 3.80 and 3.81). They show the upper limits of the wafer thicknesses at the measured points.

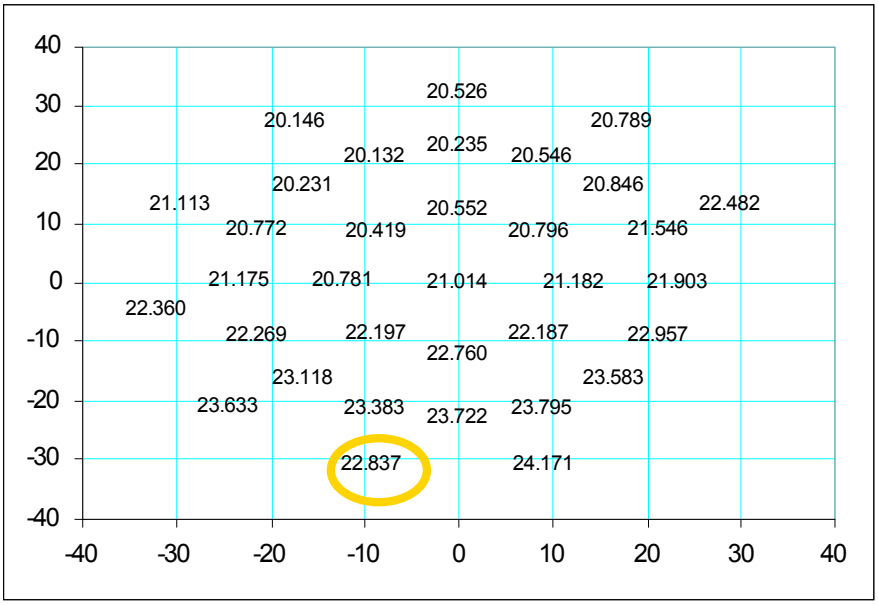


Figure 3.78 (a) Thickness map after the LBPD template (wafer HM0094-24).

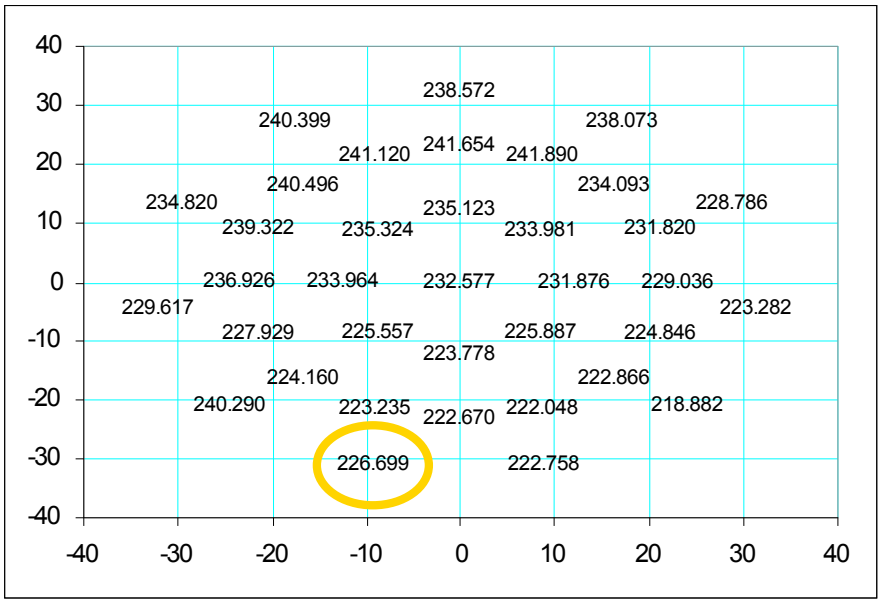


Figure 3.78 (b) Thickness map after the first epi run. The total thickness is the sum of the thicknesses of the LBPD template, the 1 µm n+ buffer layer and the n- drift layer (wafer HM0094-24).

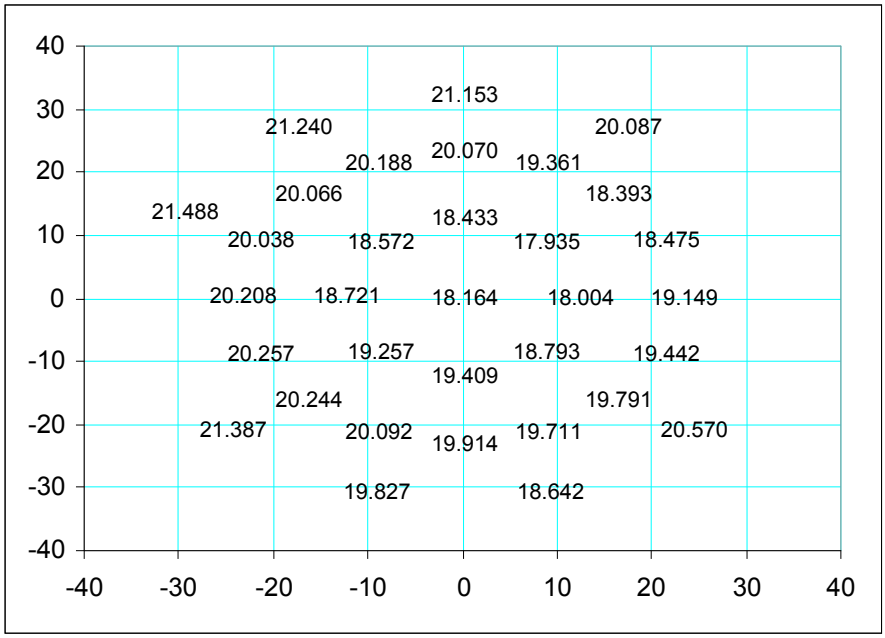


Figure 3.79 (a) Thickness map after the LBPD template (wafer BZ0688-03).

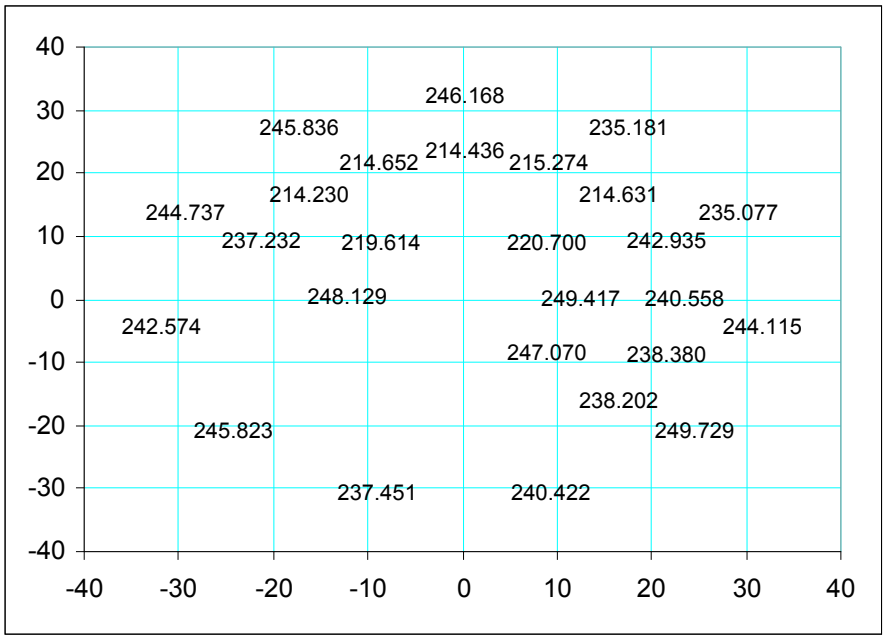


Figure 3.79 (b) Thickness map after the first epi run. The total thickness is the sum of the thicknesses of the LBPD template, the 1 µm n+ buffer layer and the n- drift layer (wafer BZ0688-03).

After polishing, both wafers were cut into four pieces at NovaSiC. Wafer HM0094-24 was broken during the polishing and cutting, as shown in Fig. 3.82. Yet wafer BZ0688-03 was completely intact (see Fig. 3.83).

Thickness measurements were conducted after these wafers came back from NovaSiC. Figures 3.84 to 3.87 are the thickness maps of the large pieces from wafer HM0094-24. After comparing them with Fig. 3.80, we found that RIE was still needed in order to make sure that all the substrate was removed. Table 3.12 lists the etching time and the material removed for the four large pieces from this wafer.

Table 3.12 RIE etching time and the thickness of the material removed. Wafer HM0094-24

Sample No.	Etching time (min)	SiC removed (μm)
1	693	35
2	99	5
3	99	5
4	198	10

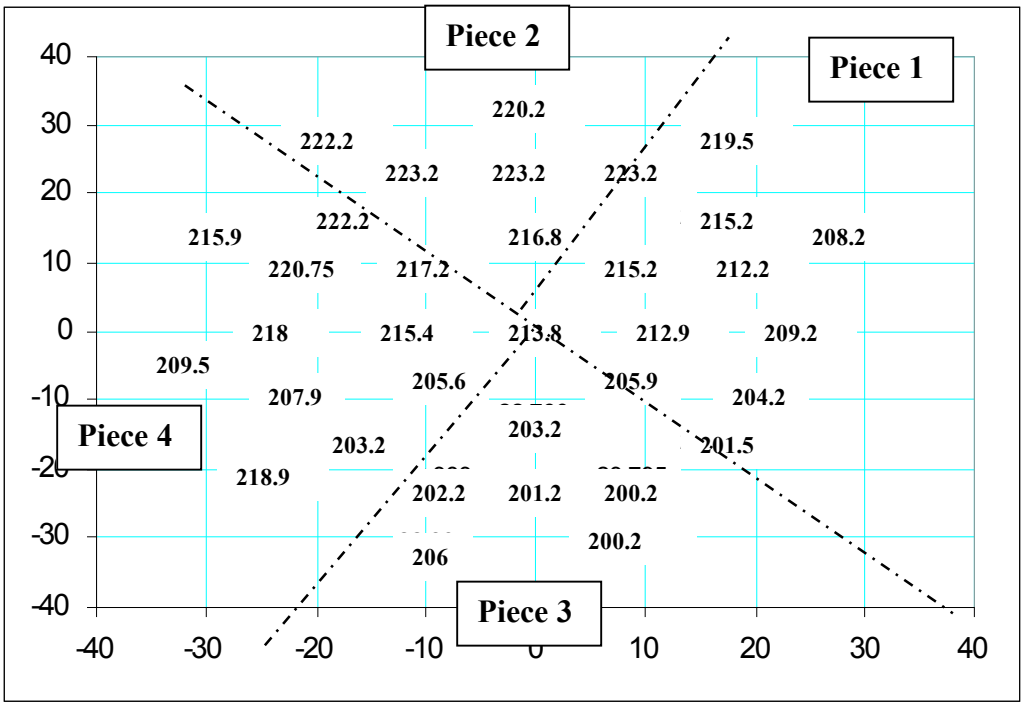


Figure 3.80 The upper limits of the wafer thicknesses after the substrate removal (at each point, the wafer thickness should not be greater than the number shown in this figure, in order to ensure that no substrate remained). The dashed lines roughly show where the wafer was cut (wafer HM0094-24).

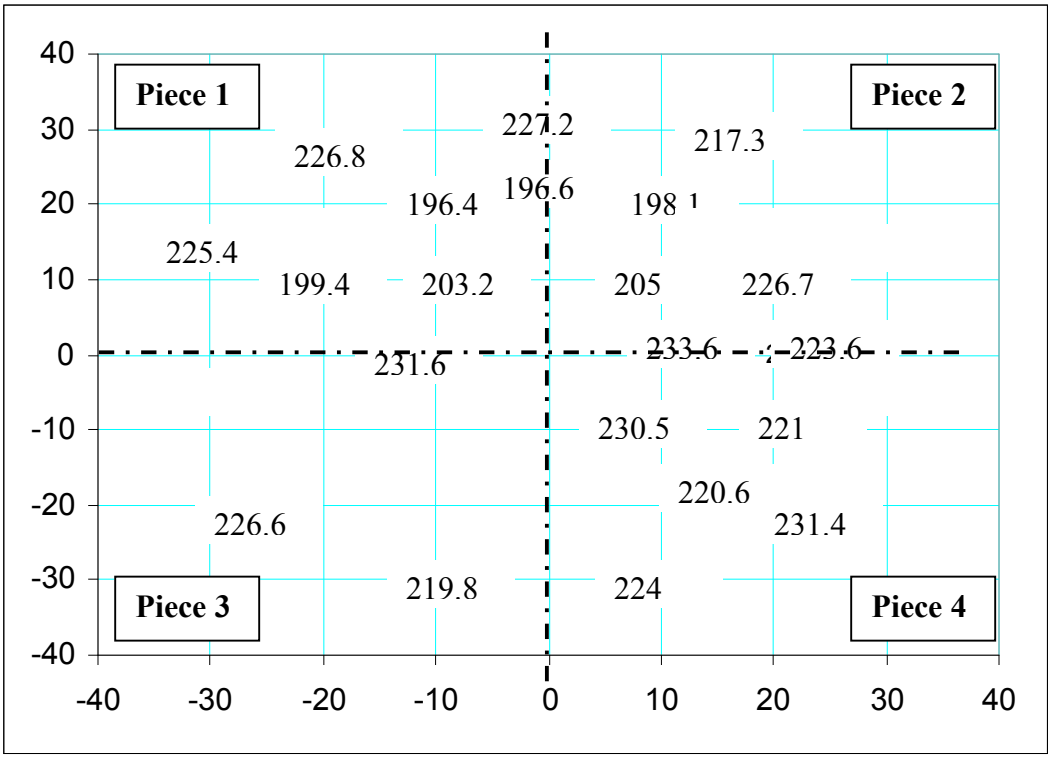


Figure 3.81 The upper limits of the wafer thicknesses after the substrate removal (at each point, the wafer thickness should not be greater than the number shown in this figure, in order to ensure that no substrate remained). The dashed lines show where the wafer was cut. (wafer BZ0688-03).

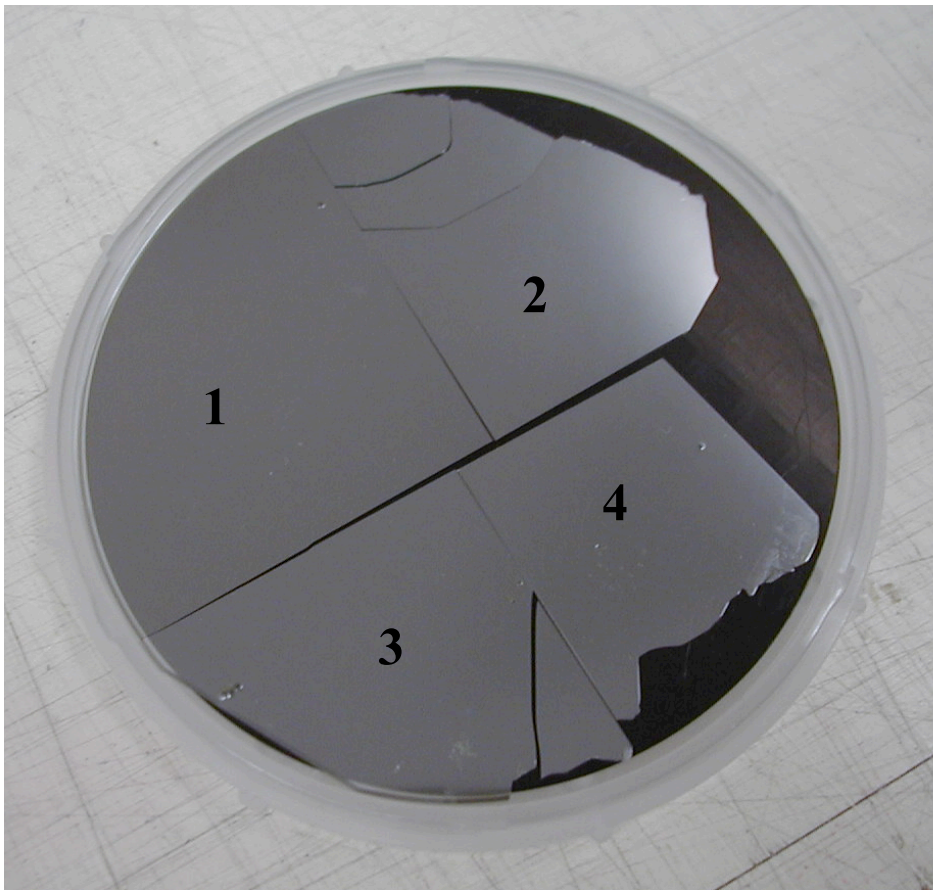


Figure 3.82 Wafer HM0094-24 after polishing and cutting at NovaSiC (C-face up).

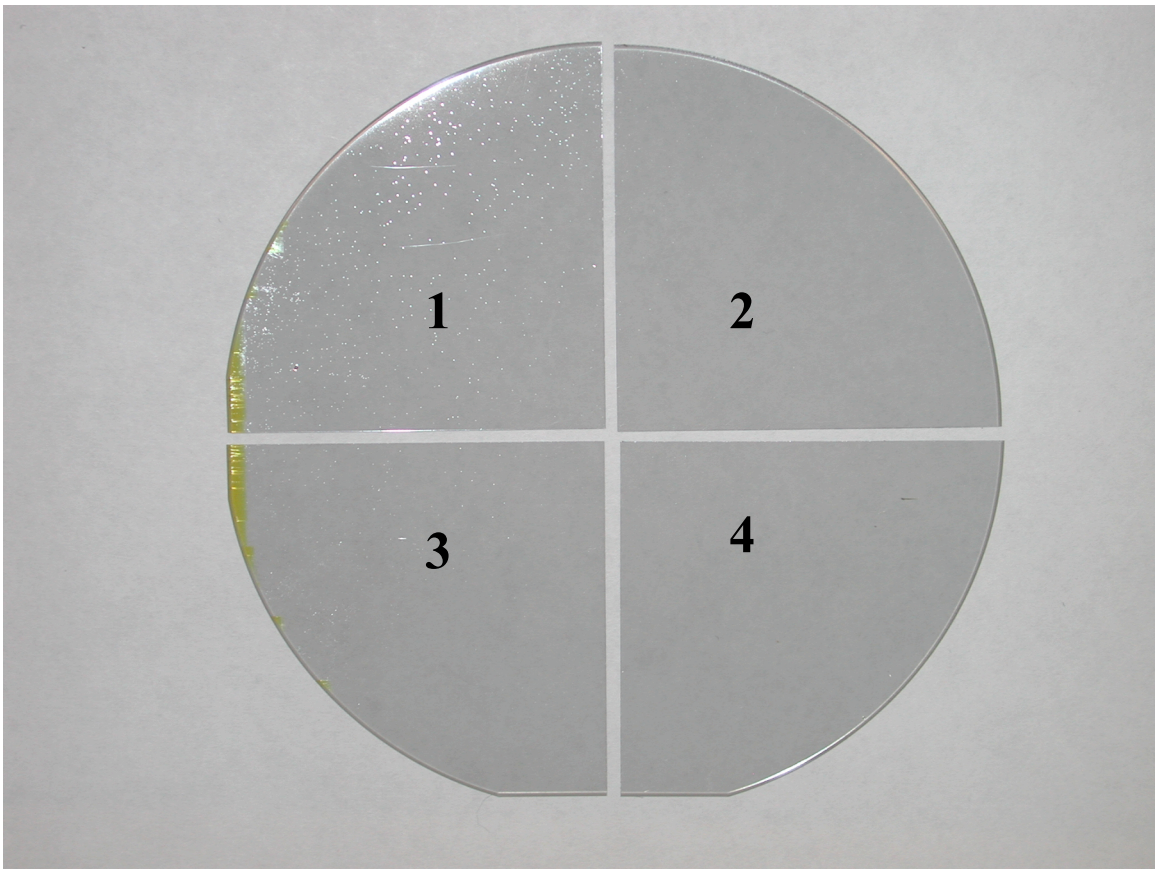


Figure 3.83 Wafer BZ0688-03 after polishing and cutting at NovaSiC (Si-face up).

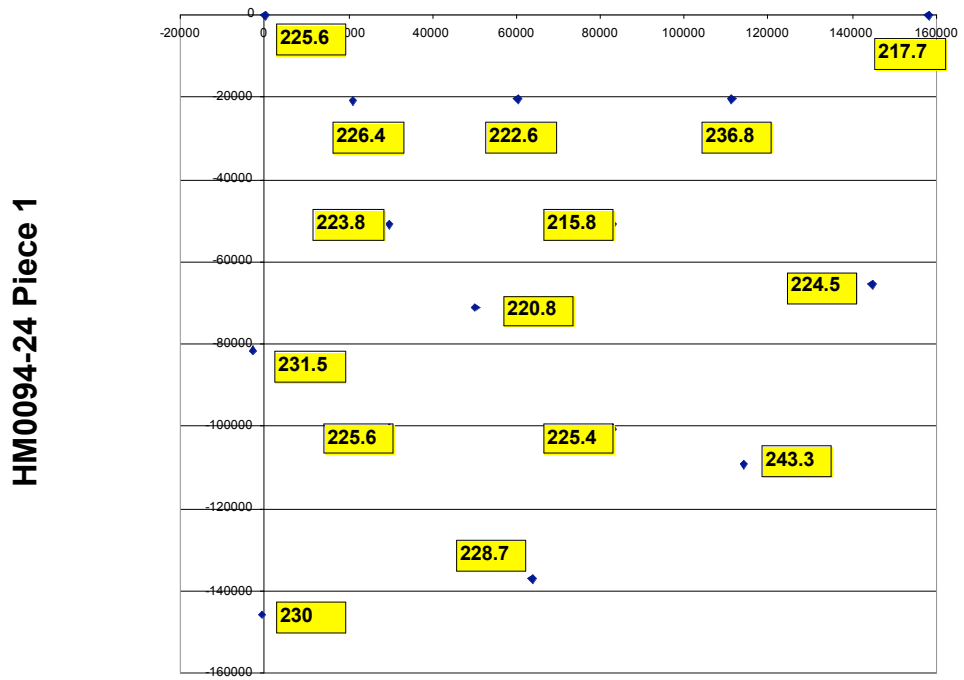


Figure 3.84 Thickness map of wafer HM0094-24 piece 1 after polishing.

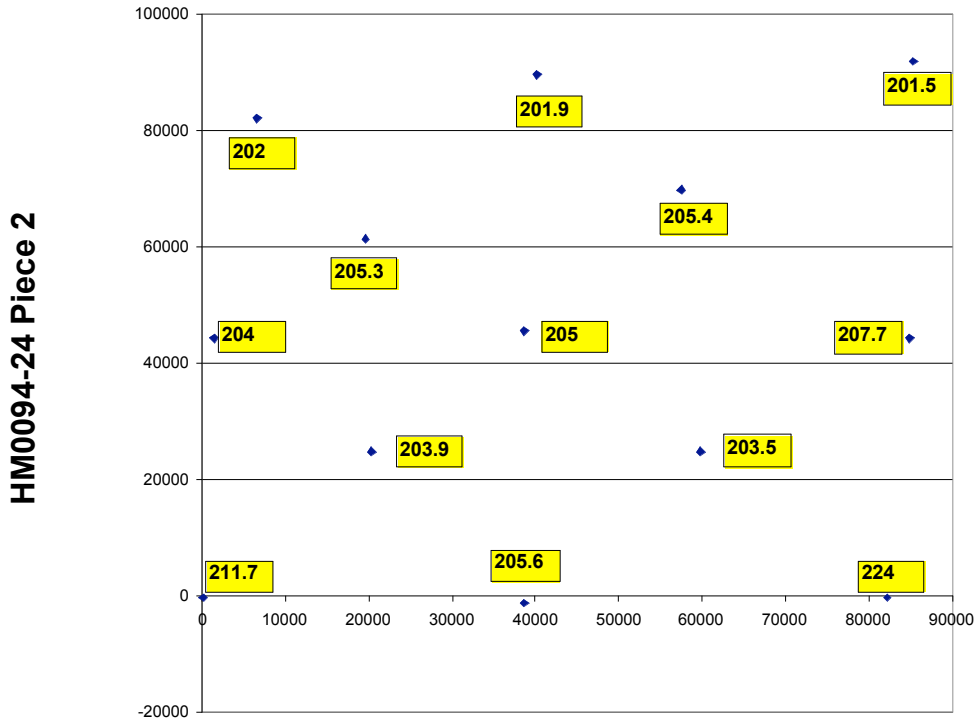


Figure 3.85 Thickness map of wafer HM0094-24 piece 2 after polishing.

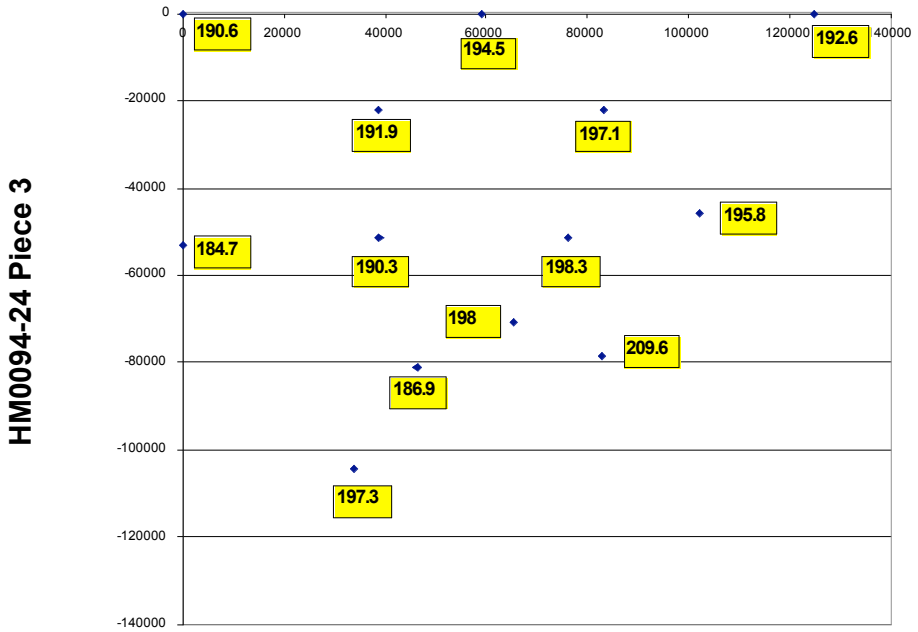


Figure 3.86 Thickness map of wafer HM0094-24 piece 3 after polishing.

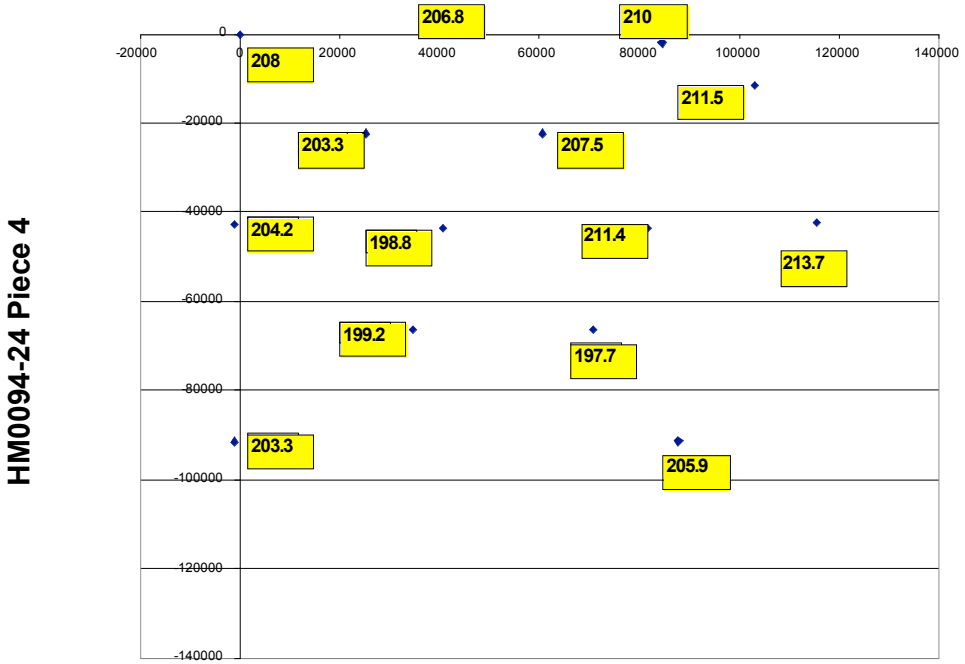


Figure 3.87 Thickness map of wafer HM0094-24 piece 4 after polishing.

Only the unbroken quarter piece of wafer HM0094-24 was processed for the IGBT fabrication. It was named sample 3.

The thickness of wafer BZ0688-03 was measured after the polishing (see Figs. 3.88 to 3.91 for the thickness maps). Since the wafer was thinner than the upper limits shown in Fig. 3.81, all the four pieces were ready for processing. They are named samples 2, 4, 5 and 6.

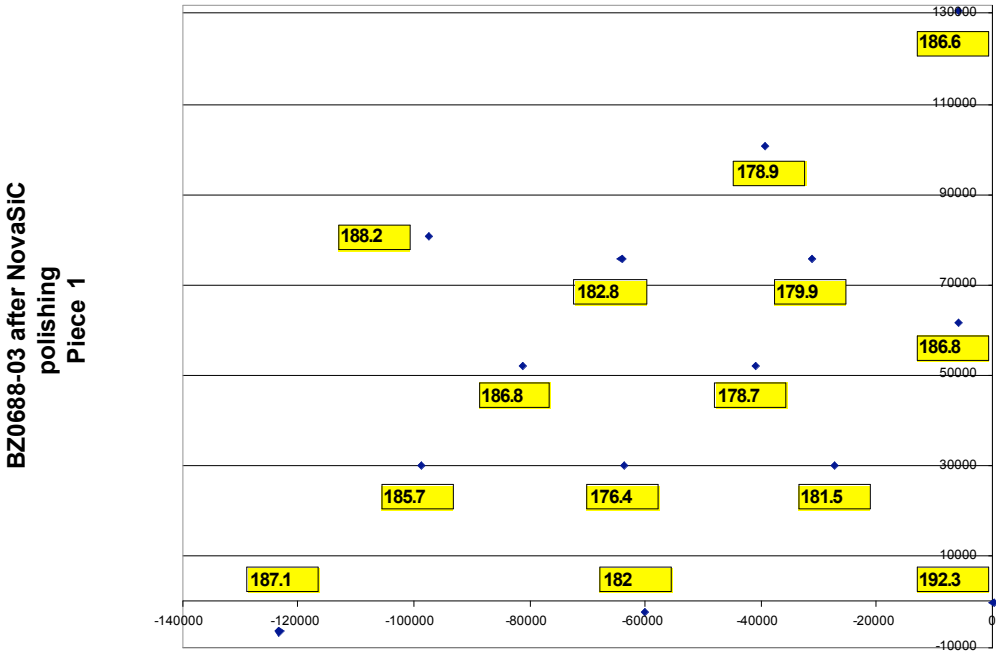


Figure 3.88 Thickness map of wafer BZ0688-03 piece 4 after polishing.

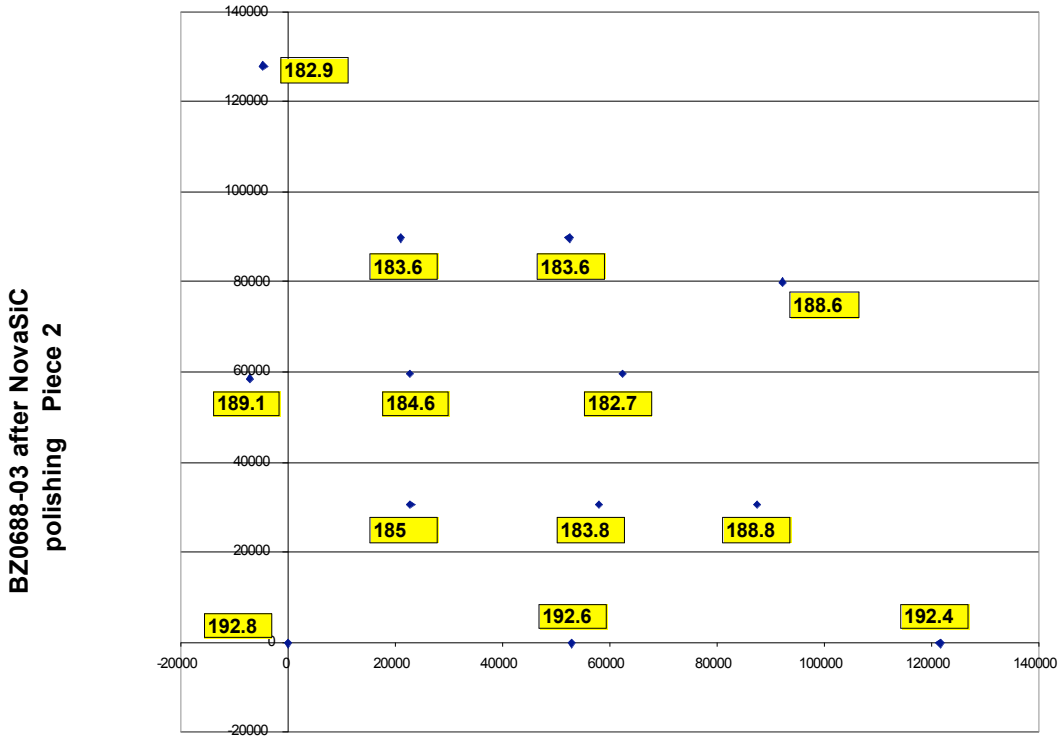


Figure 3.89 Thickness map of wafer BZ0688-03 piece 2 after polishing.

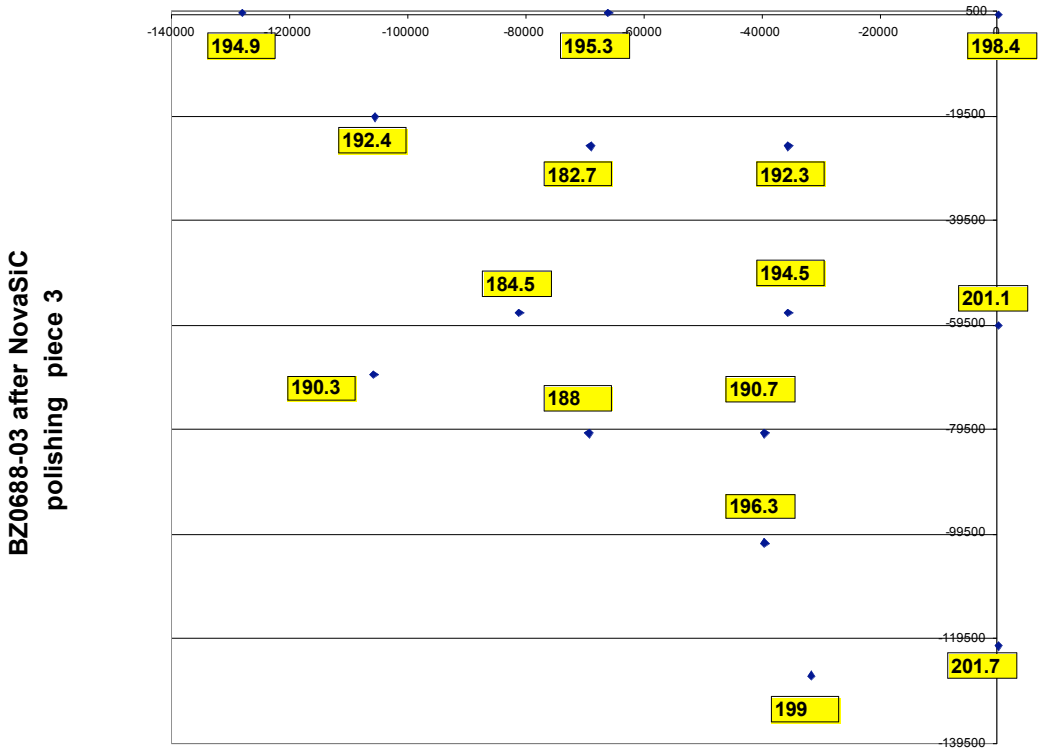


Figure 3.90 Thickness map of wafer BZ0688-03 piece 3 after polishing.

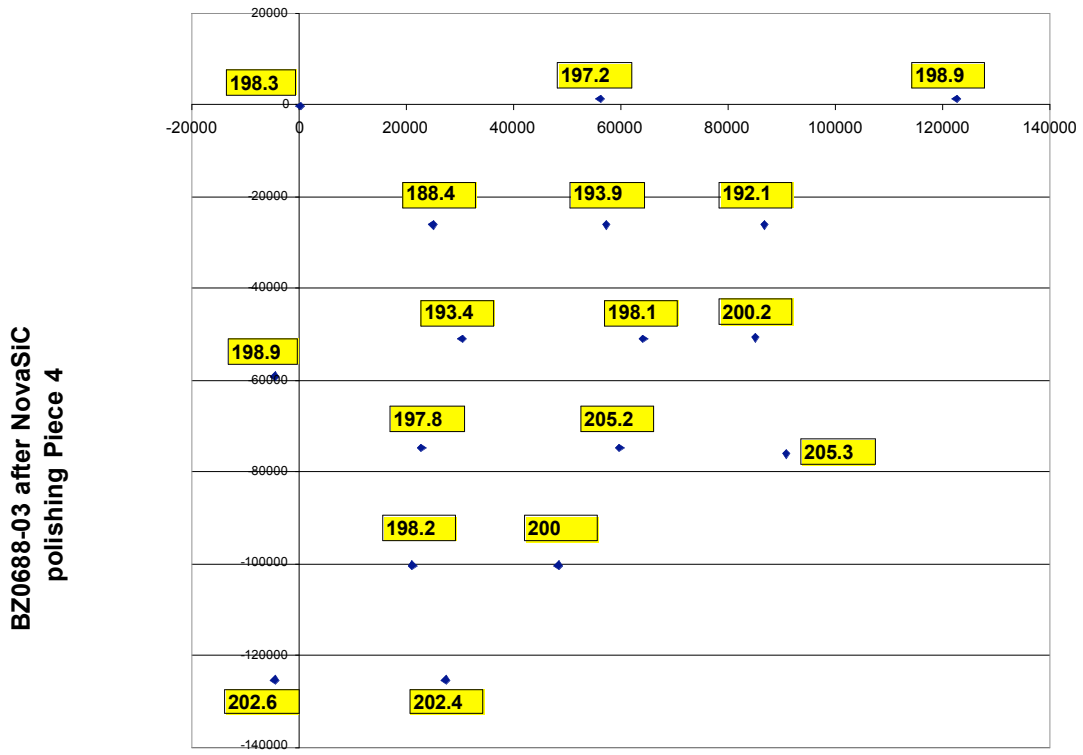


Figure 3.91 Thickness map of wafer BZ0688-03 piece 4 after polishing.

4.1.2.3 Lifetime Measurements

Two small pieces from wafer HM0094-24 were sent to Naval Research Laboratory for lifetime measurements. Both microwave photoconductive decay (μ-PCD) and time-resolved photoluminescence decay (TRPL) were used. Figure 3.92 shows the μ-PCD maps (by Dr. Joshua D. Caldwell at NRL) for both the carbon and silicon faces of the two sample pieces. The injection level was around 2.6×10^{16} cm^{-3}. The lifetime varies from around 1 μsec to around 20 μsec. To confirm these results, more measurements were made using time-resolved photoluminescence decay (by Dr. Paul Klein at NRL) (see figure 3.92(c)). The injection level was around 2×10^{14} cm^{-3}. Since the lifetime measured using TRPL is expected to be one-half the one measured using μ-PCD, the measurement results (using both techniques) are considered consistent.

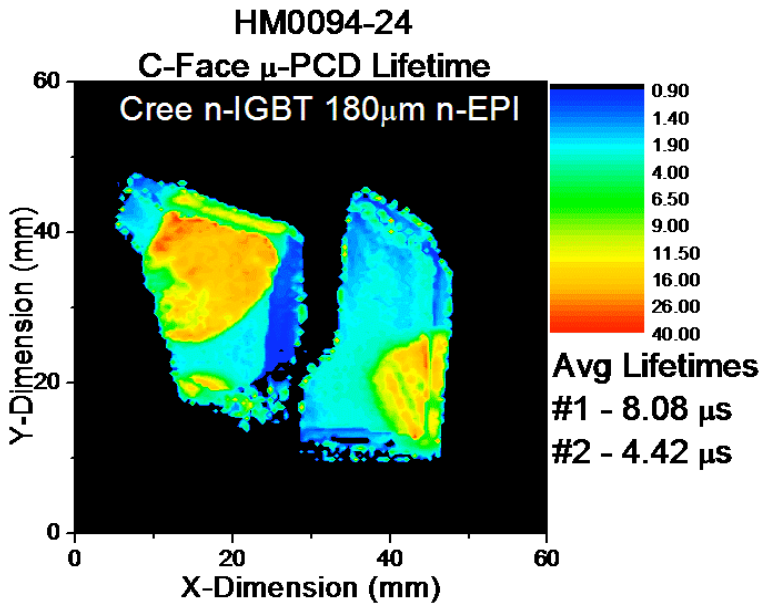


Figure 3.92 (a) Lifetime measurement on C-face at Naval Research Laboratory using microwave photoconductive decay technique (wafer HM0094-24).

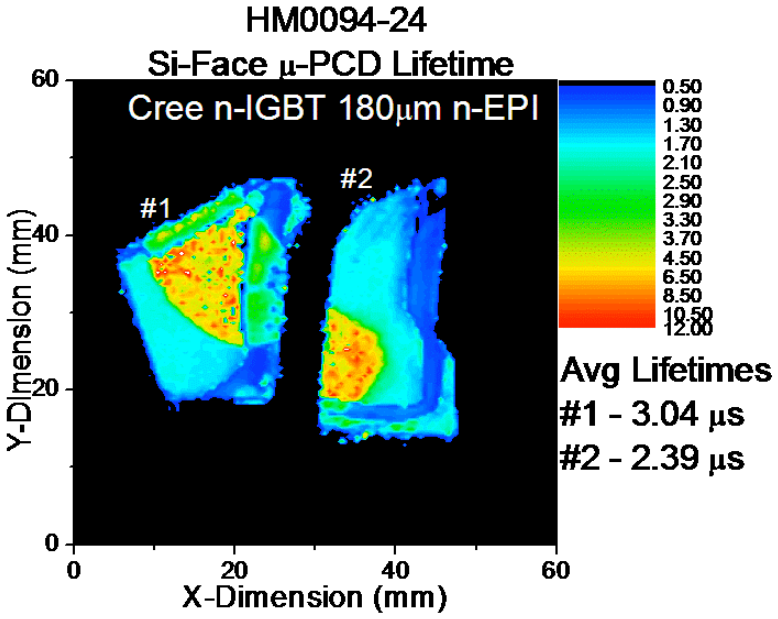


Figure 3.92 (b) Lifetime measurements on Si-face at Naval Research Laboratory using microwave photoconductive decay technique (wafer HM0094-24).

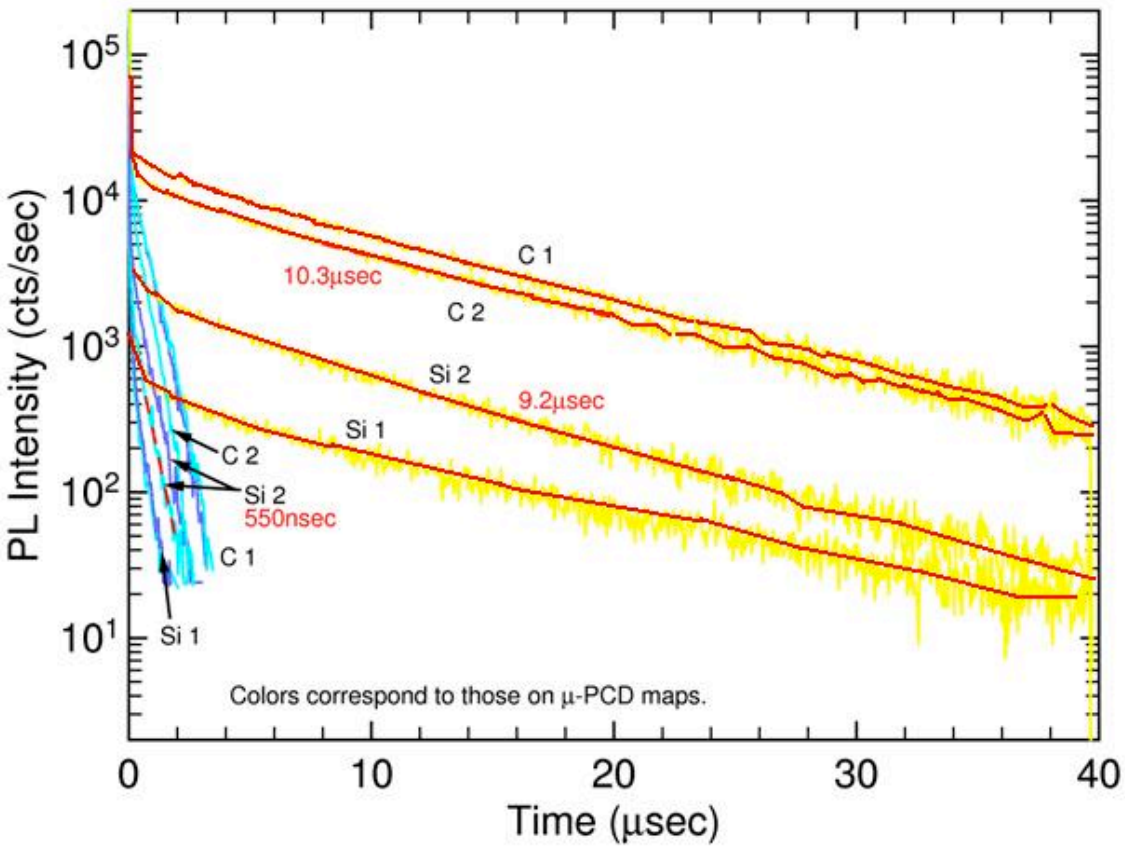


Figure 3.92 (c) Lifetime measurements at Naval Research Laboratory using time-resolved photoluminescence decay. The yellow curves were obtained in the region of high lifetime (shown in yellow and red in the µ-PCD maps) and the blue curves were collected in the areas with lower lifetime (shown as blue in the µ-PCD maps). The red lines are added to improve the visibility.

The BPD UV-PL images were taken by Dr. Bob Stahlbush and Dr. Kendrick Liu at NRL, using a photoluminescence image mapping system, which can identify dislocations and stacking faults within the epi and provide a map of their locations. The Silicon-Face image from piece 1 shows that the only difference between the regions with high and low lifetimes is an increase in the threading dislocation density. However, oddly, the region with the higher lifetime appears to have a significantly higher threading dislocation density than the regions with reduced lifetime (see Fig. 3.93).

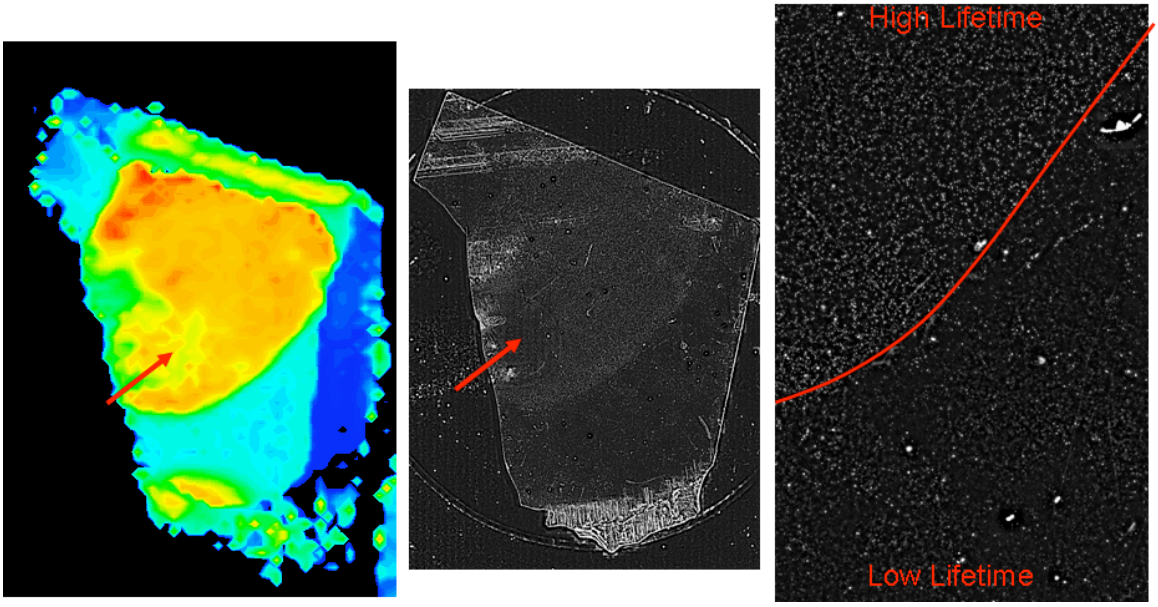


Figure 3.93 The only difference between the regions with high and low lifetimes is an increase in the threading dislocation density. However, the region with the higher lifetime actually has a higher threading dislocation density than the regions with reduced lifetime.

3.2.3.2 Pwell Implantation and Self-Aligned Process

In this section, we will first discuss the usual procedures of the pwell implantation and the self-aligned process for devices fabricated on the Si-face. Then we will discuss the changes needed when fabricating on the C-face.

After the initial cleaning, the wafer is first oxidized at 1150ºC (wet) for 90 minutes to grow a 30 nm thick oxide layer. Then around 1.5 µm thick polysilicon is deposited by LPCVD at 600 ºC. After the deposition, the polysilicon is oxidized at 900 ºC for around 20 minutes, resulting in a 20 nm thick oxide layer on the top (see Fig. 3.94a).

Positive photo resist is then applied on the wafer and patterned using the "pwell" mask. Ti/Ni (~10nm/200nm) is deposited by the ebeam evaporator and then liftoff is performed (see Fig. 3.94b). Ti/Ni will serve as the mask when RIE is performed to etch through the oxide and the polysilicon layers and open the windows for the pwell implantation(see Fig. 3.94c). Before the RIE, AZ4620 must be used to cover the large areas of the metal to prevent micromasking. AZ4620 will be stripped after the RIE. And finally, the sample is sent to Kroko and Associates (Tustin, CA) for ion implantation.

Figure 3.95 shows a photograph of the devices after the polysilicon patterning by RIE and the AZ4620 removal.

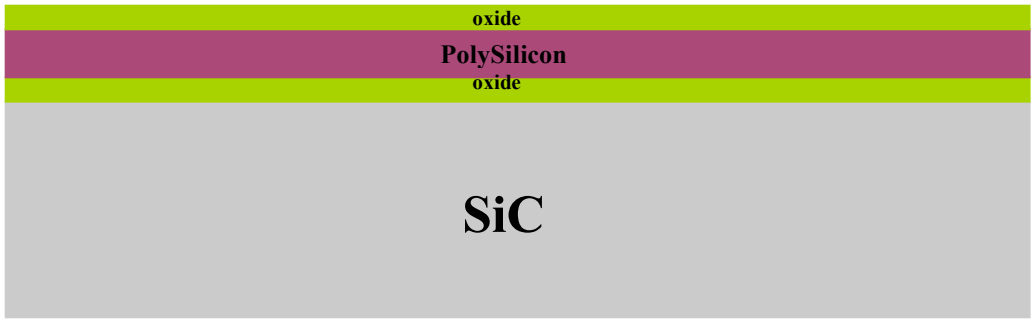


Figure 3.94 (a) A 30 nm thick layer of oxide is first grown on the SiC. Then a 1.5 µm polysilicon layer is deposited by LPCVD. And finally, the polysilicon is oxidized to grow a thin layer of oxide.

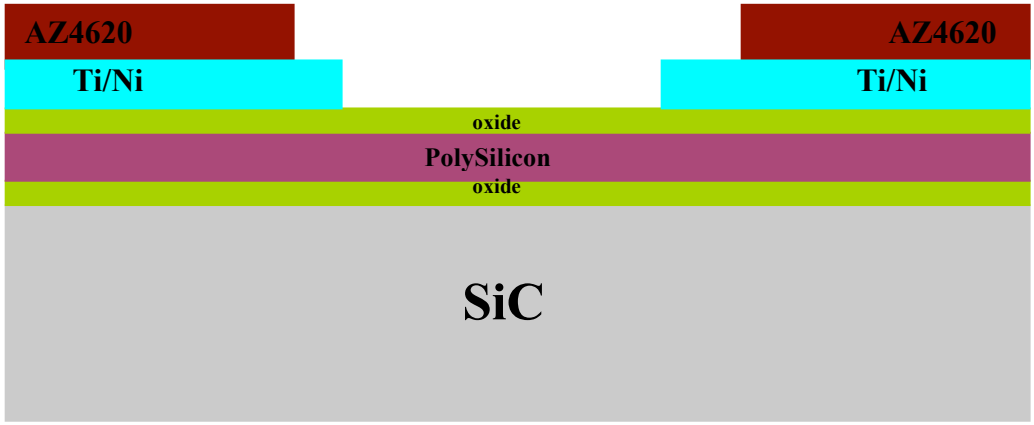


Figure 3.94 (b) Ti/Ni is deposited by e-beam evaporation. Then AZ4620 is applied to prevent micro-masking

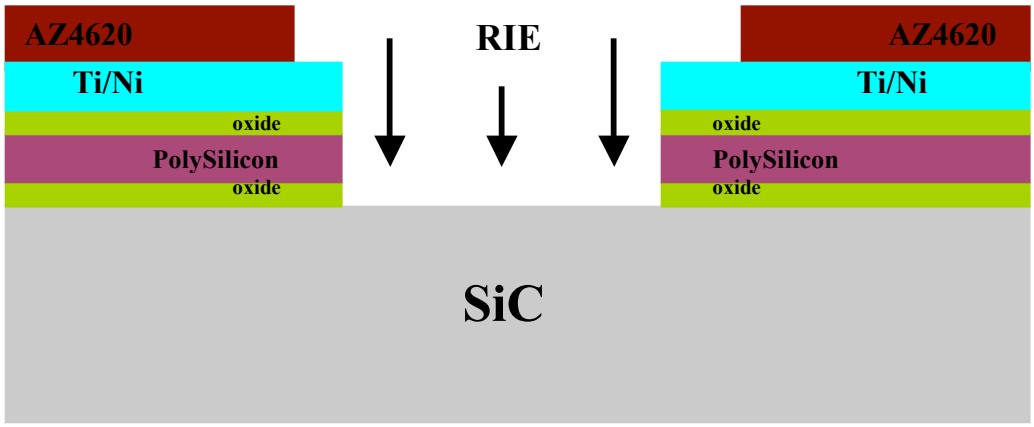


Figure 3.94 (c) RIE is performed to open the window for pwell implantation

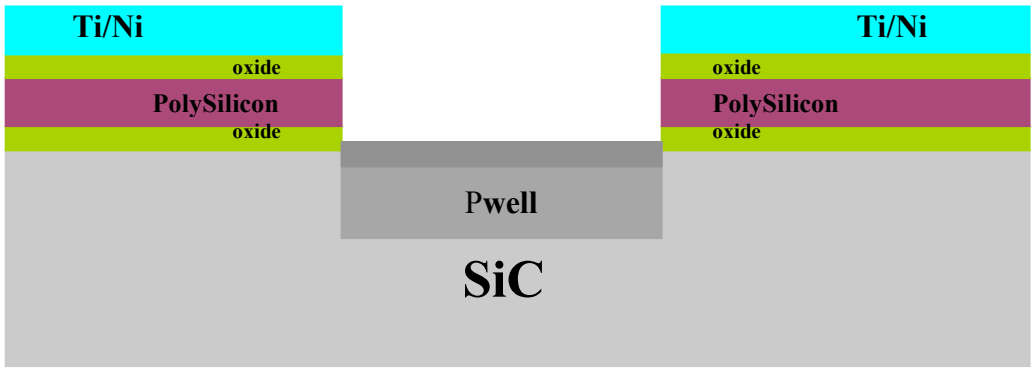


Figure 3.94 (d) Pwell implantation at Kroko and Associates.

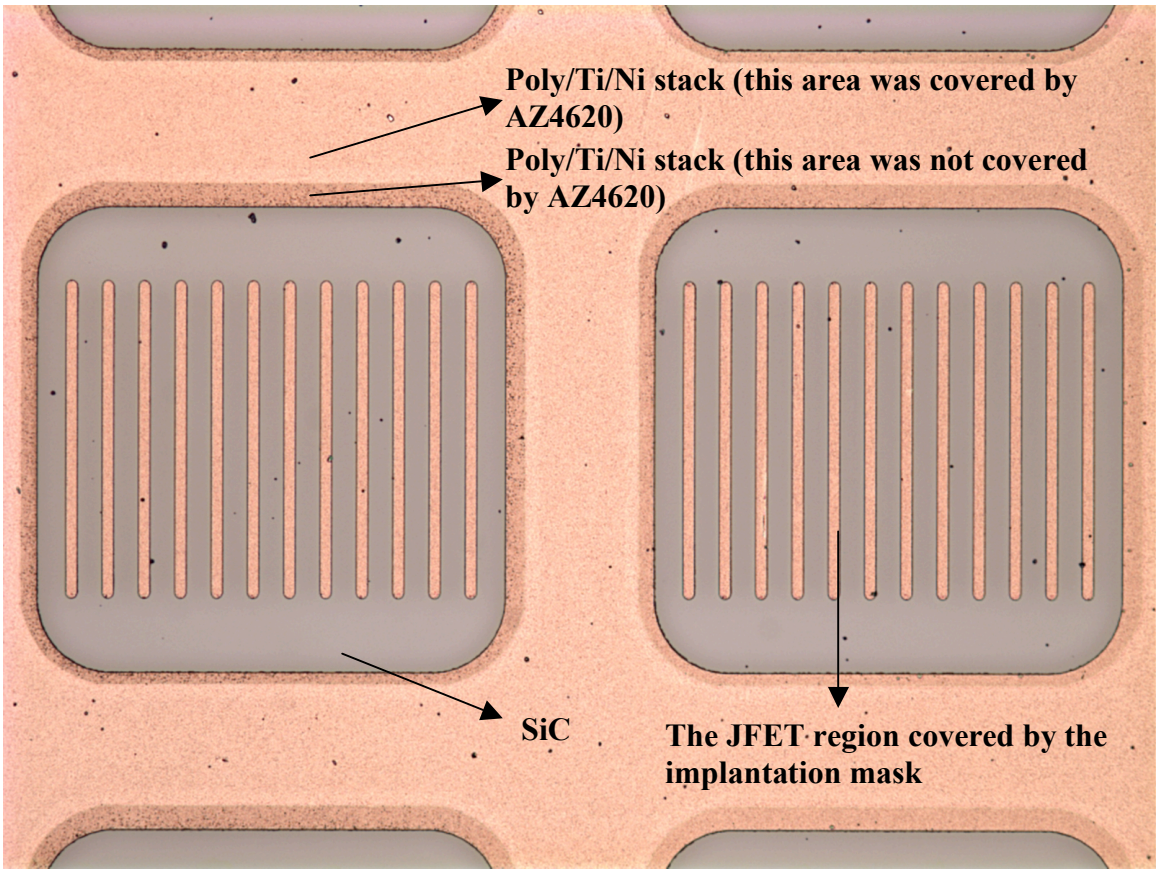


Figure 3.95 Devices after patterning the polysilicon by RIE and AZ4620 removal.

After the ion implantation, Ti/Ni is stripped by Piranha. Then the sample receives a 9-hour wet oxidation at 1000 ºC. The poly will be expanded horizontally by about 0.5 µm (see Fig. 3.96 for the cross-sectional view of the device after this step). Figure 3.97 is the dark field photograph taken after the oxidation of sample 1. The green area is the oxide surrounding the polysilicon fingers. As shown in this picture, the width of the oxide is around 1.1 µm. Since 1.1 µm thermal oxide consumes about 0.59 µm polysilicon, the horizontal expansion of the polysilicon fingers is about 0.51 µm.

The polysilicon expansion can also be measured by a Tenor α-step profilometer Figures 3.98(a) and 3.98(b) show the measurement results before and after the self-aligned process of samples 2 to 6, which were oxidized in the same run. The measurements were made on the same sample. As shown in the figures, the height of the polysilicon fingers increased by about 0.65 µm, which implies a lateral expansion of about 0.45 µm [18].

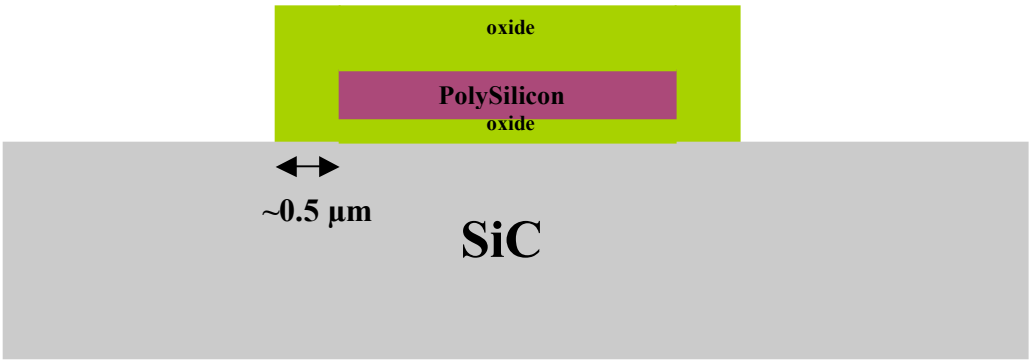


Figure 3.96 The cross-sectional view of the device after 9-hour wet oxidation at 1000 ºC. The polysilicon fingers are expanded by about 0.5 µm horizontally.

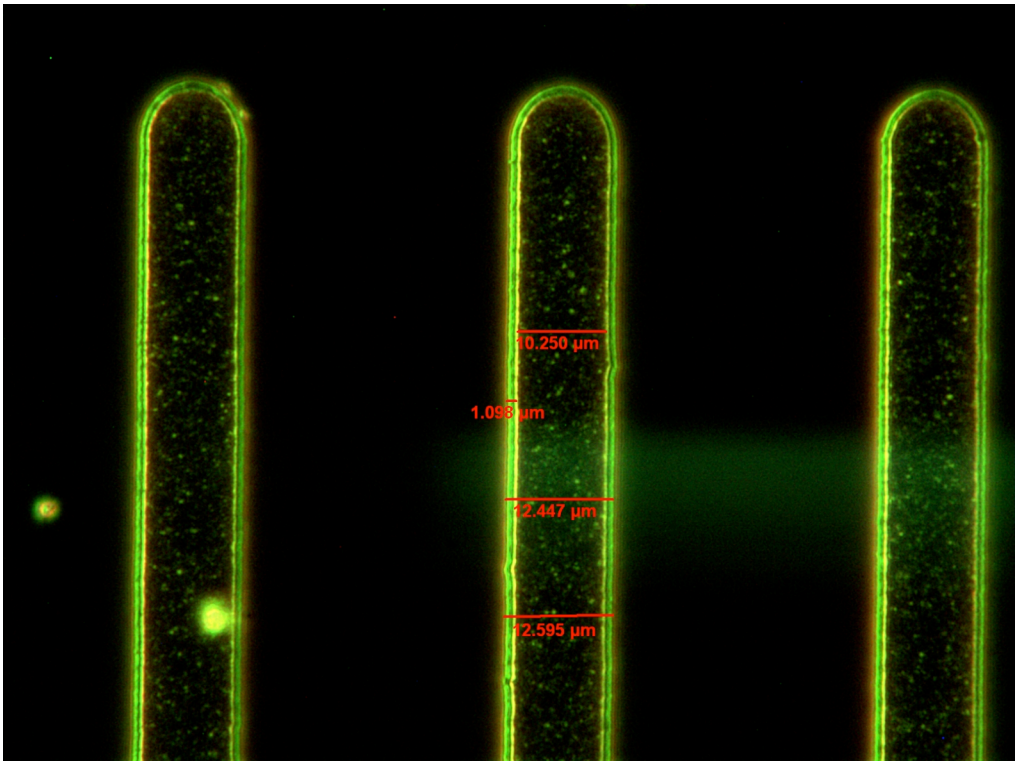


Figure 3.97 The dark field photograph taken after the oxidation of sample 1. The green area is the oxide surrounding the polysilicon fingers. Since the width of the oxide is around 1.1 µm, the horizontal expansion of the polysilicon is about 0.55 µm.

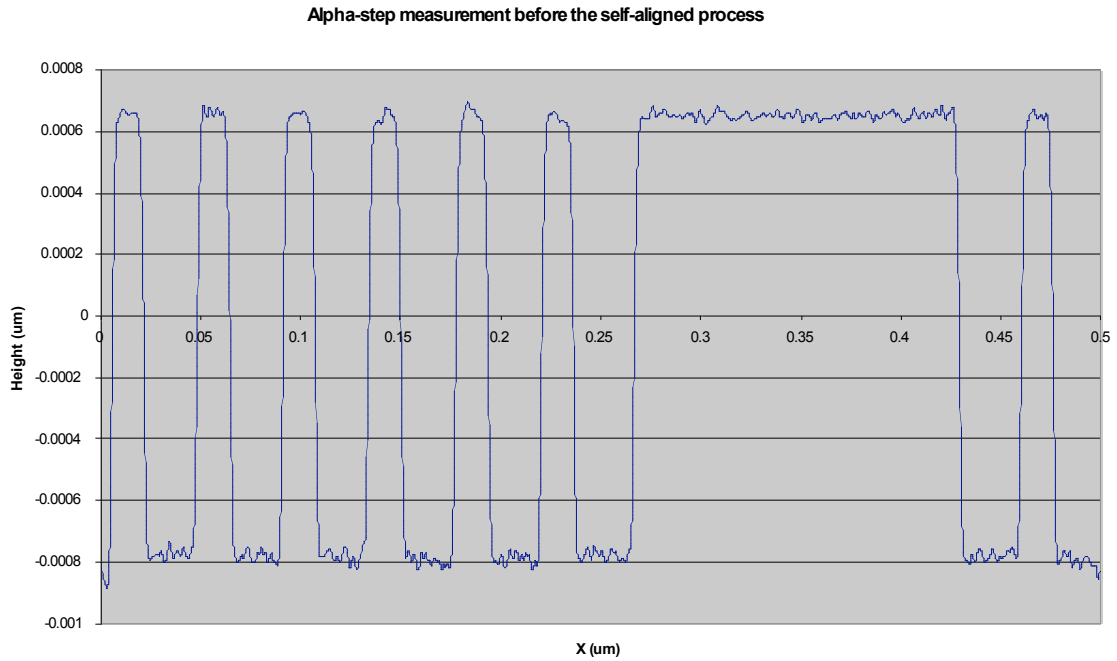


Figure 3.98 (a) α-step measurement before the oxidation. The height of the polysilicon fingers is about 1.45 µm.

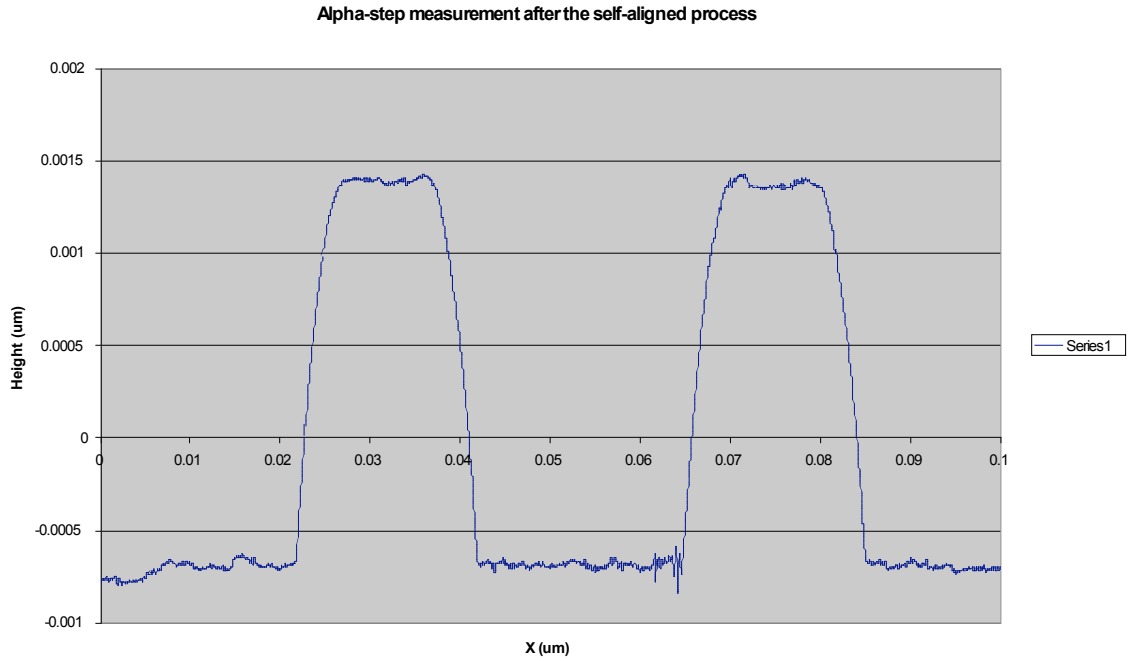


Figure 3.98 (b) α-step measurement after the oxidation. The height of the fingers is about 2.1 µm.

If the devices were fabricated on the Si-face, after the 9-hour wet oxidation at 1000 ºC, a 20 nm thick oxide layer would be grown on the SiC surface (where the sample receives the pwell implantation). Yet for C-face SiC, the oxide thickness would be around 300 nm (according to the test runs conducted at Purdue University). Since 300 nm oxide consumes about 150 nm SiC, this means about 150 nm of the 500 nm deep pwell implantation would be lost after the oxidation (as shown in FIg. 3.99). To avoid this problem, we replaced the first oxide layer by a layer of silicon nitride (~100 nm thick). Due to its low oxidation rate, silicon nitride is widely used in the LOCOS process in the industry, in which the silicon wafer is covered by a layer of patterned silicon nitride to prevent the unwanted oxidation. Test runs at Purdue University showed that a 9-hour wet oxidation at 1000ºC only consumed about 25 nm silicon nitride, therefore a layer of 100 nm silicon nitride would be thick enough to prevent the oxidation on the C-face SiC. silicon nitride was deposited by LPCVD at 825ºC. The flow rates of SiH_2Cl_2 and NH_3 were 64 sccm and 16 sccm, respectively. The deposition rate was around 3 to 5 nm/min.

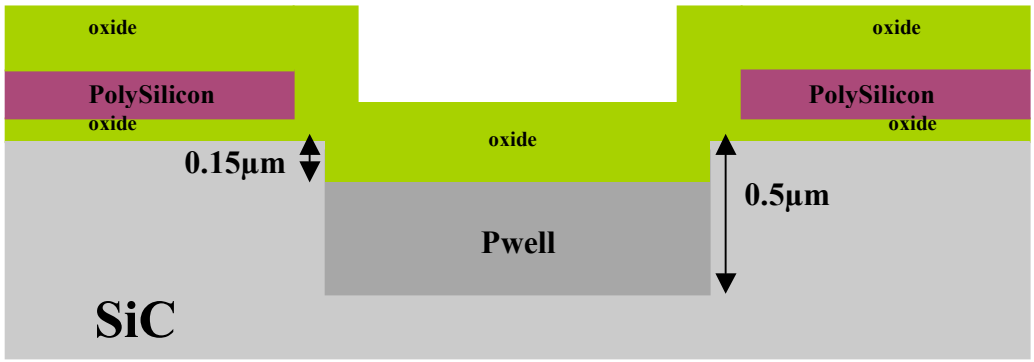


Figure 3.99 Without the silicon nitride protection, about 0.15 µm SiC would be consumed in the 9-hour wet oxidation at 1000ºC.

The pwell implant profile is shown in Fig. 3.100. Due to the 100 nm nitride on top of the SiC, the pwell implantation in the SiC actually starts at depth=100 nm. The n-type counter-doped implant was employed to reduce the threshold voltage. The species for all the p-type implants in this thesis was aluminum and n-type was nitrogen.

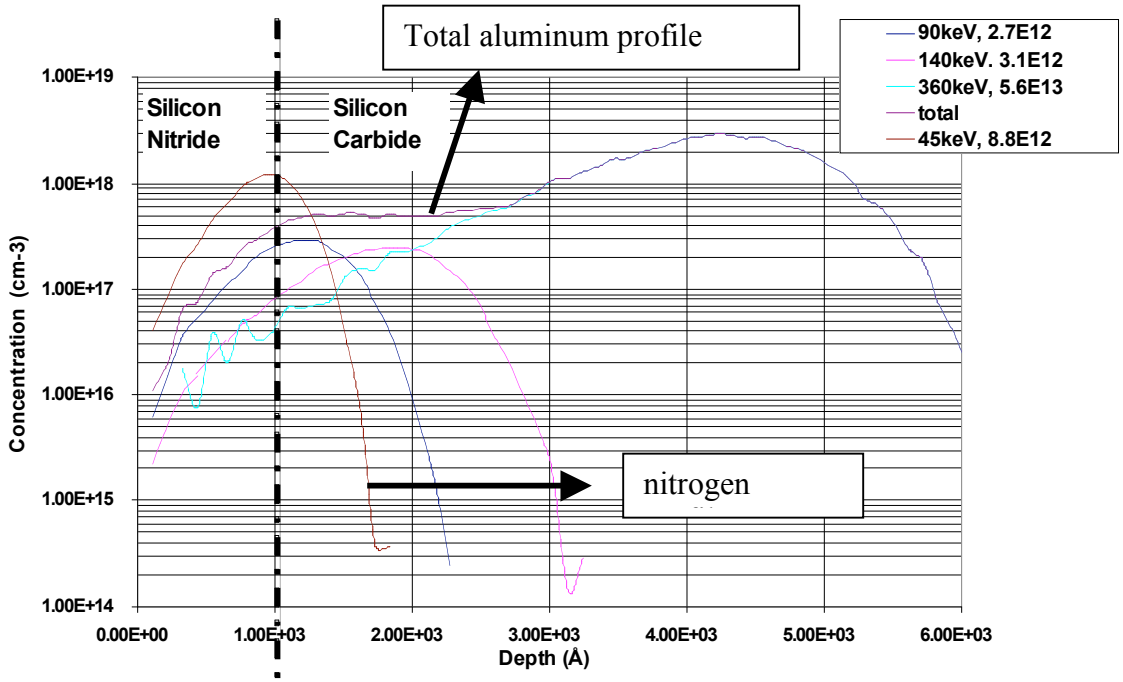


Figure 3.100 pwell retrograde implant profile (TRIM simulation). The brown curve is the counter-doped implant (nitrogen).

3.2.3.3 N+ Source Implantation

Before sending the samples to Kroko for the n+ source implantation, Ti/Au (~400 nm) was deposited to cover the areas where p+ base contact implantation will take place in the next step. Figure 3.101 is the cross-sectional view of the device after the n+ implantation and figure 3.102 is a photograph of the devices after the Ti/Au deposition. Figure 3.103 shows the n+ implant profile.

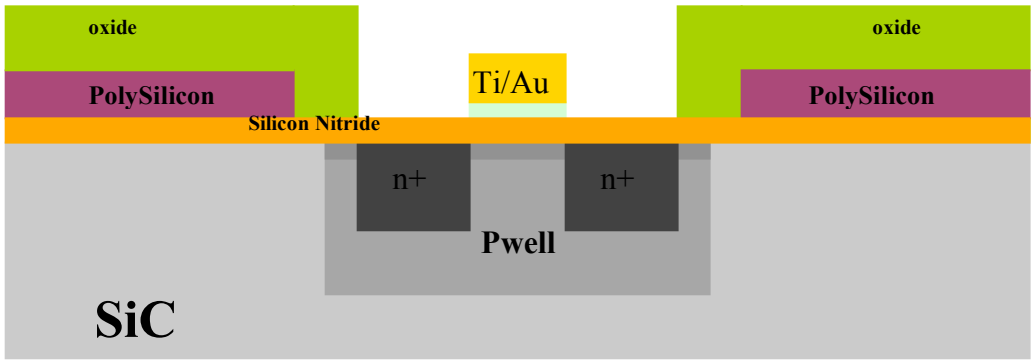


Figure 3.101 Cross-sectional view of the device after n+ implantation.

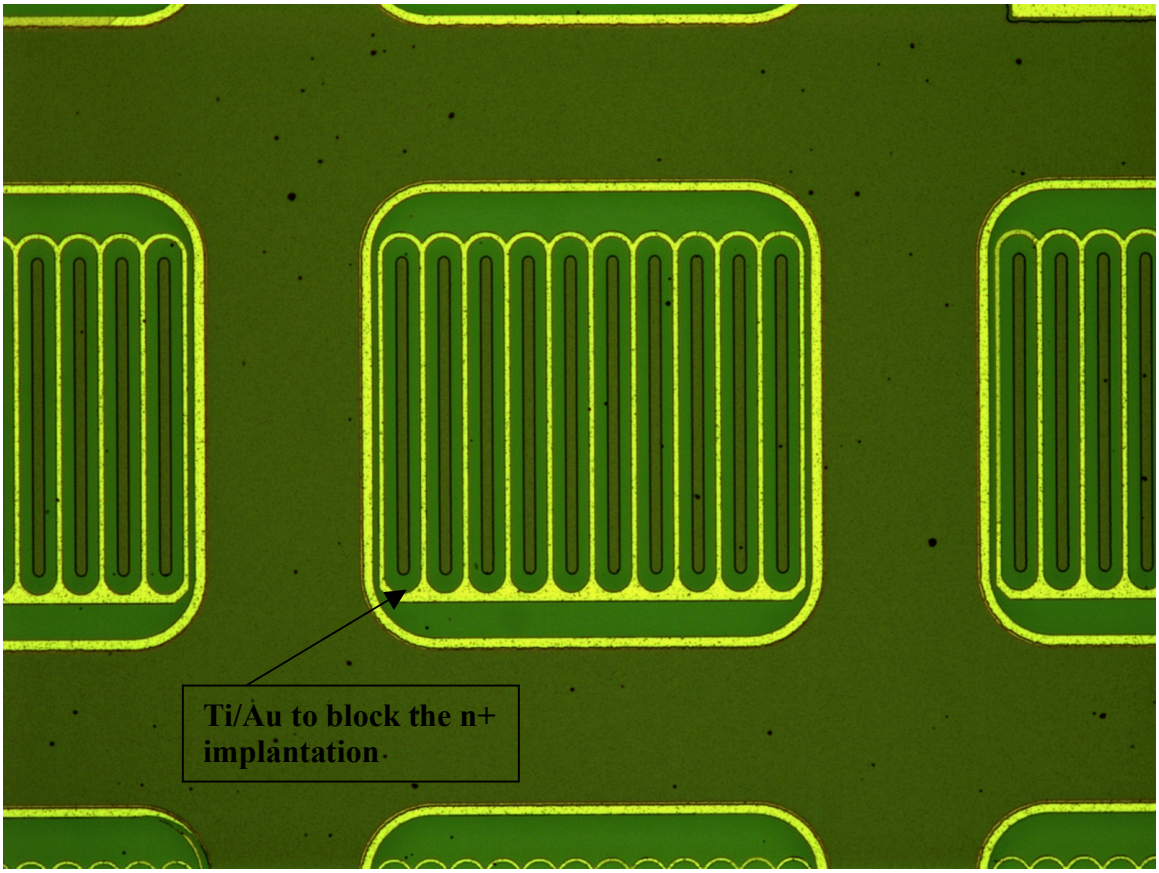


Figure 3.102 Devices right before the n+ implantation.

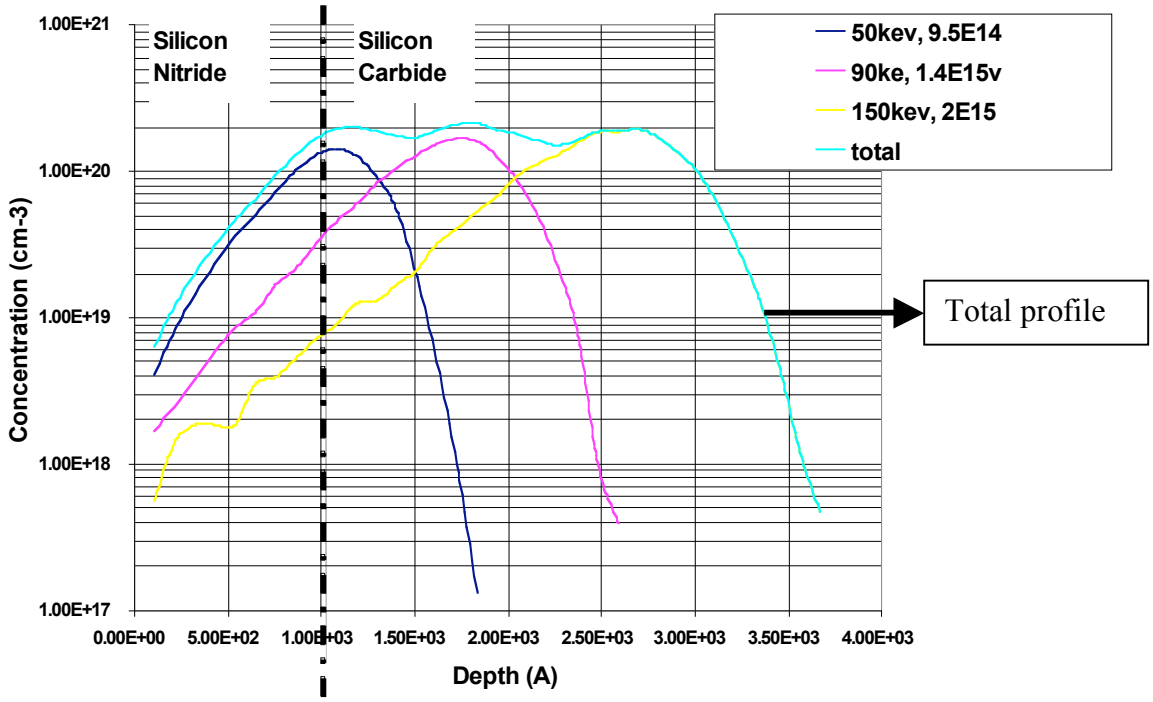


Figure 3.103 N+ implant profile (TRIM simulation).

3.2.3.4 P+ Base Contact Implantation

After the n+ source implantation, everything was stripped off the SiC surface. Then a thin layer of oxide (~20 nm) was deposited by an e-beam evaporator, or grown thermally. The purpose of the oxide layer was to avoid the direct contact of the SiC wafer and the Ti/Au layers which were deposited later as the p+ base implantation mask. Figure 3.104 shows the cross-sectional view of the device after the p+ base implantation. Figure 3.105 is a photograph of the devices after Ti/Au deposition. The implant profile is shown in figure3.106.

Unlike the SiC DMOSFETs, a portion of the on-state currents of the IGBTs flow through the p+ contacts. So a low p-type contact resistance is critical to the on-state performance of the IGBTs. Therefore, a continuous p+ implantation was employed instead of the small islands of p+ implantation sometimes used in the SiC DMOSFETs (see FIg. 3.107).

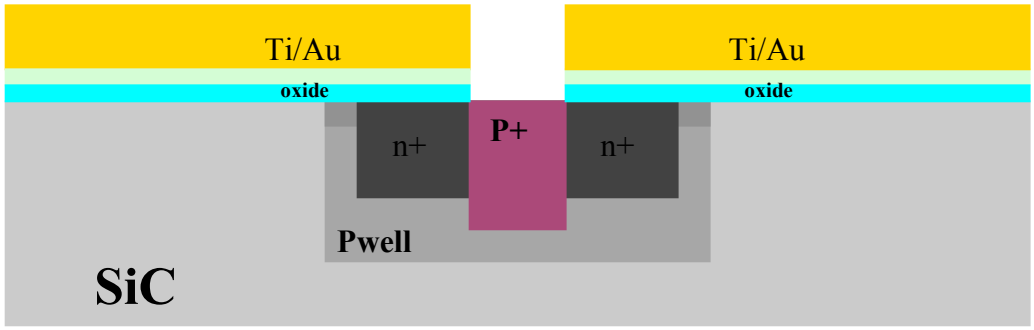


Figure 3.104 Cross-sectional view of the device after p+ implantation.

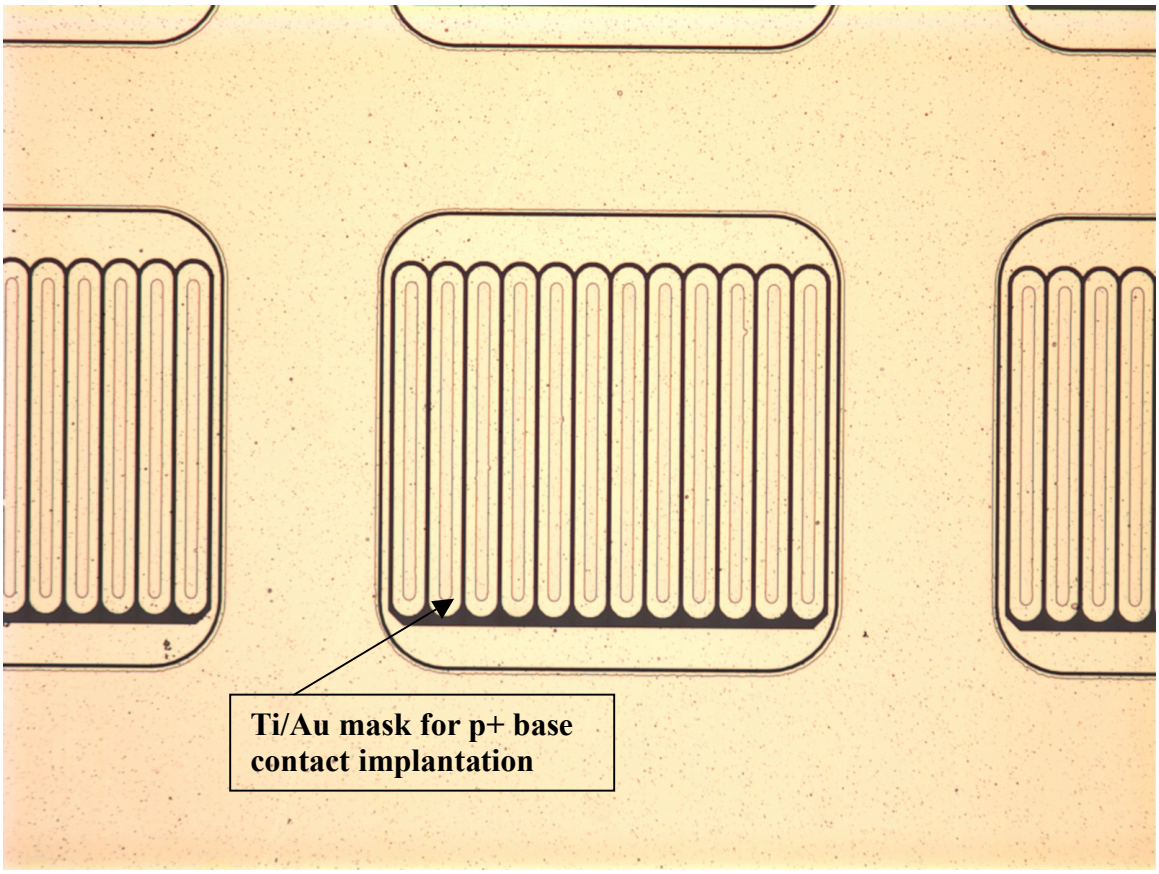


Figure 3.105 Devices right before the p+ implantation at Kroko.

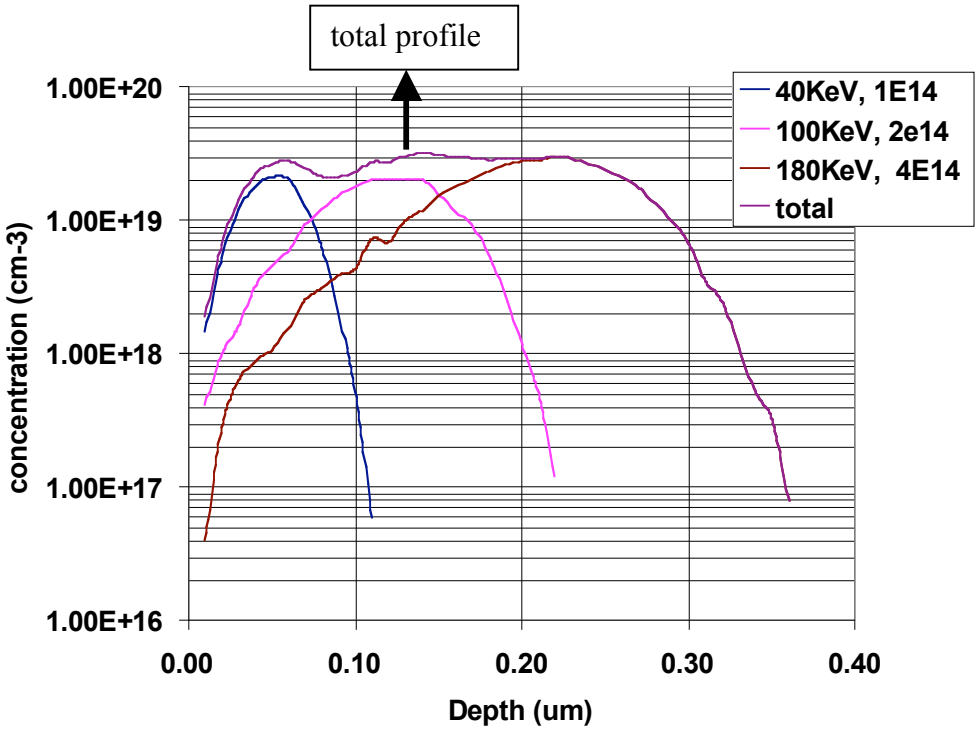


Figure 3.106 P+ implant profile (TRIM simulation).

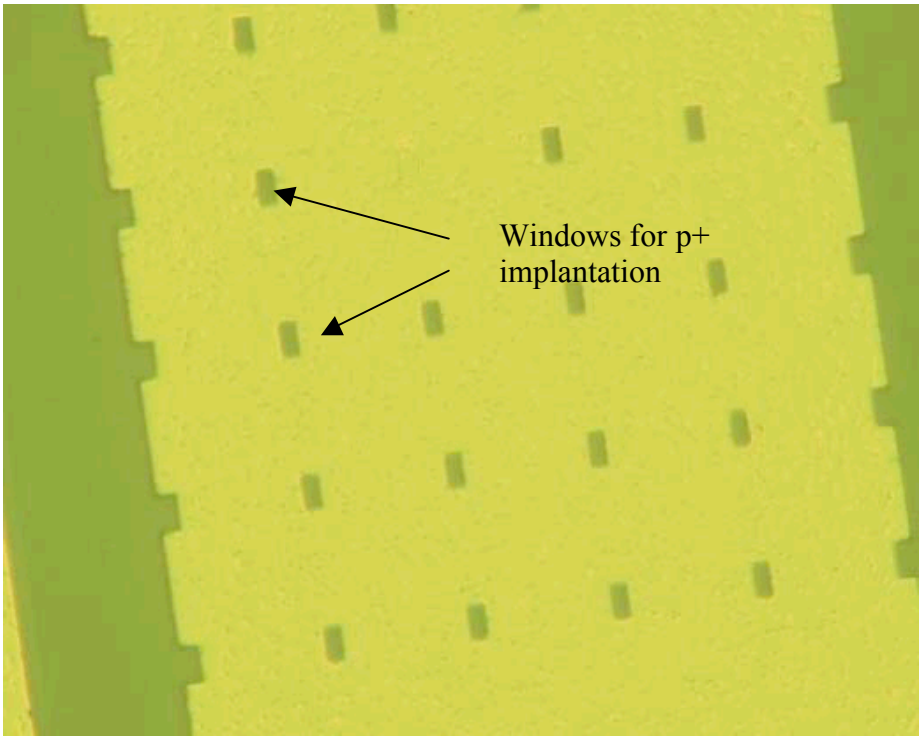


Figure 3.107 Discontinuous p+ implantation employed in the SiC DMOSFETs [19].

3.1.3.5 Implant Activation

After all the implantations were done, implant activation was performed in the Epigress VP508 SiC CVD reactor.

Sample 1 was annealed in silane (SiH_4) ambient at 1600ºC for 20 min. Severe step bunching was observed on the source region after the anneal. As shown in Figs. 3.108(a) and (b), the rms surface roughness on the n+ source region was around 17nm, which is much higher than a typical roughness after silane anneals (~5-6nm for n+ regions). Since step bunching usually occurs at high temperatures, it is likely that the actual annealing temperature was higher than 1600 ºC. Step bunching was not observed on the pwell and p+ regions. Their rms surface roughnesses were around 0.93nm and 1.1nm, respectively (see Figs. 3.109 and 3.110).

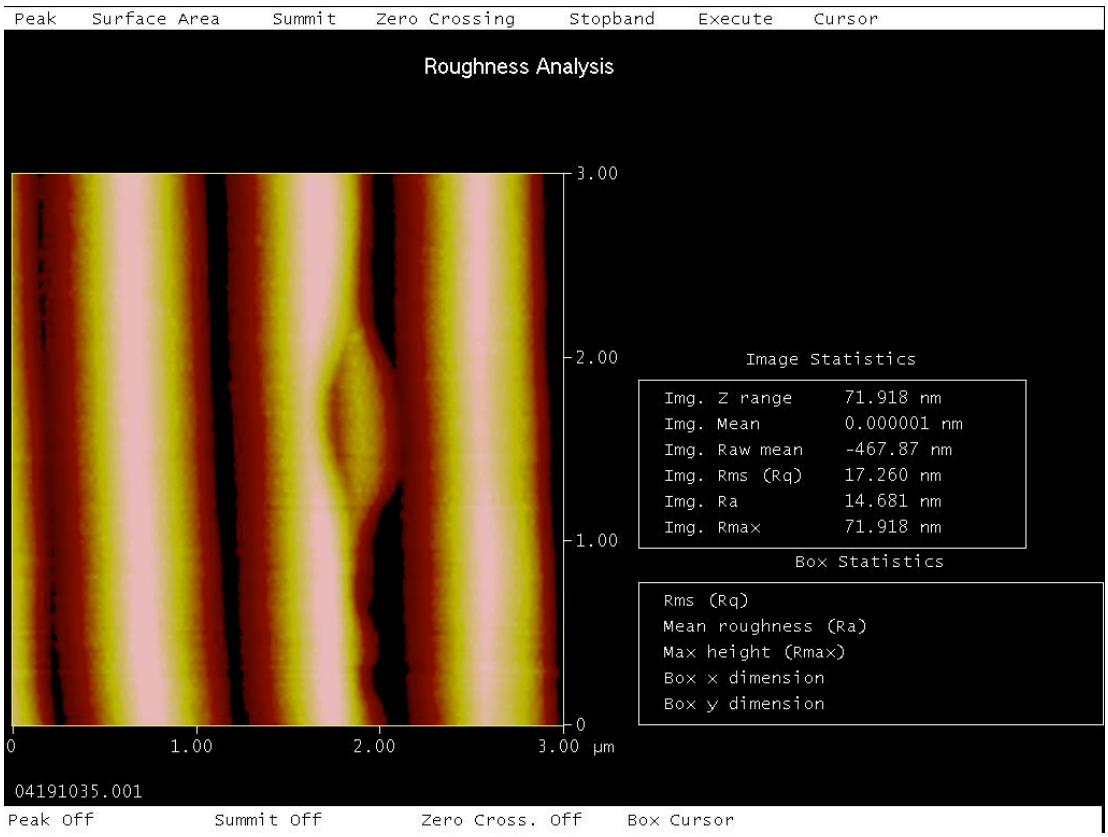


Figure 3.108 (a) AFM picture of the n+ source region in sample 1 after implant activation anneal.

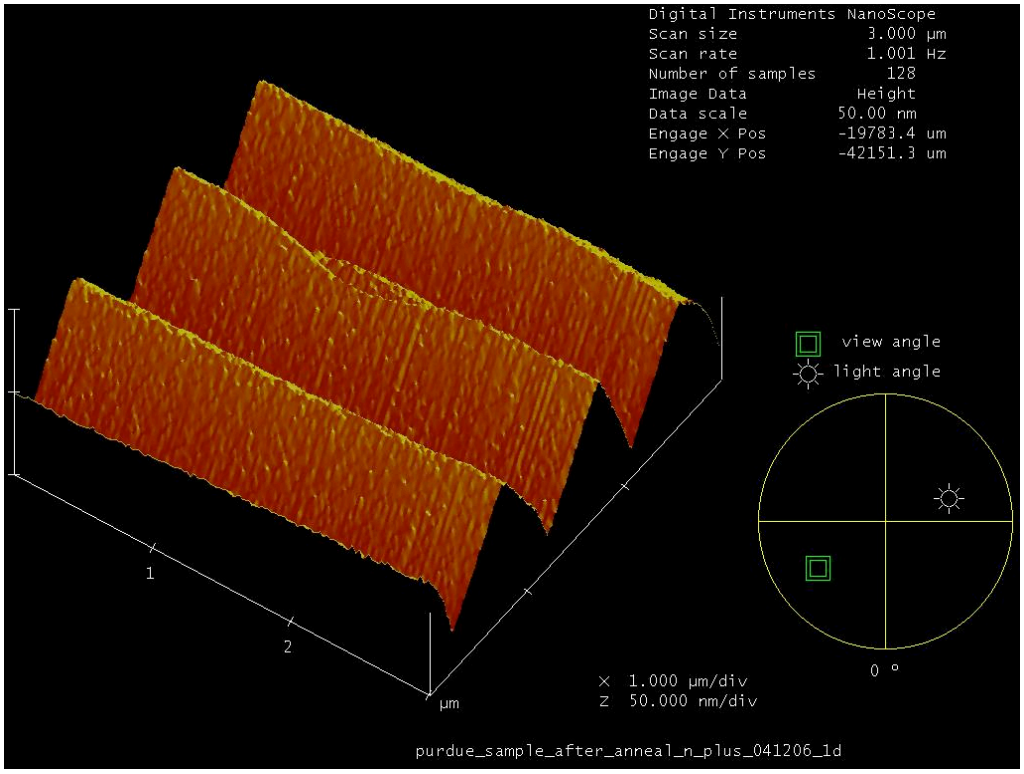


Figure 3.108 (b) 3D AFM picture of the n+ source region in sample 1.

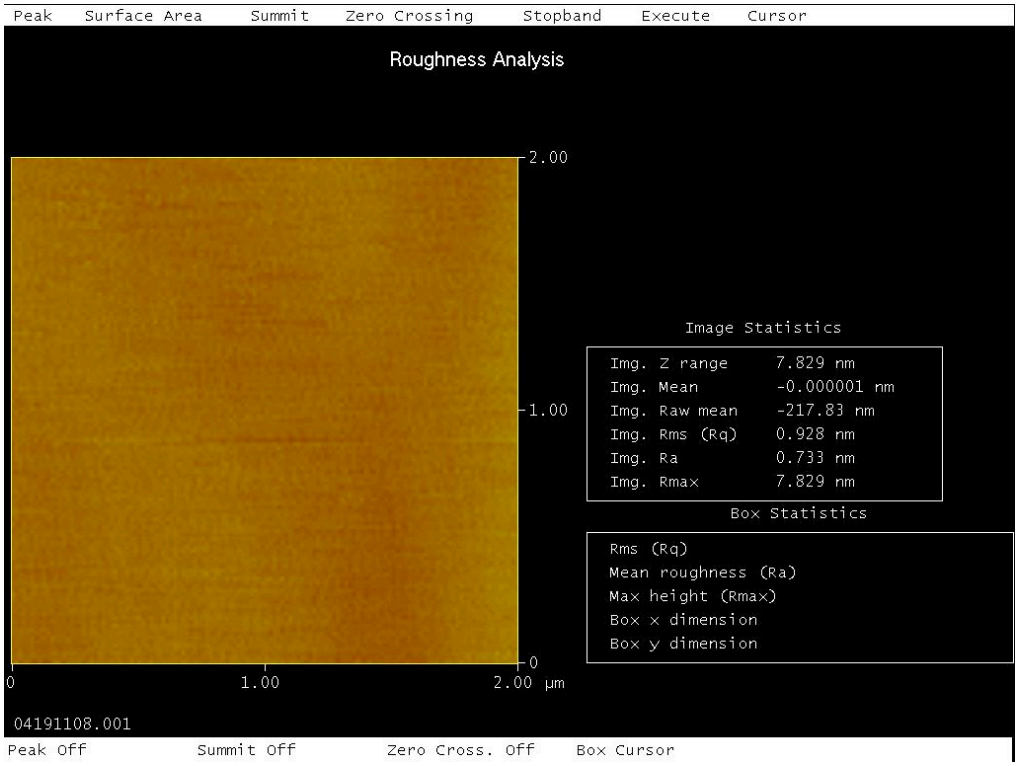


Figure 3.109 AFM picture of the pwell region in sample 1 after the anneal.

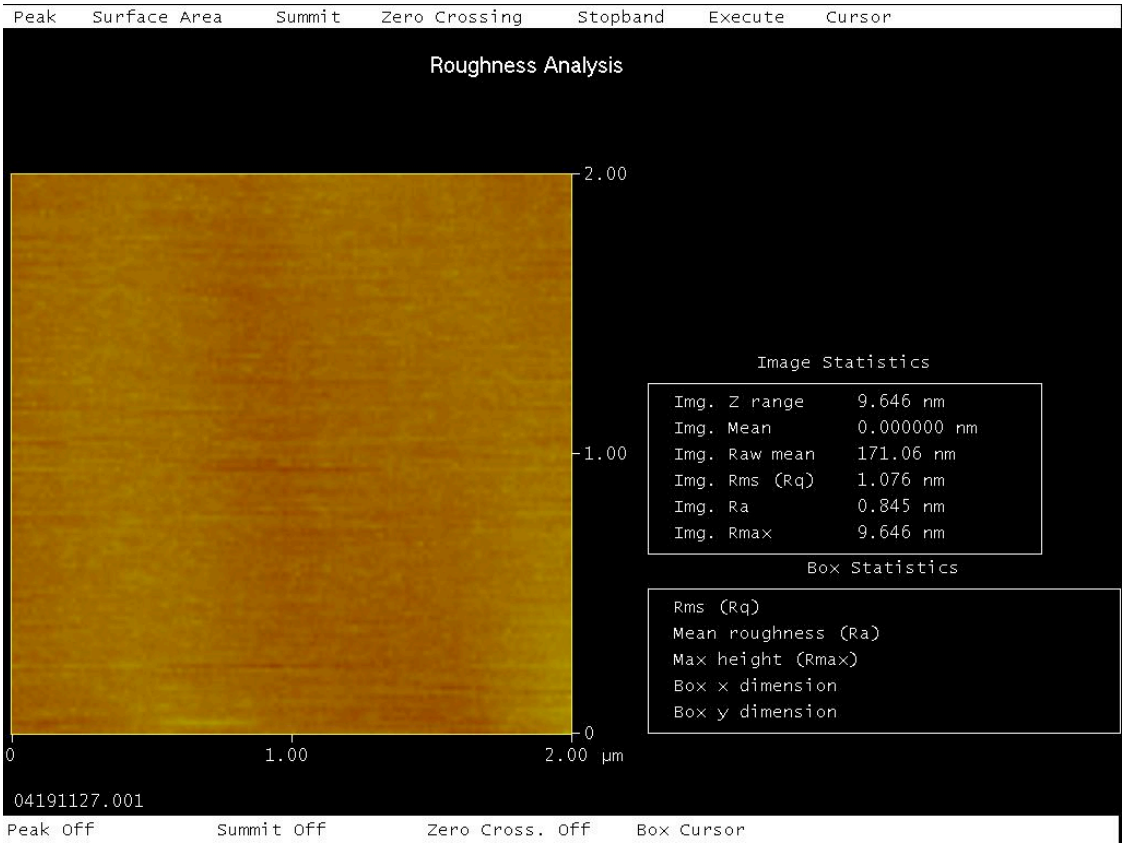


Figure 3.110 AFM picture of the p+ region in sample 1 after the anneal.

Sample 2 and sample 3 were annealed under the same conditions as sample 1. Before the anneal, AFM measurements were made on sample 2 to determine the rms surface roughnesses of the pwell, n+ and p+ regions. They were 0.34nm, 3.4nm and 0.48nm, respectively. Figure 3.111 shows the AFM pictures of sample 2 after the anneal. As shown in these pictures, the n+ source region had the roughest surface, and its rms roughness was around 9.1nm.

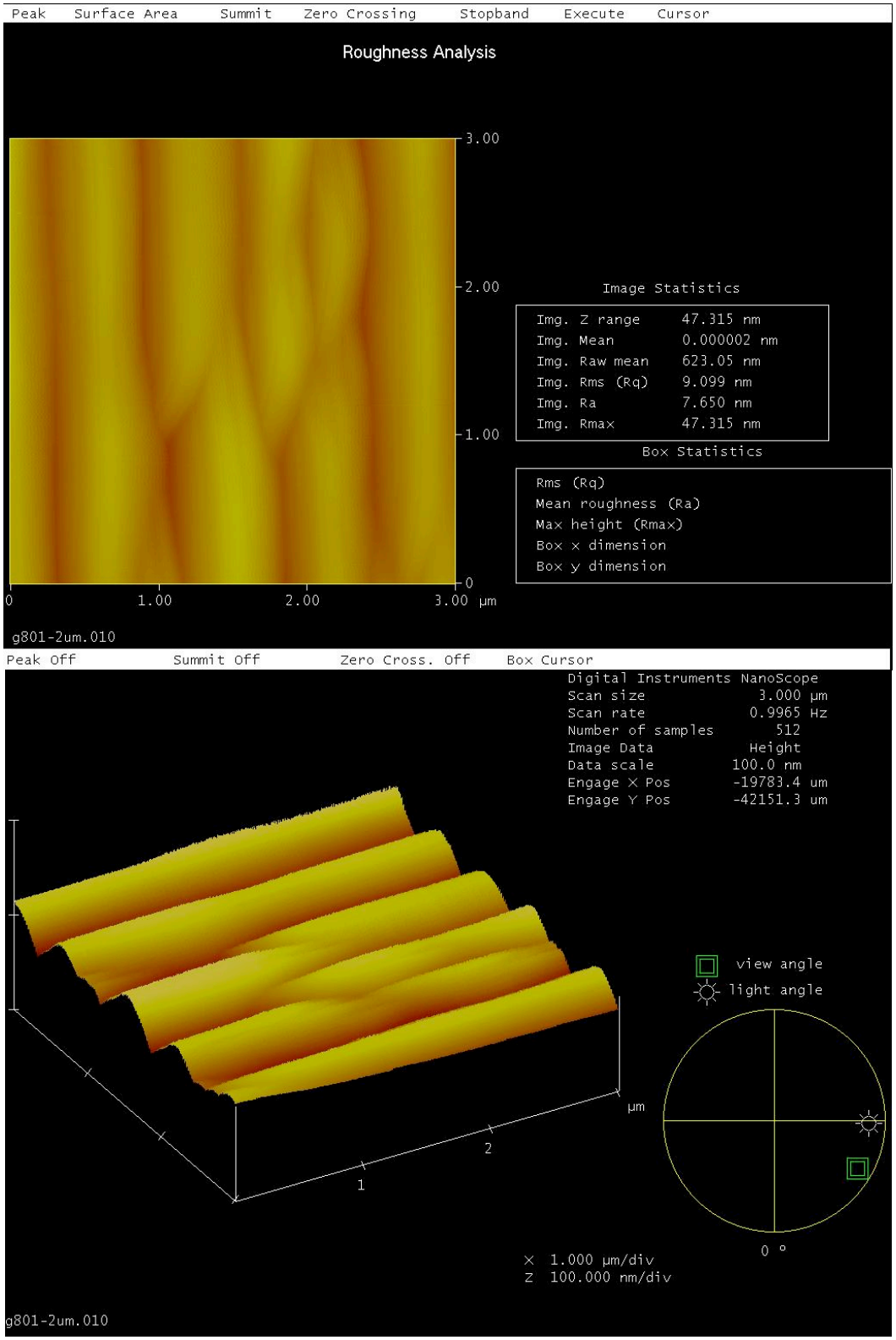


Figure 3.111(a) AFM pictures (2D and 3D) of the n+ source region in sample 2 after the anneal.

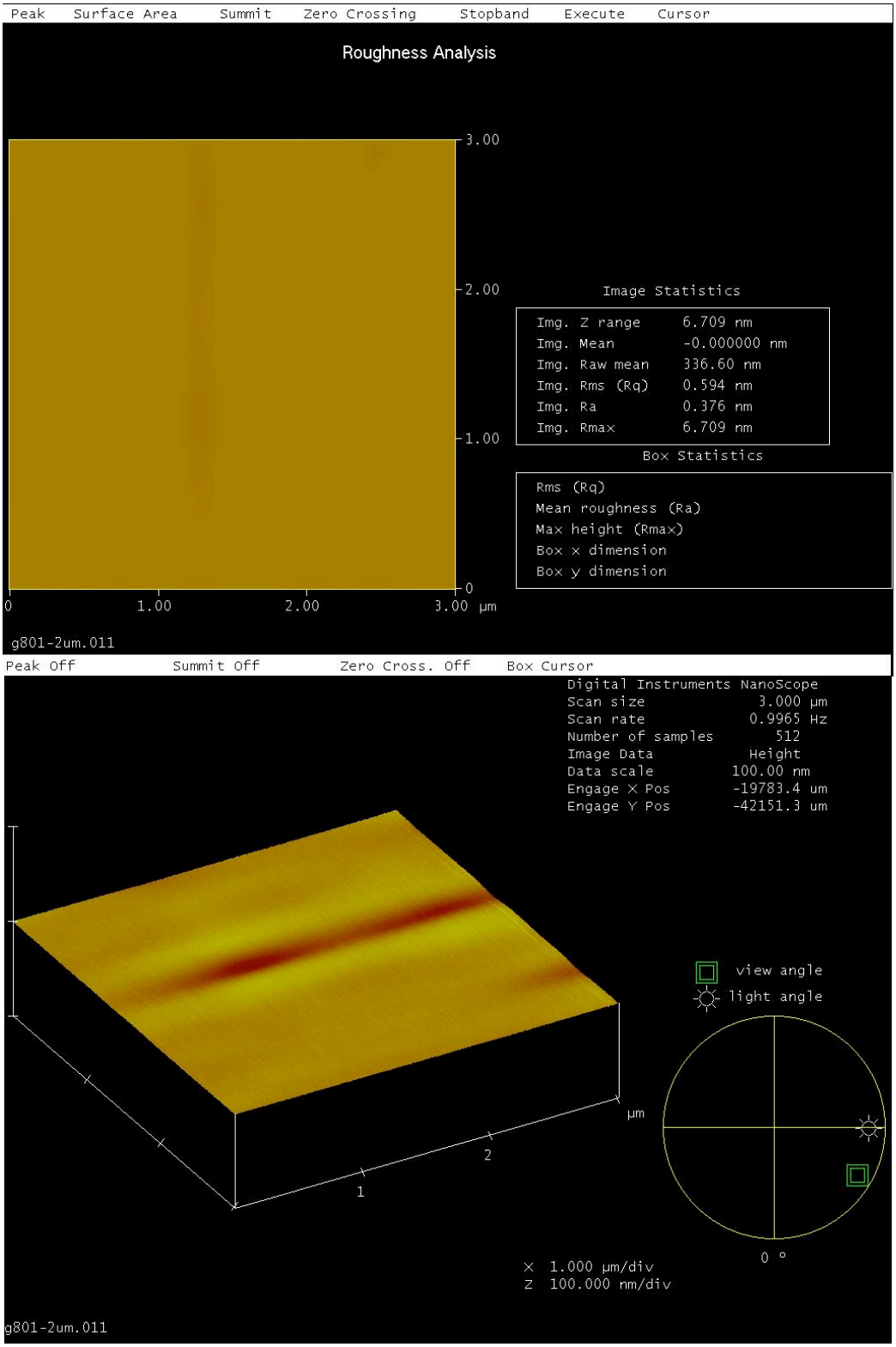


Figure 3.111(b) AFM pictures (2D and 3D) of the pwell region in sample 2 after the anneal.

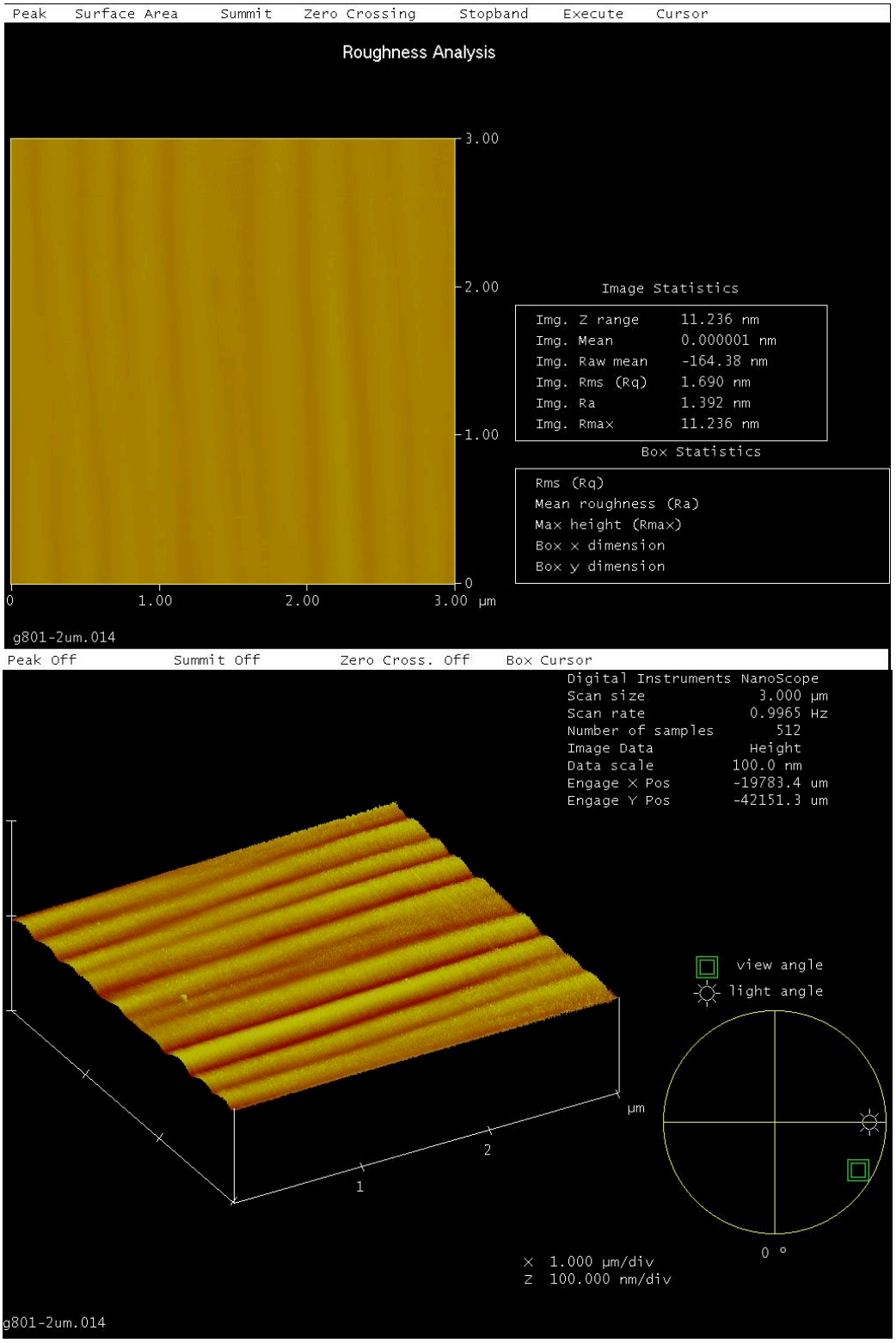


Figure 3.111(c) AFM pictures (2D and 3D) of the p+ base region in sample 2 after the anneal.

To further reduce the surface roughness, we decided to employ graphite-cap anneal on samples 4 to 6. The procedure of the graphite-cap anneal is:

1. Spin photo resist AZ1518 on the SiC wafer at 2500 RPM for 20 sec. Make sure that the wafer is fully covered with AZ1518 before spinning.
2. Hard bake at 120ºC for 20 min.
3. Graphitize the photo resist by annealing the sample in Ar at 600 ºC for 20 min.
4. Anneal the sample at 1600 ºC in Ar for 30 min to activate the implants.
5. Remove the graphite by oxidizing the sample at 900 ºC for 1 to 2 hours, or barrel etching the sample at 300 to 400 W for 1 to 3 hours in O_2, using the Branson/IPC Model 3000 barrel-type plasma etching system.

Figure 3.112 shows the AFM picture on the n+ region in sample 4 after the implant activation anneal. The rms roughness was only 0.164nm.

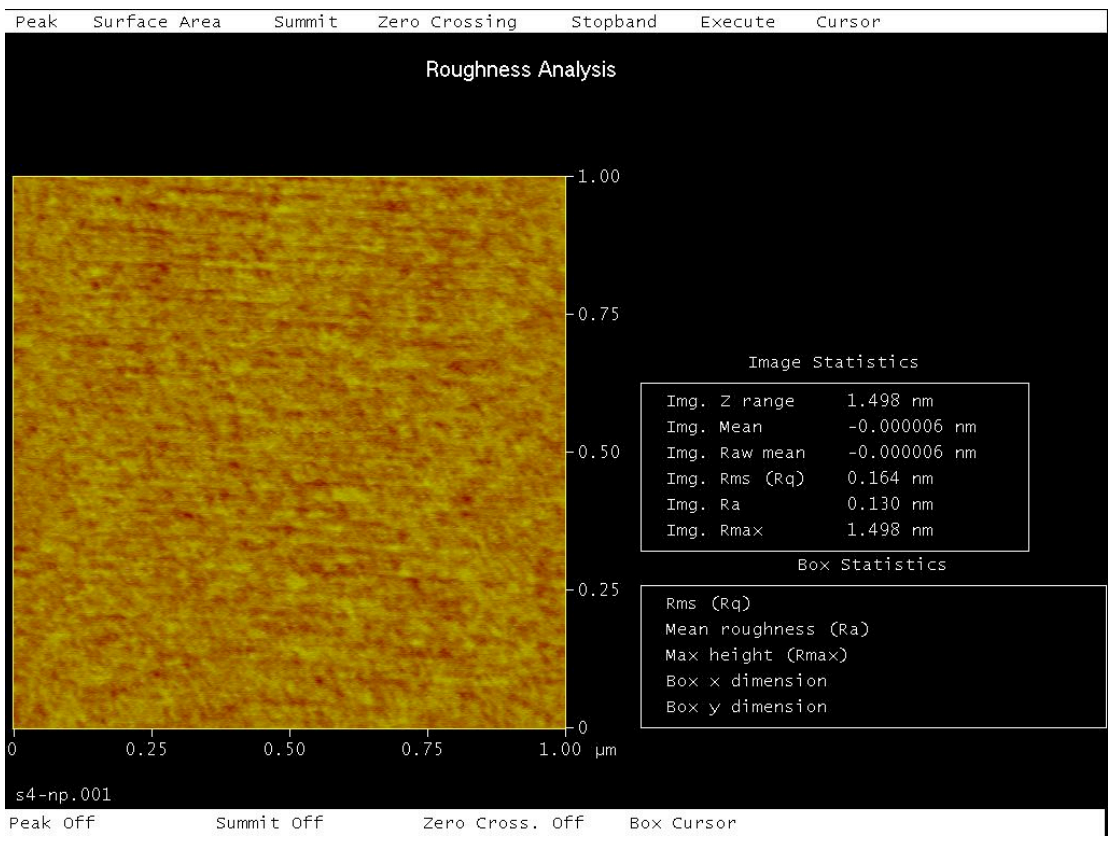


Figure 3.112 AFM picture of the n+ base region in sample 4 after the implant anneal.

3.2.3.6 Gate Oxidation, NO Anneal and Gate Deposition

After the implant activation anneal, samples 1 to 6 were oxidized in the pyrogenic system (Thermco Mini-Brute) to form the gate oxide. NO anneal was performed on samples 1, 3, 4, 5 and 6 to reduce the interface trap density.

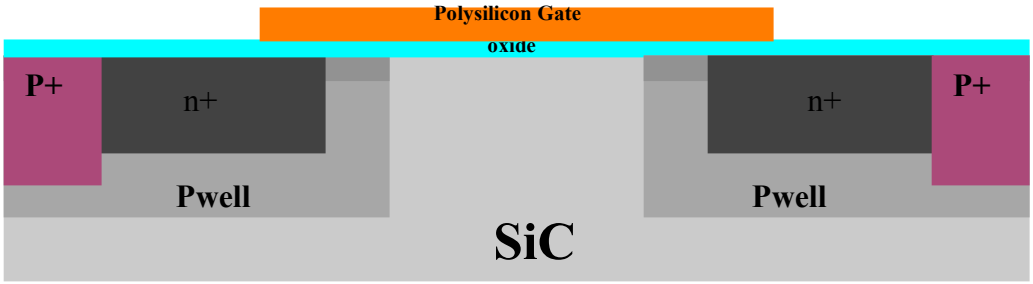


Figure 3.113 Cross-sectional view of the device after patterning the doped polysilicon layer as the gate electrode.

For samples 1 to 3, a 0.5 µm polysilicon layer was deposited, doped with phosphorus and patterned as the gates of the IGBTs. The cross-sectional view of the device after these steps is shown in Fig. 3.113. Figure 3.114 shows a photograph of the device with the gate oxide and the polysilicon gate electrode. Sample 1 was oxidized at 950ºC for 17.5 min, followed by an in-situ Ar anneal at 950 ºC for 30 min. Low temperature re-oxidation anneal was not performed. Then the sample was annealed in NO at 1175 ºC for 2 hours. The estimated oxide thickness after the NO anneal was around 40 nm. Later, the gate oxide in sample 1 was found leaky (see section 3.2.4). This could be caused by the unusually rough surface, since the oxide thickness is only about twice the rms roughness of the surface. To prevent the oxide leakage problem in samples 2 and 3, we decided to grow thicker oxides on these two samples. Sample 2 was oxidized at 1100 ºC for 45 min and the resulting oxide thickness was 115.2 nm. Sample 3 was oxidized at 1020 ºC for 24 min, then re-oxidized at 1100 ºC for 80 min. The oxide thickness after both oxidations was 240 nm. Ar anneal at 950 ºC for 30 min was performed for both samples. The low temperature re-oxidation anneal was not done for either of them. To study whether the NO anneal could cause the oxide leakage problem as found in sample 1, only sample 3 was annealed in NO after the oxidations. It was annealed at 1175 ºC for 1 hour. The estimated increase of the oxide thickness was around 4 nm [20]. Since the

counter-doped implant in the pwell was designed for 50 nm thick gate oxides, the thicker oxides in sample 2 and 3 would consume all the counter-doped implants and result in a higher threshold voltage for the IGBTs in these two samples.

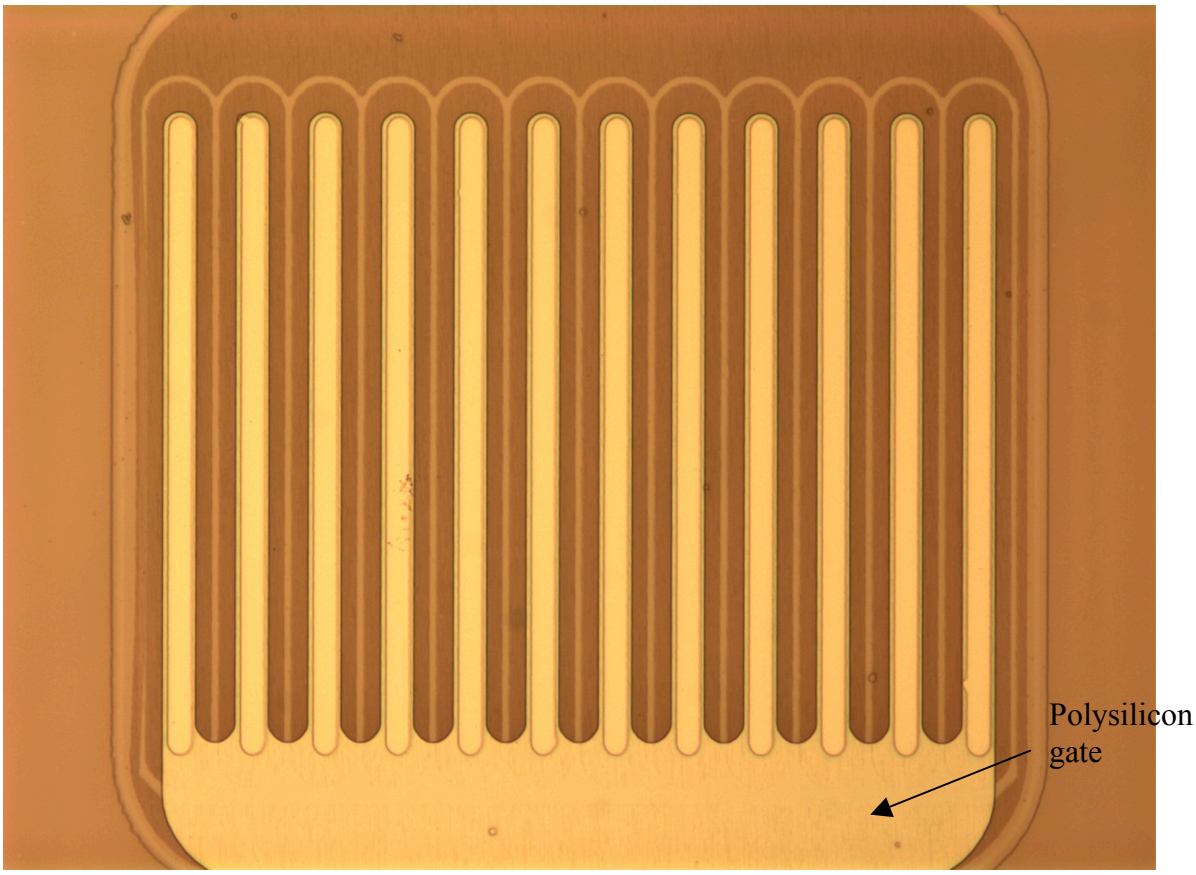


Figure 3.114 A device with gate oxide and polysilicon gate electrode.

The oxides on sample 2 and sample 3 were not leaky after the oxidations. However, oxide leakage and premature oxide breakdown occurred after the contact anneal (see details in section 3.2.4). Due to the annealed contact metals on these samples, they could not be re-oxidized in the pyrogenic system. To get an unleaky insulated layer, after stripping the polysilicon gates and the thermal oxides, sample 1 and sample 2 were sent to GE Global Research (Niskayuna, NY) for LTO (low temperature oxide) deposition (T≈450 °C). A 240 nm LTO layer was deposited. Then 100 nm Al was evaporated in an e-beam evaporator and patterned as the gate. Since the patterning of Al needs lift-off lithography as opposed to the etching lithography for patterning the

polysilicon, the polarity of the photo resist must be reversed when the same mask is used. PR AZ5214-E was used for patterning the Al gate. The procedure of the reversing lithography is as follows:

1. clean the sample by solvents
2. clean the photomask (Acetone 15 min + DI+ Piranha 15 min)
3. hard bake the wafer for 20 min at 120 ºC
4. apply HMDS at 5000 RPM for 30 sec.
5. apply AZ 5214-E at 4000 RPM for 30 sec.
6. bake the sample on a hotplate at 90 ºC for 60 sec
7. expose at 23 mW/cm^2 for 7 sec
8. bake the sample on a hotplate at 110 ºC for 1 min
9. flood expose at 23 mW/cm^2 for 20 sec
10. develop in AZ 327 for 28 sec.

Samples with LTO as the gate dielectric no longer have the gate leakage problem. However, the unannealed LTO may not have a good interface with the semiconductor. To combine the advantages of the LTO (not leaky) and the thermal oxide (good interface), we came up with following fabrication procedure for samples 4 to 6:

1. Oxidize the samples in the pyrogenic system. The oxide thickness should be less than 50 nm, so the counter-doped implants still remain.
2. Anneal the samples in NO at 1175 ºC for an hour.
3. Deposit the p+ contact and the back contact
4. Anneal the p+ and back contacts
5. Evaporate metal(s) as the gate electrode (metal gate is used because of the possible removal of the gate in a later step. Polysilicon etchant has HF in it, which etches the thermal oxide).
6. Measure the gate leakage current. If the gate is not leaky, then deposit the n+ contact (Ti/Ni without annealing) .
7. If the gate is leaky, strip the gate, and send the samples to GE for LTO deposition,
8. Put the gate back on and deposit the n+ contact.

Samples 4 to 6 were oxidized in the pyrogenic system at 1100 ºC for around 20 min, then annealed in Ar at 950 ºC for 30 min. The low-temperature re-oxidation anneal

was not performed. Then all the samples were annealed in NO at 1175 ºC for 1 hour 10 min. The estimated oxide thickness after the NO anneal was around 45 nm.

Ti/Au (around 50nm/100nm) was evaporated as the gate. Figure 3.115 shows the picture of a device on sample 4 with the Ti/Au gate.

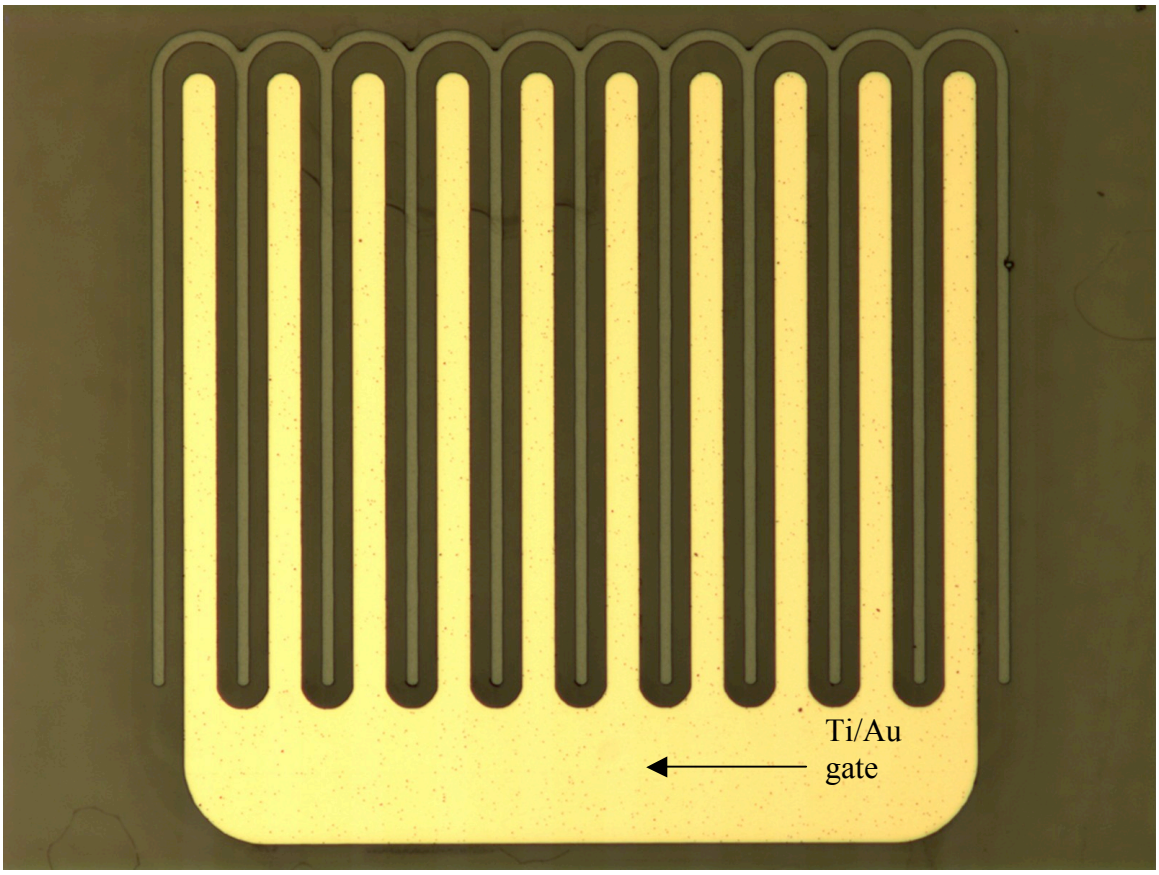


Figure 3.115 A device on sample 4 with Ti/Au gate.

3.2.3.7 P+ Contact Formation

33 nm Ti and 167 nm Al were evaporated and patterned as the p+ contact metals. After the p+ liftoff lithography was done, the samples were first soaked in BHF to remove the oxides on top of the p+ implant regions. Then RIE was done to roughen the surface of the exposed SiC. The roughened SiC surface would have a larger contact area with the contact metals, which should reduce the contact resistance. The RIE step was followed by barrel etching in O_2, which removes the residual photo resist on the SiC. The samples were dipped in BHF right before being loaded in the evaporator to remove the

thin oxide layer grown during the barrel etching. And finally, the contact metals were deposited. A layer of Ni (~50 nm) was deposited on top of Ti/Al to protect them from being stripped off when the sample is dipped in BHF before the n+ contact metal deposition in the next step. The cross-sectional view of the device at this point is shown in Fig. 3.116. Figure 3.117 and 3.118 are the photographs of devices on sample 2 (with polysilicon gate electrodes) and sample 4 (without gate electrodes) after this step, respectively. 33 nm Ti and 167 nm Al was deposited on the backside of the wafer as the drain contact. A layer of Ni (~100nm) was also deposited to cover the contact metals.

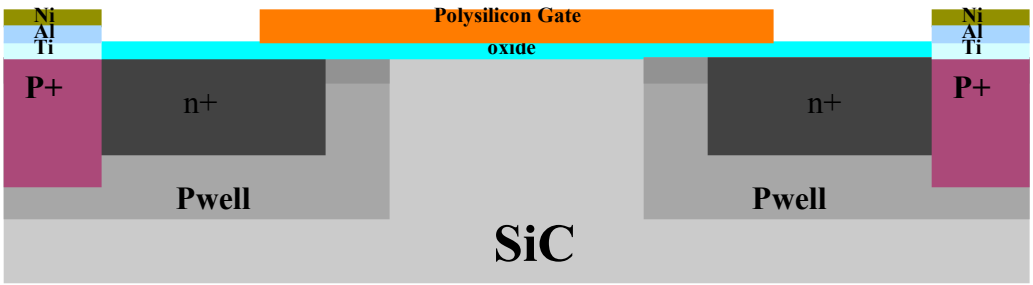


Figure 3.116 (a) Cross-sectional view of devices on samples 1 to 3.

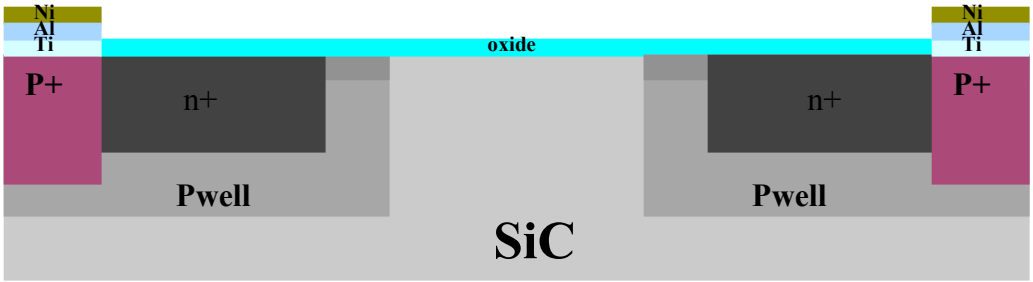


Figure 3.116 (b) Cross-sectional view of devices on samples 4 to 5.

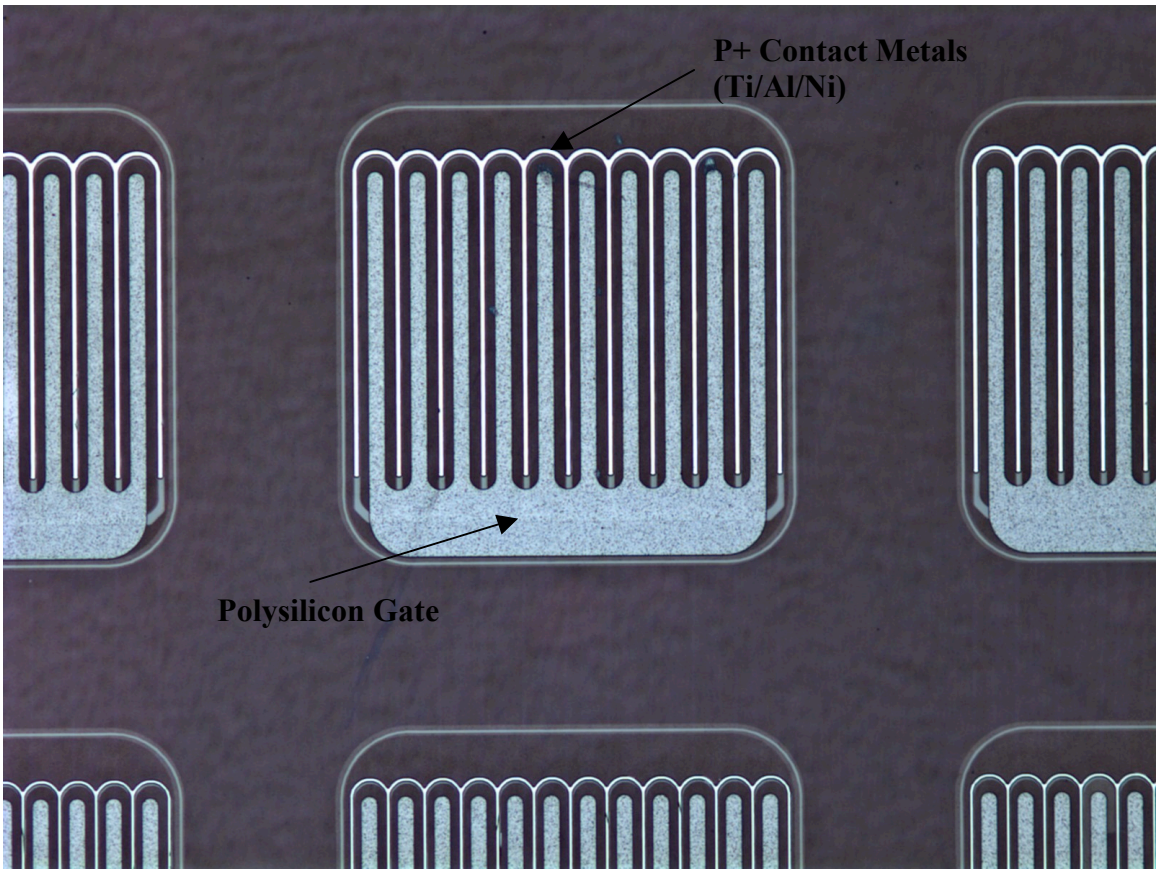


Figure 3.117 Devices on sample 2 after the p+ contact deposition.

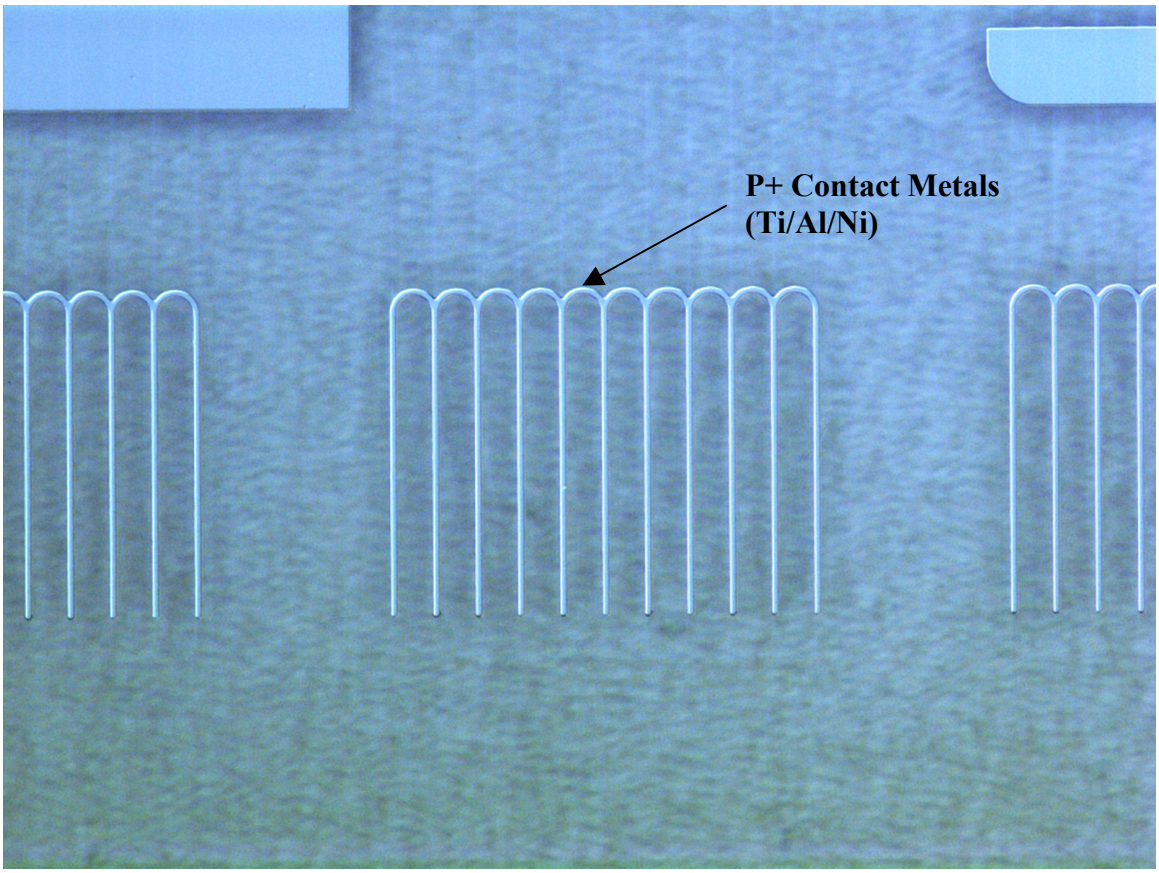


Figure 3.118 Devices on sample 4 after the p+ contact deposition.

3.1.3.8 N+ Contact Formation

N+ liftoff lithography was done, followed by BHF dipping, RIE, barrel etching and a second BHF dipping as described earlier. For samples 1 to 3, 100 nm Ni was evaporated as the contact metal before the contact anneal. For samples 4 and 5, 50 nm Ti and 100 nm Ni were evaporated as the contact metals. They were not annealed and therefore evaporated after the annealing of the p+ contacts. Figure 3.119 shows the cross-sectional view of the device after this step. Figure 3.120 and 3.121 are the photographs of the devices on sample 2 and 4, respectively.

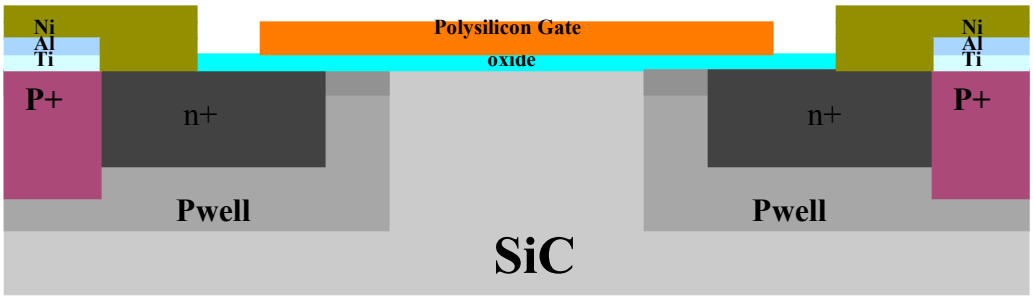


Figure 3.119 (a) Cross-sectional view of devices on samples 1 to 3.

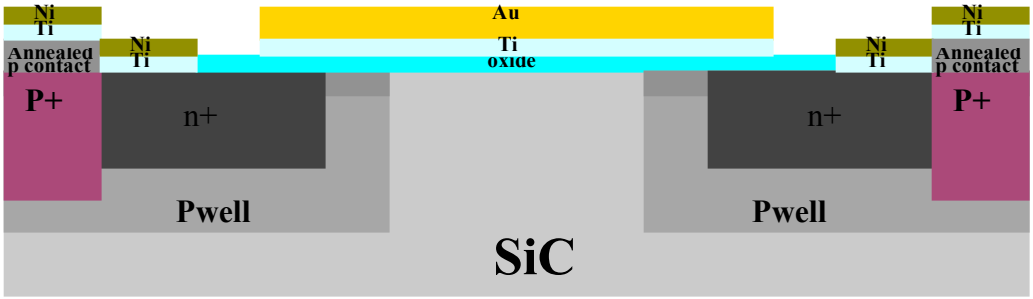


Figure 3.119 (b) Cross-sectional view of devices on samples 4.

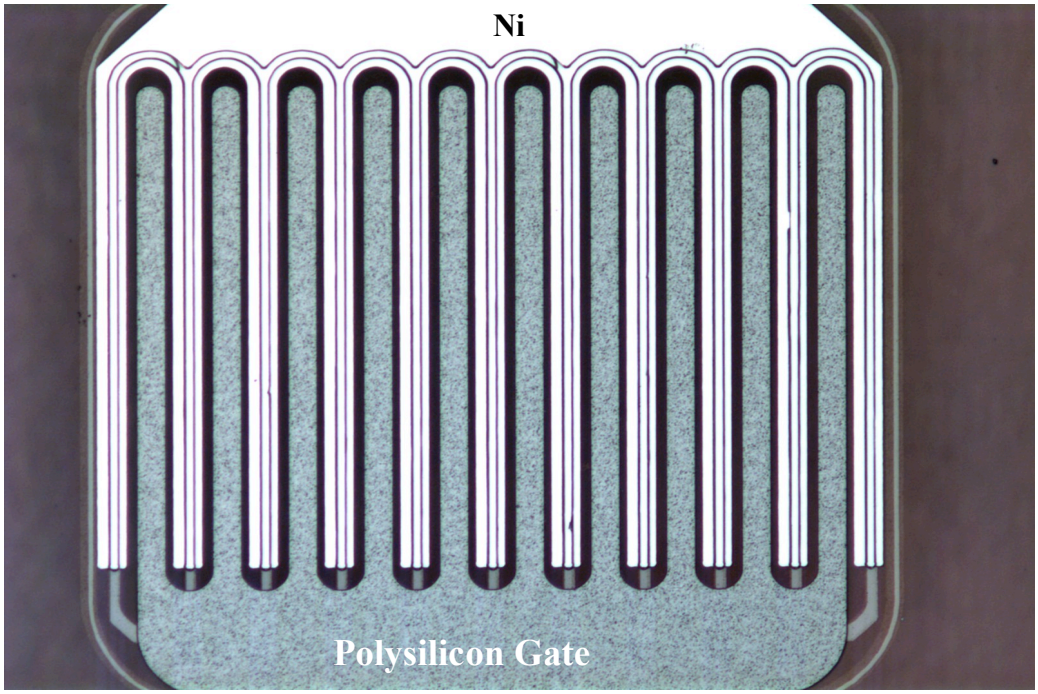


Figure 3.120 A device on sample 2 after the n+ contact deposition.

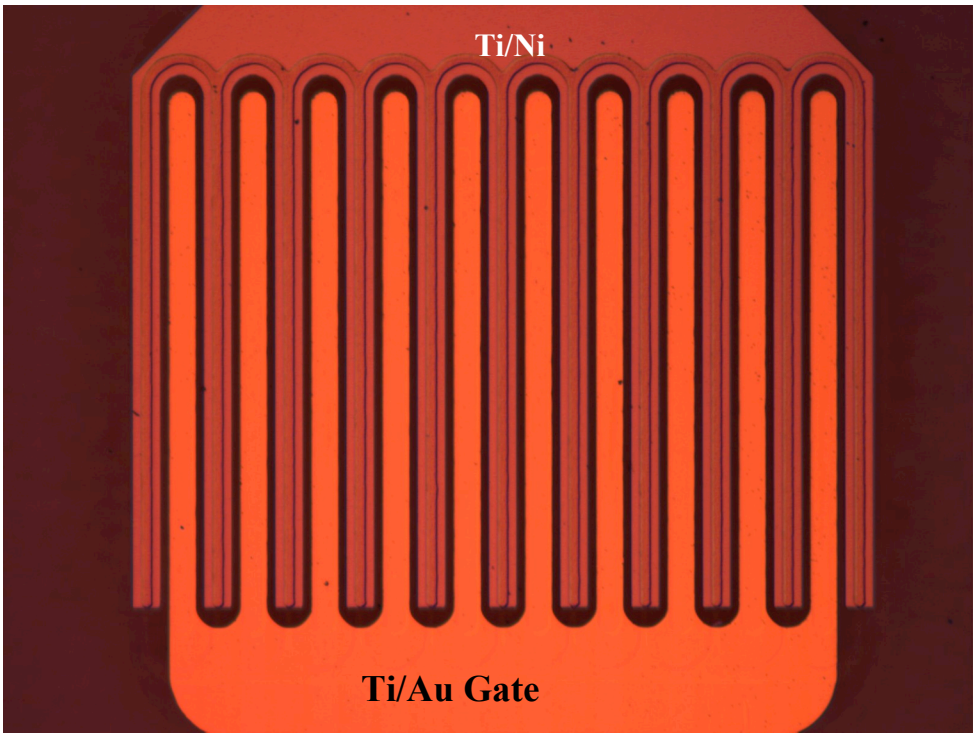


Figure 3.121 A finished device on sample 4.

3.2.2.9 Contact Anneal

The metal contacts of sample 1 were annealed in the SiC contact annealer (Kurt Leskar custom-designed dual-chamber vacuum system) in vacuum for two minutes. The targeting sample temperature was 1000 ºC. The control thermocouple was on the underside of the heater. We assumed that the sample was 100 ºC cooler than the underside of the heater, based on a temperature calibration performed a few years ago, so the setting temperature was 1100 ºC. However, a calibration performed after the contact anneals of samples 1 to 3 showed that the temperature difference of the sample and the underside of the heater was actually around 300 ºC. Therefore, the actual temperature of sample 1 during the contact anneal should be around 800 ºC.

Sample 2 was annealed at 1000ºC for two minutes in the Epigress VP508 SiC CVD reactor. Sample 3 was cut into four pieces and used as testers to study the impact of contact annealing on the gate oxide. Three of these pieces were annealed in the SiC contact annealer in vacuum for two minutes, with targeting temperatures of 850 ºC, 900 ºC and 950 ºC, respectively. The control thermocouple was on the underside of the heater when these testers were annealed, so the actual sample temperatures were around 650 ºC, 700 ºC and 750 ºC, due to the same reason stated in the last paragraph.

When annealing the contacts on sample 4 in the SiC contact annealer (in vacuum), we decided to put the control thermocouple on top of the sample. Test runs with a dummy sample were done before the actual anneal. The setting temperatures (also the targeting sample temperatures) were around 850 ºC. The test runs went well. However, when sample 4 was annealed, the temperature of the heater rose a lot faster than those of the test runs. One minute and 15 seconds after the heating started, sample 4 broke into two pieces and fell off the heater. At that moment the control thermocouple temperature (also the sample temperature) was around 600 ºC and the heater temperature was around 1100 ºC. The different behavior of the heater between the test runs and the actual run might be cause by the backside metal on sample 4, since the dummy sample had no metals on it. The p+ contact was ohmic after the contact anneal. This suggest that the sample was well above 700 ºC when it broke during the contact anneal [21]. There might be a lag in the thermometer display, or since the thermocouple could conduct heat from the sample, the area of the sample where the thermocouple was probing may have a lower temperature than the rest of the sample.

Figures 3.122 to 3.124 are the photographs of samples 1, 2 and 4 after the contact anneal.

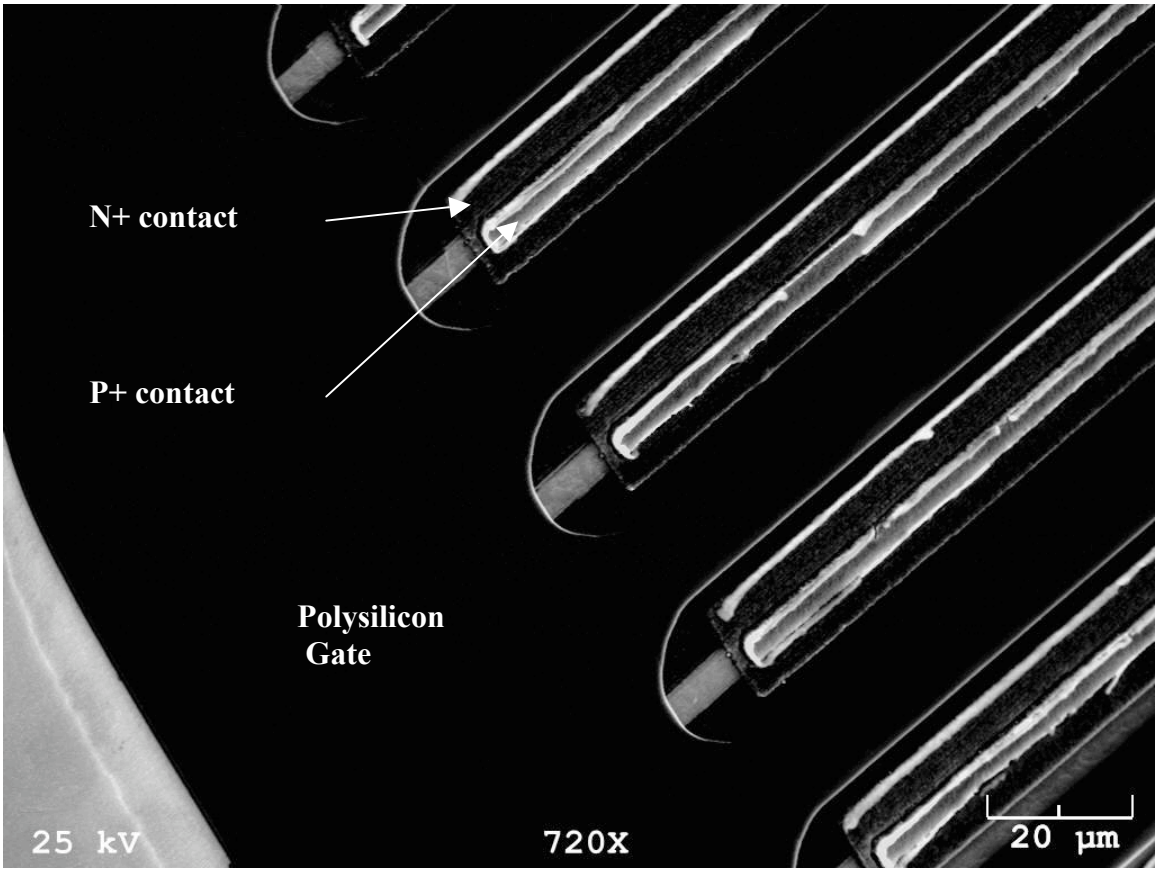


Figure 3.122 SEM picture of a device on sample 1 after the contact anneal.

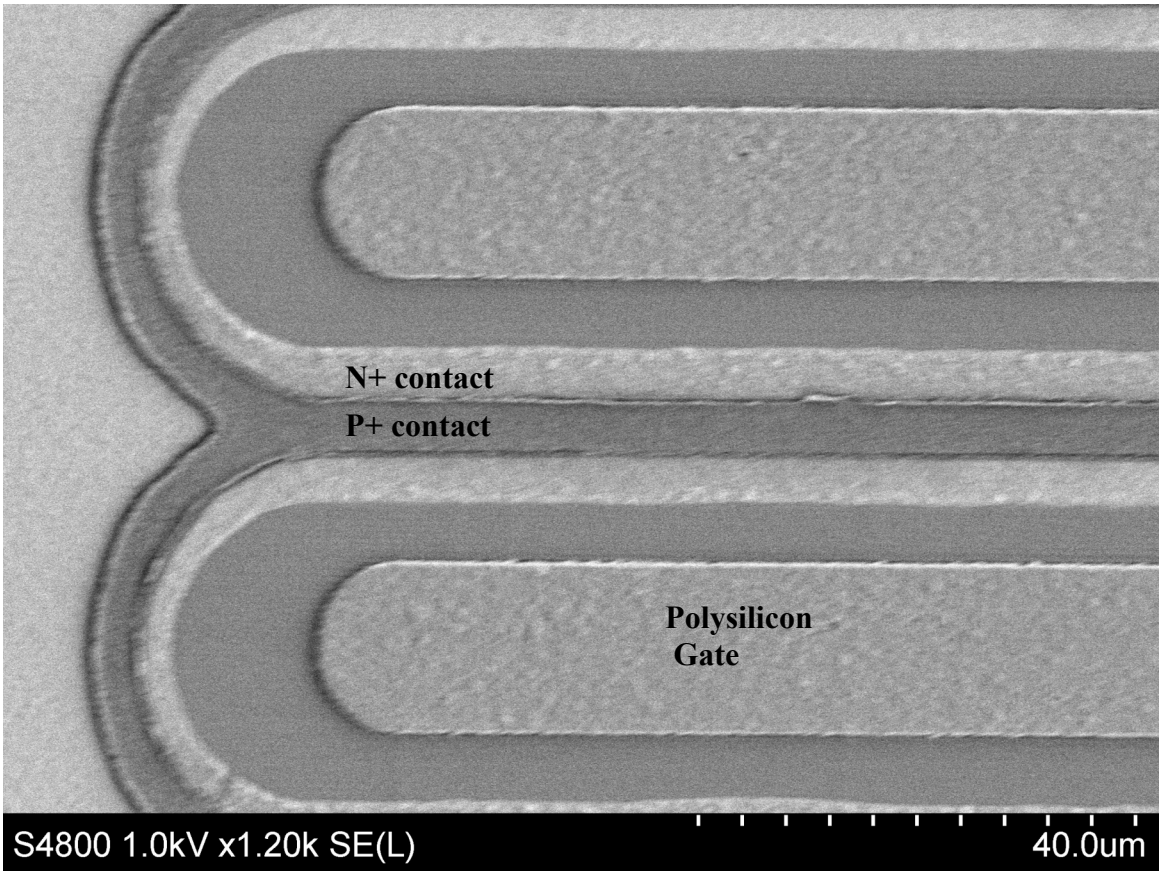


Figure 3.123 SEM picture of a device on sample 2 after the contact anneal.

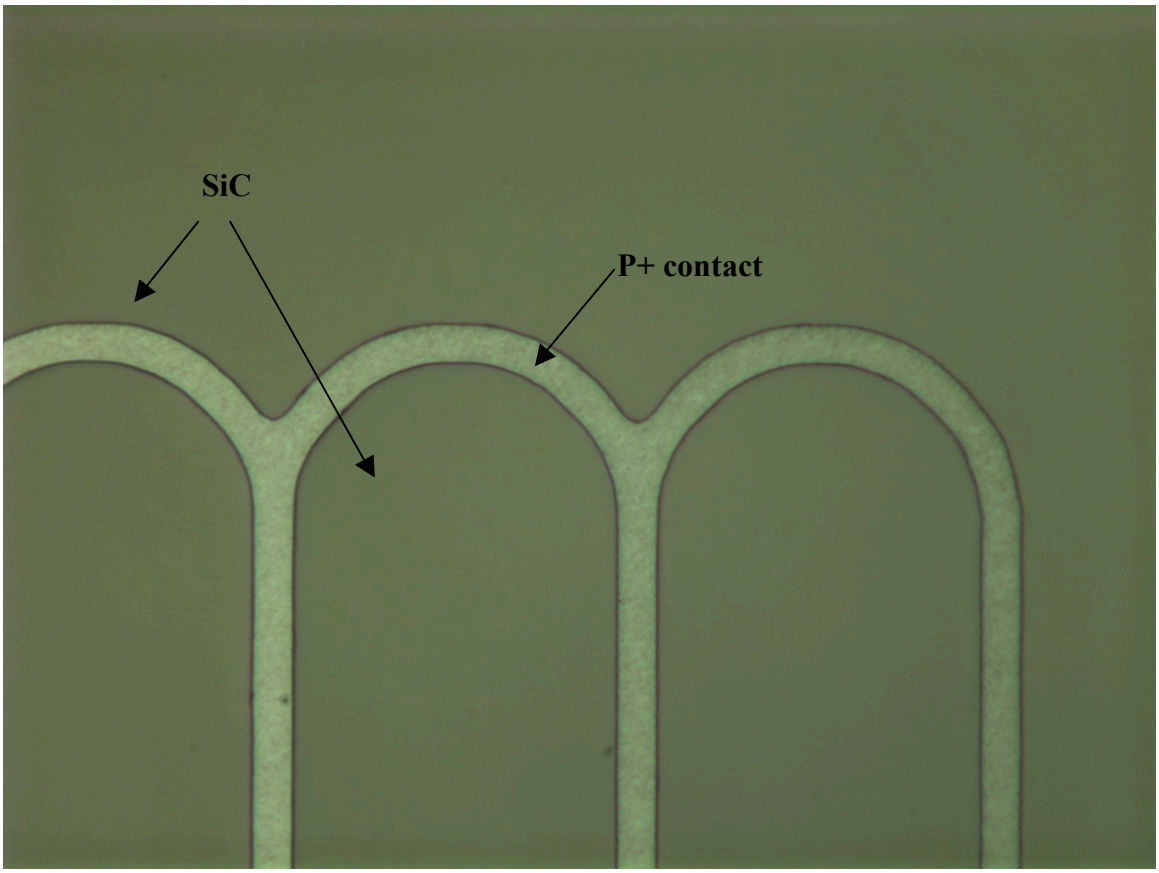


Figure 3.124 A device on sample 4 after the contact anneal. The gate and the n+ contact were deposited after the contact anneal.

3.2.3.10 Summary of Device Processing

Table 3.13 summarizes the processing steps of samples 1 to 6.

Top metal was not deposited on sample 4, since the n+ contact metals (Ti/Ni) was not annealed and they covered both the n+ source and the p+ base regions.

The processing of sample 5 discontinued after the p+ base contact formation and before the contact anneal. The processing of sample 6 discontinued after the NO anneal of the gate oxide.

Table 3.13 Summary of the Processing Steps of Samples 1 to 6

Sample	1	2	3	4	5	6
Starting Wafer	CB0517_03	BZ0688-3	HM0094-24	BZ0688-3	BZ0688-3	BZ0688-3
N- Epilayer Growth	Purdue	Cree	Cree	Cree	Cree	Cree
Substrate Removal	NovaSiC	NovaSiC	NovaSiC	NovaSiC	NovaSiC	NovaSiC
Final Step of Substrate Removal	Second CMP at NovaSiC (≈30 µm)	None	RIE at Purdue (≈35 µm)	None	None	None
Implant Anneal	Silane in Epigress	Silane in Epigress	Silane in Epigress	Graphite*, Ar Epigress	Graphite, Ar Epigress	Graphite, Ar Epigress
N+ RMS	17 nm	9.1 nm		0.2 nm		
P+ RMS	1.1 nm	1.7 nm				
P-well RMS	0.9 nm	0.6 nm				
Gate Oxide	Pyrogenic Thermal	Pyrogenic Thermal	Pyrogenic Thermal	Pyrogenic Thermal	Pyrogenic Thermal	Pyrogenic Thermal
NO Anneal	1175 ºC, 2 hours	None	1175 ºC, 1 hour	1175 ºC, 1 hour 10 min	1175 ºC, 1 hour 10 min	1175 ºC, 1 hour 10 min
Thickness	40 nm	115 nm	240 nm	45 nm	45 nm	45 nm
Characteristics	Leaky	Not Leaky	Not Leaky	No Gate Yet	No Gate Yet	No Gate Yet
Poly Gate Deposition	500 nm	500 nm	500 nm	None	None	None
Ohmic Contacts						
N+ Contact Metal	100 nm Ni	100 nm Ni	100 nm Ni	None	None	None
P+ Contact Metal	33 nm Ti/167 nm Al	33 nm Ti/167 nm Al	33 nm Ti/167 nm Al	33 nm Ti/167 nm Al	33 nm Ti/167 nm Al	Proce discont
Contact Anneal	800 ºC, 2 min	1000 ºC, 2 min	(Anneal Experiments)	20 ºC to 600 ºC in 75 sec	Processing discontinued	
Post-Anneal N+ Metal	None	None	N/A	50 nm Ti/100 nm Ni		

Table 4.4 (contd.) Summary of the Processing Steps of Samples 1 to 6

Gate Oxide Reprocessing	Thermal Oxide Stripped/240 nm LTO Deposited	Thermal Oxide Stripped/240 nm LTO Deposited	N/A	None		
Metal Gate Deposition	100 nm Al	100 nm Al	N/A	~50 nm Ti/ 100 nm Au		
Oxide Characteristics	Not Leaky	Not Leaky	N/A	Leaky		

* The top surface of sample 4 may not be fully covered by the graphite, but it was annealed with the top surface facing down.

3.2.4 Experimental Measurements

Samples 1 to 4 went through all the processing steps described in section 3.2.3 and were characterized using an HP4156 Semiconductor Parameter Analyzer. Due to the gate oxide leakage problem and the micromasking problem, which will be discussed in section 3.2.4.5, devices on sample 1 to sample 3 did not show IGBT characteristics. Devices on sample 4 showed gate-modulated drain currents. The current density was 27.3 A/cm^2 at a power dissipation of 300 W/cm^2. We will discuss the measurement results in detail in this section.

3.2.4.1 Characterization of Devices on Sample 1

The on-state characteristics of an IGBT on sample 1 before the contact anneal are shown in Fig. 3.125. At different gate voltages, the drain currents were measured while the drain voltage rose from 0 to 40 V. As shown in this figure, the drain current could not be modulated by the gate, and the device could not be turned off at V_G=0. Figure 3.126 shows the I-V between the gate electrode and source/base contact of an IGBT while the drain contact was floating. Ideally, the current should be zero. The non-zero current, which is responsible for the failure of gate modulation, means there must be a leakage path between the gate electrode and the source/base contact. To find the source of the problem, more measurements were conducted. Figure 3.127 shows the I-V between the gates of two adjacent capacitors. Since the current is almost zero, we can eliminate the possibility of surface leakage. Figure 3.128 and 3.129 are the I-V plots of capacitors over the n+ source region and the pwell region, respectively. As shown in these figures, the gate oxides over the source region and the pwell region are both leaky, though the leakage current of the capacitor over the n+ region is two orders of magnitude higher than that over the pwell region. As mentioned in section 3.2.3, the surface of the n+ region on sample 1 was unusually rough after the implant anneal (rms roughness = 17 nm). The gate oxide thickness was only about twice the rms roughness. This could cause the poor quality of the gate oxide.

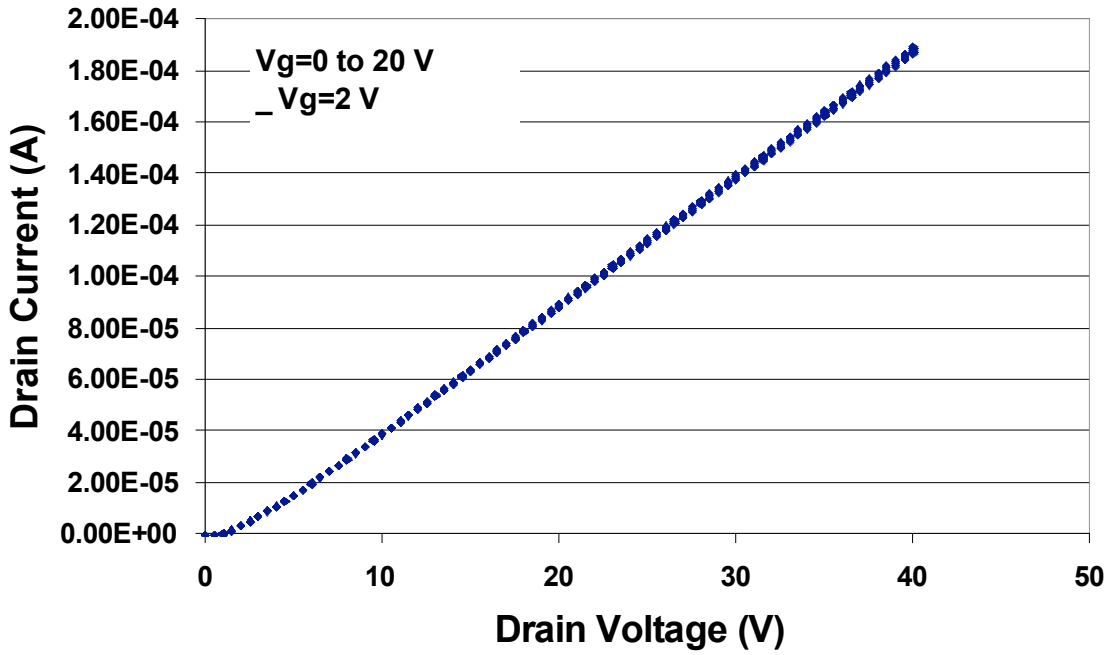


Figure 3.125 On-state characteristics of an IGBT on sample 1 before the contact anneal. All the Vg curves are on top of each other.

The contacts on sample 1 were annealed at 800°C for 2 minutes (the targeting temperatures was 1000 ºC, see details in section 3.2.3.9). We hoped that with better contacts, the drain current could be high enough to overshadow the gate leakage current. However, even though the drain current was increased after the contact anneal, so was the gate leakage current (see Figs. 3.130 and 3.131). The devices still did not behave like IGBTs.

The n contact was not ohmic after the contact anneal (see Fig. 3.132). The I-V characteristics of the p contact were basically linear (see Fig. 3.133).

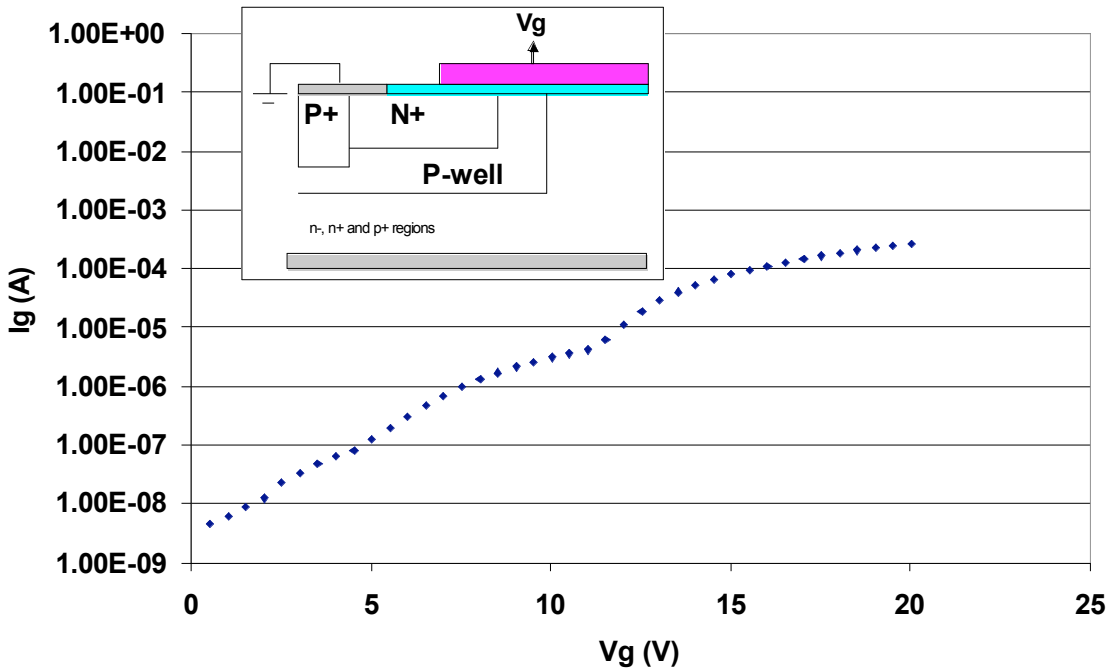


Figure 3.126 Ig-Vg of an IGBT on sample 1 while the drain contact is floating (before the contact anneal).

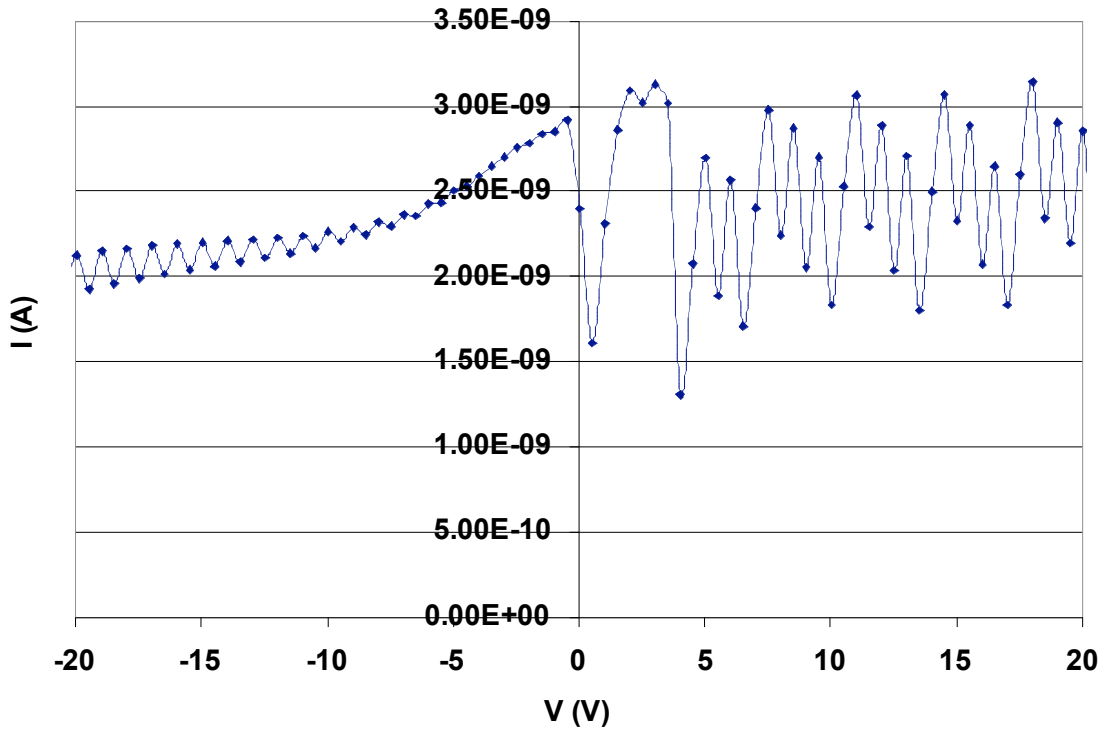


Figure 3.127 I-V between the gates of two adjacent capacitors.

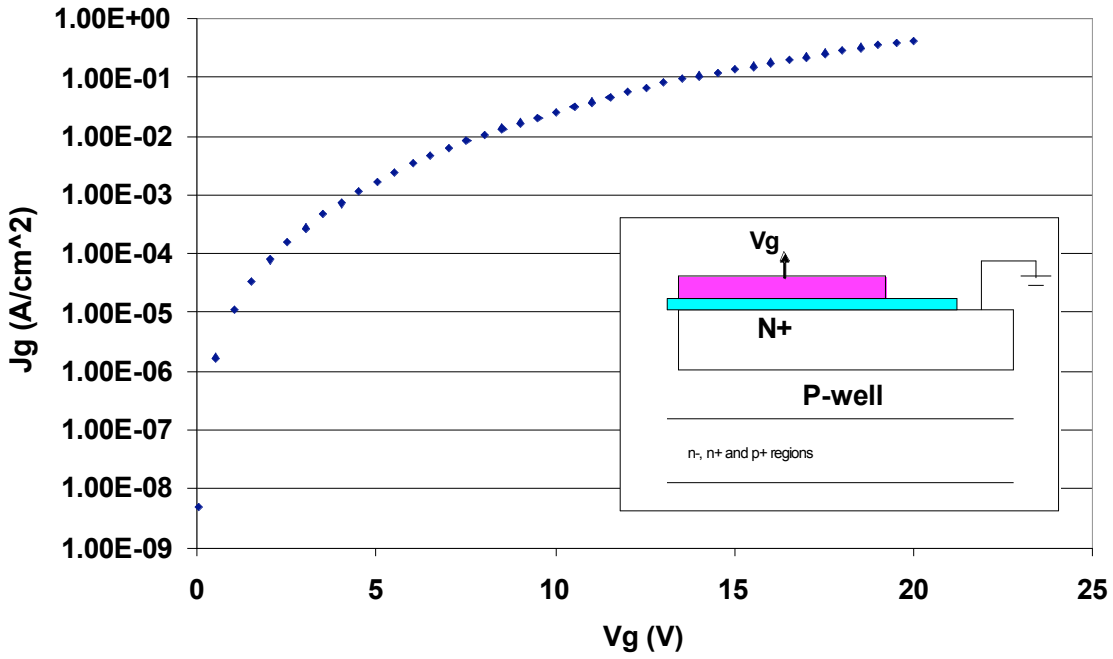


Figure 3.128 I-V of a capacitor over the n+ region on sample 1 before the contact anneal.

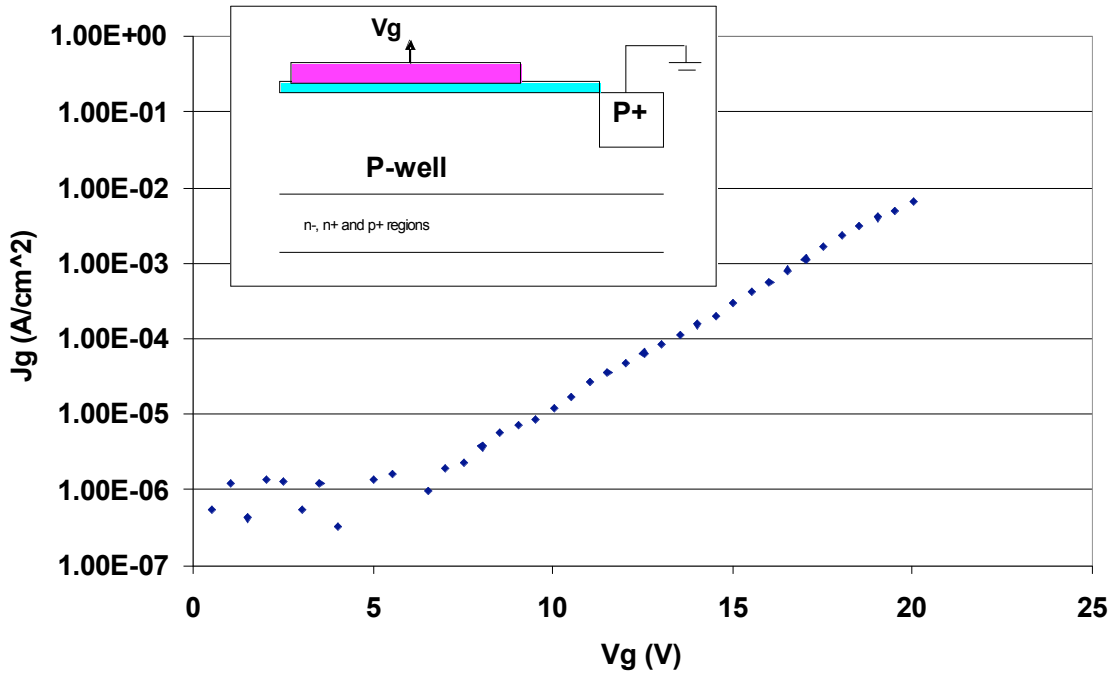


Figure 3.129 I-V of a capacitor over the pwell region on sample 1 before the contact anneal.

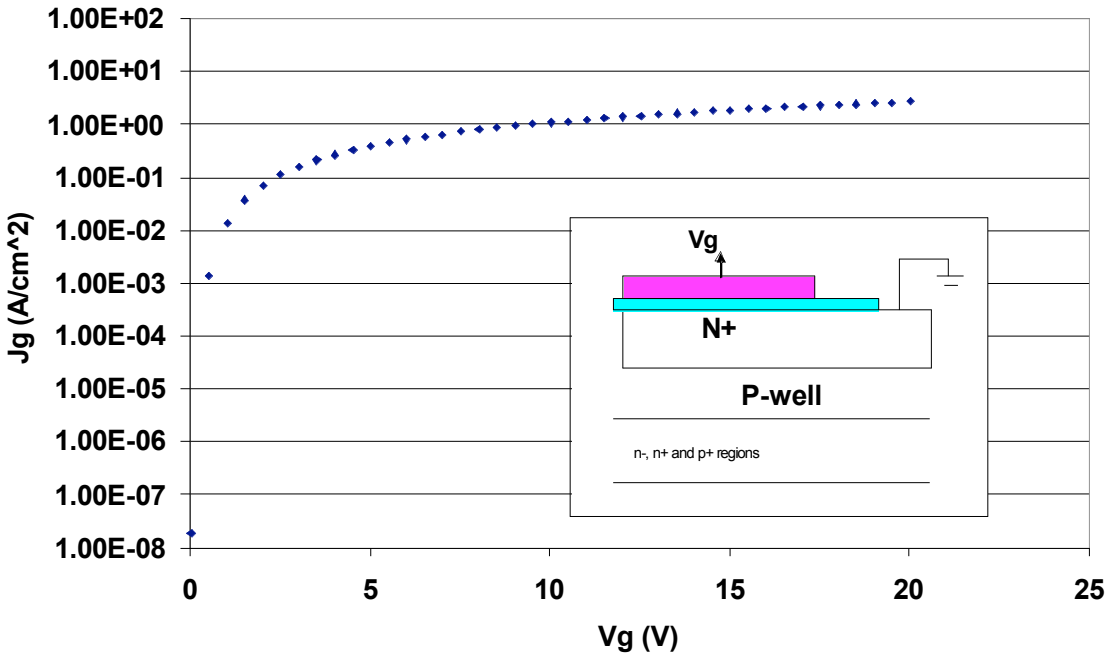


Figure 3.130 I-V of a capacitor over the n+ region on sample 1 after the contact anneal.

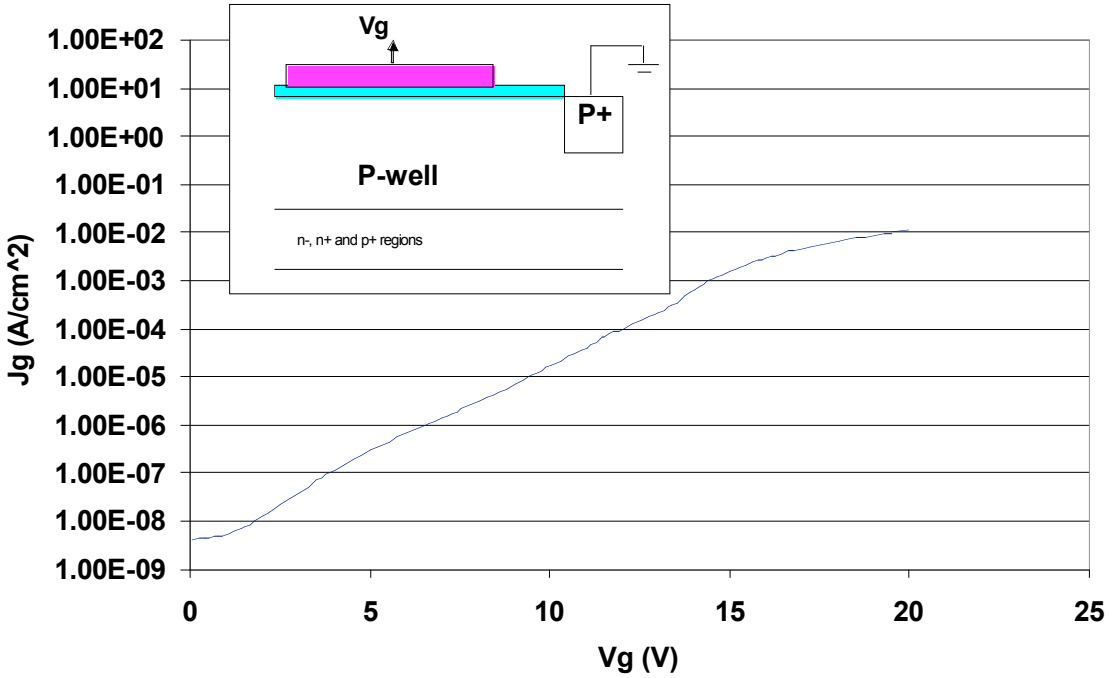


Figure 3.131 I-V of a capacitor over the pwell region on sample 1 after the contact anneal.

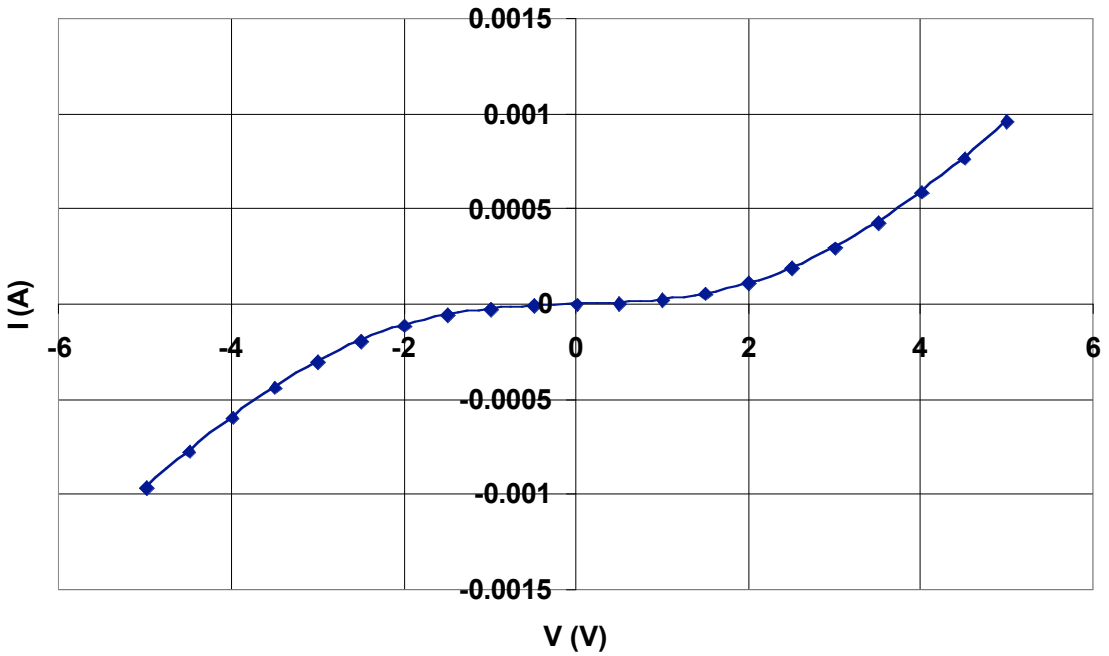


Figure 3.132 I-V characteristic of an n+ TLM on sample 1 after the first contact anneal.

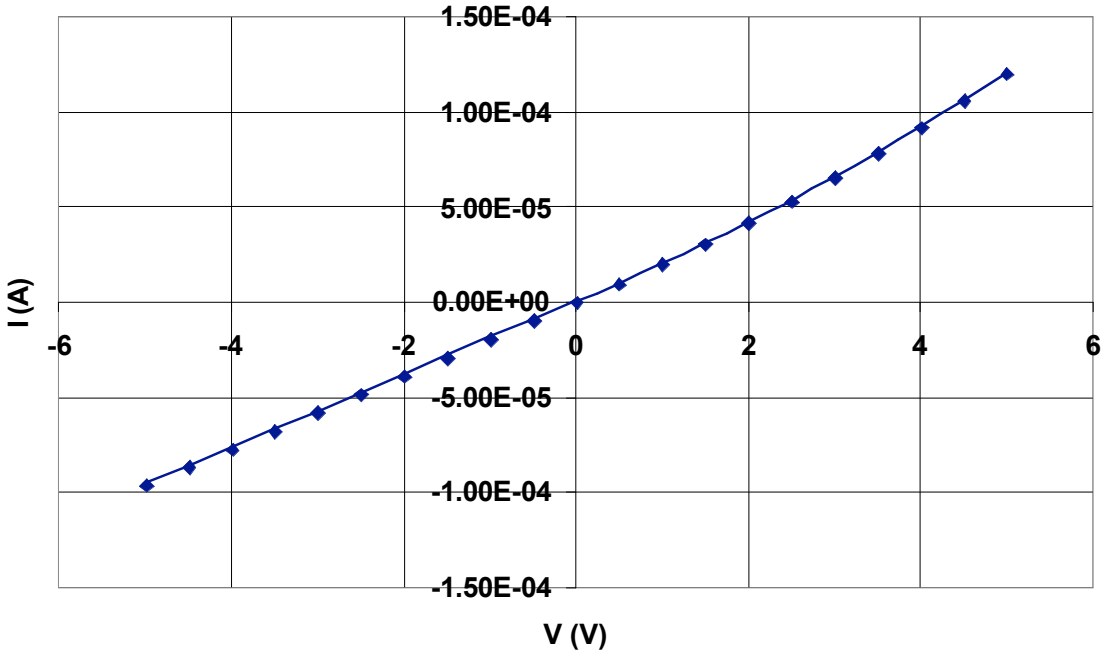


Figure 3.133 I-V characteristic of a p TLM on sample 1 after the first contact anneal.

To eliminate the oxide leakage, we decided to deposit LTO (low temperature oxide) on sample 1 to replace the thermal oxide. Before stripping the polysilicon gate and the thermal

oxide, we re-annealed the contacts on sample 1 in the Epigress VP508 SiC CVD reactor at 1000ºC for 2 minutes. Both p contacts and n contacts were ohmic after the second anneal due to the higher anneal temperature, with contact resistivities of $1x10^{-3}$ Ω cm^2 and $5.5x10^{-7}$ Ω cm^2, respectively (see Figs. 3.134 - 3.137).

As shown in Fig. 3.138, the gate was not leaky with LTO as the gate dielectric (up to V_g of 100 V). But the devices on sample 1 still didn't show IGBT characteristics (see figure 5.15). Since we had tried almost everything we could think of to make sample 1 work, we decided to move on to sample 2 which was more promising to have working devices.

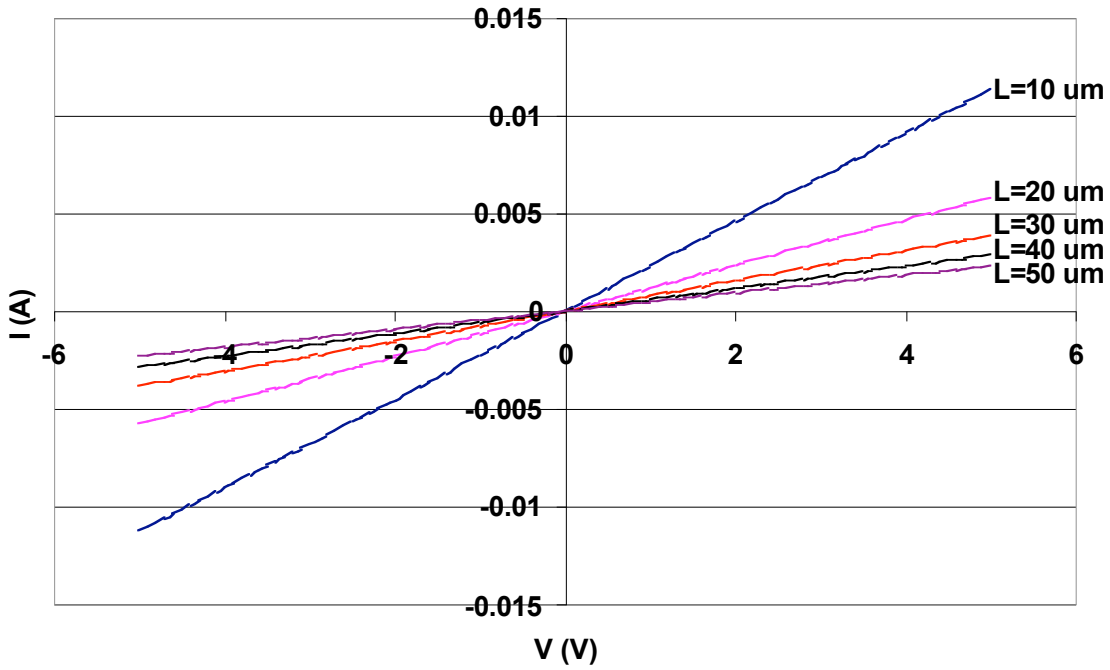


Figure 3.134 I-V characteristics of an n+ TLM on sample 1 after the second contact anneal.

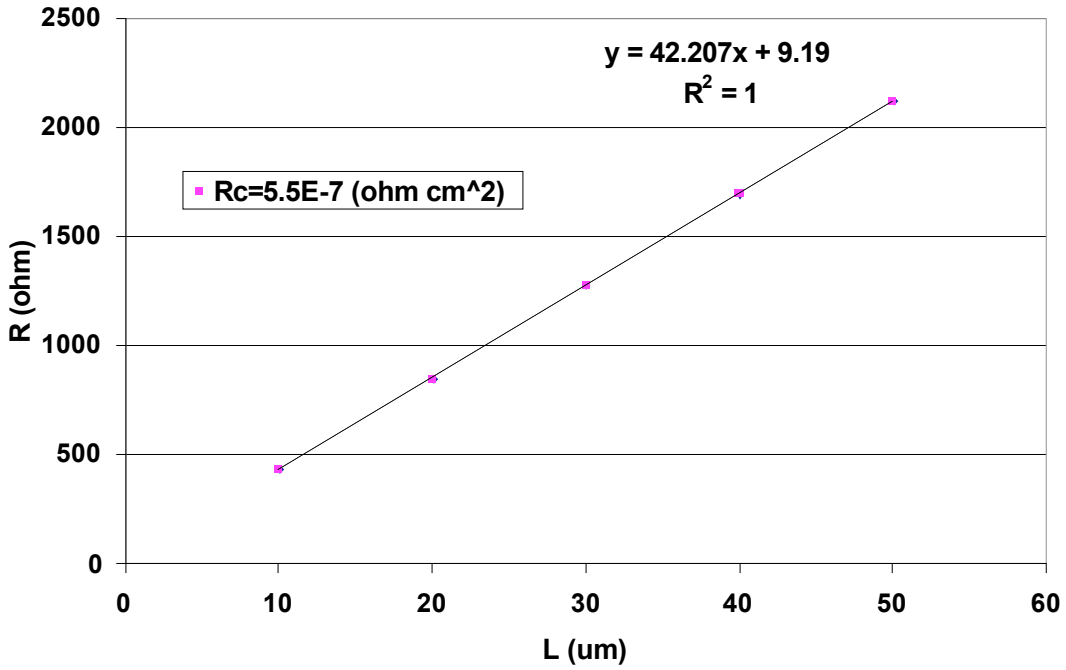


Figure 3.135 Contact resistivity of the n+ TLM on sample 1 after the second contact anneal.

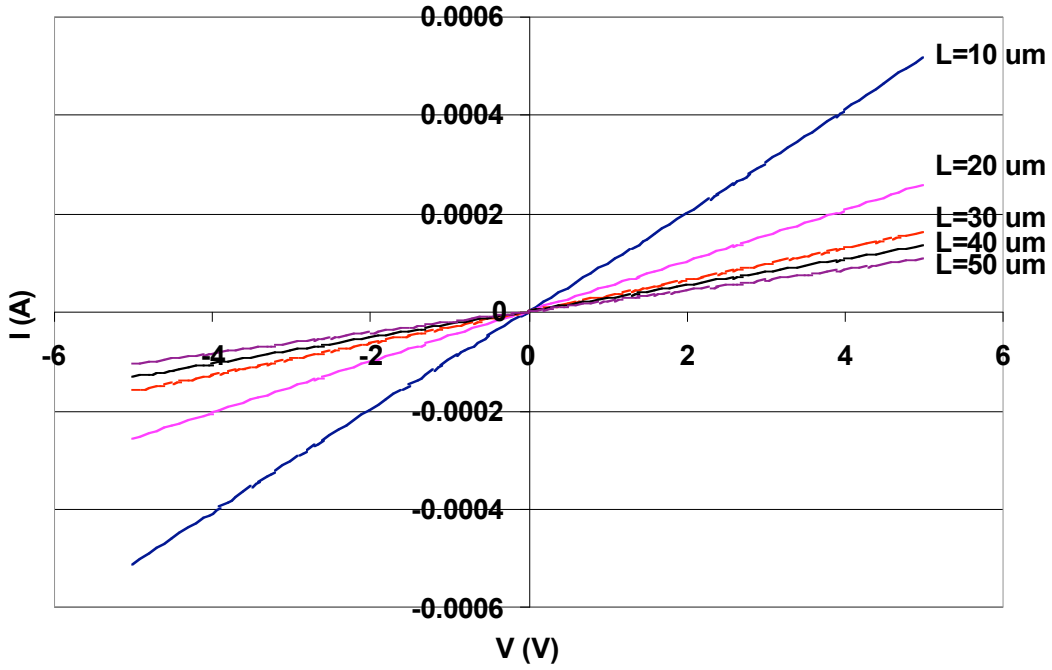


Figure 3.136 I-V characteristics of a p TLM on sample 1 after the second contact anneal.

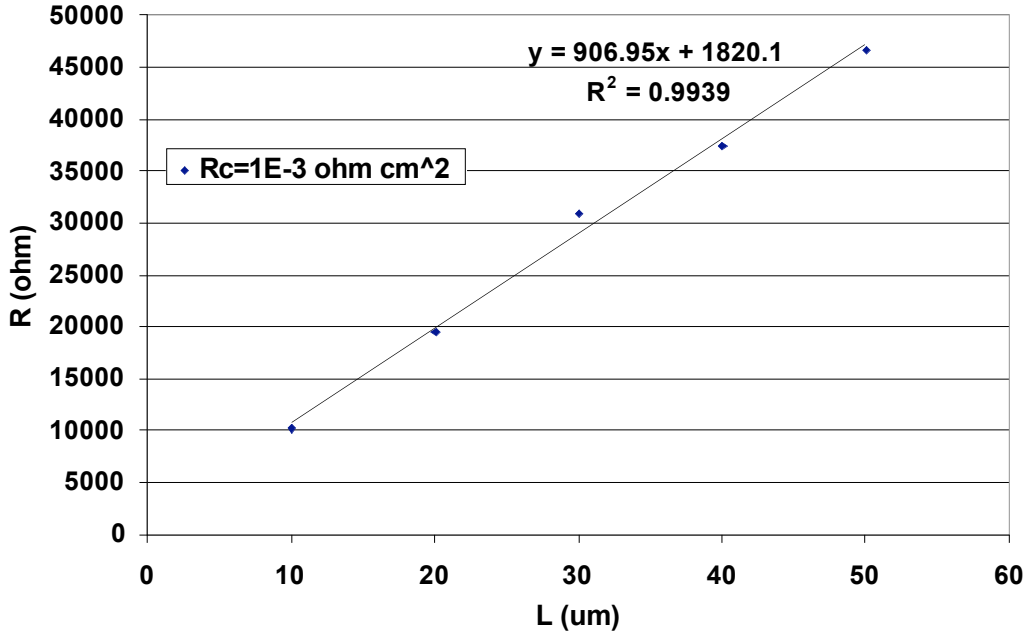


Figure 3.137 Contact resistivity of the p TLM on sample 1 after the second contact anneal.

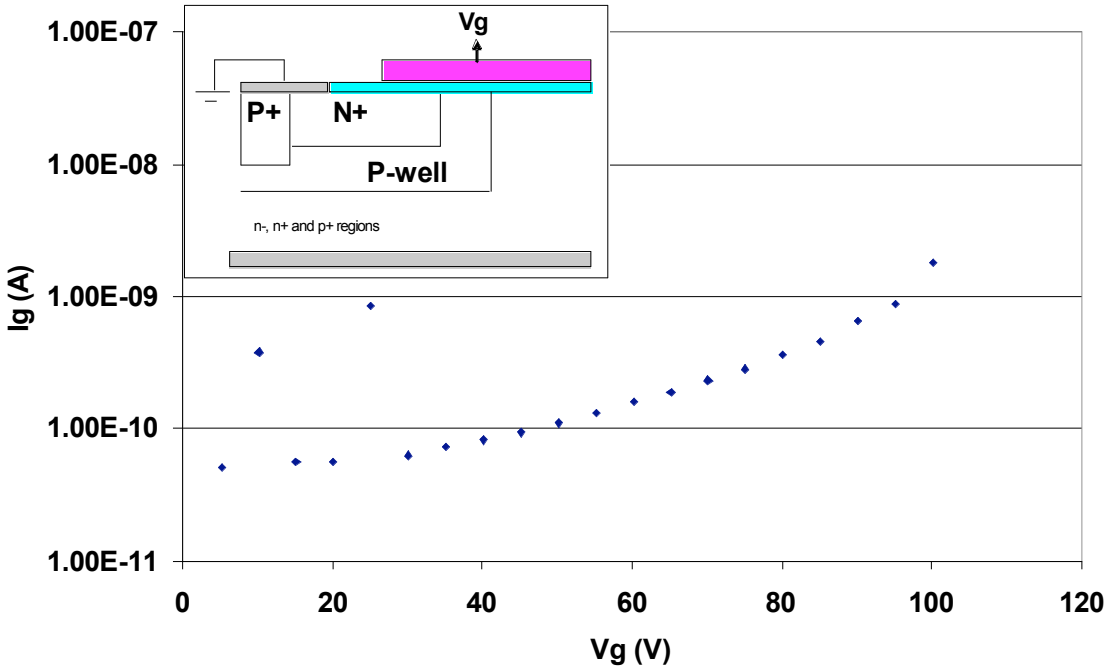


Figure 3.138 Ig-Vg of an IGBT on sample 1 after 24 nm LTO deposition.

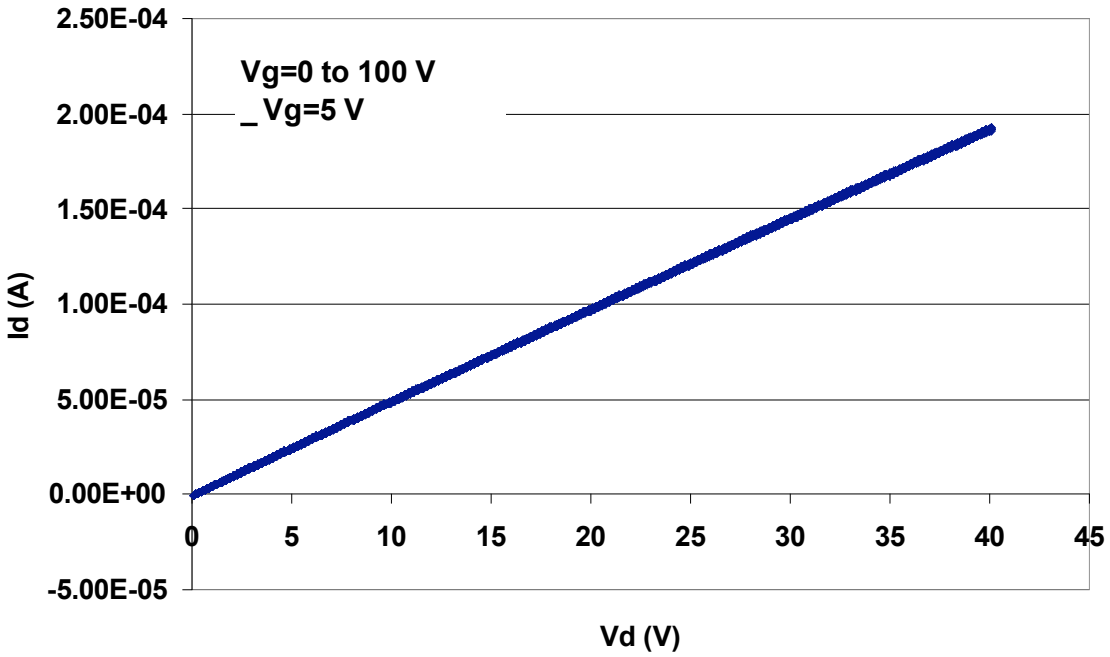


Figure 3.139 On-state characteristics of an IGBT on sample 1 with 240 nm LTO. All 20 Vg curves are on top of each other.

3.2.4.2 Characterization of the Devices on Sample 2

The rms surface roughness of the n+ region on sample 2 was 9.1 nm. To prevent the oxide leakage problem, we decided to grow a thicker gate oxide on sample 2. The thickness of the thermal oxide was 110 nm. NO anneal was not performed.

Figure 3.140 shows the on-state characteristics of an IGBT on sample 2 before the contact anneal. The gate leakage current was less than $4x10^{-8}$ A up to Vg=40 V (see Fig. 3.141). The drain current can be modulated by the gate. However, the current density was five orders of magnitude lower than expected. In addition, the 3 V offset was not observed in the plot. The MOSFET-like characteristics of the device will be discussed in detail in section 3.2.4.4. The threshold voltage of the device was around 26 V. There are three factors that could contribute to the high threshold voltage. First, the gate oxide thickness is 110 nm, which doubles the thickness we usually use for DMOS devices (~50 nm). Secondly, NO anneal was not performed after the gate oxidation. This would result in a higher interface charge density. Thirdly, the profile of the n-type counter-doped implant in the pwell was designed for devices with 50 nm gate oxide. All the counter-doped implant, which could lower the threshold voltage, would be consumed when the thermal oxide is as thick as 110 nm.

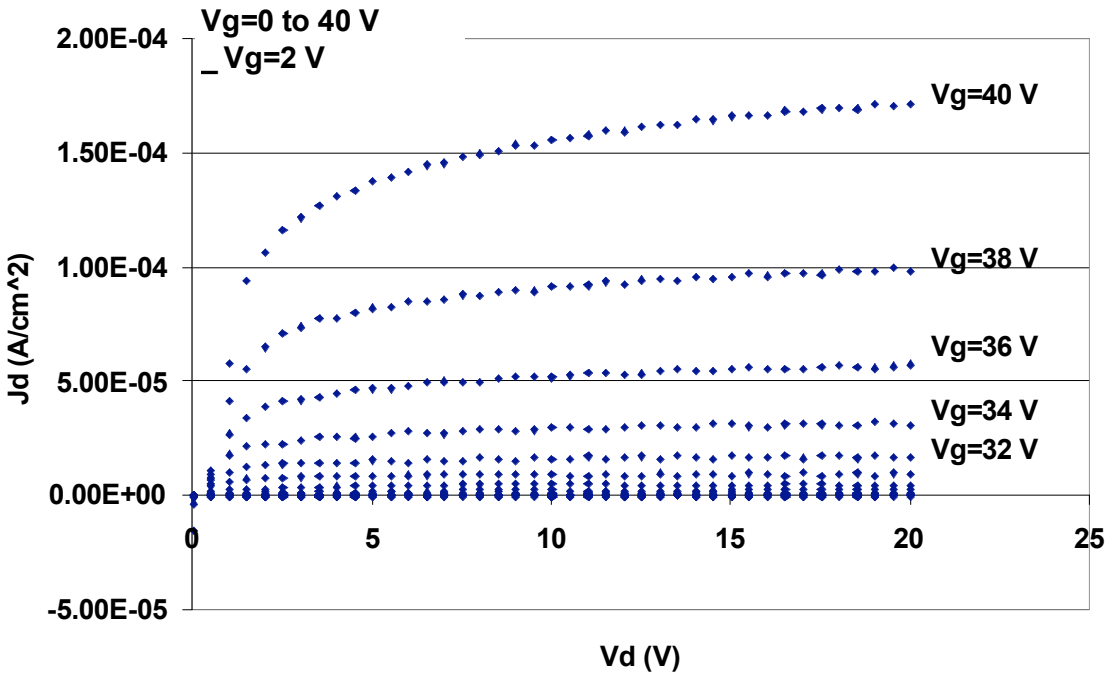


Figure 3.140 On-state characteristics of an IGBT on sample 2 before contact anneal.

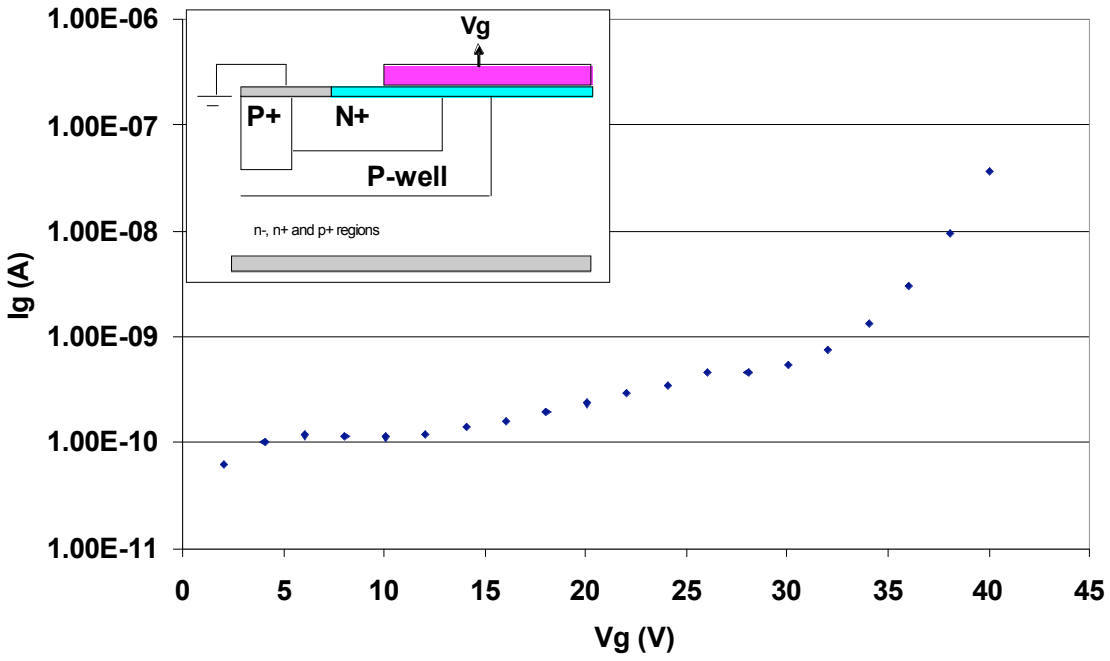


Figure 3.141 Ig-Vg of the IGBT on sample 2 before contact anneal.

The contacts of sample 2 were annealed in the Epigress VP508 SiC CVD reactor at 1000°C. From our experience of fabricating p-channel SiC DMOS IGBTs, the drain current should increase drastically after the contact anneal [22]. But unfortunately, the gate oxide on sample 2 became very leaky after the contact anneal, as shown in Figs. 3.142 – 3.144. Figure 3.145 shows the I-V characteristics of an IGBT on sample 2 after the contact anneal. The IGBT could not be turned on. The drain currents at low drain voltages were negative. When Vd=0, both the source and the drain contacts were grounded. So the negative drain current at Vd=0 could only come from the gate. This is consistent with the oxide leakage current detected in the capacitor over the n- region (see Fig. 3.144).

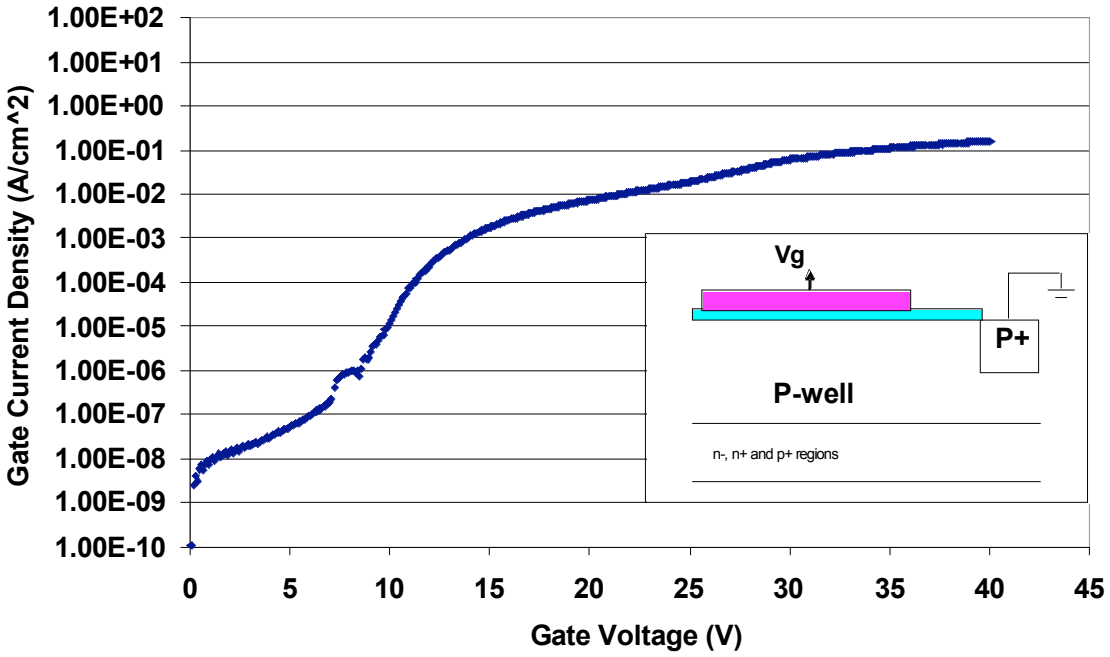


Figure 3.142 I-V of a capacitor over the pwell region on sample 2 after the contact anneal.

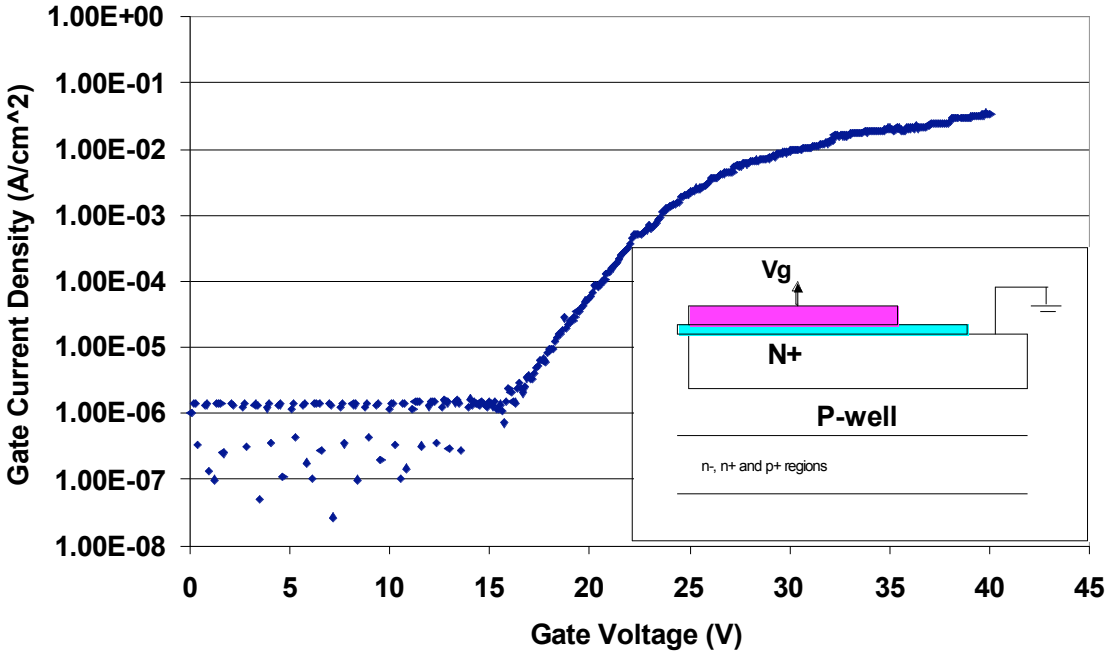


Figure 3.143 I-V of a capacitor over the n+ region on sample 2 after the contact anneal.

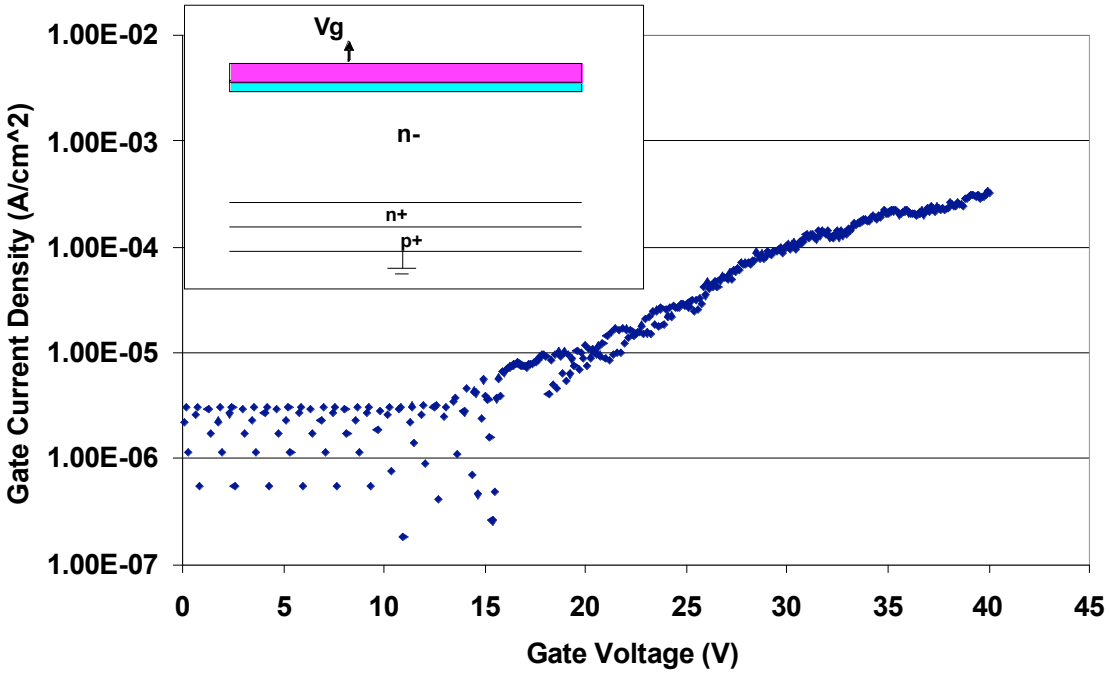


Figure 3.144 I-V of a capacitor over the n- region on sample 2 after the contact anneal.

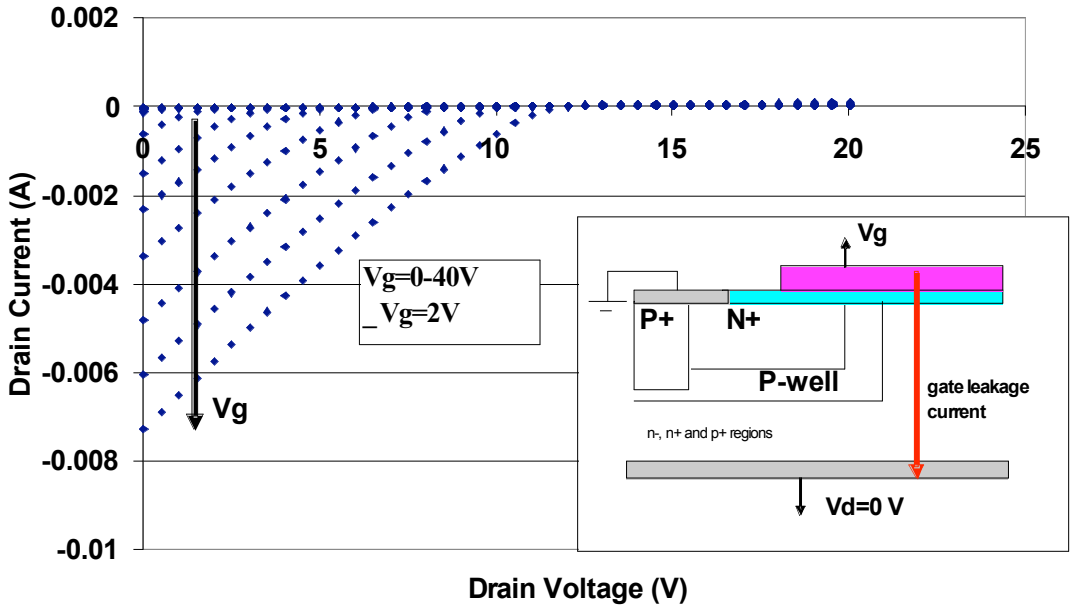


Figure 3.145 Id-Vd of an IGBT on sample 2 after the contact anneal. When Vd=0, both the source and the drain contacts were grounded. So the negative drain current at Vd=0 could only come from the gate.

The contacts on sample 2 were ohmic after the contact anneal. The contact resistivities were $4x10^{-4}$ ohm cm^2 and $4.9x10^{-2}$ ohm cm^2 for n contact and p contact, respectively (see Figs. 3.146 to 3.149).

Sample 2 was re-annealed in the contact annealer at 800ºC for 4 minutes (the targeting temperatures was 1000 ºC). The p contact resistivity was decreased to $1.3x10^{-2}$ ohm cm^2 (see Figs. 3.150 and 3.151). The n contacts were not improved.

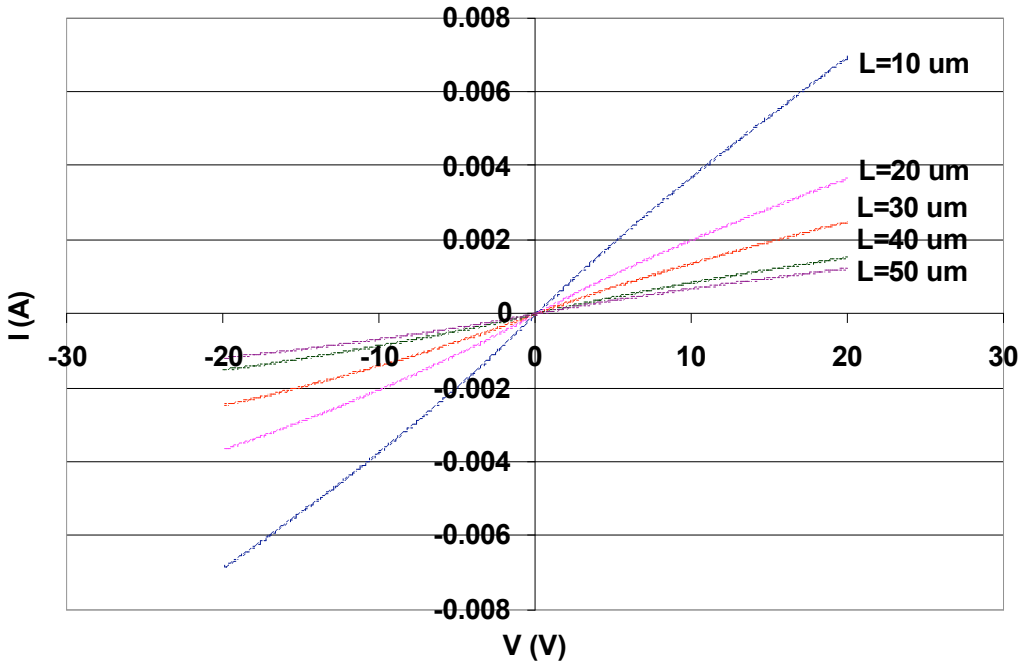


Figure 3.146 I-V characteristics of an N+ TLM on sample 2 after the first contact anneal.

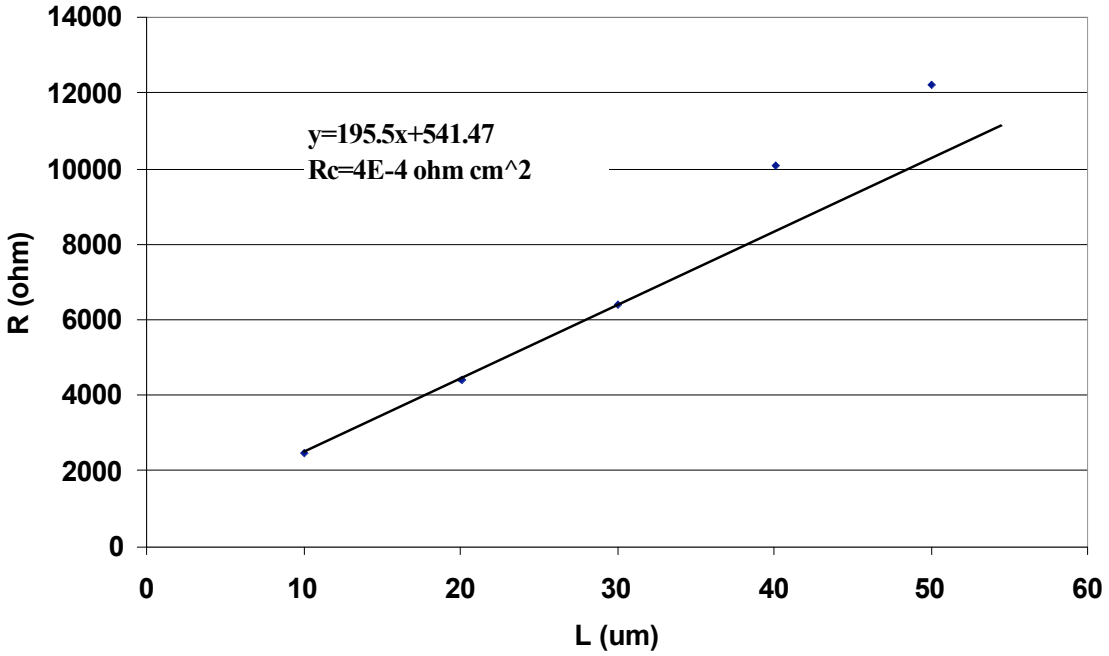


Figure 3.147 Contact resistivity of the N+ TLM on sample 2 after the first contact anneal.

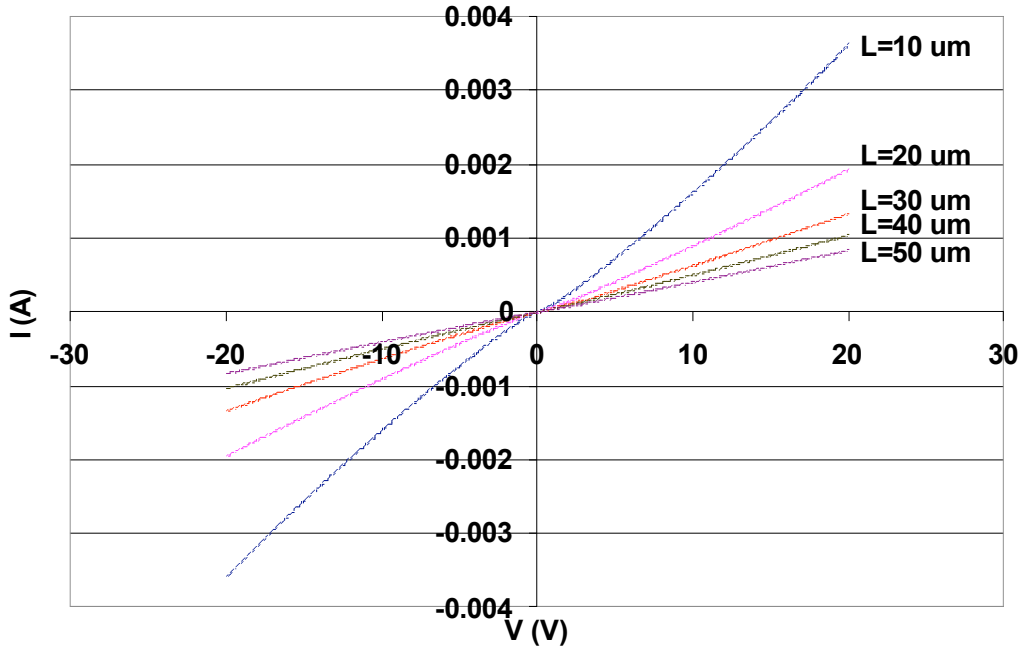


Figure 3.148 I-V characteristics of a P+ TLM on sample 2 after the first contact anneal.

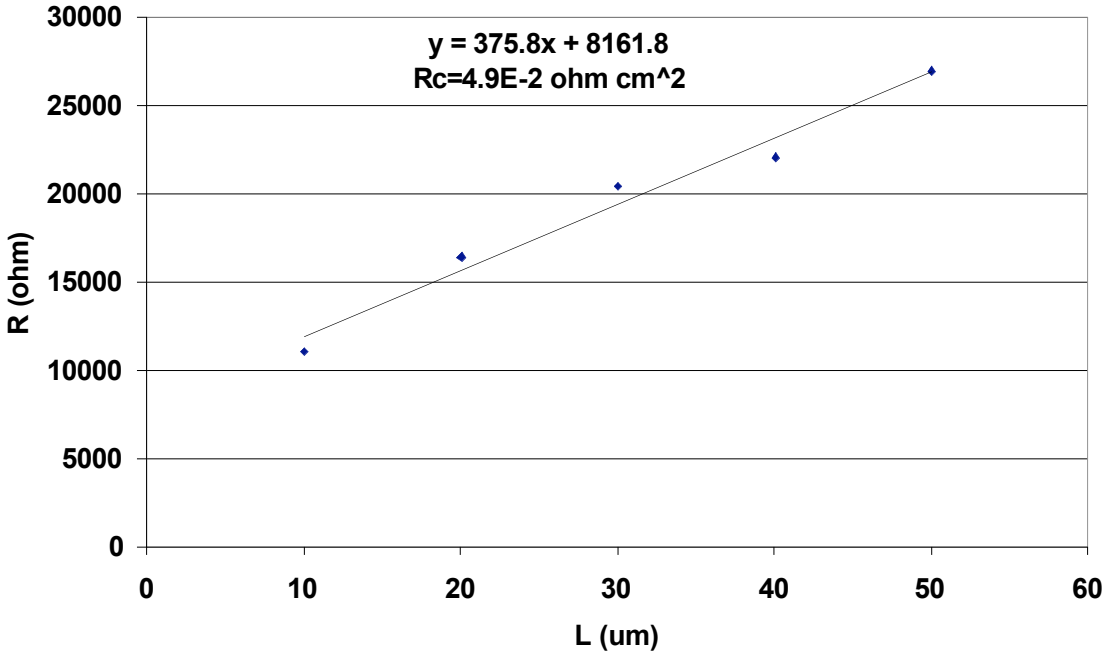


Figure 3.149 Contact resistivity of the P+ TLM on sample 2 after the first contact anneal.

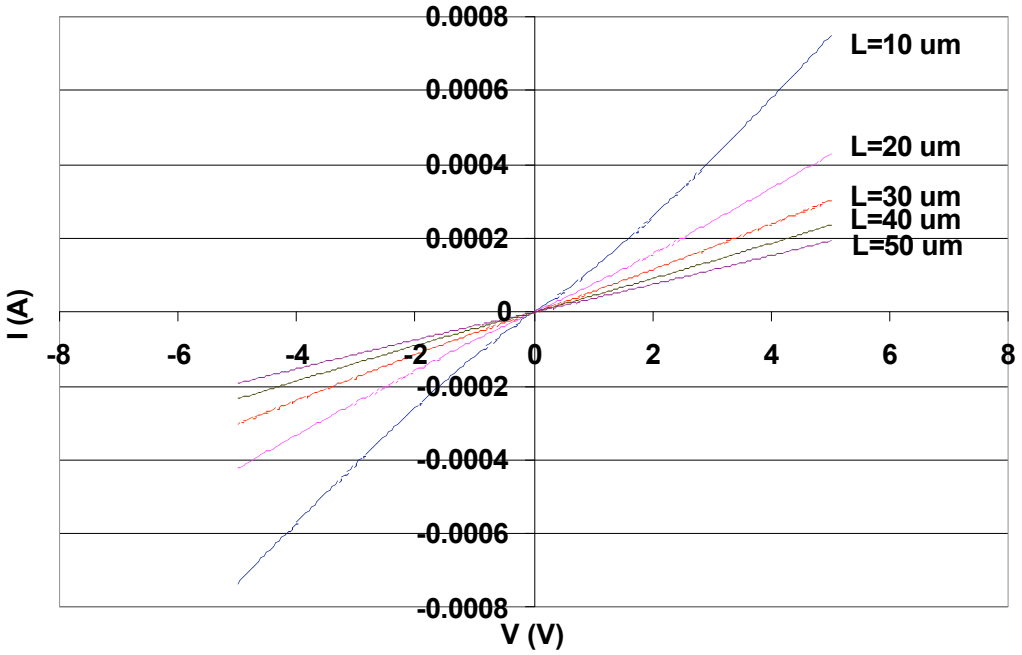


Figure 3.150 I-V characteristics of a p TLM on sample 2 after the second contact anneal.

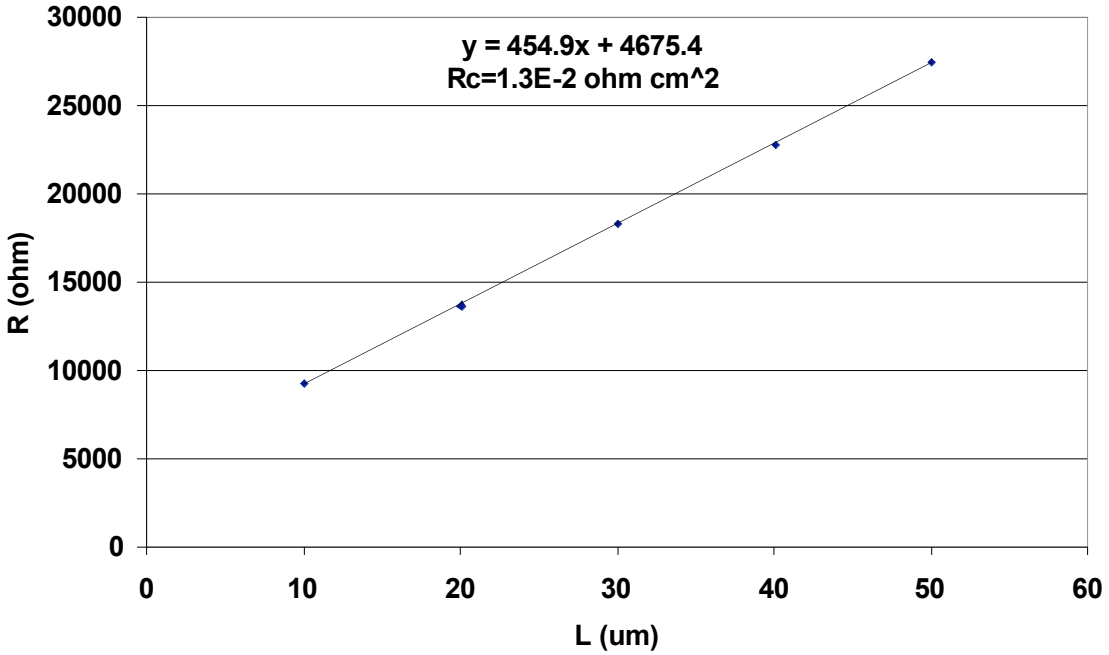


Figure 3.151 Contact resistivity of the p TLM on sample 2 after the second contact anneal.

After stripping the polysilicon gate and the gate oxide, sample 2 was sent to GE for the LTO deposition. 240 nm LTO was deposited. The LTOs over the n+, pwell and n- regions were not leaky (up to Vg of 100 V), as shown in Figs. 3.152 to 3.154.

Figure 3.155 shows the on-state characteristics of an IGBT on sample 2 after the LTO deposition. The drain current can be modulated, though the current density is still about four orders of magnitude lower than expected. The device was normally on. In addition, at low drain voltages, the device behaved like a MOSFET as shown in Fig. 3.156. This phenomenon will be discussed in section 3.2.4.4 in detail. Sample 2 was also measured at higher temperatures. Figure 3.157 shows the on-state characteristics of an IGBT on sample 2 at 300ºC. The drain current density approximately doubles that measured at room temperature.

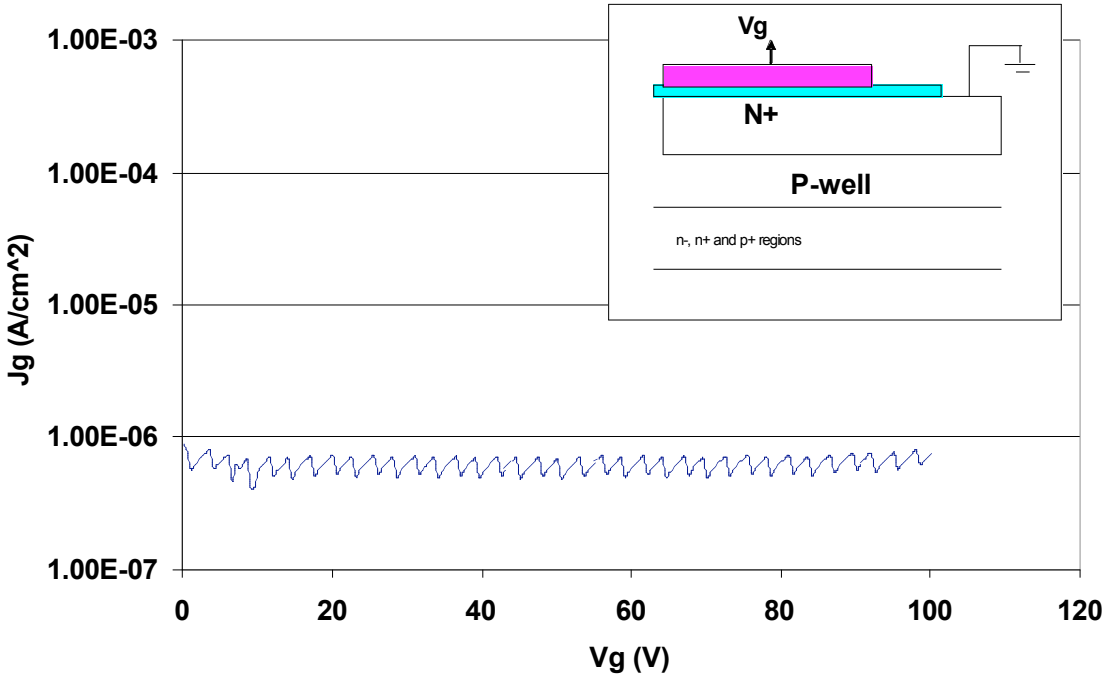


Figure 3.152 I-V of a capacitor over the n+ region on sample 2 with LTO as the gate dielectric.

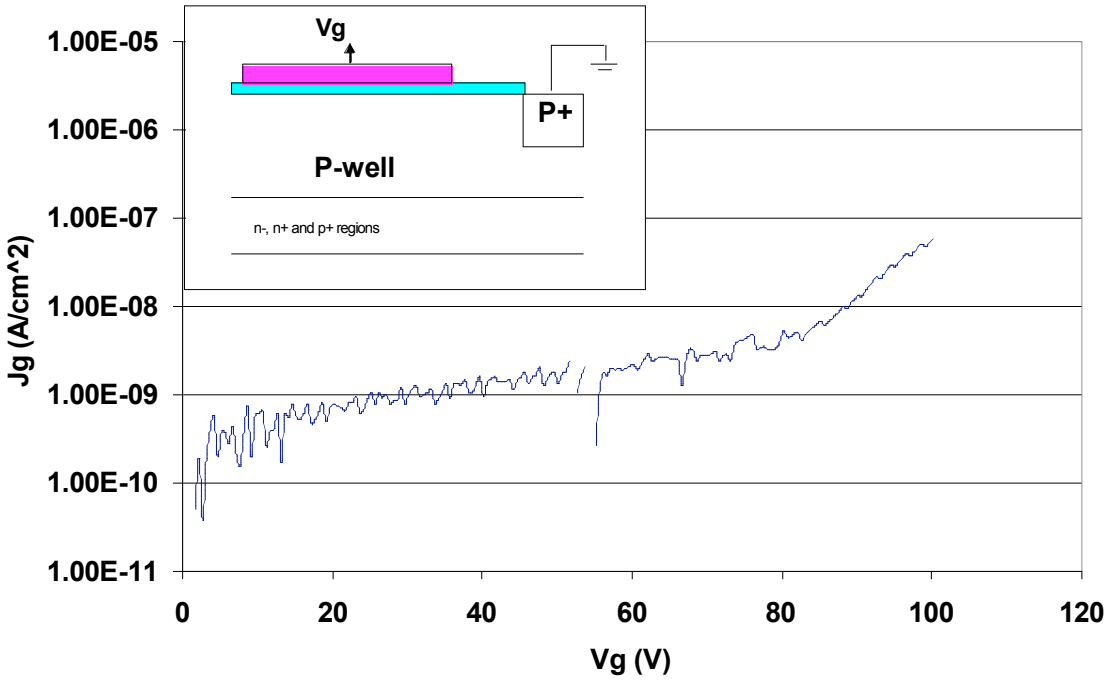


Figure 3.153 I-V of a capacitor over the pwell region on sample 2 with LTO as the gate dielectric.

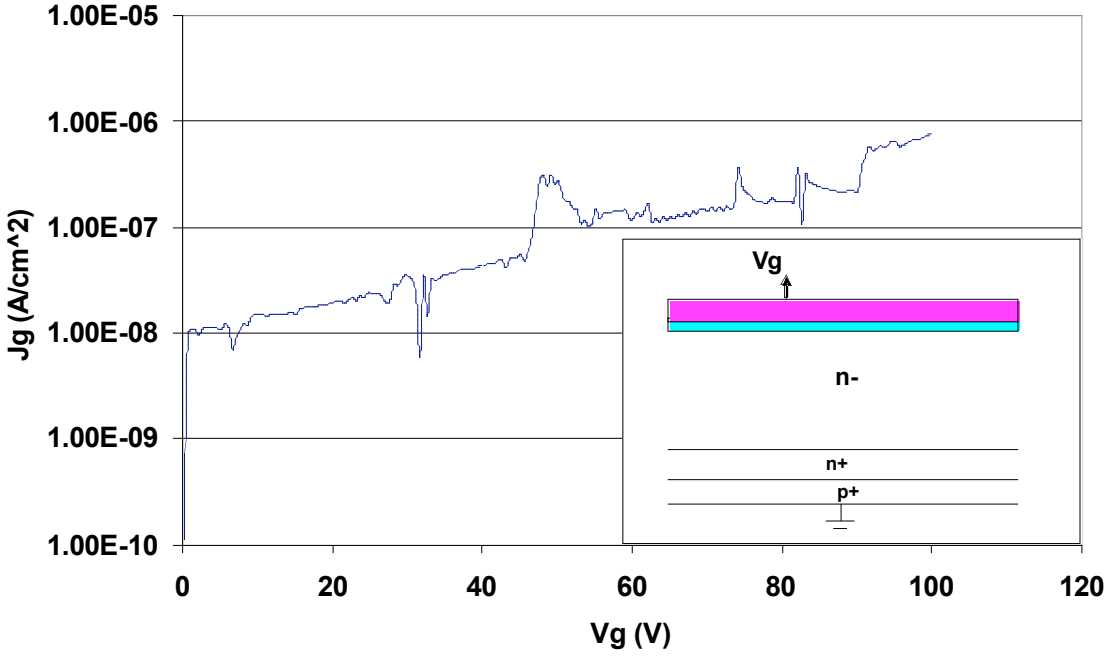


Figure 3.154 I-V of a capacitor over the n- region on sample 2 with LTO as the gate dielectric.

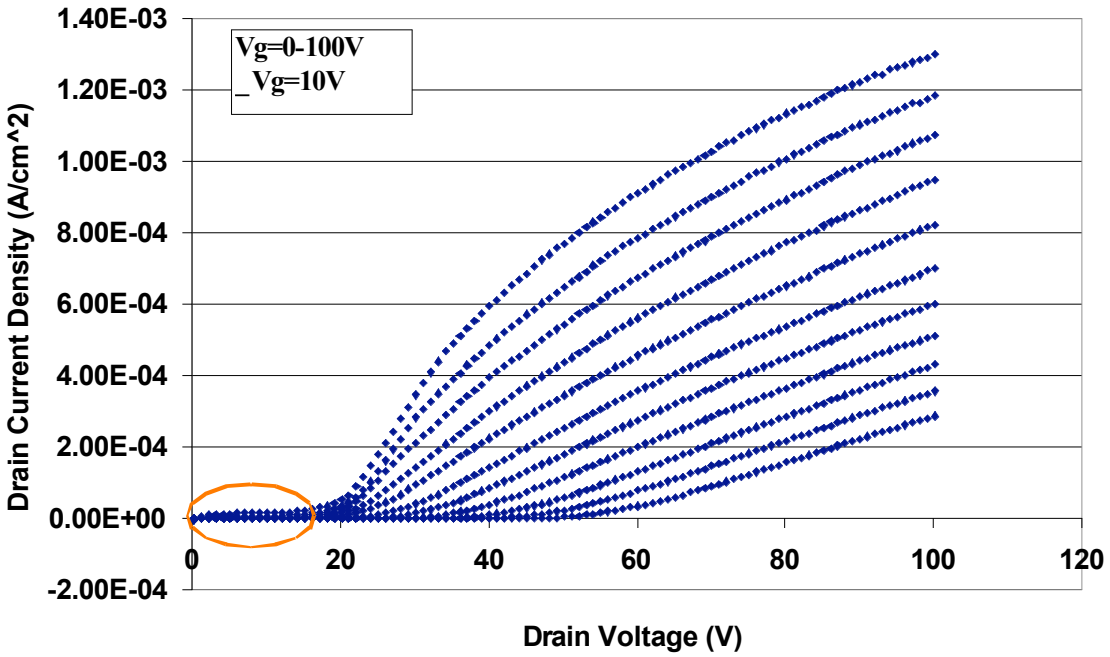


Figure 3.155 On-state characteristics of an IGBT on sample 2 with 240nm LTO as the gate dielectric (room temperature).

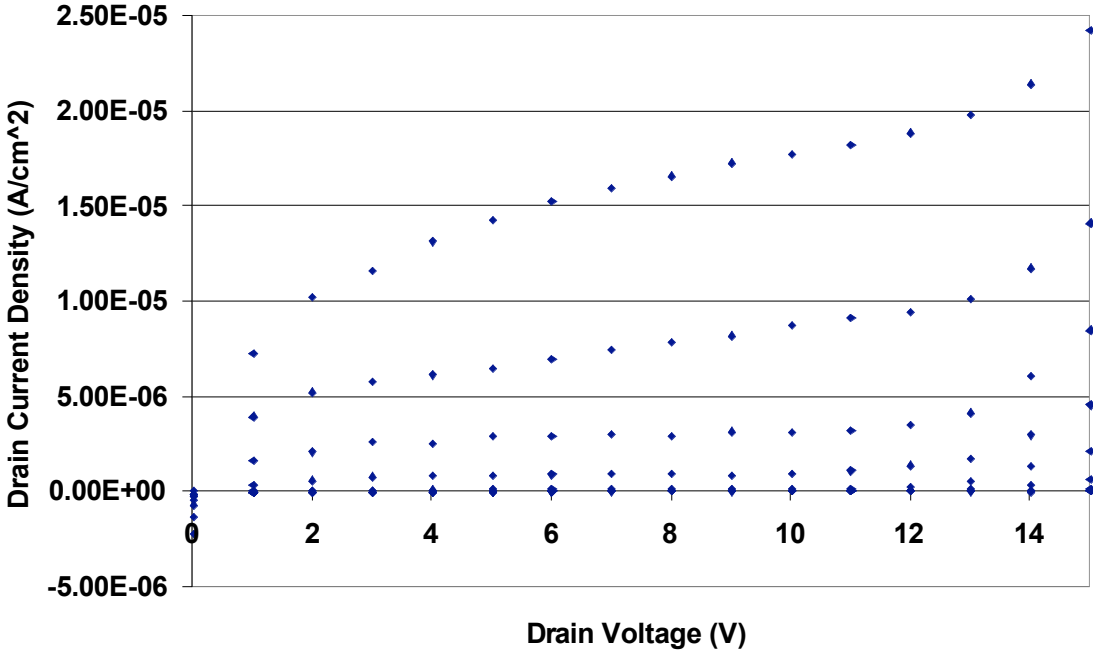


Figure 3.156 On-state characteristics of the IGBT on sample 2 with 240nm LTO at low drain voltages (a blowup of the circled area in Fig. 3.155).

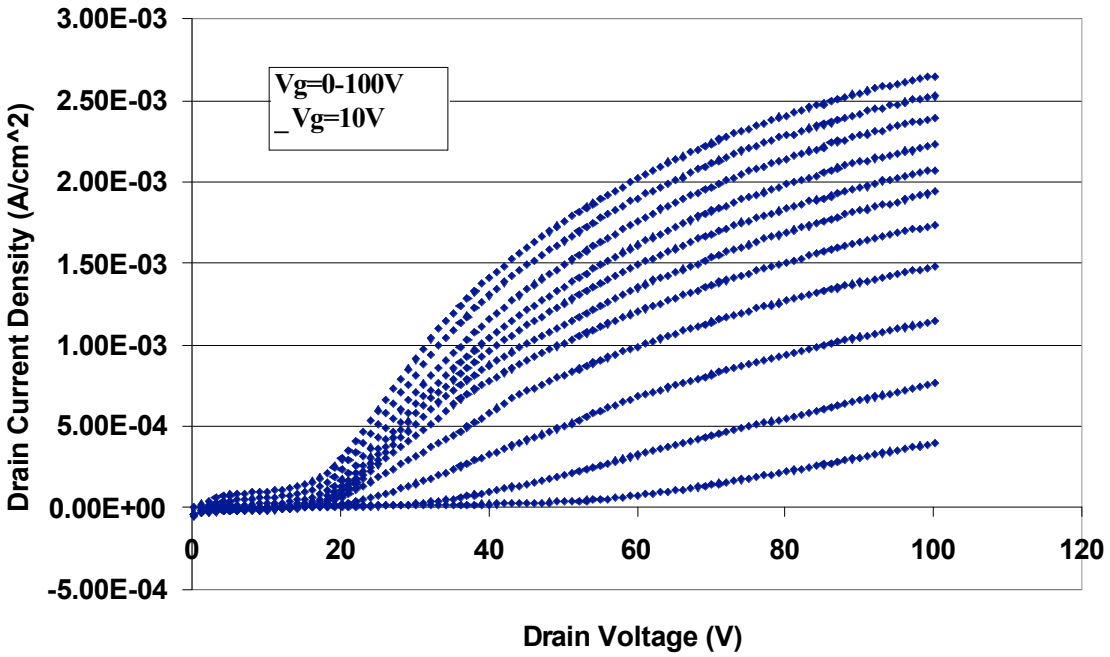


Figure 3.157 On-state characteristics of an IGBT on sample 2 with 240nm LTO as the gate dielectric (T=300ºC).

3.2.4.3 Contact Anneal Test Runs

In order to find the suitable contact annealing temperature, sample 3 was cut into small pieces, three of which were annealed in the contact annealer at 650 ºC, 700 ºC and 750 ºC, respectively (the targeting temperatures were 850 ºC, 900 ºC and 950 ºC, see details in section 3.2.9) . The annealing time was 2 minutes for all the pieces. The gate oxide on sample 3 was thermally grown with a thickness of 240 nm. NO anneal was performed after the gate oxidation at 1175 ºC for 1 hour.

3.2.4.3.1 650 ºC anneal

After the contact annealing at 650 ºC, the oxides over the pwell region and the n+ region were not leaky up to Vg=100 V (see Figs. 3.158 and 3.159). The capacitor over the n- region had a lot higher leakage current. At Vg=100 V, the leakage current density was about $5x10^{-5}$ A/cm^2 (see Fig. 3.160).

The p contact was not ohmic and the n contact was not conducting, as shown in Figs. 3.161 and 3.162.

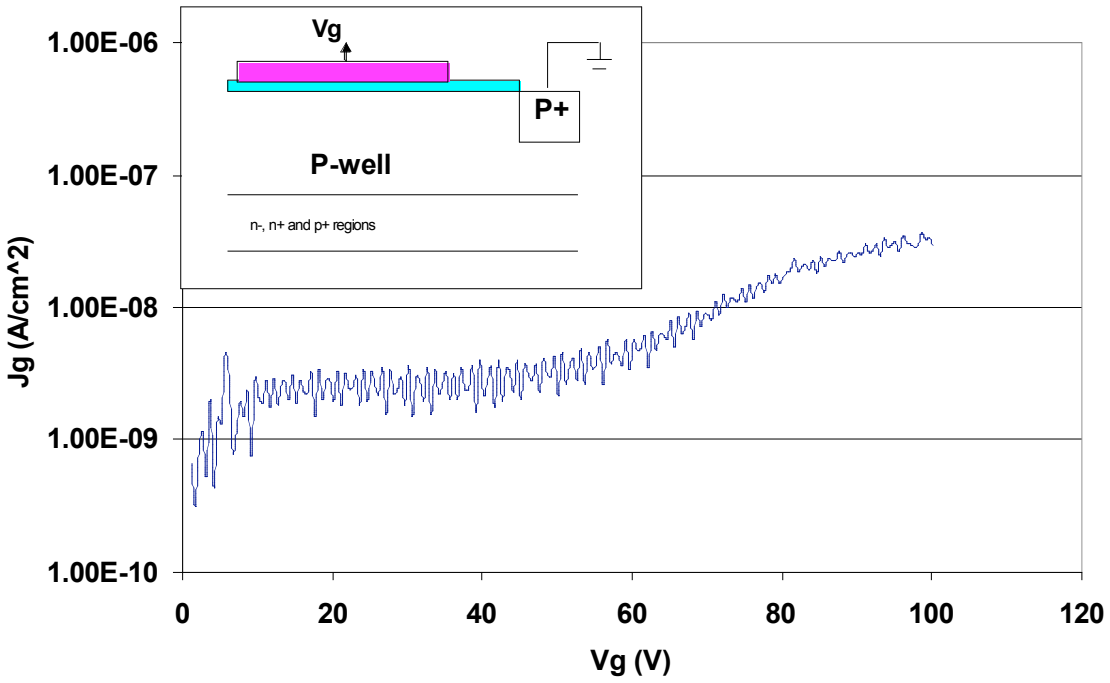


Figure 3.158 I-V of a capacitor over the pwell region after 2-minute 650 ºC contact anneal (240 nm thermal gate oxide).

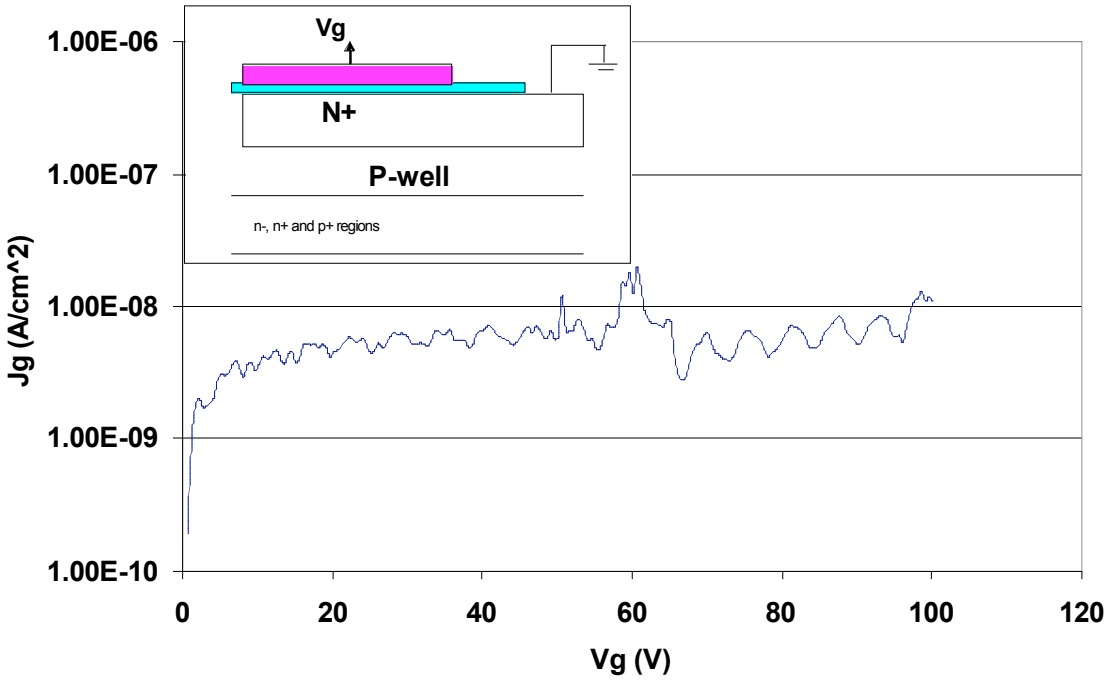


Figure 3.159 I-V of a capacitor over the n+ region after 2-minute 650 ºC contact anneal (240 nm thermal gate oxide).

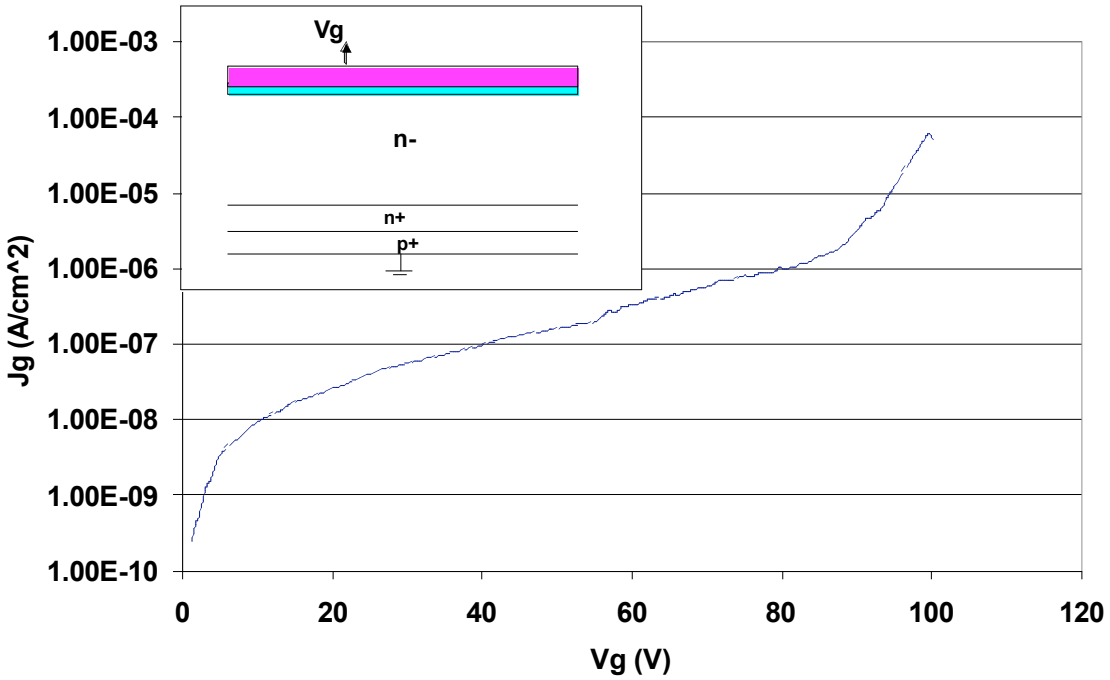


Figure 3.160 I-V of a capacitor over the n- region after 2-minute 650 ºC contact anneal (240 nm thermal gate oxide).

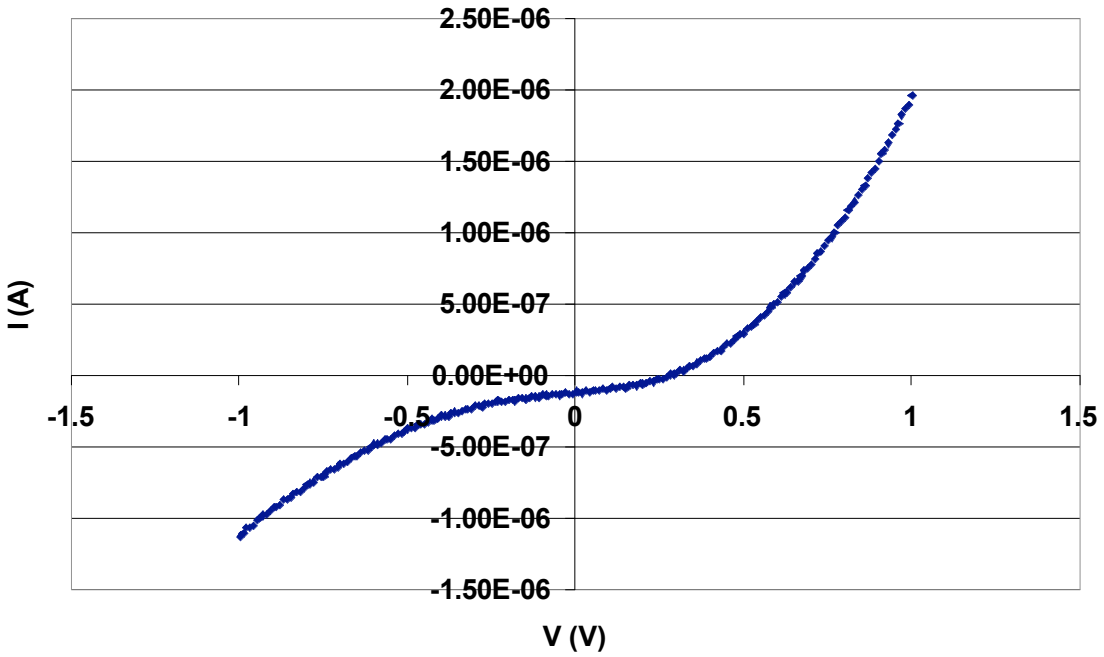


Figure 3.161 I-V of a p TLM after the 2-minute 650 ºC contact anneal.

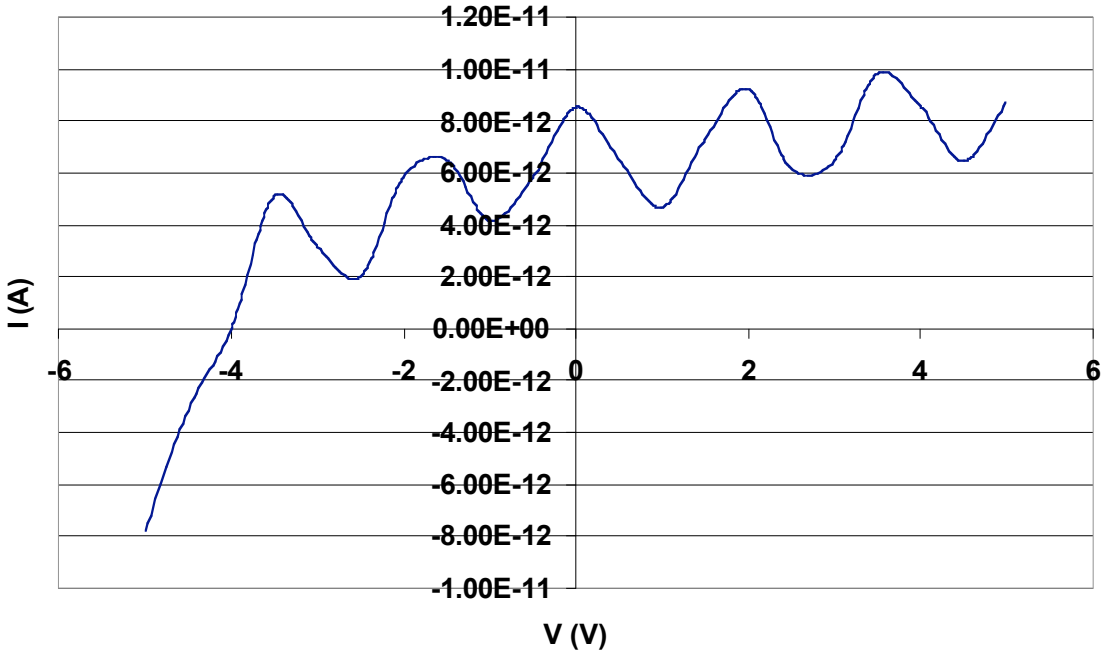


Figure 3.162 I-V of an n+ TLM after the 2-minute 650 ºC contact anneal.

3.2.4.3.2 700 ºC anneal

After the contact annealing at 700 ºC, the oxide over the n+ region was not leaky as shown in Fig. 3.163. However, the oxide over the pwell region had considerable amount of leakage current flowing through it, as shown in Fig. 3.164. The oxide over the n- region broke down at a V_G of about 87 V (see Fig. 3.165).

The p contacts were ohmic after the anneal (see Fig. 3.166). The contact resistivity was around $4.3 \times 10^{-5}\ \Omega\ cm^2$ or $4.8 \times 10^{-4}\ \Omega\ cm^2$ based on the linear fits of the R vs L plot (Fig. 3.167). The n contacts still did not conduct any current after the anneal as shown in Fig. 3.168.

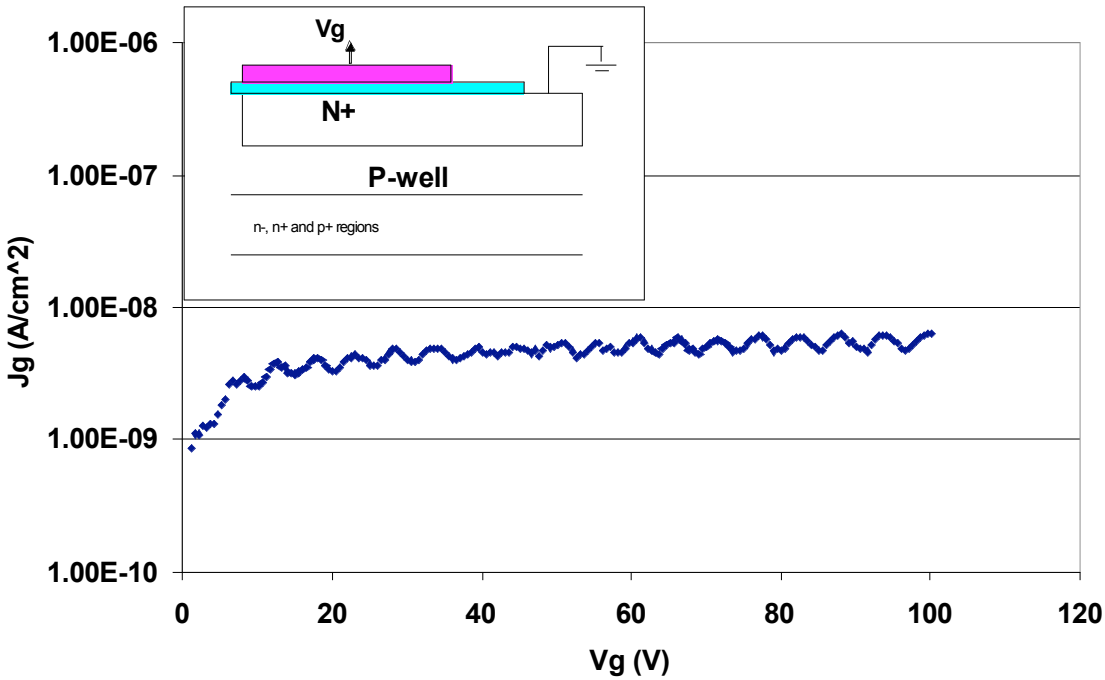


Figure 3.163 I-V of a capacitor over the n+ region after 2-minute 700 ºC contact anneal (240 nm thermal gate oxide).

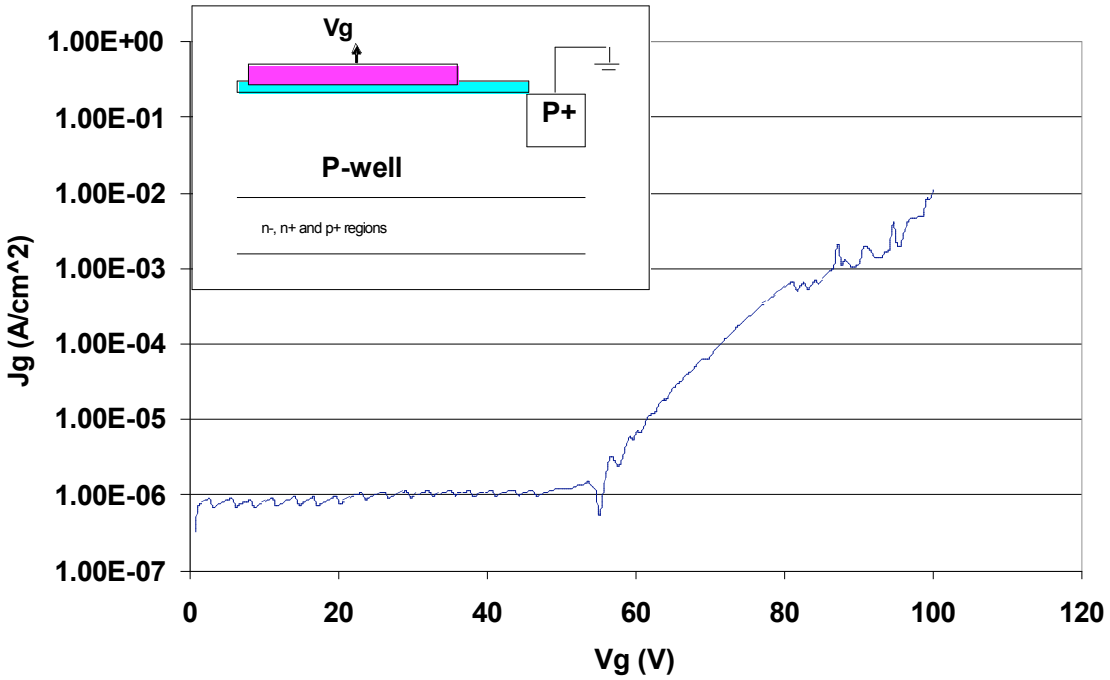


Figure 3.164 I-V of a capacitor over the pwell region after 2-minute 700 ºC contact anneal (240 nm thermal gate oxide).

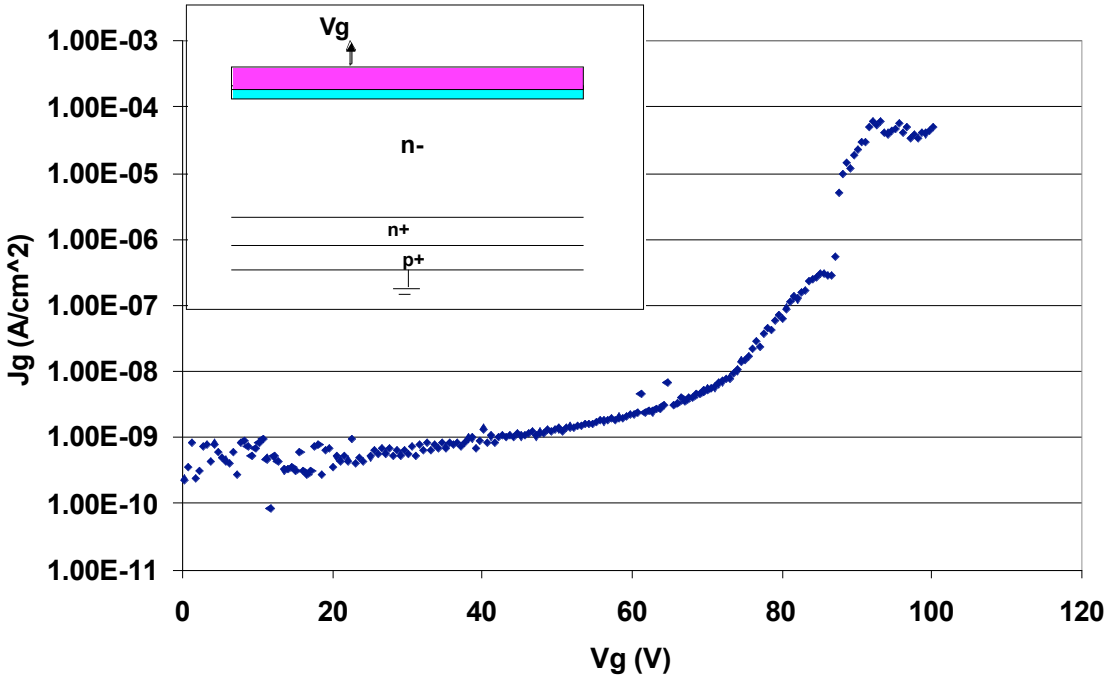


Figure 3.165 I-V of a capacitor over the n- region after 2-minute 700 ºC contact anneal (240 nm thermal gate oxide).

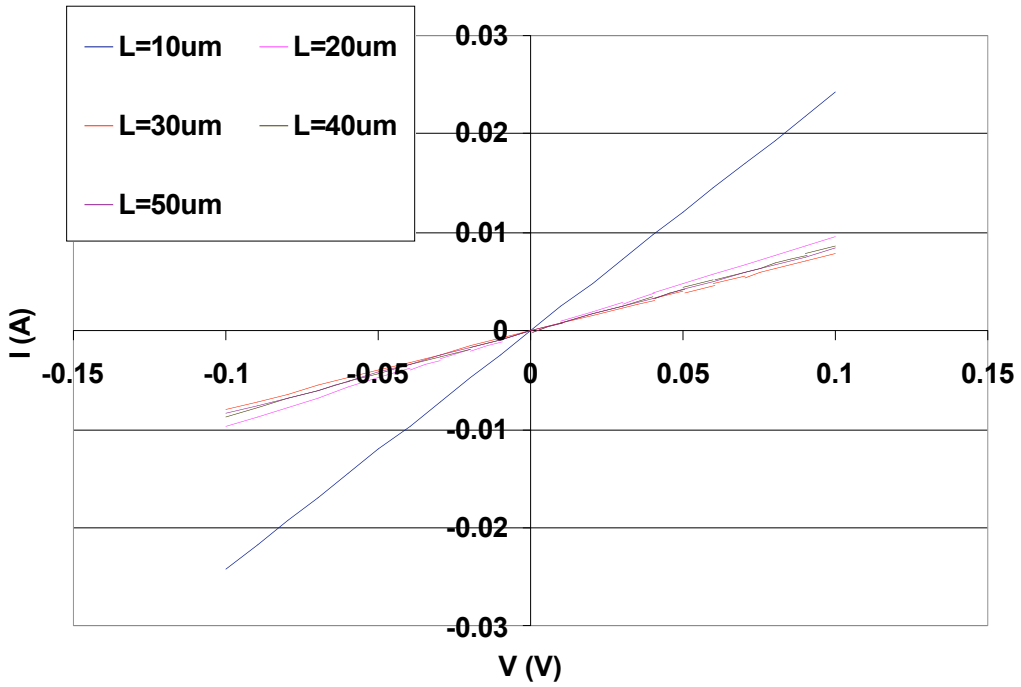


Figure 3.166 I-V characteristics of a p TLM after 2-minute 700 ºC contact anneal.

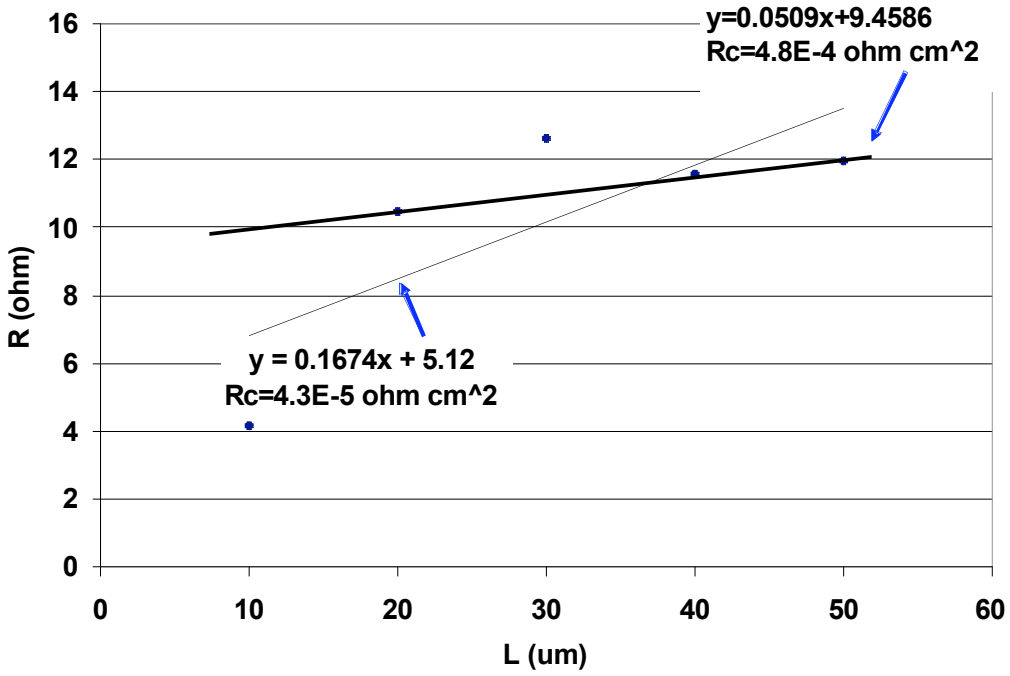


Figure 3.167 Contact resistivity of the p TLM after the 2-minute 700 ºC contact anneal.

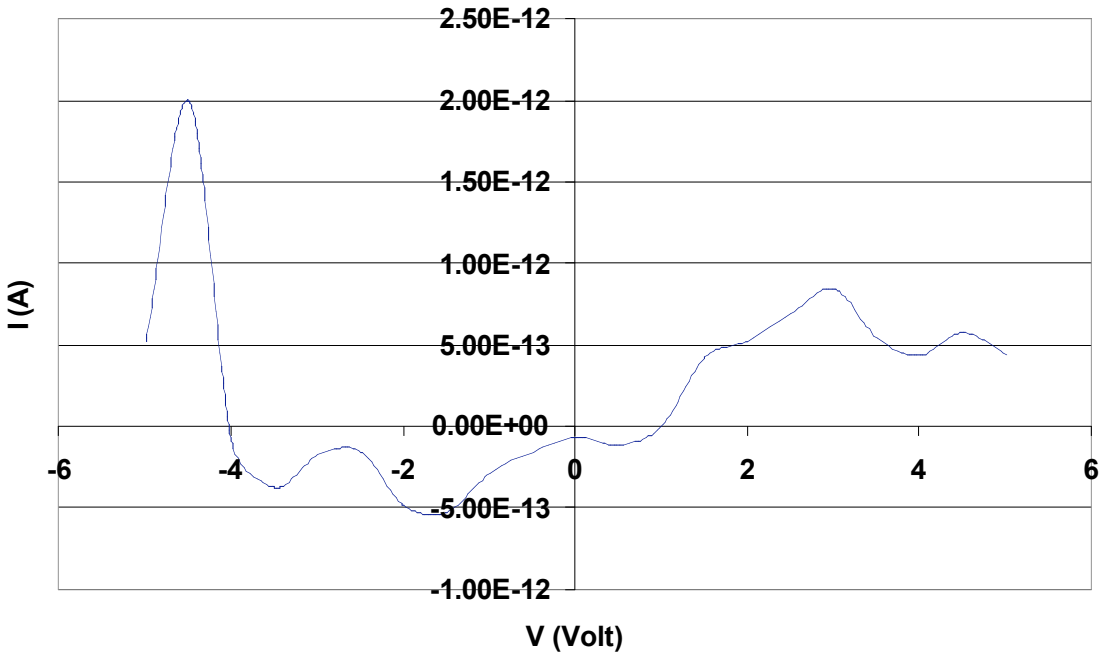


Figure 3.168 I-V of an n+ TLM after the 2-minute 700 ºC contact anneal.

3.2.4.3.3 750 ºC anneal

After the contact annealing at 750 ºC, the oxide over the n+ region was not leaky (see Fig. 3.169). However, the oxides over the pwell region and the n- region broke down at 37 V and 73 V, respectively, as shown in Figs. 3.170 and 3.171.

The n contact could conduct current after the anneal as shown in Fig. 3.172, but its I-V characteristics were not linear. The p contacts were ohmic after the anneal (see Fig. 3.173). The contact resistivity was 1.9×10^{-3} ohm cm^2 based on the best linear fit of the R vs L plot (Fig. 3.174).

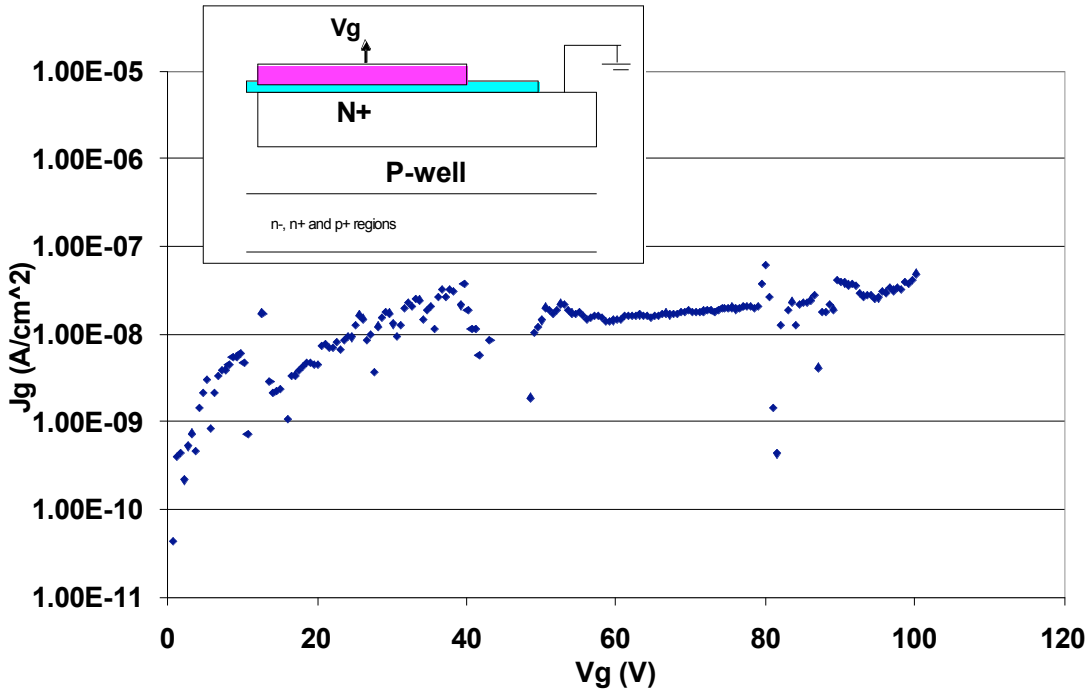


Figure 3.169 I-V of a capacitor over the n+ region after 2-minute 750 ºC contact anneal (240 nm thermal gate oxide).

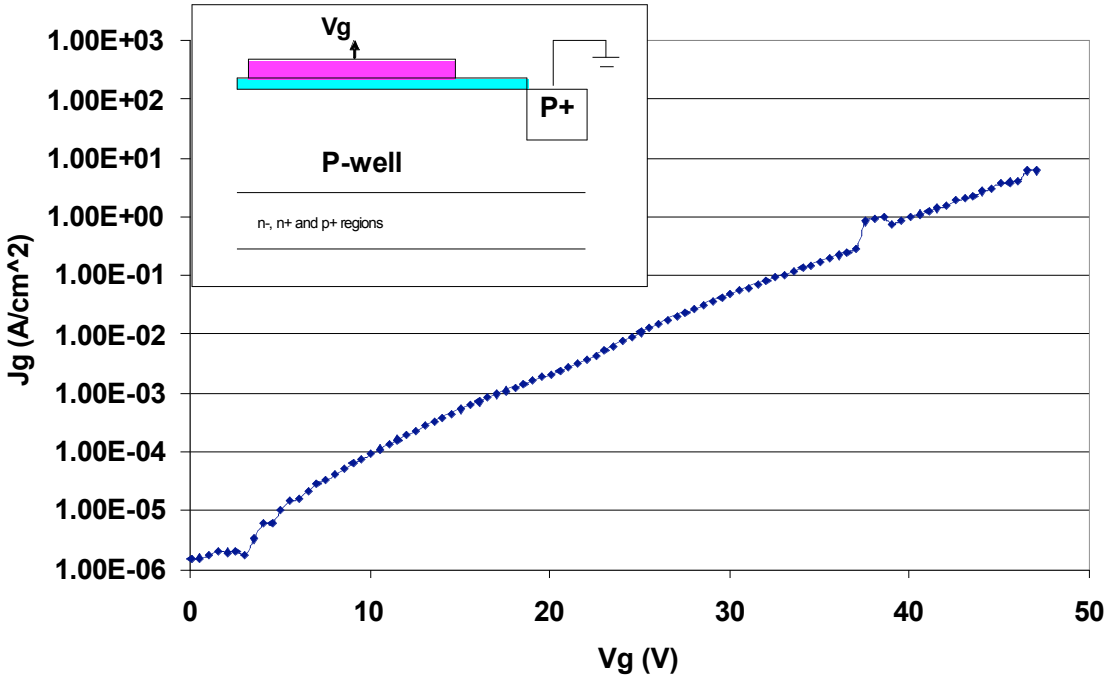


Figure 3.170 I-V of a capacitor over the pwell region after 2-minute 750 ºC contact anneal (240 nm thermal gate oxide).

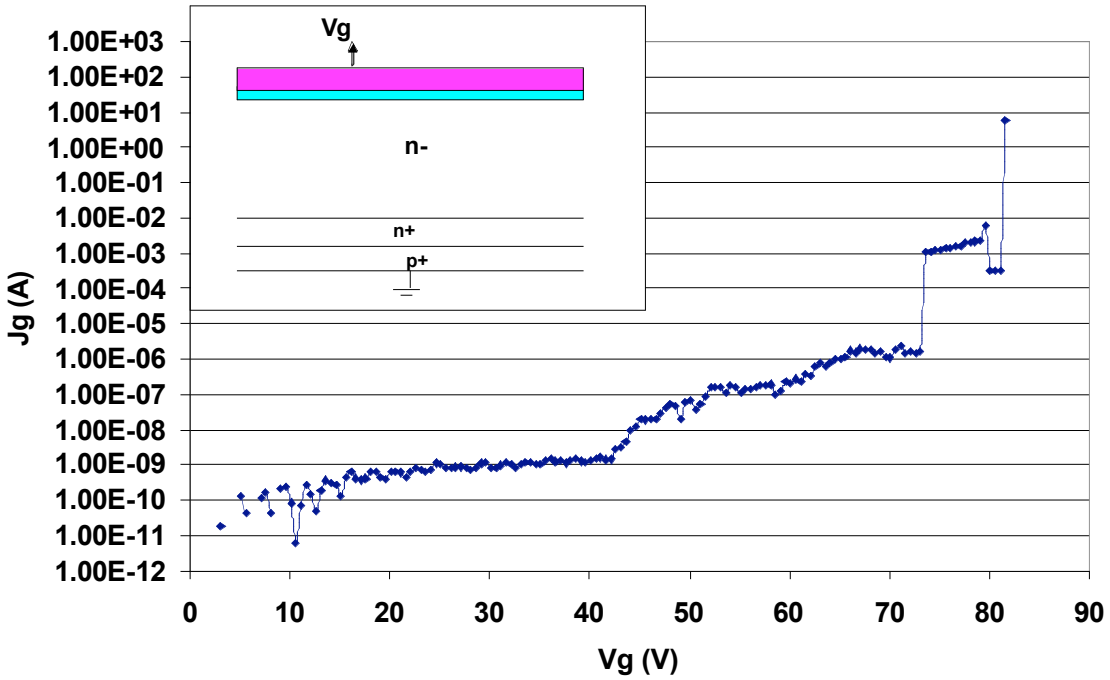


Figure 3.171 I-V of a capacitor over the n- region after 2-minute 750 ºC contact anneal (240 nm thermal gate oxide).

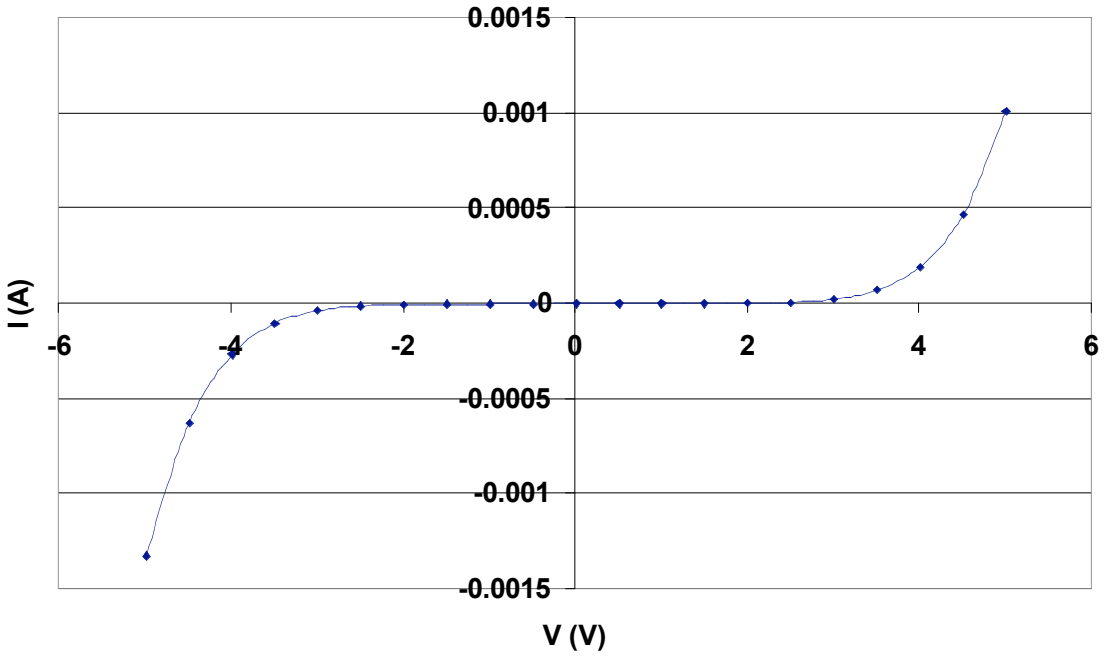


Figure 3.172 I-V of an n+ TLM after the 2-minute 750 ºC contact anneal.

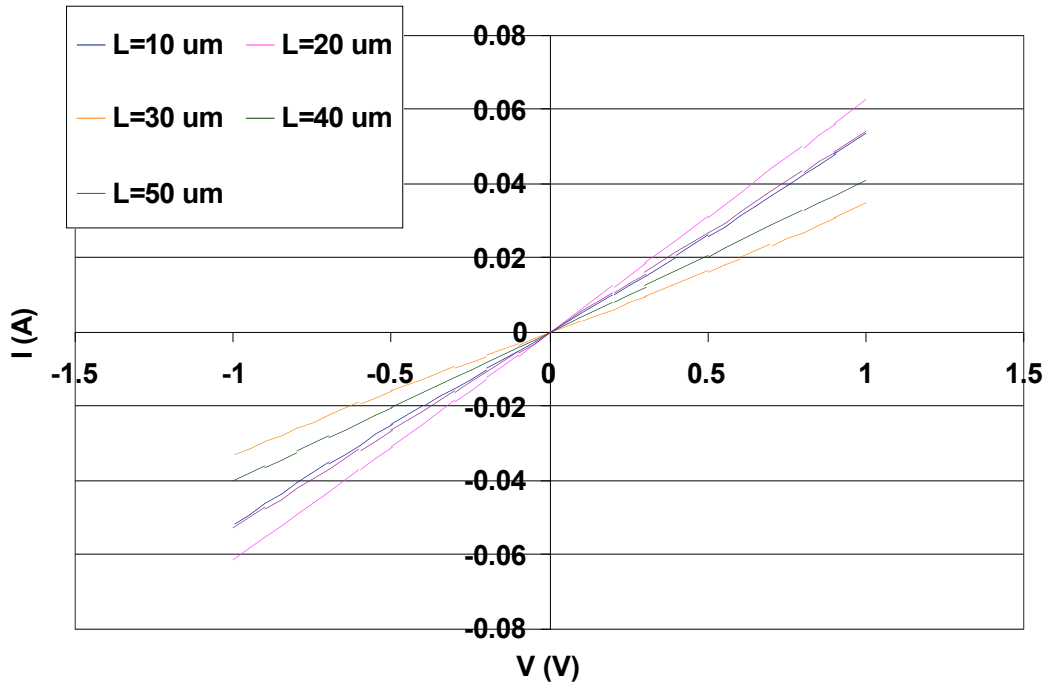


Figure 3.173 I-V characteristics of a p TLM after 2-minute 750 ºC contact anneal.

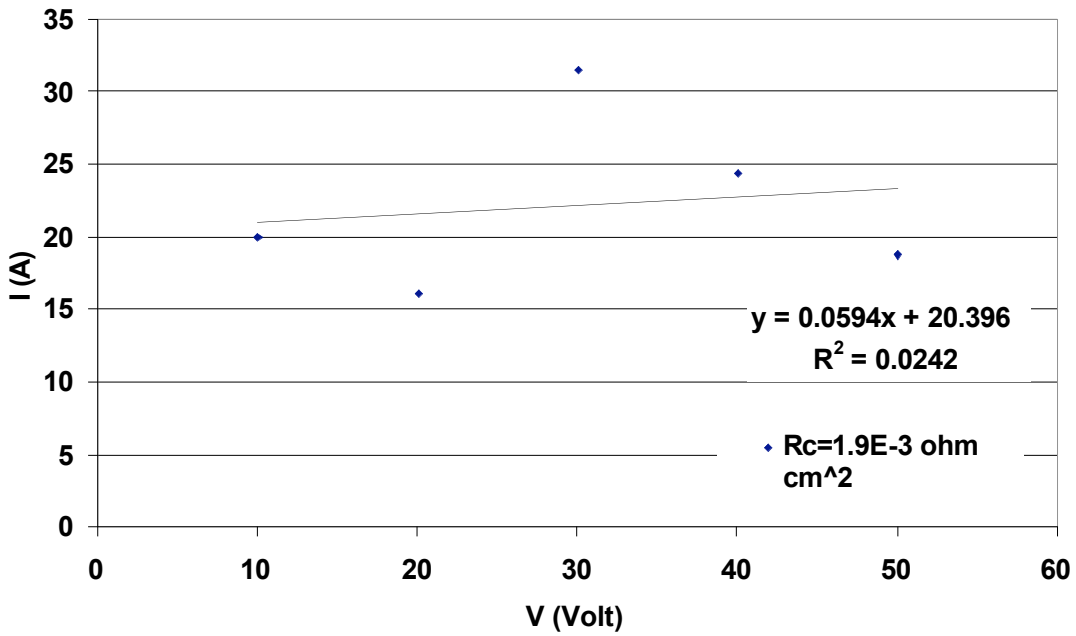


Figure 3.174 Contact resistivity of the p TLM after the 2-minute 750 ºC contact anneal.

3.2.4.4 Characterization of Devices on Sample 4

For sample 4, only the p+ base contact (33 nm Ti/ 167 nm Al) was annealed in the SiC contact annealer (in vacuum). The n+ source contact (50 nm Ti/ 100 nm Ni) was not annealed. Both the p+ contact and the n+ contact were ohmic, as shown in Figs. 3.175 and 3.177, with contact resistivities of 1.167×10^{-2} ohm cm^2 and 1.886×10^{-2} ohm cm^2, respectively.

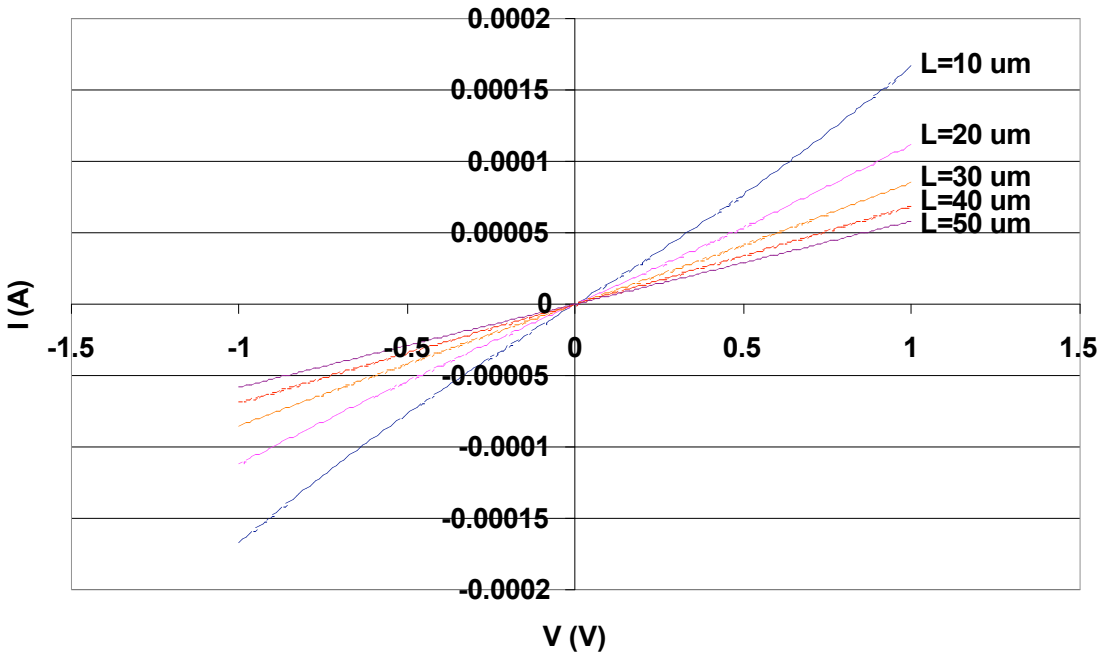


Figure 3.175 I-V characteristics of an n+ TLM on sample 4.

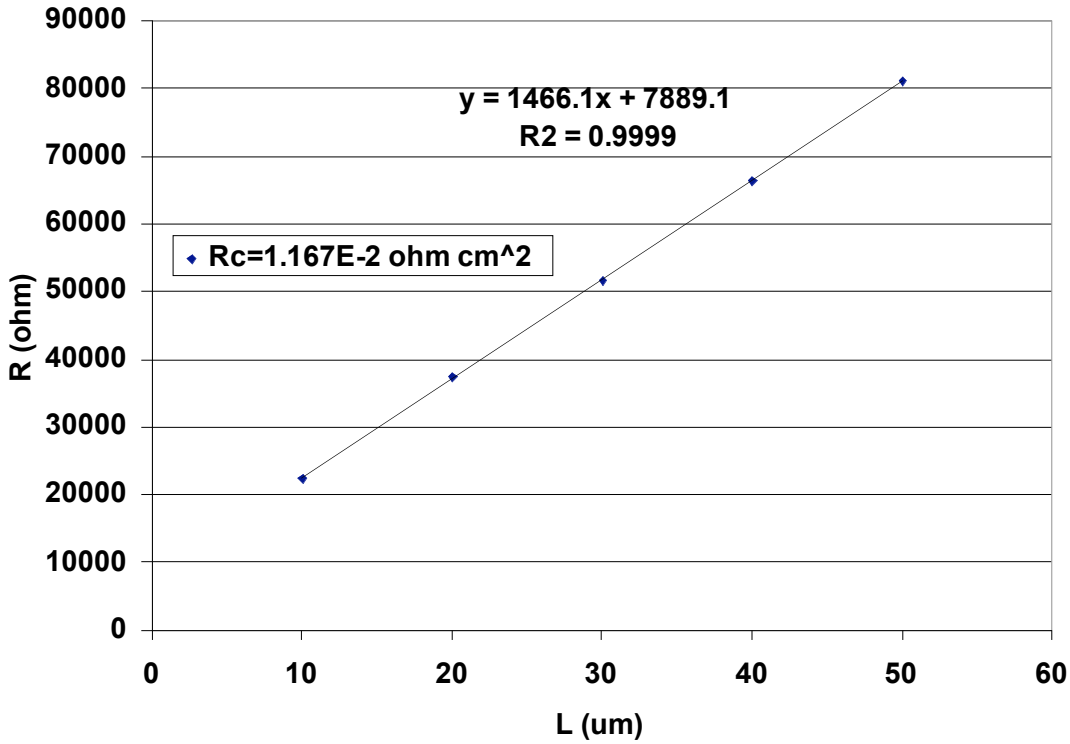


Figure 3.176 Contact resistivity of the n+ TLM on sample 4.

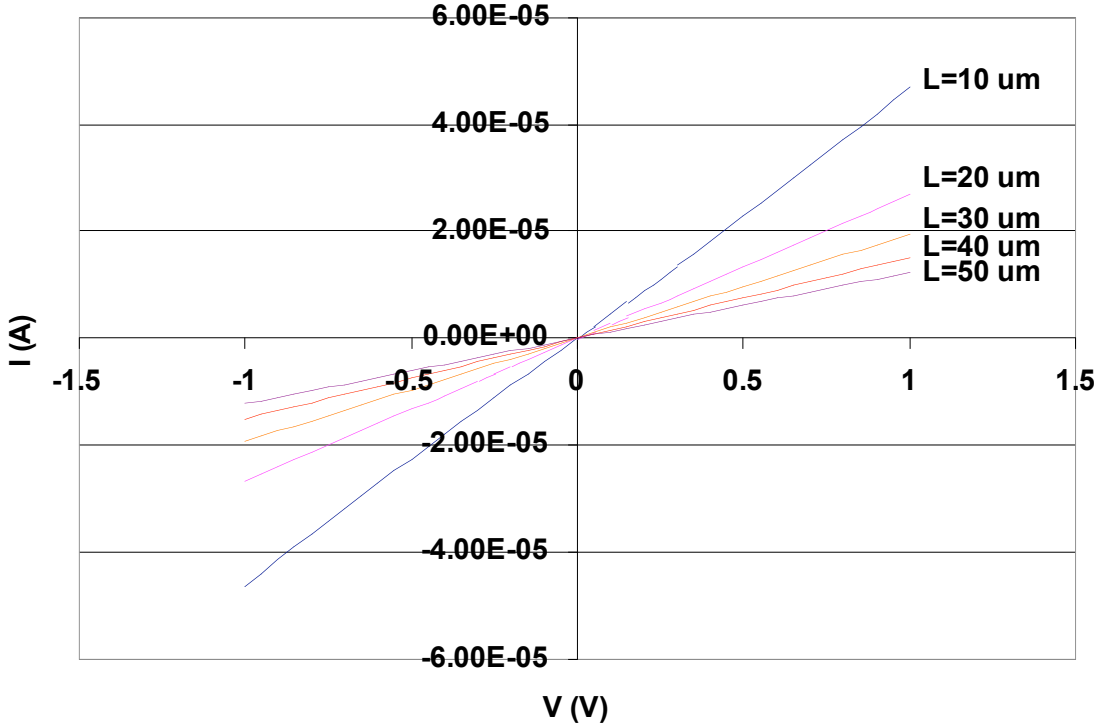


Figure 3.177 I-V characteristics of a p+ TLM on sample 4.

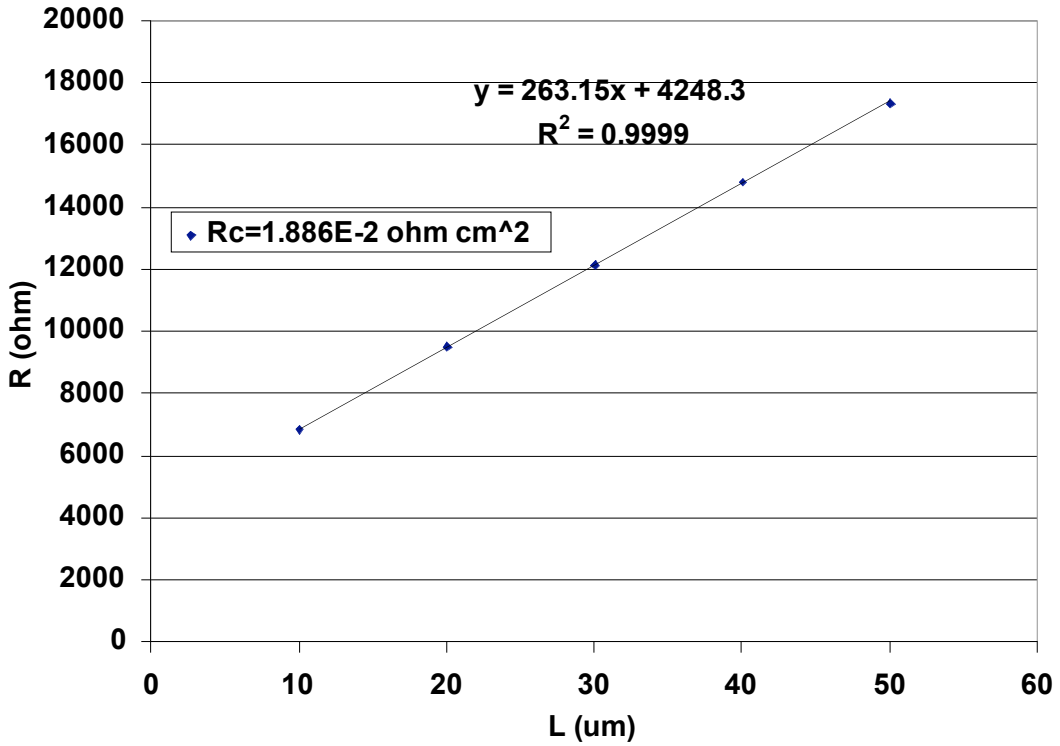


Figure 3.178 Contact resistivity of the p+ TLM on sample 4.

Figure 3.179 shows the on-state characteristics of a c-type IGBT (with separated p+ base and n+ source contacts) on sample 4. The drain currents can be modulated by the gate. A gate leakage exists, as manifested by the slightly negative drain currents near the origin. Figure 3.180 shows the I-V between two adjacent pwell TLMs. Since the current is almost zero, we can eliminate the possibility of surface leakage. Figure 3.181 shows the drain, base, source and gate currents at V_d=0 and V_g= 20 V. Around 90% of the gate leakage current goes through the oxide over the n+ source region, around 9.8% through the oxide over the n- region and only about 0.2% through the oxide over the pwell. Figure 3.182 shows the drain, base, source and gate currents vs V_d at V_g= 0. The drain current and the gate current are almost equal to each other with opposite polarities. This is consistent with what we observed in Fig. 3.178 (the oxide over the n- region is leaky). Figures 3.183 to 3.185 are the I-V curves of capacitors over the n+, pwell and n- regions. The oxide over the n+ region breaks down at $V_g \approx 12$ V. The leakage current density of the oxide over the n- region is around 7 A/cm^2 at V_g=20 V. The leakage current density of the oxide over the pwell is only around 1×10^{-7} A/cm^2 at V_g=20 V.

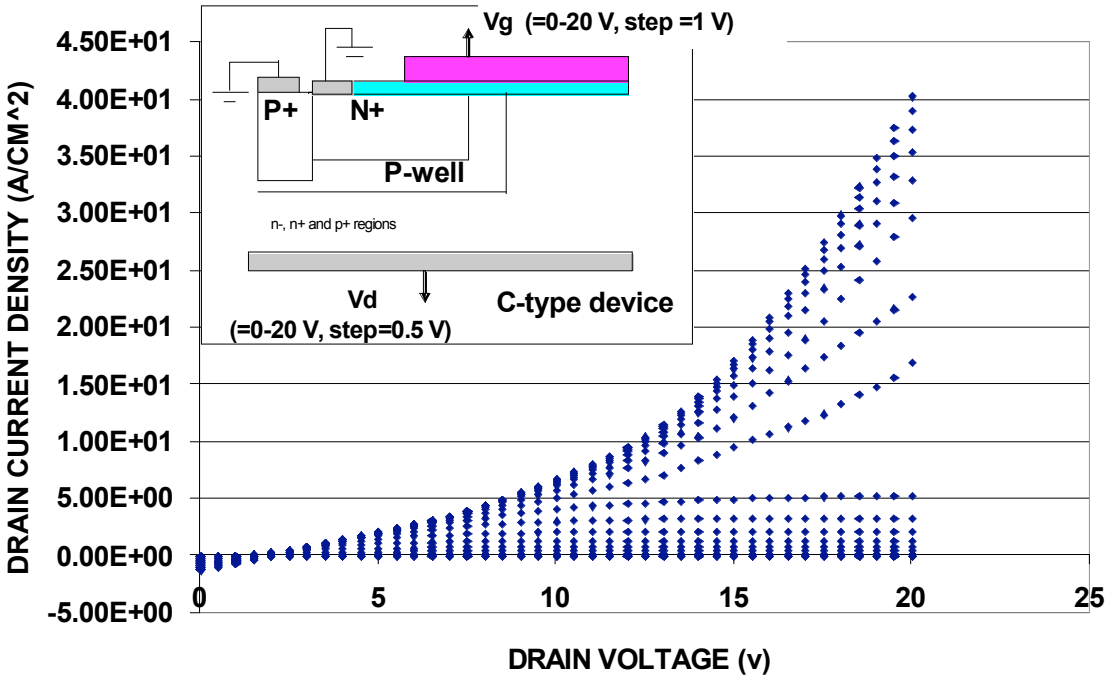


Figure 3.179 On-state characteristics of a c-type IGBT on sample 4. The p+ base contact and the n+ source contact are separated.

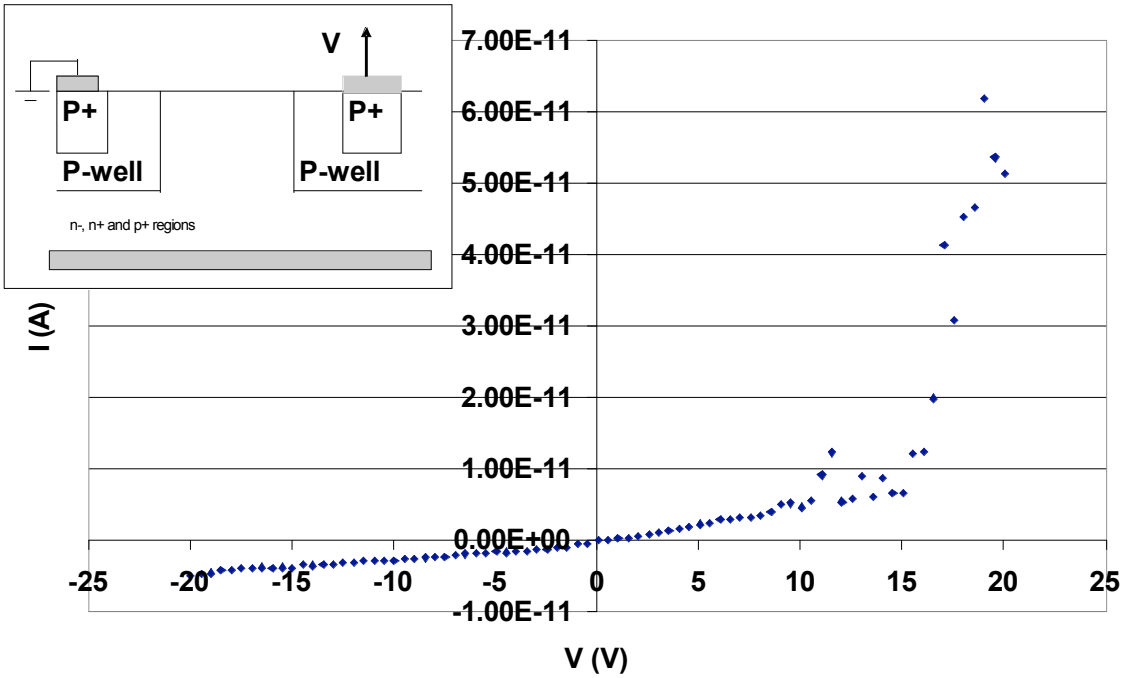


Figure 3.180 I-V between two adjacent pwell TLMs.

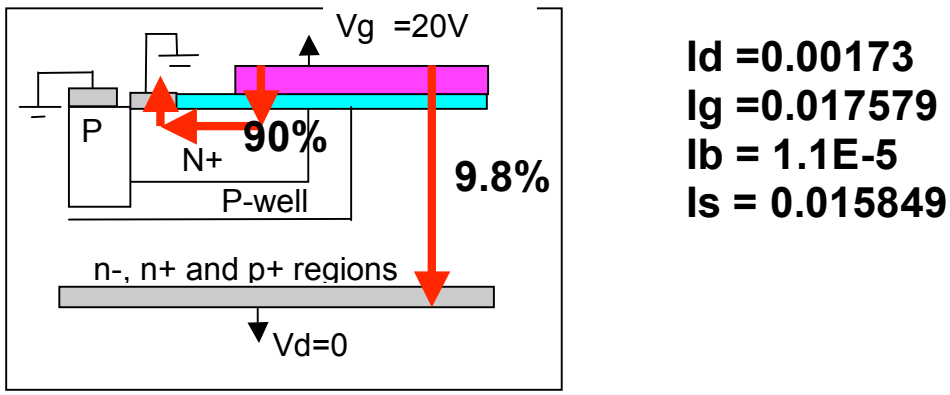


Figure 3.181 Drain, source, base and gate currents at V_d=0 and V_g=20 V.

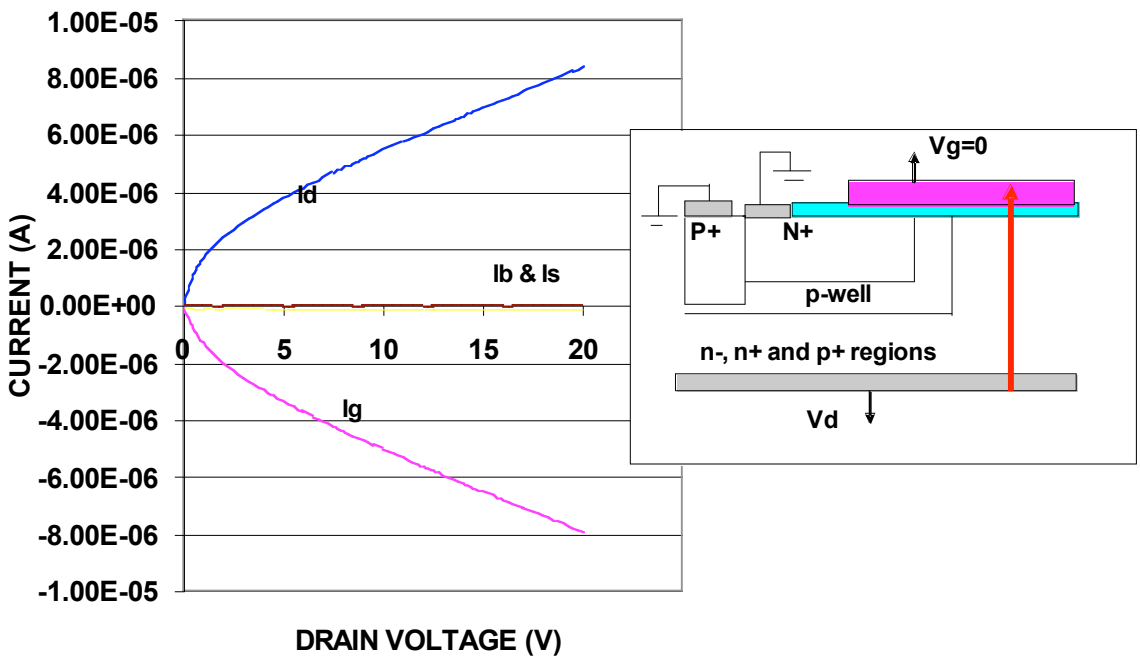


Figure 3.182 Drain, source, base and gate currents vs V_d at V_g=0.

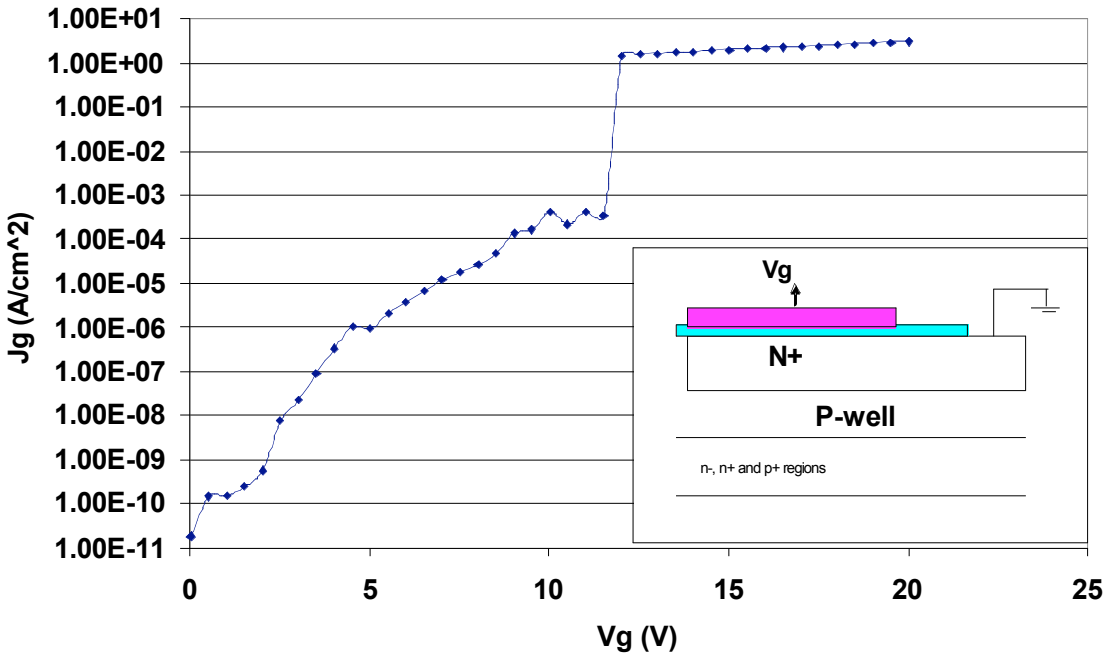


Figure 3.183 I-V of a capacitor over the n+ region on sample 4. Thickness of the thermal gate oxide is around 45 nm.

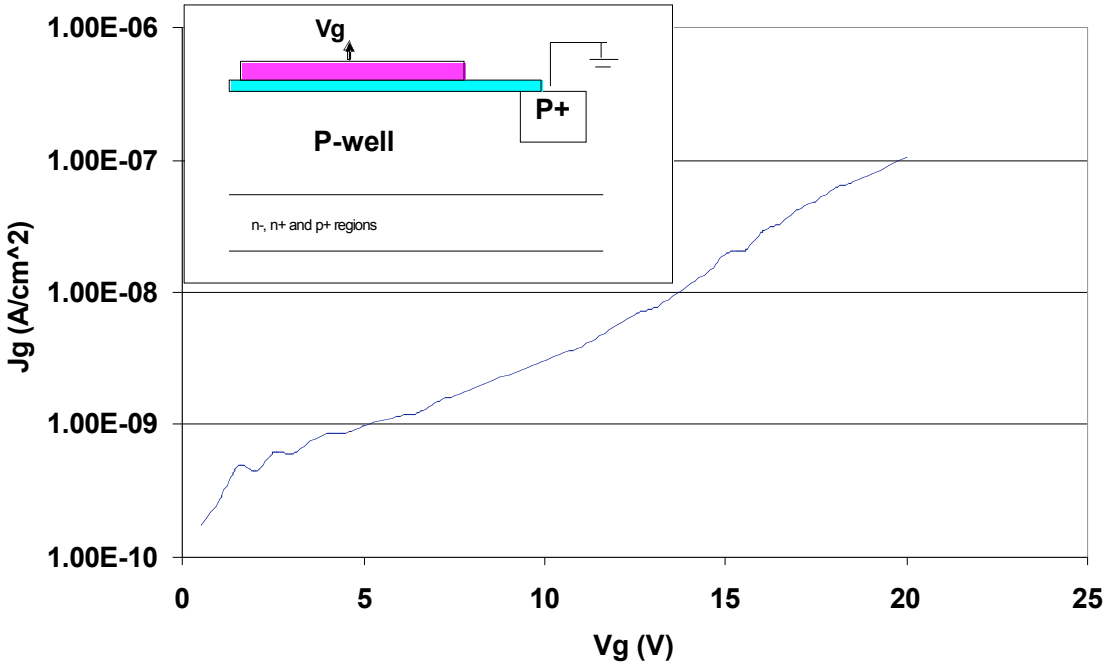


Figure 3.184 I-V of a capacitor over the pwell region on sample 4. Thickness of the thermal gate oxide is around 45 nm.

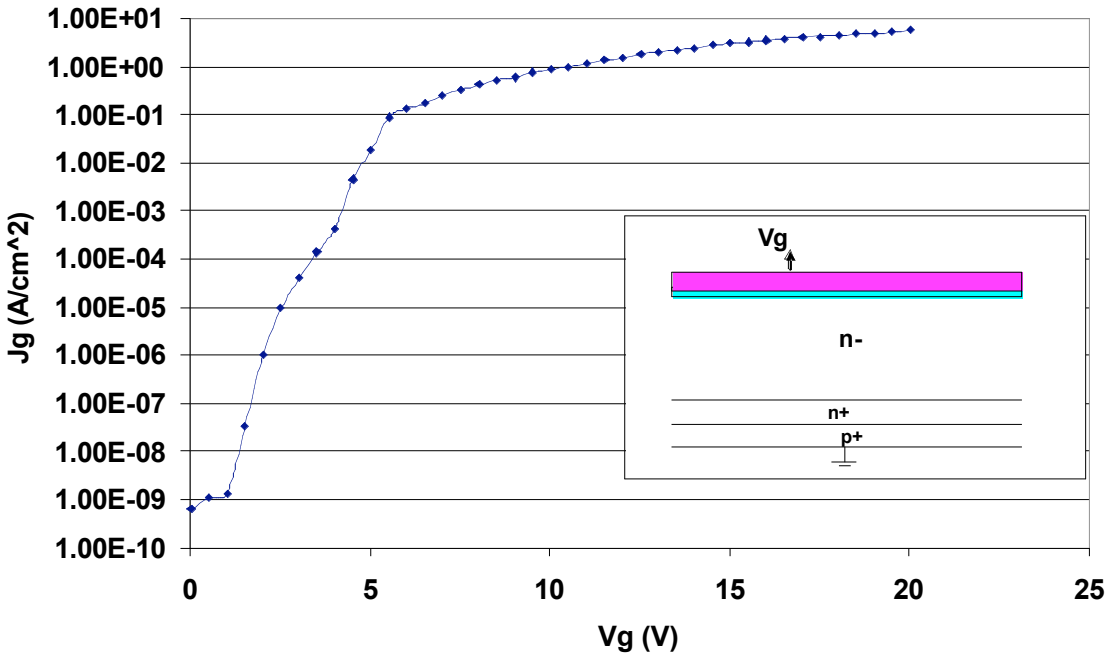


Figure 3.185 I-V of a capacitor over the n- region on sample 4. Thickness of the thermal gate oxide is around 45 nm.

Figure 3.186(a) shows the comparison of the on-state characteristics of the c-type IGBT on sample 4 with the MEDICI simulation data. In the simulation, the contact resistivities of the actual devices on sample 4 were used and the gate voltage was 20 V. All the other parameters of the device simulated are given in Fig. 3.186 (b). At a power dissipation of 300 W/cm^2, the drain current density is 35 A/cm^2 from the simulation, but is only 19 A/cm^2 for the actual device (for the best devices on sample 4 after the first contact anneal, which will be shown later, the current density is 23-24 A/cm^2).

In addition, at low gate or drain voltages, the device behaves like a MOSFET (see Fig. 3.187). This is similar to the devices on sample 2 before the contact anneal (with thermal gate oxide) and after the LTO deposition. This could be explained by a leakage path parallel to the junction of the p+ anode layer and the n+ buffer layer. Figure 3.188 shows the I-V characteristics of a "diode" on sample 4. Unlike conventional diodes, this "diode" actually has two back-to-back pn junctions. No matter if the voltage applied is positive or negative, there should be no current conducting in this device. However, when the voltage applied to the top is positive relative to the backside (junction J1 in Fig. 3.186 is reverse biased), this device behaves like an ordinary diode with a large reverse resistance. This means there must be a leakage path at junction J1. The leakage path can be modeled as a resistor parallel to junction J1 as shown in Fig. 3.189. This resistor shorts the p+/n+ junction until the voltage across it exceeds 2.8 V. Before the

current in the IGBT is high enough for the voltage across the resistor to exceed 2.8 V, the device behaves just like a MOSFET. Once the voltage drop exceeds about 2.8 V, the p+/n diode is forward biased and injects holes into the n- drift region, inducing conductivity modulation. Figure 3.190 shows the MEDICI simulation of an IGBT with the parallel leakage path. At low gate or drain voltages, where the p+/n substrate diode is not strongly forward biased, the characteristic of the IGBT resembles that of a MOSFET.

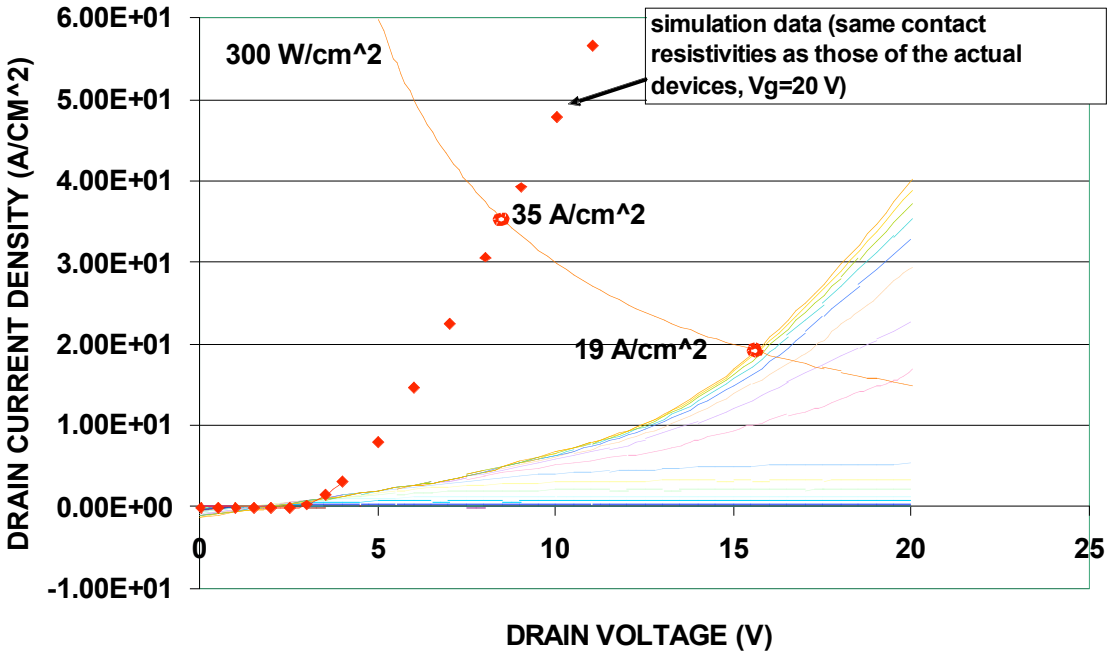


Figure 3.186 (a) Comparison of the on-state characteristics of the c-type IGBT on sample 4 with the MEDICI simulation data.

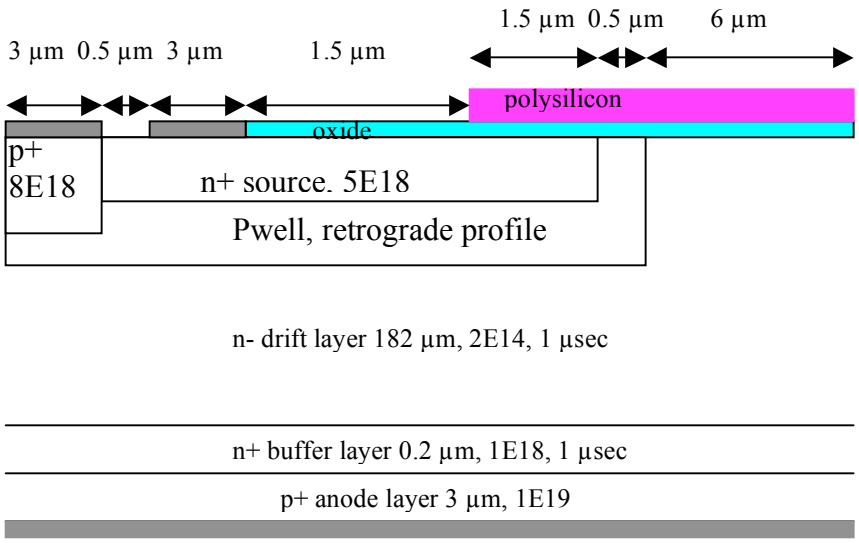


Figure 3.186 (b) Parameters of the device simulated. The lifetime shown in this figure is ambipolar lifetime.

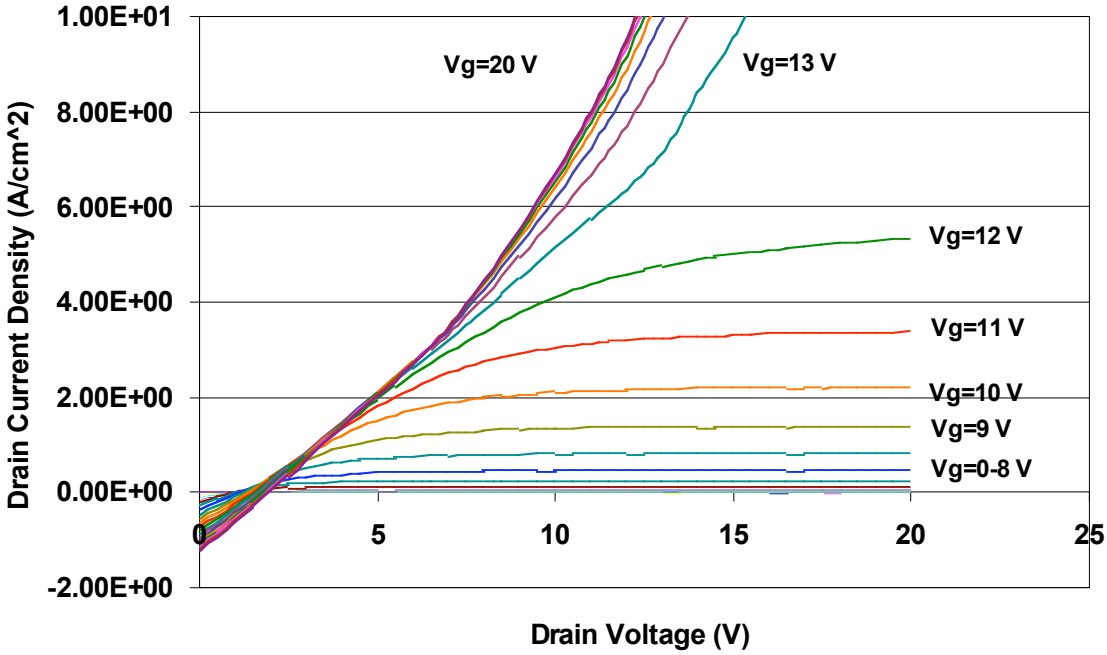


Figure 3.187 I-V characteristics of the c-type IGBT on sample 4 (the vertical axis is scaled so that the maximum

drain current density shown in this figure is 10 A/cm^2). At low gate or drain voltages, the device behaves like a MOSFET.

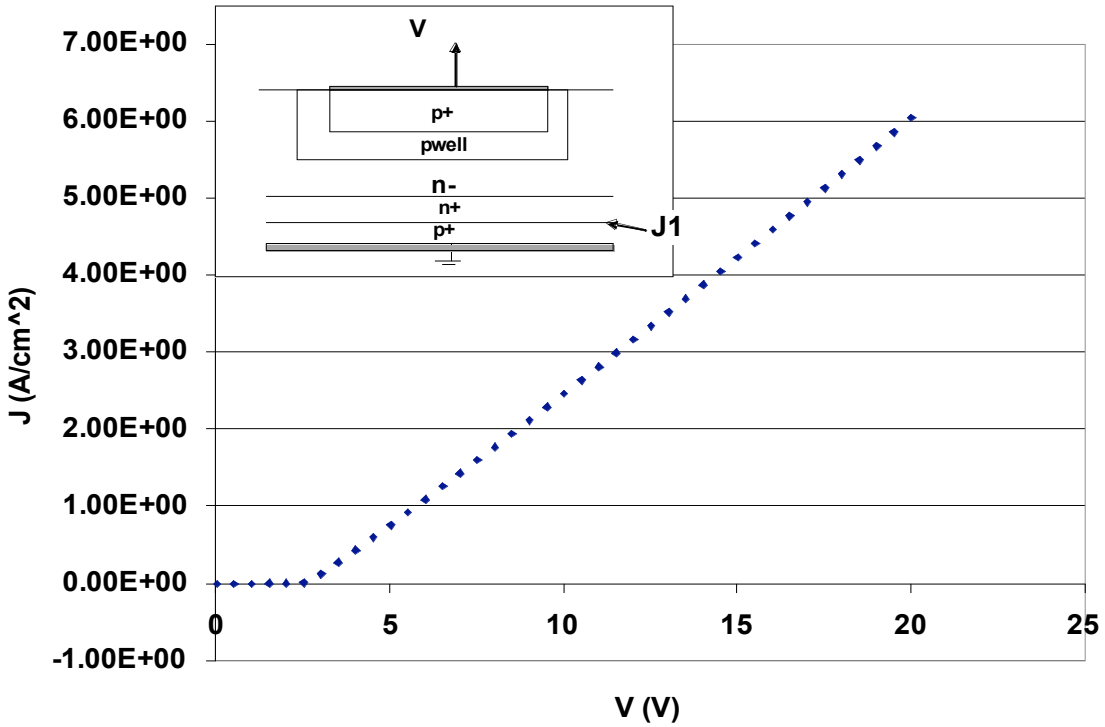


Figure 3.188 I-V characteristics of a diode on sample 4.

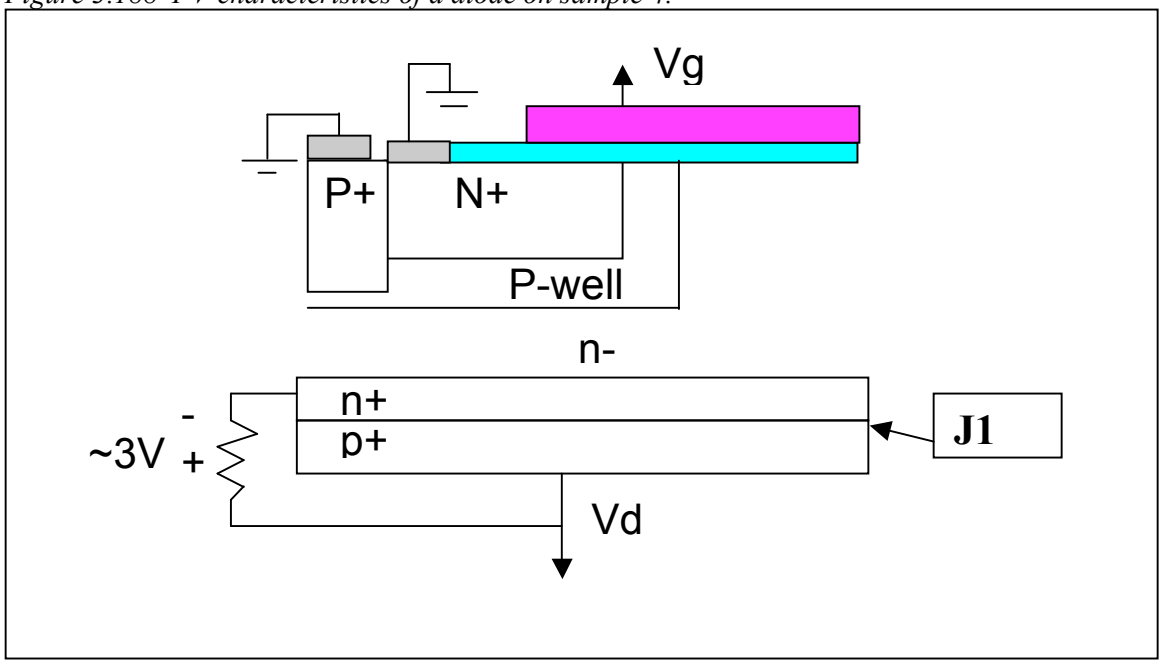


Figure 3.189 IGBT with a leakage path parallel to junction J1.

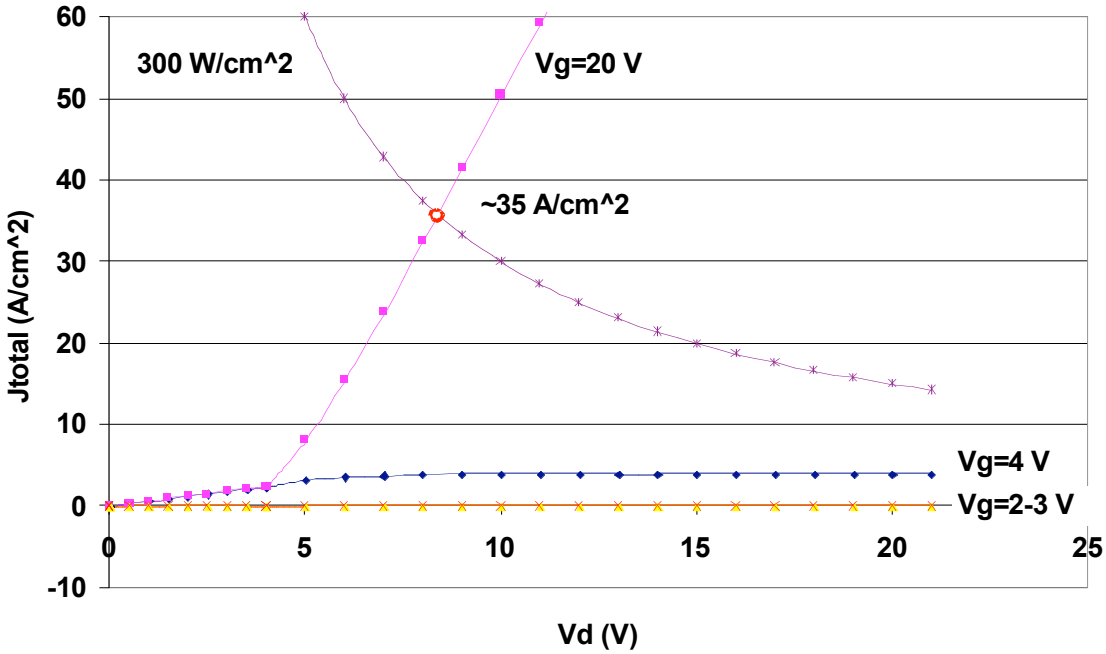


Figure 3.190 MEDICI simulation of an IGBT with a leakage path parallel to the junction of the p+ anode layer and the n+ buffer layer. At low drain or gate voltage, the device behaves like a MOSFET.

As shown in Medici simulations of Fig. 3.190, with the parallel leakage path, the current density (at V_g=20 V) is still around 35 A/cm^2 at a power dissipation of 300 W/cm^2. One explanation of the lower current density in the actual device is that the p+ anode layer is not completely ionized, leading to low hole injection efficiency. If this were the explanation, the current density should increase at elevated temperatures. However, as shown in Fig. 3.191, the current densities at a power dissipation of 300 W/ cm^2 are almost the same for the same device measured at 30 ºC and 250 ºC. In addition, we included incomplete ionization in the simulation, so we can conclude that freeze-out in the p+ anode layer is not the explanation to this problem

Another explanation is that the p+ back contact of sample 4 may not be ohmic. For a non-ohmic contact, the differential resistance decreases as the current increases. At low drain currents, the differential resistance of the p+ back contact is high, resulting in a gradual increase of the drain current. With increasing drain current, the p+ back contact resistance gets lower and lower. When it is low enough, we will see the “turn-on” of the IGBT.

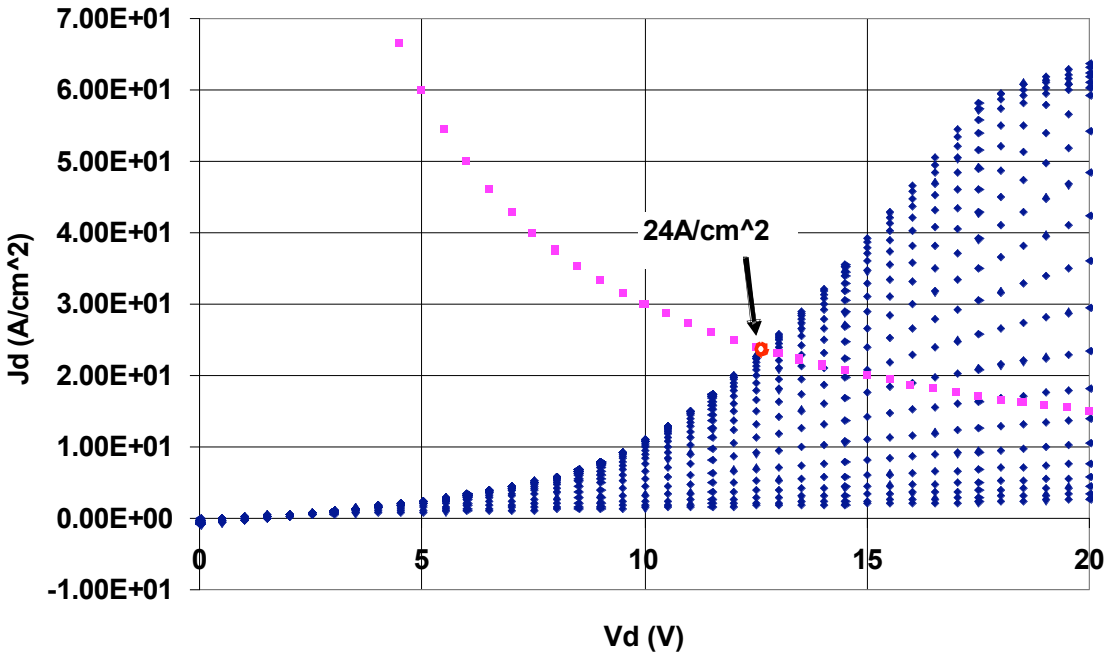


Figure 3.191 (a) I-V characteristics of an IGBT on sample 4 (T=30 ºC)

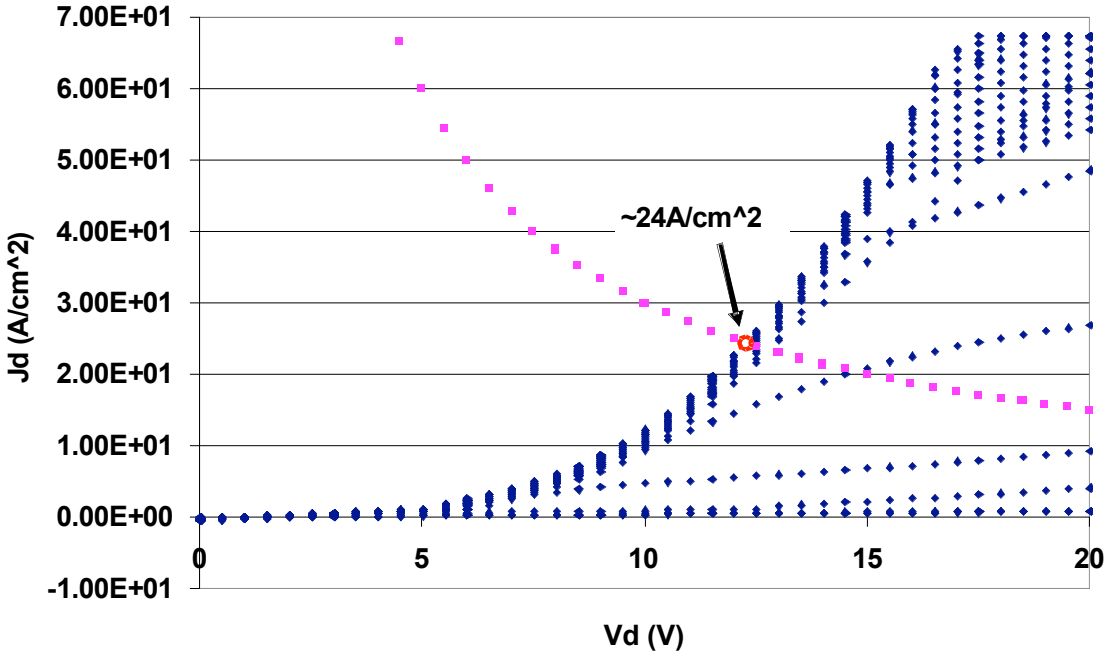


Figure 3.191 (b) I-V characteristics of an IGBT on sample 4 (T=250 ºC)

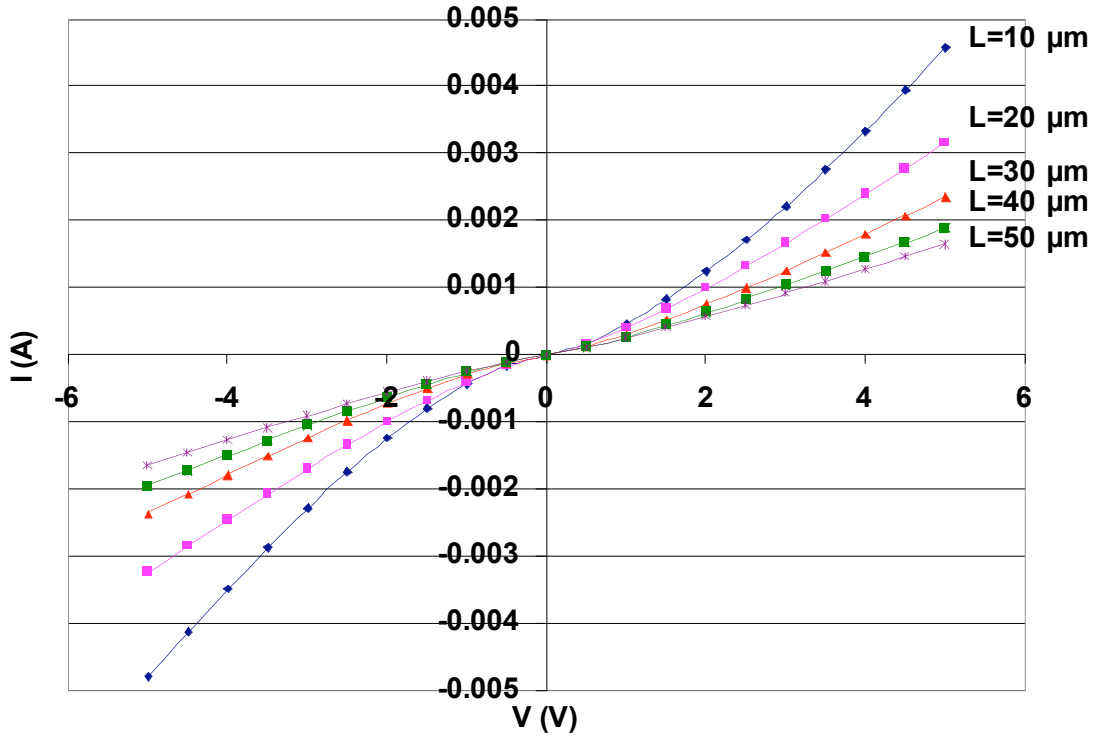


Figure 3.192 I-V characteristics of an n+ TLM on sample 4 after the second contact anneal.

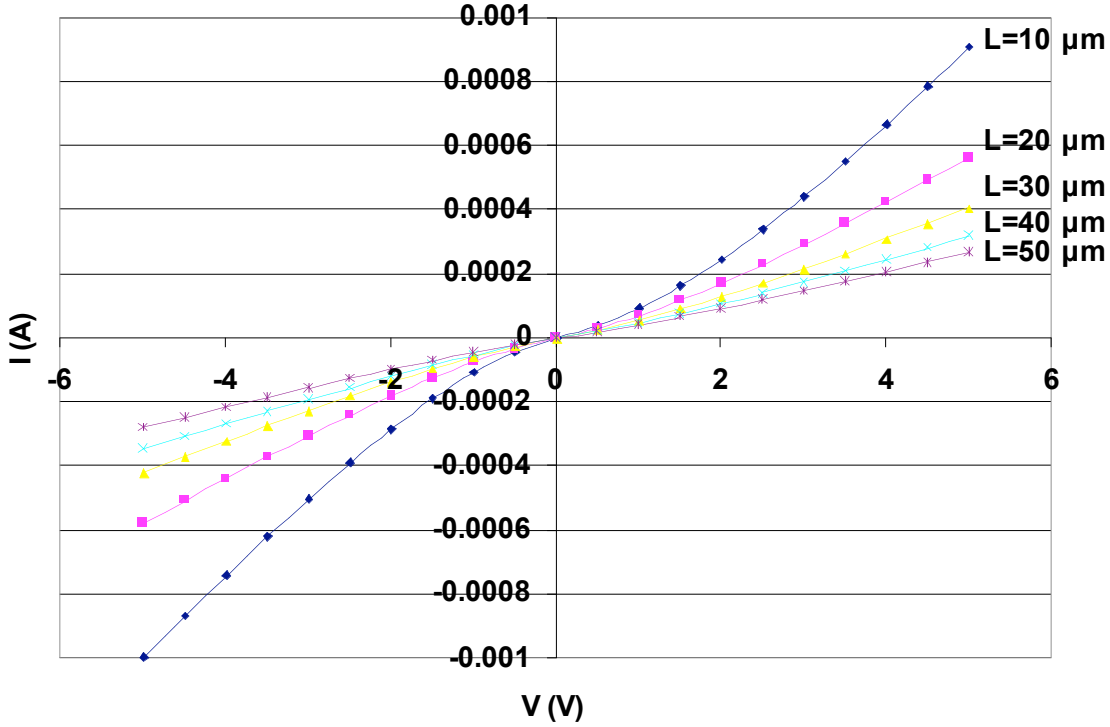


Figure 3.193 I-V characteristics of a p+ TLM on sample 4 after the second contact anneal.

The contacts on sample 4 were re-annealed at around 800 ºC for 2 minutes (at the end of the 2-minute anneal, the temperature was 820 ºC). The n+ contact was improved after the contact anneal, but the p+ contact was not improved (see Figs. 3.192 and 3.193). The current density of an IGBT on sample 4 at the power dissipation of 300 W/cm^2 is 27.3 A/cm^2 (see Fig. 3.194).

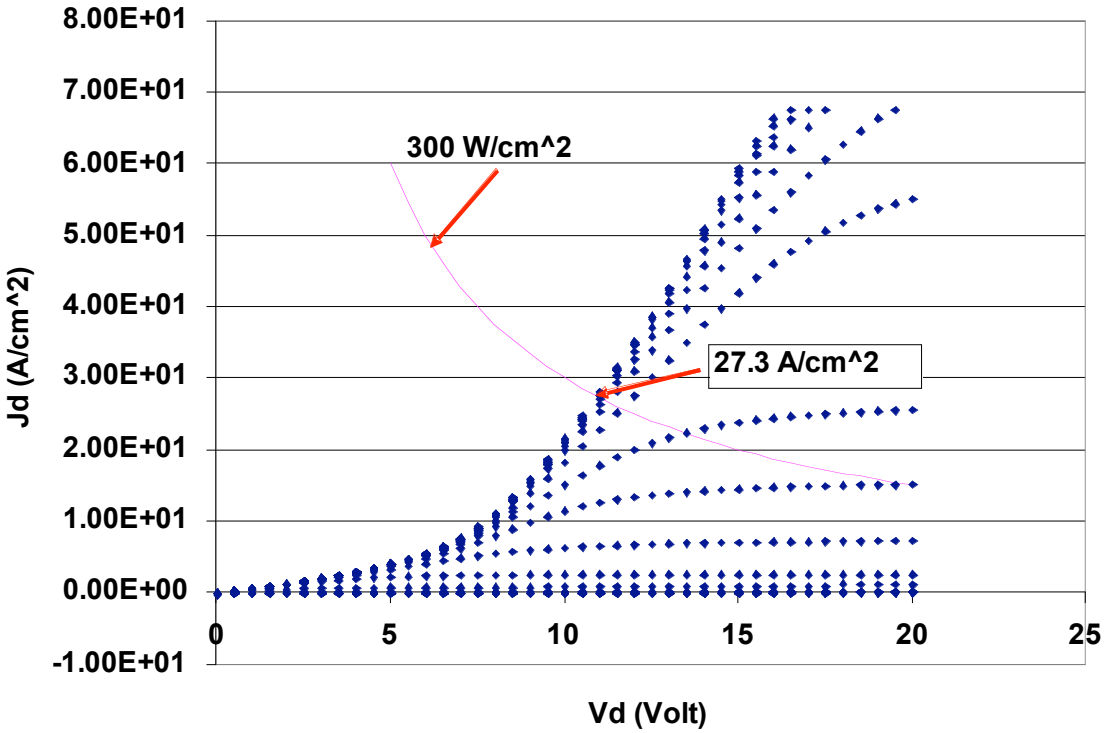


Figure 3.194 On-state characteristics of an IGBT on sample 4 after the second contact anneal.

3.2.4.5 Point Defects

In almost all the IGBTs on samples 3 and 6, and some of the IGBTs on samples 2, 4 and 5, a so-called point defect problem was found. Figure 3.195 shows the I-V characteristics between the n+ sources of two IGBTs on sample 4 right after the implant activation anneal (there was nothing on the surface of SiC). For normal devices, at such low voltages, the current should be zero. The non-zero current could come from surface leakage. However, surface leakage was not detected on sample 4. Another explanation is defects in the pwell. As shown in Fig. 3.196, if the pwell implantation is not deep enough in some localized spots, the n+ implantation will be shorted to the n- drift layer and current will be able to conduct between the sources of two IGBTs. Such defects may be caused by micromasking during the patterning of the pwell implant mask. Micromasking is unwanted sputtering of the nickel implant mask, resulting in particles of nickel falling onto the area where the implant is to be performed. As shown in Fig. 3.197, these nickel particles block the p-base implant in isolated spots, leaving conduction paths between the n+ sources of the IGBTs. We normally eliminate micromasking by coating the large nickel areas with PR 4620. However, in some of these samples, we used PR 1518, which is thinner than PR 4620, instead. For the other samples, no PR was applied to prevent micromasking.

Figure 3.198 shows the I_d-V_d curve (at V_g=0) of an IGBT on sample 4 with point defects. Around 97% of the current flows through the point defects and 3% through the oxide. The current tends to increase almost linearly at low voltages, and saturate at higher voltages. This looks very much like a JFET, with the grounded pwell acting as the gate and the n-type “pipe” as the channel.

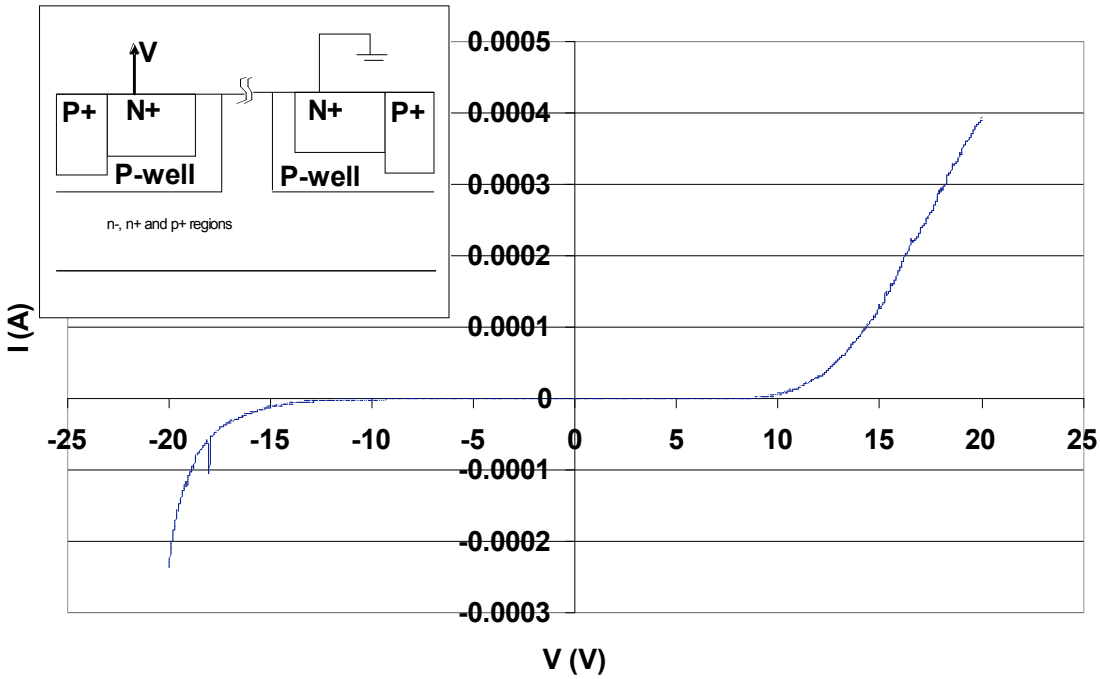


Figure 3.195 I-V characteristics between the n+ sources of two IGBTs on sample 4.

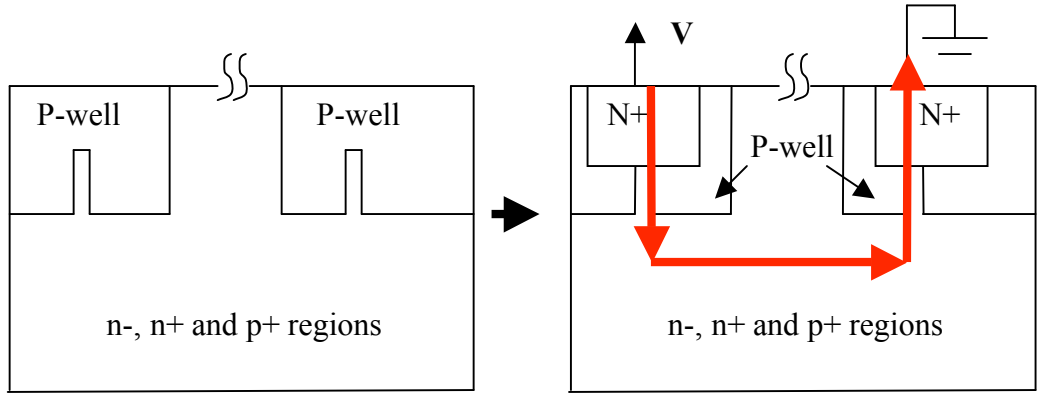


Figure 3.196 Point defects in the pwell. If the pwell implantation is not deep enough in some area, the n+ implantation will be in direct contact with the n- drift layer and current will flow between the sources of two IGBTs.

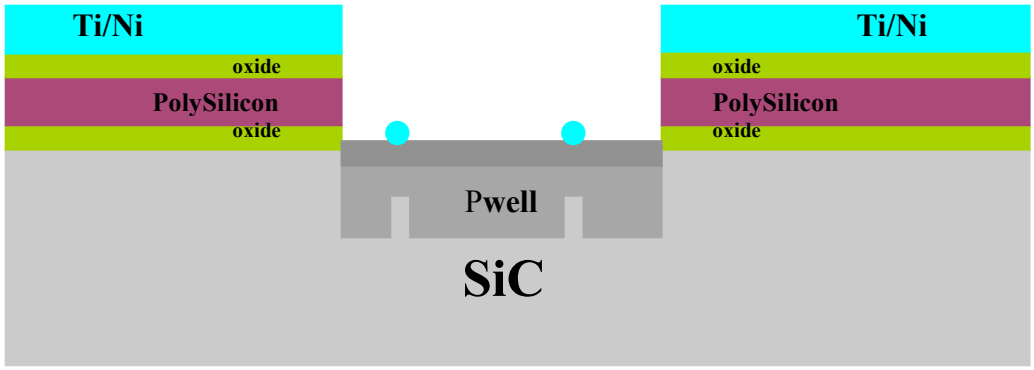


Figure 3.197 Micromasking. The nickel particles are sputtered onto the area where the implant is to be performed, blocking the implant in isolated spots.

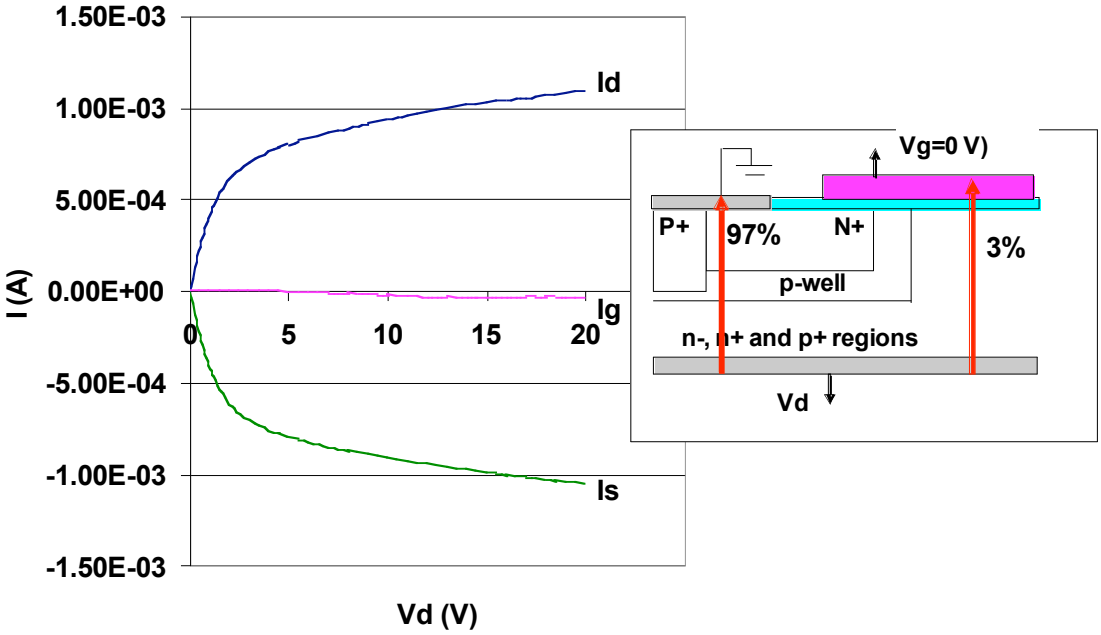


Figure 3.198 Drain, source/base and gate currents vs V_d at V_g=0. An IGBT on sample 4 with point defects.

3.2.4.6 Thermal Oxide on C-face SiC

Studies at Vanderbilt University show that thermal oxide on C-face SiC (epi) has a lower breakdown field than that on Si-face SiC. As shown in Fig. 3.199, for oxides passivated in NO, the breakdown field of the oxide grown on C-face is around 5.5 MV/cm and on Si-face around 9.8 MV/cm. The breakdown field could be lower for thermal oxides on Al-implanted regions, based on an experiment conducted by Dr. Kung-Yen Lee at Purdue University [23]. In this experiment, an Al-implanted (dose=$8x10^{12}$ cm^{-2}, annealed at 1600 ºC for 10 min in Ar) C-face SiC sample was oxidized (wet) at 950 ºC for 17.5 min, followed by NO anneal at 1175 ºC for 2.5 hours. Figure 3.200 shows that the oxide breakdown field is only about 3 MV/cm.

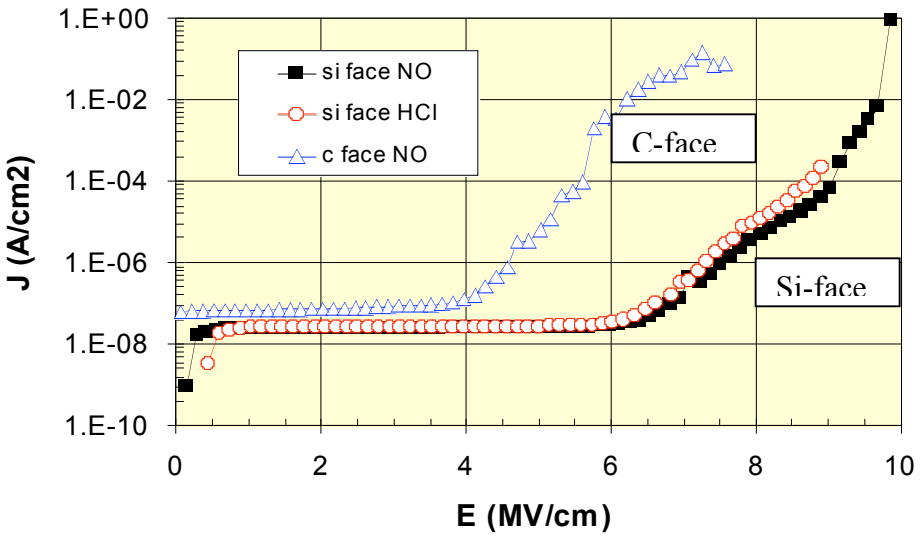


Figure 3.199 Current density versus electric field curves for passivated oxides on C-face SiC and Si-face SiC (data from L.C. Feldman, Vanderbilt University).

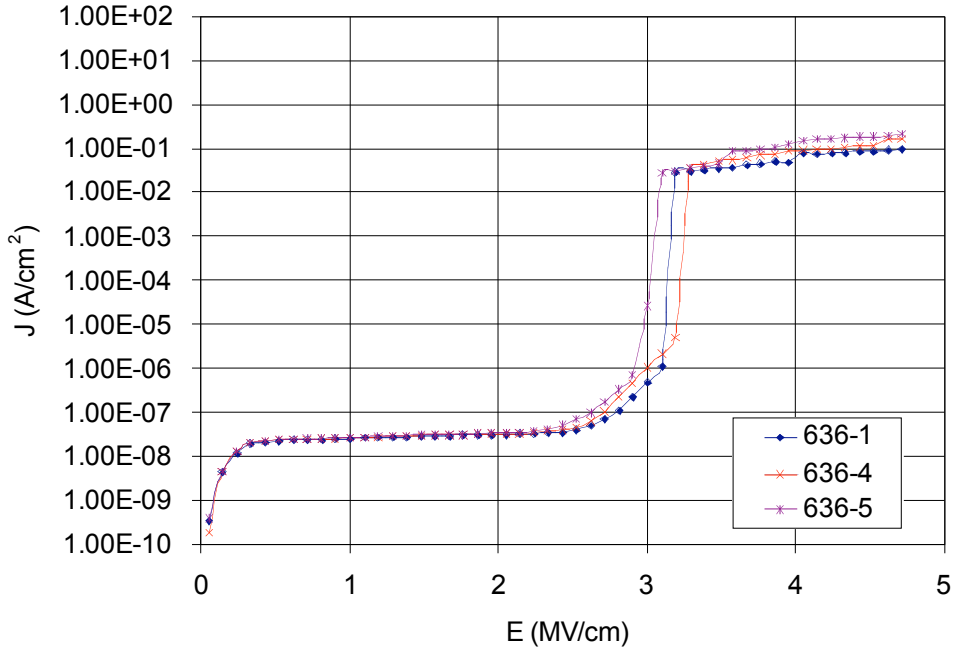


Figure 3.200 Current density versus electric field curves for passivated oxides on Al-implanted (dose=8x10^{12} cm^{-2}, annealed at 1600 ºC for 10 min in Ar) C-face SiC. Wet oxidation at 950 ºC for 17.5 min, followed by NO anneal at 1175 ºC for 2.5 hours.

The interface trap density of oxides grown on C-face SiC was studied at Auburn University. Figure 3.201 shows that for NO passivated oxides, the interface trap density of the oxide grown on C-face is generally higher than that on Si-face deep in the bandgap, but gets closer to (and even exceeds) the density on the Si-face near conduction band [24].

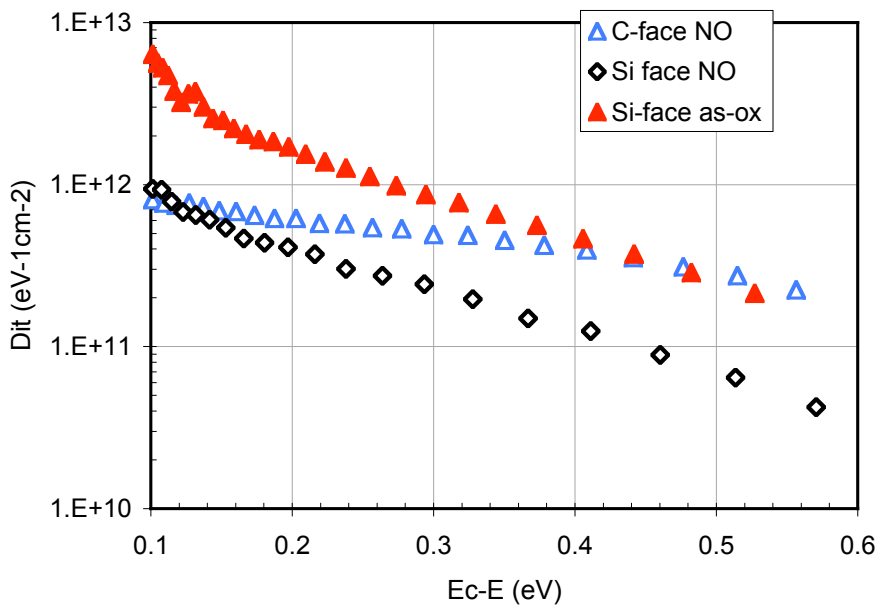


Figure 3.201 Interface trap density of oxides grown on C-face and Si-face SiC.

3.2.5 Summary of Results for the High-Voltage N-Channel IGBT

In this project we designed and fabricated high voltage n-channel DMOS IGBTs on the C-face of 4H SiC.

Three wafers (six pieces) were processed, including one 50 mm wafer grown at Purdue University and two 75 mm wafers grown at Cree. A novel "inverted growth process" was employed when the n- drift layer, n+ buffer layer and p+ anode layer of the Cree wafers were grown. The "inverted growth process" results in processing on thinned wafers, which was proved feasible by test experiments as well as the actual device fabrication.

Since the critical epi-layers were grown on the Si-face of the substrate, devices were fabricated on the C-face. Fabrication on C-face added some complications to this project. First, the oxidation rate on C-face is about ten times faster than that on Si-face. Experiments showed that the 9-hour wet oxidation at 1000 ºC in the self-aligned process could consume 150 nm of the pwell implant if the fabrication took place on the C-face. We deposited a layer of silicon nitride on top of SiC to solve this problem. Secondly, studies at Vanderbilt University showed that the breakdown field of oxides grown on the C-face was lower than that grown on the Si-face. The breakdown field could be even lower for oxides grown on Al-implanted C-face regions, according to the data from an experiment conducted at Purdue University. In the IGBT samples,

we found that the oxides on C-face were very easy to degrade. The gate oxide became leaky even after contact anneals at low temperatures. However, we could deposit a layer of LTO on top of the thermal oxide to eliminate the leakage.

Ambipolar lifetime in the n- layer needs to be large enough to obtain strong conductivity modulation in the on-state. Lifetime measurements on pieces from the Purdue wafer and one of the Cree wafer showed that the ambipolar lifetime is at least 1 μsec in these pieces.

Samples 1 to 6 had various problems. The surface of the n+ source region on sample 1 became very rough after the implant activation anneal (rms roughness= 17 nm). Almost all the devices on samples 3 and 6 and some of the devices on samples 2, 4 and 5 had "point defects", which might be caused by micromasking during patterning of the pwell implant mask. The gate oxide on sample 1 was leaky even before the contact anneal and became leakier after the contact anneal. The gate oxide on sample 2 was not leaky before the contact anneal, but became leaky afterwards. LTO was deposited on samples 1 and 2 after stripping the thermal oxides. Devices on sample 1 still did not show IGBT characteristics with LTO as the gate dielectric, though there was no gate leakage. Devices on sample 2 had gate modulated drain currents, but the currents were about four orders of magnitude lower than expected and could not be turned off at V_g=0. Sample 3 was cut into small pieces, which were annealed at different temperatures in the SiC contact annealer to study the impact of annealing temperatures on the quality of thermal oxide. We found that the oxide became leaky even after a very low temperature anneal (T=650 ºC). The oxide on sample 4 was leaky after the contact anneal (highest sample temperature was around 600 ºC), but the gate was still able to modulate the drain current. For the best devices on sample 4, the current density at a power dissipation of 300 W/cm^2 is 27.3 A/cm^2. The I-V characteristics of the IGBTs on sample 2 (before contact anneal and after LTO deposition) and sample 4 at low drain voltages resemble those of a MOSFET. This could be explained by a leakage path parallel to the p+ anode layer/n+ buffer layer junction.

For future work, first, we could improve the quality of metal contacts. Simulation shows that with better contacts (in the simulation, the contact resistivities of the p+ base contact and the n+ source contact are 5x10^{-3} ohm cm^2 and 5x10^{-4} ohm cm^2, respectively), the current density at a power dissipation of 300 W/cm^2 is 50 A/cm^2, which almost doubles the current handling capability of current device.

Secondly, we need to eliminate the gate oxide leakage. A literature search produced little information on C-face oxide quality after contact anneals. The gate oxide of the mobility MOSFET fabricated by Dr. Shurui Wang at Auburn University had a oxide breakdown field between 2 MV/cm and 4 MV/cm after the contact anneal (900 ºC, 4 min) [25]. More study is needed for us to have a better understanding of the oxides on C-face SiC.

3.2.6 Bibliography for Section 3.2

[1] Mrinal Kanti Das, "Drift Free, 10kV, 20A, 4H-SiC PiN Diodes", 2004 TMS Electronic Materials Conference & Exhibition. June 23-25, 2004

[2] B.J. Baliga, M.S. Adler, R.P. Love, P.V. Gray and N.D. Zommer, "The Insulated Gate Transister: A New Three Terminal MOS-Controlled Bipolar Power Device", *IEEE Trans. Electron Devices*, Vol. ED-31, pp.821-828, 1984.

[3] J.P. Russell, A.M. Goodman, L.A. Goodman, J.M. Neilson, "The COMFET- A new high conductance MOS-gated device", *IEEE Electron Device Letters,* Vol. EDL-4, March 1983, P.63-65

[4] Private Communications with Prof. J.A. Cooper, Jr.

[5] N. Ramungul, et al., *IEEE Device Research Conf.*, Santa Barbara, CA, June 24-26, 1996

[6] A.R. Hefner and D.L. Blackburn, "An Analytical Model for the Steady-State and Transient Characteristics of the Power Insulated-Gate Bipolar Transistor," *Solid-State Electronics*, Vol. 31, pp. 1513-1532, 1988

[7] J. Sumakeris, et al., ICSCRM 2003, Oct 2003, Lyon, France.

[8] H. Lendenmann, et al., Mat. Sci. Forum 433-436 (2003) 901.

[9] Mirnal K. Das, et al., *DARPA HPE Program Rev.,* Monterey CA, May 2004.

[10] J.R.Williams, L.C. Feldman, et al., *DARPA HPE Program Rev.,* Monterey CA, May 2004.

[11] O. Kordina et al, *Phys. Stat. Solidi (b)* 202, 321 (1997)

[12] Kordina O, Bergman J P, Hallin C, Janzen E 1996, "The minority carrier lifetime of n-type 4H- and 6H-SiC epitaxial layers", *Appl. Phys. Lett.* 69, 679-81

[13] A. Saha, et al., "A 1 kV 4H-SiC Power DMOSFET Optimized for Low On- [illegible]", *IEEE Transcations on Electron Devices*, to appear in October 2007

[14] V. A. K. Temple, *IEDM Tech. Dig*, 1977, pp. 423-426.

[15] A. Konstantinov, et al., *Appl. Phys. Lett.* **71**, 90 (1997).

[16] Sei-Hyung Ryu, et al., *IEEE Electron Device Letters*, VOL. 25, NO. 8, pp. 556-558, Aug. 2004

[17] Private Communication with Prof. T. Kimoto of Kyoto University

[18] Asmita Saha, “SiC Short Channel Power DMOSFET: an Optimized Design”, Ph.D. thesis, Purdue University, December, 2006

[19] Asmita Saha, “SiC Short Channel Power DMOSFET: an Optimized Design”, Ph.D. thesis, Purdue University, December, 2006

[20] Private Communication with Dr. Shurui Wang

[21] J. Crofton, et al., “Finding the optimum Al-Ti alloy composition for use as an ohmic contact to p-type SiC”, Solid-State Electronics 469 (2002) 109-113

[22] Yang Sui, “Development of high voltage p-channel DMOS-IGBTs in 4H-SiC”, Ph.D. thesis, Purdue University, May, 2007

[23] Kung-Yen Lee, “An Investigation of SiC Surfaces and Interfaces”, Ph.D. thesis, Purdue University, December, 2005

[24] S. Wang, A. C. Ahyi, T. Issacs-Smith, Zengjun Chen and J. R. Williams at Auburn University and S. Dhar, J. Rozen, S. K. Dixit, S. H. Choi and L. C. Feldman at Vanderbilt University, “SiO2/SiC Interface Optimization”, DARPA HPE II Final Program Review, October 25, 2006

[25] Private Communication with Dr. Shurui Wang