

Known Good Substrates – Year 1

Final Report

COTR: Dr. Colin Wood
Office of Naval Research

Contractor:
Dow Corning Corporation
Dow Corning Compound Semiconductor Solutions
Midland, MI 48686

Period of Performance: December 2005-April 2007

Contributors:

M.J. Loboda (Technical Point of Contact), E.P Carlson (Principle Investigator), G. Chung (Principle Investigator), D.H. Hansen, C.L. Parfeniuk

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number. PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.				
1. REPORT DATE (DD-MM-YYYY) 12-05-2007		2. REPORT TYPE Final Report		3. DATES COVERED (From-To) 12-01-2005 to 04-30-2007
4. TITLE AND SUBTITLE Known Goods Substrates Year 1 Final Report		5a. CONTRACT NUMBER N00014-05-C-0324		
		5b. GRANT NUMBER		
		5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S) Loboda, Mark; Carlson, Eric; Chung, Gilyong; Russell, Brian		5d. PROJECT NUMBER		
		5e. TASK NUMBER		
		5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Dow Corning Semiconductor Solutions, LLC 2200 West Salzburg Rd, P.O. Box 994 Midland, MI 48686-0994		8. PERFORMING ORGANIZATION REPORT NUMBER N/A		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS Office of Naval Research 875 North Randolph St. Suite 1425 Arlington, VA 22203-1995 Attn: Colin Wood, Code : 312		10. SPONSOR/MONITOR'S ACRONYM(S) ONR (Office of Naval Research)		
		11. SPONSOR/MONITOR'S REPORT NUMBER(S)		
12. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified/Unlimited				
13. SUPPLEMENTARY NOTES				
14. ABSTRACT: The Known Good Substrates (KGS) Phase I program is complete. Results are reported for the entire program, including subcontractor activities.				
15. SUBJECT TERMS SiC wafer, SiC epi, SiC material metrology				
16. SECURITY CLASSIFICATION OF: U			17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES 60
a. REPORT U	b. ABSTRACT U	c. THIS PAGE U		
				19b. TELEPHONE NUMBER (989) 496-6249

Office of Naval Research
Dow Corning Corporation
Known Good Substrates Year One program December 2005-April 2007

Executive Summary

The first period of performance corresponding to 2005 ONR fiscal year funding of the Dow Corning Compound Semiconductor Solutions (DCCSS or CSS) “Known Good Substrates” research program was conducted during the period 12/2005 to 4/2007. The program team consisted of Dow Corning, Naval Research Laboratory, Northrup Grumman, Semiconductor Technology Research, Carnegie Mellon University, State University of New York at Stony Brook, University of Alabama, University of South Carolina, Arizona State University and Fred Dall Consulting. A key objective of the program was to establish the foundation for a production line capable of producing repeatable device quality 4H SiC wafers and epitaxy, at crystal/wafer diameters 76mm to 100 mm. The key focus of the program was improvement of 76mm diameter 4H SiC substrates and epitaxy, and assessment of performance metrics using statistically large data sets and wafer mapping metrology.

During the program micropipe defect density in Dow Corning 4H-SiC was significantly reduced, meeting published objectives. SiC homoepitaxy processes using chlorosilane based chemistry were shown to yield record setting carrier lifetime values and very low concentrations of point defects. Epiwafers delivered for fabrication of RF static induction transistors showed operational devices yields equivalent to that obtained using wafers from legacy SiC suppliers. First generation 100mm 4H SiC n⁺ wafers were demonstrated. A new process for gas phase crystal growth using chlorosilane precursors was also developed and demonstrated.

In the last third of the program Dow Corning initiated efforts to create a step change improvement in 76mm diameter 4H SiC crystal quality. Early results show that the further reduction of micropipes and grain boundaries can be realized with this “second generation” crystal growth methods. The demonstrated improvement motivated Dow Corning to re-start its 100mm crystal growth effort to incorporate the improvements in that effort.

In year two of the Known Good Substrates Program, Dow Corning will focus to qualify and deliver wafers generated using second generation SiC crystal growth technology in the first half of the program, and deliver sample quantities of epiwafers to device fabrication partners for evaluation in the second half of the program. Schottky barrier diodes, RF-SITs and PiN diodes will be used to evaluate the quality of the SiC substrates. Efforts will continue to drive correlations between the within wafer distribution of device properties and the within wafer distribution of crystal defects and material metrics.

Key Results by Program Task:

Task 1 SiC Wafers Products

Task 1 required Dow Corning produce statistically significant quantities of 76-100 mm diameter SiC wafers for use and consumption in the program. The wafers are required to support all or part of Task 2 Materials Applied Research, Task 3 Metrology for Wafer Specification, and Task 4 Device Technology Maturation. The task has no labor component.

Sub-tasks for Task 1 include:

- **Task 1.1 - 76 mm PVT/CVD SiC Crystal HVM Wafer Fabrication:** Provide 4H n+ wafer substrates for use in the program..
- **Task 1.2 – 100 mm PVT SiC Crystal HVM Wafer Fabrication:** Provide 4H SI wafer substrates for use in the program.

Within the scope of this effort, projects conducted with Dow Corning Compound Semiconductor Solutions (“DCCSS”) IR&D funds were focusing on key process and improvements aligned to well accepted SiC industry materials cost reduction initiatives. Areas of focus committed to the KGS program included

- Deliver first generation 4H n+ 100mm wafers
- Timing for 4H 76 mm diameter – produce at a rate of >30 crystal growth starts/quarter at the end of program quarter 1.
- Timing for 4H 100 mm diameter - produce at a rate of >30 crystal growth starts/quarter at the end of program quarter 5.

The basis of growths originally proposed were 75% n+ and 25% SI. An early Q1 task was to finalize the distribution of resistivity types to be prepared under the program. Kickoff meeting discussions resulted in testing and device fabrication plans that required a majority of n+ substrates, and these became the focus of the growth work. Unintentionally doped crystals were still grown during the program as a means to develop a process for semi-insulating substrates, but only a few wafers from these growths were targeted as deliverables.

SiC crystal growth work for this program started in January, 2006. Figure 1 shows a bar chart of the monthly 76mm diameter 4H SiC crystal growth starts for the period Oct 2005 to Feb 2006, which shows the baseline performance in 2005, prior to the KGS program work.

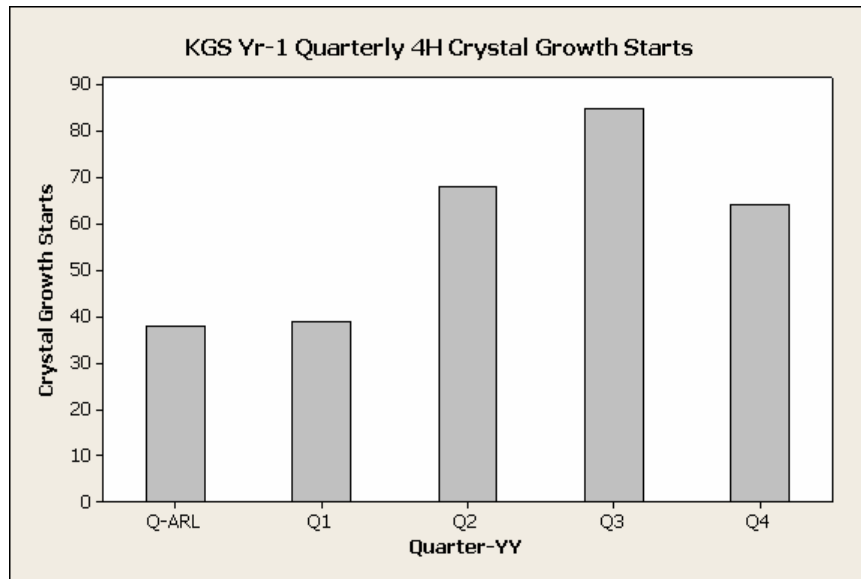


Figure 1: SiC crystal growth starts by quarter.

Figure 2 shows a bar chart of the monthly 76mm diameter 4H SiC crystal growth starts for the period Oct 2005 to Feb 2006 by resistivity type, n+ or UID.

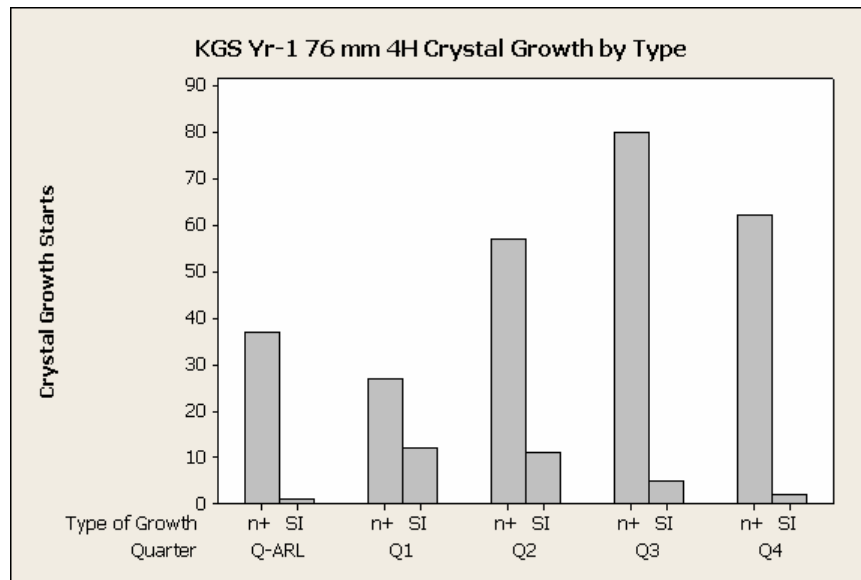


Figure 2: SiC crystal growth starts by resistivity type and quarter

Appendix 4 lists the wafers expended to the program and their current disposition. Numerous additional wafers were supplied at expense to Dow Corning for use in subcontractor efforts.

Task 2 Materials Applied Research

Task 2 focused on tasks related to the materials applied research aspect of the program. Each quarter, analysis of wafer fabrication and defect yield loss using Pareto analysis techniques was performed. Based on these results the PVT growth process and/or the wafer fabrication process was adjusted and applied in the subsequent quarter in an attempt to reduce the sources of the failures.

As an alternative means to growth of high quality 4H SiC crystals, DCCSS embarked on the development of a prototype process for gas fed crystal growth process using technology based on CVD growth.

Sub-tasks related to Task 2 include:

- **Task 2.1 – 76 mm PVT SiC Crystal HVM Wafer Pilot:** Research and development for improvements to the 76 mm PVT process. Work focused on modeling the process for longer (50 mm) boules and on improved furnace uniformity (adding rotation, etc.). Pareto analysis was performed on wafer yield loss at the start of every quarter and a technical plan generated to address the top failure issues.
- **Task 2.2 – 100 mm PVT SiC Crystal HVM Wafer Pilot:** Research and development for 100mm PVT process. Work focused on modeling the process for longer (50 mm) boules and on improved furnace uniformity. Pareto analysis was performed on wafer yield loss at the start of every quarter and a technical plan was generated to address the top failure issues.
- **Task 2.3 – 76 mm CVD SiC Crystal Growth Development:** Chemical and physical modeling of 76 mm CVD bulk crystal growth was performed. A PVT furnace was converted to a CVD process based on the output of the modeling.
- **Task 2.4 – Batch SiC Epitaxy 75mm & 100mm Wafers:** SiC homoepitaxy was applied on the majority of the wafers produced in Task 1.

Within the scope of this effort, projects conducted with Dow Corning Compound Semiconductor Solutions focusing on key processes to establish improved capability and reduce defects. Focus areas included:

- Complete effort started at DCCSS in 2005 to mathematically model 76 and 100 mm diameter SiC PVT growth
- 50%-80% sliced off cut wafer increase per crystal for 4H 76 mm diameter crystals
- Reduce the sum of 76mm 4H n+ MPD and opaque inclusion density to a median(30th percentile) value less than 30(10) cm⁻²
- Wafer scratches (total length), visual inspection (Dark field microscopy, 100x magnification) to a median (30th percentile) value of 75%(50%) of one wafer diameter.
- Areal density surface particles and pits in epiwafers, equivalent diameter >0.5 um to a median(30th percentile) value less than 10(5) cm⁻²
- Total impurity bulk metals concentration [B, Al, Ti, V, Fe (atoms/cm³)] to a median(30th percentile) value less than 5(1) x 10¹⁵ atoms/cm³
- Stable Epi drift layer carrier concentration (atoms/cm³) to a median(30th percentile) value less than 5(1) x 10¹⁴ atoms/cm³

- Epi thickness uniformity to a median(30th percentile) value less than 10%(8%) sigma/mean.
- Epi Doping Uniformity (1015-1019/cm³ layers) to a median(30th percentile) value less than 15%(10%) sigma/mean.

Modeling of the PVT Process

Modeling of the 76 and 100 mm physical vapor transport process was performed using STR's "Virtual Reactor" software. DCCSS personnel developed a baseline model for the growth process using the standard software. The 76 mm growth model and experimental data were transferred to STR where the STR staff then refined the model by incorporating additional capability. STR focused on the following key facets of the 76 mm growth process in order to tune the model to match the experimental data:

- SiC source material evaporation process and its real-time influence on the mass transport
- Impact of the thermal conductivity of the graphite crucible
- Impact of the porosity of the graphite crucible and its influence on the escape of source vapors and thermal gradients.

Initial work established that the mass transport model could closely reproduce the experimental final crystal shape and the terminal growth rate (crystal height at end of growth cycle divided by growth time). This was achieved through the tuning of the facet formation and adding porosity to the graphite crucible. Yet at the same time, the properties of the source residuals were not consistent with the experimental observations.

The focus shifted to further comparison of models of source evolution – the SiC source can be modeled using either bulk sublimation or surface sublimation. The bulk sublimation model represents the real process of SiC source graphitization characterized by formation of SiC core covered by graphitized shell. The surface sublimation model assumes the source porosity to be negligible so that the source is impermeable for the active species, there is no mass sublimation in the source bulk, and the evaporation occurs only on the source external surface that moves during the growth. Under the same process conditions and the same model parameters, the bulk sublimation technique yields more source residue at the end of the growth cycle compared to the surface evaporation approach and the boule height exceeds the experimental value. At this time, the crucible porosity (pore radius and pore density) emerged as a key parameter to account for the source material losses in the model. What's more, as source vapors react with the crucible, the crucible degrades and its thermal properties are affected. It is evident that these factors needed to be coupled to model both the crystal growth and source decomposition accurately.

Further tuning of the model to represent source losses, coupled with adjustments for the thermal conductivity of the crucible were successful to realize congruency between experiment and model. Conclusions key to this result are as follows:

- Material loss through porous graphite of the crucible combined with crystal faceting threshold angle allows accurate adjustment to experimental data.

- Coil vertical position proved to be a good additional parameter for model adjustment. In the Virtual Reactor software, 3D helix coil is approximated with 2D coil which leads to some uncertainty in its position. A major learning here is the high impact of coil position and shape irregularities on the crystal growth.
- Computational model can be adjusted to the experiment for different thermal properties of the crucible graphite.
- Higher graphite thermal conductivity provides better heating of the source bulk which results in more realistic shape of the SiC source residue.

In parallel with this work, modeling efforts at DCC focused on an initial model for expansion of the crystal diameter in order to support development efforts to grow 100mm crystals. A key issue was that the crucible design approach used at DCCSS in the 2003-2004 periods was inadequate for the 100mm expansion project, as the formation of polycrystalline SiC was routinely observed experimentally in the legacy design. In particular the effort focused to model the stresses and growth along the expansion direction. The model indicated that above a critical diameter expansion/crystal length ratio the formation of polycrystalline SiC was favorable. The results of this work formed the basis of the initial crucible design for expansion work. Iterations of the model and experiment were performed and a new crucible design capable of efficient expansion emerged. Growth rate, crystal weight and source efficiency can now be modeled to within 5-10% of the experimental data.

Several key actions are going forward as a result of this effort:

1. DCCSS and STR will work to continue to better understand the impact of the coil on the growth process, particularly the reproducibility. In KGS year 2 an additional subcontractor will be added to the team, bringing considerable experience in induction heating and coil design.
2. DCCSS will embark to characterize the graphite porosity to confirm the values required in the model to achieve congruency with experimental data.
3. New capabilities and model attributes identified for 76mm growth now must be transferred to 100 mm growth modeling.

Pareto Analyses and 4H SiC Crystal Growth Effort

The following failure modes were used as categories for failure analysis at the crystal growth level:

- PVT growth execution failure (useable crystal boule not produced)
- Crystal machining mechanical failure (conversion of raw crystal to sliceable crystal)
- Crystal quality inspection failure (non-4H polytype, excessive inclusions, etc)
- MPD >30/cm²
- Good crystal, micropipes <30/cm².

Figure 3 shows the quarterly crystal growth progress as viewed from Pareto data:

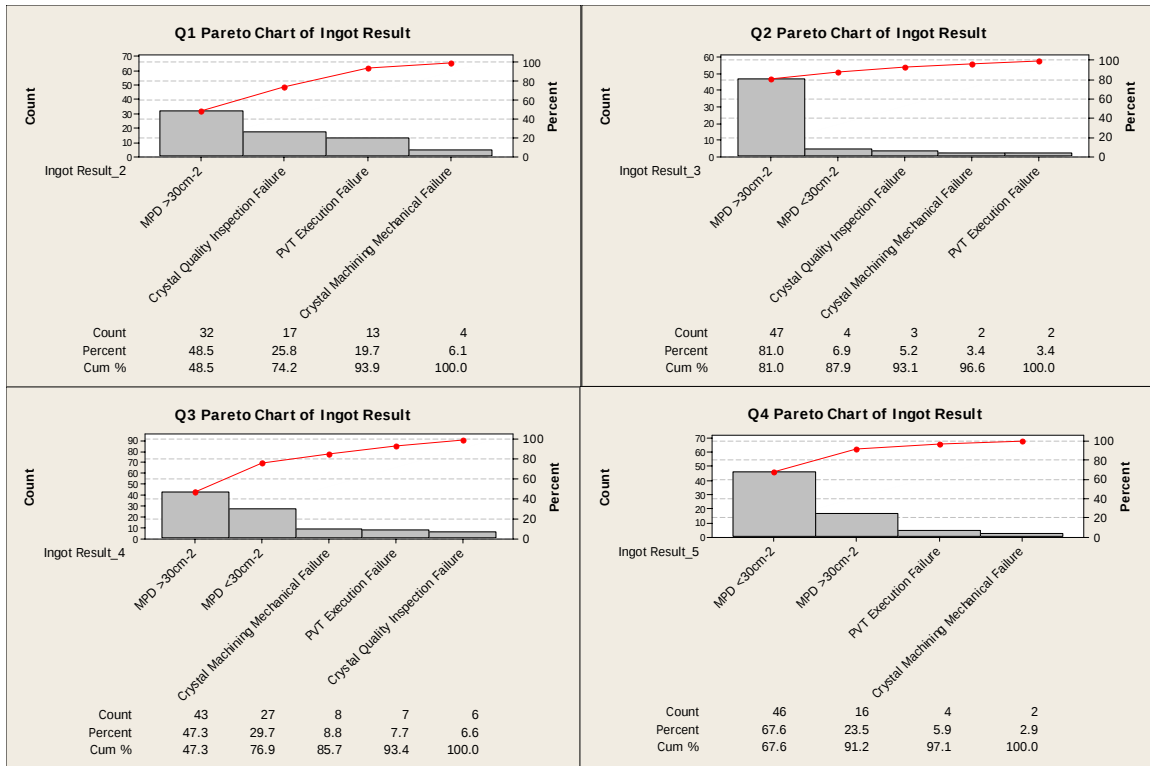


Figure 3: Quarterly SiC crystal growth Pareto analyses.

Figure 4 shows the chronological evolution of the 4H n+ SiC crystal growth effort as extracted from the quarterly Pareto analyses:

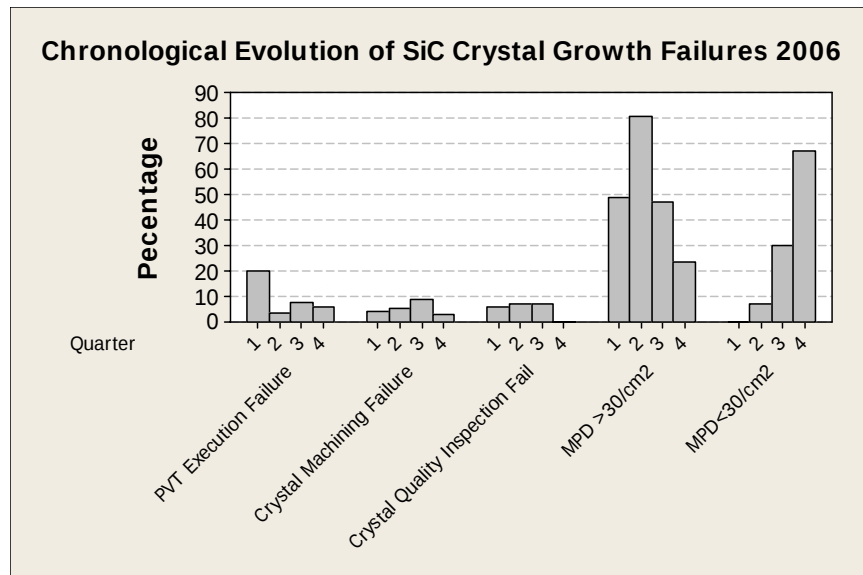


Figure 4: SiC growth Pareto analysis by category.

Pareto analysis results of the 4H n+ SiC growth process drove primary development efforts to focus on MPD reduction over the KGS year 1 effort. Steady improvement was achieved on a quarter by quarter basis. The improvements in MPD were achieved through implementation of:

- Improved seed crystal inspection and selection (Q1).
- Improved seed preparation (Q2-Q3).
- Modification of the PVT growth nucleation sequence (Q2-Q3).
- Adjustment of the growth cell design to create improved temperature uniformity and favorable vapor chemistry conducive to MPD reduction (Q3-Q4).
 - Improved polytype stability was achieved

The quarterly distributions for MPD are shown in Figure 5, based on a 3 mm edge exclusion (outer region where micropipes are not counted)

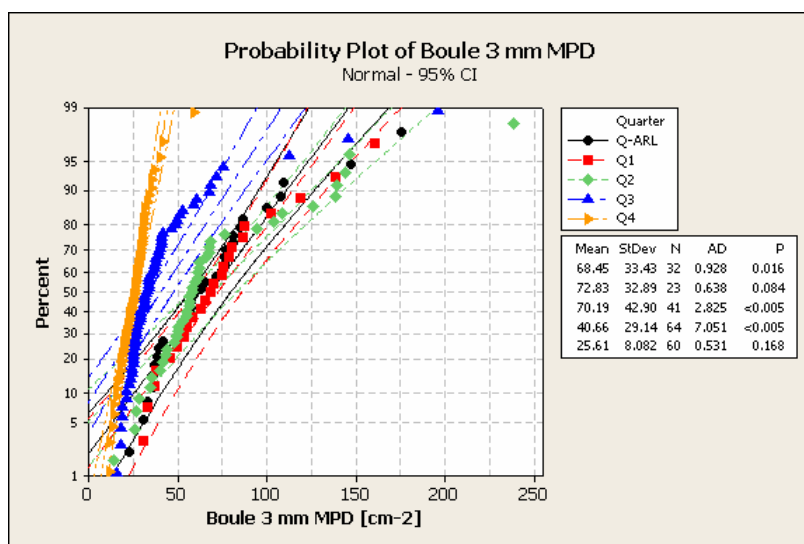


Figure 5: Distribution of micropipe density measured on 76mm 4H SiC crystals broken out by program quarter. The baseline quarter (prior to program start) is labeled Q-ARL.

Significant improvement in ability to reduce micropipe density emerged in Q3.

As a result of these efforts, a very consistent pattern of MPD reduction has emerged. This is shown graphically in Figure 6. The graph shows not only is the MPD value declining, but also the distribution is reducing. This “roadmap” predicts that at this development rate, MPD<5/cm2 will be routinely achieved in 2008. A 1 mm edge exclusion was used for this projection.

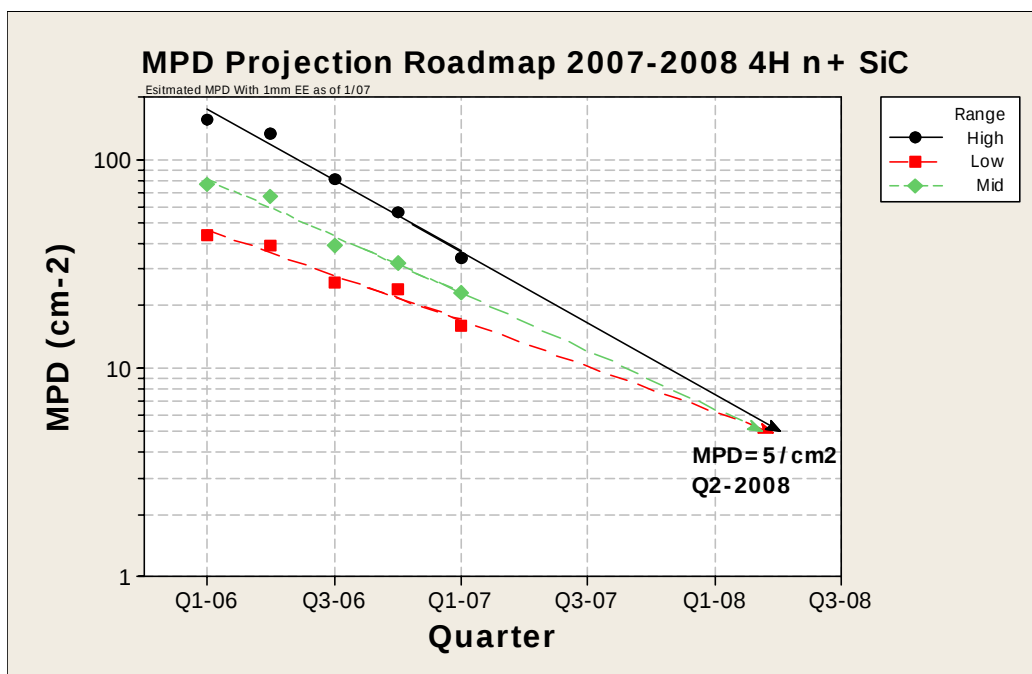


Figure 6: Micropipe reduction trendline for 76mm 4H SiC n+ crystals.

Crystal quality failures assessed at post growth inspection were also significantly reduced during the program. A separate change in the growth cell design in Q2 and improved seed mounting reduced the occurrence of crystals with excessive evaporation voids, cracks and polytype errors.

Along with micropipe defects, opaque inclusions in the wafers are a killer defect for device yields. Opaque inclusions encompass carbon inclusions which emerge from the formation of evaporation cavities at the backside of the seed during PVT growth, from localized carbon condensation or from hexagonal plate defects formed during crystal growth. These opaque inclusions lead to the formation of surface depressions during polishing and also impede step flow during epitaxial layer growth, resulting in crystalline surface defects formed in the epitaxy process. The sum of opaque inclusions and micropipes in the polished wafer is a better metric of defect impact on yield compared to micropipes alone.

Wafers with gross levels of opaque inclusions are removed from processing in early inspection steps following wafer slicing using a 1x visual inspection. These wafer sliced are not polished.

Opaque inclusions were assessed in this program using a 100x bright field visual microscope inspection on polished wafers. Sixteen sites were examined, four points on circles at four radius values on the wafer. The counting process counts all opaque defects, and can include micropipes. Defects were summed and converted to an equivalent defect density of opaque defects.

Figure 7 shows the quarterly distribution of opaque defect density measured on wafers.

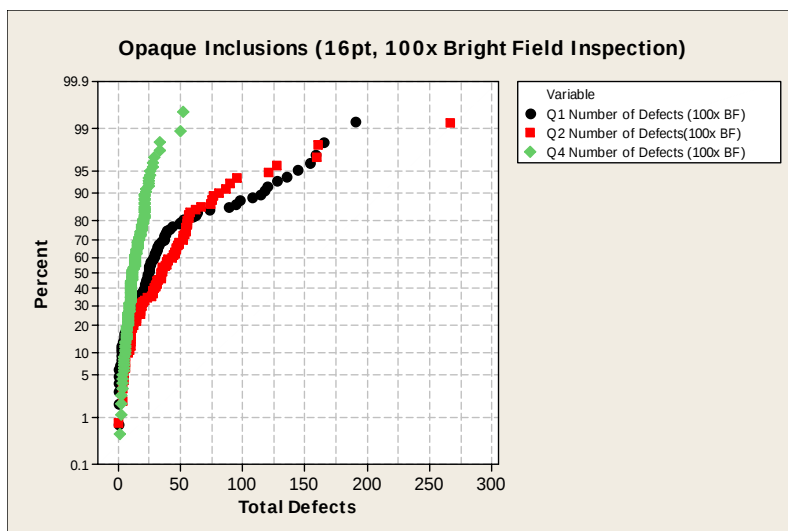


Figure 7: Probability chart plotting the quarterly distributions of opaque inclusions in 76mm diameter 4H n+ SiC wafers.

The defect densities corresponding to the data in the figure are 54/cm², 61/cm², and 20/cm² for Q1, Q2, and Q4, respectively. Q3 crystal data is lumped with Q4 as wafers from both quarters were tested in Q4 of the program.

A sub-task in the program was to develop and mature a 100 mm diameter 4H SiC crystal growth process. This process started with seed wafers of approximately 70mm diameter and using crystal diameter expansion methods incrementally expanded the diameter to yield 100 mm wafers.

Figure 8 shows a bar chart of the monthly 4H SiC 100mm program expansion crystal growth starts for the period Jan 2005 to Nov 2006 and the diameter progression as a result of crystal expansion growths by month for the period Jan 2005 to Nov 2006.

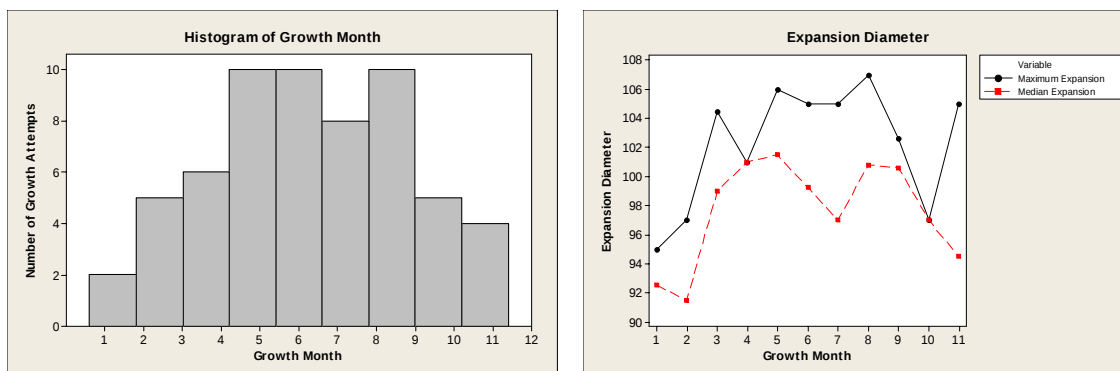


Figure 8: Growths and diameter progression for 100mm diameter 4H n+ SiC.

While the program succeeded to deliver samples of 100 mm wafers, from the end of Q3, the wafer edges had a larger than desirable concentration of low angle grain boundaries. This can be observed in the stress birefringence images in Figure 9.

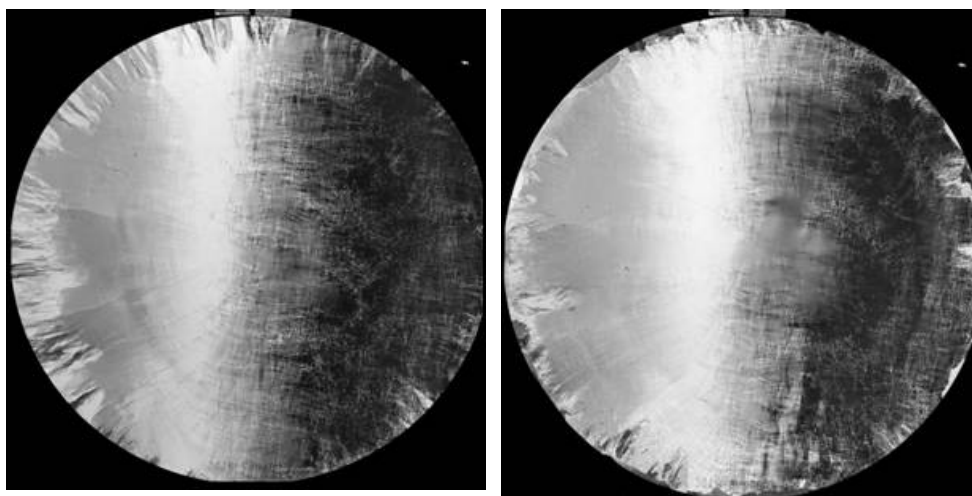


Figure 9: Stress birefringence images of 100mm diameter 4H n+ SiC wafers delivered in the program.

Progress in 76mm 4H SiC crystal quality improvements offered a means to improve the seed feedstock for 100mm processes. Early in the fourth quarter a decision was made to re-start the 100mm crystal expansion effort in order to improve the overall crystal quality of the 100mm wafers. This decision resulted in a delay in the ability to execute growth starts >30/quarter by Q5 of the program. It is expected that the second generation of expansion work will be completed by June 2007, and wafer growth ramp to 30/quarter can initiate at that time if the seed quality is consistent with the crystal quality goals.

Step change improvement to reduce crystal defects in Dow Corning SiC crystal growth processes is critical to deliver material meeting device yield goals. Two approaches to achieve step change improvements used in this program are 1) gas source crystal growth

and 2) a second generation PVT growth method focused on controlling vapor composition to reduce micropipes. The gas source crystal growth is discussed later in this report.

Second generation PVT processes were explored in the latter part of the year one program to support capability development for low MPD ($\text{MPD} < 10/\text{cm}^2$) 4H SiC crystals. The second generation process employs the best learning from 2006 PVT work and adds radically new growth process conditions.

Figure 10 compares stress birefringence images of seed crystals from the generation 1 PVT process and wafers from crystals grown on these seeds using the generation 2 PVT processes. The seeds and the wafer from the crystal grown on the seed are aligned in the figure.

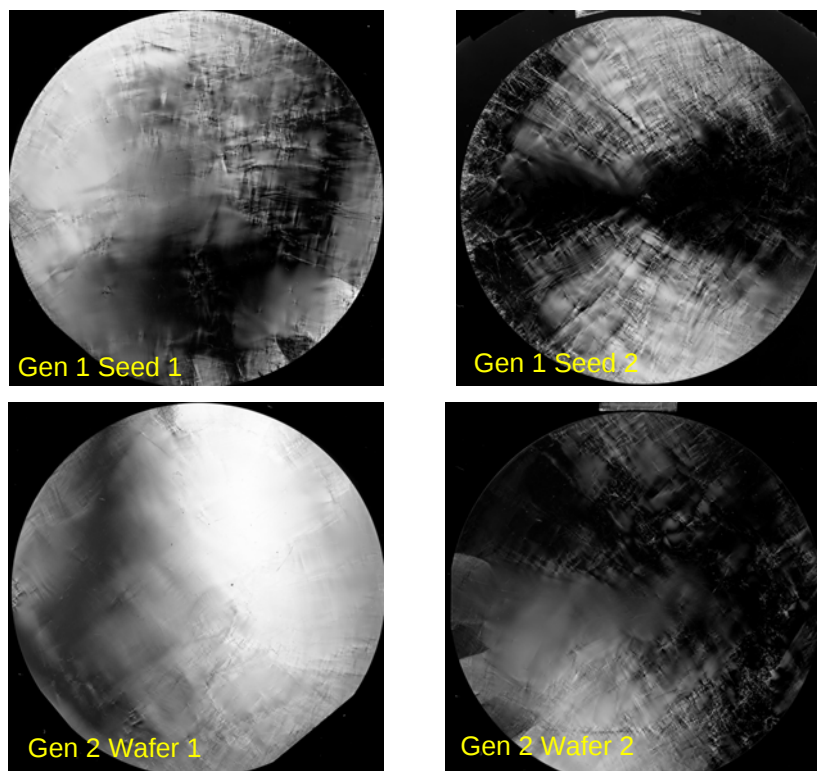


Figure 10: Stress birefringence images of 76mm 4H n+ SiC wafers made using successive generations of PVT growth processes. Wafer was extracted from the crystal grown on the seed imaged above.

Comparison of the top and bottom images on the left and right of the figure show that the approach used in the second generation PVT process can reduce the highly defective regions of the seed which link to zones of high birefringence. The second generation PVT process results in an improved capability to reduce the micropipe density from the seed to

the new crystal, resulting in reduced MPD over 70% of the time compared to 50% of the time in the generation one process. This is exemplified in Figure 11, where the generation two process is the only process to have a mean corresponding to MPD reduction relative to the seed crystal.

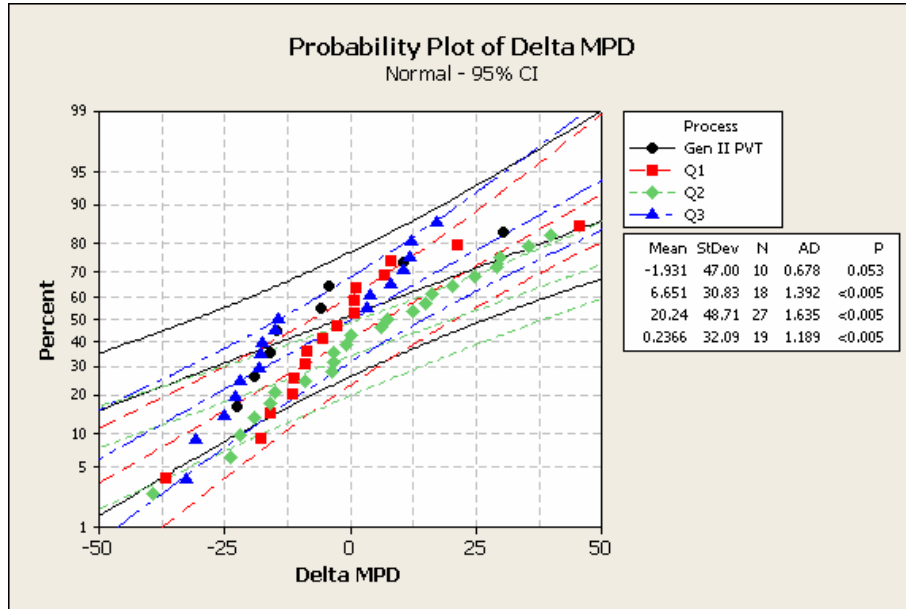


Figure 11: Change in micropipe density distributions for quarterly PVT growth of 76mm 4H n+ SiC and the Generation II PVT Process.

Generation Two PVT also demonstrates the ability to significantly improve the resistivity uniformity in 4H n+ wafers. A comparison of the PVT processes is shown in Figure 12.

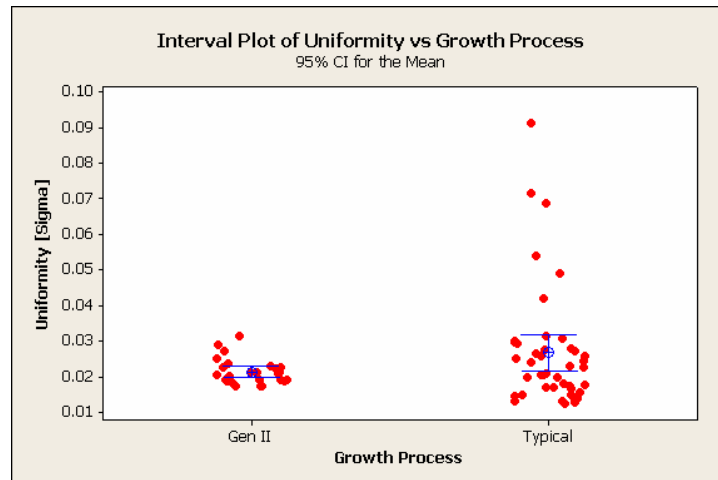


Figure 12: Boxplot comparison of within wafer resistivity uniformity of 76mm 4H n+ wafers grown using the legacy and second generation PVT processes.

Efforts at the end of year one and the start of the year two KGS program will focus to mature the second generation PVT process for delivery of wafers to the program.

Limited effort was reserved in the KGS program to explore new PVT processes to grow undoped 4H boules targeted for applications requiring semi-insulating substrates. The approach used at Dow Corning focuses on the production of ultra-high purity SiC crystals, where the goal is to reduce the concentration of nitrogen, along with the concentration of all metallic impurities to less than $5E15/cm^3$. Later in this report it will be shown that Dow Corning has been successful to lower the metallic impurities, including boron, to the target levels. Modification of the PVT process and system has shown a consistent trend to reduce nitrogen as well. This is shown in the Figure 13.

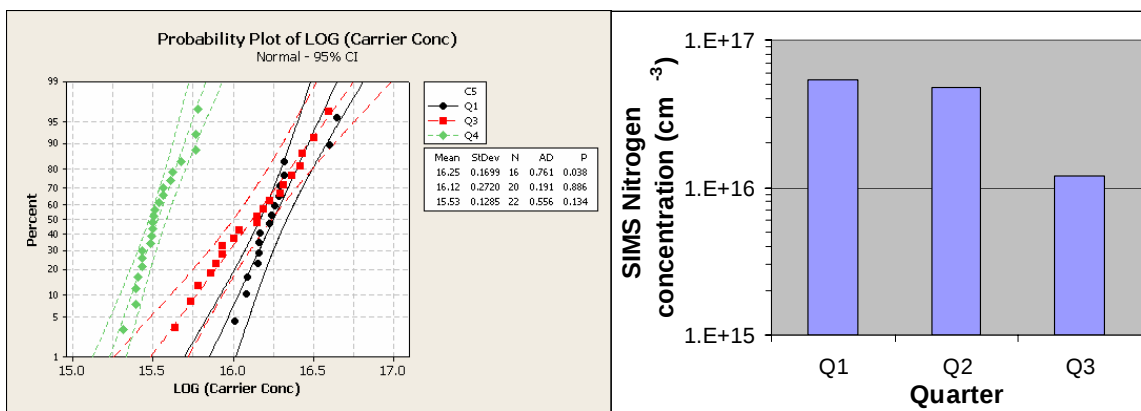


Figure 13: Quarterly distributions of net carrier density and sampled nitrogen concentration by SIMS for undoped 76mm diameter 4H SiC crystals.

Current process capability in the third quarter corresponded to a nitrogen concentration of $1E16/cm^3$ – measured by capacitance voltage testing (left figure) and by SIMS (right figure). IR-PL data measured on undoped SiC wafers from Dow Corning shows that at $1E16/cm^3$ nitrogen concentration, key defect bands indicative of near semi-insulating performance emerge (Figure 14) indicating that another factor of two reduction in nitrogen should result in semi-insulating electrical performance.

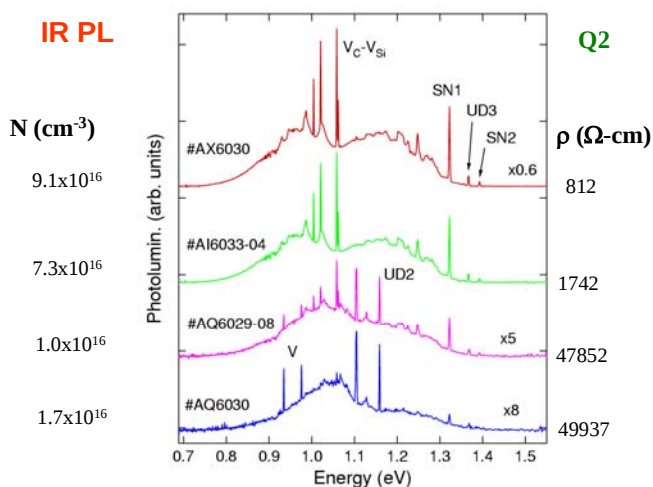


Figure 14: Photoluminescence spectra measured on undoped 4H SiC wafers produced in Q2 of the program.

In the fourth quarter net doping levels corresponding to a mean of $3.4E15/cm^3$, which is three times lower than the third quarter, were achieved. Some regions of these crystals resulted in semi insulating performance, but the overall concentration of nitrogen

“Monotonic Decrease of V_C-V_{Si} , SN1, and SN2 with $\uparrow \rho$ ($\downarrow [N]$)”

was still above the target. The trends in nitrogen reduction and electrical behavior support that the process strategy can inevitably deliver semi-insulating SiC. The current furnace and process is at a limit requiring physical modification to achieve the next level of nitrogen reduction. The modification will be complete by April-May 2007 timeframe, and work on the final nitrogen reduction step should resume at that time.

Pareto Analyses and 4H SiC Wafering Efforts

The following failure analyses were applied in the wafering process flow:

- Failure Post Slice (mechanical or crystal defects)
- Failed in Lap (cracks, breakage, chipping)
- Other Failures/Failed in Polishing (scratches, cracks, breakage, chipping)
- Good polished wafers

Figure 15 shows the Pareto trends related to crystal slicing and polishing of 4H n+ SiC wafers.

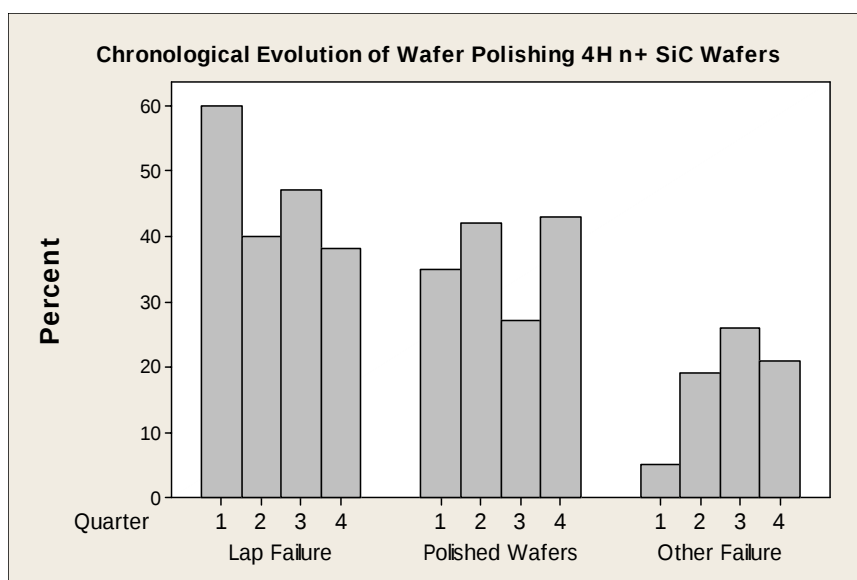


Figure 15: Pareto analyses of the 4H SiC wafer inspection and fabrication process.

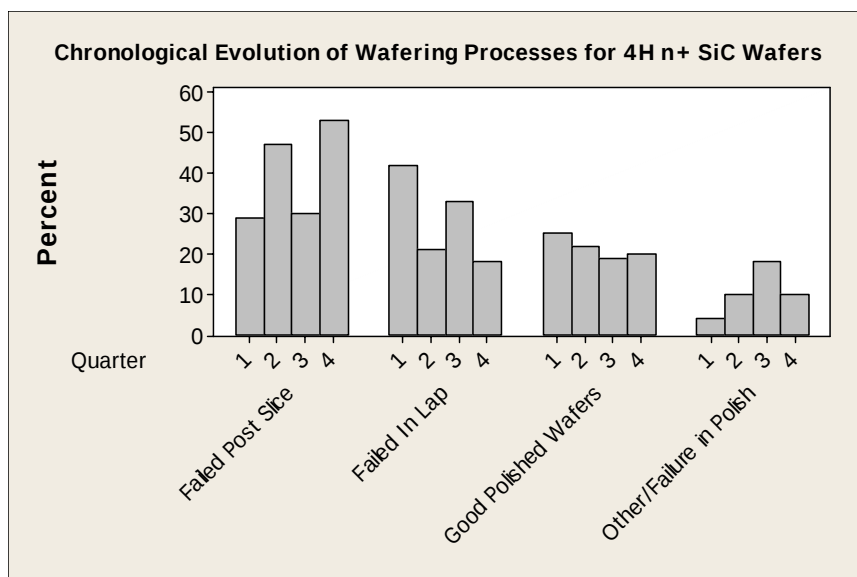


Figure 16: Pareto analyses of the wafering process with focus only on wafering failures

Averaged over the program period, about 40% of wafers were not sent on to lapping and polishing from the slicing process. The particular failure modes assessed post slicing were either related to evaporation cavities (seed attachment defects), polytype failures, excessive crystal defects, chips or sliced wafer warp. The second largest failure mode was breakage or chipping during lapping of the wafer.

Figure 16 shows similar data, except with the post slice failures removed. Process limitations with sliced wafer warpage and excessive crystal imperfection at the wafer edge persisted during the program period. The warpage of the sliced wafers was significantly reduced by new processes implemented in Q3 for annealing of the 4H n+ SiC material. At the end of the third quarter, significant problems with polishing systems resulted in considerable polishing failures. Many wafers sliced in the third quarter were held to the fourth quarter for completion of processing. Equipment issues were resolved at the end of 2006 and wafer polishing was completed in early 2007.

While not a deliverable metric of performance in the KGS effort, wafer shape and its evolution during polishing is a key measure of crystal quality and an important parameter for epitaxy. Figure 17 shows the thickness, TTV, bow, and warp distributions of batch processed wafers on a quarterly basis.

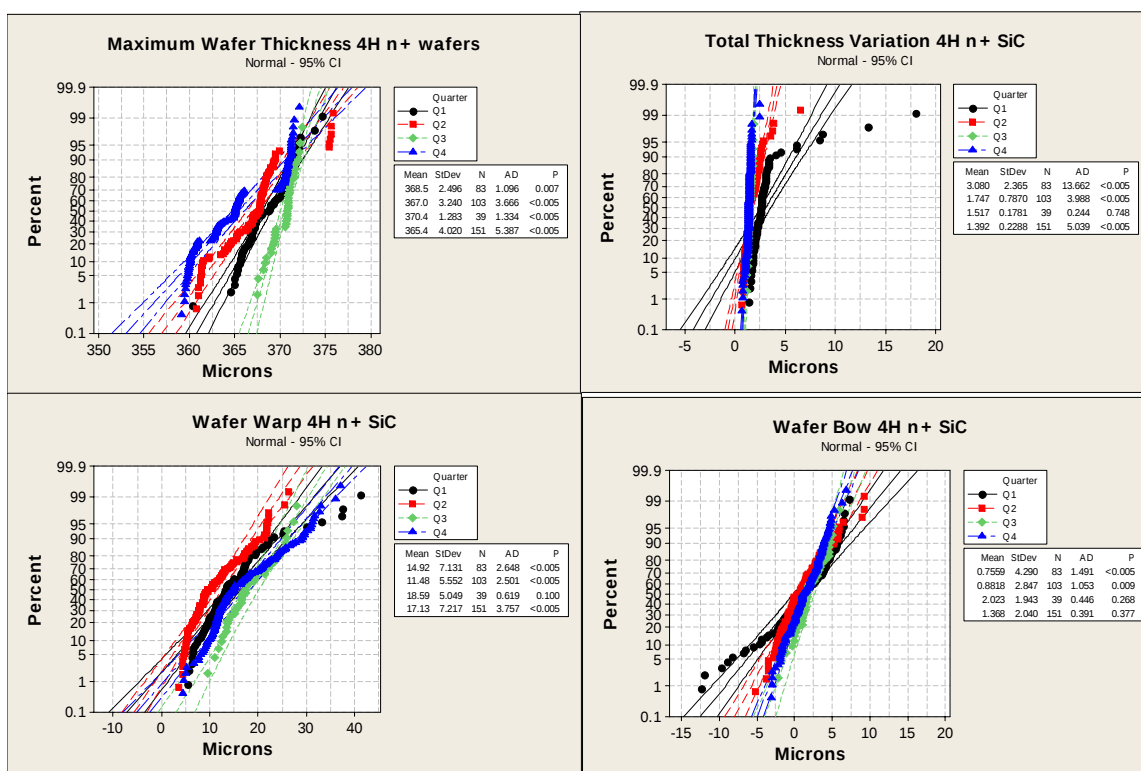


Figure 17: Quarterly distributions of wafer shape parameters measured on polished 76mm diameter 4H n+ SiC wafers.

Wafer shape distributions for 76mm diameter 4H n+ wafers are very consistent quarter to quarter. The wafer shape values meet the requirements for use in stepper lithography systems required for fabrication of designs with submicron features.

Defects can emerge during the polishing process. In particular surface pits and scratches can lead to the formation of defects in the epitaxial layer which in turn will limit device yield. The goal of the year 1 effort was to reduce polishing scratches on the silicon face to less than the diameter of the wafer. This was achieved in Q2 of the program.

Both laser light scattering (LLS) and 100 x dark field microscope visual inspections of the silicon face were used to assess scratches and pits on post polished wafers. An algorithm was developed to segregate the pits by their area. Closer inspection of scratches reveals that often the defect is a trail of pits. Since the bottom of a scratch is not even, as polishing action works on a scratch it leaves a train of pit defects which are the deepest parts of the scratch. Because of this the LLS measurement system has a difficult time to assign scratch defects. Figure 18 shows an example of a LLS defect map with scratches and pits. Clearly some of the pits identified are part of the scratch trail.

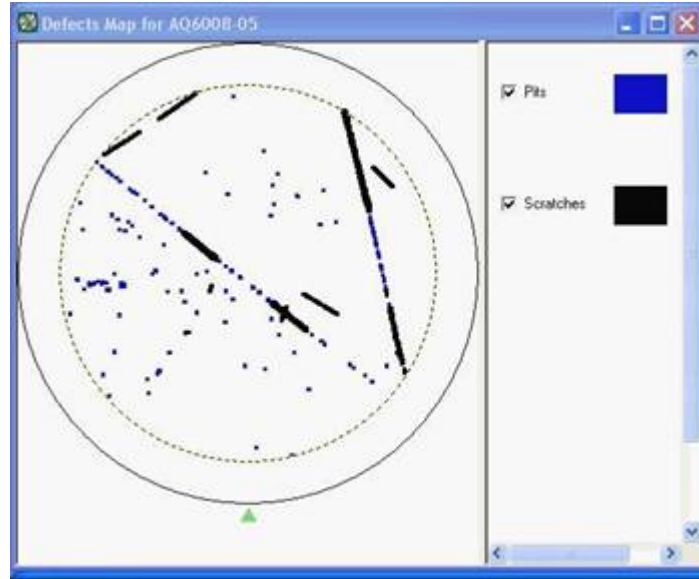


Figure 18: Example of a LLS scratch and pit defect map measured using the Candela C2 system.

The best method available to the program was to assess scratches from a topographic wafer image obtained from the LLS test. This is discussed in the Metrology section of the report. Using this method, congruency was achieved between LLS and visual inspection tests of wafer surface scratches.

Figure 19 shows the distribution of scratch length measured on LLS topographic wafer maps by quarter.

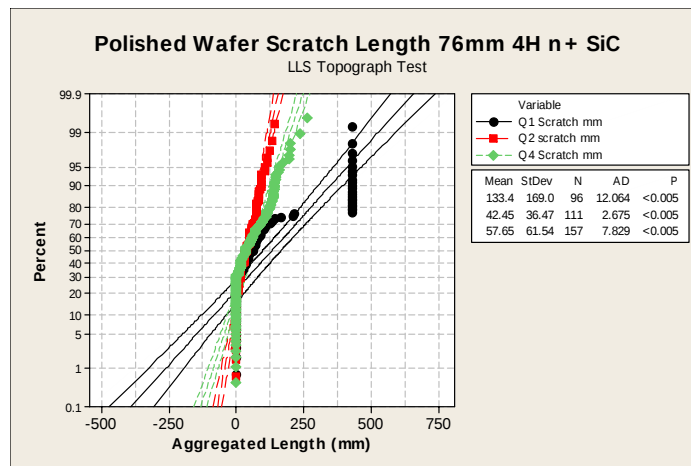


Figure 19: Quarterly distribution of scratch lengths measured by LLS on polished 4H n+ SiC wafers.

Due to equipment issues wafers were not polished in Q3. The distribution of scratch lengths Q2-Q4 were 50% of wafers <36mm length and 30% of the wafers <19 mm. These values exceed the program goals.

In the LLS test, pits are binned according to a defect area. The defect area is equated to effective diameter by setting it equal to the area of a circle. The bin ranges and effective diameters are shown in the table below:

	Area(μm^2)	Upper Diameter (μm)	Lower Diameter (μm)
Bin 1	500	36	25
Bin 2	1000	50	36
Bin 3	2000	62	50
Bin 4	3000	113	62
Bin 5	10000	113+	113

Figure 20 shows the wafer pit counts on a quarterly basis. Wafers initiated in Q3 are aggregated with the Q4 results.

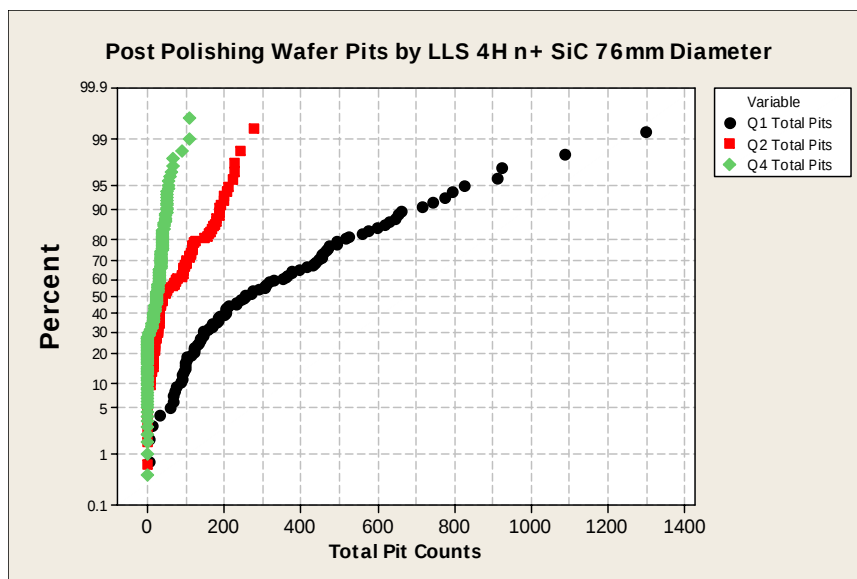


Figure 20: Quarterly distributions of pit counts on polished 76mm diameter 4H n+ SiC wafers.

The goal of the first year program was to reduce the pits in the wafers to the equivalent of less than 5/cm² (c.a 90 pits/wafer) for effective diameters >0.5 μm . The optimization of the pit detection capability using laser light scattering was limited to effective diameters of >25 μm due to signal to noise issues, further work will be required in year to in order to achieve higher sensitivity. The data shows continuous improvement in reduction of

polishing pits over the four quarters of the KGS program. The improvements are a combination of reduction of crystal defects and improved polish processes. By the fourth quarter, >90% of wafers exhibited <1/cm² pit density for effective diameters >25 μ m.

A focus area in this program was to reduce the metallic impurities added to the crystal during the PVT growth process. Impurities impact resistivity and when present on the surface can negatively impact Schottky barrier heights. Impurity metals originate in the raw materials used in SiC crystal growth: silicon metal, carbon, and the graphite materials used to build the growth cell. Key metal impurities pertinent to SiC semiconductors are B, P, Al, Ti, V. Prior to the beginning of the KGS program, total concentration of impurities in Dow Corning SiC exceeded 1E16/cm³. These levels were too high to allow for growth of uncompensated semi-insulating substrates and also the high boron had negative impact on the n⁺ crystal properties. During the KGS year one effort, the entire raw materials set was examined for contaminants and appropriate changes were implemented.

Improvements in raw materials provided the key driver to reduce the impurities in Dow Corning SiC crystals to state of the art levels. The impurity level capability meets the program goal of <5E15/cm³ and is shown to be repeatable over one year. This is shown in Figure 21.

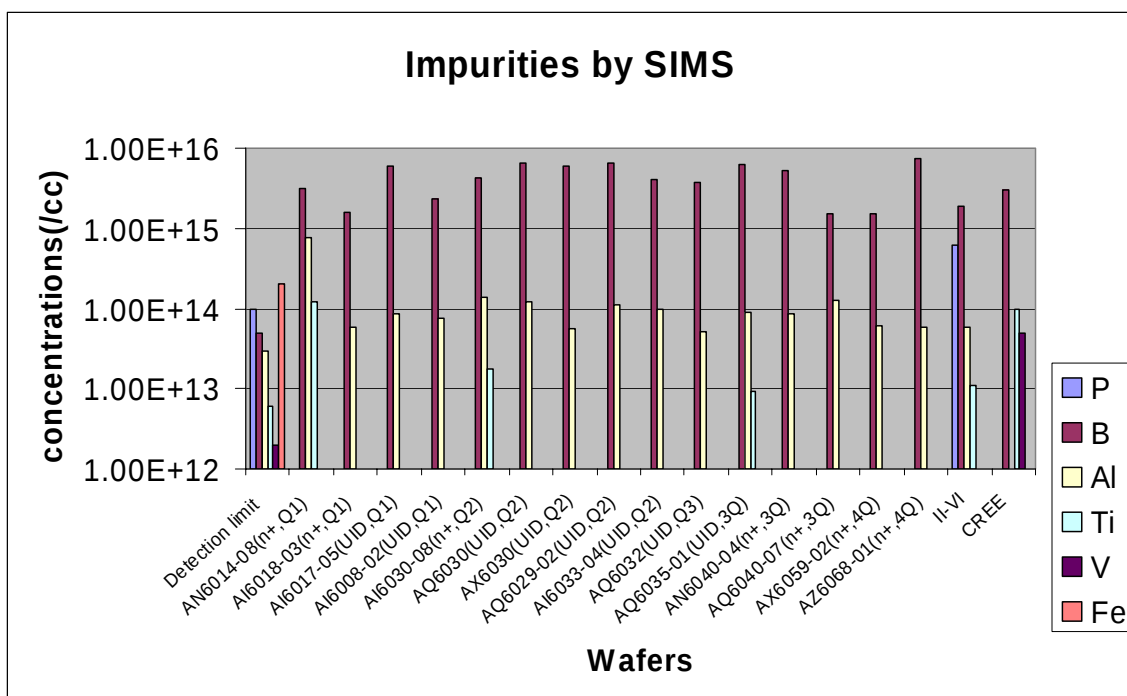


Figure 21 - B, P, Al, Ti, and V impurity levels measured by SIMS on wafers grown each quarter of the program.

4H SiC Chlorosilane-based Crystal Growth and Epitaxy Development Efforts

Aligned to its core competencies as a high technology provider of silicon based chemicals, Dow Corning has focused on the implementation of chlorosilane based chemistry for use in epitaxial growth.

In addition, the favorable properties of a gas sourced crystal growth process and access to source chemicals have prompted the pursuit of a gas phase crystal growth process in the KGS effort.

Gas Source Crystal Growth – Chemical Vapor Transport

The approach used by Dow Corning for gas sourced crystal growth is known as Chemical Vapor Transport (CVT). The key essence of the CVT approach is to control the growth process by strategic controlled chemical reactions of the source gases. Source gas selection and establishment of desirable growth kinetics is optimized to provide high rate deposition on seed crystals. Targeted rates are to be comparable to PVT growth rates (200-400 $\mu\text{m/hr}$).

The year one program goal was to define and prototype a CVT process and establish efficacy for its use in 4H n+ SiC crystal growth. The approach consists of the following steps:

- Reaction cell design/modeling and chemical reaction modeling to demonstrate growth rates and uniformity at reasonable process temperatures for crystal growth (1800-2000 C).
- Modify an existing PVT furnace to the design of the model CVT system and generate experimental data to tune the model.
- Demonstrate bulk crystal growth.

Modeling efforts at STR, Inc. demonstrated that growth rates comparable to PVT could be easily achieved using chlorosilane molecules. Figure 22 shows the results from the model for calculated growth rate as a function of temperature and pressure.

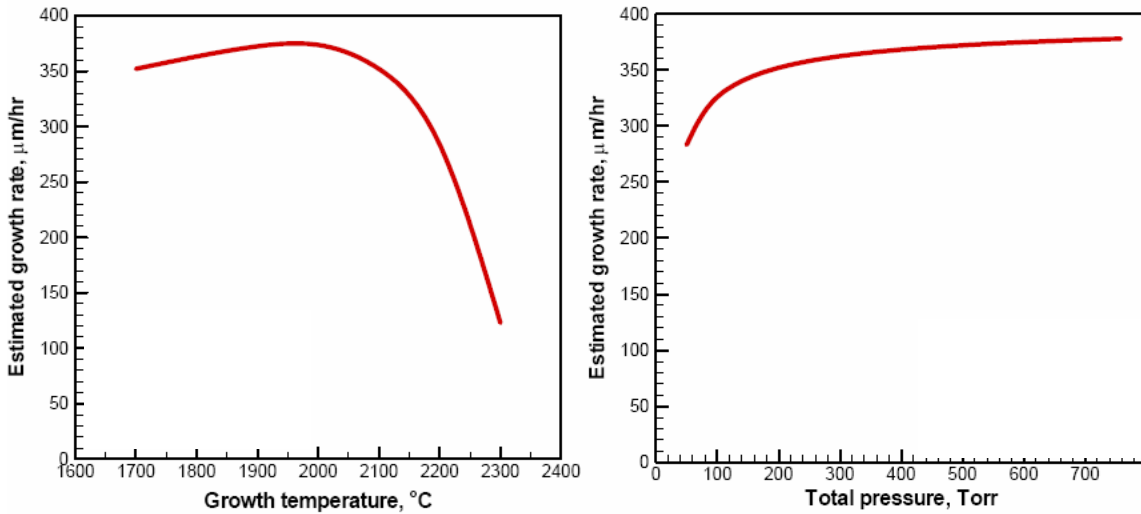


Figure 22 - Modeled growth rate for CVT of chlorosilane and propane as a function of temperature and pressure.

To confirm the gas decomposition and growth model accuracy, the model was applied to Dow Corning's chlorosilane epitaxy process data. Figure 23 shows the results of two dimensional modeling of the hot wall epitaxy process, indicating that the model provides reasonable prediction capability for the growth of SiC by CVD.

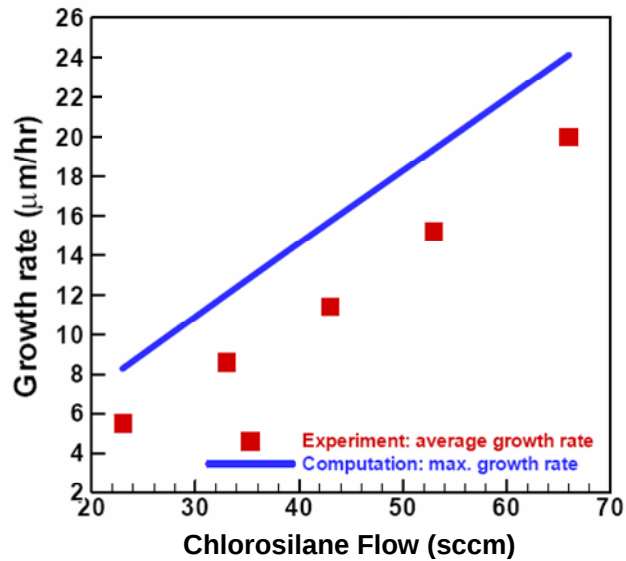


Figure 23- CVT chemical reaction model applied to CVD epitaxy. Figure shows modeled and experimentally determined growth rate trends as a function of chlorosilane flow.

The CVT deposition equipment was modified and installed at Dow Corning in third calendar quarter of 2006. Experimental work performed confirmed the deposition rate data predicted by the model. Figure 24 shows the deposition rate as a function of C/Si ratio in the precursor gas stream for growth times of 1-5 hours.

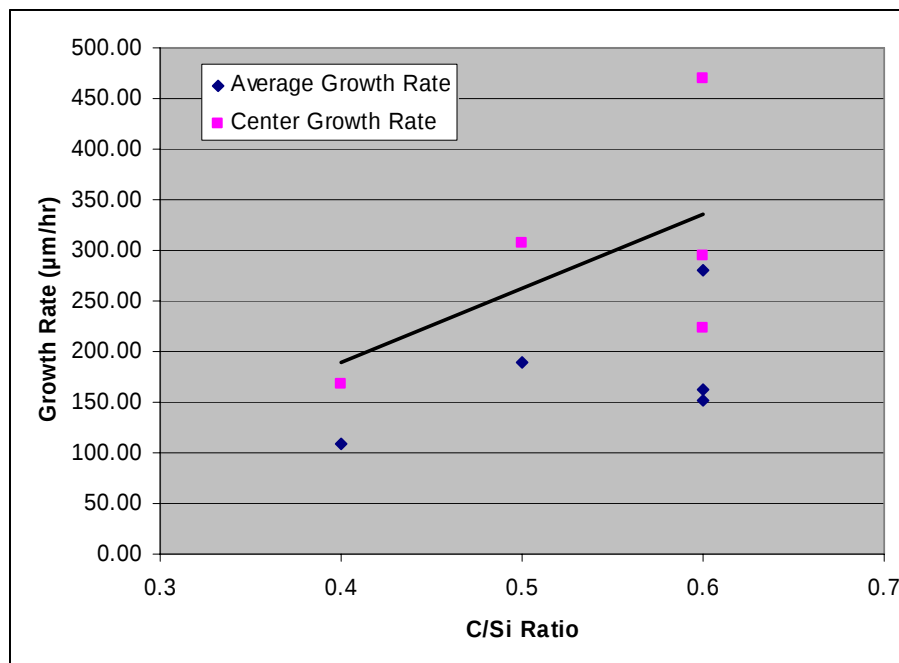


Figure 24 – CVT Growth Rate vs. C/Si Ratio.

Reports of gas phase SiC crystal growth in the literature often highlight early difficulty with ancillary deposition of species in the gas injectors and exhaust stream. Early CVT work exhibited these issues as well. Redesign of the exhaust system was required due to downstream condensation of reactants, and successful suppression of the deposits was achieved. A more difficult challenge was confronted as a result of spurious deposition of silicon upstream of the CVT reaction zone. At the end of KGS year 1, some improvement was achieved but the problem was not eliminated. In order to demonstrate bulk growth, a crystal was grown by sequential depositions at time intervals of about 5 hours (limited by injector clogging). In between each growth run the gas injectors were changed to prevent system failure due to the parasitic deposition clogging of the injectors. Also after each step the growth height was measured using a drop gauge at the center of the growth. Figure 25 shows the growth thickness as measured along with a calculated growth rate at the center of the wafer. The growth rate over sequential runs was fairly consistent at ~225μm/hr. This indicates the viability of the CVT growth system for long growth runs once the parasitic deposition issues are solved. A cross section of the 5mm boule produced can be seen in Figure 25. The zoomed in section in Figure 26 shows stripes due to doping differences at the start of each growth.

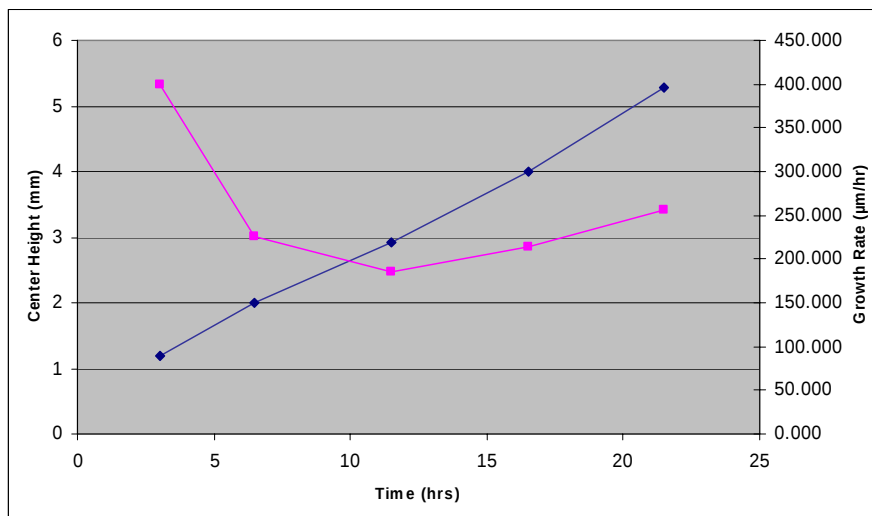


Figure 25 – Growth thickness (blue) and rate (magenta) for each step in the aggregated CVT growth run.

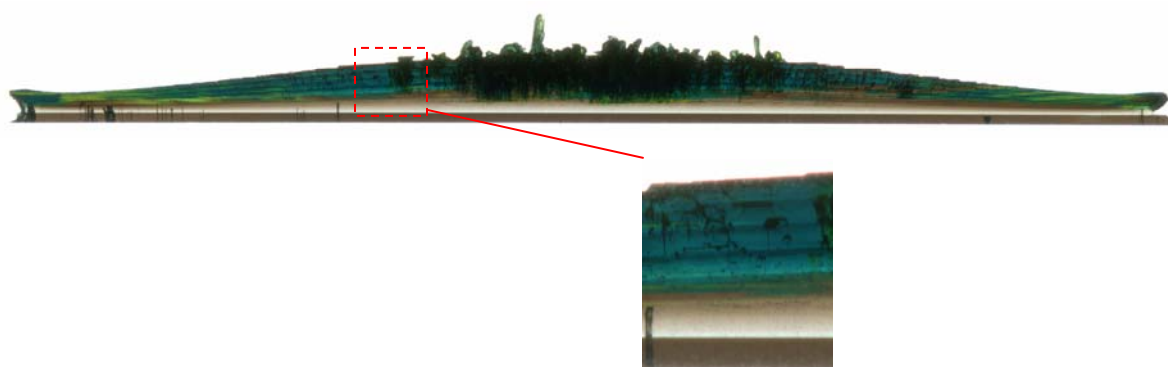


Figure 26 – Cross-Section of the 5mm boule grown in the aggregated CVT growth run. Magnified section shows doping stripes at the beginning of each growth run.

Work in 2007 focuses to eliminate parasitic deposition in the injector with the goal to achieve a 5-10mm thick crystal growth by Q2- 2007.

Chlorosilane-based SiC Epitaxy Development

KGS year one effort focused to transfer Dow Corning's chlorosilane SiC epitaxy process from the single wafer hot wall CVD system to a batch (5 wafer, 76 mm diameter wafer) system, develop the doping control, optimize uniformity and produce device wafers for subcontractors in the program.

Device types for the program are Schottky barrier diodes (SBD), static induction transistors (SIT) and PiN diodes. This required that the batch reactor be qualified and capable of thickness in the range of 1-30 μm with thickness uniformity of <10% (standard

deviation/mean), n-type dopant concentrations of $3\text{E}15\text{-}1\text{E}19/\text{cm}^3$ with uniformity of <15%.

The following tables present the uniformity achieved in epitaxy film development work in the first half of the program.

	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Inter-wafer variation (sigma/mean)
Average thickness (um)	2.12	2.13	2.17	2.16	2.14	0.97%
Average doping (cm^{-3})	$1.18\text{e}16$	$1.17\text{e}16$	$1.22\text{e}16$	$1.18\text{e}16$	$1.14\text{e}16$	2.43%

Table 1: Inter-wafer variations of thickness and doping for 5 wafer process lot

Company	Intra-wafer thickness variation	Inter-wafer thickness variation	Intra-wafer doping variation	Inter-wafer doping variation
Burk, et.al [1]	~0.5-1.1%	~1%	~2.3-5.2%	~5%
Thomas. et al [2]	~1.5-2.5%	~2.2%	~3.4-4.8%	~1.35%
This Work SiClx	~0.4-1%	~0.97%	~5.6-7.7%	~2.43%

Table 2: Comparison of epitaxial film uniformity with published results from other multi-wafer reactors with SiH_4 / propane chemistry.

[1] A. A. Burk, et al, Materials Science Forum Vols 483-485 (2005) pp.137

[2] B. Thomas, et al, Mater. Res. Soc. Symp. Proc. Vol 911 (2006) B09-02

The within wafer and wafer to wafer target control, uniformity and repeatability achieved were in the range of the program objectives.

Round robin doping tests were conducted between Dow Corning and Northrup Grumman to insure that the doping in the epitaxy layers would meet the device operation targets.

Automated epitaxy processes were developed for growth of static induction transistors. Three lots of wafers were supplied to Northrup Grumman for device fabrication. Doping was tuned and inspected as each lot was delivered. Assessment of the device operations and results are discussed in Task 4. Of relevance to the epitaxy discussion is that device testing revealed that the channel doping in lots one and two was slightly off and high of the target. Lot 3 was on target.

At the end of year one several wafers were fabricated with SBD structures and PiN structures. Results of SBD testing are discussed in Task 4. PiN structure will be processed for device fabrication in Year 2 of the program.

One of the key discoveries in the KGS program pertained to the carrier lifetime values measured on the chlorosilane-based SiC epitaxial layers. Lifetime measurements are discussed in Task 3.

Lifetime testing results revealed that the epitaxial films produced using chlorosilane precursors have much higher values (0.75 to >3 usec) than the values reported in the literature for SiH₄-based SiC epitaxy processes.

Figure 27 shows lifetime values collected along the diameter of a 76 mm diameter 4H n⁺ epiwafer (N~E15/cm³, 30 μ m) measured using two different techniques at two different laboratories (DCCSS and NRL). The measurement locations are as close as could be achieved.

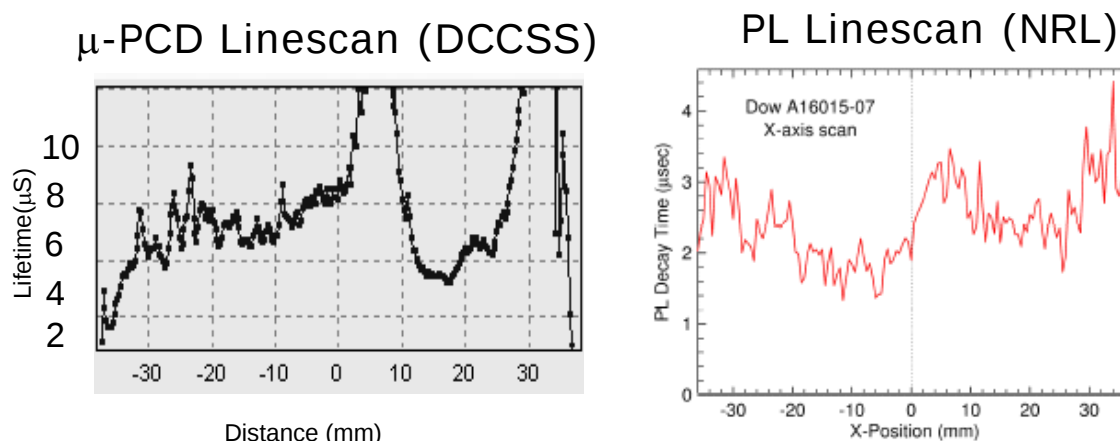
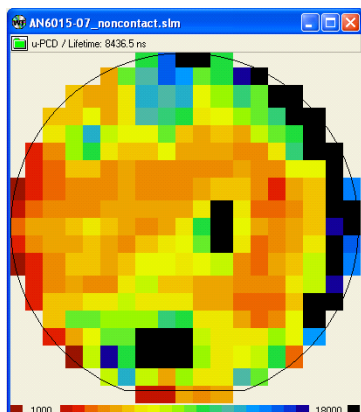


Figure 27: Excess carrier lifetime measurements made along the diameter of a 76mm 4H epiwafer (N~E15/cm³ to ~30 μ m). Left-microwave photoconductive decay, right-photoluminescence decay. Injection level was >1E16/cm³.

The left figure shows data from microwave photoconductive decay (u-PCD) testing and the right figure shows the data from photoluminescence decay (PLD) tests. The variations along the diameter are consistent between the testing. The values of >5 usec for u-PCD and nominally >2 μ m for PLD are to the best of our knowledge the highest values ever reported for SiC epilayers.

u-PCD testing was used to assess several wafers from one batch epitaxy growth to assess the consistency of the lifetime. Figure 28 shows the results. High lifetime values were measured on all five wafers. Uniformity of the lifetime values was consistent with the uniformity of the epilayer thickness and doping.

μ -PCD Carrier Lifetime Values From Batch Epitaxy Process*



A typical lifetime map of a 3-inch epiwafer.

Wafer #	Mean (μ s)	Median (μ s)	σ (σ /mean)
1	1748	1338.6	80 (5%)
2	2694	1640.6	122 (5%)
3	1197	1044.9	45 (4%)
4	8497	5969.1	96 (1%)
5	11627	5158.2	157 (1%)

Table 3: Lifetime data on 5 wafer load from a batch epitaxy process
($t_f \sim 30\mu\text{m}$, $N_D \sim 6E14\text{ cm}^{-3}$)

* tested by a modified WT-2000 μ -PCD system at an injection level of $5E16\text{ cm}^{-3}$

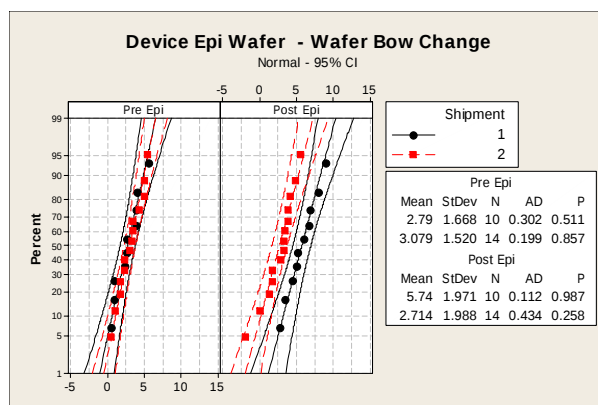
Figure 28: μ -PCD carrier lifetime map and summary data for a single batch run of five epiwafers grown using chlorosilane chemistry.

Future work in KGS year two will evaluate PiN diode performance associated with the high carrier lifetime epitaxy and offer the first opportunity to correlate device performance with non-destructive lifetime tests performed on the blanket layers prior to epitaxy.

A provisional patent application pertaining to the technology to produce CVD SiC materials with long carrier lifetime has been filed and the filing communicated to ONR.

The wafer processing can have a direct impact on epilayer growth performance and device fabrication. As an example, non-flat wafers can limit epilayer growth uniformity and also yield in lithography operations associated with device fabrication. Excessive bow and warp following SiC epitaxy processes has been an issue discussed in the SiC community. An unexpected result in the evaluation of the epilayers is that low values of bow coming from DCCSS polishing processes are maintained during growth of epitaxial layers to at least 30 μm thick. Figure 29 shows a typical result obtained for two lots of wafer produced with SIT epitaxial structures. A bow value of $<6\text{ }\mu\text{m}$ is maintained after SiC epitaxy is performed.

Figure 29: Wafer bow change pre and post epitaxy for two batch epitaxy groups.



Defectivity in epitaxial layers is known to be linked to the substrate defects. Defects can also emerge from particles on the wafer surface which impact step flow resulting in pits in the epilayer. Graphite hardware used in the reaction zone in SiC epitaxy is particularly prone to particle shedding, especially after several deposition cycles. LLS tests were employed at Dow Corning in order to try and develop leading indicators for particle excursions in the CVD epitaxy system. LLS epitaxial layer pit counts were monitored during the lifetime of the graphite parts. Figure 30 shows the trends observed in the work on SIT epitaxy.

Each arrow indicates a cleaning process or the replacement of new graphite parts in the reaction zone. The tests show that the particle will drop when aged parts are replaced. A “seasoning” effect is observed when parts are replaced – the particle shedding is high on the first process using the new parts. A test run is inserted to allow the new parts to stabilize. Following this action, the instances of particle related defects drop to a baseline level. The test allows proactive part replacement before particle related defects in the epitaxial layer reach an unacceptable level.

Doping uniformity was assessed on 12 CVD SIT epitaxy lots. Each lot contained five wafers, one wafer was tested per lot. Figure 31 shows the distribution of measured values of within wafer uniformity broken out by device layer type. Thickness uniformity for all of the films was between 2% and 7%. Uniformity is not reported for the buffer and contact layers, which are highly doped n+. Currently there is not a convenient test to measure the thickness and doping uniformity in such layers.

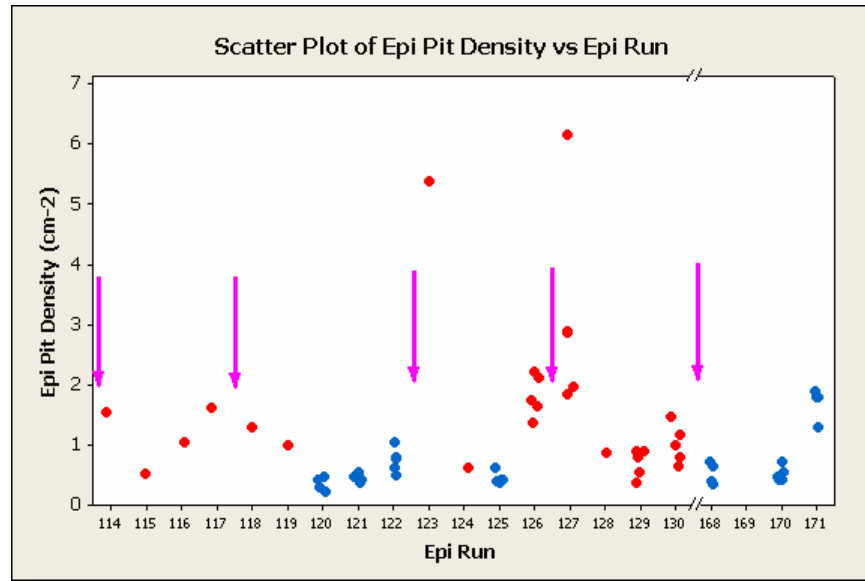


Figure 30: Example of chronological pit measurements on epiwafers. Arrows highlight when consumables in the reaction zone were replaced.

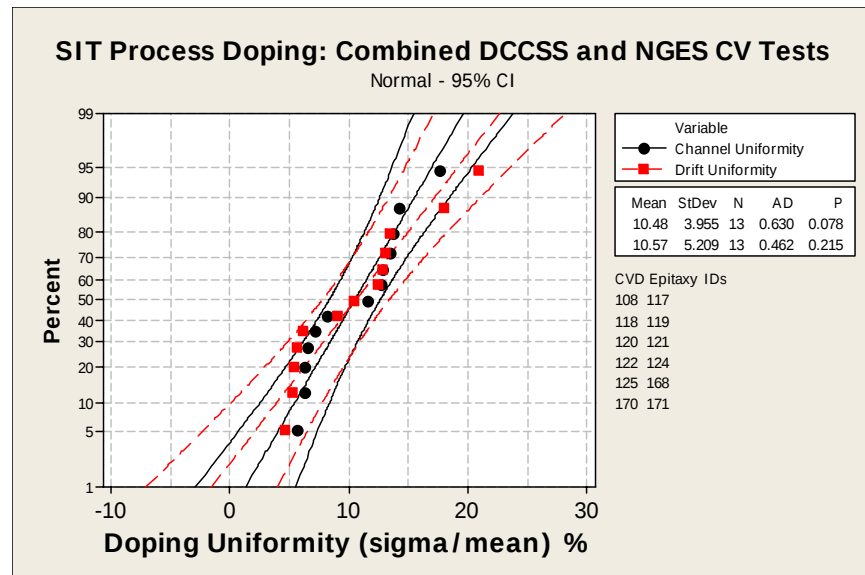


Figure 31: Distribution of doping uniformity for epiwafers produced for use in fabrication work on static induction transistors.

Task 3 Metrology for Wafer Specifications

During Task 3, advanced wafer mapping technology was used to evaluate substrate shape, resistivity, carrier lifetime, crystal quality, defects, and epitaxy characterization. Laser light scattering spectroscopy was developed for mapping of wafer/epitaxy defects. Automated u-PCD mapping was developed to evaluate wafer carrier lifetime and assess lifetime defects. Sub-tasks related to Task 3 include:

- **Task 3.1 – Non-destructive LLS Testing of Wafer & Epi Defects:** Complete calibration of automated laser light scattering spectroscopy (LLS) for detection and sizing of surface particle, pit and scratch defects (0.35 um and larger).
- **Task 3.2 – Ingot/Wafer Resistivity Testing:** This task is focused to develop resistivity screening for SI SiC based on microwave frequency electrical loss testing. Once a successful wafer screening test method development is completed, the development of a screening method for resistivity in SiC boules will be explored.
- **Task 3.3 – Lifetime Mapping:** This task focuses on the extension to SiC wafers and epitaxy of the microwave photoconductive decay (u-PCD) technology used in silicon wafer testing. In collaboration with the Naval Research Laboratory, several complementary tests will be employed to identify key lifetime killers in SiC and link the defect to its signature in the u-PCD map.

LLS Testing on Wafers and Wafers with Epitaxy

A KLA-Candela C2 Optical Surface Analyzer was purchased at Dow Corning to facilitate automated surface inspections of SiC polished wafers and epiwafers. This tool rasters a laser across the wafer surface and uses several detectors to capture reflected and scattered light from the wafer surface. The method is commonly referred to as laser light scattering spectrometry (LLS). In order to be detected, defects must impact the reflected or scattered light intensity. The challenge to the user is to develop image processing strategies within the tool's software which allows discrimination of the different defects on the wafer surface. In LLS testing, defects such as particles, pits and scratches are often tested. A particular challenge in testing SiC wafers pertains to the transparency of SiC and the interaction of the laser with defects lying below the upper surface of the wafer.

The main focus of the LLS task in the KGS program is to use the method to find killer defects on the wafer's surface prior to device fabrication. The effort focused to establish a correlation between the LLS detected defect level and the device yields. With this correlation wafers can be screened and not used in device fabrication when the LLS defect counts implied that the device yields would be poor.

The first area of focus was on surface scratches. Scratches can be imaged on the wafer surface using C2 system. Figure 32 shows example LLS images of wafer surfaces measured using the C2 system. The images are digitally filtered to remove wafer waviness and to highlight the wafer scratches. The scratches are very faint, fine features and to date, while they are visible in the image to the eye, Dow Corning has not been

successful to get the CS software to recognize the scratches. At this time the scratches are assessed manually from the image.

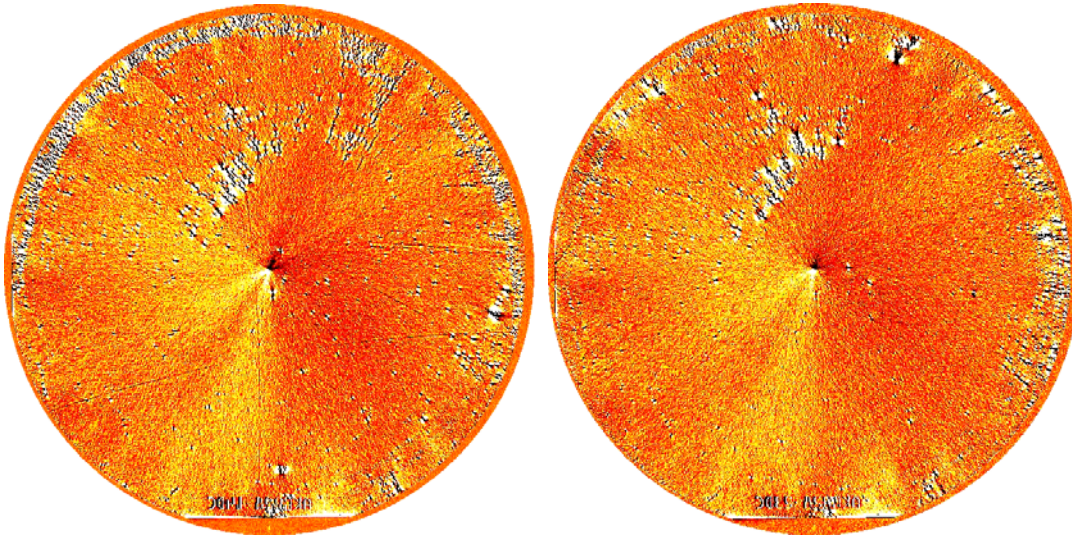


Figure 32: Examples of topographic light scattering maps measured on 76mm 4H n+ SiC wafers. The wafer on the left has scratches visible on the bottom half, while the wafer on the right has very little scratch defects.

As a verification plan, scratches were also assessed on wafers using dark field microscopy with 100x magnification. Figure 33 shows the correlation between the LLS and dark field tests. When the scratch length on the wafer exceeded 80 mm, the value was assigned as 80 mm. In the inspection of four lots of polished wafers, comparisons of the 30th, 50th, and 90th percentile scratch values show that there is good agreement between the LLS and microscopy testing.

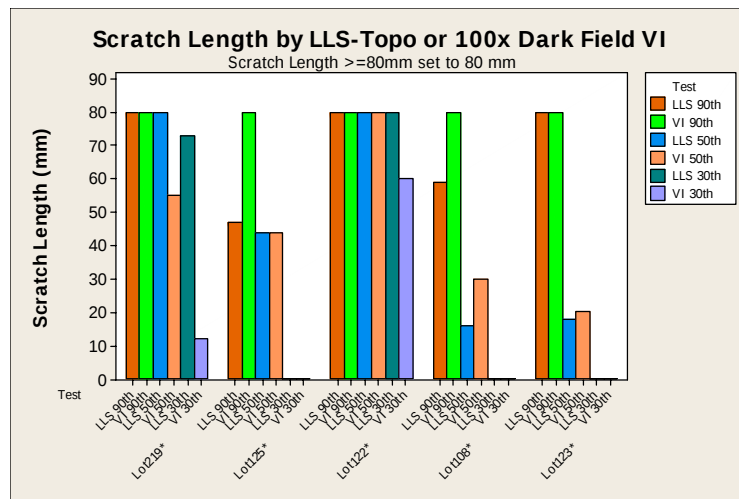


Figure 33: Correlations between microscope imaging and LLS image counting of wafer scratches for 5 sample polishing lots.

LLS filtered images for scratch analysis were gathered for all epiwafers used in the program. The scratch data will be examined in light of the device yield to see at what level scratching corresponds to device operation failure.

Another key defect related to device performance is the formation of pits and particles on the wafer surface. Particularly related to epitaxy, particles and pits on the wafer can lead to disruptions in step flow, leaving holes in the epilayer. A LLS method to count and categorize pits and particles would be important to screen epitaxy processes for device yield limiting defect densities.

The C2 software was configured to count particles/pits on bare wafer or epiwafer surfaces. At this time the pits are binned into groups from as small as 25 μm to greater than 100 μm . Defects of these sizes could be verified easily with microscopy and would be expected to lead to device failures. The light scattering background from the wafer significantly limited the signal to noise of the system with respect to smaller defect sizes. This was especially the case in the testing of wafers with epitaxy. While the C2 system was rated at the vendor for defect detection capability to $<0.5 \mu\text{m}$, realizing this on SiC wafers is not yet possible at Dow Corning.

The LLS pit measurement results are contained in the discussion of Task 2 work and correlations to device measurements are contained in the discussion of the Task 4 work.

Microwave Loss Testing on High Resistivity SiC Wafers

Emerging high frequency RF applications for SiC now focus on the fabrication of MMIC structures for building high power transmitters and receivers. In these designs, attenuation or excess loss of RF energy has to be managed carefully, or device reliability issues can emerge. Currently, the SiC materials community relies on resistivity testing to verify the utility of high resistivity or “semi-insulating” SiC wafers. Due to the wide bandgap of SiC, it is very difficult to make accurate DC resistivity tests on SiC wafers. Contact resistance can be very high if not addressed correctly; measurements can result in over-estimation of the resistivity of the SiC material. Reliable resistivity testing even becomes more challenging when the idea of a non-destructive test is considered.

What’s more, the DC resistance is only one part of the energy loss mechanisms in SiC material. At frequencies above 100 MHz, capacitive losses can become comparable to and even more substantial than DC resistive losses. Accurate assessment of the losses in the SiC material is important to successfully predict device performance.

Compared to resistivity testing, one advantage to characterizing dielectric energy loss is that it can be done non-destructively. In the 1990’s Dow Corning developed a RF loss test for silicon carbide ceramic fibers. Using this test method as a foundation, the KGS effort focused to extend the method to the test of SiC wafers and even to mapping the variability of loss across the SiC wafer.

The basics of the test involve building a resonant circuit element where the wafer can be inserted. This can be a waveguide or an antenna. The frequency response of the resonant circuit is tested using a RF Network Analyzer. The frequency response is used to measure the quality factor (Q) of the resonant circuit. The Q measures the energy stored in the resonant circuit. By placing the SiC material into the RF fields, dielectric losses occur and the Q value degrades. The loss tangent and Q are inversely proportional. Calibrated measurements of the Q and calculation of the loss can be made using waveguides. In the frequency range of interest (2-20 GHz), the size of the waveguide is comparable to the wafer diameter, and so while it is possible to get a measurement, the measurement is an aggregated value of the wafer and the technique is not useful for wafer mapping. To get maps of the wafer loss variation, a coaxial antenna can be used. In this work, the strategy is to employ both approaches – waveguide and antenna, and to test well known low loss materials used in MMIC fabrication – GaAs and alumina. Maps of Q will be used to understand the variation across the wafer.

Figure 34 is a bar chart of the results of measurements on several materials of dielectric constant and loss tangent made using a waveguide. Several frequencies were tested. Dielectric constant values are consistent with values established in the open literature.

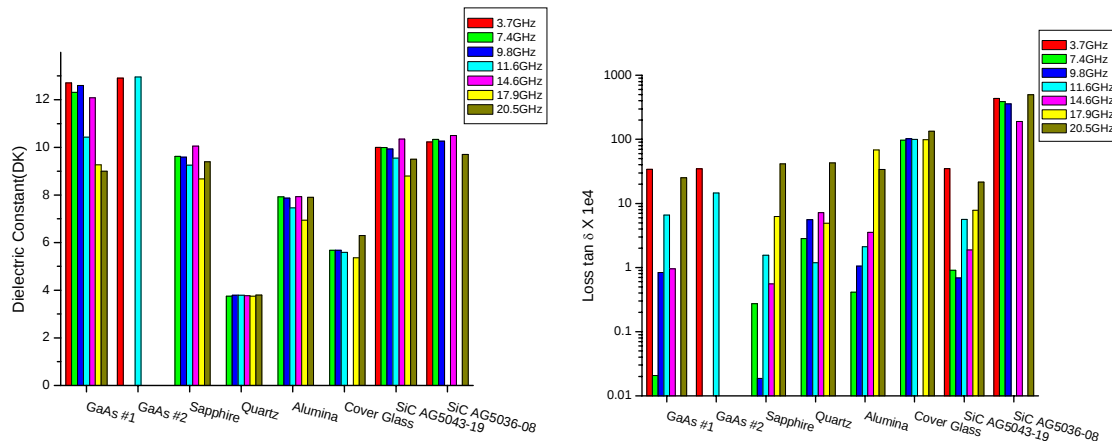


Figure 34: Values of dielectric constant and loss tangent measured on undoped 6H SiC wafers, and standard microwave device substrates (GaAs, sapphire, alumina, quartz)

The loss data shows that the energy loss is generally flat or slightly increasing with frequency. Generally, for this frequency window loss tangents in the range $1\text{E}-4$ to $5\text{E}-4$ are considered to be low loss materials suitable for use in high frequency RF electronics. In testing unintentionally doped SiC wafers fabricated at DCCSS, the loss values can be comparable or higher than GaAs or alumina. Typical commercial literature values of loss tangent for SiC and GaAs are in the range of $2\text{E}-4$ to $2\text{E}-3$.

Figure 35 shows the comparison of S-Band measurements on SiC using the large area waveguide test data and the average of small area antenna data measured at 9 points on a SiC wafer surface.

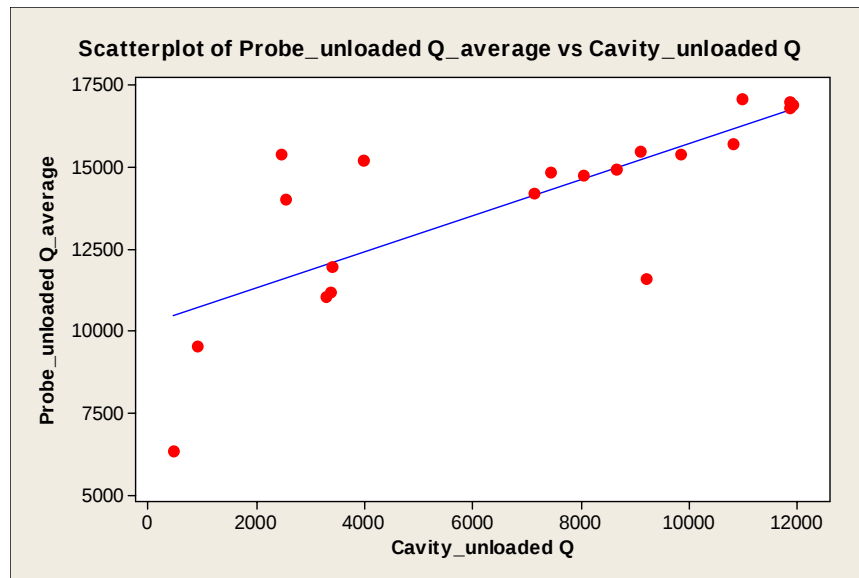


Figure 35: Comparison Q values for 6H SiC for probe (antenna) local area test and the full wafer cavity test.

The average Q of the antenna mapped surface test is about twice that of the waveguide test. It is important to note that while the waveguide test measures the majority of the wafer area in one test, the data will not correspond to an integrated average of the material in the waveguide cavity. This is because the distribution of loss values across the wafer surface will result in inhomogeneous loading of the cavity, thereby distorting the energy distribution (coupling) between waveguide modes compared to a homogeneously loaded cavity. A higher loss sub-volume of the wafer will weight the response of the cavity toward lower Q. For comparison with MMIC devices which would be built on die regions of 1-4 cm², the antenna results are likely to better represent the distribution of performance of each device related to the wafer.

Many undoped 4H and 6H SiC sample wafers were tested. From current voltage resistivity tests these materials cover the range of resistivity from 1E3 to 1E10 ohm-cm. Typically, samples with resistivity <1E4 ohm-cm show very high loss values. Above resistivity of 1E5 ohm-cm the material shows no distinct correlation between resistivity and Q. This is not surprising as the materials properties which impact resistance are not expected to be the same as those impacting the value of the capacitive losses.

Figure 36 is an example of Q median value as a function of wafer mean resistivity measured on undoped 6H SiC wafers.

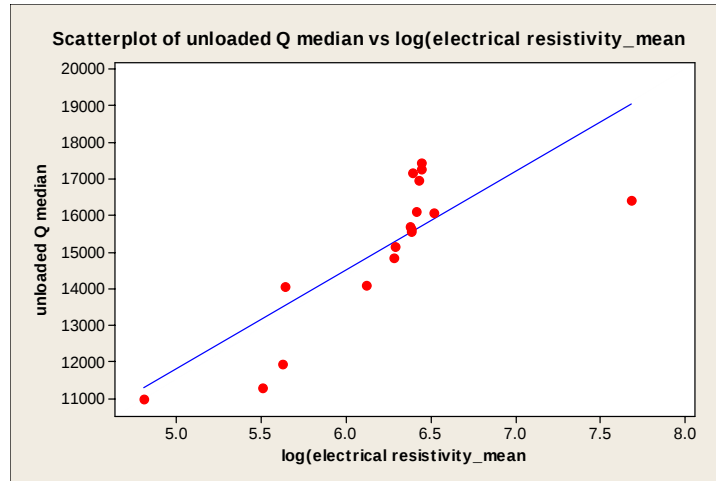


Figure 36: Variation of Q value as a function of wafer resistivity measured on undoped 6H SiC wafers.

Figure 37 shows wafer maps of quality factor for representative 6H undoped SiC wafer and a semi-insulating GaAs wafer measured at two frequencies. Figure 38a shows summary data from measurements on several SiC wafers using the antenna method. Figure 38b shows the range of within wafer values of Q measured on several undoped SiC wafers at both 4.5 GHz and 15 GHz. For the nine point measurement, the range of Q values within a wafer is nominally 10%. The shape of the Q value distribution does not appear to imply any obvious relationship to the SiC PVT process, though more studies must be completed to get a clear understanding of the factors of the SiC materials properties that limit Q (and loss tangent) values.

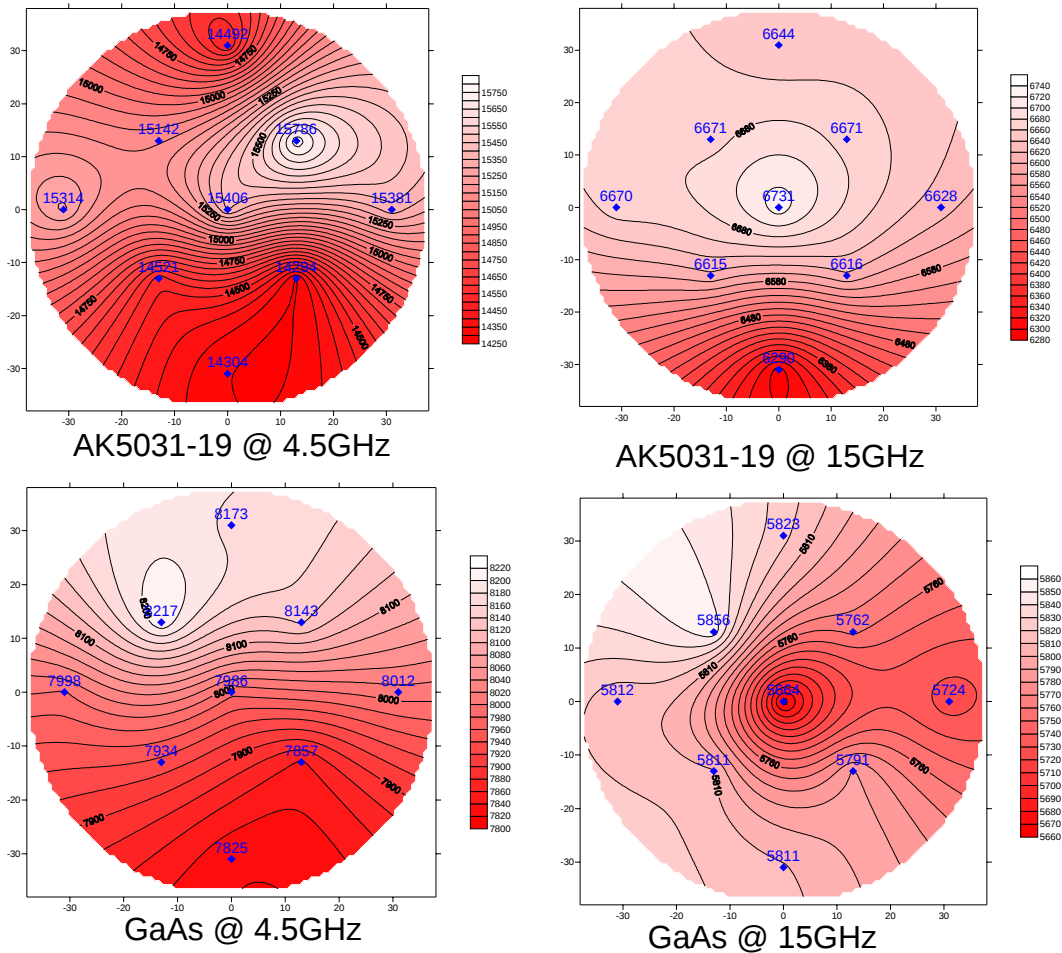


Figure 37: Spatial distribution of Q values measured on undoped 6H SiC and on a commercially available semi-insulating GaAs wafer.

4.5GHz						15GHz					
Wafer number	Mean	SD	Min	Max	Range	Wafer	Mean	SD	Min	Max	Range
AG5036-01	15219.78	1781.37	11234	16754	5520	AG5036-01	6578.89	136.79	6359	6755	396
AG5036-03	15407.56	1925.19	10892	16737	5845	AG5036-03	6568.22	135.31	6376	6787	411
AG5036-08	9566.00	4720.62	3993	16021	12028	AG5036-08	6181.00	460.91	5113	6665	1552
AG5036-09	6356.22	5426.48	2152	14521	12369	AG5043-04	6424.44	166.38	6174	6696	522
AG5043-07	15497.00	589.29	14461	16252	1791	AG5043-09	6559.22	122.09	6359	6698	339
AG5043-08	14862.00	1802.54	10155	15968	5813	AG5043-10	6589.33	103.43	6444	6688	244
AG5043-09	15413.33	600.77	14223	15961	1738	AG5043-17	6233.22	355.12	5939	6795	856
AG5043-10	15711.44	952.61	13770	16409	2639	AG5043-18	6470.78	88.60	6299	6571	272
AG5043-17	17102.44	1696.99	13041	18752	5711	AG5043-20	6206.89	77.63	6060	6279	219
AG5043-18	17007.11	1032.89	14694	18171	3477	AK5032-06	6448.22	106.12	6203	6558	355
AG5043-19	16905.67	827.18	15020	17557	2537	AK5032-07	6423.67	178.31	6117	6590	473
AG5043-20	16836.11	1413.81	13333	18015	4682	AK5032-08	6383.89	100.38	6220	6503	283
AK5032-06	11961.89	514.33	10966	12618	1652	AK5032-12	6343.67	536.56	6122	7770	1648
AK5032-07	11179.89	513.60	10115	11614	1499	AK5032-17	6750.89	121.14	6563	6921	358
AK5032-08	11049.22	489.90	10179	11734	1555	AK5032-18	6499.11	89.08	6361	6628	267
AK5032-16	14046.67	271.77	13611	14478	867	AK5032-19	6615.11	127.18	6290	6731	441
AK5032-17	14207.56	598.13	13241	15093	1852	AK5032-20	6670.56	245.89	6157	7011	854
AK5032-18	14789.33	596.89	13576	15372	1796	GaAs	5783.78	58.61	5664	5856	192
AK5032-19	14960.00	559.30	14294	15786	1492						
GaAs	8016.11	137.34	7825	8217	392						

Figure 38a: Tabulated within wafer statistics corresponding to loss tests on undoped 6H SiC wafers. Measurements were performed at 4.5 GHz and 15 GHz.

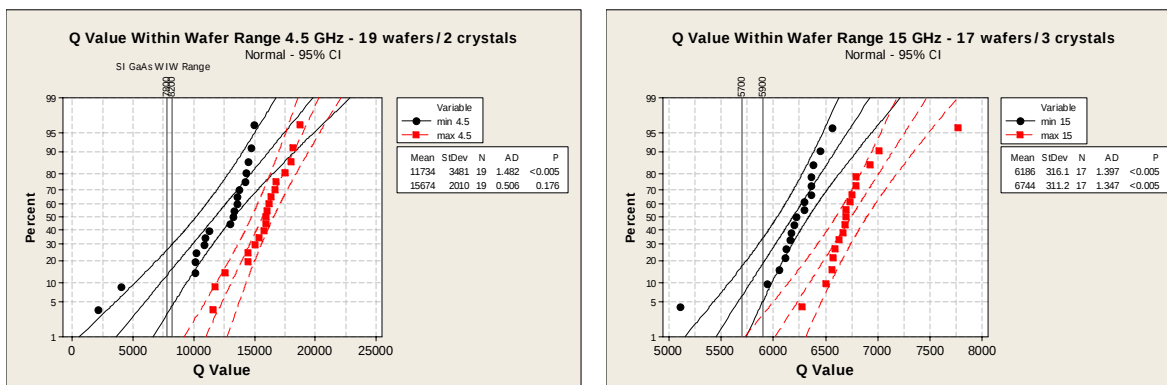


Figure 38b: Distribution of within wafer Q values compared to GaAs as measured at 4.5 and 15 GHz.

Figure 39 shows the range of loss tangent values estimated from the average within wafer Q values assessed from the wafers associated with Figure 38a. Also shown are the loss tangent values for the reference sample semi-insulating GaAs wafer. As expected the loss increases with frequency for both materials. Over the 4-15 GHz range the SiC and GaAs materials show comparable and very low loss values. Measurements of loss tangent for SiC wafers with resistivity $>1E5$ ohm-cm have been measured using a) coplanar waveguide (Royet, et. al., Mat Sci Forum Vol. 38-342 (2000) p. 1267) and reported a value of $2.8E-3$ at 8 GHz and b) millimeter wave resonant cavity (Afsar, et.al., IEEE Instrumentation and Measurement Technology Conf., (2005) p. 1975) and reported a value of $2.7E-3$ at 60 GHz. DCCSS measurements on SiC with resistivity $>1E5$ ohm-cm range about $1E-4$ to $1.5E-4$ over $3 < f(\text{GHz}) < 15$. At this time it is not possible to assign the difference in values to the materials tested or to the test, but it may pertain to the DCCSS data coming from antenna testing and the published data being whole wafer data.

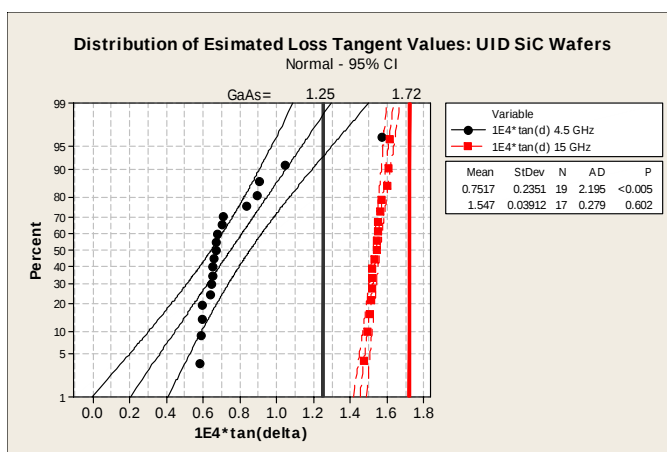


Figure 39: Distribution of loss tangent values calculated from the SiC and GaAs wafer data in Figure 38.

Carrier Lifetime Measurements and Mapping

Silicon carbide semiconductors are expected to offer significant performance extension in the area of power devices when compared to silicon and gallium arsenide. In silicon semiconductors, a key metric for the performance of the material is the carrier lifetime. Using the microwave photoconductive decay (u-PCD) method, silicon material engineers can inspect wafers and epiwafers for contamination and crystalline defects such as stacking faults and slip. The u-PCD test offers fast, high resolution results and allows for rapid interpretation of process anomalies. In the KGS program effort was dedicated to the investigation of the use of u-PCD as a means to characterize SiC materials. The test could potentially provide rapid feedback on crystal defects which limit carrier lifetime. To date, little is known about what governs carrier lifetime and recombination in SiC. Also, reported SiC lifetime values are traditionally much lower than expected from theory. Therefore a thorough investigation of this metric could help to identify new ways to improve on SiC material quality and accelerate commercialization efforts.

As interpretation of lifetime variations is difficult for SiC a two prong approach was followed. First, Dow Corning would contract and purchase (with internal funds) a u-PCD system commonly used in the silicon industry and have it customized for use in SiC. With this system lifetime testing could be performed on SiC materials. The tested materials would then be provided to NRL for lifetime testing via photoluminescence (PL) testing. Using two methods to define the lifetime would provide for a standard test and interpretation. In latter years of the KGS program, lifetime testing would be correlated to power device results to see if the lifetime map could be used as a leading indicator for device performance.

In March 2006 Dow Corning received a u-PCD system modified with a UV laser and high speed digitizer. The modifications are required to accommodate the larger bandgap of SiC and typically low lifetime values in SiC, respectively.

Tests were initiated on 4H SiC epiwafer material. The materials tested included epitaxial SiC films deposited by CVD using either SiH₄ or chlorosilane precursors on Dow Corning 4H n+ substrate material. Comparison of the results exposed a very unexpected trend – the SiC epitaxial layers grown using chlorosilane routinely exhibited longer lifetimes compared to those deposited with SiH₄. Figure 40 shows a plot of some of the early results, where the trend of lifetime with SiH₄-based SiC epilayer thickness reported in the literature was much different than the trend observed for chlorosilane based material. When corrected for surface effects, the equivalent bulk lifetimes measured on chlorosilane-based SiC epilayers appeared to be as much as 10x higher than that reported for SiH₄-based SiC epilayers. Concurrently, DLTS testing at CMU revealed that the chlorosilane SiC epitaxy exhibited 5-10x lower deep centers than commonly reported for SiH₄-based films. A survey of published results on deep centers and lifetime is tabulated below.

Metric	SiH ₄ -Chemistry Values	SiCl ₄ -Chemistry Values	[REF]
Concentration of Deep Centers by DLTS	Z1/Z2: 5x10 ¹² /cm ³ EH6/7: 3x10 ¹² /cm ³	Z1/Z2: 1x10 ¹² /cm ³ EH6/7: 2-5x10 ¹¹ /cm ³	[LaVia,Klein]
Minority Carrier Lifetime by μ -PCD and EBIC (10 < t _f (um)<40)	<0.15 μ s	0.25-0.80 μ s	[Kumar]
Dependence of Deep Center Concentration on Gas Phase C/Si Ratio	Z1/Z2 Concentration decreases as C/Si Ratio increases	Z1/Z2 Concentration decreases as C/Si Ratio increases, but lifetime not dependent on Z1/Z2. D-center increases as C/Si ratio increases.	[Huh]
Defects Limiting Minority Carrier Lifetime	Z1/Z2, D-Center (Boron)	Lifetime insensitive to Z1/Z2 Concentration, but inversely proportional to concentration of D-Centers.	[Huh, Storasta]

LaVia, F. *et al.*, Mat. Sci. Forum Vols. 483-485 (2005), p.429-432
Kumar, R.J., *et al.*, Mat. Sci. Forum Vols. 483-485 (2005),p.405-8
Huh, S.W., *et al.*, MRS – Silicon Carbide – Materials, Processing, and Devices, 2006 B5.15.
Klein, P.B. *et al.*, Appl. Phys. Lett. **88**:52110 (2006)
Kimoto, T. *et al.*, Appl. Phys. Lett. **79**:2761 (2001)
Storasta, L., *et al.*, Mat. Sci. Forum Vols. 389-393 (2002), p.549-552

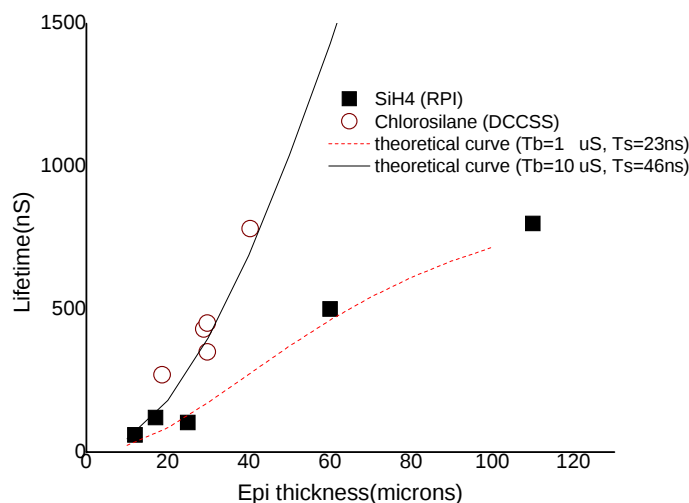


Figure 40: Carrier lifetime data measured by microwave photoconductive decay on DCCSS chlorosilane epitaxy, compared with published results for SiH4-based epitaxy.

During the program several chlorosilane-based epitaxy samples were prepared at Dow Corning with 30 um of n- SiC epitaxy ($[N] < 5E15/cm^3$). Mapping was performed on the films at both Dow Corning (u-PCD) and at NRL (PL). In these measurements care was taken to normalize the carrier injection levels to $1E16/cm^3$ range to facilitate comparisons between the measurements. Multiple instances of carrier lifetime values exceeding 1 usec were observed.

Throughout the testing, the lifetime value comparison between u-PCD and PL are close, and the differences can be attributed to slight variations in the injection level and the portion of the decay curve where the lifetime values are extracted. The discussion in Task 2 reviewed several examples of high lifetime epilayers, results representative of the highest values reported to date in the literature.

Several PiN diode structures were prepared at Dow Corning. PiN diodes will be fabricated in the second year of the program. Testing of lifetime was performed on several test wafers to ascertain the role of the p+ layer. All wafers were tested so that the correlations with the device performance could be studied.

Figure 41 shows the results of lifetime measured in the presence of the p+ layer and after removal of the p+ layer. The p+ layer was removed using high temperature HCl etching.

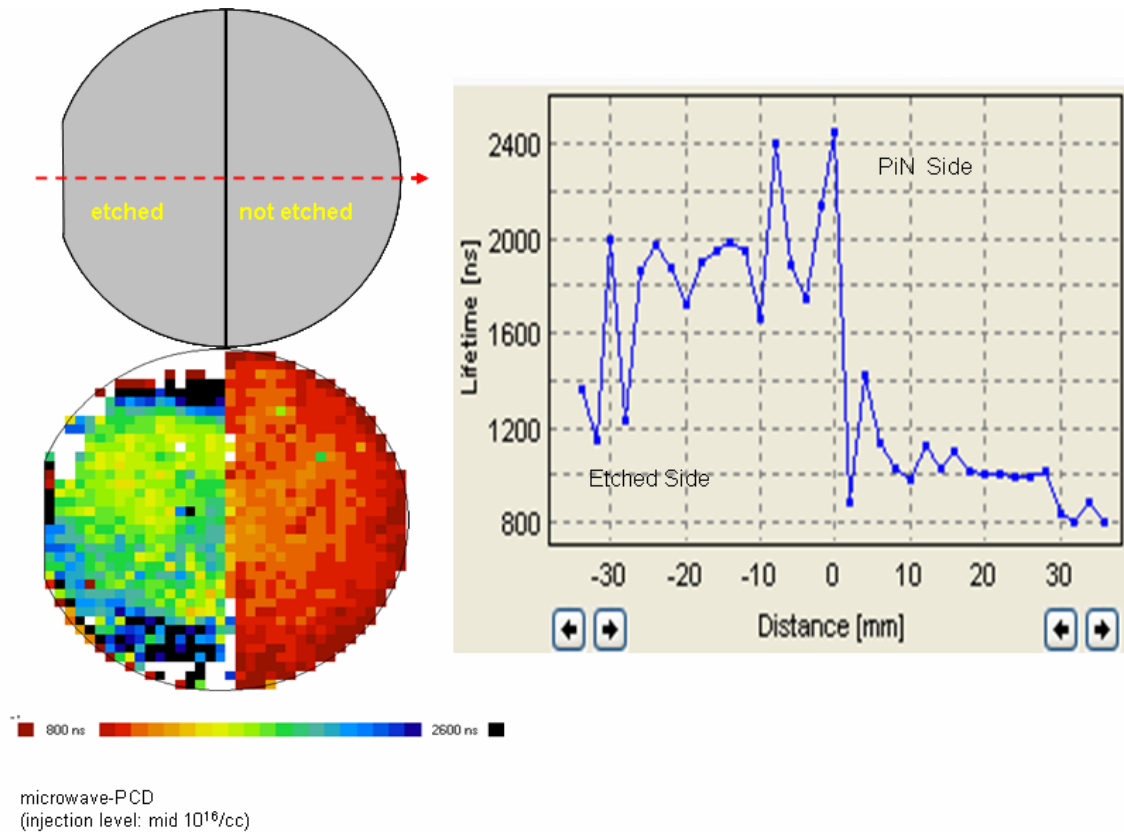


Figure 41: Carrier lifetime measured on PiN epitaxy structure. The p+ layer was removed from one half of the wafer by etching.

The results indicate that the presence of the p+ layer acts as to reduce the lifetime measured in the u-PCD test. The reduced lifetime in the presence of the p+ layer may be due to surface recombination effects near the p+/n- interface. Twenty six PiN wafers were prepared and tested, the distribution of the lifetime values was found to be a function of the n+ buffer layer thickness. Figure 42 shows the distribution of average lifetime results with the average lifetime of distribution being very close to 1 usec. PiN diode testing in the year two KGS program will possibly reveal the linkage between the mapped lifetime values and the lifetime related performance of the device operation.

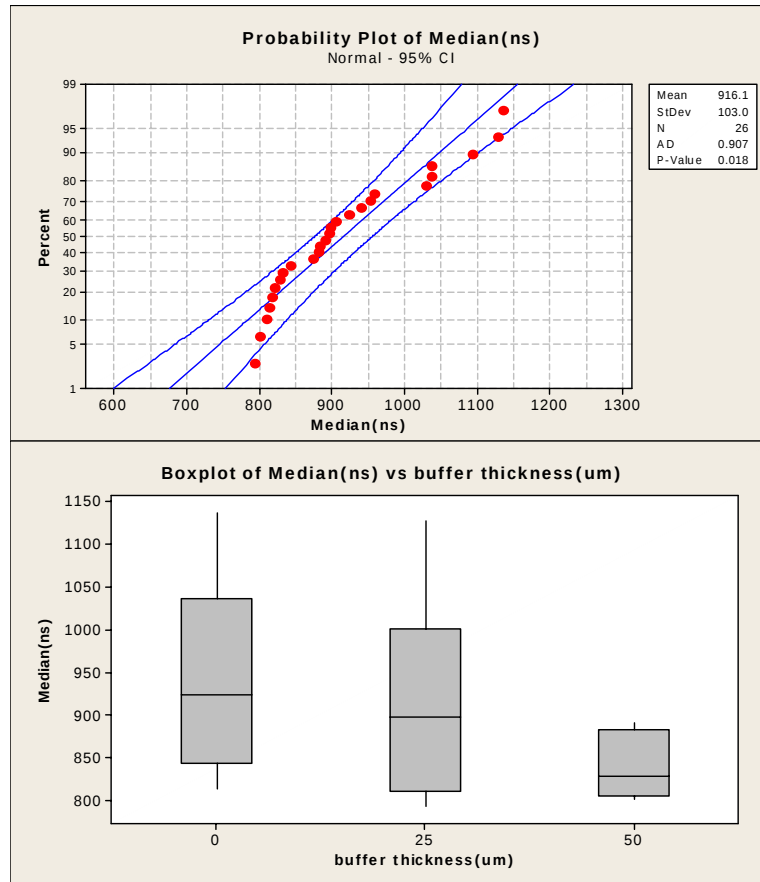


Figure 42: Distribution of median carrier lifetime measured on PiN epiwafers with n+ buffers of various thicknesses.

Task 4 Device Technology Maturation

During Task 4, wafers with SiC epitaxial layers were supplied to commercial and DoD contractors for fabrication of RF and power devices. The goal of this task is to link together the wafer/epitaxy defects, the device yield killers, and the SiC wafer continuous improvement roadmap. Sub-tasks related to Task 4 include:

- **Task 4.1 – Device Fabrication:** One primary subcontractor has been identified to support this program and specifically fabricate RF and power devices on a portion of the wafers fabricated in Task 1.

To evaluate the performance of DCCSS substrates and epitaxy in an established device process, NGC fabricated SiC junction-gate static induction transistors (JSITs) designed for RF applications on six wafers sampled from 3 batch epitaxy runs. Two wafers from NGC's standard SiC supplier were processed in the same fabrication lot for comparison. The p-n junction-gated SIT device has an arrangement of parallel n-type source fingers bordered on both sides by recessed, ion-implanted p+ gates, with the n+ substrate of the wafer used as the drain contact. The total gate periphery of a single device is 28 mm, occupying an area of 7.6×10^{-4} cm². The standard process places several thousand of

these devices on a 3" wafer. This provided a large statistical sample set to compare the device performance of DCCSS material to that of NGC's standard vendor. All processing was performed at the NGC ATC fab lines, using the baseline JSIT process.

The six DCCSS wafers successfully completed all fabrication steps and did not present any major difficulties in processing. No wafer breakage occurred, and the good flatness of the wafers enabled high-resolution patterning using the NGC photolithographic stepper. A measure of the wafer thickness variation used by the stepper during focusing, the "total indicated readout (TIR)", gave comparable averages for the DCCSS (3.30 μm) and standard-supplier wafers (2.89 μm). A few minor processing differences, however, were observed. First, as anticipated from the results of the material inspection, a larger density of localized defects could be seen on the DCCSS wafers compared to those from the standard supplier. Defects that affected the surface topology sometimes disrupted lithography or other processing in localized areas. They did not appear, however, to affect neighboring devices or die, and the statistical affect on yield was difficult to estimate in-process.

NGES performed its standard dc parametric analysis of the wafer-level test data for all eight wafers in the fabrication lot. The analysis was delivered to DCCSS included wafer maps, histograms, and commentary. An overall assessment of basic material quality is provided by the functional yield of working SIT cells on the wafers. The DCCSS wafers gave average functional yields nearly identical to the average functional device yield of the two control wafers in the lot, which were fabricated from wafers procured from NGES's baseline SiC wafer vendor. Thus, the basic material quality of the DCCSS wafers seems adequate for making SIT devices with good yield and performance.

Maps of the measured drain-gate breakdown voltage were compared to defect maps of the epiwafer measured using LLS and also to the wafer micropipe map, stress birefringence image, wafer shape map, and wafer resistivity map. The maps of micropipe map, stress birefringence image, wafer shape map, and wafer resistivity map did not correlate to the variations of breakdown on the wafer surface. Scratch maps extracted from the LLS images of the epiwafer did not correlate with sites of failed breakdown. The epitaxial wafer LLS pit defect map correlated very well with the occurrence of sites with failed breakdown voltage, indicating that this test can be developed into a leading indicator of the cells where device yield will be low. The number of pits detected on the wafer ranged 110-200 total, equates to <2% of the device total, thus it is not possible to draw a correlation between the global within wafer yield and the pit count. Locations of pits in the epilayer were also compared to the micropipe maps. Where large clusters of micropipes occur, frequently pits will form. Generally, pits in the epilayer are randomly distributed and at this time are believed to originate with particle defects transferred to the wafer during the epitaxy process.

While the transistor functional yields were very high, the yield against the targeted threshold voltage value range was near zero. Analysis shows that doping in the drain and channel from the epiwafer lots used to generate the wafers, while consistent, was higher than the targeted value. Much effort was made during the program to perform round

robin testing for layer doping, but tuning of the dopant concentration was not successfully achieved until the last group of wafers delivered and tested at both DCCSS and NGES. These wafers have not been fabricated into devices.

On wafer testing of several epiwafers with Schottky barrier diodes (SBD) was performed during the last quarter of the Year 1 program. Diodes were fabricated without edge termination and 2 mm diameter Ni contacts on 37 sites on the wafer. Diodes were tested for reverse bias leakage current with 100 V bias applied to the diode.

Figure 43 shows the distribution calculated defect density for each wafer based on diodes per wafer with low leakage. The defect density is calculated from the equation

$$\text{Yield} = e^{-A \cdot D}$$

where A=device area and D is the defect density assuming no clustering of defects. Also plotted is the distribution of micropipe density of the wafers. There appears to be four flyers in the dataset, with these excluded, the defect density based on operational diodes is aligned with the expected results from the micropipe defect density.

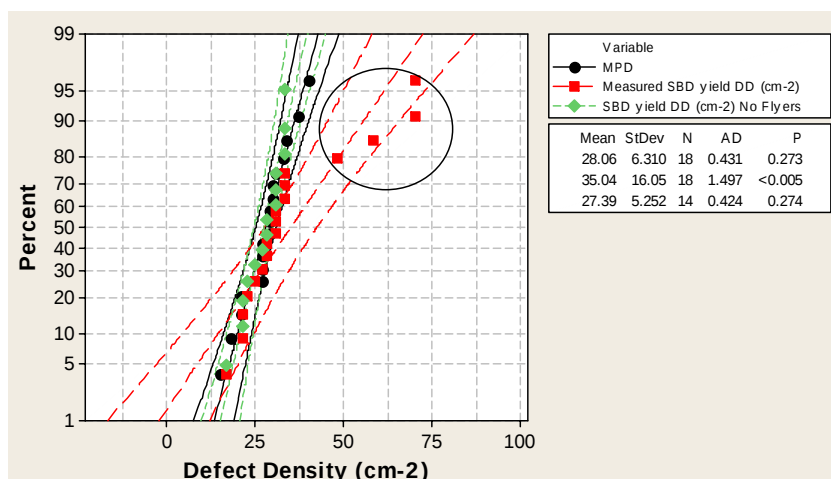


Figure 43: Distribution of defect density values obtained from SBD leakage on 18 4H SiC epiwafers and the distribution of micropipe defect density for the same wafer set. Circled points are outside 2 standard deviations of the SBD defect density distribution and considered flyers (not statistically consistent).

The data in Figure 43 implies that “statistically” the micropipe defect density is the limiting factor in the yields of low leakage diodes for the wafers tested. Inspection of the wafer defect density versus the wafer micropipe density shows a different picture, this is shown in Figure 44.

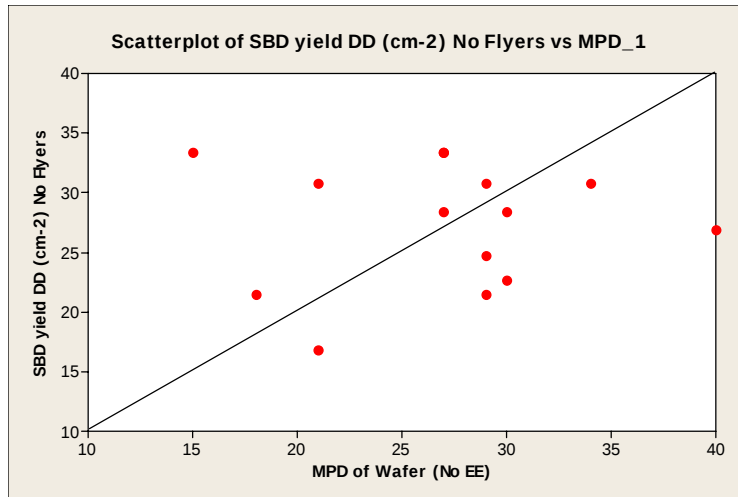


Figure 44: Defect density associated with SBD high reverse leakage failures plotted as a function of the micropipe defect density of the wafer. Flyer wafers highlighted in Figure 43 were removed for this plot.

Figure 44 shows the defect density associated with the count of leaky diodes per wafer does not correlate to the wafer micropipe defect density. Points below the black line indicate that clustering of defects is likely (more than one defect per failed device). Points above the black line have density of killer defects that is higher than the micropipe defect density; these are likely epi pit defects caused by particulates and possibly other crystal defects that reduce the Schottky barrier height.

- **Task 4.2 – Roadmap Development:** The information collected in the various tasks was used to develop and deliver a wafer quality roadmap by the end of the program.

From the data collected in the first year of the KGS program identified three major areas where improvements will directly impact device performance:

- Micropipe density – while not a major factor to limit yield on the JSIT material, the current performance level (20-30/cm²) will have a negative impact on operation of power devices with active areas greater than 2 mm². Micropipe clusters in the wafer appear to increase the occurrence device killing defects (pits) in the epitaxial layers.
- Surface defects in the epitaxial layers (pits) – the defects result in two problems for device fabrication. First, devices fabricated on sites containing pits will not function, and second, pits limit local uniformity of photoresist layers. Local non-uniformity of the photoresist will result in device fabrication errors, and yield loss.
- Epi dopant targeting – non-destructive in process testing of epi dopant targets is key to realizing product which will meet yield and cost expectations.

More device related information will emerge in the second and third quarters of the second year of the program.

Appendix 1 – Tabulated summary of metrics and milestone progress

Key: Green=complete, Yellow=near complete Red=incomplete

KGS Final Progress Against Year 1 Goals

KGS Program Goal Metrics	Status	Top 30% Goal	Top 50% Goal
Timing for 76 mm diameter	Pilot Production	Q1/06	
Timing for 100 mm diameter	100 mm wafers produced, grain boundary count unsatisfactory level = 6 months behind schedule	Q1/07	
MPD and inclusions (cm ⁻²)	MPD Top 50% is <24 cm ⁻² MPD Top 30% is <18 cm ⁻² Inclusions Top 50% is <20 cm ⁻²	<10	<30
Scratches (total length), visual inspection	Met Program goal	<50% diameter	<75% diameter
Areal density surface particles and pits in epiwafers, diameter >0.5 um	LLS Pits <1 cm ⁻² at diameter >25um (test method not mature for <2.5um)	<5 cm ⁻²	<10 cm ⁻²
Bulk Metals Contamination B, Al, Ti, V, Fe (atoms/cm ³)	100% is between 1E15 and 5E15	<1E15	<5E15
Stable Epi drift layer carrier concentration (atoms/cm ³)	100% is less than 5E14 (process development)	<1E14	<5E14
Epi thickness uniformity	100% is less than 8%	<8%	<10%
Epi Doping Uniformity (10 ¹⁵ -10 ¹⁹ /cm ³ layers)	Top 60% is <15%; 20% is <10%	<10%	<15%

KGS Program Chronological Milestones – Year 1

Thrust	Quarter	Milestone
Task 1: SiC Wafer Products	1	50% sliced wafer increase for 76 mm diameter crystals
	2	Complete model of 100 mm PVT growth*
	3	80% sliced wafer increase for 76 mm diameter crystals
	4	Deliver first generation 4H n+ 100mm wafers - DELAYED
Task 2: Materials Applied Research	1	Complete model of Generation1 bulk gas growth
	1	Qualify Batch Epitaxy processes for program
	2	Demonstration of CVT growth
	4	Deliver first 76mm CVT wafers - DELAYED
Task 3: Metrology for Wafer Specifications	2	Implement LLS inspection with particles, pits, and scratches delineated.
	3	Start routine microwave loss inspection of 4H SI wafers
	2	u-PCD tool installed and lifetime measurements implemented for epitaxy layers and SI wafers
Task 4: Device Technology Maturation	1	Publish Rev-0 roadmap for wafer and epi goals
	2	Complete disposition strategy for n+ epiwafers
	4	Publish revised roadmap to reflect power and RF device progress

Appendix 2 - External Papers and Patents

Presented at the 2006 European Conference on SiC and Related Materials, Newcastle England

Scaling of Chlorosilane SiC CVD to Multi-Wafer Epitaxy System

J. Wan, M. J. Loboda, M. F. MacMillan, G. Chung, E. P. Carlson, and V. M. Torres,
Dow Corning Compound Semiconductor Solutions

Carrier lifetime analysis by microwave photoconductive decay (u-PCD) for 4H SiC epitaxial wafers.

G. Chung, M.J. Loboda, M.F. MacMillan, J. Wan and D.M. Hansen, Dow Corning Compound Semiconductor Solutions

Submitted to the 2007 Electronic Materials Conference and to Applied Physics Letters

Evidence of Negative Bias Temperature Instability in 4H-SiC Metal Oxide Semiconductor Capacitors

M. J. Marinella and D. K. Schroder

Department of Electrical Engineering and Center for Solid State Electronics Research,
Arizona State University, Tempe 85287-5706

T. Isaacs-Smith, A.C. Ahvi, and J.R. Williams

Physics Department, Auburn University, AL 36849

G.Y. Chung, J.W. Wan, and M.J. Loboda

Dow Corning Compound Semiconductor Solutions, LLC, Midland, MI 48611

Provisional Patent Application Submitted

“Method of Manufacturing Substrates Having Improved Carrier Lifetime”

US 60/831839

Communicated to ONR via DD Form 882 November 2006

Appendix 3 – Summary of University Subcontractor Efforts.

I. University of Alabama/Birmingham - Dr. M.E. Zvanut

Wafer Mapping of SI SiC: point defects and polytype (UAB)

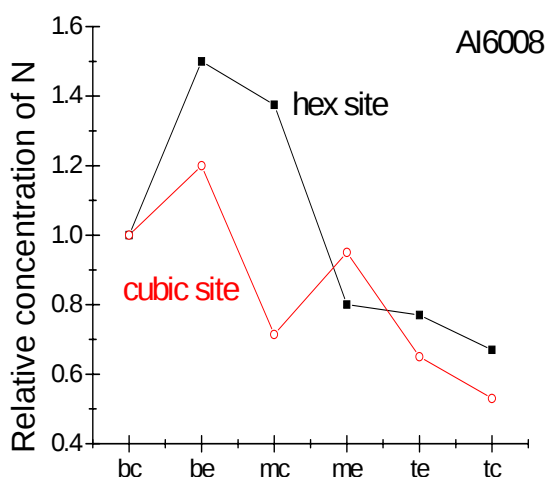


Figure 1. Distribution of substitutional nitrogen in the 4H SiC boule. b, m and t are bottom, middle and top of the boule. c and e are center and edge of the wafer.

The technical objective of this work was to measure the amount and types of point defects distributed across a semi-insulating (SI) SiC wafer and among different wafers by using electron paramagnetic resonance (EPR) spectroscopy.

The only defect observed in the wafers from KGS phase 1, without illumination, was substitutional nitrogen at the cubic and hexagonal sites. The nitrogen detected under the measurement conditions primarily represents the uncompensated nitrogen. The nitrogen distribution varies by no more than 50% across one wafer and throughout the boule. A representative nitrogen distribution is shown in Figure 1, where the unfilled circles represent the cubic site nitrogen and the filled squares are the hexagonal site.

Several intrinsic defects were detected using laser irradiation at 532 nm and 5 mW. The types of defects and their concentration as well as measured nitrogen concentrations are listed in Table 1.

Table 1. Concentrations of various defects.

Concentration	AG5024-04 (pre-start)	AI6008 (1 st Q)	AQ6029-08 (2 nd Q)	AI66033-04 (2 nd Q)	AQ6030 (2 nd Q)	AQ6035-01 (3 rd Qrt)
Nitrogen (10 ¹⁶ cm ⁻³)	< 0.1	2	0.4	4	<0.1	<0.1*
V _C ⁺	5x10 ¹⁴ cm ⁻³	?	?	?	?	?
V _{Si} (10 ¹⁵ cm ⁻³)	ND	ND	1	ND	1	0.5
P6	ND	1	ND	1	ND	Maybe?
X 10 ¹⁴ -10 ¹⁵ cm ⁻³	ND	0.5	ND	1	ND	ND

The type of defect depends on the uncompensated nitrogen concentration. V_C⁺ was only observed in the 6H SI wafer (AG5024-04) and the '?' means that V_C⁺ was not seen in the dark, but not all illumination conditions have been tried. V_{Si} was only observed in the UID samples with the

lowest N concentration. X defect is commonly seen in N-doped SiC and has been suggested to be a N-N pair. Several experimental observations lead to the conclusion that the center is not the same as the substitutional nitrogen donor. The concentration of X

defect scales with the SIMS measured nitrogen doping concentration rather than Nd-Na from C-V measurements as expected for a nitrogen pair-related center. In conclusion, the only point defect from all UID wafers was substitutional nitrogen at the cubic and hexagonal sites without illumination. The type of defect with illumination depends on the uncompensated nitrogen and V_c^+ was not observed in the 4H UID samples. X defect is not the same as the substitutional nitrogen donor and correlates with the SIMS measured nitrogen doping concentration as a nitrogen pair-related center.

II. University of South Carolina - Dr. T. Sudarshan

SiC Epiwafer Quality Assessment by Device Performance

The primary objective is to assess the quality of Dow Corning SiC epiwafers by fabricating SBD and PiN diodes on the epiwafers, performing electrical testing and failure analysis, and by performing defect-device performance correlation analysis using KOH etching and the Electron Beam Induced Current (EBIC) mode of SEM. SBDs and epitaxial PiN diodes with diameter of 300 and 150 μm on the quarter segments were fabricated.

SBD reverse characteristics have been correlated with various defect types. Figure 1 (a) shows dependence between number of screw dislocations and threshold voltage at 10^{-2} A/cm^2 for SBDs on the 10 μm epitaxial wafer. Devices containing few screw dislocations (<5) exhibited wide spread of blocking voltages and show no correlation with threshold voltage. Presence of other type of defects was examined on these devices and summarized in fig. 1 (b). Leakage current for the devices containing zero or one screw dislocations increases as the number of threading edge dislocations increases. However, overall dependence between the leakage current density and number of TEDs shows wide spread of leakage current which means that TEDs are not the only detrimental factor in the leakage current of the tested SBDs. No correlation was found between number of BPDs and reverse characteristics. Grain-boundaries and 3C inclusions formed during epi growth were found to degrade reverse blocking voltages.

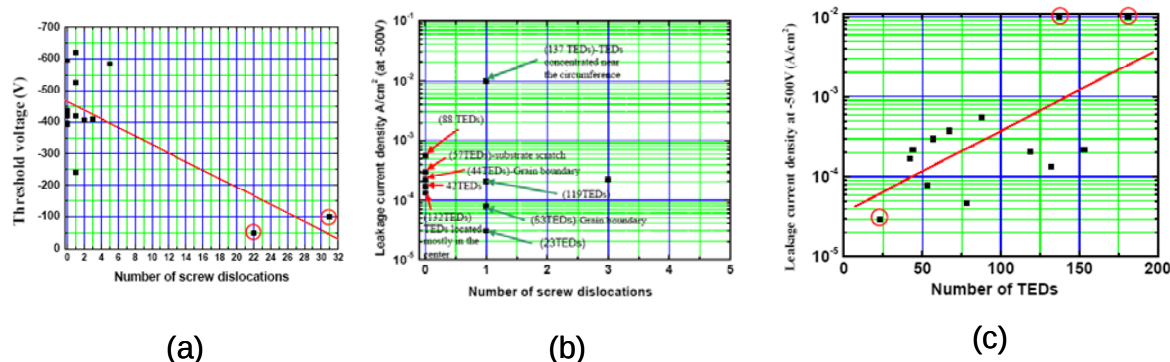


Figure 1. Reverse characteristics and number of defects. (a) number of screw dislocation vs. threshold voltage (b) number of TED is included (c) number of TED vs. leakage current at reverse bias of 500V.

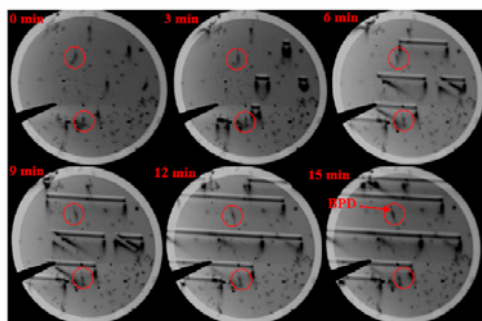


Figure 2. Chronological EBIC images for the mesa-isolated epitaxial PiN diode.

Stacking fault development was visualized using EBIC during the degradation test ($100\text{A}/\text{cm}^2$ for 15 min) on PiN diodes. The typical forward voltage drift for 15 minutes of degradation was a bout 0.7V. Figure 2 shows the chronology of EBIC images and some BPDs initially present within device active area did not develop into SFs (circled in red).

In conclusion, some correlation has been observed between number of screw and edge dislocations and SBD reverse characteristics. Grain-boundaries and 3C inclusions were found to degrade SBD reverse blocking capability.

PiN diodes show forward drop degradation with SF development from BPDs. It was observed that some of BPDs do not develop SFs and additional work needs to understand BPD propagation mechanism with forward bias stressing in the second year.

III. Arizona State University – Dr. D. Schroeder

SiC Carrier Generation Lifetime Measurements

The major focus has been the characterization of generation lifetime with pulsed Metal Oxide Semiconductor (MOS) capacitors. Oxide leakage current and interface state density (D_{it}) are also examined. Some of the first evidence of negative bias temperature instability (NBTI) in SiC was observed, which may play an important role in MOS and IGBT devices. 4H-SiC n-type samples with an epitaxial layer thickness of $20\text{ }\mu\text{m}$ and a doping concentration of 10^{16} cm^{-3} were used and Lifetimes were extracted by the Zerbst plot technique at 400°C . One of the samples and measured generation lifetime data are shown in Fig 1.

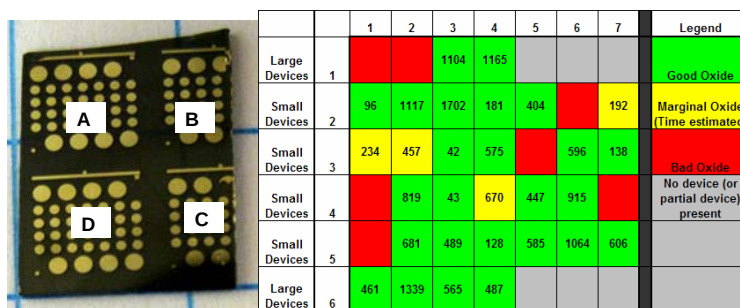


Figure 1: (a) Micrograph of 4H-SiC sample and (b) generation lifetime map for one quadrant. Lifetimes are given in ns.

Recombination lifetime also was measured by TR-PL at NRL. TR-PL clearly has fundamental differences from the pulsed MOS-C method, and the two methods gave somewhat different results. Average generation and recombination lifetimes from the tested sample are 1489 and 605 ns, respectively. Standard deviation of generation lifetime

is two orders of magnitude higher than that of recombination lifetime. The reason for the differences is currently under investigation. Previously generation lifetimes between 10 and 45 ns were reported with 6H-SiC MOS capacitors and higher generation lifetimes from this work might be related with less electrical defects in epitaxial layers. The reason for the differences is currently under investigation.

It is observed that if two generation lifetime measurements are made consecutively at the same temperature, there is a significant change in recovery time – indicating that the lifetime has decreased. Results of several consecutive pulsed MOS measurements are given in Fig. 2(a). We believe that this behavior is due to negative bias temperature instability (NBTI). NBTI is a significant reliability concern of the Si semiconductor industry. When an MOS capacitor is biased with a negative gate voltage while at high temperatures, holes at the semiconductor-oxide interface in conjunction with the oxide electric field cause an increase in the density of interface states, leading to a decrease in lifetime. To validate this theory, conductance measurements were made between the pulsed MOS measurements (Fig. 2(b)), indicating an increase in D_{it} .

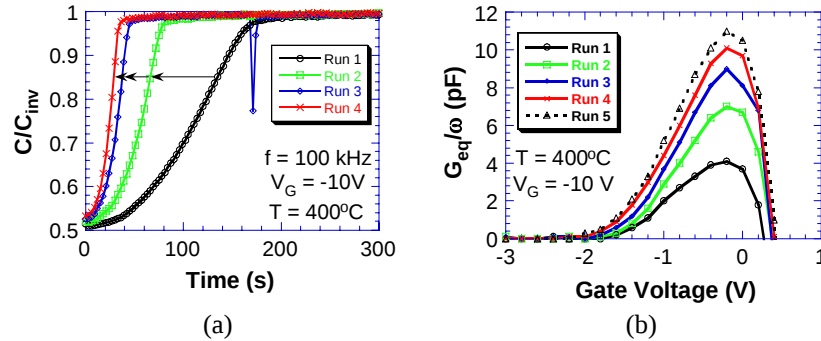


Figure 2: (a) Decreasing MOS-C transient times for consecutive measurements on a single device and (b) corresponding conductance versus gate voltage curves indicating increasing D_{it} .

In conclusion, we have mapped the generation lifetime and leakage current and compared results with recombination lifetime measurements. The difference between these results is the subject of ongoing investigation. We noted evidence of NBTI in SiC and devised a novel technique for measuring leakage current. Correlating lifetime data with material defects is underway.

IV. Carnegie Mellon University – Dr. M. Skowronski

HR-XRD and TEM Crystal Defect Analysis

Carnegie Mellon University (CMU) proposed to perform structural and electrical characterization of silicon carbide wafers and crystals grown by Dow Corning Compound Semiconductor Solutions (DCCS), Inc. Extended defect densities and distribution maps were produced by x-ray topography, KOH etching, High Resolution X-ray Diffraction (HRXRD) and Transmission Electron Microscopy (TEM). Based on the above tests, nucleation mechanisms of slip bands and bending of the basal planes in 4H-SiC boules

were identified. Electrical characterization was focused on determination of deep levels spectra.

SiC boules produced by the DCCS PVT process exhibited bending of the basal planes. HRXRD of 4H wafers shows the position of the reflection shifted across the 3 inch wafer by 1-2°. This basal plane bending was proposed to be due to the presence of plastic deformation induced basal plane dislocations with at least partial edge character. The sign of bending (concave toward the growth surface) would have to correspond to extra half planes of dislocations pointing toward the seed wafer (Figure 1). The estimated net density of 60° BPDs on the prismatic face of the boule corresponding to a radius of curvature of 1.7 m, was $2.2 \times 10^5 \text{ cm}^{-2}$.

Dislocation distribution across the 3 inch wafers off cut by 8° was determined by KOH etching. The average densities of screw, threading edge, and basal plane dislocations were $5 \times 10^2 \text{ cm}^{-2}$, $7 \times 10^4 \text{ cm}^{-2}$, and $1 \times 10^5 \text{ cm}^{-2}$, respectively. This density of BPDs on the wafer surface corresponds to $8 \times 10^5 \text{ cm}^{-2}$ on the prismatic face of the boule. This puts the actual density about 3-4 times larger than the estimated density from the crystal bending, which accounts for the fact that some of the dislocations could be of screw character. One of the characteristic features observed on etched surfaces were the parallel arrays of basal plane dislocations extending in directions perpendicular to the off cut direction (Figure 2). Such arrays have been previously interpreted as slip bands corresponding the primary slip system in hexagonal silicon carbide [1].

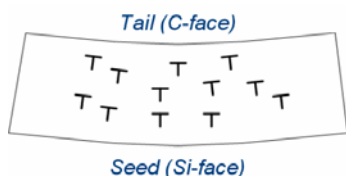


Figure 1

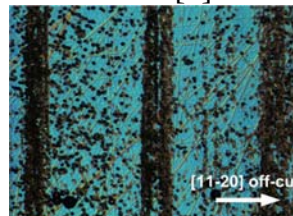


Figure 2

Figure 1: Basal plane bending in 4H-SiC DCCS boules and the corresponding distribution of basal plane dislocations. Figure 2 Optical image of basal plane slip bands as vertical lines of etch pits in a DCCS 4H-SiC wafer.

The interpretation discussed above was tested in a TEM experiment. Several plan view samples were prepared from the part of the wafer exhibiting slip bands and carefully positioned in such a way as to contain the slip band dislocations in the thin section of the specimen. TEM allowed for the identification of the dislocations as partial edge dislocations with the extra half plane extending toward silicon face of the crystal. Since this particular boule was grown on the carbon face, this observation conclusively supports the model presented in Figure 1.

The correlation of the global bending of the basal planes and primary slip mechanism in SiC as-grown boules implies that the crystals were deformed by the macroscopic stress resulting from the thermal gradients imposed on the crystal during growth process. The sign of bending is in agreement with the sign of the shear stress distribution modeled in DCCS growth process.

Deep center types and concentrations were monitored on DCCS n-type 6H and 4H-SiC boules. Two distinct differences were observed between the two polytypes. First, the overall concentration of deep centers in 6H appeared to be higher than that of 4H. Secondly, the uniformity of center distribution was much better in 4H compared to 6H-

SiC. Both changes are likely due to the growth polarity. 6H-SiC boules were grown on the Si face while 4H on the C-face. Since most electron traps are known to be associated with excess silicon in the crystal [2] (C vacancies, Si antisites, etc) and exhibit site competition mechanisms [3], the availability of Si sites during 6H growth is consistent with observed effects.

References:

1. Ha, S., et al., J. Appl. Phys. 92: 778 (2002)
2. Li, Q., et al., Applied Physics Letters. 86: 202102 (2005)
3. Larkin, D.J., et al., Appl. Phys. Lett. 65: 1659-1661 (1994)

V. State University of New York – Dr. M. Dudley

XRT and TEM Analysis of Crystal Defects

Stony Brook University

Stony Brook University was given the task of studying the threading defect replication/modification during the CVD growth of silicon carbide single crystals using plan-view Synchrotron Wide Beam X-ray Topography (SWBXT) and TEM. This included the plan-view SWBXT study of replication/dissociation of MPs during epilayer growth; cross-sectional SWBXT study of replication/modification of TDs after epitaxial growth; computer modeling of the SWBXT images of MP after dissociation into 1c Threading screw dislocation (TSD) cluster; TEM study of MP dissociation after epilayer growth.

SWBXT studies have been carried out at various processing stages during the development of n- n⁺ - n⁻ type device structures. Plan view topography was initially carried out on ten 3 inch, n type substrates. This was then repeated on eight of the ten following the growth of a 50 micron thick n⁺ buffer layer and then again for seven out of the eight following the growth of a 20 micron thick n- drift layer. One of the wafers was used to provide cross sectional samples for SWBXT and plan view samples for TEM studies of micropipe closing.

Generally, plan-view SWBXT shows that very few MPs are modified during epitaxial growth. Comparison of topographs before and after epi-growth shows that only a few hollow cores are closed during the CVD deposition. However, optical examination of the epi surface suggests that over 90% of micropipes have dissociated to a defect with no empty core. By comparing the KOH etch pit patterns before and after CVD growth, etch pit clusters were observed in the MP region after CVD growth. MPs probably have dissociated into TSDs, although plan-view grazing-incidence SWBXT does not show significant change before and after CVD growth. Optical images of cross-sectional samples also verify that some hollow cores are closed after epitaxial growth. Specific cases were studied (see image below) in both plan-view and cross-section. The observation of the dissociation is complicated because the dissociated TSDs are close to each other and their strain fields overlap.

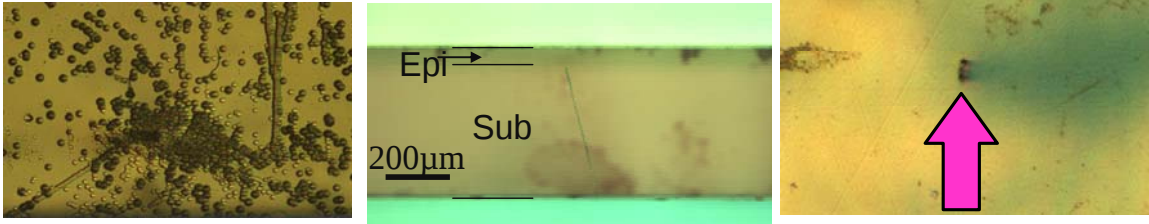


Figure 1. Optical images showing the dissociation of MPs into closed-core TSDs. Left: KOH etch pattern on the epilayer surface; middle: cross sectional view of the closing of MP at the substrate-epilayer interface; right: MP from the back side (C-face) of the wafer.

The “ray-tracing” method has been used to simulate the image of MP before and after dissociation in grazing-incidence SWBXT. When a MP with Burgers vector $n \cdot b$ is dissociated into n elementary TSDs which are close to each other, the total displacement field, which is the combination of those of all the TSDs, is what contributes to the SWBXT image. Simulations indicate that significant changes are not expected on SWBXT images when such dissociation occurs. Therefore, although no significant change of the images of MPs might be observed, this does not necessarily mean that the MPs are not dissociated since the overlapping strain fields of independent elementary TSDs result in similar SWBXT images.

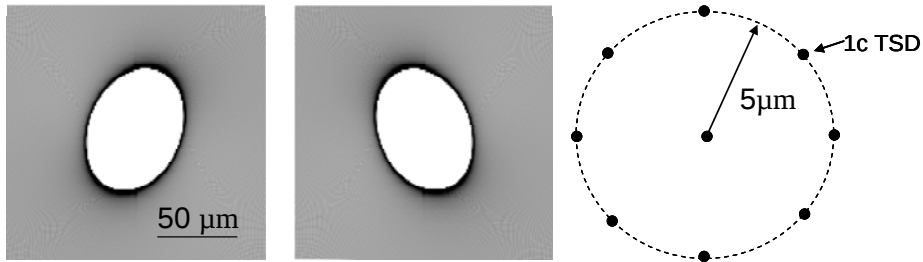


Figure 2. Ray-tracing simulated images of dissociated 1c TSD cluster. The simulated image elementary TSD cluster which consists of n number of 1c TSDs appears as the same configuration as a MP with Burgers vector $n \cdot c$ (see Fig. 10). The configuration of the 1c TSDs is shown in the right image.

Appendix 4 – Expensed Wafers and Disposition

Wafer ID	Wafer type/ Orientation	Res type	Epitaxial layer	Intended Usage	Location of Material
AI6016-09	76mm 4H / 8°	N+	----	Inspection wafer	NGES
AN6009-02	76mm 4H / 8°	N+	----	Inspection wafer	NGES
AI6015-08	76mm 4H / 8°	N+	Yes	Epi characterization	NRL
AN6015-07	76mm 4H / 8°	N+	Yes	Epi characterization	NRL
AQ6015-02	76mm 4H / 8°	N+	Yes	Epi characterization	CMU
AI6015-07	76mm 4H / 8°	N+	----	Program Deliverable	ONR
AN6015-06	76mm 4H / 8°	N+	----	Program Deliverable	ONR
AQ6015-08	76mm 4H / 8°	N+	----	Program Deliverable	ONR
AI6015-12	76mm 4H / 8°	N+	Yes	Device Fabrication (SBD)	DCCSS
AI6016-05	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6016-08	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5048-03	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5048-06	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6015-09	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6015-10	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6015-11	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6016-12	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6016-13	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AN6009-03	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AX5050-04	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AX5050-06	76mm 4H /	N+	Yes	Device Fabrication	NGES

	8°			(SIT)	
AI5050-03	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6028-01	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6028-07	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AX5050-02	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6026-09	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5048-02	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5048-05	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5050-07	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AN6028-02	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6026-02	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5048-08	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6028-05	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AN6028-03	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AX5050-11	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6026-07	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5050-09	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI5050-06	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6026-01	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6028-06	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6026-10	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AI6030-10	76mm 4H / 8°	N+	Yes	Epi characterization	NRL
AX6025-03	76mm 4H / 8°	N+	Yes	Epi characterization	NRL
AX6024-03	76mm 4H /	N+	----	Program	ONR

	8°			Deliverable	
AX6025-05	76mm 4H / 8°	N+	----	Program Deliverable	ONR
AX6026-01	76mm 4H / 8°	N+	----	Program Deliverable	ONR
AX6028-09	76mm 4H / 8°	N+	----	Program Deliverable	ONR
AX6029-01	76mm 4H / 8°	N+	----	Program Deliverable	ONR
AJ6026-02	76mm 4H / 8°	N+	Yes	Device Fabrication (SBD)	USC
AX6026-04	76mm 4H / 8°	N+	Yes	Device Fabrication (SBD)	USC
AQ6040-12	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AQ6043-08	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
BH6045-07	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
BH6045-11	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AN6040-11	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AQ6043-03	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AQ6043-10	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AX6047-04	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AX6044-01	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
BH6045-03	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AQ6041-02	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AQ6041-04	76mm 4H / 8°	N+	Yes	Device Fabrication (SIT)	NGES
AQ6038-05	76mm 4H / 8°	UID	----	NRL Epi Development	NRL
AQ6038-06	76mm 4H / 8°	UID	----	NRL Epi Development	NRL
AQ6038-07	76mm 4H / 8°	UID	----	NRL Epi Development	NRL
AQ6038-09	76mm 4H / 8°	UID	----	NRL Epi Development	NRL
AB6048-01	100mm 4H /	N+	----	Program	ONR

	4°			Deliverable	
AB6047-02	100mm 4H / 4°	N+	----	Program Deliverable	ONR
AB6047-01	100mm 4H / 4°	N+	----	Program Deliverable	ONR
AJ6061-01	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AJ6061-10	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AJ6061-11	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6049-02	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6049-03	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6049-04	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6049-06	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6049-09	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6052-01	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6052-04	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AQ6052-05	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6055-01	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6055-02	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6055-03	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6055-04	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6055-05	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6055-06	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6055-07	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6057-04	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6057-05	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AX6057-06	76mm 4H /	N+	----	Program	ONR

	0°			Deliverable	
AZ6065-01	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6052-01	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6052-02	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6052-03	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6052-05	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6052-06	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6052-07	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6052-08	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6055-01	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6055-02	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6055-03	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6056-04	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6056-05	76mm 4H / 0°	N+	----	Program Deliverable	ONR
BH6056-07	76mm 4H / 0°	N+	----	Program Deliverable	ONR
AJ6062-02	76mm 4H / 8°	N+	----	NRL Epi Development	NRL
AJ6062-04	76mm 4H / 8°	N+	----	NRL Epi Development	NRL
AJ6062-10	76mm 4H / 8°	N+	----	NRL Epi Development	NRL
AQ6058-01	76mm 4H / 8°	N+	----	NRL Epi Development	NRL
AX6062-03	76mm 4H / 8°	N+	----	NRL Epi Development	NRL
AI6015-06	76mm 4H / 8°	N+	Yes	Device Fabrication (PIN)	DCCSS