Q1 Known Good Substrates Technical Report
CONTRACT/PR NO. N00014-07-C-0918 Dow Corning Corporation
Quarterly Technical Report
Reporting Period: 1 Sept 2007 – 30 Nov 2007

Executive Summary

The Known Good Substrates (KGS) Phase II program was initiated 1 September 2007. There was a delay between the Phase I program end of over 6 months. All Phase II subcontractors were under contract by December 2007. Appendix 1 shows the subcontractors and their focus areas in the program.

Technical Progress

The following table documents the key program end metric goals.

Metric	50th Percentile	20th Percentile
MPD distribution 4H n+ 76 mm diameter (cm^{-2})	10	5
MPD distribution 4H n+ 100 mm diameter (cm^{-2})	20	10
Net scratch length by LLS relative to wafer diameter (%)	40	20
Equivalent Epitaxy Defect Density 76 mm diameter (cm^{-2})	<10	<5
Epitaxy Doping Target Accuracy	+/- 25%	+/-10%
Epitaxy Doping Variation within wafer (Max-Min/Min, %)	35%	10%
Substrate Resistivity Maximum 4H n+ 76mm	0.025	0.020

Progress Against Metrics

The following charts show early progress against the program metrics. Due to extended processing cycles, data tends to become available 4-6 weeks in the rears.

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14. ABSTRACT
The Known Good Substrates (KGS) Phase II program was initiated 29 August 2007. Wafer, epitaxy, modeling and metrology work has been the main focus of efforts in Q1. This technical report summarizes the progress by all team members against the tasks and milestones.

15. SUBJECT TERMS
SiC wafer, SiC epitaxy, SiC material metrology

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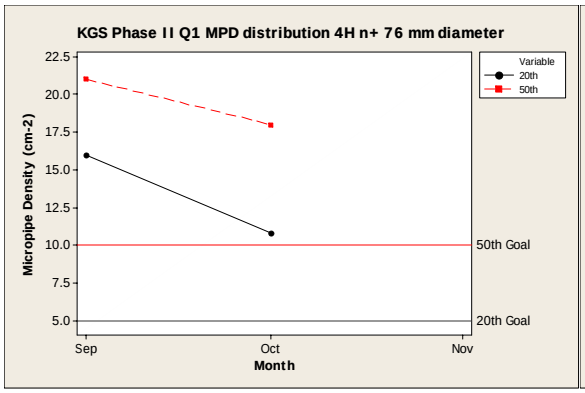
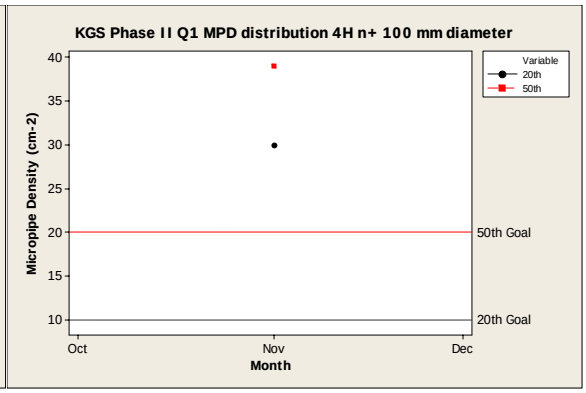
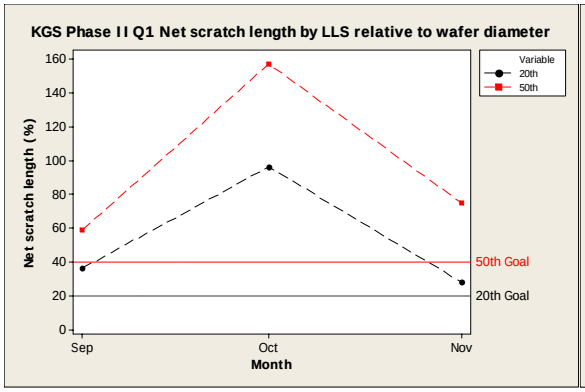
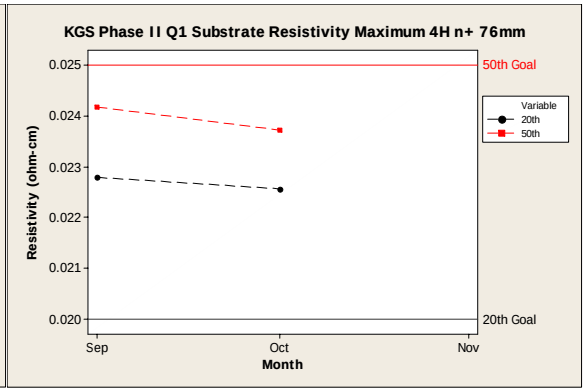
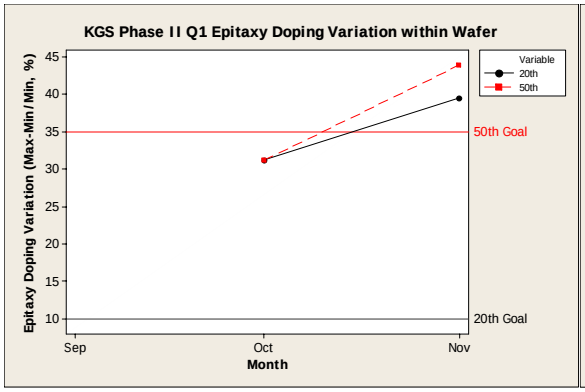
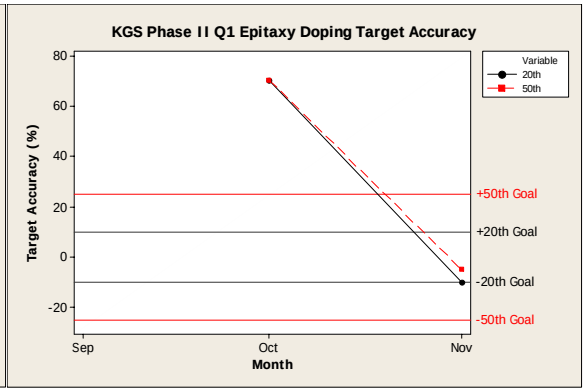

KGS Phase II Q1 MPD distribution 4H n+ 76 mm diameter
Micropipe Density (cm-2)
22.5
20.0
17.5
15.0
12.5
10.0
7.5
5.0
Sep
Oct
Nov
Month
Variable
20th
50th
50th Goal
20th Goal

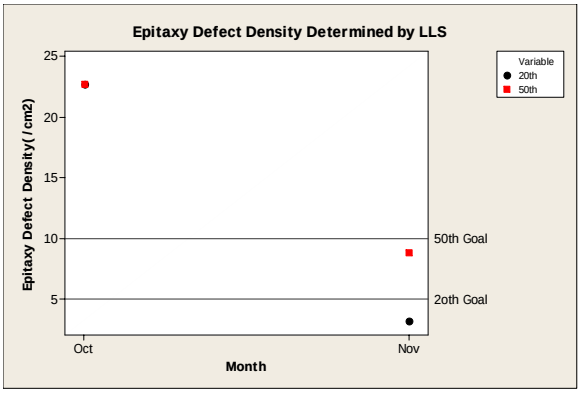

KGS Phase II Q1 MPD distribution 4H n+ 100 mm diameter
Micropipe Density (cm-2)
40
35
30
25
20
15
10
Oct
Nov
Dec
Month
Variable
20th
50th
50th Goal
20th Goal


KGS Phase II Q1 Net scratch length by LLS relative to wafer diameter
Net scratch length (%)
160
140
120
100
80
60
40
20
0
Sep
Oct
Nov
Month
Variable
20th
50th
50th Goal
20th Goal


KGS Phase II Q1 Substrate Resistivity Maximum 4H n+ 76mm
Resistivity (ohm-cm)
0.025
0.024
0.023
0.022
0.021
0.020
Sep
Oct
Nov
Month
Variable
20th
50th
50th Goal
20th Goal


KGS Phase II Q1 Epitaxy Doping Variation within Wafer
Epitaxy Doping Variation (Max-Min/Min, %)
45
40
35
30
25
20
15
10
Sep
Oct
Nov
Month
Variable
20th
50th
50th Goal
20th Goal


KGS Phase II Q1 Epitaxy Doping Target Accuracy
Target Accuracy (%)
80
60
40
20
0
-20
Sep
Oct
Nov
Month
Variable
20th
50th
+50th Goal
+20th Goal
-20th Goal
-50th Goal


Epitaxy Defect Density Determined by LLS
Epitaxy Defect Density(/ cm2)
25
20
15
10
5
Oct
Nov
Month
Variable
20th
50th
50th Goal
2oth Goal

With respect to metrics, MPD values are tracking down toward goals, polishing defects oscillate about goals. Resistivity is in range and epitaxy defectivity moving down toward goals. 4H n+ 100 mm and 4H UID 76mm growths are performed at about a 1:10 ratio to 4H n+ 76mm crystal growths. Details by task follow:

Task 1: SiC Wafers Products

Highlights:

- Pareto analysis performed on bulk SiC growth monthly has identified problems with the formation of pinholes as a primary defect. Failure analysis, and modeling at DCCSS identified undesirable radial gradient in the reaction cell resulted in pinhole and cluster micropipe formation at crystal perimeter. Alterations to the reaction cell were implemented in October. Results obtained on first dozen growths show desired improvements. Early results of MPD data for November are now tracking close to 10/cm2.

Roadblocks:

- Pinhole problems in crystal growths during Sept limited material available for use in program. Supply of wafers into epitaxy for KGS projects is about 6-8 weeks behind schedule. Wafers stock is now replenishing and epitaxy growths for delivery of wafers to subs will begin in late December.

Task 2: Continuous Improvements in SiC Substrates

Highlights

- UID 4H material achieved ~$5x10^{15}$ cm^3 nitrogen concentration by SIMS measurements.
- Next generation SiC crystal growth process under development for the past year at DCCSS is now moving to pilot scale volume (4-10 runs/month). Initial MPD values are <5/cm2 on several crystals. Mosaicity and lattice curvature appear to be improving 2x per run. The new process also exhibits significantly more efficient nitrogen incorporation and can help to meet program resistivity reduction targets.
- Detailed measurements and models made of the growth furnace RF heat source show routes to improve growth variability. Results will be fed into the SiC growth mathematical model to improve the accuracy of the model relative to growth data.

Roadblocks

- While consistently low N and B levels are found in DCCSS 4H undoped SiC, levels consistent with semi-insulating SiC, material yields to electrical specifications vary significantly. Support from partners will be used to see if the variations can be traced to inconsistent concentrations of deep level impurities.

Task 3: Metrology for Wafer Specifications.

Highlights

- Thick (100+ um) CVT grown epilayer films were deposited on 76mm C-face 4H n+ substrates. Growth rates were nominally 50 um/hr. Microwave photoconductive decay tests were performed and show lifetimes of about 1.15 μsec with the uniformity of 9% (sigma/mean) and indicate low concentration of deep centers in CVT materials. We believe these are high lifetime values based on reports in the literature, especially considering the high growth rates.
- Laser light scattering (LLS) image analyses algorithms used to assess post epitaxy defect impact on epiwafers have now been applied to bare wafers. Strong correlations with MPD are observed and when the data is compared to post epitaxy it is now possible to get better assessment of the defects which emerge during epitaxy. This method can be applied now to every wafer and allow us to gain a large statistical dataset which can be used to better screen incoming bare wafers and also assess performance of epitaxy.

Task 4: Device Technology Maturation

MOS and SBD characterization

- The ratio of the generation to recombination lifetime is much different in SiC compared to Si. Activation energy calculated from SiC generation lifetimes shows that traps with energy levels near mid-gap dominate the generation lifetime. Comparison of both generation and recombination lifetimes and dislocation counts measured in the device area show no correlation in either case.
- Local surface defect patches can account for large generation lifetime variations at the constant dislocation density. Schottky barrier height and ideality factor variations from SBD tests supports local lower barrier height are associated with the patches of defects.

Progress Toward Milestones for End of Program (Sub-bullets are progress this quarter)

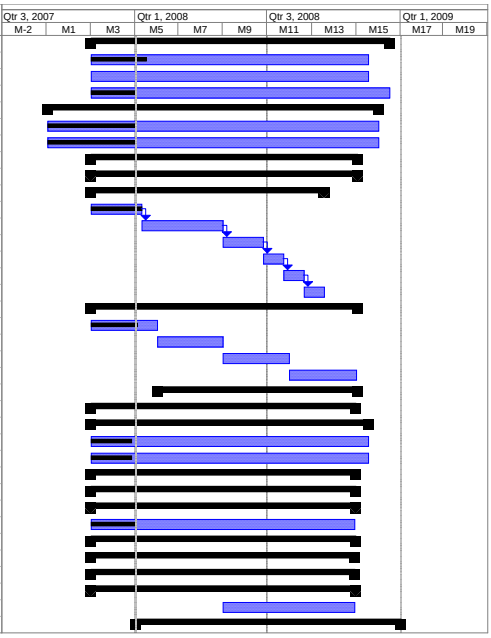
- Correlation Maps of PiN forward IV characteristics and recombination lifetime
- Correlation of PiN forward IV characteristics and n+ epitaxial buffer layer/MP blocking
- Primary SiC material defect limiting PiN performance (Roadmap input - GeneSiC)
    - Epiwafers in device fabrication
- SiC materials parameter assessed as most important for SIT performance improvements based on wafer probe data (Roadmap input - NGES)
    - Wafers in polish line, growths due in early January
- SiC materials parameter assessed as most important for SBD performance improvements based on wafer probe data (Roadmap input - Microsemi)

    - Ten of twenty wafers complete and in queue for epi – MPD ranges 11-14/cm2 which is the lowest range of any epiwafer group produced by DCCSS
- Generational improvement of 4H SiC wafer crystal quality summarized by XRT and MPD analysis
    - Growths in progress
- Assessment of oxide quality for 76mm/100mm 4H epiwafers and link to generation lifetime
    - Epiwafers to ship to subcontractors in January

Schedule

A detailed description of achievements and progress against milestones and deliverables was provided above. The project schedule is provided below as an overview of the progress against the high level tasks on the program. Progress is on track in all areas. Expect to see subcontractor activities really ramp up beginning in December.

ID	WBS	Task Name	Duration	Start	Finish
1	**1**	**SiC Wafer Products**	**294 days**	**11/1/07**	**12/16/08**
2	1.1	76mm SiC Crystal HVM Epiwafer Fabrication	13 mons	11/1/07	11/17/08
3	1.2	100mm SiC Crystal HVM Epiwafer Fabrication	13 mons	11/1/07	11/17/08
4	1.3	Wafer Fabrication Failure Analysis	14 mons	11/1/07	12/16/08
5	**2**	**Continuous Improvements in SiC Substrates**	**325.5 days?**	**9/3/07**	**12/1/08**
6	2.1	76mm Diameter 4H SiC Crystal Wafer Pilot	15.5 mons	9/3/07	12/1/08
7	2.2	100mm Diameter SiC Crystal Wafer Pilot	15.5 mons	9/3/07	12/1/08
8	**2.3**	**Demonstration of Process Limits for Growth of SiC Crystals & Epiwafers**	**262 days?**	**11/1/07**	**11/3/08**
9	**2.3.1**	**Process Modeling and Analytical Testing**	**262 days?**	**11/1/07**	**11/3/08**
10	**2.3.1.1**	**Fluxtrol - Modeling, Analysis & Recommendation on Induction Coil**	**230 days**	**11/1/07**	**9/17/08**
11	.3.1.1.1	Stage 1: Characterize the current production induction coils	10 wks	11/1/07	1/9/08
12	.3.1.1.2	Stage 2: Design of improved induction coil	16 wks	1/10/08	4/30/08
13	.3.1.1.3	Stage 3: Engineering and manufacturing of improved coil	8 wks	5/1/08	6/25/08
14	.3.1.1.4	Stage 4: Study of improved coil in Fluxtrol laboratory	4 wks	6/26/08	7/23/08
15	.3.1.1.5	Stage 5: Coil tests at Dow Corning on real machines	4 wks	7/24/08	8/20/08
16	.3.1.1.6	Stage 6: Final report development and future project planning	4 wks	8/21/08	9/17/08
17	**2.3.1.2**	**STR - Modeling of SiC Bulk Crystal Growth & Epitaxy**	**262 days?**	**11/1/07**	**11/3/08**
18	.3.1.2.1	Q1: Modelling Support for Fluxtrol, Chemistry, & CVT	66 days	11/1/07	1/31/08
19	.3.1.2.2	Q2: Continue Modeling, Optimize Models	64 days	2/1/08	4/30/08
20	.3.1.2.3	Q3: Continue Modeling, Optimize Models	66 days	5/1/08	7/31/08
21	.3.1.2.4	Q4: Continue Modeling, Optimize Models	66 days?	8/1/08	10/31/08
22	**.3.1.2.5**	**Reporting**	**196 days**	**2/1/08**	**11/3/08**
27	**2.3.1.3**	**SUNY - Defect Structure Evolution & Correlation to Device Performance**	**261 days**	**11/1/07**	**10/31/08**
33	**3**	**Metrology for Wafer Specifications**	**273 days**	**11/1/07**	**11/17/08**
34	3.1	Non-destructive LLS testing of Wafer & Epi defects	13 mons	11/1/07	11/17/08
35	3.2	Lifetime Mapping	13 mons	11/1/07	11/17/08
36	**4**	**Device Technology Maturation**	**261 days**	**11/1/07**	**10/31/08**
37	**4.1**	**Device Fabrication**	**261 days**	**11/1/07**	**10/31/08**
38	**4.1.1**	**PiN Diode**	**261 days**	**11/1/07**	**10/30/08**
39	4.1.1.1	GeneSiC - PiN Fabrication & Device Failure Analysis	52 wks	11/1/07	10/29/08
40	**4.1.1.2**	**ASU - Processing, Characterization, and Mapping of SiC Epiwafers**	**261 days**	**11/1/07**	**10/30/08**
55	**4.1.2**	**Schottky Barrier Diode**	**260 days**	**11/1/07**	**10/29/08**
57	**4.1.3**	**Static Induction Transistor**	**260 days**	**11/1/07**	**10/29/08**
59	**4.1.4**	**MOS Technology**	**261 days**	**11/1/07**	**10/31/08**
69	4.2	Roadmap Development	26 wks	5/1/08	10/29/08
70	**5**	**Program Management**	**262 days**	**1/1/08**	**1/1/09**



Program Management

Efforts in Q1 have focused on ramping up internal activities as well as negotiating subcontract agreements. Six of nine subcontracts were in place in Q1 with the final three agreements expected to be in place early in Q2. Epi reactor materials have been ordered and some subcontractor invoices have started to come in for processing.

Appendix 1: KGS Subcontractors and Quarterly Progress Points

Subcontractor	Area of Focus	Progress This Quarter
Northrup Grumman Electronics Systems	J-SIT fabrication and testing	Contract negotiations near completion, epi specifications communicated
Microsemi	SBD fabrication and testing	Now under contract, epi specifications communicated
GeneSiC Semiconductors	PiN diode fabrication and testing	Now under contract, epi wafers delivered
SUNY – Stoney Brook	Crystal Structure of SiC	Performing first rounds of XRT tests on PVT material
Arizona State University	SiC Oxides, carrier lifetime and device failure analysis	Completing comparison of barrier height tests pre and post oxidation
Fluxtrol	Modeling and design of high uniformity induction heating systems	Modeling of coil design on PVT furnace shows about 10-15% in power density exists across furnaces used in program. Now designing alterations to coils to reduce variations.
NRL	SiC Oxides, Epitaxy, Lifetime testing, materials testing, device testing	LTPL data shows mid-year 4H SiC growths exhibits spectral signature comparable to benchmark semi-insulating SiC.
STR	Modeling of CVD and PVT SiC Growth Processes	Initiated modeling of epitaxy process and PVT growth variations due to coil variations.

Publications

Charge Bursts through Dielectric Layers of 4H-SiC/SiO_2 Metal Oxide Semiconductor Capacitors - M.J. Marinella, D.K. Schroder, G.Y. Chung, M.J. Loboda, T. Isaacs-Smith, and J.R. Williams – ONR Approval 43-583-07,

- Submitted to IEEE Int'l Reliability Physics Symposium