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THESIS

FIELD PROGRAMMABLE GATE ARRAY CONTROL OF POWER SYSTEMS IN GRADUATE STUDENT LABORATORIES

by

Joseph E. O'Connor

March 2008

Thesis Advisor:	Alexander Julian
Second Reader:	Roberto Cristi

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FIELD PROGRAMMABLE GATE ARRAY CONTROL OF POWER SYSTEMS IN GRADUATE STUDENT LABORATORIES

Joseph E. O'Connor
Captain, United States Marine Corps
B.S., University of South Carolina, 2001

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March 2008

Author: Joseph E. O'Connor

Approved by: Alexander L. Julian
Thesis Advisor

Roberto Cristi
Second Reader

Jeffrey B. Knorr
Chairman, Department of Electrical and
Computer Engineering

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ABSTRACT

The Department of Electrical and Computer Engineering at the Naval Postgraduate School (NPS) continuously develops new design and education resources for students. One area of focus for students in the Power Electronics curriculum track is the development of a design center that explores Field Programmable Gate Array (FPGA) control of power electronics. Utilizing Mathworks® and XILINX® software to interface the FPGA with a voltage source converter (VSC), students gain experience with digital design, simulation, and hardware testing. This thesis focuses on the design, implementation and testing of a Student Design Center (SDC) employing an FPGA based digital controller. This thesis especially concentrates on the hardware interface between the FPGA and the power electronics and the development of laboratory procedures for students utilizing the design center.

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LIST OF SYMBOLS, ACRONYMS, AND ABBREVIATIONS

A	Amps
AC	Alternating Current
A/D	Analog to Digital Converter
BNC	Bayonet Nut Connector
BOM	Bill of Materials
CAD	Computer Aided Design
COTS	Commercial-Off-The-Shelf
dB	Decibel
DC	Direct Current
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FPD	Field Programmable Device
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
kHz	Kilohertz
LUT	Lookup Table
LPF	Lowpass Filter
NPS	Naval Postgraduate School
OPAMP	Operational Amplifier
PCB	Printed Circuit Board
RAM	Random Access Memory
SDC	Student Design Center
SOP	Standard Operating Procedure
SVM	Space Vector Modulation
V	Volts
VHDL	Very-High-Speed-Integrated-Circuit Hardware Description language
VSC	Voltage Source Converter

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EXECUTIVE SUMMARY

The Student Design Center (SDC) at the Naval Postgraduate School (NPS) Electrical Engineering Department (Solid State Microelectronics and Power Systems track) was created to expose students to the process of basic solid state power design and control, also known as "digital power". The SDC enables students to make accurate predictions of voltage source converter (VSC) behavior using software simulation; furthermore, the SDC allows students to test their simulations on the actual hardware to verify results.

The primary components of the SDC architecture are a Field Programmable Gate Array (FPGA), a VSC (augmented by other commercial, off-the-shelf components for various laboratories), a circuit board interface between the FPGA and the VSC, a circuit board interface between the FPGA and the power source, and a desktop computer. The design center is shown in Figure 1.

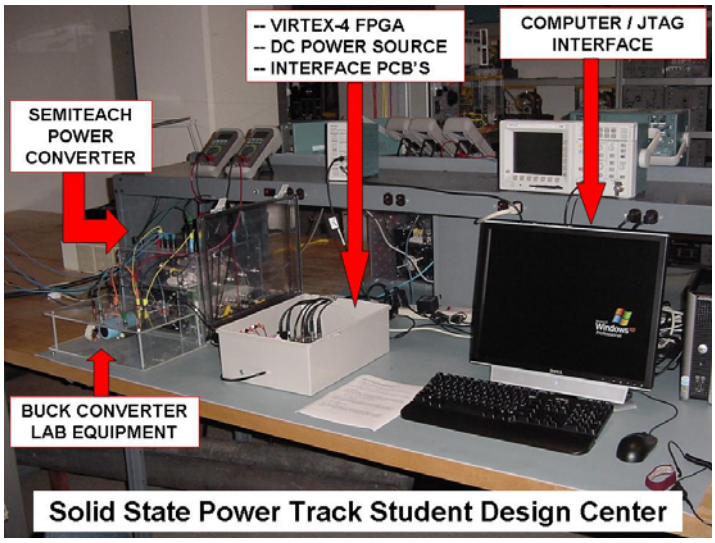

Figure 1. Student Design Center.

The SDC utilizes Mathworks' Simulink® software to generate hardware control simulations and run virtual experiments on VSCs and other power systems. XILINX® software produces Verilog Hardware Description Language (VHDL) code to interface the FPGA with hardware components; hence, basic knowledge of programming is required, but prior experience with VHDL coding is unnecessary.

The Semikron® VSC used in the SDC employs three parallel-connected half-bridges with an IGBT-diode brake for protection. Custom interface Printed Circuit Boards (PCBs) were designed, constructed, and tested to interface the FPGA with the VSC and the switching power source. The FPGA controls two analog-to-digital (A/D) converters for sampling VSC load currents and voltages. The FPGA was programmed with XILINX® software (embedded in the Simulink® model) and used to drive the VSC. The PCBs were thoroughly tested for compatibility and faults, and a digital low pass filter was designed and installed to reduce high frequency interference in the sampled signals. Four laboratory systems (buck converter, boost converter, H-bridge DC/AC converter and a diode-rectifier) were built to augment the VSC for various laboratories used in graduate power electronics courses.

The main thrust of this thesis was the exploration of the interface between the FPGA and the VSC and the actual construction and testing of the SDC. Emphasis was placed on the design, layout, and testing of each PCB as well as techniques used to minimize or eliminate adverse performance due to electromagnetic interference.

A secondary objective was to present the reader with a background and overview of the hardware and software used in the SDC including a brief description of current FPGA technology and its wide variety of applications in academic settings. A detailed derivation of Space Vector Modulation (SVM) was accomplished since it is the VSC control technique used in power electronics laboratories at NPS.

Finally, the last objective was to develop a Standard Operating Procedure (SOP) for laboratories conducted in the SDC in order to provide students with a better understanding of design flow prior to execution and to supplement laboratory assignments as a resource for frequently asked questions.

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I would like to express my sincere appreciation to the faculty and staff of the Naval Postgraduate School for their dedication to the ideals of higher education. You make it possible for professional military men and women to pursue their academic goals while supporting their family and this great country.

Thank you to Professor Julian for his genuine outlook on my educational experience and for his common-sense approach to life in general. Working side-by-side with him was an honor and privilege. I hope his attitude towards teaching and mentoring students is recognized by the department and used as a template for future hires.

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Finally, and most importantly, thank you to my wife, Kelly, and to my children. Without you I would not be the man and Marine I am today. You give my life meaning and purpose, and I hope I never let you down.

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I. INTRODUCTION

A. BACKGROUND

The Student Design Center (SDC) for the Naval Postgraduate School Electrical Engineering Department (Solid State Microelectronics and Power Systems track) was created for the purpose of exposing students to the process of transforming performance requirements into basic design. The center exposes students to basic power electronics design, enables accurate behavior predictions using software simulation, and allows students to test their simulations on the actual hardware to verify results. Students enrolled in power electronics courses complete assigned laboratories and become thoroughly indoctrinated in the design simulation and testing process. Each laboratory strives to give students practical problems in a real-world environment while preparing them for future study in product design and control [1].

The primary components of the SDC architecture are a Field Programmable Gate Array (FPGA); a voltage source converter (augmented by other commercial, off-the-shelf equipment for various laboratories); a Printed Circuit Board (PCB) interface between the FPGA and the VSC; a PCB interface between the FPGA and the power source; and a desktop computer. Students use Mathworks' Simulink® software to generate hardware control simulations and run virtual experiments on VSCs and other power systems. XILINX® software produces Verilog Hardware Description Language (VHDL) code to interface the FPGA with hardware

components; hence, basic knowledge of programming is required, but prior experience with VHDL coding is unnecessary.

B. RESEARCH OBJECTIVES

The main thrust of this thesis is the exploration of the interface between the FPGA with the VSC, and the FPGA with the switching power source. Emphasis is placed on the design, layout, and testing of each interface PCB as well as techniques used to minimize or eliminate adverse performance due electromagnetic interference.

A secondary objective is to present the reader with a background and overview of the hardware and software used in the SDC, present a brief overview of current FPGA technology and its wide variety of applications in academic settings, and develop the voltage conversion technique used in Power Electronics laboratories.

Finally, a Standard Operating Procedure (SOP) is developed to provide graduate students with a better understanding of design flow prior to executing experiments. The SOP is intended to supplement laboratory assignments as a resource for frequently asked questions.

C. APPROACH

The equipment used to build the SDC included a Semikron® VSC employing three parallel-connected half-bridges with an Insulated Gate Bipolar Transistor (IGBT) diode brake for protection; a MEMEC™ Virtex-4™ Development Board containing a XILINX® FPGA; and a stand-alone personal computer workstation incorporating a Pentium® processor. Custom interface PCBs were designed, constructed, and

tested to interface the FPGA with the VSC, and the FPGA with the switching power source. The analog signal interface PCB included an output control for the VSC and two analog-to-digital (A/D) converters for detecting load currents and voltages. The FPGA was programmed with XILINX® software (imbedded in the Simulink® model) and used to drive the VSC. The PCB was thoroughly tested for compatibility and faults [2]. A digital low pass filter was designed to reduce high frequency interference from the converted signals. Four laboratory systems (buck converter, boost converter, H-bridge DC/AC converter and a diode-rectifier) were built to augment the VSC for various laboratories used in graduate power electronics courses. Finally, the SDC SOP was developed and implemented.

D. RELATED WORK

The subject of FPGA based learning in graduate laboratories has received considerable attention in literature. Iowa State University, the University of Vigo (Spain) and the University of Alabama, among others, have instituted laboratories or capstone design courses combining hardware and software tools to facilitate FPGA learning for students with a basic knowledge of digital electronics and VHDL [[1], [3], [4]]. FPGA based learning is not just limited to digital power applications, but may include control theory application and robotics as well. For example, the University of Alabama's capstone design course focuses on the design, implementation and testing of an FPGA-based robotic vehicle capable of performing a number of competition specific tasks [3]. Many universities

around the world are recognizing the value, both monetary and educational, of incorporating FPGA based learning in their academic institutions.

E. THESIS ORGANIZATION

- Chapter I introduces research goals and presents the organization of the thesis.
- Chapter II presents the SDC's hardware and software, gives background information on VSC control principles, and covers the computer aided design (CAD) layout of the SDC.
- Chapter III explores the design, construction, and testing of the analog signal interface PCB and power interface PCB.
- Chapter IV addresses conclusions and future research opportunities.
- Appendix A provides information on the XILINX® Virtex-4™ Development Board.
- Appendix B contains PCB schematics and the Virtex-4™ Development Board's bill of materials (BOM).
- Appendix C provides information on the SEMITEACH® VSC.

F. CHAPTER SUMMARY

This chapter gave a brief introduction of SDC objectives, research goals, and the approach taken to meet those goals. It concluded with the organization of this thesis. Chapter II introduces the reader to the hardware

and software used in the SDC, presents a background in FPGA technology, and discusses the voltage conversion technique used in Power Electronics laboratories.

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II. STUDENT DESIGN CENTER OVERVIEW

A. FIELD PROGRAMMABLE GATE ARRAY

1. Overview

A Field Programmable Device (FPD) is a general term that refers to any type of integrated circuit used for implementing digital hardware, where the chip can be configured by the end user to realize different designs. Programming of such a device usually involves interfacing the device with specially designed programming software [5]. An FPGA is a semiconductor device containing programmable logic components and programmable interconnects. The programmable logic components can be programmed to duplicate the functionality of basic logic gates or more complex combination functions such as decoders and simple mathematical functions [6]. A major advantage of this technology is that FPGAs can execute codes in parallel whereas Digital Signal Processors (DSPs) execute codes in series. Hence, FPGA's do not have to "store" as much data as DSPs, and the need for large amounts of Random Access Memory (RAM) degrades significantly [7]. Another advantage of using FPGAs is their ability to work with whatever wordlength the programmer chooses. Whereas DSP processors must be selected to handle the longest wordlength that occurs in the code (thereby reducing efficiency when processing shorter wordlengths) FPGAs allow greater flexibility and efficiency by utilizing the smallest necessary wordlengths [8].

2. SDC FPGA

XILINX®, a leading manufacturer of FPGA's, primarily builds array-based circuits. These circuits incorporate chips comprised of two dimensional arrays of logic blocks that can be interconnected via horizontal and vertical routing channels [8]. An example of a generic, two-dimensional FPGA architecture is shown in Figure 2.

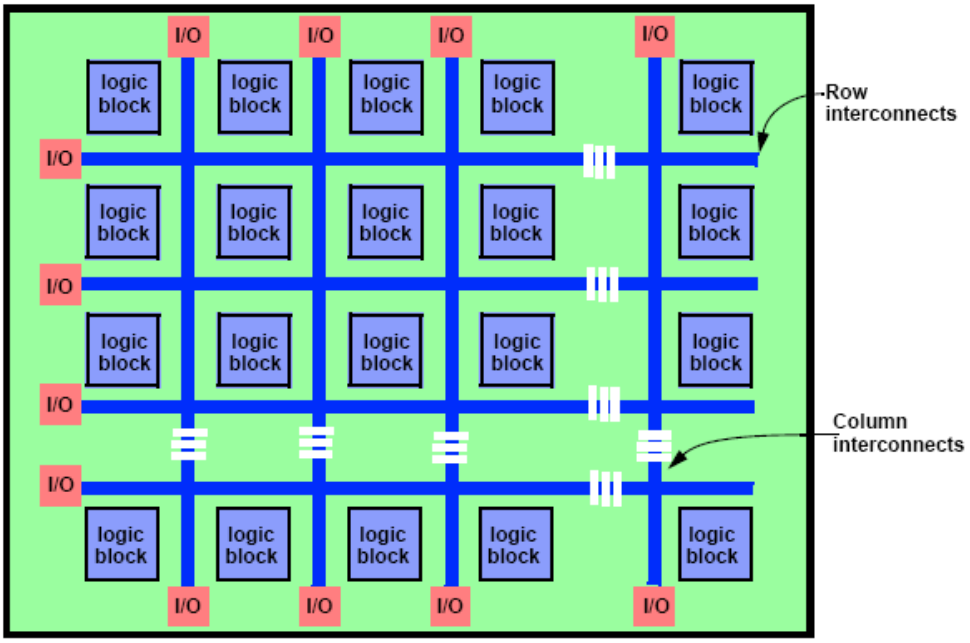

Figure 2. FPGA Architecture [From [8]].

The key difference between an FPGA and a "gate array" is that the former can be reprogrammed in the “field” since the logic program is changeable. Furthermore, whereas early gate arrays were composed of NAND gates, FPGA's are a carefully balanced selection of multi-input logic, flipflops, multiplexors and memory [8]. A typical layout for an FPGA is shown in Figure 3.

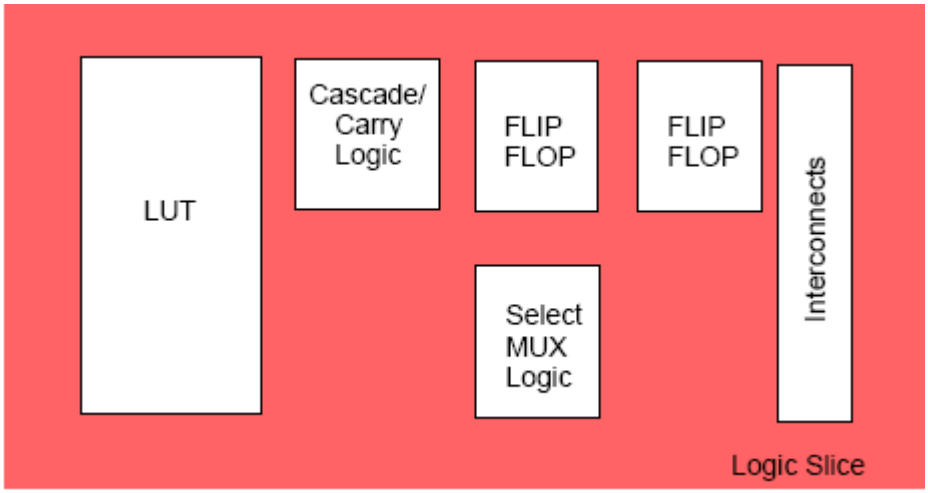

Figure 3. FPGA Logic Block [From [8]].

For the XILINX® FPGA used in this thesis, each logic block references Look-Up Tables (LUTs), which are small, one-bit wide memory arrays. The LUT input is composed of address lines while the output is a one-bit output of the memory. A LUT with "K" inputs corresponds to a "2K x 1" bit memory and can realize any logic function of its "K" inputs by programming the logic function's table directly into the memory [5]. FPGA's provide an excellent alternative for applications that require flexibility for various applications while avoiding the extra cost of multiple, hard-wired circuit boards. The SDC demands such flexibility since various design criteria are presented to students and the need to reprogram the board is essential.

For this thesis, a XILINX® Virtex-4™ Development Board incorporating a XC4VLX25-10SF363 FPGA was utilized and is shown in Figure 4.

Figure 4. XILINX® Virtex-4™ Development Board [From [9]].

The Virtex-4™ was designed as a user friendly platform for prototyping and verifying designs. This concept is a central requirement for the SDC. A high-level block diagram of the Virtex-4™ Development Board is shown in Figure 5. A complete description of each board subsection is provided in a condensed form of the Virtex-4™ user's guide found in Appendix B.

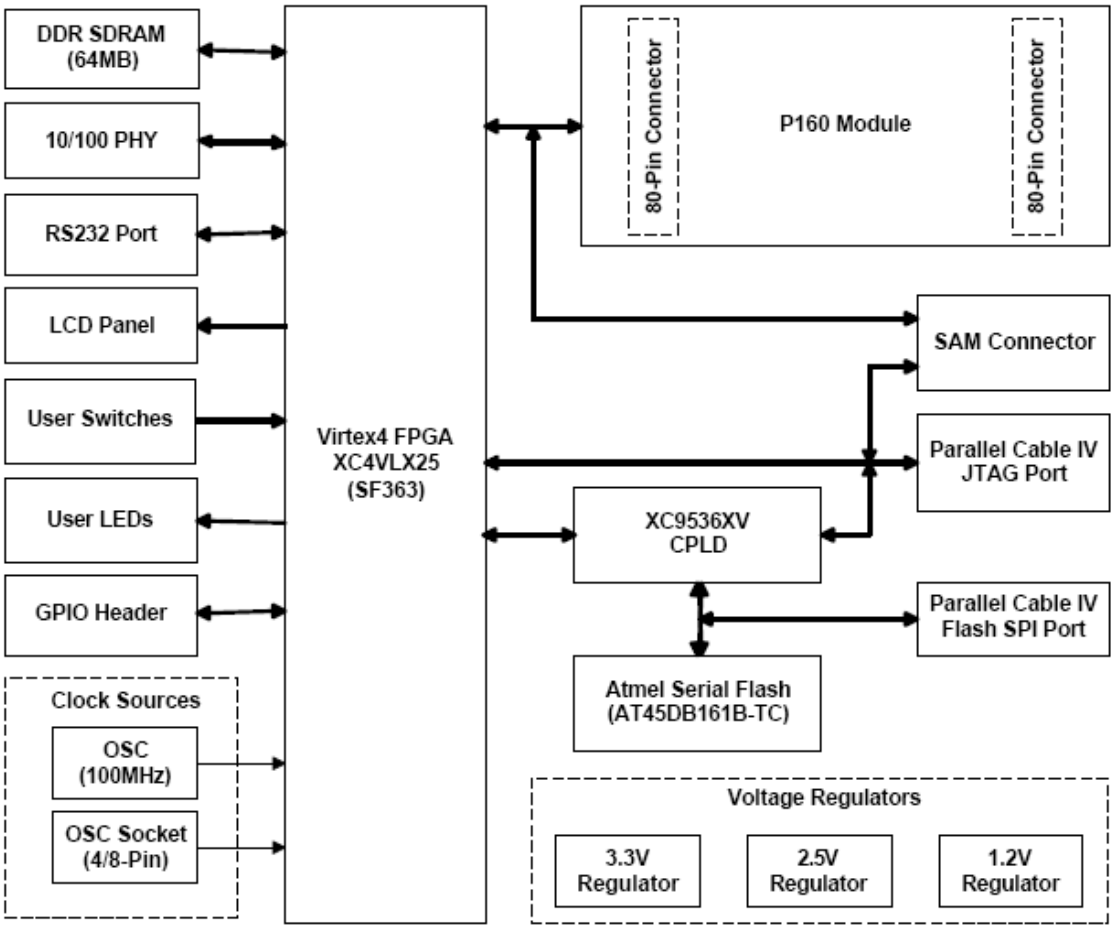

Figure 5. Virtex-4™ Development Board Block Diagram [From [9]].

The Virtex-4™ Development Board provides 64MB of DDR SDRAM memory (32Mx16). The clock generation section of the board provides all necessary clocks for the I/O devices located on the board as well as the random access memory. An on-board 500MHz oscillator provides the system clock input to the XILINX® XC4VLX25-10SF363 FPGA; however, the SDC uses only a fraction of this clock speed. In addition to the clock input, a socket is provided on the board that can be used to provide a single-ended clock input to the FPGA via an 8- or 4-pin oscillator. The board provides a

10/100 Ethernet port for network connection and an 8-bit interface to a 2x16 LCD panel. The board also provides four user push button switches allowing an active low signal to be generated when a given switch is pressed. These switches can be remotely toggled using ChipScope™ Pro software (addressed later in this chapter). A JTAG connector is used as a port to load the software from a desktop computer, and the 5.0V connector pin is used to supply the main power to the card. The board has two interface connectors that provide easy access to the PCB interface [9]. An overview of the Virtex-4™ Development Board's layout is shown in Figure 6.

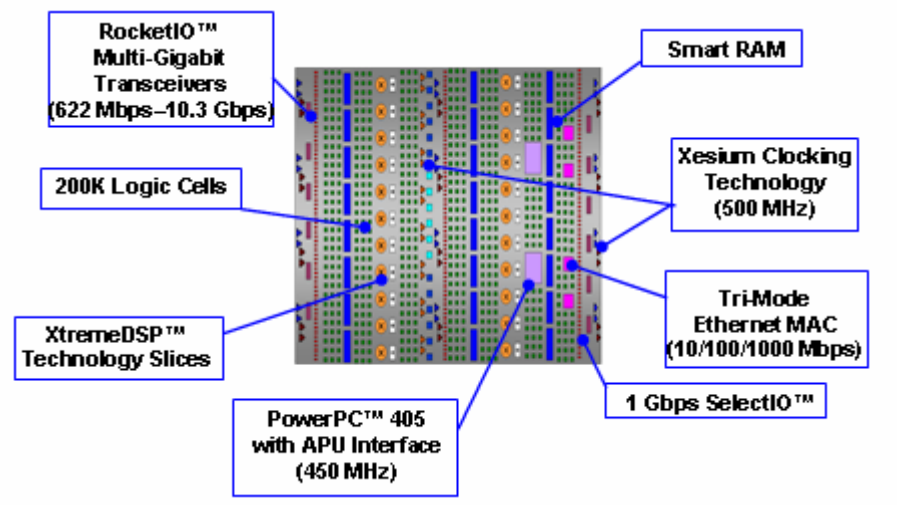

Figure 6. Virtex-4™ Development Board Layout [From [10]].

B. VOLTAGE SOURCE CONVERTER AND SPACE VECTOR MODULATION

The VSC used in the SDC is a three-phase, rectifier/converter specially equipped to allow students visualization of every part. The VSC is contained inside an external interface for safety and is produced by

Semikron® as an educational demonstrator. A photo of the converter is shown in Figure 7. The converter's data sheet is listed in Appendix C [11].

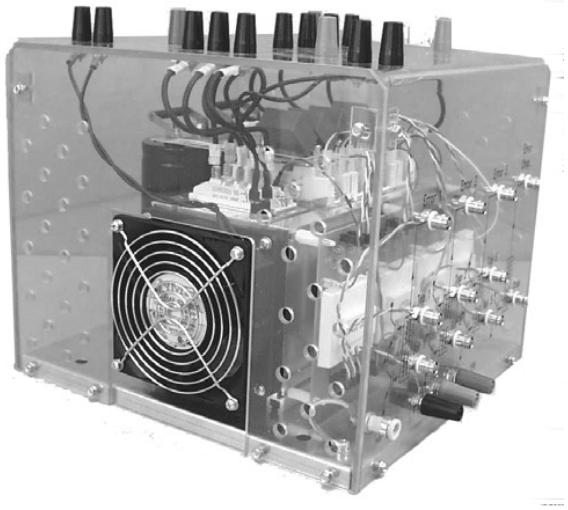

Figure 7. SEMITEACH® Voltage Source Converter [From [11]].

The basic schematic of the VSC is shown in Figure 8.

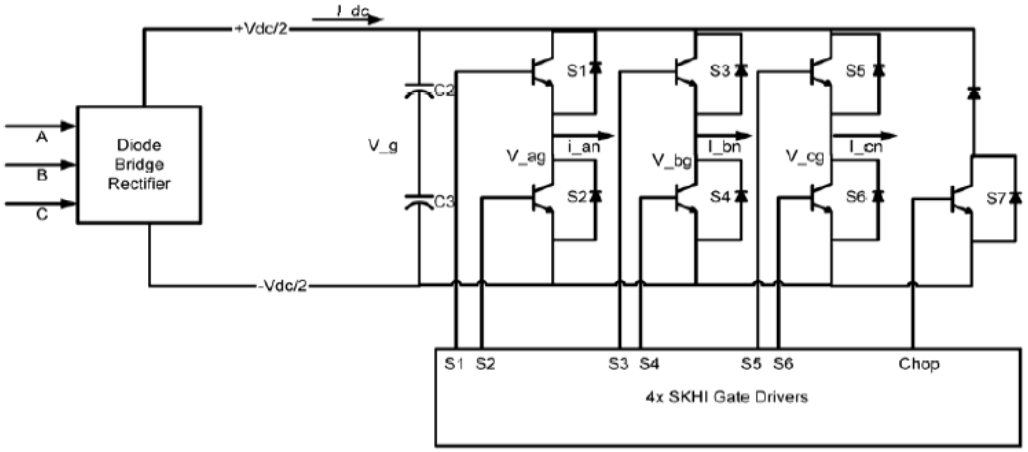

Figure 8. SEMITEACH® VSC Schematic [From [11]].

Controlled three phase (or single phase) output of the VSC can be obtained by a number of methods, but this thesis

adopted the Space Vector Modulation (SVM) model approach since it was utilized in existing laboratories [[12] and [13]]. SVM utilizes voltage commands assigned as "**q**" and "**d**" variables from the "**qd**" reference frame. The reference frame contained in the SVM hexagon is show in Figure 9.

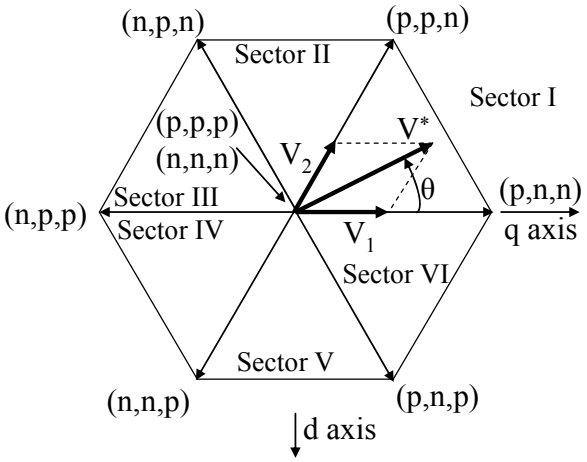

Figure 9. Space Vector Modulation Hexagon [From [12]].

The derivation and transformation below is an excerpt taken from [12] with variables adopted from the simple converter schematic shown in Figure 10.

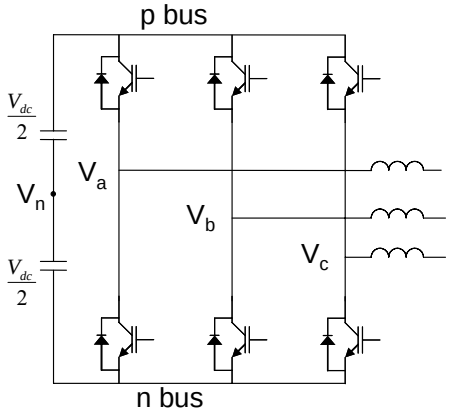

Figure 10. Simple Converter Schematic [From [12]].

The modulation indexes are described as **q**-axis and **d**-axis voltages in the stationary reference frame. The SVM hexagon maps the **qd** voltages for each of the eight possible switching states (zero axis in the 3rd dimension mapped to the center of the hexagon). Transformation into the **qd0** frame is defined by [12]:

$$K_s = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-1}{2} & \frac{-1}{2} \end{bmatrix} \qquad 2.1$$

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = K_s \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \qquad 2.2$$

where V_{an}, V_{bn}, and V_{cn} are the line-to-neutral voltages for the three phase system shown in Figure 10. For the case where Va is connected to the **p** bus and Vb and Vc are connected to the **n** bus (p, n, n), the **qd0** voltages are [12]:

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = \frac{v_{dc}}{2} K_s \begin{bmatrix} 1 \\ -1 \\ 1 \end{bmatrix} = \begin{bmatrix} \frac{2v_{dc}}{3} \\ 0 \\ \frac{-v_{dc}}{6} \end{bmatrix} \qquad 2.3$$

Equation 2.3 also defines the length of the radii forming the corners of the hexagon, 2/3 Vdc. In the case

where Va and Vb are connected to the **p** bus and Vc is connected to the **n** bus (p,p,n), the **qd0** voltages are [12]:

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = \frac{v_{dc}}{2} K_s \begin{bmatrix} 1 \\ 1 \\ -1 \end{bmatrix} = \begin{bmatrix} \frac{v_{dc}}{3} \\ \frac{-v_{dc}}{\sqrt{3}} \\ \frac{v_{dc}}{6} \end{bmatrix} \qquad 2.4$$

The two states defined by Equations 2.3 and 2.4 forms the sides of Sector I. When the reference voltage is in this sector, these two states and the zero states are used to produce an output voltage that, on average, equals the reference voltage.

Now let T_s be the total switching period, and let T_1 and T_2 represent the amount of time spent on states (p, n, n) and (p, p, n) respectively. The vectors V_1 and V_2 are proportional to the time spent on each state [12]:

$$v_1 = \frac{T_1}{T_s} \frac{2v_{dc}}{3} \qquad 2.5$$

$$v_2 = \frac{T_2}{T_s} \frac{2v_{dc}}{3} \qquad 2.6$$

The law-of-sines can be used to find the duty cycles for each state [12]:

$$\frac{2v^*}{\sqrt{3}} = \frac{v_1}{\sin(60^o - \theta)} = \frac{v_2}{\sin(\theta)} \qquad 2.7$$

Substituting Equations 2.5 and 2.6 into Equation 2.7 yields solutions for the time spent on each state [12]:

$$T_1 = \frac{v^* \sqrt{3}}{v_{dc}} T_s \sin(60^o - \theta) \qquad 2.8$$

$$T_2 = \frac{v^* \sqrt{3}}{v_{dc}} T_s \sin(\theta) \qquad 2.9$$

The time spent on each state cannot exceed the total switching period so the modulation index (mi) is between zero and one [12]:

$$mi = \frac{v^* \sqrt{3}}{v_{dc}}, 0 < mi < 1, 0 < v^* < \frac{v_{dc}}{\sqrt{3}} \qquad 2.10$$

Finally, the amount of time spent in the zero state is the time remaining in the period [12]:

$$T_0 = T_s - T_1 - T_2 \qquad 2.11$$

When choosing a switching method for SVM, consideration should be given to minimizing switching events and minimizing distortion. Switching patterns for each sector are shown in Figure 11. Switching states are shown on the right, and time duration is on the left.

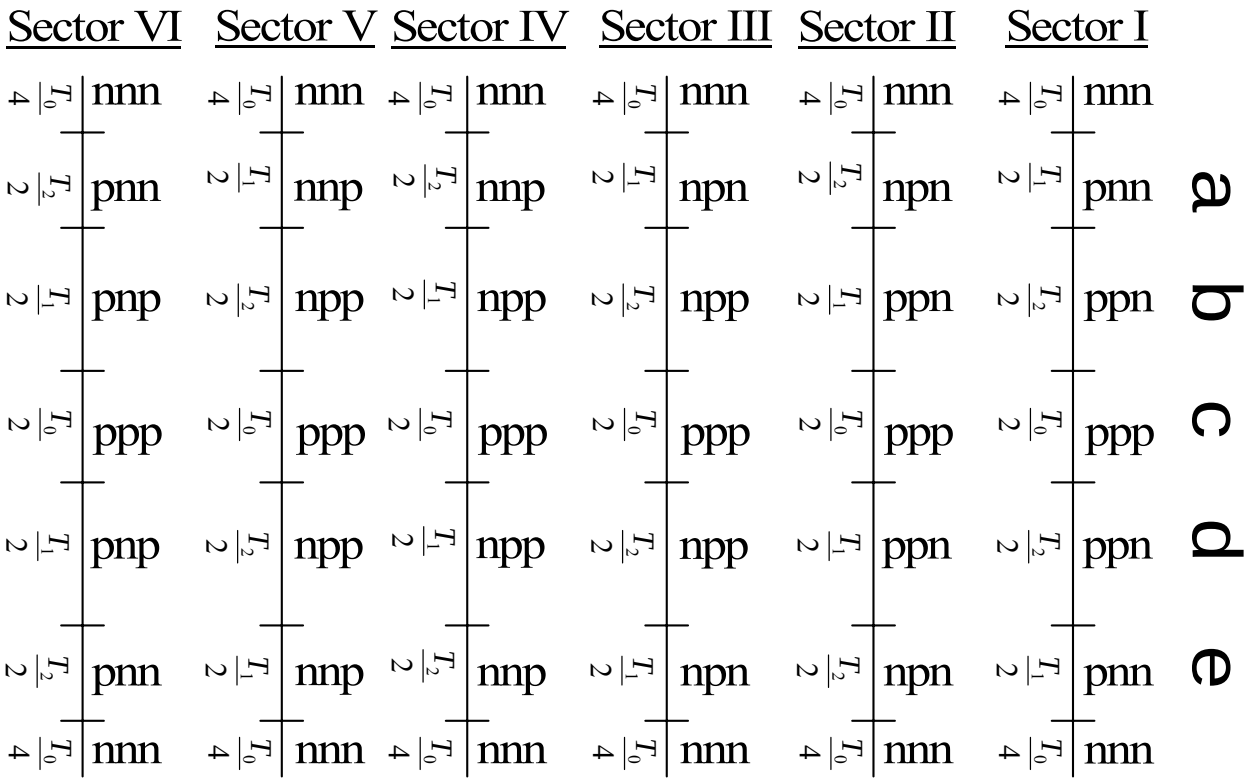

Figure 11. Switching Pattern for Each Sector [From [12]].

C. HARDWARE AND SOFTWARE

The SDC utilizes Simulink® for modeling power electronics systems and for running simulations to test designs. Simulink® enables multi-domain simulation and model-based design for dynamic systems and provides an interactive graphical environment as well as a customizable set of block libraries. Most importantly, Simulink® enables model analysis and diagnostics tools to ensure model consistency and identify modeling errors prior to hardware setup and testing [14].

XILINX® software produces VHDL code from the Simulink® model in order to program the FPGA. VHDL is the most commonly used design-entry language for field-programmable gate arrays and learning the code is not a trivial task; however, XILINX® enables the student to compile VHDL code without becoming proficient in VHDL programming. The block diagram for loading VHDL from the computer to the FPGA is shown in Figure 12.

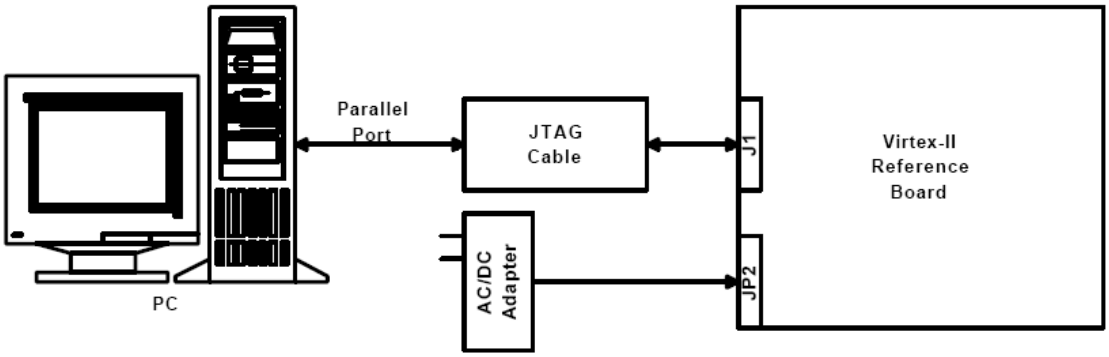

Figure 12. Software Interface Block Diagram [From [9]].

Once the VHDL code is obtained, it is converted to a netlist and verified again using XILINX® *Project Navigator*.

Project Navigator allows the netlist to be compiled into a form that can be directly loaded into the FPGA. It also reports on the percentage of the FPGA usage. After verification, the netlist can be fitted to the FPGA by XILINX® *Impact* using a process called place-and-route. The graphical interface is very easy to use by right-clicking on the icon and selecting the appropriate file to load [9].

D. SDC COMPUTER AIDED DESIGN ARCHITECTURE

A block diagram of the SDC hardware configuration including Computer Aided Design (CAD) tools, including the Semikron® power module, passive components, and measuring instruments, are shown in Figure 13.

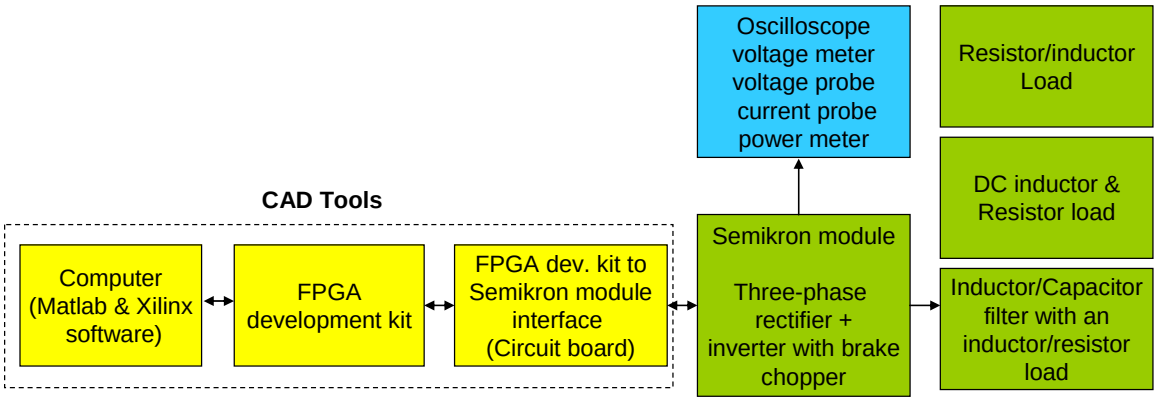

Figure 13. SDC Hardware Configuration [From [15]].

The design process is summarized as follows: A Simulink® is developed to simulate a power system. Elements of the model internal to the FPGA are designed using the *System Generator* library. The rest of the system is designed using Simulink® library blocks. Once the system is modeled, VHDL code is generated for the portion of the simulation controlled by the FPGA. After the VHDL is generated, the project is loaded into *ISE Foundation*

software and the design is synthesized. Then the program is uploaded into the FPGA through the JTAG cable, and ChipScope™ Pro is used to communicate with the target hardware. Finally, data is downloaded from the FPGA and imported into Matlab for measurement and plotting. The CAD architecture is shown in Figure 14.

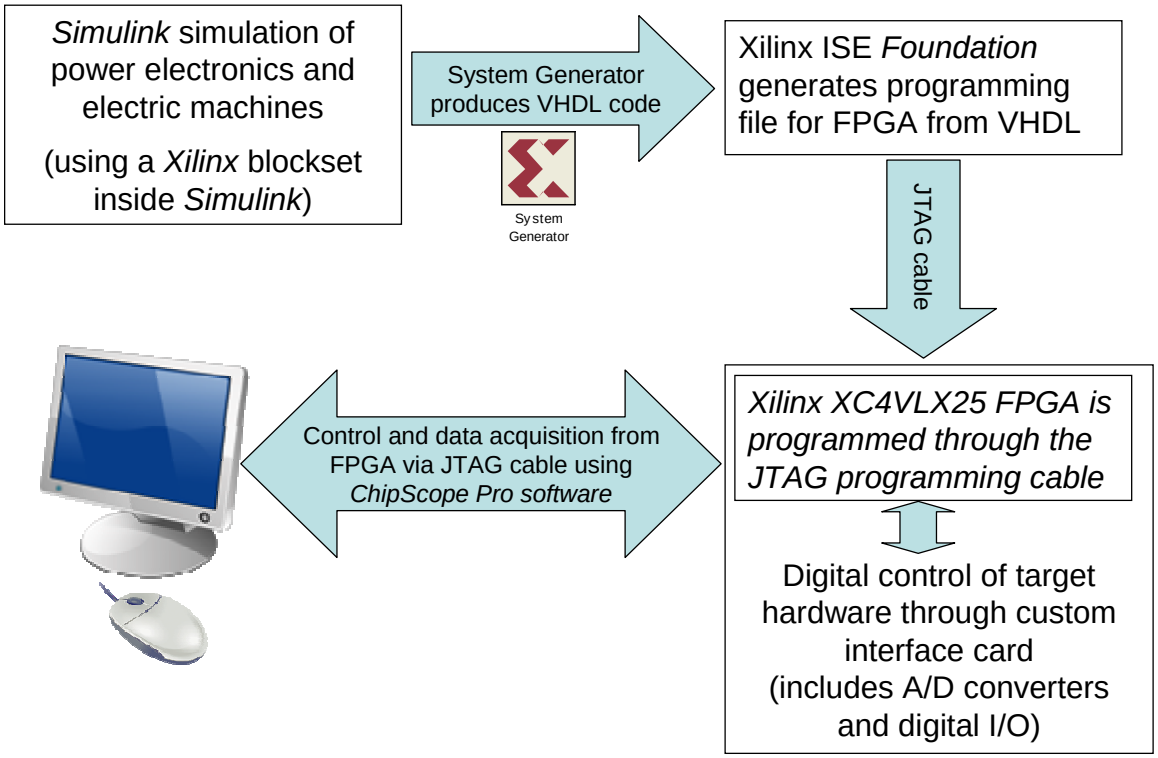

Figure 14. Computer Aided Design Architecture [From [15]].

The XILINX® library blocks inside the Simulink® library browser behave like other library blocks during simulation. A screen snapshot of the Simulink® library browser with the XILINX® blocks highlighted is shown in Figure 15.

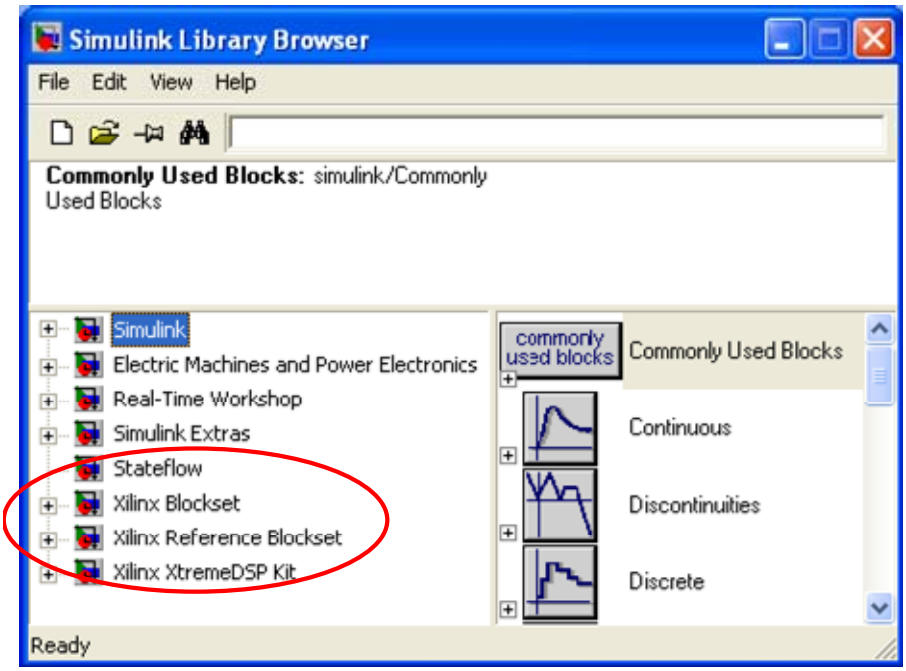

Figure 15. XILINX® Blocks for Simulink® Library Browser.

Every simulation that has *System Generator* library blocks inside must have the System Generator block at the top level. Note the *System Generator* block in the Buck-Converter Laboratory model shown in Figure 16.

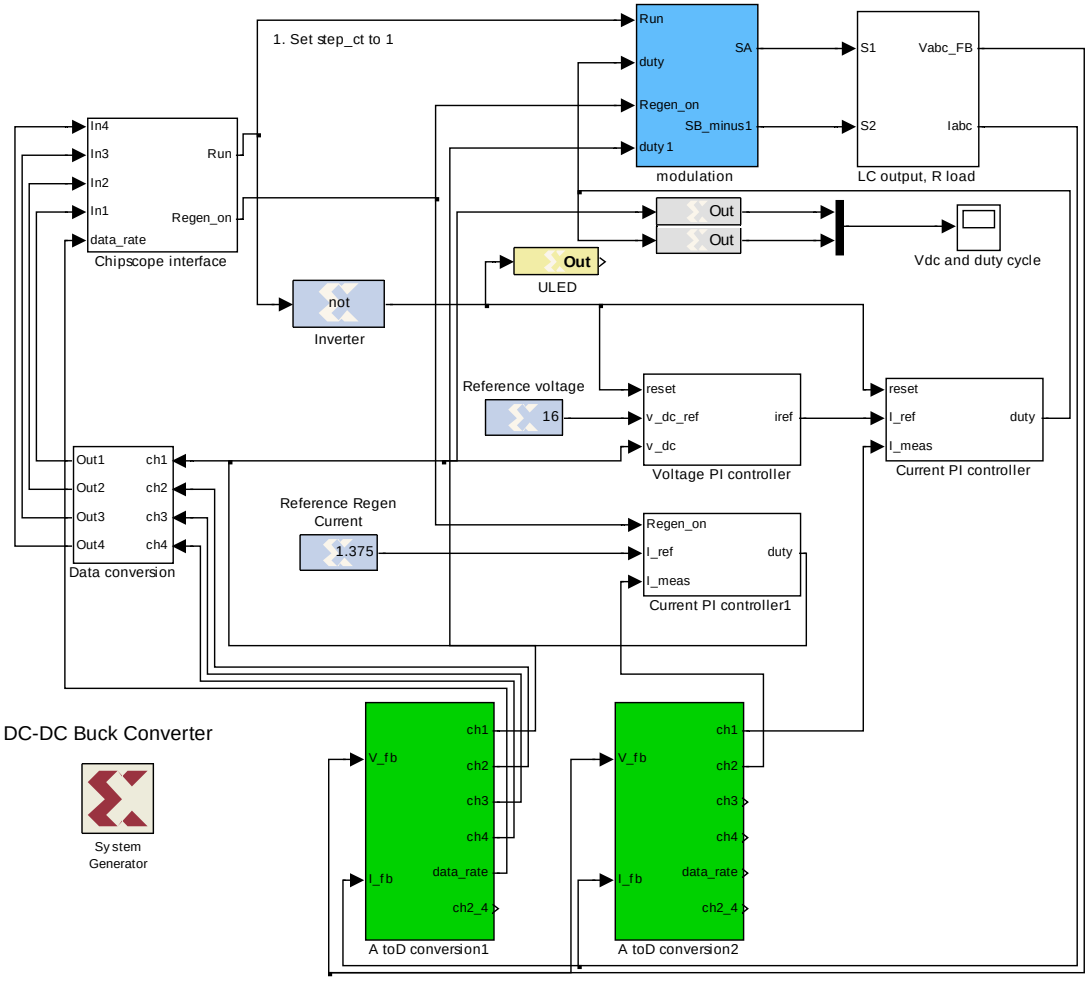

Figure 16. DC-DC Buck Converter Simulink® Model [After [16]].

After the VHDL code is compiled, *ISE Foundation* generates project files containing the VHDL code. Menu choices are shown in Figure 17.

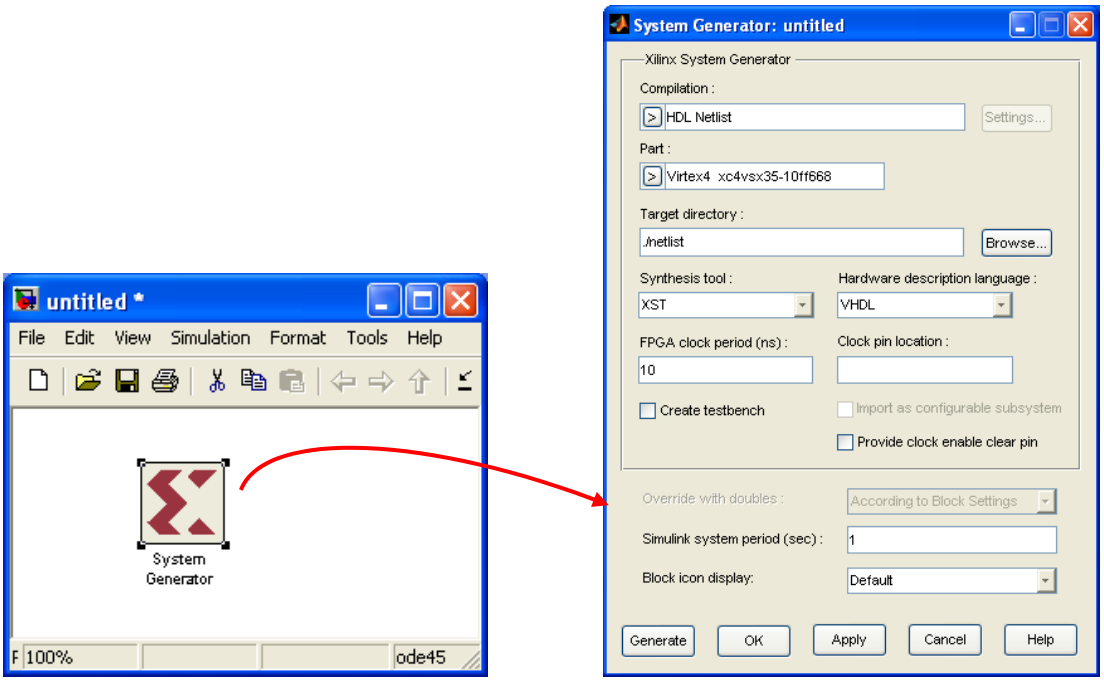

Figure 17. *System Generator* Block and Menu.

1. VHDL Synthesis Using *ISE Foundation*

The design is synthesized using *ISE Foundation* software by opening the project file, generating the program file, and configuring the device in *Impact*. Once synthesized, the programming file is generated and the FPGA is programmed. The ISE Foundation window is shown in Figure 18.

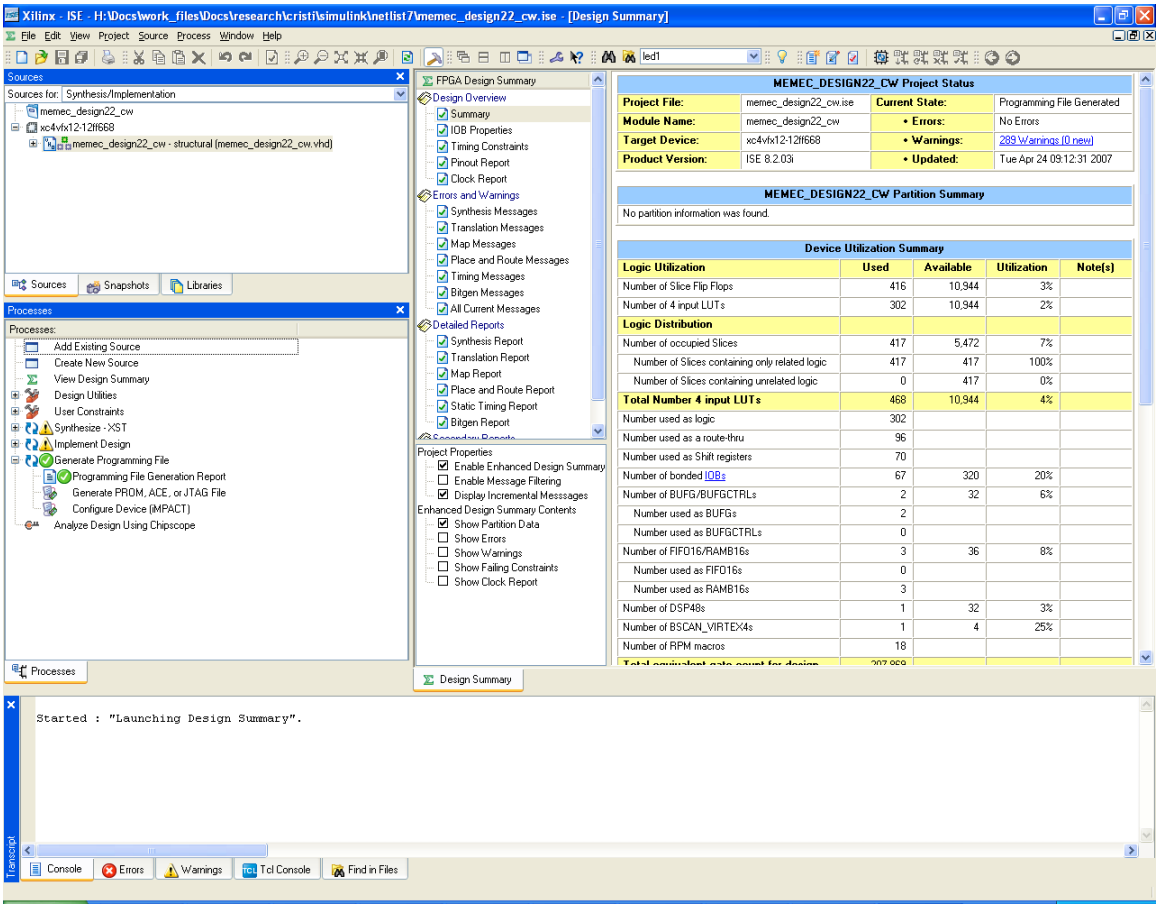

Figure 18. XILINX® ISE Window.

2. Hardware Interface Using ChipScope™ Pro

The user can remotely control the converter through the computer using ChipScope™ Pro software. ChipScope™ Pro inserts a logic analyzer, bus analyzer, and virtual I/O low-profile software core directly into the design. This allows the user to view any internal signal or node, including embedded hard or soft processors. Signals are captured at or near operating system speed and the process is limited only by the speed of the A/D converter. The data is then viewed through the programming interface and analyzed with the ChipScope™ Pro Logic Analyzer [8].

ChipScope™ Pro is opened from the ISE Foundation window. The control screen is shown in Figure 19.

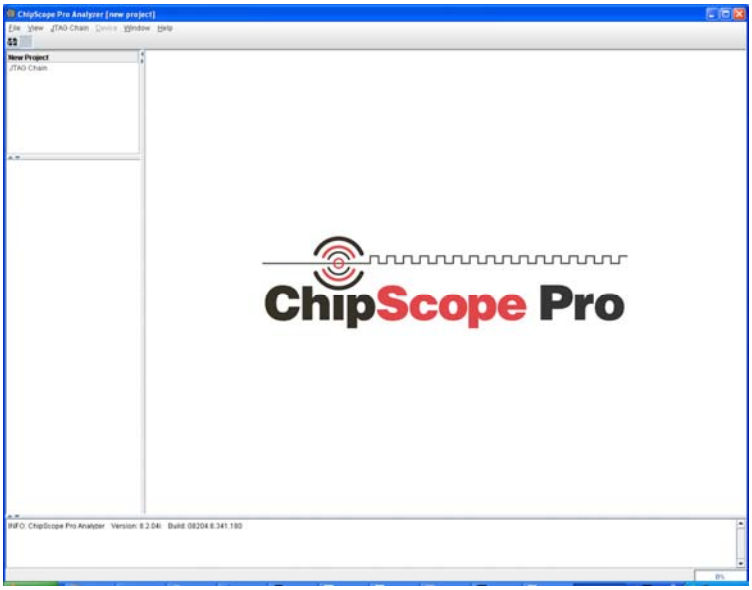

Figure 19. ChipScope™ Pro Window.

In order to establish communication with the hardware the user must establish communication through the JTAG Chain with the FPGA and configure the device with a ChipScope™ program. The "configure" screenshot is shown in Figure 20.

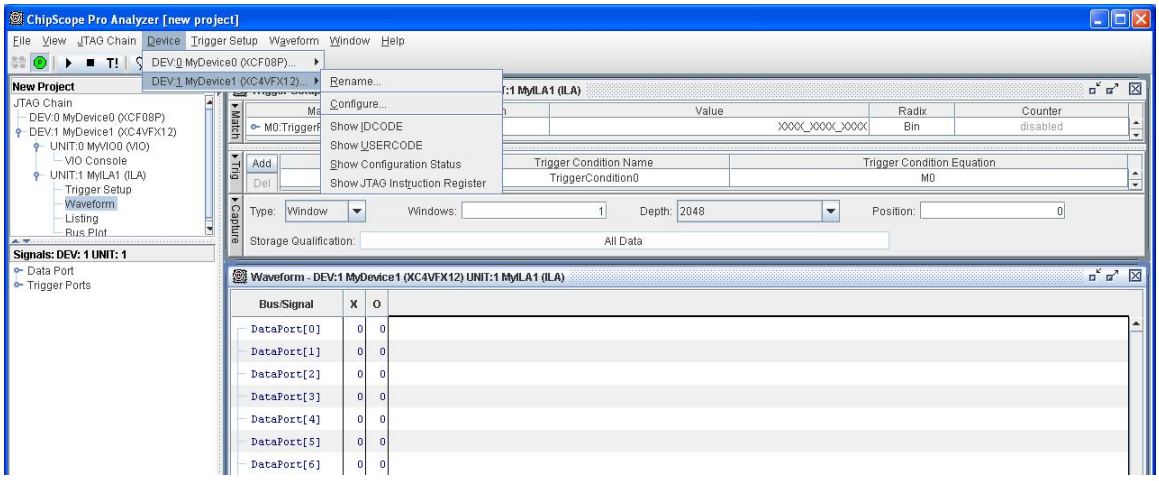

Figure 20. The “Configure” Command under the “Device” Menu.

The VIO Console allows the user to control the hardware. For example, one bit can be toggled to turn the converter on and off. The VIO Console is shown in Figure 21.

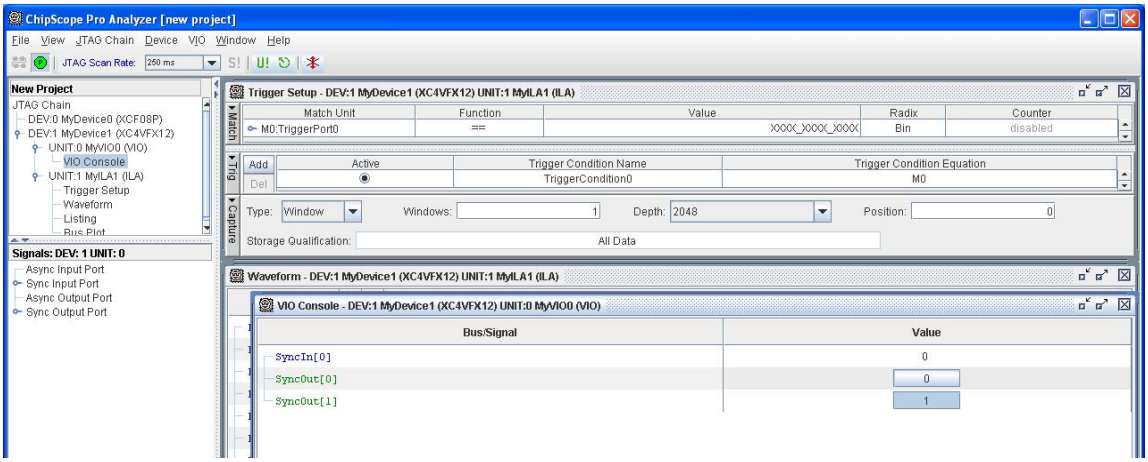

Figure 21. VIO Console in ChipScope™ Pro.

Now the user can remotely control the FPGA, and thus the VSC digital control process, using ChipScope™ Pro; hence, detailed analysis of input and output signals can be accomplished digitally without instruments. The user can evaluate a signal bit-by-bit if necessary, and calibration of the sampled signal can be acommplished by simply adjusting gain blocks in the Simulink® model. For this power conversion laboratories, digital calibration is an essential feature given that laboratory instruments are often out of calibration. An example of digital calibration will be expounded on in the next chapter.

E. CHAPTER SUMMARY

An overview of the hardware and software utilized in the SDC was presented with a brief background of VSC digital control. A thorough development of the SDC's CAD

process was offered as well. The next chapter covers the design, construction, and testing of the analog signal interface PCB and the power source interface PCB.

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III. PRINTED CIRCUIT BOARD DESIGN AND TESTING

A. SCHEMATIC LAYOUT AND PCB DESIGN

The main objective of this phase was to interface with the Virtex-4™ Development Board and provide power to the boards while maintaining signal clarity in the sampled signals. PCB123 software was used to prepare the board schematics for manufacture. A primary objective for the design was the elimination of circuit interference, and a thorough implementation of noise reduction techniques was necessary to attain that objective. Signal decoupling, shielding of tracks and proper ground plane layout were critical to the success of the design. A summary of steps taken to attain these goals is outlined below:

- A common-mode choke was used on the ribbon cable connecting the analog and power PCBs.
- Snap grid and default track/pad sizes were chosen to minimize signal loss and properly space key components.
- Critical tracks were identified early so that traces would not be routed too close to the digital clock and other "noisy" components.
- All traces were kept as short as possible to minimize signal loss and coupling.
- Active components drawing significant switching current were “bypassed” using capacitors across power rails. Capacitors were placed as close to

the desired component as possible. 22uF and 0.1uF capacitors were used (depending on the voltage) throughout the PCBs.

- A design rule check on the completed PCBs ensured manufacturability, circuit connectivity, and electrical clearance.

The analog signal interface PCB is shown in Figure 22. The power source interface PCB is shown Figure 23. Each board's schematic is contained in Appendix A.

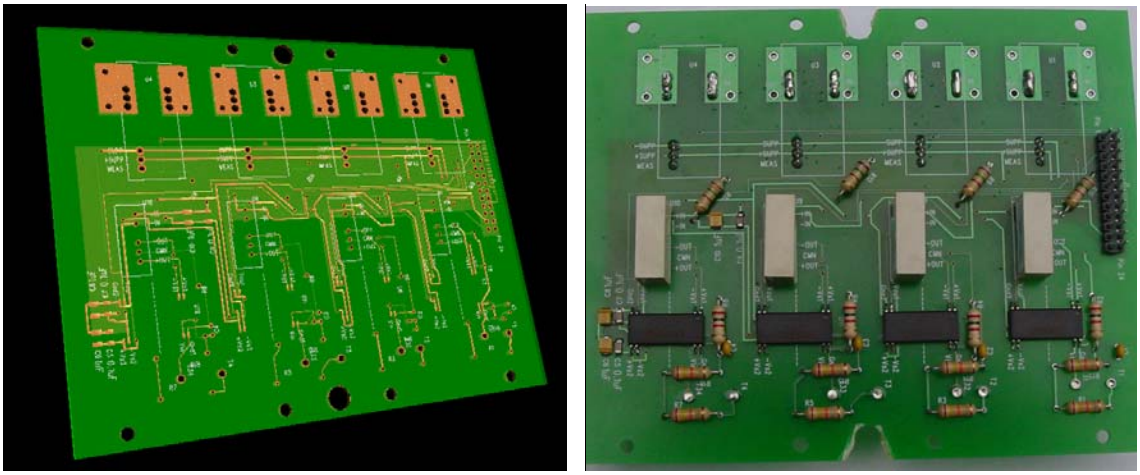

Figure 22. Analog Signal Interface PCB.

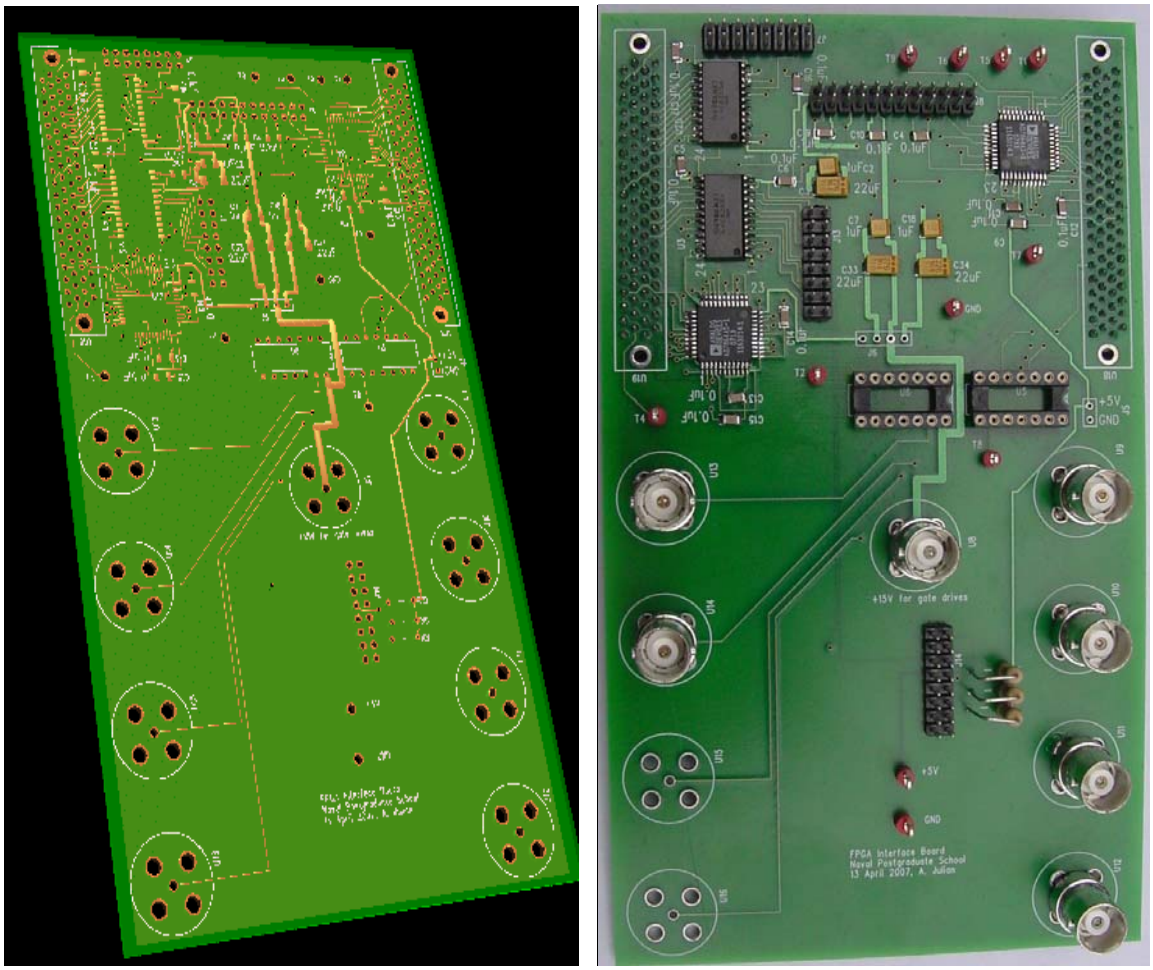

Figure 23. PCB123® 3-D View and Photo of Power Source Interface PCB.

Individual components were manually placed on the board, and a system check revealed a manufacture defect (short) between the +/- 15V tracks and a missing track to the fourth sampling channel operational amplifier (OPAMP). The short and track were manually repaired. A follow-up test revealed electrical continuity and proper grounding throughout the circuits. The system was powered up and tested using the computer interface.

B. MAJOR COMPONENT PACKAGING

Student safety was the top priority during the component packaging phase. All equipment was physically insulated from students while still allowing a clear view of each component for visual inspection. The final component placement is shown in Figure 24. (Note that the clear-plastic shield is tilted up for the photograph.) The final layout for the SDC is shown in Figure 25. Grounding mats were installed to prevent electrostatic discharge to sensitive hardware, and students are required to use the grounding tether when inspecting components.

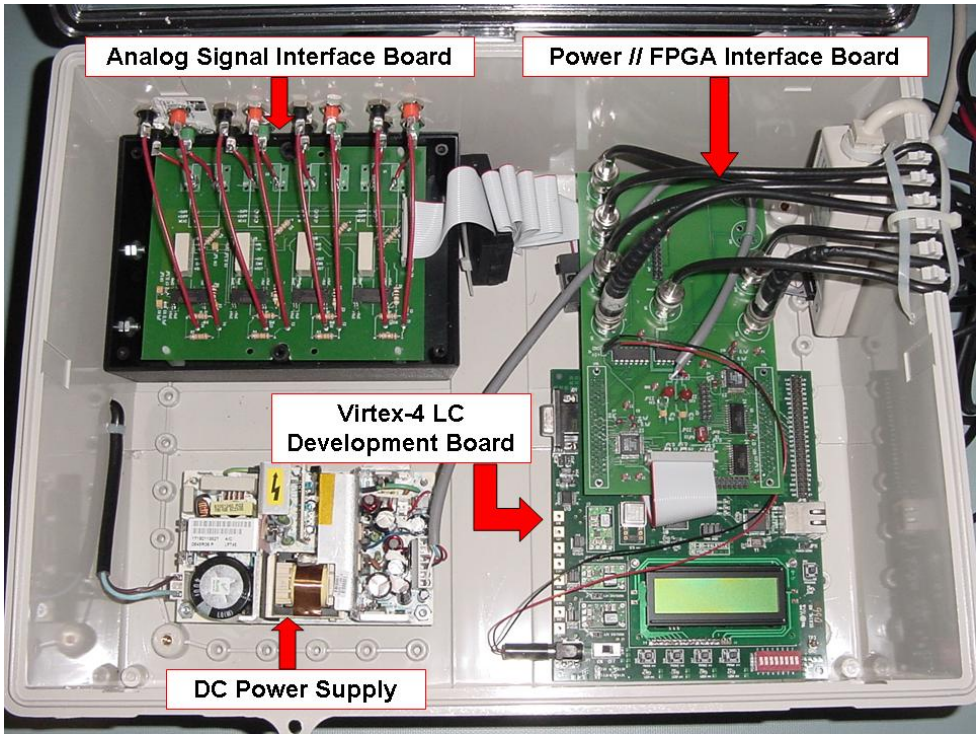

Figure 24. Student Design Center System Interface.

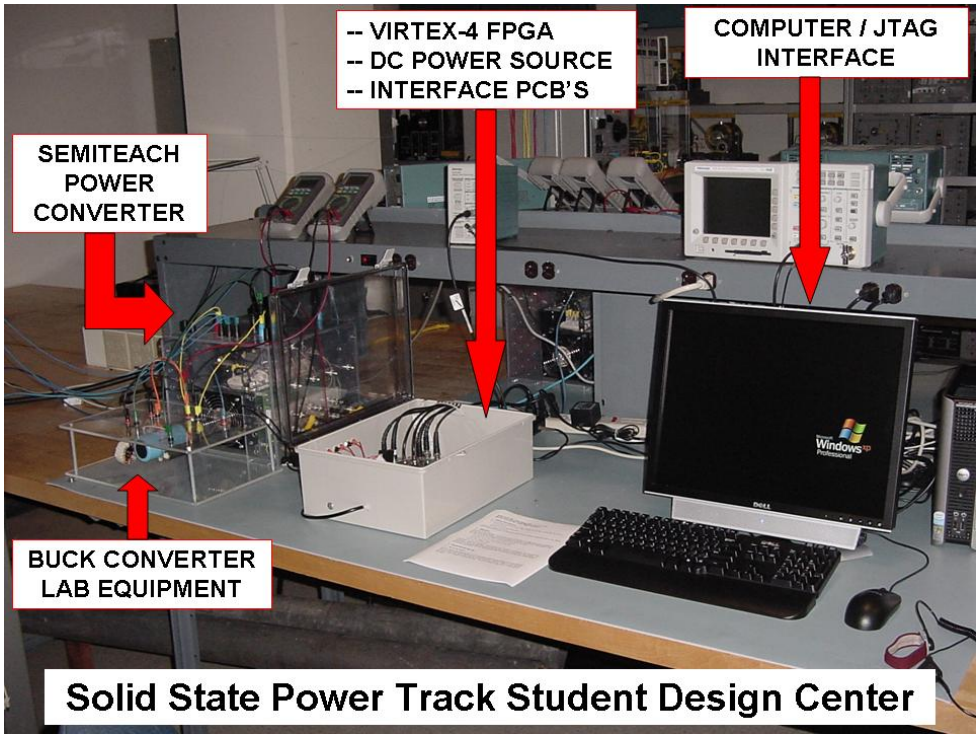

Figure 25. Student Design Center.

C. ANALOG-DIGITAL CONVERSION OF FEEDBACK SIGNALS

The analog signal interface PCB contains four channels to sample circuit voltages and four channels to sample circuit currents. An AD-7864 analog-to-digital (A/D) converter operating at a 500 kHz sampling rate was dedicated to each set of channels. Sample-and-hold for each channel was conducted in series for a total sampling rate of 133kHz for each channel. This sampling rate was more than sufficient to prevent aliasing when sampling low frequency measurements typical for power electronics laboratories. A diagram illustrating the conversion time for each channel and the overall timing sequence is shown in Figure 26.

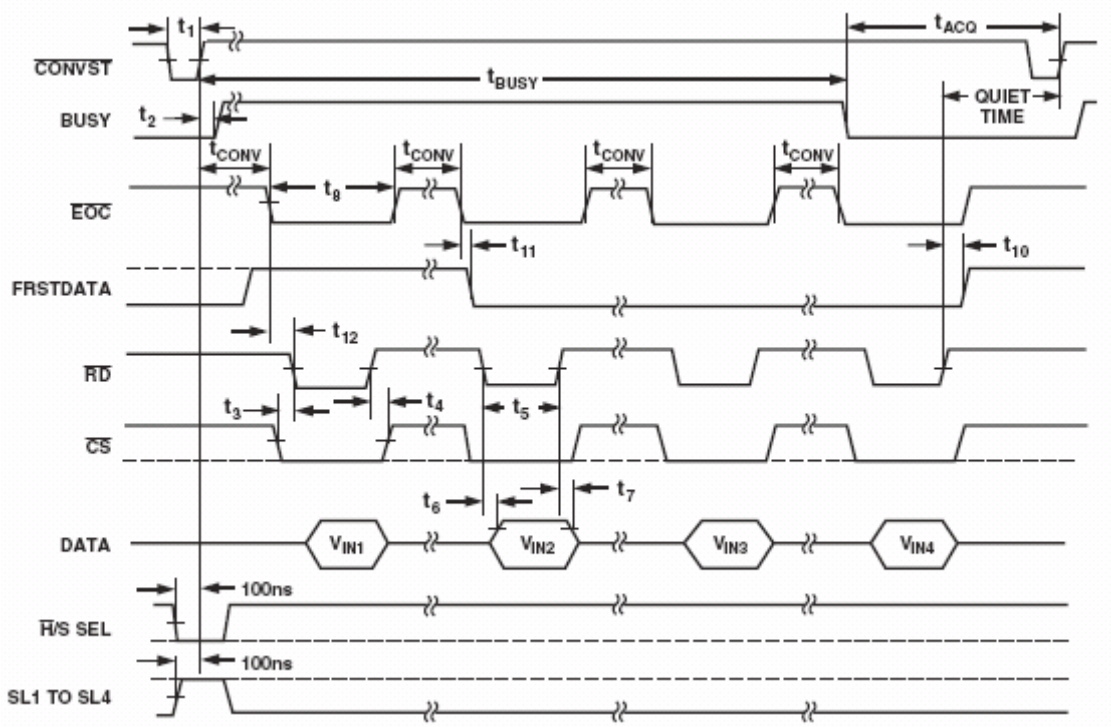

Figure 26. Four Channel AD-7864 Timing Diagram [From [17]].

The measurements taken by the AD-7864s are displayed in ChipScope™ Pro (or a standard oscilloscope) to enable the detailed analysis of the signals. Sampled signals can be calibrated precisely by adjusting the gain of the feedback signals in the Simulink® model, thus enabling accurate representation of physical samples. An example of gain adjustment in Simulink® to enable digital calibration is shown in Figure 27.

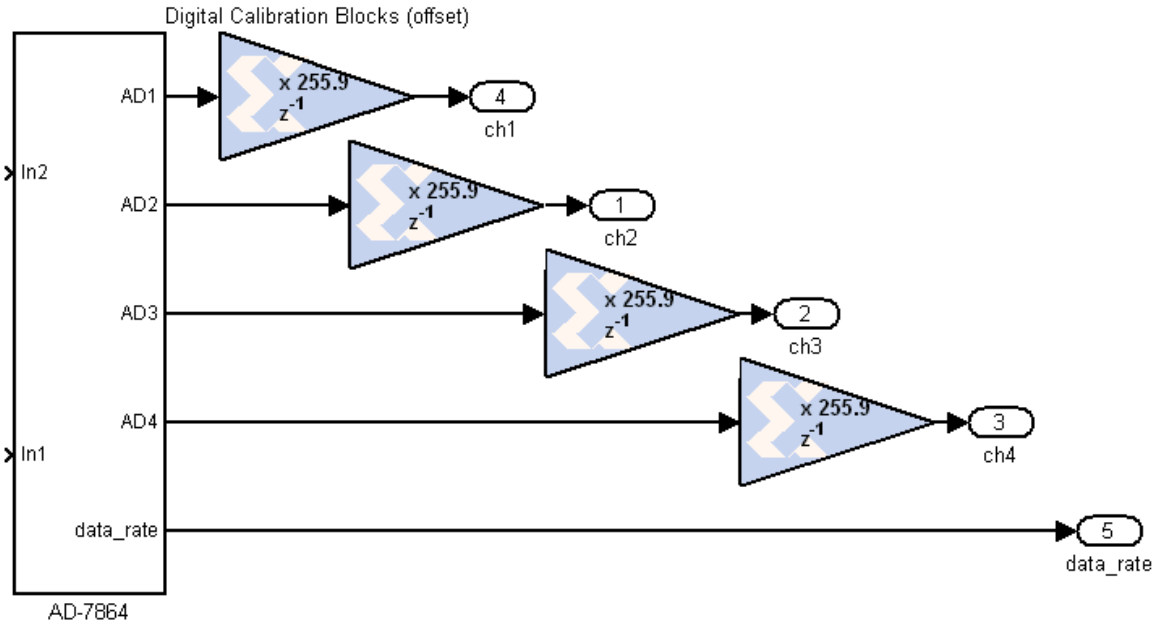

Figure 27. Simulink® Digital Calibration of Signals [After [16]].

1. Power Requirements

The Virtex-4™ board uses 1.2V, 2.5V, 3.3V and 5V power buses, but operates from a single 5V power supply and steps the voltage down internally. The analog signal interface PCB uses a 5V and +/- 15V bus. A compact, off-the-shelf AC/DC "switching" power source was chosen for the system so that a bulkier, linear DC power source would not be required in the SDC. It was also convenient to use a DC source that would fit inside the component box to maximize laboratory safety and usable space. The main shortcoming of the switching power supply was electromagnetic emission. A switching power supply for programmable circuits creates the potential for EMI and system re-boot. The high-frequency switching within an electronic power supply can also interfere with AD sampling and system clock operation. Switching power supplies generate more EMI because they

switch large currents at very high frequencies, anywhere from 50 KHz to 1 MHz. At these high frequencies, optimal power efficiencies and smaller components can be used in the construction of the system which is why they are much smaller than linear power sources. Because of its efficiency and size, a switching power supply was the first choice for the SDC [[18] and [19]].

To be certain that the power source did not interfere with the circuit, a test of each of the eight channels was conducted utilizing a linear power source (Tektronics PS280 DC power source) and a switching source to determine the difference in noise levels. An analysis of signal output showed no significant variation in signal noise due to the switching source.

2. Conditioning of Sampled Signals

Although careful consideration was given to implementing noise reduction techniques during PCB design and construction and extensive testing was done using both linear and switching power supplies, significant interference from high frequency noise was observed in ChipScope™ Pro during testing of the sampling channels. Since the switching power supply was ruled out as the primary source of noise in the preceding section, attention was focused on the signal-to-noise ratio of the AD-7864 converters. For a 12 bit converter, noise + distortion is in the range of 74dB, which is certainly enough to effect distortion in the channels [17]; hence, there was good reason to suspect that the AD converters were the source of the noise observed in ChipScope™ Pro. Regardless of the cause, a digital Low-Pass Filter (LPF) was utilized to

filter out the unwanted high-frequency interference. The addition of a digital LPF into the Simulink® model was easily achieved [[20] and [21]], and the SDC's software foundation prevented the addition of a hardware LPF into the design.

A cutoff frequency for the digital LPF was selected at 5kHz which was sufficient to pass all frequencies below 1kHz without significant attenuation. The 1kHz bandwidth was adequate for SDC laboratories since it satisfied frequency analysis requirement for all planned solid state laboratories. To minimize the filter order and reduce computational burden on the simulation software and the FPGA, a large transition band was used. A 5kHz band required only a 3rd order LPF for 20dB of attenuation in the stop band. The derivation of the difference equation coefficients for a symmetric Finite Impulse Response (FIR) Butterworth filter is shown below.

$$\left(\begin{array}{c} F_S = \frac{24\ \text{MHz}}{170} \quad F_C = 5\ \text{kHz} \\ F_{passband} = 5\text{-}10\text{kHz} \quad F_{stopband} = 10\text{kHz} \\ \\ \theta_1 = \omega_1 T = 2\pi\,(F_C) / F_S \\ \theta_2 = \omega_2 T = 2\pi\,(F_{stopband}) / F_S \end{array} \right) \tag{2.12}$$

The prewarped analog frequencies are:

$$\left(\omega_1' = \tan\frac{\theta_1}{2} \qquad \omega_2' = \tan\frac{\theta_2}{2} \right) \tag{2.13}$$

$$\left(\omega_1' = \tan\frac{\theta_1}{2} \qquad \omega_2' = \tan\frac{\theta_2}{2} \right) \tag{2.14}$$

Translating the prewarped analog frequencies into a normalized butterworth filter gives:

$$\left(\omega = \omega_1' \qquad \omega_a = \frac{\omega_2'}{\omega_1'} \right) \tag{2.15}$$

Deriving the minimum butterworth filter order gives:

$$\left(N=[\log(10^{-M_{dB}/10} - 1)] / 2\log(\omega_a) = 2.58 \approx 3 \right) \tag{2.16}$$

Hence the transfer function for the normalized butterworth filter is:

$$H_{LP}(s) = \left[H_{LP}(s)\right]_{s=\frac{s}{\omega_1'}} = \left[\frac{1}{s^3 + 2s^2 + s + 1}\right]_{s=\frac{s}{\omega_1'}} \tag{2.17}$$

Utilizing the bilinear transform $\left[s = \frac{z-1}{z+1}\right]$, substituting into $\left[H_{LP}(s)\right]$, and deriving the difference equation gives:

$$\left(\begin{array}{l} H_{LP}(z) = \left[H_{LP}(s)\right]_{s=\frac{z-1}{z+1}} = \\ 0.2450e\text{-}6\ x(n) + 0.7349e\text{-}6\ x(n-1) \\ +0.7349e\text{-}6\ x(n\text{-}2) + 0.2450y(n-3) - 2.9749y(n-2) \\ +2.9500y(n-1) = 0.9752y(n) \end{array} \right) \tag{2.18}$$

The coefficients were verified using the Matlab "maxflat" function, and the filter was integrated in the simulation AD converter subsystem. The magnitude response of the filter is shown in Figure 28. The filter subsystem is shown in Figure 29.

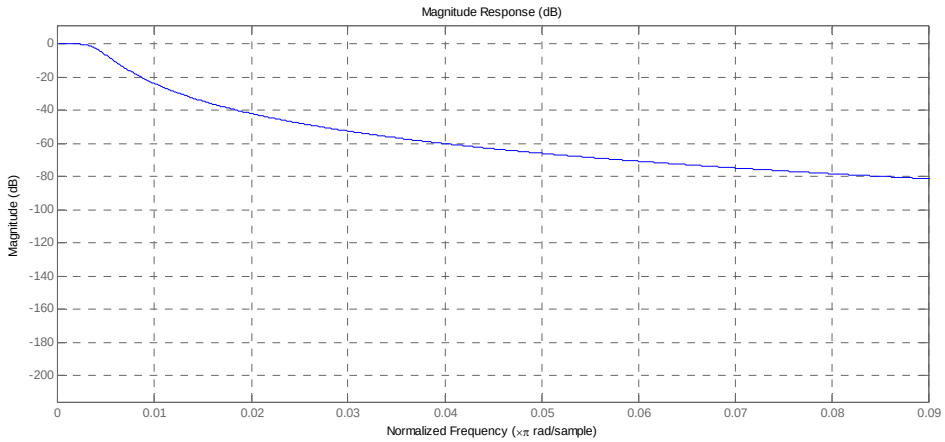

Figure 28. Lowpass Filter Magnitude Response.

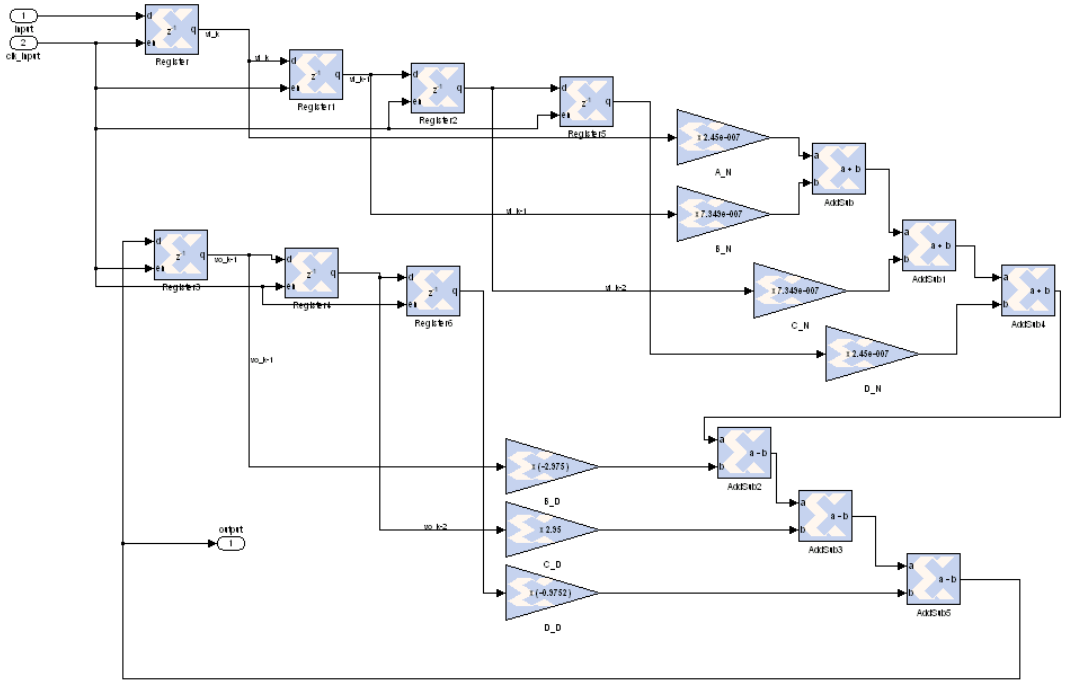

Figure 29. Symmetric FIR Butterworth Filter [After [20]].

The results of the filter design were dramatic. A comparison of a sampled three input signals (shown in blue) at 1kHz, 5kHz and 10kHz and their filtered counterparts (shown in green) are shown in Figure 30.

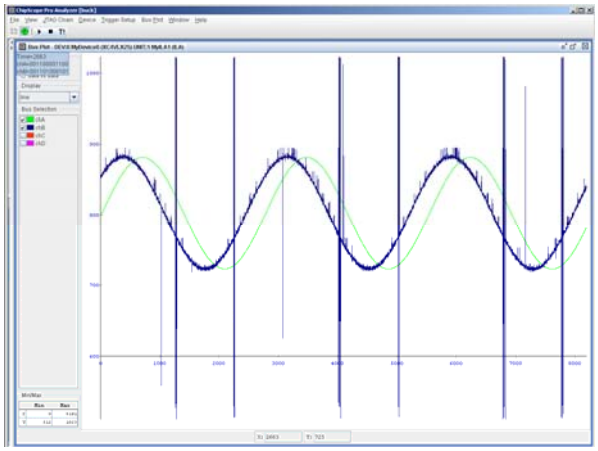

Figure 30. Original and Filtered 1kHz Signal.

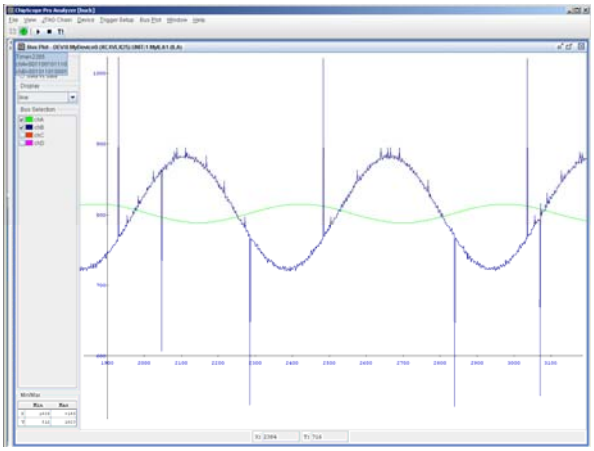

Figure 31. Original and Filtered 5kHz Signal.

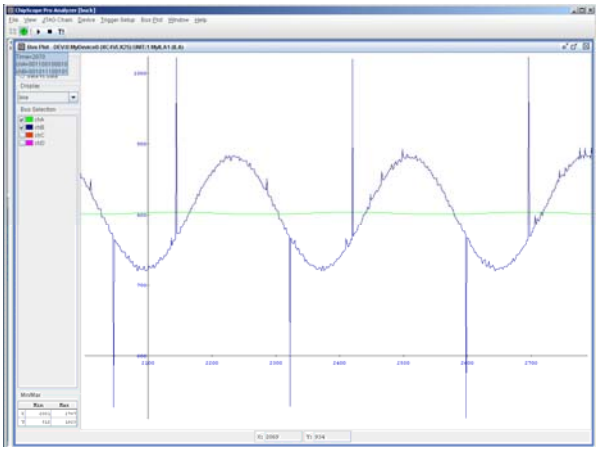

Figure 32. Original and Filtered 10kHz Signal.

Excellent attenuation was shown as the frequency approached the stop band and virtually all high-frequency interference was blocked.

D. CHAPTER SUMMARY

This chapter covered the analog signal interface PCB and the power source interface PCB design, construction and testing. An overview of why a switching power source was used in the SDC and techniques used to troubleshoot and reduce system noise was presented. Finally, a digital LPF was developed and implemented to eliminate EMI. Chapter III summarizes this thesis and presents topics for future research.

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IV. CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY

This thesis began with an overview of the SDC objectives and descriptions of the hardware and software used therein. The purpose and function of each component was explained in order to develop a working knowledge of SDC capabilities. Standard operating procedures were developed to serve as a working document for future students conducting laboratories in the SDC and to provide them with a better understanding of design flow prior to execution. The thesis expounded on the design and testing of the interface PCBs and system performance testing was done to ensure EMI from the switching power supply did not inhibit signal sampling. Finally, a lowpass filter was designed and implemented to reduce the high frequency interference on the channel signals noted in ChipScope™ Pro during testing.

B. CONCLUSIONS

The SDC is an excellent resource for digital control of power electronics design. Students gain a fundamental understanding of the advantages of FPGA digital control of power systems and digital signal analysis using ChipScope™ Pro. The SDC enables students to make accurate predictions of component behavior using software simulation and testing to verify results. The SDC can be adapted as necessary to changing technology due to its flexible FPGA foundation. New programs and ideas can be implemented without changing hardware and increasing cost. Moreover, as noted in Chapter I, the SDC is not limited to power electronics design and

control. Since three systems are available, students in other curriculums can explore the potential of FPGA design and control of other electrical systems.

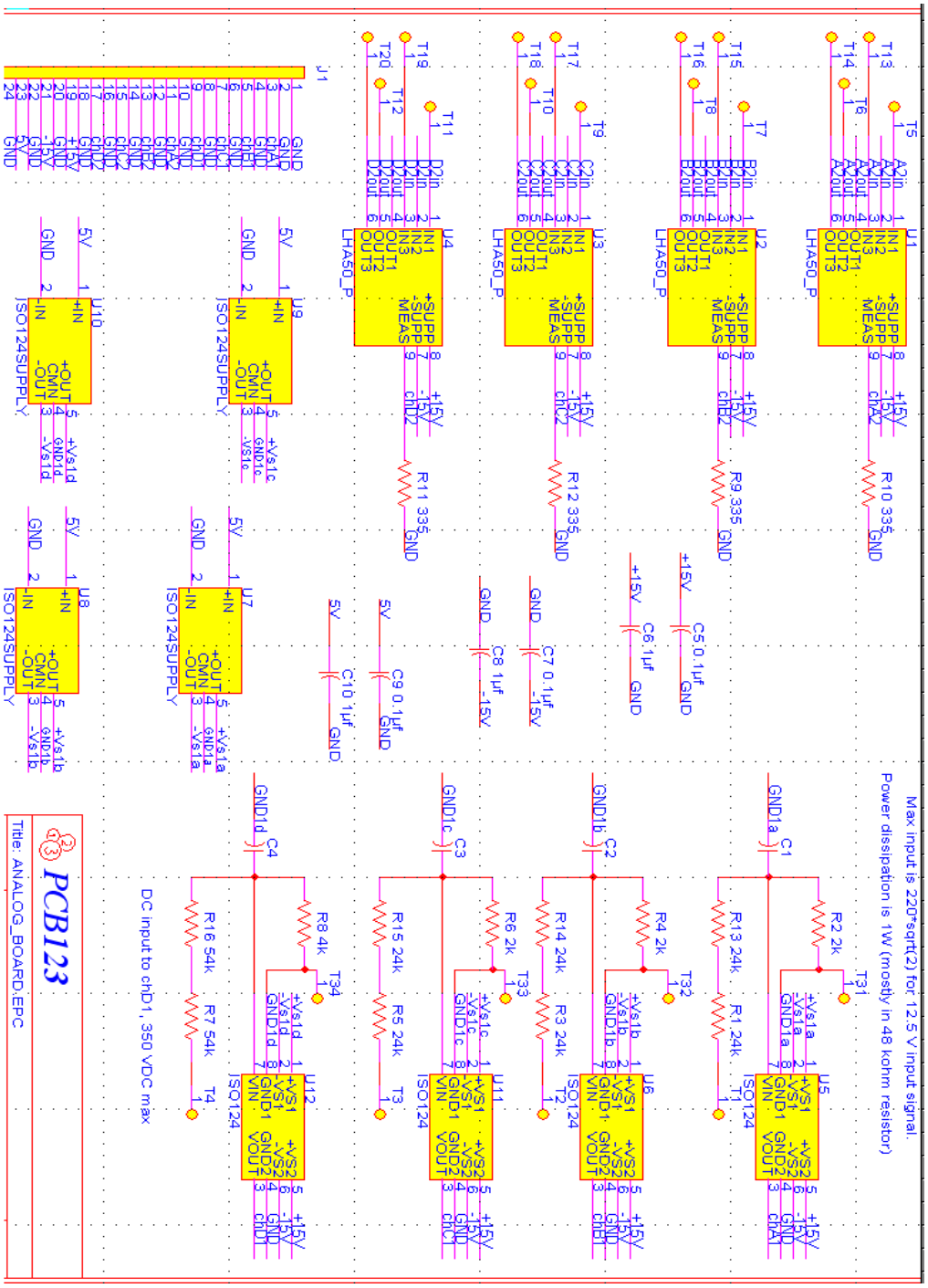
C. RECOMMENDATIONS FOR FURTHER RESEARCH

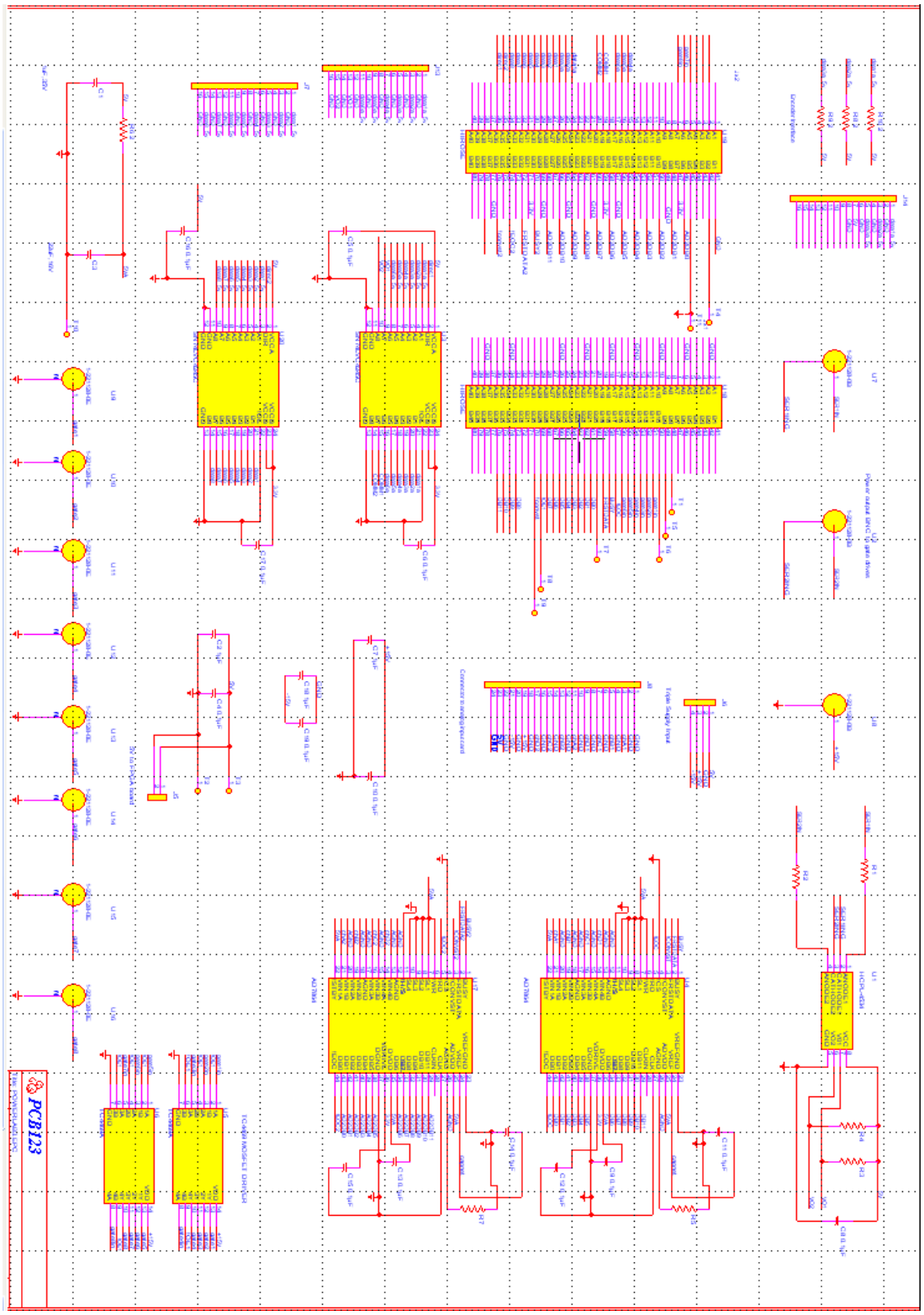
There are many opportunities for research in the area of FPGA digital control of power electronics. Below are three ideas to serve as platforms for further research:

- Development of FPGA laboratories for other electrical engineering curriculum tracks.
- Redundant FPGA control of power electronics in order to improve system reliability.
- Design and Implementation of FPGA "soft-radio" systems.

The reprogrammable nature of the FPGA hardware enables a large number of programs and systems to be explored without the burden of purchasing and installing new hardware; hence, electrical engineering design, especially at the graduate level, can benefit greatly from the use of FPGA technology.

APPENDIX A:PCB SCHEMATICS AND VIRTEX-4™ BOM




PCB123

Item	Qty	Reference	Part Number	Description	Manufacturer	Supplier	DEPOP	ASSEMBLY NOTES
62	1	R15	RES-1000-XXX-10-0201-0050	100, 1/20 W, 1% 0201 resistor				
63	1	R17	RES-5R11-XXX-10-1206-0125	5.11, 1/8 W, 1% 1206 resistor			Y	
64	1	R21	RES-1151-XXX-10-0603-0062	1.15k, 1/16 W, 1% 0603 resistor				
65	1	R22	RES-3012-XXX-10-0603-0062	30.1k, 1/16 W, 1% 0603 resistor				
66	2	R24	RES-0600-XXX-10-0402-0050	60, 1/20 W, 1% 0402 resistor				
		R23	RES-0600-XXX-10-0402-0050	60, 1/20 W, 1% 0402 resistor				
67	2	R58	RES-1001-XXX-10-0603-0062	1k, 1/16 W, 1% 0603 resistor				
		R36	RES-1001-XXX-10-0603-0062	1k, 1/16 W, 1% 0603 resistor				
68	2	R38	RES-0330-XXX-10-0603-0062	33, 1/16 W, 1% 0603 resistor				
		R39	RES-0330-XXX-10-0603-0062	33, 1/16 W, 1% 0603 resistor				
69	1	R41	RES-1241-XXX-10-0603-0062	1.24k, 1/16 W, 1% 0603 resistor				
70	1	R45	RES-2003-XXX-10-0603-0062	200k, 1/16 W, 1% 0603 resistor				
71	1	R56	RES-1582-XXX-10-0603-0062	15.8k, 1/16 W, 1% 0603 resistor				
72	1	SW1	1101M2S3CQE2	Slide Switch 6A @ 28VDC SPDT TH	C&K			
73	5	SW2	TL1105SPF160Q	Push button switch	ESWITCH			
		SW5	TL1105SPF160Q	Push button switch	ESWITCH			
		SW6	TL1105SPF160Q	Push button switch	ESWITCH			
		SW7	TL1105SPF160Q	Push button switch	ESWITCH			
		SW8	TL1105SPF160Q	Push button switch	ESWITCH			
74	1	SW9	KA-S-1-1-08-R	8 position DIP switch SPST	ESWITCH			
76	1	TP3	KEYSTONE 5011	Color Coded PCB Test Point - Black	Keystone			
77	3	U1	PTH05050WAH	Regulated Step-down DC/DC ADJ @ 6A with tracking	TI	Memec		
		U2	PTH05050WAH	Regulated Step-down DC/DC ADJ @ 6A with tracking	TI	Memec		
		U3	PTH05050WAH	Regulated Step-down DC/DC ADJ @ 6A with tracking	TI	Memec		
78	1	U4	XC4VLX25-SF363	Virtex-4 1.2 V Field Programmable Gate Array	Xilinx	Memec		
79	1	U5	REF3025AIDBZ	CMOS Voltage Reference	TI	Memec	Y	
80	1	U6	XC9536XV-7VQ44C	CPLD 36 macrocell 2.5 volt VQ44	XILINX	Memec		
81	1	U7	AT45DB321B-TC	Serial DataFlash TSOP32, 32Mb	Atmel		Y	
82	1	U8	AT45DB161B-TC	Serial DataFlash TSOP28, 16Mb	Atmel			
83	1	U9	NT5DS32M16AF-75B	512Mb DDR SDRAM, CSP60	Nanya	Memec		
84	1	U10	TPS73101DBV	Adjustable, 150mA LDO regulator, SOT23-5	TI	Memec		
85	1	U13	BCM5221A4KPT	10/100 Ethernet PHY	Broadcom	Memec		
86	1	U14	TPS3809K33DBV	Power Supply Supervisor	TI	Memec		
87	1	U15	MAX3223CDB	RS232 Interface IC SSOP20	TI	Memec		
88	1	U16	SN74TVC3010DBQR	10-bit voltage clamp	TI	Memec		
89	1	U21	TPS72218DBV	Adjustable, 50mA LDO regulator, SOT23-5	TI	Memec	Y	
90	1	U22	XCF08PFS48C	Platform Flash In-system programmable PROM 8Mb	Xilinx	Memec	Y	
91	1	Y1	SM13T-20-25.0M-REX	25MHz crystal, SM, 50ppm, 0/+70 degrees	Pletronics	Memec		
92	1	Y2	SM7745DV-100.0M-REX	100MHz clock, SM, 50ppm, 3.3V, 0/+70 degrees	Pletronics	Memec		
93	1	Y3	DIP14	14 pin .100" DIP socket, .300" width, **MACHINED** pins	Any			

Board Name : V4LX25LC Development Board
Board Part Number : DS-BD-V4LX25LC
Board Revision : 1
Release : 1
Date : October 27th, 2004
Designer : JBE

Item	Qty	Reference	Part Number	Description	Manufacturer	Supplier	DEPOP	ASSEMBLY NOTES
1	16	C1	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C2	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C4	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C5	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C7	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C8	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C10	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C36	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C46	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C47	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C54	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C55	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C67	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C87	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C90	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
		C201	293D337X96R3D2	330uFd solid tantalum capacitor, 6.3V, 7343 case	Sprague			
2	7	C3	CAP-0106-X5R-2020-1206-006	10uF ceramic capacitor, 1206 6.3V X5R -20/+20%				
		C6	CAP-0106-X5R-2020-1206-006	10uF ceramic capacitor, 1206 6.3V X5R -20/+20%				
		C9	CAP-0106-X5R-2020-1206-006	10uF ceramic capacitor, 1206 6.3V X5R -20/+20%				
		C86	CAP-0106-X5R-2020-1206-006	10uF ceramic capacitor, 1206 6.3V X5R -20/+20%				
		C89	CAP-0106-X5R-2020-1206-006	10uF ceramic capacitor, 1206 6.3V X5R -20/+20%				
		C109	CAP-0106-X5R-2020-1206-006	10uF ceramic capacitor, 1206 6.3V X5R -20/+20%				
		C151	CAP-0106-X5R-2020-1206-006	10uF ceramic capacitor, 1206 6.3V X5R -20/+20%				
3	4	C11	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%			Y	
		C12	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%			Y	
		C189	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%			Y	
		C191	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%			Y	
4	7	C13	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%			Y	
		C190	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%			Y	
		C192	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%			Y	
		C197	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%			Y	
		C198	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%			Y	
		C199	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%			Y	
		C200	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%			Y	
5	1	C14	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%			Y	
6	14	C15	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C20	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C31	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C39	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C42	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C45	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C50	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C53	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C59	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C62	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C66	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C85	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				

Item	Qty	Reference	Part Number	Description	Manufacturer	Supplier	DEPOP	ASSEMBLY NOTES
		C88	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
		C167	CAP-0016-X5R-2020-0603-006	1uF ceramic capacitor, 0603 6V X5R -20/+20%				
7	38	C16	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C18	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C21	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C23	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C30	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C37	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C38	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C41	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C43	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C44	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C49	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C52	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C58	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C61	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C65	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C81	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C82	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C83	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C84	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C91	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C92	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C93	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C94	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C107	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C152	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C153	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C154	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C161	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C162	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C163	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C164	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C165	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C168	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C169	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C171	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C172	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C175	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
		C176	CAP-1009-X7R-2020-0402-006	0.1uF ceramic capacitor, 0402 6.3V X7R -20/+20%				
8	40	C17	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C19	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C22	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C24	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C25	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C26	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C27	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C28	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C29	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C32	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C33	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C34	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C35	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C40	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C48	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C51	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				

Item	Qty	Reference	Part Number	Description	Manufacturer	Supplier	DEPOP	ASSEMBLY NOTES
		C56	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C57	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C60	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C63	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C64	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C68	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C69	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C70	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C71	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C72	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C73	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C74	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C75	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C76	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C77	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C78	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C79	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C80	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C155	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C156	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C166	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C170	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C173	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C174	CAP-0109-X7R-2020-0402-006	0.01uF ceramic capacitor, 0402 6V X7R -20/+20%				
9	7	C99	CAP-0109-X5R-2020-0201-006	10nF ceramic capacitor, 0201 6.3V X5R -20/+20%				
		C100	CAP-0109-X5R-2020-0201-006	10nF ceramic capacitor, 0201 6.3V X5R -20/+20%				
		C101	CAP-0109-X5R-2020-0201-006	10nF ceramic capacitor, 0201 6.3V X5R -20/+20%				
		C102	CAP-0109-X5R-2020-0201-006	10nF ceramic capacitor, 0201 6.3V X5R -20/+20%				
		C108	CAP-0109-X5R-2020-0201-006	10nF ceramic capacitor, 0201 6.3V X5R -20/+20%				
		C113	CAP-0109-X5R-2020-0201-006	10nF ceramic capacitor, 0201 6.3V X5R -20/+20%				
		C114	CAP-0109-X5R-2020-0201-006	10nF ceramic capacitor, 0201 6.3V X5R -20/+20%				
10	1	C110	CAP-100C-X7R-2020-0603-016	100pF ceramic capacitor, 0603 16V X7R -20/+20%				
11	2	C116	CAP-0227-X7R-2020-1206-010	2.2uF ceramic capacitor, 1206 10V X7R -20/+20%				
		C111	CAP-0227-X7R-2020-1206-010	2.2uF ceramic capacitor, 1206 10V X7R -20/+20%				
12	2	C112	CAP-1009-X7R-2020-0603-006	0.1uF ceramic capacitor, 0603 6V X7R -20/+20%				
		C115	CAP-1009-X7R-2020-0603-006	0.1uF ceramic capacitor, 0603 6V X7R -20/+20%				
13	4	C149	CAP-0013-X7R-2020-0402-006	0.001uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C150	CAP-0013-X7R-2020-0402-006	0.001uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C157	CAP-0013-X7R-2020-0402-006	0.001uF ceramic capacitor, 0402 6V X7R -20/+20%				
		C160	CAP-0013-X7R-2020-0402-006	0.001uF ceramic capacitor, 0402 6V X7R -20/+20%				
14	2	C158	CAP-015C-X7R-2020-0603-016	15pF ceramic capacitor, 0603 16V X7R -20/+20%				
		C159	CAP-015C-X7R-2020-0603-016	15pF ceramic capacitor, 0603 16V X7R -20/+20%				
15	10	DS1	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS2	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS3	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS4	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS5	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS6	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS7	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS8	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS9	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
		DS11	LGQ971	CHIPLED, 0603, green	Infineon	Memec		
16	2	DS10	LSQ976	CHIPLED, 0603, red	Infineon	Memec		
		DS12	LSQ976	CHIPLED, 0603, red	Infineon	Memec		
17	2	FB1	FB321611T-601Y-S	Ferrite Bead 600ohm@100MHz 200mA max	Cal Chip			
		FB3	FB321611T-601Y-S	Ferrite Bead 600ohm@100MHz 200mA max	Cal Chip			

Item	Qty	Reference	Part Number	Description	Manufacturer	Supplier	DEPOP	ASSEMBLY NOTES
18	1	FB2	FB321611T-601Y-S	Ferrite Bead 600ohm@100MHz 200mA max	Cal Chip		Y	
19	1	JD1	K22-E9S-N30	D-Subminiature 9 pin female	Kycon			
20	1	JM1	HFJ11-2450E	FASTJACK WITH 10/100BASE-T MAGNETICS	HALO			
21	1	JP1	PJ-002A-SMT	4 pin barrel jack, SMT	CUI Stack			
22	3	JP2	HEADER-04-V-100-D-T	.100" pin header, 2x2 Vertical				
		JP5	HEADER-04-V-100-D-T	.100" pin header, 2x2 Vertical				
		JP8	HEADER-04-V-100-D-T	.100" pin header, 2x2 Vertical				
23	6	JP4	HEADER-02-V-100-S-T	.100" pin header, 1x2 Vertical				
		JP7	HEADER-02-V-100-S-T	.100" pin header, 1x2 Vertical				
		JP10	HEADER-02-V-100-S-T	.100" pin header, 1x2 Vertical				
		JP11	HEADER-02-V-100-S-T	.100" pin header, 1x2 Vertical				
		JP27	HEADER-02-V-100-S-T	.100" pin header, 1x2 Vertical				
		JP28	HEADER-02-V-100-S-T	.100" pin header, 1x2 Vertical				
24	1	JP12	HEADER-08-V-100-D-T	2x4 .100" TH header Vertical				
25	2	JP13	HEADER-02-H-100-S-T	.100" pin header, 1x2 RA				
		JP29	HEADER-02-H-100-S-T	.100" pin header, 1x2 RA				
26	1	JP14	HEADER-06-H-100-S-T	.100" pin header, 1x6 RA				
27	2	JP18	HEADER-14-H-079-D-T	2x7 2mm TH Header, RA, Shrouded				
		JP15	HEADER-14-H-079-D-T	2x7 2mm TH Header, RA, Shrouded				
28	1	JP16	HEADER-50-V-100-D-T	2x25.100" TH header Vertical				CUT PIN 50
29	2	JP24	HEADER-03-V-100-S-T	.100" pin header, 1x3 Vertical				
		JP23	HEADER-03-V-100-S-T	.100" pin header, 1x3 Vertical				
30	1	JP26	HEADER-08-H-100-D-T	2x4 .100" TH header RA				
31	1	JP33	HEADER-03-H-100-S-T	.100" pin header, 1x3 RA			Y	
32	2	JX1	FX2C-80P-1.27DSAL	P160 80 position board-to-board plug (header)	Hirose			
		JX2	FX2C-80P-1.27DSAL	P160 80 position board-to-board plug (header)	Hirose			
33	1	J3	HEADER-14-V-100-S-T	1X14 .100" pin header				
34	4	NE1	SJ5018-0-ND	Stick on rubber foot - thick	3M			MOUNT TO BOTTOM AS PER SSB
		NE2	SJ5018-0-ND	Stick on rubber foot - thick	3M			MOUNT TO BOTTOM AS PER SSB
		NE3	SJ5018-0-ND	Stick on rubber foot - thick	3M			MOUNT TO BOTTOM AS PER SSB
		NE4	SJ5018-0-ND	Stick on rubber foot - thick	3M			MOUNT TO BOTTOM AS PER SSB
35	1	NE10	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP2[1-2] (SEE CF)
36	1	NE11	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP2[3-4] (SEE CF)
38	1	NE15	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP5[1-2] (SEE CF)
39	1	NE17	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP5[3-4] (SEE CF)
40	1	NE18	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP8[1-2] (SEE CF)
41	1	NE19	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP8[3-4] (SEE CF)
42	1	NE20	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP12[1-2]
43	1	NE21	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP12[3-4]
44	1	NE22	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP12[5-6]
45	1	NE23	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP13[1-2]
46	1	NE24	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP14[1-2]
47	1	NE25	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP14[4-5]
48	1	NE27	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP23[2-3]
49	1	NE28	SHUNT-LO-CL	Shunt, closed, low body				INSTALL ON JP24[1-2]
50	1	NE29	MOC-16216B-B	2X16 Character LCD Module	MYTECH			SOLDER TO J3
51	2	NE30		Metal Standoff				USE TO MOUNT LCD TO BOARD
		NE32		Metal Standoff				USE TO MOUNT LCD TO BOARD
52	4	NE31		Screw -				USE TO MOUNT LCD TO BOARD
		NE33		Screw -				USE TO MOUNT LCD TO BOARD
		NE34		Screw -				USE TO MOUNT LCD TO BOARD
		NE35		Screw -				USE TO MOUNT LCD TO BOARD
53	1	NE36	SHUNT-LO-CL	Shunt, closed, low body			Y	INSTALL ON JP33[1-2]
54	2	Q2	BCR108	Digital Silicon NPN SOT23 package	Infineon	Memec		
		Q1	BCR108	Digital Silicon NPN SOT23 package	Infineon	Memec		
55	4	R1	RES-3000-XXX-10-0603-0062	300, 1/16 W, 1% 0603 resistor				

Item	Qty	Reference	Part Number	Description	Manufacturer	Supplier	DEPOP	ASSEMBLY NOTES
		R2	RES-3000-XXX-10-0603-0062	300, 1/16 W, 1% 0603 resistor				
		R14	RES-3000-XXX-10-0603-0062	300, 1/16 W, 1% 0603 resistor				
		R19	RES-3000-XXX-10-0603-0062	300, 1/16 W, 1% 0603 resistor				
56	1	R3	RES-6980-XXX-10-1206-0125	698, 1/8 W, 1% 1206 resistor				
57	9	R4	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R6	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R40	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R43	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R44	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R63	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R64	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R65	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
		R66	RES-1300-XXX-10-0603-0062	130, 1/16 W, 1% 0603 resistor				
58	1	R5	RES-2211-XXX-10-1206-0125	2.21k, 1/8 W, 1% 1206 resistor				
59	1	R7	RES-1742-XXX-10-1206-0125	17.4k, 1/8 W, 1% 1206 resistor				
60	8	R8	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
		R9	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
		R32	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
		R33	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
		R35	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
		R37	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
		R120	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
		R121	RES-49R9-XXX-10-0402-0050	49.9, 1/20 W, 1% 0402 resistor				
61	33	R10	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R11	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R12	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R13	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R16	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R18	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R20	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R34	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R42	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R46	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R47	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R48	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R49	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R50	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R51	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R52	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R53	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R54	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R55	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R57	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R59	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R60	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R61	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R62	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R67	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R68	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R69	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R70	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R71	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R72	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R73	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R74	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				
		R75	RES-4701-XXX-10-0603-0062	4.7k, 1/16 W, 1% 0603 resistor				

APPENDIX B:VIRTEX-4™ CONDENSED USER'S GUIDE

A. VIRTEX-4™ DEVELOPMENT BOARD COMPONENTS

All figures and information in this appendix were excerpted verbatim from the Virtex-4™ LC Development Board user's guide. Figure numbers were changed to correspond with this thesis.

1. DDR SDRAM

The Virtex-4™ LC Development Board provides 64MB of DDR SDRAM memory (32Mx16). A high-level block diagram of the DDR SDRAM interface is shown below.

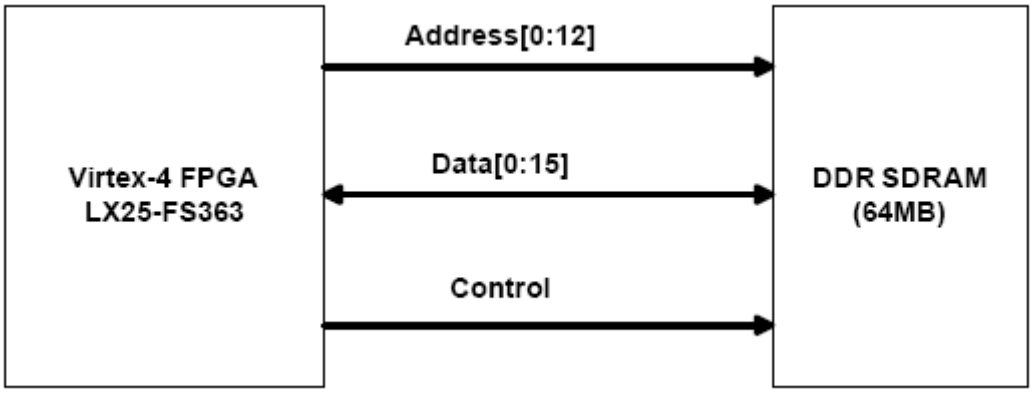


Figure 33. DDR SDRAM Interface.

2. Clock Sources

The clock generation section of the Virtex-4™ LC Development Board provides all necessary clock for the I/O devices located on the board as well as the DDR SDRAM memory. An on-board 100MHz oscillator provides the system clock input to the FPGA. In addition to the above clock input, a socket is provided on the board that can be used

to provide a single-ended LVTTL clock input to the FPGA via an 8 or 4-pin oscillator. The following figure shows the clock.

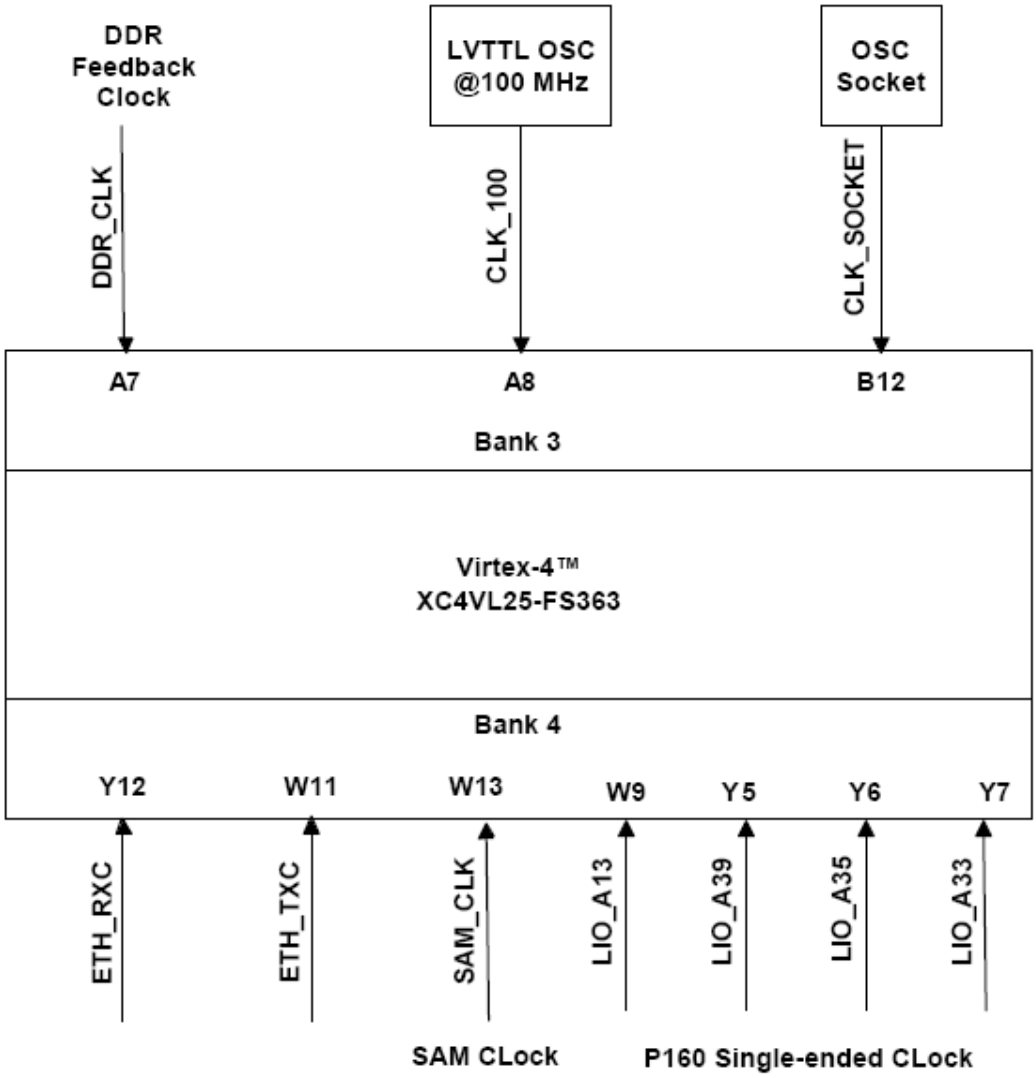


Figure 34. Clock Sources on the Virtex-4™ board.

3. 10/100 Ethernet PHY

The Virtex-4™ LC Development Board provides a 10/100 Ethernet port for network connection. A high-level block diagram of the 10/100 Ethernet interface is shown in the figure below.

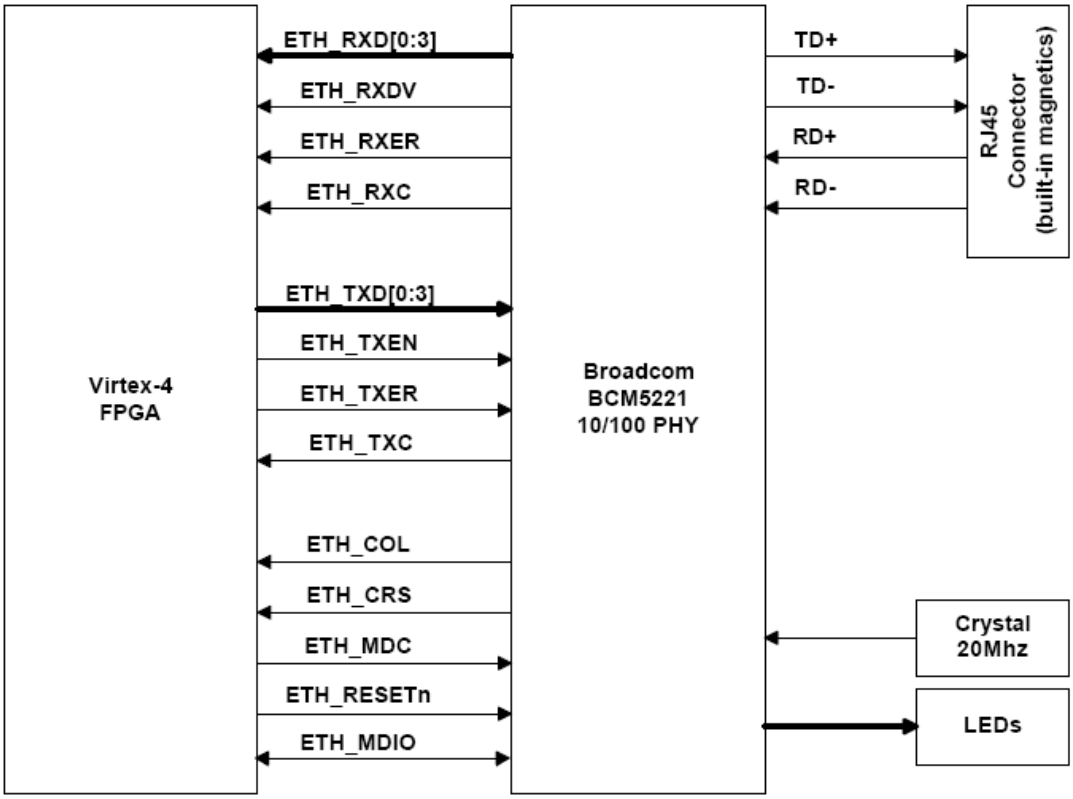


Figure 35. 10/100 Ethernet Interface.

4. LCD Panel

The Virtex-4™ LC Development Board provides an 8-bit interface to a 2x16 LCD panel (MYTECH MOC-16216B-B). The following table shows the LCD interface signals.

Signal Name	Description	Virtex-4 Pin #
D0	LCD Data Bit 0	T2
D1	LCD Data Bit 1	T1
D2	LCD Data Bit 2	R2
D3	LCD Data Bit 4	T3
D4	LCD Data Bit 4	R4
D5	LCD Data Bit 5	R3
D6	LCD Data Bit 6	R1
D7	LCD Data Bit 7	R5
EN	LCD Enable Signal	R6
RW	LCD Write Signal (this signal is connected to logic "0" on the Virtex-4 LC board, enabling write only cycles).	NA
RS	LCD Register Select Signal	T6

Table 1. LCD Interface Signals.

5. RS232 Interface

The Virtex-4™ LC Development Board provides an RS232 interface with RX and TX signals and jumpers for connecting the RTS and CTS signals. The following figure shows the RS232 interface to the Virtex-4™ LX25 FPGA.

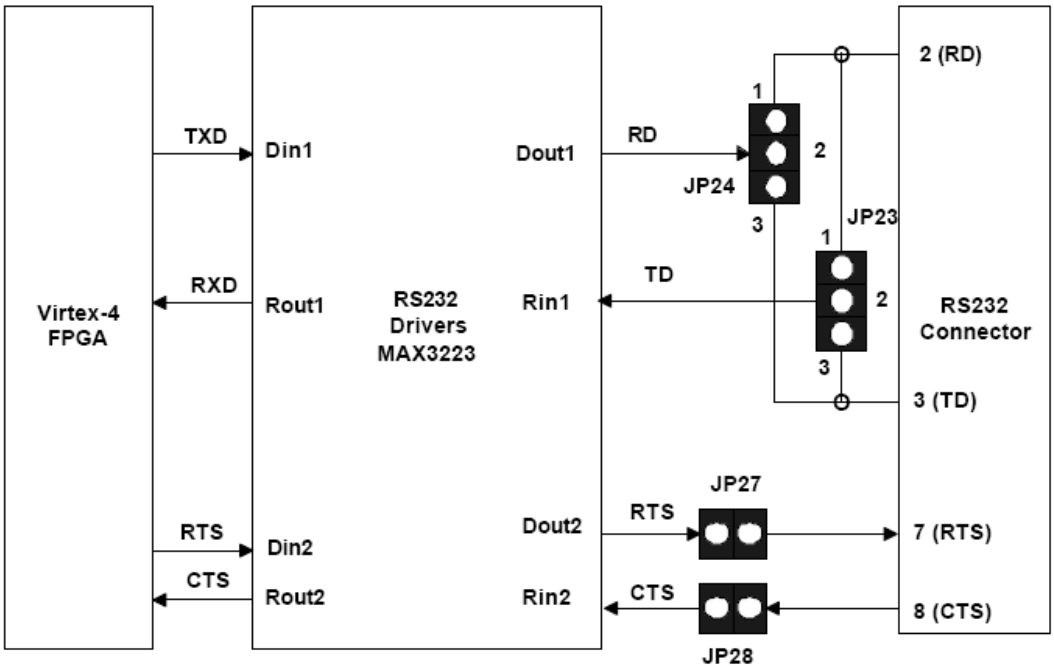


Figure 36. RS232 Interface.

6. User DIP and PB Switches

The Virtex-4™ LC Development Board provides four user push button switches as described in the following table. An active low signal is generated when a given switch is pressed.

Signal Name	Description	Virtex-4 Pin #
PUSH1	SW5	B4
PUSH2	SW6	C2
PUSH3	SW7	C1
PUSH4	SW8	F2

Table 2. Push Button Switch Pin Assignments.

The Virtex-4™ LC Development Board provides an 8-position DIP switch as described in the following table. An active low signal is generated when a given switch is ON.

Signal Name	Description	Virtex-4 Pin #
DIP1	User Switch Input 1	T4
DIP2	User Switch Input 2	U3
DIP3	User Switch Input 3	U4
DIP4	User Switch Input 4	V4
DIP5	User Switch Input 5	W2
DIP6	User Switch Input 6	W3
DIP7	User Switch Input 7	W4
DIP8	User Switch Input 8	Y4

Table 3. DIP Switch Pin Assignments.

7. User LEDs

The Virtex-4™ LC Development Board provides four user LEDs that can be turned “ON” by driving the LEDx signal to a logic “0”. The following table shows the user LEDs and their associated FPGA pin assignments.

LED Designation	LED #	Virtex-4 Pin #
DS9	LED1	M5
DS10	LED2	M3
DS11	LED3	M6
DS12	LED4	N5

Table 4. LED Pin Assignments.

8. User GPIO

The Virtex-4™ LC Development Board provides a general-purpose GPIO header (JP26) that consists of 6 user signals, a 3.3V power pin and a ground pin. The following table shows the GPIO pin assignments.

Signal Name	Connector Pin #	Virtex-4 Pin #
GPIO_0	2	V18
GPIO_1	3	V17
GPIO_2	4	W19
GPIO_3	5	W18
GPIO_4	6	W17
GPIO_5	7	Y17
3.3V	1	-
GND	8	-

Table 5. GPIO Pin Assignments.

9. Configuration and Debug Ports

Various methods of configuration and debug support are provided on the Virtex-4™ LC Development Board to assist designers during testing and debugging of their applications. The following sections provide brief descriptions of each of these interfaces.

a. JTAG Gain

The following figure shows the JTAG chain on the Virtex-4™ LC Development Board. The XC9536XV along with a serial data flash is used to configure the FPGA.

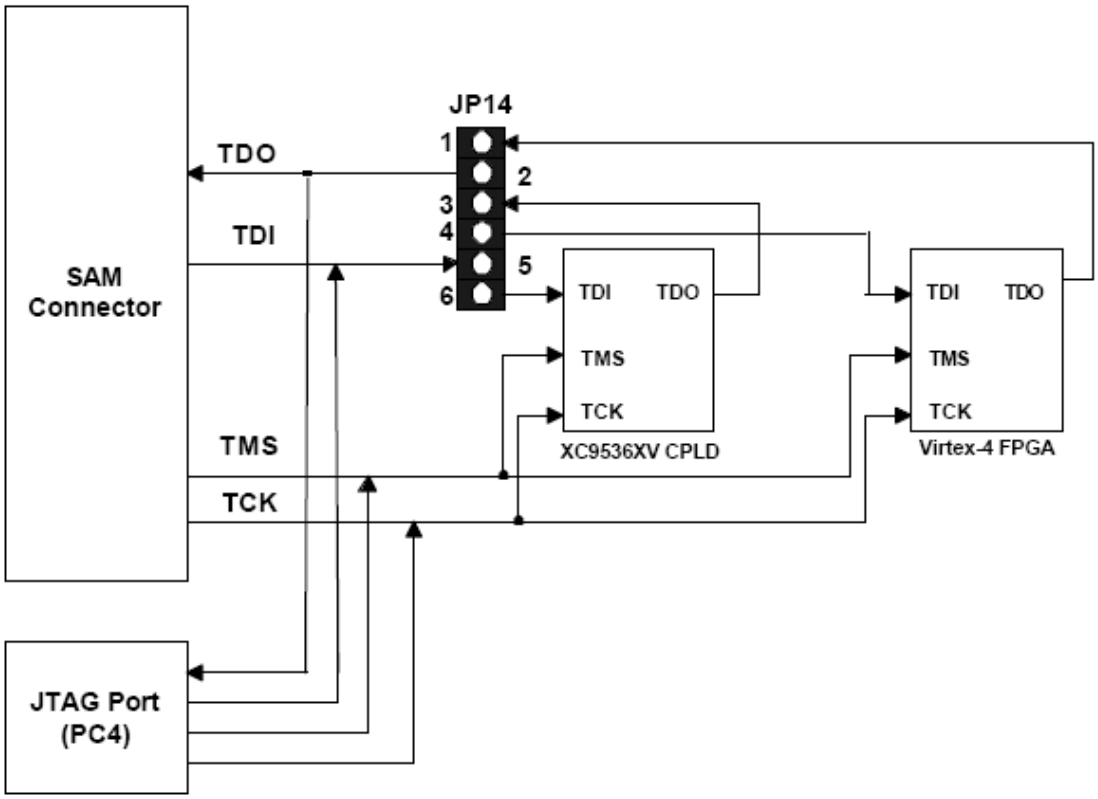


Figure 37. Vitex-4 LC Development Board JTAG Chain.

b. System ACE Module Connector

The Virtex-4™ Development Board provides the SAM 50-pin connector on the board for using the Memec System ACE Module (SAM). The SAM can be used to configure the FPGA or to provide bulk flash to a MicroBlaze processor implementation. The Virtex-4™ Development Board provides a System ACE interface that can be used to configure the Virtex-4 FPGA. The interface also gives software designers the ability to run realtime operating systems (RTOS) from removable CompactFlash cards. The Memec System ACE module (DS-KIT-SYSTEM ACE) can be used to perform both of these functions. The figure below shows the System ACE module connected to the header on the Virtex-4™.

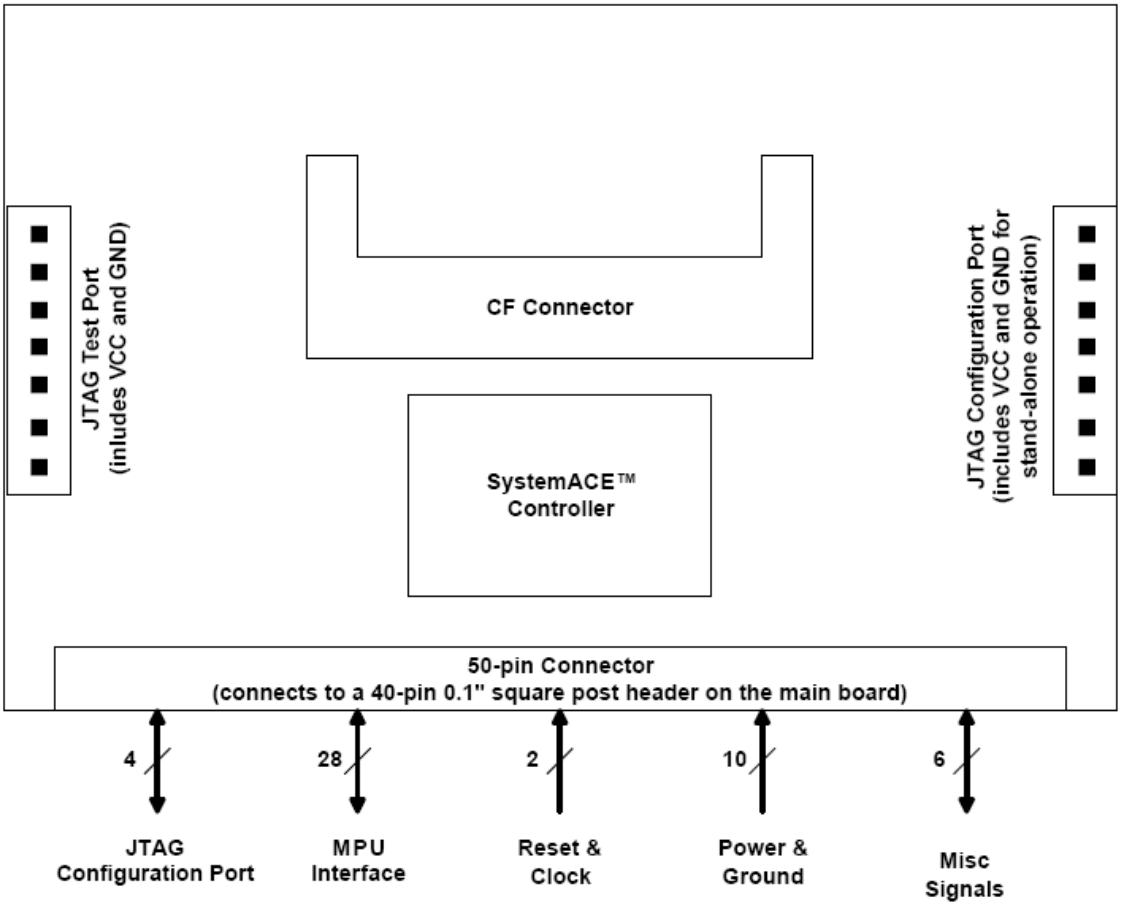


Figure 38. System ACE module connecter.

c. System ACE Controller Signal Description

The following table shows the System ACE Module signal assignments to the FPGA I/O pins. It should be noted that on the V4LC development board the System ACE module and the P160 slot share a common bus structure. These two interfaces use a dedicated chip select for processor access while the other signals such as the address/data and control are shared.

Virtex-4 Pin #	System ACE Signal Name	SAM Connector Pin # (JP16)		System ACE Signal Name	Virtex-4 Pin #
	3.3V	1	2	**3.3V**	
	TDO	3	4	**GND**	
	TMS	5	6	CLOCK	W13
	TDI	7	8	**GND**	
	PROGRAMn	9	10	TCK	
	GND	11	12	**GND**	
J19	OEn	13	14	INITn	
U13	MPA0	15	16	WEn	T7
R19	MPA2	17	18	MPA1	R20
	2.5V	19	20	MPA3	V16
N18	MPD00	21	22	**2.5V**	
N16	MPD02	23	24	MPD01	N17
U19	MPD04	25	26	MPD03	T15
R17	MPD06	27	28	MPD05	U17
P17	MPD08	29	30	MPD07	V19
T18	MPD10	31	32	MPD09	M17
P16	MPD12	33	34	MPD11	U15
K19	MPD14	35	36	MPD13	R18
U9	MPA4	37	38	MPD15	H19
T19	MPA6	39	40	MPA5	T20
E20	IRQ	41	42	**GND**	
E16	RESETn	43	44	CEn	F19
	DONE	45	46	BRDY	U8
	CCLK	47	48	BITSTREAM	
	GND	49	50	**NC**	

Table 6. GPIO Pin Assignments.

d. Serial Flash

This section describes the procedure for programming the Atmel serial data flash on the Memec Virtex-4™ Development Board. This serial flash along with a CPLD is used to configure the Virtex-4™ FPGA located on the development board on power up. The following figure shows a high-level block diagram of the serial flash interface to the Virtex-4™ FPGA.

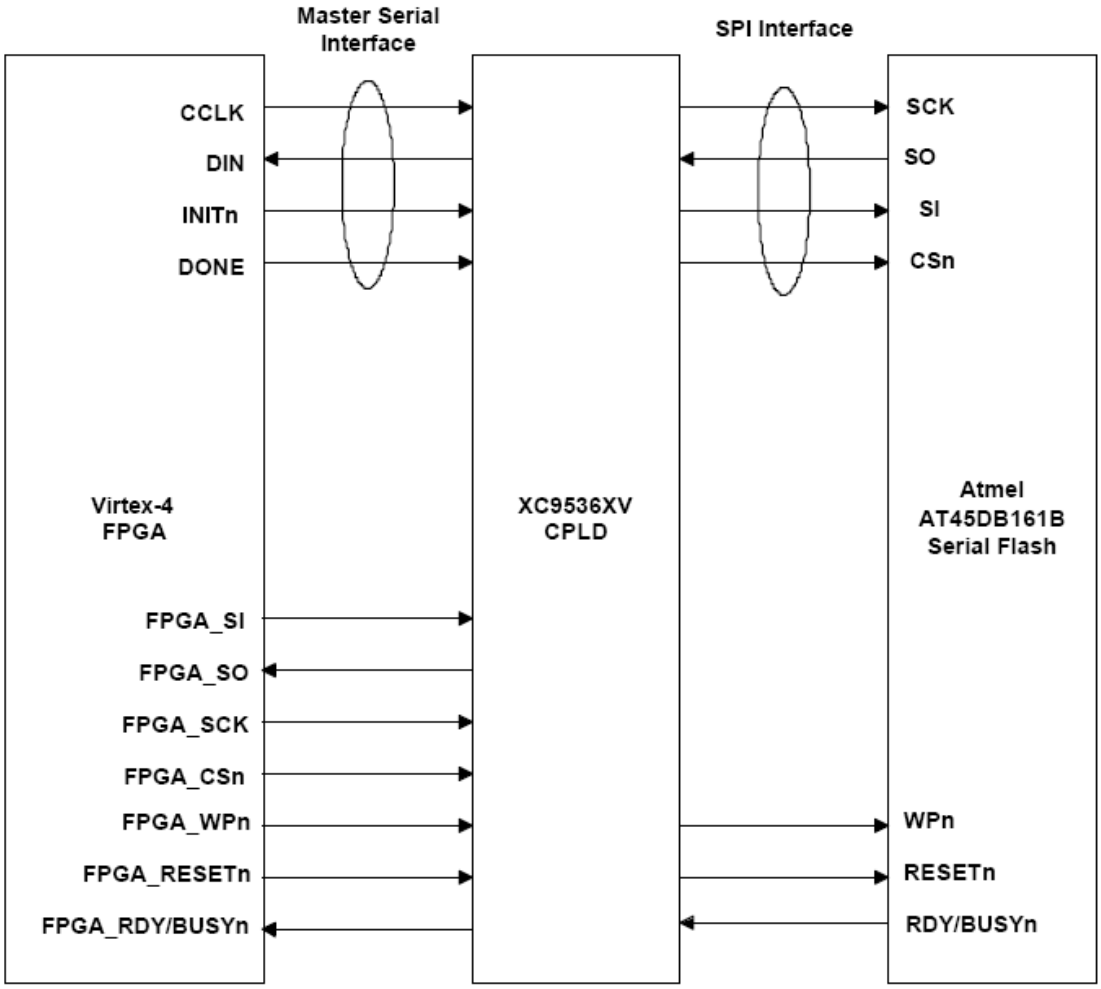


Figure 39. Virtex-4™ Configuration Interface.

An interface is provided between the FPGA and the CPLD to allow access to the serial flash after the FPGA has been configured. This interface uses FPGA I/O pins to interface to the serial flash via the SPI port. The Virtex-4™ FPGA uses 8Mb of the serial flash memory for configuration and this interface allows the other 8Mb to be used for general-purpose application after the FPGA has been configured. The following table shows the signals used to implement the interface between the FPGA and the CPLD after the FPGA has been configured.

Signal Name	Description	Virtex-4 Pin #
FPGA_SI	Serial Flash SPI port data input signal	P4
FPGA_SO	Serial Flash SPI port data output signal	P5
FPGA_SCK	Serial Flash SPI port clock input signal	P1
FPGA_CSn	Serial Flash SPI port chip select input signal	N2
FPGA_WPn	Serial Flash SPI port write protect input signal	N3
FPGA_RESETn	Serial Flash SPI port reset input signal	P2
FPGA_RDY/BUSYn	Serial Flash SPI port ready output signal	N4

Table 7. FPGA SPI Interface Pin Assignments.

The primary function of the CPLD is to translate the Master Serial interface to the SPI interface of the serial flash. The XC9536XV CPLD uses the FPGA CCLK clock along with the INITn and DONE signals to drive the SPI SI, SCK and CSn signals. The SO output of the serial flash is used by the CPLD to drive the DIN signal of the FPGA.

e. JTAG Chain on the Virtex-4™ Development Board

The following figure shows the JTAG chain on the Virtex-4™ Development Board. As mentioned, the CPLD is used for interfacing to the configuration flash and does not provide any user logic. Hence, this CPLD is programmed by Memec prior to shipping the board. The programming file for the CPLD is provided in case re-programming of the CPLD becomes necessary. The CPLD must be programmed prior to performing any operations on the serial flash such as erasing, programming, reading or verifying.

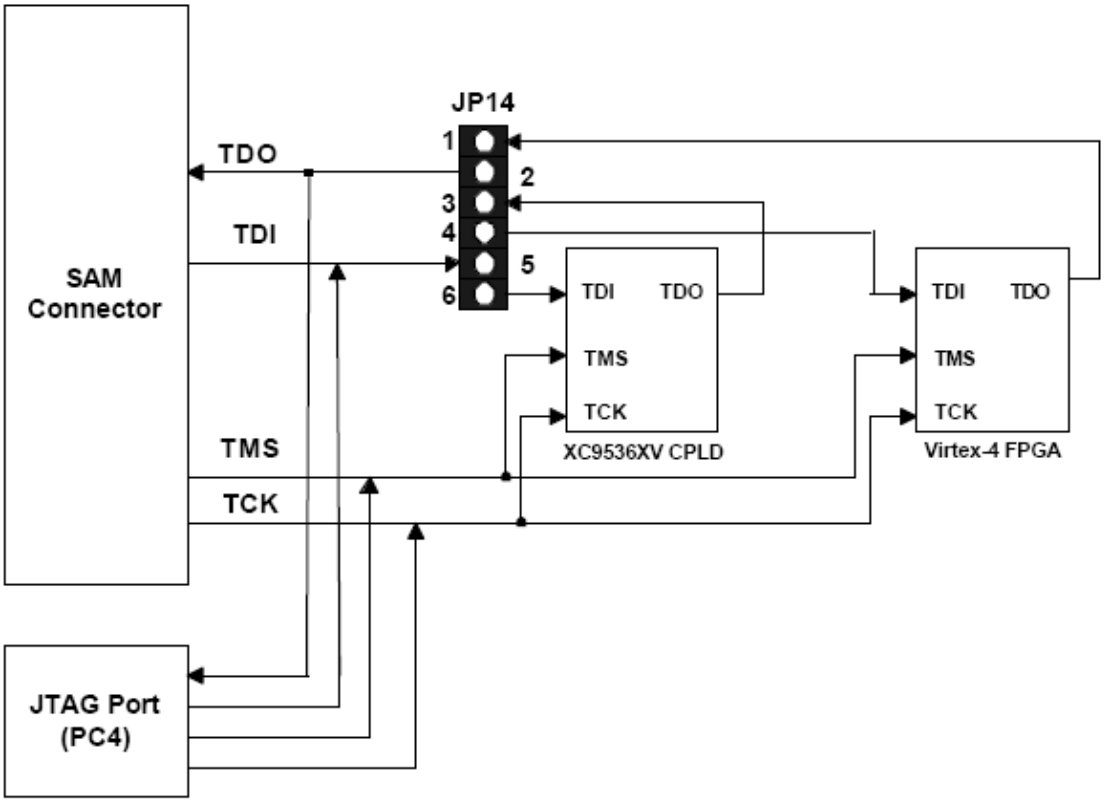


Figure 40. Virtex-4™ Development Board JTAG Chain.

The following table shows jumper settings for the JTAG chain on the Virtex-4™ Development Board.

Devices in the JTAG Chain	JP14 Jumpers Installed
CPLD and FPGA	Pins 1-2, 3-4 and 5-6
CPLD	Pins 2-3 and 5-6
FPGA	Pins 1-2 and 4-5

Table 8. JTAG Chain Jumper Settings.

f. Configuration Flash on the Virtex-4™ Development Board

The following figure shows the detail of the interface between the FPGA and the serial flash. A PC4 cable is used to program the serial flash with the FPGA bitstream. Once the flash is programmed, on power-up, the

CPLD will read the data from the flash and configure the FPGA over the Master Serial interface.

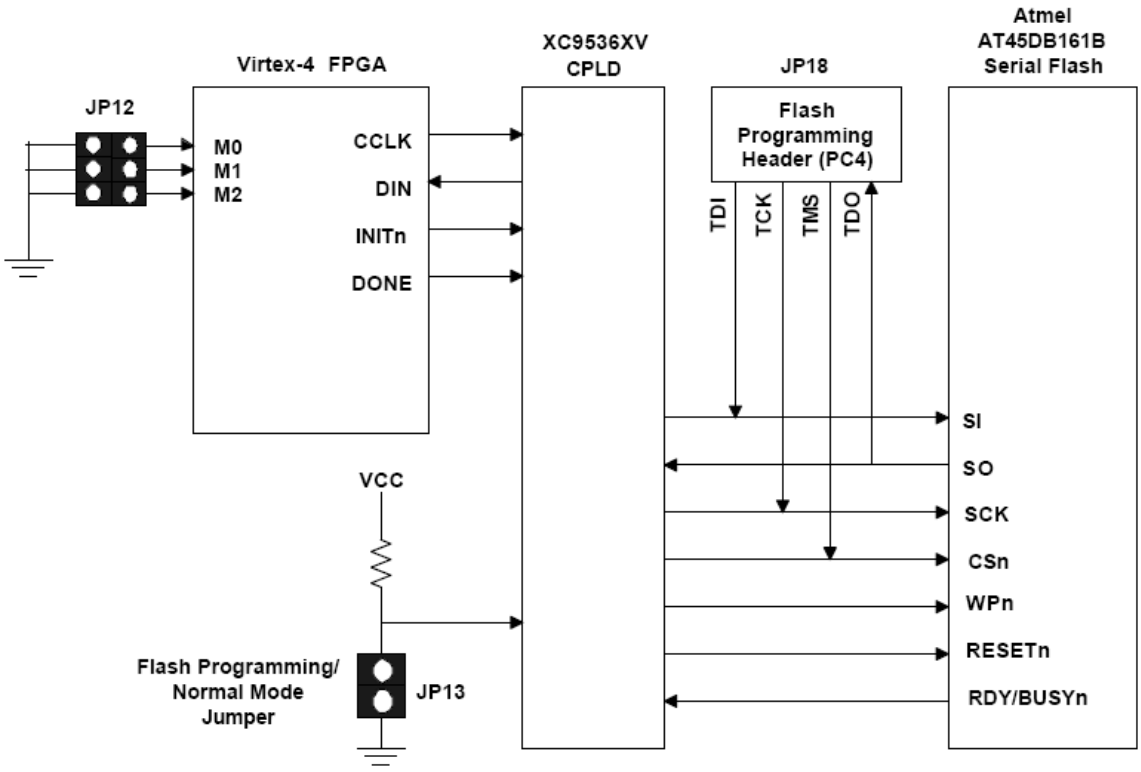


Figure 41. Serial Flash Configuration Interface.

g. JTAG Port

The Virtex-4™ Development Board provides a JTAG port (PC4 type) connector for configuration of the FPGA. The following figure shows the pin assignments for the PC4 header on this development board.

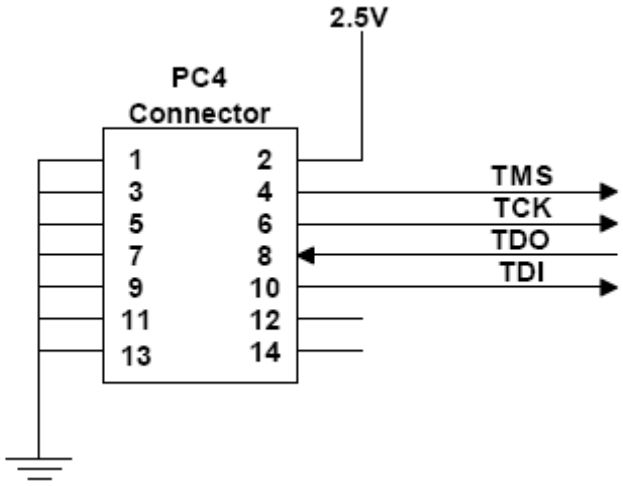


Figure 42. PC4 JTAG Port Connector.

h. Configuration Modes

The following table shows the Virtex-4™ Development Board configuration modes.

Mode	PC Pull-up	Configuration Mode Jumpers			
		1-2 (M2)	3-4 (M1)	5-6 (M0)	7-8 (HSWAP_EN)
Master Serial	Yes	Closed	Closed	Closed	Closed
Master Serial	No	Closed	Closed	Closed	Open
Slave Serial	Yes	Open	Open	Open	Closed
Slave Serial	No	Open	Open	Open	Open
Master SelectMap	Yes	Closed	Open	Open	Closed
Master SelectMap	No	Closed	Open	Open	Open
Slave SelectMap	Yes	Open	Open	Closed	Closed
Slave SelectMap	No	Open	Open	Closed	Open
JTAG	Yes	Open	Closed	Open	Closed
JTAG	No	Open	Closed	Open	Open

Table 9. FPGA Configuration Mode Jumper Settings.

10. Voltage Regulators

The following figure shows the voltage regulators that are used on Virtex-4™ Development Board to provide various on-board voltage sources. As shown in the following figure, a connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all onboard regulators to generate the 1.2V, 2.5V, and 3.3V voltages.

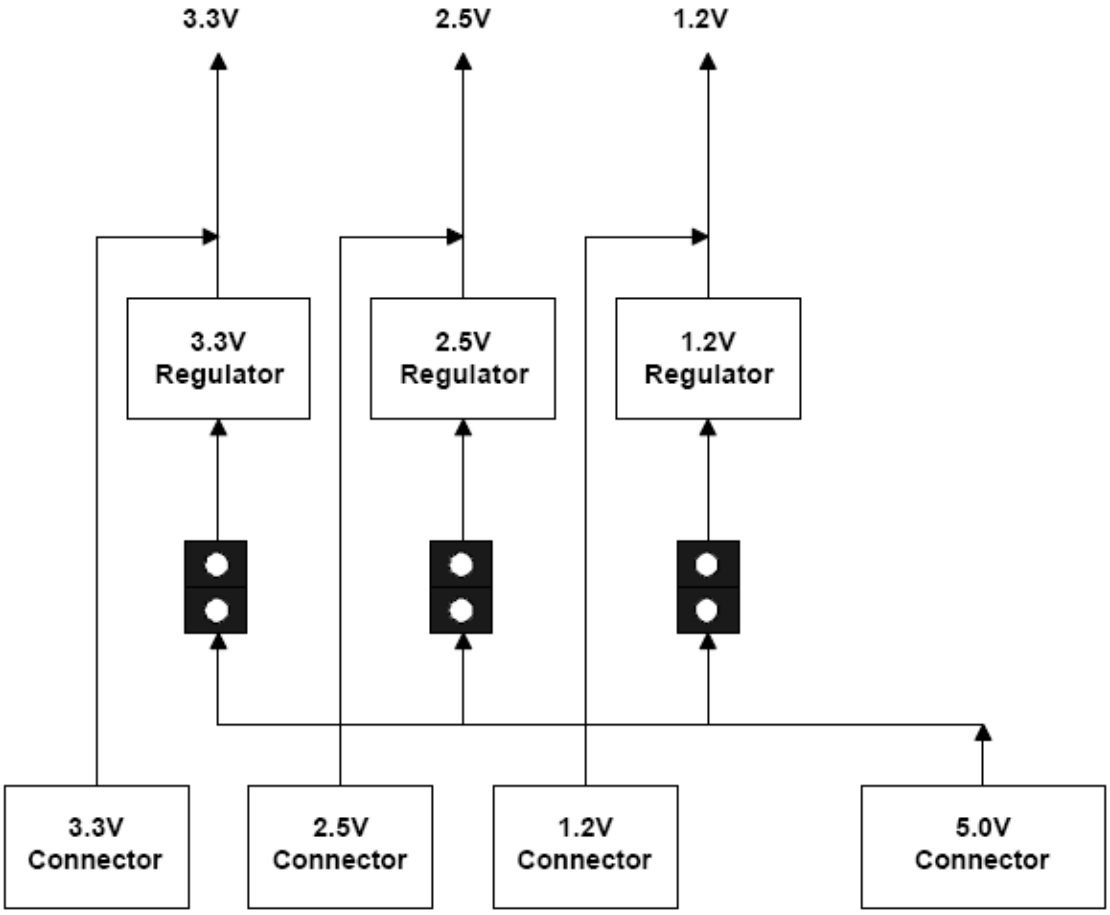


Figure 43. Voltage Regulators.

The following table shows the power provided on the development board for the on-board voltage sources. A 32.5W power adapter (5V @ 6.5A) is used to provide power to the on-board regulators. The following table shows typical power usage on the Virtex-4™ Development Board.

Voltage	Current (A)	Power (W)	Comments
1.2V	1.5	1.8	FPGA Core voltage
2.5V	1.5	3.75	FPGA I/O voltage, P160 supply voltage
3.3V	3	9.9	FPGA I/O voltage, P160 supply voltage.
Total Power		**15.45**	

Table 10. FPGA Configuration Mode Jumper Settings.

If the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage source and bypass the on-board regulators.

11. Bank I/O Voltage

The following table shows the Virtex-4™ Development Board bank I/O voltages on the Virtex-4™ Development Board.

Bank #	I/O Voltage
0	2.5V
1	3.3V
2	3.3V
3	2.5V
4	3.3V
5	3.3V
6	2.5V
7	3.3V
8	3.3V

Table 11. I/O Bank Voltages.

12. P160 Expansion Module Signal Assignments

The following tables show the Virtex-4™ pin assignments to the P160 Expansion Module connectors (JX1 & JX2) located on the Virtex-4™ Development Board.

Virtex-4 FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	Virtex-4 FPGA Pin #
NC	TCK	A1	B1	FPGA.BITSTREAM	NC
	GND	A2	B2	SM.DOUT/BUSY	NC
NC	TMS	A3	B3	FPGA.CCLK	NC
	Vin	A4	B4	DONE	NC
NC	TDI	A5	B5	INITn	NC
	GND	A6	B6	PROGRAMn	NC
NC	TDO	A7	B7	NC	NC
	3.3V	A8	B8	LIOB8	D18
D17	LIOA9	A9	B9	LIOB9	C18
	GND	A10	B10	LIOB10	G17
D16	LIOA11	A11	B11	LIOB11	C17
	2.5V	A12	B12	LIOB12	F17
W9	LIOA13	A13	B13	LIOB13	C16
	GND	A14	B14	LIOB14	F18
E18	LIOA15	A15	B15	LIOB15	D15
	Vin	A16	B16	LIOB16	G19
G20	LIOA17	A17	B17	LIOB17	C15
	GND	A18	B18	LIOB18	F19
F20	LIOA19	A19	B19	LIOB19	D13
	3.3V	A20	B20	LIOB20	E20
E19	LIOA21	A21	B21	LIOB21	C13
	GND	A22	B22	LIOB22	D19
C20	LIOA23	A23	B23	LIOB23	D12
	2.5V	A24	B24	LIOB24	C19
B19	LIOA25	A25	B25	LIOB25	C12
	GND	A26	B26	LIOB26	B18
A18	LIOA27	A27	B27	LIOB27	D9
	Vin	A28	B28	LIOB28	B17
B16	LIOA29	A29	B29	LIOB29	C9
	GND	A30	B30	LIOB30	A16
B15	LIOA31	A31	B31	LIOB31	D8
	3.3V	A32	B32	LIOB32	A15
Y7	LIOA33	A33	B33	LIOB33	C8
	GND	A34	B34	LIOB34	J16
Y6	LIOA35	A35	B35	LIOB35	H16
	2.5V	A36	B36	LIOB36	G16
F16	LIOA37	A37	B37	LIOB37	E16
	GND	A38	B38	LIOB38	E15
Y5	LIOA39	A39	B39	LIOB39	F15
	Vin	A40	B40	LIOB40	E14

Table 12. P160 Connector Pin Assignments.

Virtex-4 FPGA Pin #	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	Virtex-4 FPGA Pin #
H18	RIOA1	A1	B1	**GND**	
H17	RIOA2	A2	B2	RIOB2	K16
J18	RIOA3	A3	B3	**Vin**	
J17	RIOA4	A4	B4	RIOB4	J15
K18	RIOA5	A5	B5	**GND**	
K17	RIOA6	A6	B6	RIOB6	L16
L17	RIOA7	A7	B7	**3.3V**	
M18	RIOA8	A8	B8	RIOB8	M15
M17	RIOA9	A9	B9	**GND**	
N18	RIOA10	A10	B10	RIOB10	N16
P17	RIOA11	A11	B11	**2.5V**	
T15	RIOA12	A12	B12	RIOB12	N17
U15	RIOA13	A13	B13	**GND**	
T18	RIOA14	A14	B14	RIOB14	P16
U19	RIOA15	A15	B15	**Vin**	
R17	RIOA16	A16	B16	RIOB16	U17
R18	RIOA17	A17	B17	**GND**	
H19	RIOA18	A18	B18	RIOB18	V19
J19	RIOA19	A19	B19	**3.3V**	
K20	RIOA20	A20	B20	RIOB20	U18
K19	RIOA21	A21	B21	**GND**	
L20	RIOA22	A22	B22	RIOB22	R16
L19	RIOA23	A23	B23	**2.5V**	
M20	RIOA24	A24	B24	RIOB24	T17
M19	RIOA25	A25	B25	**GND**	
N19	RIOA26	A26	B26	RIOB26	R15
P20	RIOA27	A27	B27	**Vin**	
U12	RIOA28	A28	B28	RIOB28	V20
P19	RIOA29	A29	B29	**GND**	
V11	RIOA30	A30	B30	RIOB30	U16
V10	RIOA31	A31	B31	**3.3V**	
V9	RIOA32	A32	B32	RIOB32	U13
U9	RIOA33	A33	B33	**GND**	
R20	RIOA34	A34	B34	RIOB34	V13
R19	RIOA35	A35	B35	**2.5V**	
T20	RIOA36	A36	B36	RIOB36	V16
T19	RIOA37	A37	B37	**GND**	
V8	RIOA38	A38	B38	RIOB38	V12
U8	RIOA39	A39	B39	**Vin**	
T7	RIOA40	A40	B40	RIOB40	V15

Table 13. P160 Connector Pin Assignments.

APPENDIX C: SEMITEACH® POWER CONVERTER

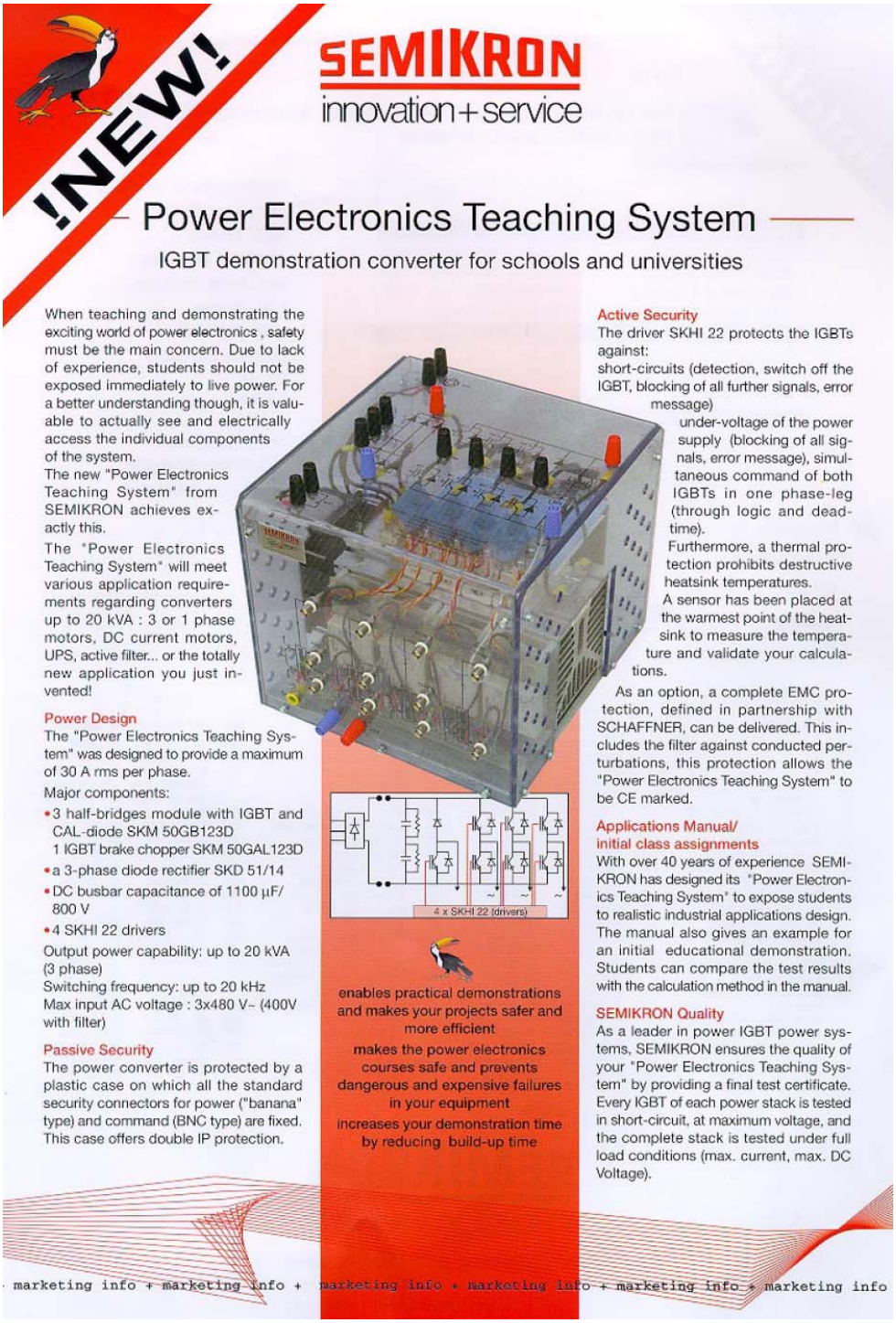


Figure 44. SEMITEACH® Power Converter [From [11]].

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