



AFRL-RZ-WP-TR-2008-2107

**HIGH-DENSITY POWER SUPPLIES USING SILICON
CARBIDE (SiC)
Delivery Order 0001**

David C. Sheridan, Ph.D.

SemiSouth Laboratories, Inc.

**MARCH 2008
Final Report**

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REPORT DOCUMENTATION PAGE				Form Approved OMB No. 0704-0188	
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1. REPORT DATE (DD-MM-YY) March 2008		2. REPORT TYPE Final		3. DATES COVERED (From - To) 28 August 2006 – 27 August 2007	
4. TITLE AND SUBTITLE HIGH-DENSITY POWER SUPPLIES USING SILICON CARBIDE (SiC) Delivery Order 0001				5a. CONTRACT NUMBER FA8650-06-D-2608-0001	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER 63175C	
6. AUTHOR(S) David C. Sheridan, Ph.D.				5d. PROJECT NUMBER 1168	
				5e. TASK NUMBER 13	
				5f. WORK UNIT NUMBER 11681312	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) SemiSouth Laboratories, Inc. 201 Research Boulevard Starkville, MS 39759				8. PERFORMING ORGANIZATION REPORT NUMBER AFRL-SSL-012-FR-2006-12	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Air Force Research Laboratory Propulsion Directorate Wright-Patterson Air Force Base, OH 45433-7251 Air Force Materiel Command United States Air Force				10. SPONSORING/MONITORING AGENCY ACRONYM(S) AFRL/RZPE	
				11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S) AFRL-RZ-WP-TR-2008-2107	
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited.					
13. SUPPLEMENTARY NOTES Report contains color. PAO Case Number: WPAFB 08-3011, 22 Apr 2008.					
14. ABSTRACT This program was designed to improve the reliability and performance of electrical power systems and components, while reducing operational life cycle costs for a wide variety of aircraft and space electrical power-system generation, conditioning, and utilization equipment applications. To achieve these objectives, research efforts were conducted for the advancement of silicon carbide (SiC) power device technology in the technical areas of advanced design, manufacturability, and component reliability. This delivery order was successful in developing of a normally off enhancement mode vertical junction field effect transistor (VJFET) switch that is capable of blocking 600V-1200V with a zero voltage gate bias. These devices were shown to operate and maintain blocking voltage up to 200 °C, and could be used as a high temperature and harsh-environment capable transistor technology. Reliability of the VJFET device was also investigated showing excellent stability after initial infant mortality issues were screened.					
15. SUBJECT TERMS Silicon carbide, vertical junction field effect transistor, reliability, enhancement mode, high temperature					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT: SAR	18. NUMBER OF PAGES 72	19a. NAME OF RESPONSIBLE PERSON (Monitor)
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			James D. Scofield, Ph.D. 19b. TELEPHONE NUMBER (Include Area Code) N/A

Abstract

The Power Division (AFRL/RZP) of the Propulsion Directorate (AFRL/RZ) conducts in-house and contractual efforts on a wide variety of aircraft and space electrical power-system generation, conditioning, and utilization component technologies. These programs are designed to improve the reliability and performance of electrical power systems and components, while reducing operational life cycle costs for a wide range of weapon system platforms. To achieve these objectives, research efforts were conducted in DO1 for the advancement of silicon carbide (SiC) power device technology in the technical areas of advanced design, manufacturability, and component reliability.

This delivery order was successful in developing of a normally-off VJFET switch that is capable of blocking 600V-1200V with a zero voltage gate bias. These devices were shown to operate and maintain blocking voltage up to 200 °C, and could be used as a high temperature and harsh-environment capable transistor technology. Reliability of the VJFET device was also investigated showing excellent stability after initial infant mortality issues were screened.

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1. EXECUTIVE SUMMARY

The Power Division (AFRL/RZP) of the Propulsion Directorate (AFRL/RZ) conducts in-house and contractual efforts on a wide variety of aircraft and space electrical power-system generation, conditioning, and utilization component technologies. These programs are designed to improve the reliability and performance of electrical power systems and components, while reducing operational life cycle costs for a wide range of weapon system platforms. To achieve these objectives, research efforts will be conducted in DO1 for the advancement of silicon carbide (SiC) power device technology in the technical areas of advanced design, manufacturability, and component reliability.

2. TASK 1: ADVANCED DEVICE DESIGN

2.1. Overview

Task 1 includes the research and development of the optimal device structure for PT and NPT 600V/1200V SiC VJFETs, and companion Schottky diodes. A true high voltage enhancement mode SiC VJFET would be an ideal switch for use in high power switching applications due to its theoretically high switching speed, low conduction and switching losses compared to a Si IGBT, capable of high temperature operation ($>300^{\circ}\text{C}$), and a positive temperature coefficient for ease of paralleling. Attempts at developing normally-off high-voltage VJFETs usually yield designs using a depletion mode device in a cascode configuration, have complex buried gate structures that are limited by short channel DIBL effects at high voltages, or are unfavorably biased far into the bipolar mode of operation. Figure 1 gives a comparison of the types of devices available with a VJFET design. As

shown, there are depletion mode, quasi-enhancement mode, and devices that are fully enhancement mode. In this delivery order, full enhancement mode devices are designed and demonstrated with excellent electrical characteristics that enable high-temperature normally-off operation that is suitable for power supply and converter applications.

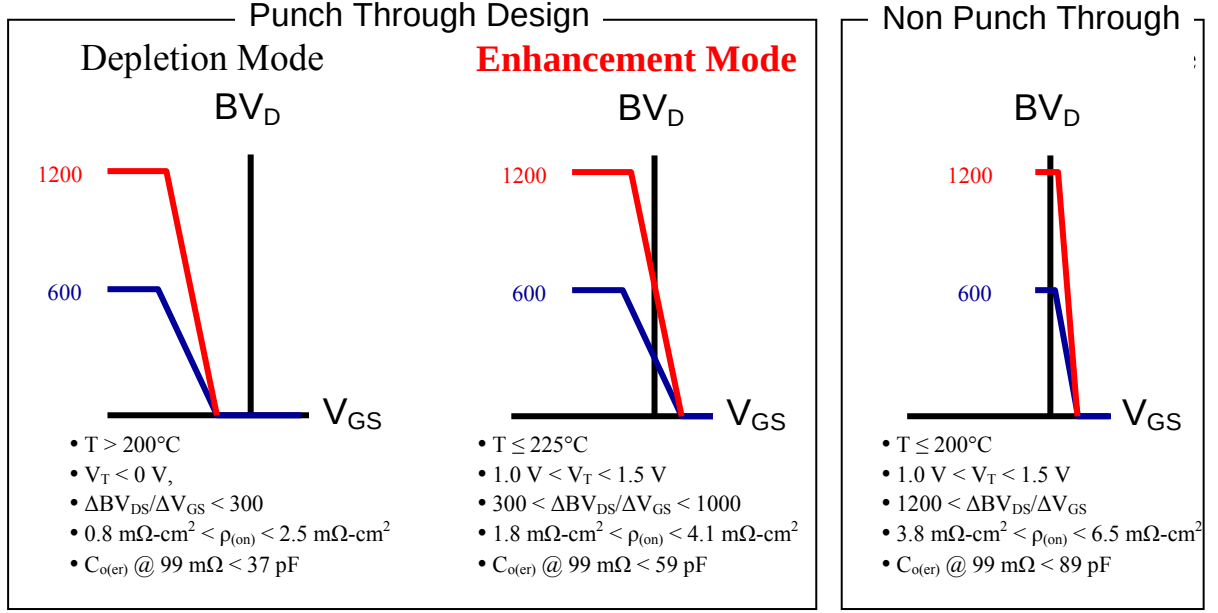


Figure 1: Comparison of the range of device types available in the standard VJFET design space.

2.2. Semi-analytical VJFET device simulator

For a relatively small drain-source bias V_{DS} , when self-heating effects could be neglected, the on-state I-V characteristics of a VJFET die could be approximated with the following non-linear equation:

$$V_{DS} = V_{CH}(V_{GS}, I_{DS}) + I_{DS} R_S \quad (2.1)$$

This series resistance (or “overhead” resistance) consists of the source contact ohmic resistance R_{Ohm_S} , drain contact ohmic resistance R_{Ohm_D} , drift resistance R_{Drift} , and substrate resistance R_{Sub} :

$$R_S = R_{Ohm_S} + R_{Ohm_D} + R_{Drift} + R_{sub} \quad (2.2)$$

When the self-heating effects are neglected, the series resistance of VJFET die R_S can be assumed independent on the current flowing through the structure. In other words, in the on-state, the VJFET die can be represented schematically as a set of resistive components connected in series as shown in Figure 2.

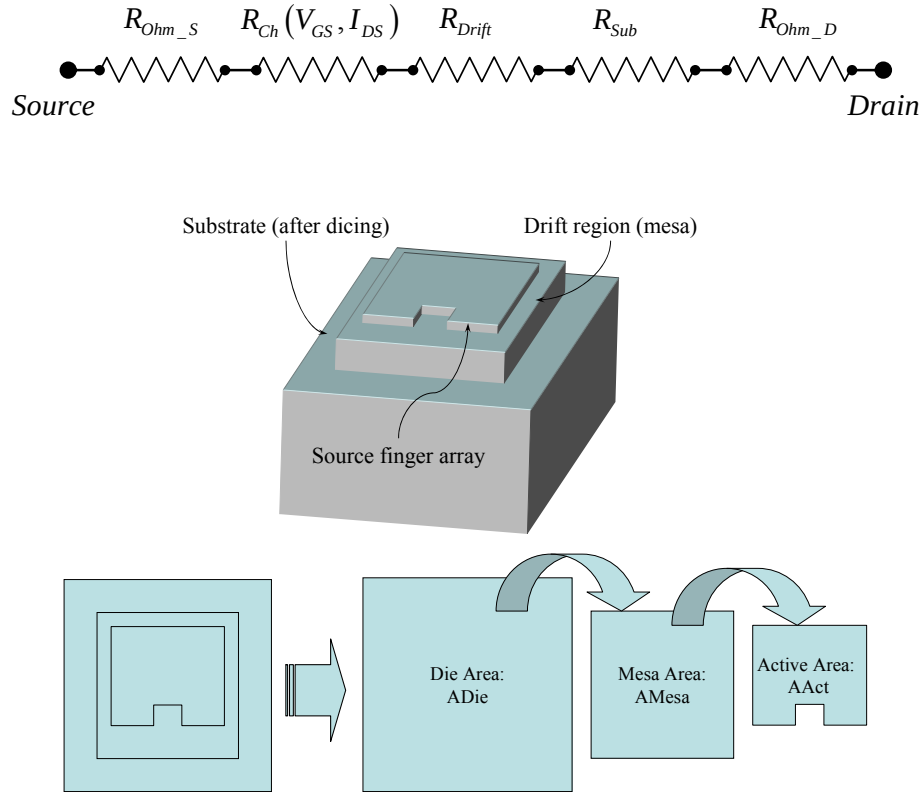


Figure 2: Simplified equivalent circuit of a VJFET at the on-state conditions and schematic view of a typical VJFET die.

The components of the series resistance introduced by the source and drain ohmic contacts could be determined using experimentally measured specific contact resistances and designed contact areas. The drift and substrate components can be calculated for a given ambient temperature using known thicknesses and doping concentrations of semiconductor layers as well as designed areas. The schematic isometric and aerial views of a typical VJFET die are shown in Figure 2. Current spreading through the extrinsic areas of the drift and substrate (outside the active area) can be approximated with the first-order of accuracy. The larger the die area (*i.e.*, the larger the ratio A_{Act}/A_{die}), the smaller the error introduced with such approximation.

The non-linear current dependence of the voltage drop on the channel region requires special investigation. The non-linear nature of the channel resistance is caused by the change of the depletion width along the implanted sidewall junctions and is further complicated by the non-linear geometry of the channel structure itself. Figure 2 shows a cross-sectional SEM image of a typical VJFET channel structure formed by dry etching and ion implantation. Light areas along the source finger sidewalls are p-type gate regions formed by aluminum implantation followed by the post-implant anneal.

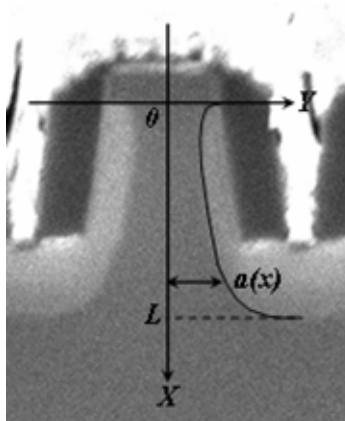


Figure 3: Typical cross-sectional SEM image of channel structures formed by dry etching and ion implantation.

The “textbook” JFET channel equation shown below

$$I_{ch} = \frac{q\mu N_{CH} W a_{ch}}{L} \left[V_{ch} - \frac{2}{3} \frac{\left[(V_{ch} + V_{bi} - V_{GS})^{\frac{2}{3}} - (V_{bi} - V_{GS})^{\frac{2}{3}} \right]}{\sqrt{\frac{qN_{ch} a_{ch}}{2\epsilon}}} \right] \quad (2.3)$$

was originally derived integrating expression for the potential drop along the channel axis

$$dU = \frac{I_{ch}}{2} dR = \frac{I_{ch}}{Wq\mu N_{ch} \left[a_{ch} - \sqrt{\frac{2\epsilon [U(x) + V_{bi} - V_{GS}]}{qN_{ch}}} \right]} dx, \quad (2.4)$$

assuming that mobility μ , doping N_{ch} , and the channel half-width a_{ch} are constant along the channel axis. W in (2.3) and (2.4) stands for the channel width (*i.e.*, total channel periphery). Moreover, the expression (2.3) does not account for the mobility dependence on the channel doping and its degradation toward implanted junction caused by implantation damage. Equation (2.3) also neglects drift velocity saturation at high electric fields. All of the above makes the equation (2.3) difficult to use, especially in the case of normally-off VJFETs, where the current saturation at low V_{DS} becomes a serious problem. In order to eliminate the limitations of the classical model, a simple algorithm was implemented in MATLAB that numerically solves the following system of non-linear equations:

$$\begin{cases} V_{ch} = I_{ch} \int_0^L \rho(x) dx \\ \rho(x) = Wq\mu_{ch}(I_{ch}\rho(x))N_{ch}(x) \left[a_{ch}(x) - \sqrt{\frac{2\epsilon[U(x) + V_{bi} - V_{GS}]}{qN_{ch}(x)}} \right] \\ V_{ch} = V_{DS} - I_{ch}R_S \end{cases} \quad (2.5)$$

where VJFET series resistance R_S is taken from (2.2), and $U(x)$ stands for the axial distribution of the electrostatic potential along the channel. Mobility “Effective” values for the mobility and doping μ_{ch} and N_{ch} are calculated assuming degradation of the channel parameters toward implanted sidewall junctions caused by the sidewall implantation damage. In the proposed model, the influence of such damage is accounted with the degradation coefficient calculated using normal probability distribution function (2.6):

$$y = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \quad (2.6)$$

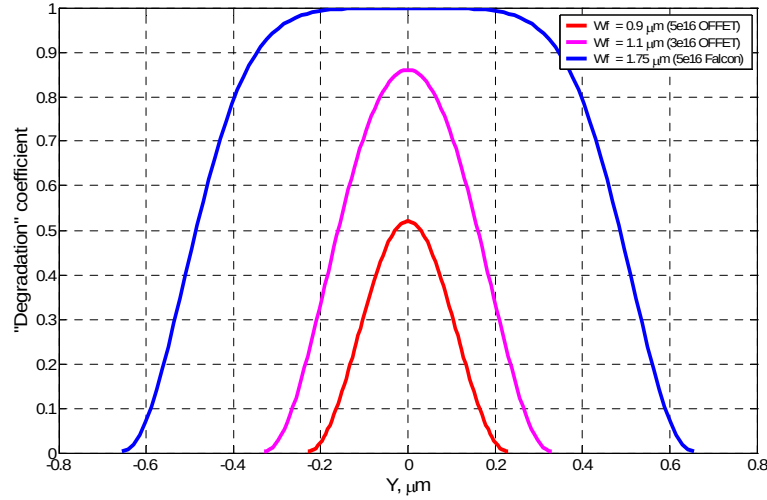


Figure 4: Degradation coefficients across the channels of different widths calculated for the same depth of implanted junction (0.2 μm) and the same characteristic length of distribution function (0.36 μm).

The comparison of the degradation coefficients across the channels with different widths calculated for the same depth of the implanted junction ($0.2\text{ }\mu\text{m}$) and the same characteristic length of the distribution function ($\sigma=0.36\text{ }\mu\text{m}$) is shown in Figure 4. This comparison illustrates that the impact of the sidewall implantation damage becomes very significant for the narrow fingers if the same implantation schedule is used to form gate regions.

The models described above were used to compile a convenient semi-analytical tool for a quick analysis of VJFET structures for a wide range of applications. Technology-related parameters such as sidewall junction depth and characteristic length of degradation function were found empirically to fit simulated characteristics to the measured data. Typical output screen shown in Figure 5 provides a set of drain family of curves, transfer characteristics, pie-chart showing relative contributions of different components of on-resistance, and input parameters and assumptions used in the simulation.

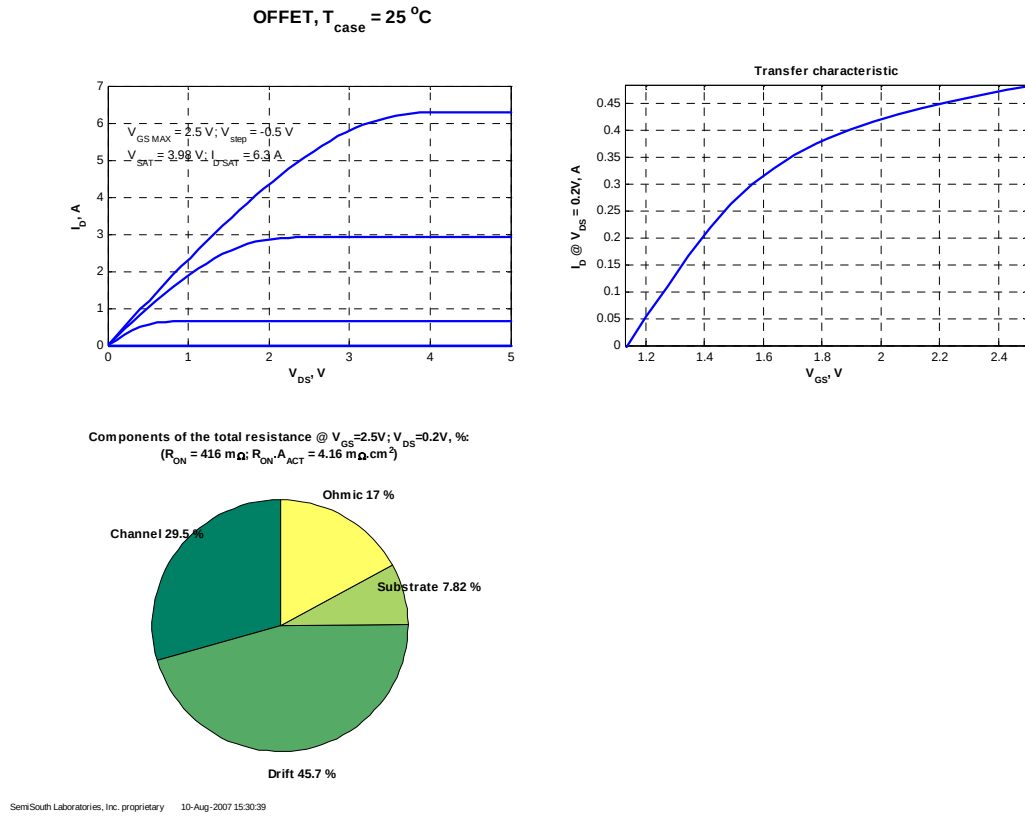
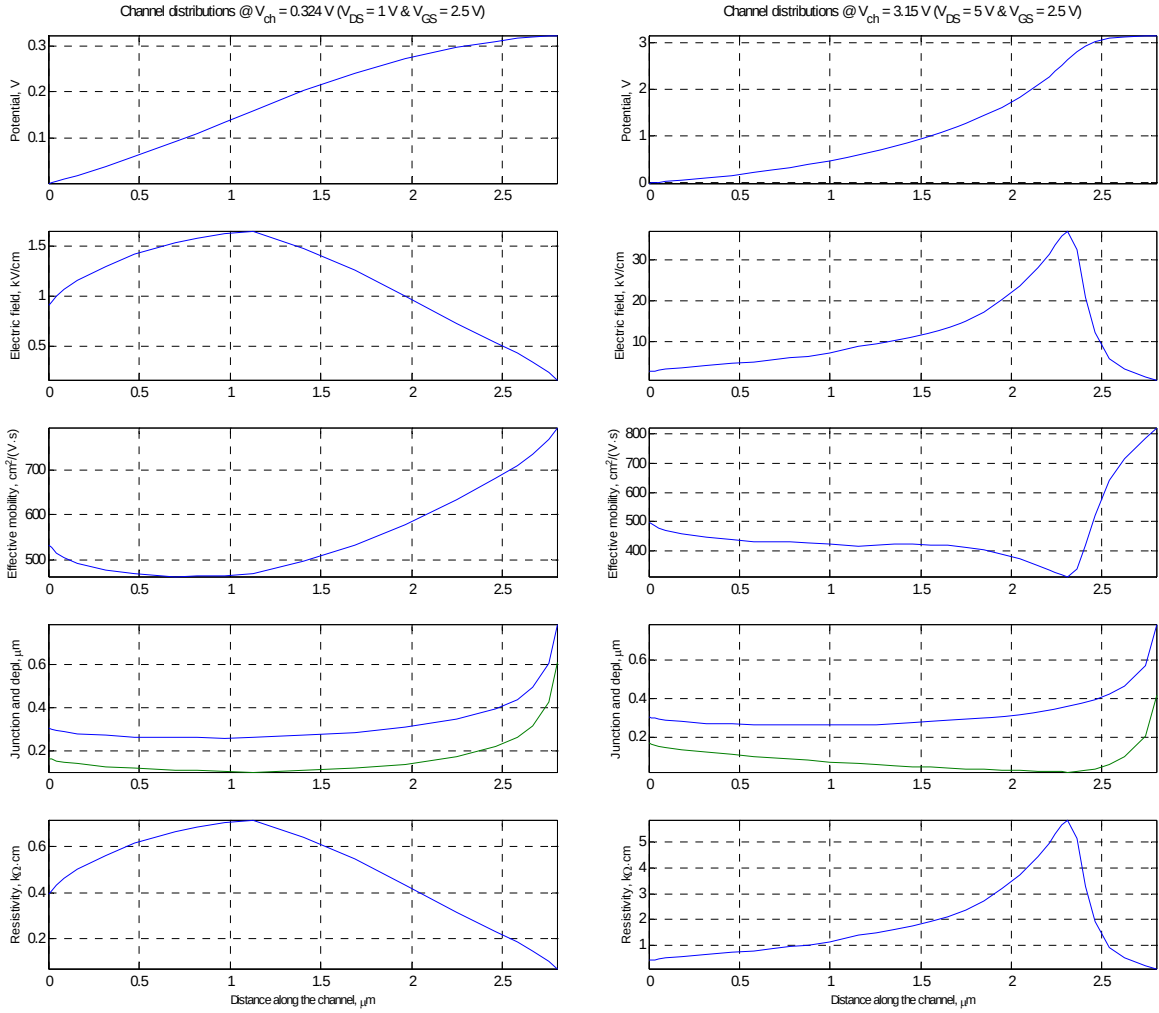


Figure 5: Typical output screen of a semi-analytical VJFET device simulator

The axial distributions of electrostatic potential and electric field, as well as the effective electron mobility, shape of depletion region and channel resistivity can be monitored along the vertical JFET channel for better understanding of physical processes that happen inside the channel at different bias conditions. Channel distributions for the device from Figure 5 simulated in linear region at $V_{DS} = 1\text{ V}$ and in deep saturation at $V_{DS} = 5\text{ V}$ are shown in Figure 6 (a) and Figure 6 (b), correspondently.



a)

b)

Figure 6: Channel distributions for the device from Figure 5 simulated in linear region at $V_{DS} = 1 \text{ V}$ (a) and in deep saturation at $V_{DS} = 5 \text{ V}$ (b).

Figure 7 shows measured and calculated drain characteristics of a packaged transistor superimposed on the same plot. It can be noticed from Figure 7, that the proposed semi-analytical model does not account for the effective channel length reduction caused by growing drain potential. As a result of that, slight increase of the drain current in the

saturation region shown by the actual measurements cannot be modeled at the present time. Despite certain limitations imposed by 1-D nature of the model and the fact that self-heating mechanism is not accounted, the described semi-analytical tool provides sufficient accuracy of simulations as shown in Figure 7.

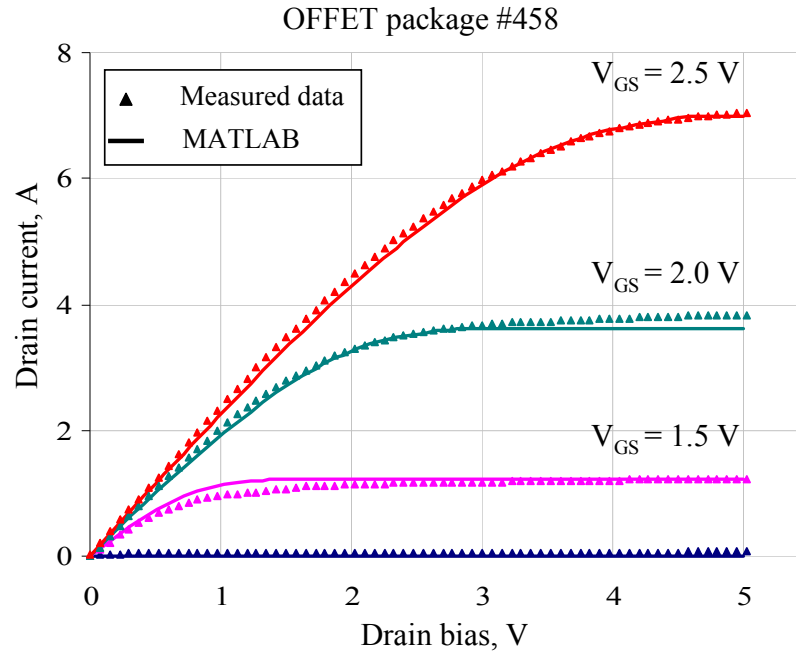


Figure 7: Superimposed measured and calculated characteristics of a packaged normally-off VJFET die.

2.3. Device Lots

2.3.1. 600V Lot A:

Objective: Lot A has been designed as a vehicle for a thorough investigation of the design space including the major design variables of source finger width, channel doping, channel length, and channel pitch. Using 2 wafers per split, we intend to derive the design trade-offs for both PT/ NPT and enhancement mode (EM) and depletion mode (DM) VJFET designs applicable for 600-1200V class devices.

The 8 wafers to be used in this engineering test lot have been identified and the epitaxy has been ordered as described in Table 1.

Table 1: Engineering Design Lot 1 Epitaxy Specifications

Split	# Wafers	Source Cap	Channel	Drift
1	2	0.5 μm / >1E19	2.0 μm / 1E16	5.0 μm / 1E16
2	2	0.5 μm / >1E19	2.5 μm / 3e16	5.0 μm / 1E16
3	2	0.5 μm / >1E19	3.0 μm / 3E16	5.0 μm / 1E16
4	2	0.5 μm / >1E19	3.0 μm / 5E16	5.0 μm / 1E16

Each wafer has a device split containing 4 different finger widths to enable a full channel design verification. Each device layout (Figure 8) is contained in a 4 device unit cell repeated over the entire wafer to ensure equal distribution of designs and limited the effects of lithography and material variation.

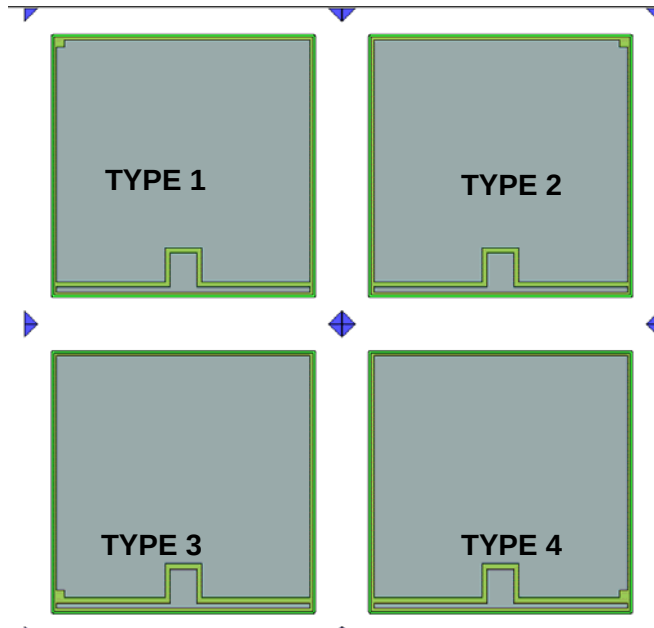


Figure 8: Layout of the four production die designs.

In addition to the production die, test die are selectively distributed across the wafer and contain a wide range of small test VJFETs to systematically study effects of trench width and finger spacing on threshold voltage, blocking gain, and manufacturing issues such as planarization efficiency. Other standard manufacturing SPC and process control monitors (TLM, resistors, alignment marks) are also included (Figure 9).

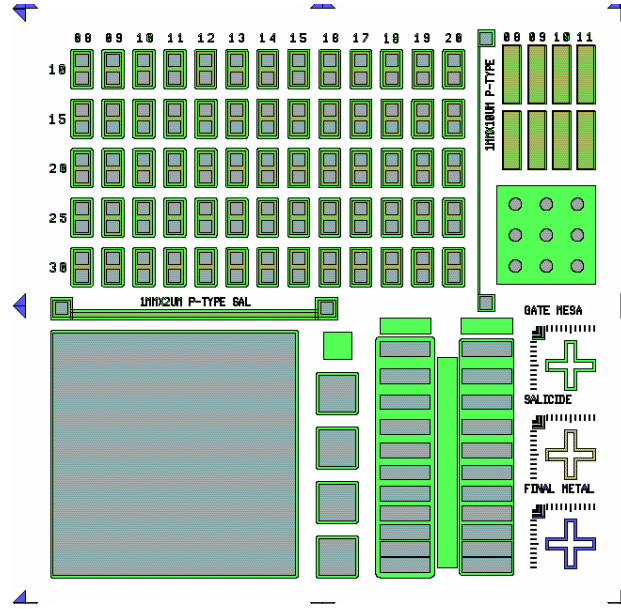


Figure 9: Test die layout.

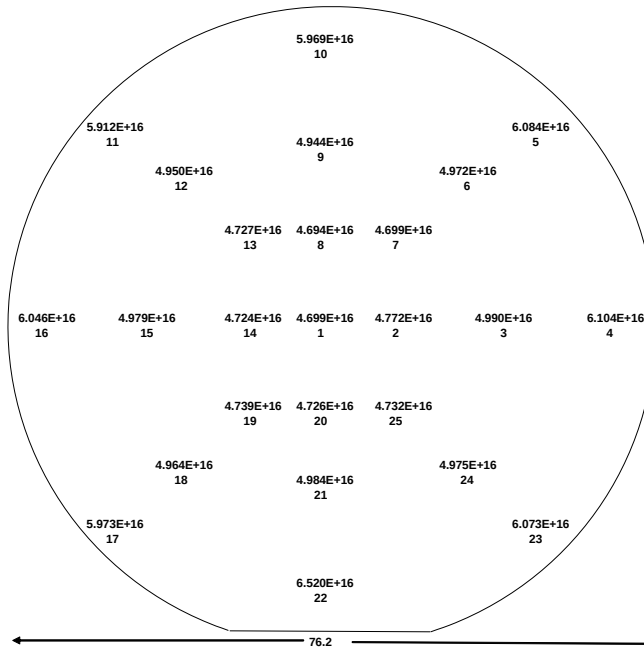


Figure 10: 25 point CV doping map of the VJFET channel epi.

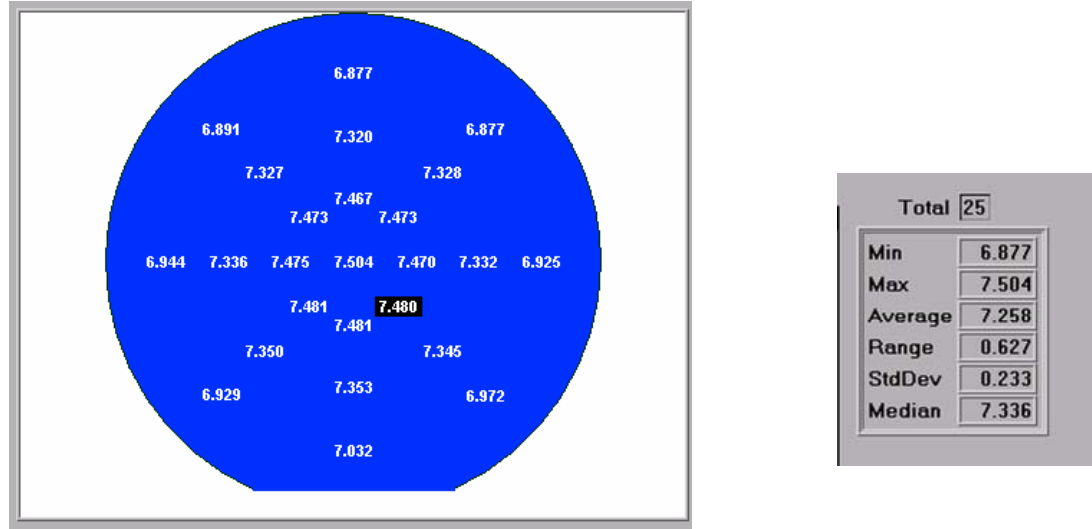
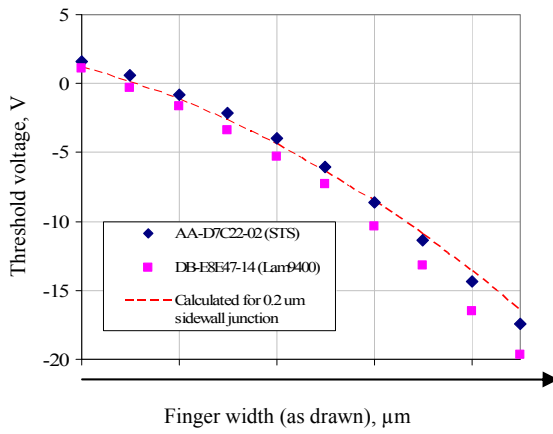


Figure 11: FTIR Thickness profile of the channel and drift epitaxy for the wafer shown in Figure 10.

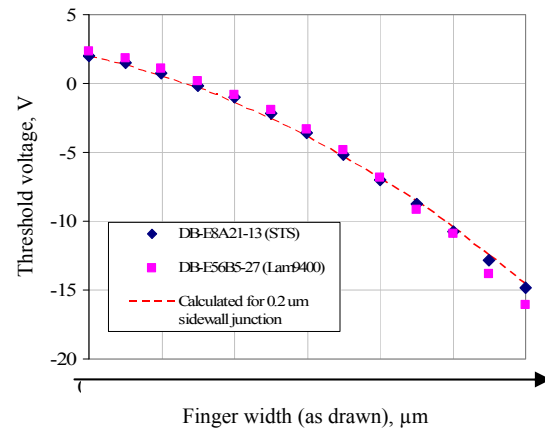
Inline Measurements

After ohmic contact formation, threshold voltage was measured on the arrays of test VJFETs with 140 μm channel periphery. Figure 12 compares the measured and predicted theoretical dependence of threshold voltage on the channel doping and finger width for the devices with source fingers etched in different tools. Theoretical values of the threshold voltage were calculated with the assumption that the depth of sidewall implanted junctions is equal to 0.2 μm . The measured values are the *average* threshold values measured on the devices with the same finger width and the trench widths of 1 μm , 1.5 μm , 2 μm , 2.5 μm , and 3 μm . It can be noticed from Figure 13, that the devices received a source finger etch exhibit threshold voltage closer to theoretically predicted value than devices etched in the second etch too. The systematic behavioral difference between the measured and calculated VTH characteristics (when source finger width increases, the measured VTH goes to more negative values faster

than the theoretically predicted) can be also noticed. One of the possible causes of the difference could be that the theoretical VTH was calculated with the assumption that the channel doping is constant between the junctions. This assumption is not accurate because the p-type implantation tail compensates n-type doping inside the channel along the sidewall junctions.



(a)



(b)

Figure 12: Comparison of the measured and theoretical values of threshold voltage as a function of source finger width for (a) 2 μm , $5\text{e}16 \text{ cm}^{-3}$ channel, and (b) 3 μm , $3\text{e}16 \text{ cm}^{-3}$ channel. Calculations were done for RT conditions.

Threshold voltage measurements on the wafers with 3 μm , $7\text{e}16$ channel were taken also.

These measurements resulted in very inconsistent data as shown in Figure 13.

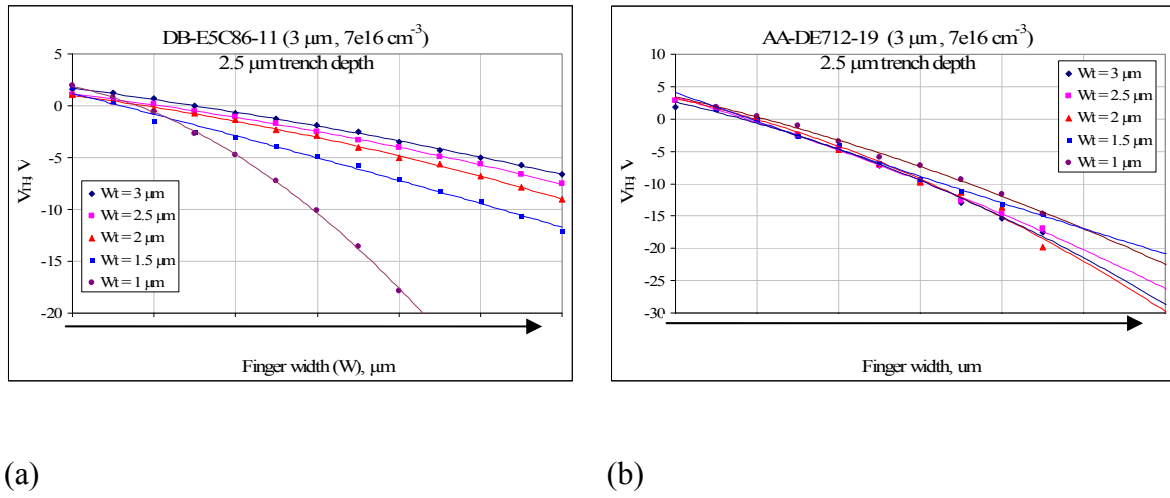
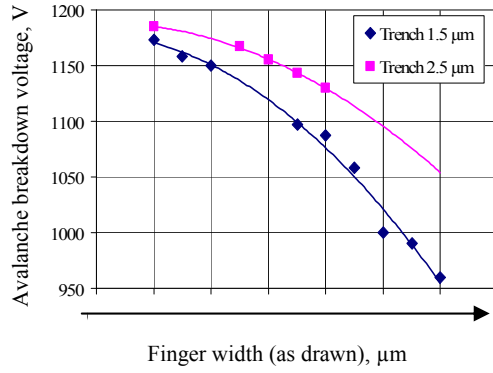
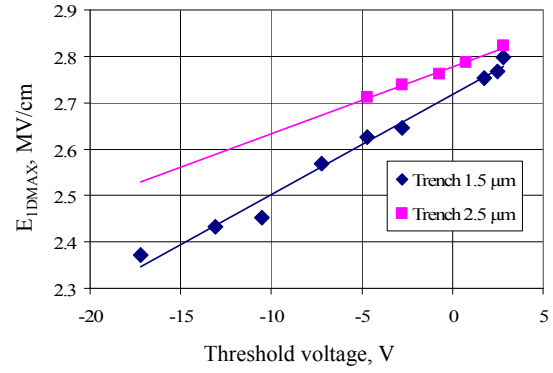


Figure 13: Threshold voltage measurements on the wafers with $7 \times 10^{16} \text{ cm}^{-3}$ channel doping and source fingers etched in Lam9400 (a) and STS (b)

Dependence of the avalanche gate-drain diode breakdown voltage on the channel structure geometry was measured on the substrate with 3×10^{16} channel doping etched in Lam9400. The results of these measurements done in Fluorinert using a Tektronix curve-tracer are shown in Figure 14 (a). The measured dependencies are consistent with the theoretical predictions. It can be noticed from Figure 14 (a), the curves corresponding to the different trench widths tend to merge at smaller finger widths as they go to ideal plane implanted junction. The wider the finger, the more pronounced become junction singularities at the channel entrances resulting in more significant field enhancement that ultimately leads to avalanche breakdown. The wider the trench, the larger becomes the radii of the gate junction “cylinders,” resulting in smaller field enhancements and, correspondently, higher breakdown voltages. Interestingly, when plotted in terms of the maximum 1-D electric field and threshold voltages, even despite the incomplete data, these dependencies show convincingly linear behavior as shown in Figure 14 (b).



(a)



(b)

Figure 14: (a) Measured dependence of avalanche breakdown voltage on the source finger width and gate trench width, and (b) dependence of the calculated maximum 1-D electric field on the threshold voltage for different gate trench widths.

Figure 15 shows the output characteristics from the wafer with the best measured on-resistance. These enhancement mode parts show an exceptionally low $0.168\Omega\text{-mm}^2$ on-resistance at 3V V_{gs} . The blocking gain and breakdown measurements for the same device is shown in Figure 16, demonstrating the first non-punch through designs with avalanche at 900V while maintaining a full enhancement mode functionality at 500uA drain leakage. This drain leakage is higher than seen for other devices, and should not be a limitation of the particular design. Further measurements on other wafers have shown high blocking gain while maintaining low drain-source leakage.

Die area: 1.44 mm²; Mesa area: 1 mm²; Source pad area: 0.864 mm²

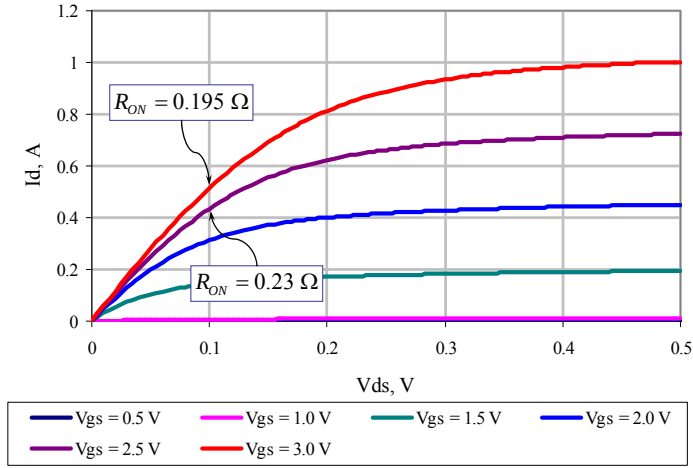


Figure 15: 800V Enhancement mode VJFET output characteristics showing low 0.168Ω-mm² on-resistance at 3V V_{gs} .

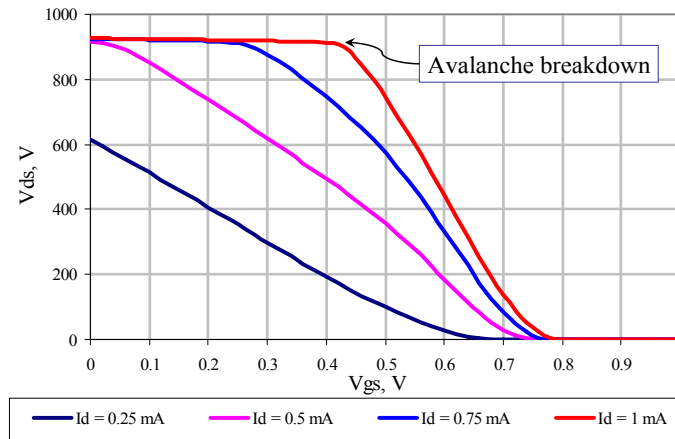
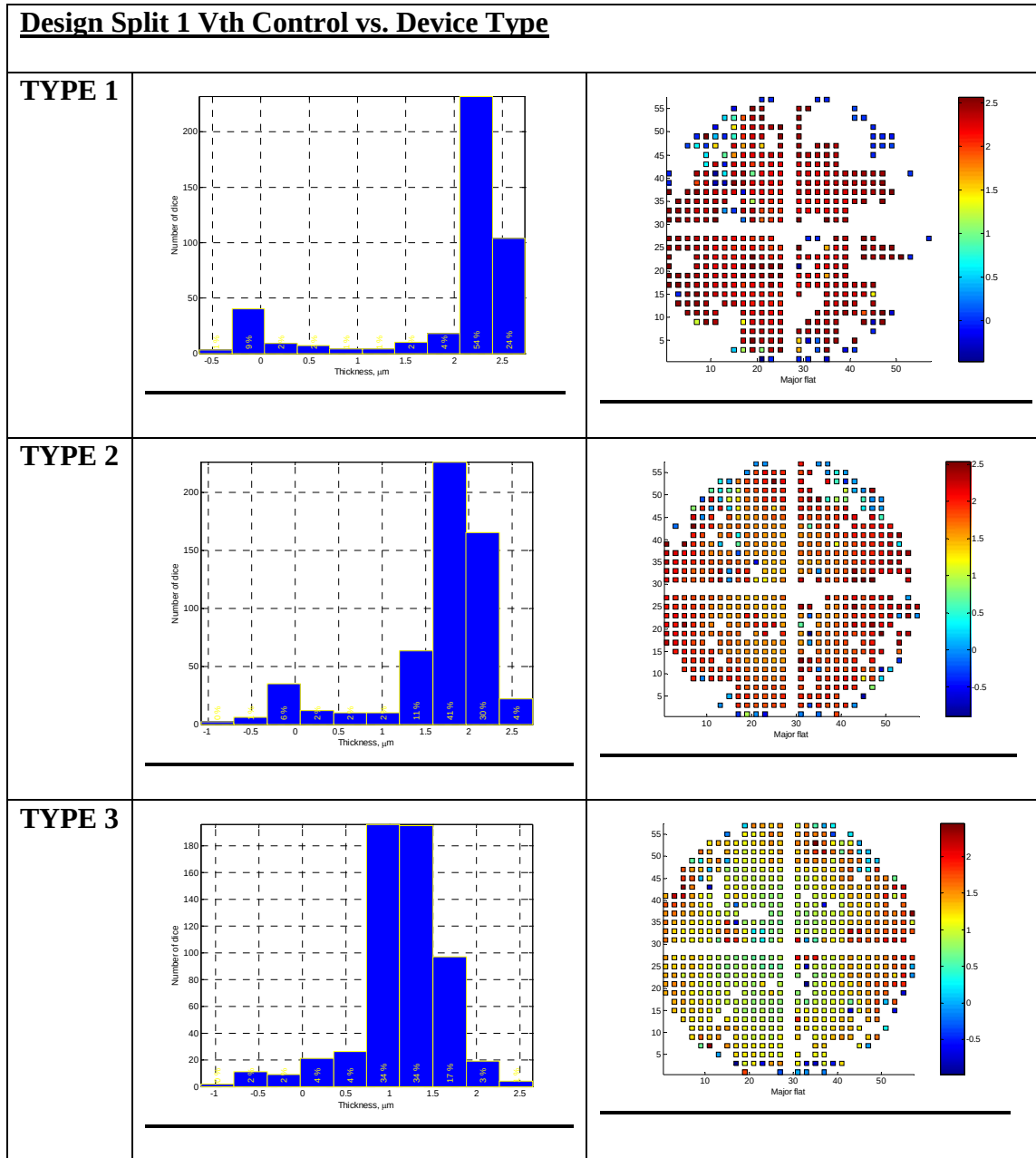


Figure 16: 800V Enhancement mode VJFET blocking gain characteristics for different drain leakage currents.

Post processing, final wafers were tested on an automatic production test system. Figures 17 and 18 show wafer maps and histograms of threshold voltage variation over 2 different wafers with significantly different epitaxy channel designs. Both designs have a standard

deviation of $\sim 0.5V$, which is caused by both lithography variations from process and wafer defects as well as epitaxy doping variation.



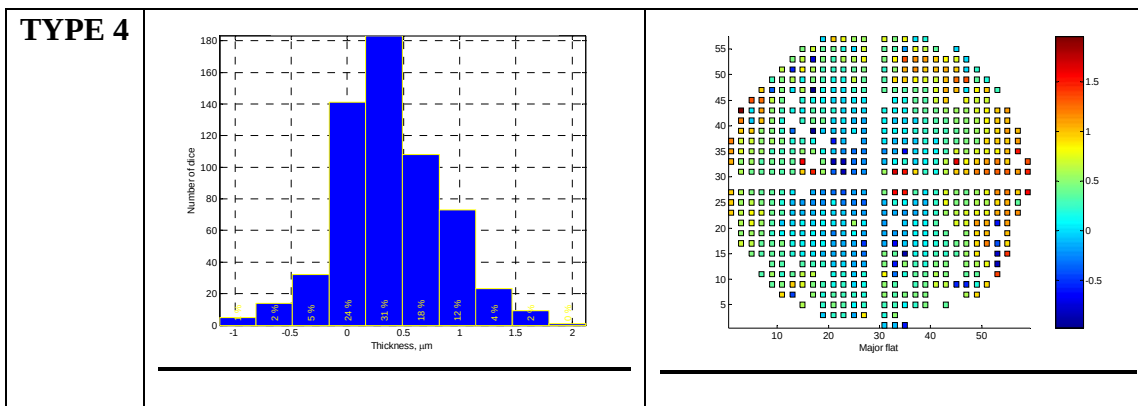
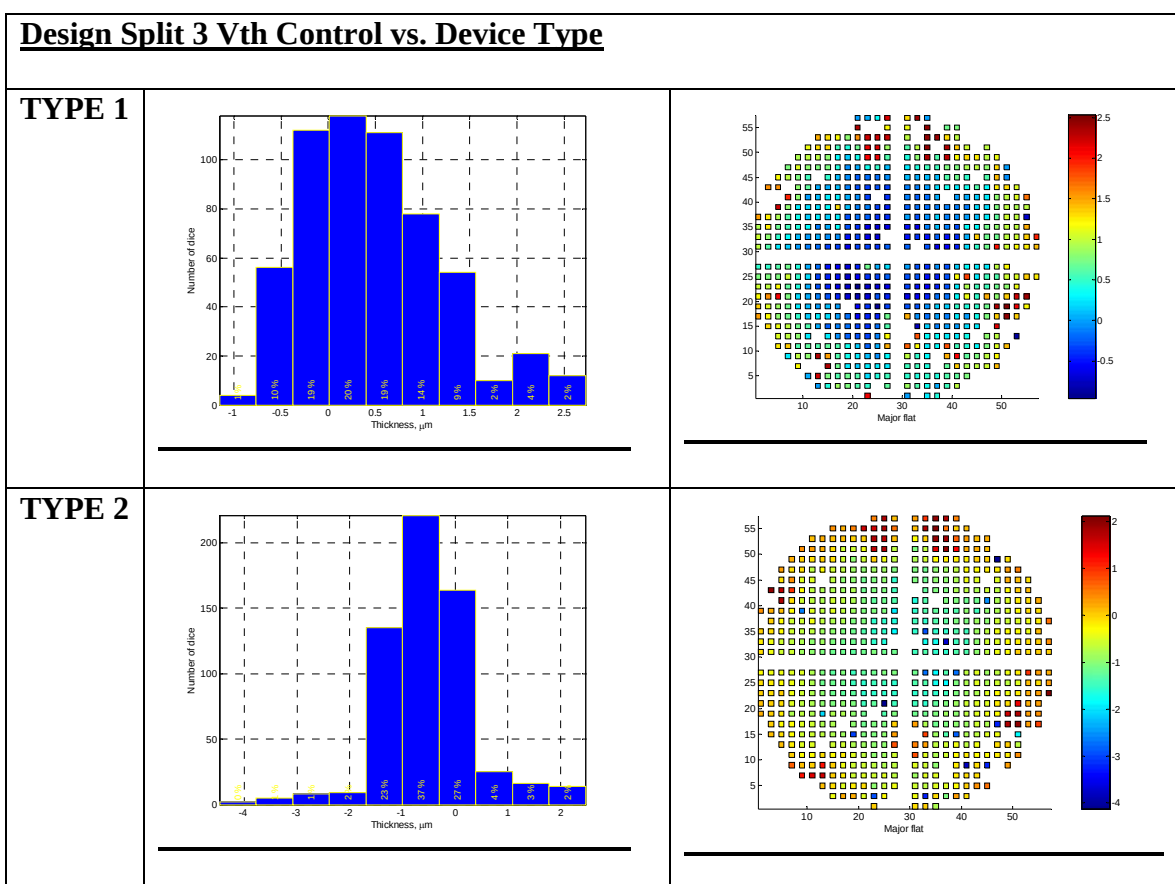


Figure 17: Vth variation from Design split 1 for the 4 different device types on the wafer.



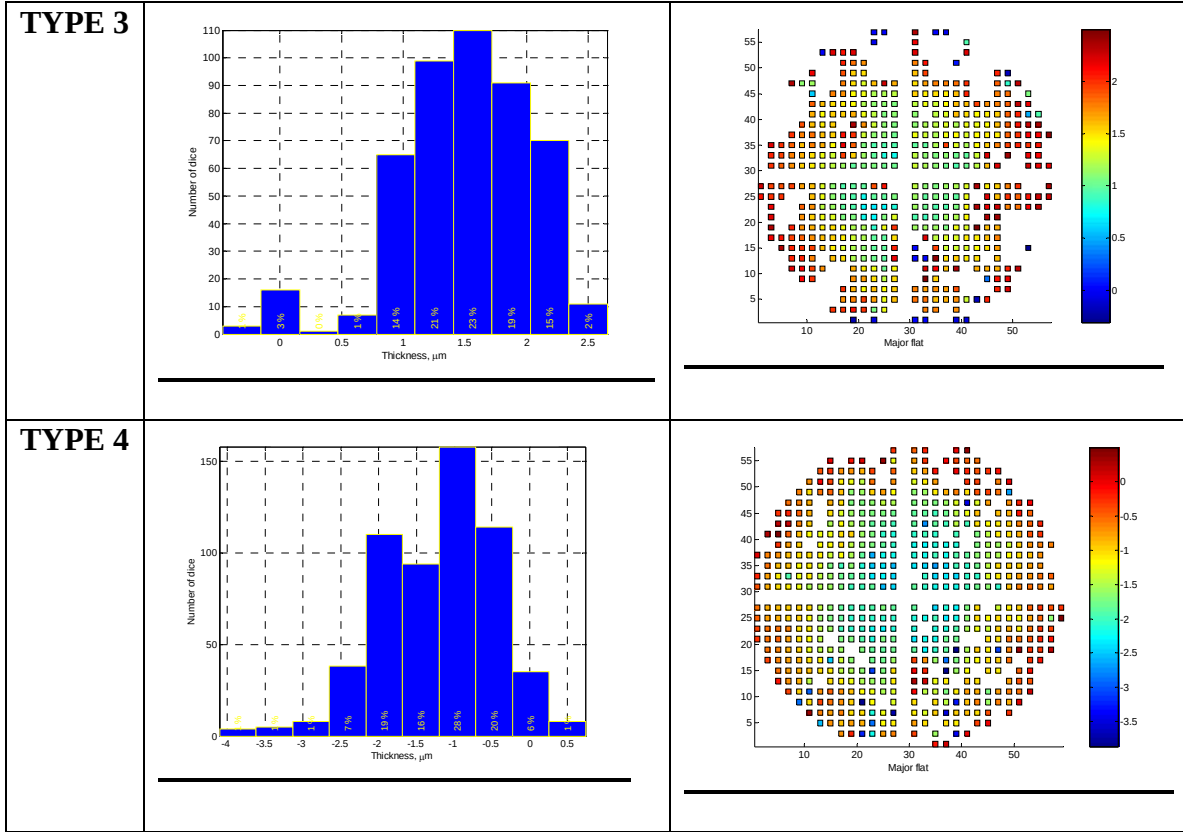


Figure 18: Vth variation from Design split 3 for the 4 different device types on the wafer.

DC characteristics of the devices packaged in TO-257 packages were measured at ambient temperatures ranging from 20°C to 200°C. Drain families of curves are shown in Figure 19, and the temperature dependencies of the threshold voltage and the gate leakage current, as well as the blocking characteristics are shown in Figure 20. The on-resistance normalized to the active area (source pad area) measured at $V_{DS}=1$ V and $V_{GS}=2.5$ V did not exceed $2.9 \text{ m}\Omega\cdot\text{cm}^2$ and $6.6 \text{ m}\Omega\cdot\text{cm}^2$ at RT and 200°C, respectively. Fabricated devices exhibited stable 900 V avalanche breakdown measured from RT to 200°C. The on-state saturation current measured at $V_{DS}=3$ V and $V_{GS}=2.5$ V was equal to 4 A and 2.3 A at RT and 200°C

respectively. The threshold voltage shift with temperature showed linear behavior and did not exceed 1.8 mV/°C from 25°C to 200°C. The gate leakage current measured at $V_{GS}=2.5$ V exhibited rather parabolic dependence on the temperature when growing by two orders of magnitude from 0.5 mA at 25°C to 50 mA at 200°C. The summary of the DC characteristics measured at 25°C, 100°C, 150°C, and 200°C is given in Table 2.

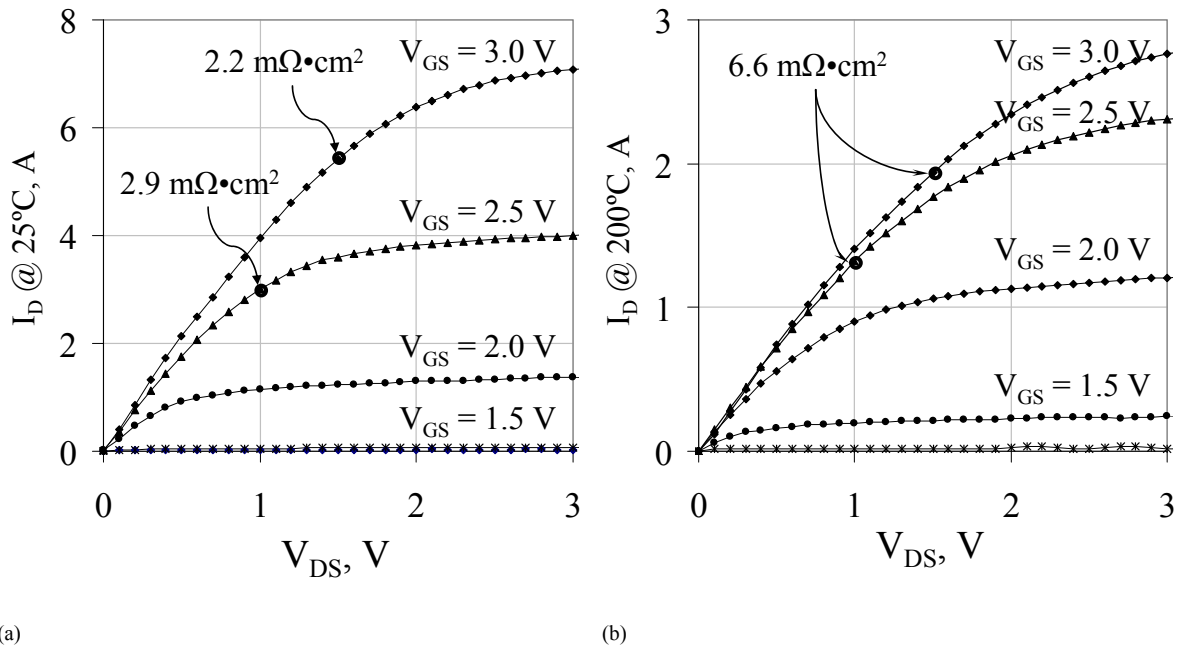


Figure 19: Drain families of curves measured on 800 V VJFET at room temperature (a) and at 200°C (b).

Unfortunately, the overall yield on these wafers were poor due to a tooling issue that caused a random defect generation in the gate pad area that resulted in poor breakdown characteristics.

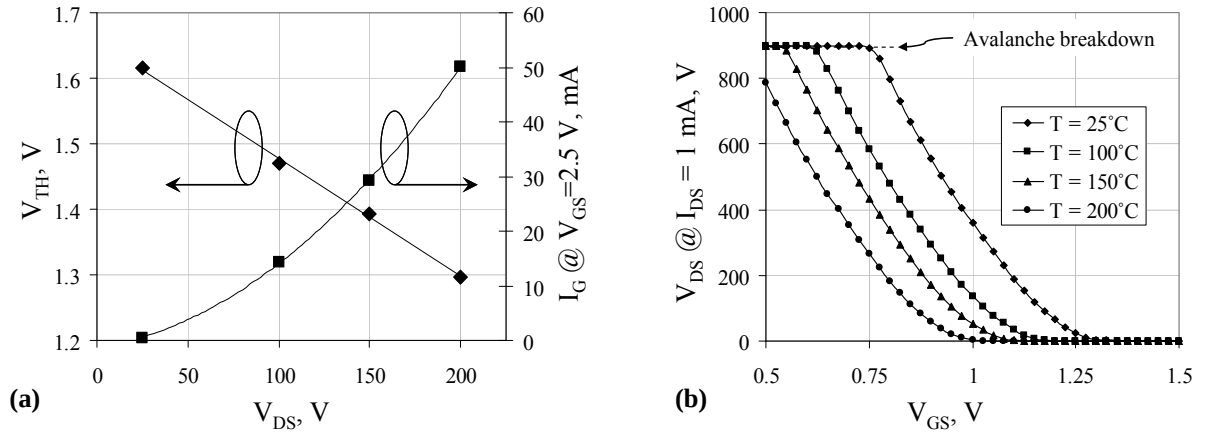


Figure 20: Temperature characteristics of threshold voltage and gate leakage (a), and blocking characteristics (b).

Table 2: DC summary of typical device from Lot A.

	R_{ON-SP} @ $V_{DS} = 1$ V, $m\Omega \cdot cm^2$				I_{DSS} @ $V_{DS}=3$ V, A		Gate leakage, mA	
	Normalized to die area (1.44 mm ²)		Normalized to source pad area (0.864 mm ²)					
T, °C	$V_{GS} = 3$ V	$V_{GS}=2.5$ V	$V_{GS} = 3$ V	$V_{GS} = 2.5$ V	$V_{GS} = 3$ V	$V_{GS} = 2.5$ V	$V_{GS} = 3$ V	$V_{GS} = 2.5$ V
25	3.65	4.79	2.19	2.87	7.09	4.01	65	0.52
100	5.68	6.54	3.41	3.93	4.89	3.40	133	14.3
150	7.69	8.42	4.62	5.05	3.68	2.88	153	29.2
200	10.25	10.91	6.15	6.55	2.76	2.31	253	50.1

2.3.2. 600V Lot B:

Objective: This 5 wafer lot was intended to be a less aggressive design split to complement the 600V Lot A devices. These wafers have epitaxy profiles listed in Table 3.

Table 3: Engineering Design Lot 1 Epitaxy Specifications

Split	# Wafers	Source Cap	Channel	Drift
1	2	0.5 μm / >1E19	3.0 μm / 1E16	8.5 μm / 8E15
2	2	0.5 μm / >1E19	3.0 μm / 3e16	8.5 μm / 8E15
3	1	0.5 μm / >1E19	2.0 μm / 1E16	8.5 μm / 8E15

The lead two wafers received the new single Ni layer and single stage RTA ohmic process on both front and back sides as described later in this report. The initial results on 2 μm x 1mm gate silicide line measurement give a silicide sheet resistance of $R_s=10.82 \Omega/\text{sq}$. Ohmic contact resistance from in-line TLM measurements show acceptable 6.67m $\Omega\text{-cm}^2$. The remainder of the lot is in queue to receive the new single stage ohmic process.

During processing, several of the wafers were scrapped in the trailing lot. A single wafer was completed through fabrication and has been tested for on-wafer yield and electrical characteristics. The total yield was 28% for devices that could block a minimum of 600V at $V_{gs}=0\text{V}$, as shown in Figure 21. The total functional yield was much higher, with a blocking yield of 55%.

The threshold voltage distributions for this channel doping and width are shown in Figure 22. Each channel design had a good statistical distribution that when added to the other lots in this task, give a very comprehensive design space for further developing the normally-off transistors.

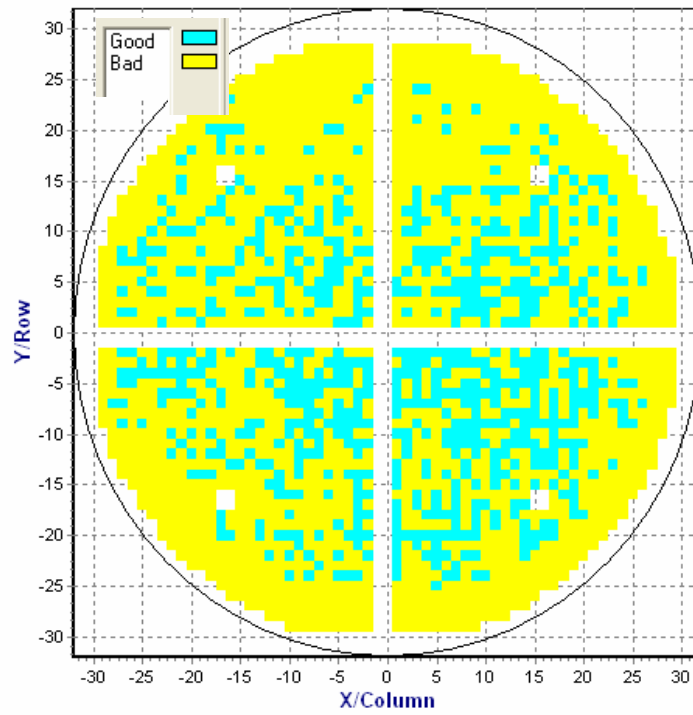


Figure 21: Wafer map of yielding devices with a minimum of 600V enhancement mode blocking capability at $V_{gs}=0V$.

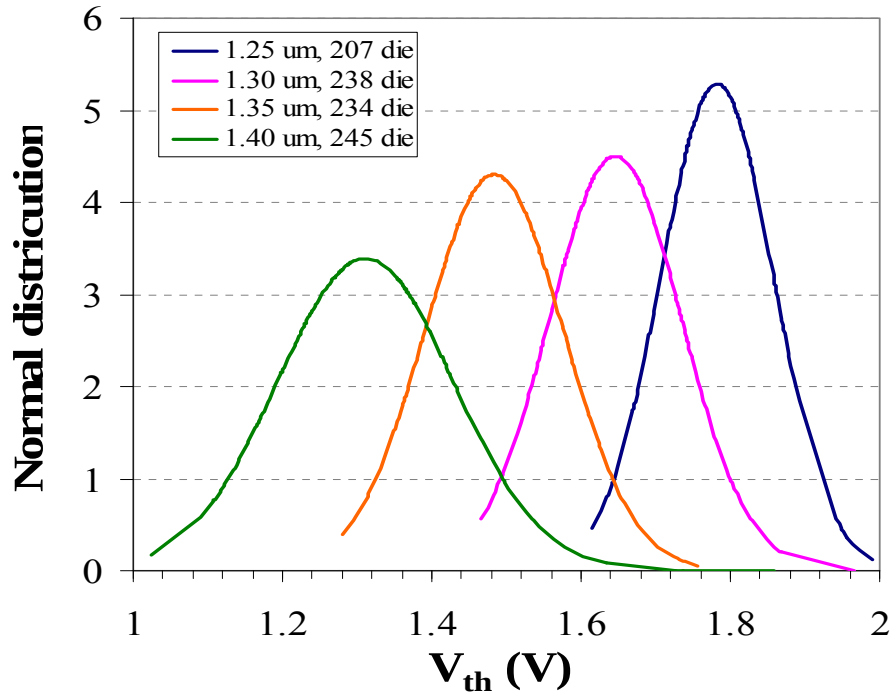


Figure 22: Distribution of threshold voltages for the 4 different device types from the 600V Lot B wafer.

2.3.3. 1200V Lot A

Objective: A second VJFET lot targeting a 600V blocking capability at $V_{gs}=0V$ and a full 1200V+ at $V_{gs}=-5V$ was designed and the epitaxy was been completed per the specifications for the epitaxy on this lot is given in Table 4. These wafers will use the same mask set at the 600V Lot A wafers.

Table 4: Engineering 1200V Lot A Epitaxy Specifications

Split	# Wafers	Source Cap	Channel	Drift
1	1	0.5 μm / >1E19	2.0 μm / 1E16	12.0 μm / 5E15
2	2	0.5 μm / >1E19	3.0 μm / 3E16	12.0 μm / 5E15
3	2	0.5 μm / >1E19	3.0 μm / 5E16	12.0 μm / 5E15

Status: All wafers from this lot have finished fabrication and were tested post final metal. Table 5 lists the wafer status, epi split, and complete functional yield. Since all wafers have on-wafer source finger width splits, the yielding die have thresholds ranging from complete depletion mode devices to full enhancement mode functionality.

Figure 23 shows a packaged device from wafer DB-10 with the heavier doped channel. Initial switching measurements were taken from wafer DB-10 on both enhancement and depletion mode devices. Figure 24 shows the switching waveforms for a strong enhancement mode device. This device was driven with 300V Vds and a gate drive from -4V to +2.5V and load current of $\sim 3A$. Under these conditions, the switching times were $t_r=720ns$, $t_f=22ns$, $t_{don}=25ns$, and $t_{doff}=28ns$. The rise-time was limited by the +2.5V positive gate drive, and would improve significantly if a larger gate swing was allowed for the initial charging period.

Table 5: Engineering 1200V Lot A Wafers

Wafer	Status	Channel	Drift	Yield
CF-17	Scrapped	2.0 μm / 1E16	12.0 μm / 5E15	Scrapped
CF-13	Complete	3.0 μm / 3E16	12.0 μm / 5E15	11%
CF-12	Complete	3.0 μm / 3E16	12.0 μm / 5E15	53.7%
DB-10	Complete	3.0 μm / 5E16	12.0 μm / 5E15	18.2%
DB-09	Complete	3.0 μm / 5E16	12.0 μm / 5E15	11%

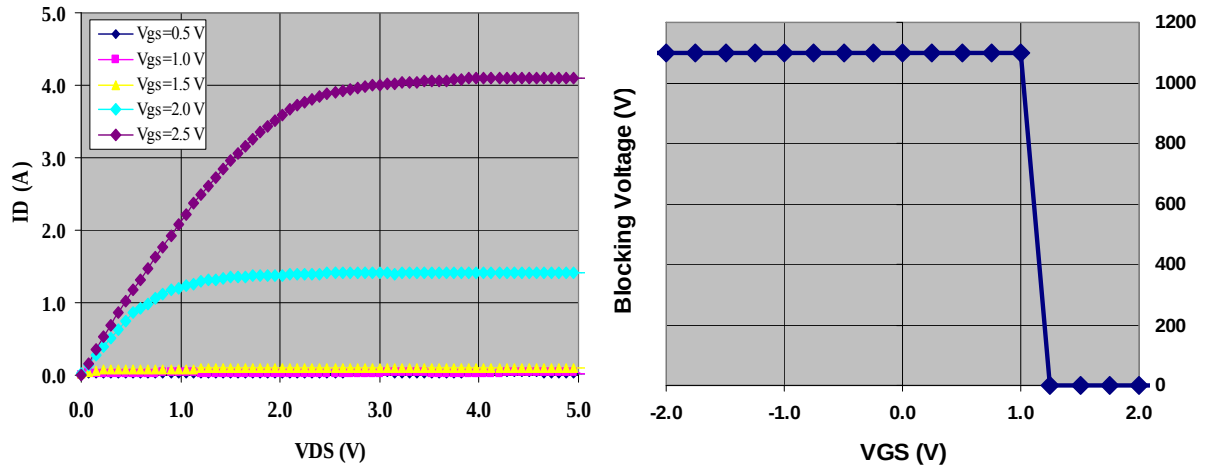


Figure 23: Packaged device from wafer DB-10, showing the output family of curves for a fully enhancement mode 1200V VJFET. $R_{ds(on),sp}$ is $< 3.9m\Omega\text{-cm}^2$ for this device.

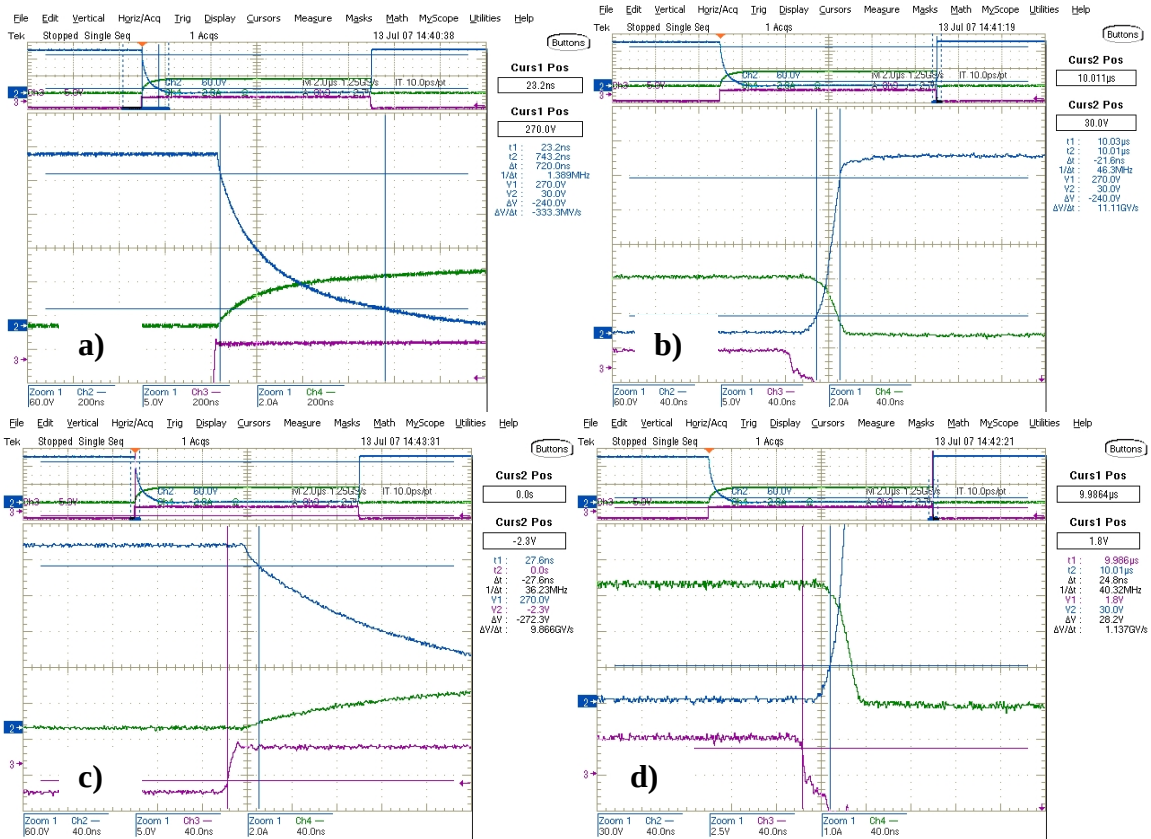


Figure 24: Switching waveforms for a packaged enhancement mode device from wafer DB-10; a) turn-on transient; b) turn-off measurement; c) turn-on delay measurement; d) turn-off delay measurement.

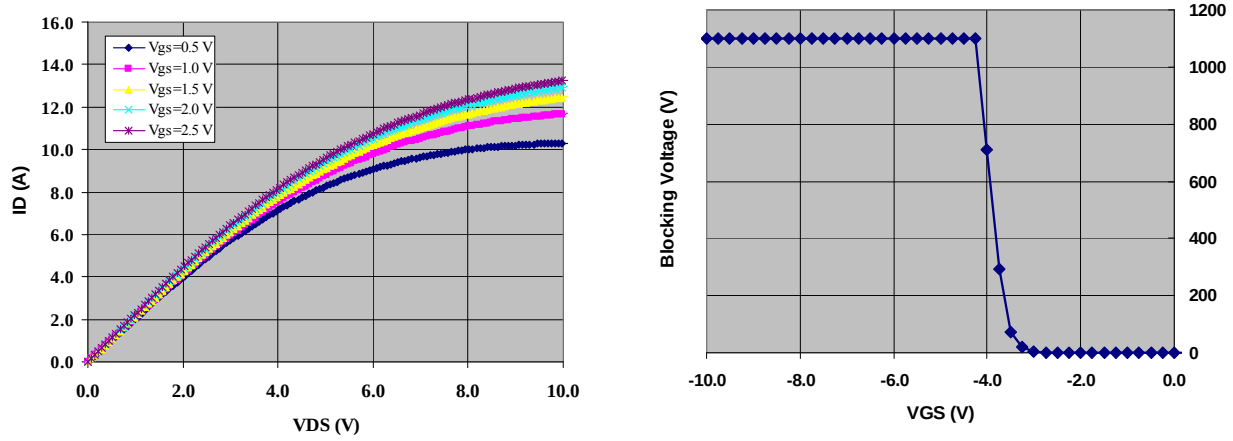


Figure 25: a) Forward output family and b) blocking gain curves for a normally-on depletion mode 1200V VJFET designed on the DB-10 wafer.

Fully depletion mode devices were also designed on all wafers. Figure 25 shows the forward characteristics of a depletion mode device with a V_{th} of ~ -2 V. Combined with the high blocking gain (Figure 25b) the aggressive channel design allows for complete control over the device with low 5V power rails, eliminating the need for exotic gate drives.

The device curves in Figure 26 are for one of the few large area (5mm^2) devices that were included in the layout. The device shows 1200V blocking and almost 30A at 5V V_{ds} . This is the largest enhancement mode device currently fabricated by Semisouth.

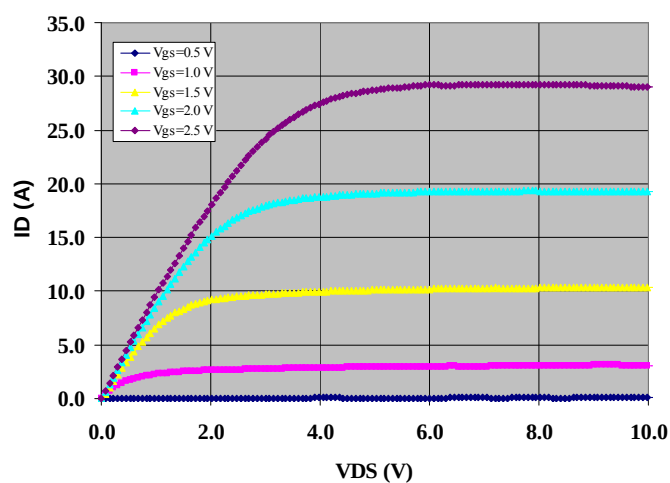


Figure 26: 5mm2 quasi-off VJFET from wafer CF-12. This device will block 600V at 0V and 1200V with -2.5V VGS.

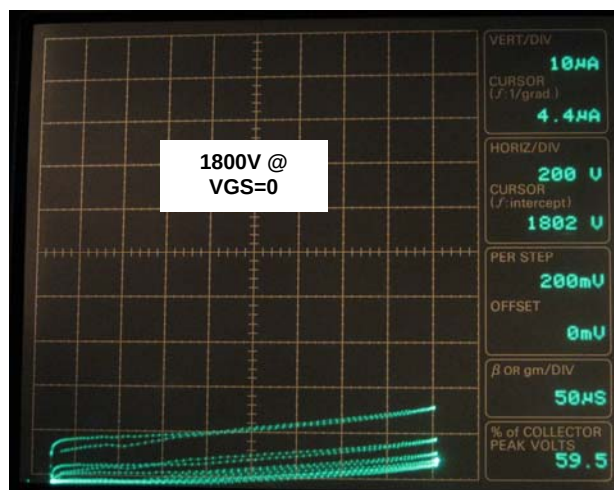


Figure 27: Curve tracer picture showing 1.8kV blocking capability at VGS=0V.

While the automatic engineering probe system is limited to 1100V, Figure 27 shows a screenshot of a Tektronics 371A curve tracer showing 1800V blocking capability for an enhancement mode VJFET from this lot. This device had a threshold voltage closer to 1.5V and therefore could maintain blocking with this stronger channel design.

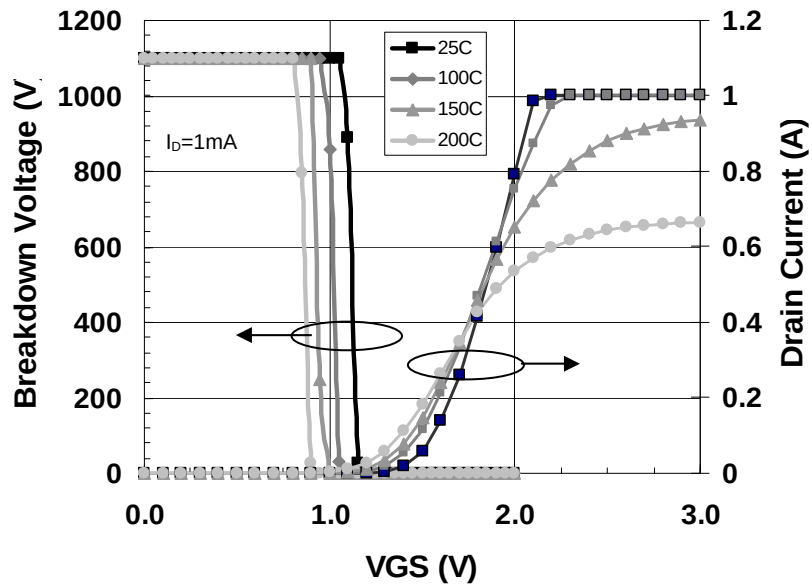


Figure 28: Blocking gain and threshold voltage curves vs. temperature for a 1200V device from Lot A.

High temperature performance was also measured for devices on this lot. The blocking gain and threshold voltage shift versus temperature is shown in Figure 28. This 1200V device had a RT threshold voltage of $\sim 1.4\text{V}$ and did not significantly change ($>1\text{V}$) at 200C. Similarly, the blocking gain was stable with temperature, able to block full 1200V at 200C with a leakage current less than 1mA.

2.3.4. 1200V Lot B

Objective: 1200V Lot B is a reproduction of the 1200V Lot A VJFET lot targeting a 600V blocking capability at $V_{gs}=0\text{V}$ and a full 1200V+ at $V_{gs}=-5\text{V}$. These wafers used the same mask set at the 1200V Lot A wafers and was intended to provide additional statistical design

information with a slightly higher electric field and drift doping. Table 6 lists the epitaxy specifications for this lot.

Table 6: Engineering 1200V Lot B Epitaxy Specifications

Split	# Wafers	Source Cap	Channel	Drift
1	6	0.5 μm / >1E19	3.0 μm / 1E16	10.0 μm / 6.5E15
2	6	0.5 μm / >1E19	3.0 μm / 3E16	10.0 μm / 6.5E15

Due to the scheduling of these lots, they were not started until the next delivery order was underway.

2.3.5. Diode Lot A [600V/1200V Diodes]

Objective: Companion Schottky diodes to the 600V and 1200V VJFETs have been designed for low leakage and high blocking capability. This lot will serve as a verification of the design and a foundation for the manufacturing process development. Table 7 details the epitaxy plan for both 600V and 1200V diodes. Both lots contains on-wafer splits of JBS channel design ranging from 3-5 μm in width, and having a total active area $\sim 1.5\text{mm}^2$.

Diode Lot A was processed through the edge termination and mesa etch modules, but suffered from the Ni mask degradation as a result of a etch rate drift in the ICP etch tool. At this point in the process, it is unclear how the degradation of the etch mask, and subsequent spurious etching into the active area will affect final device performance.

Table 7: Epitaxy Specifications for 600V/1200V JBS Diodes

Device	Drift	JBS Design	Channel Design
600V JBS	6 μm / 8E15	2.0 μm	2-5 μm
1200V JBS	10 μm / 8E15	2.0 μm	2-5 μm

Once the lot reached final test, the results from this lot were disappointing in terms of yield and specific on-resistance. From the 4 wafers, the best yield was 11%. The primary failure mechanism was GD leakage due to poor Schottky interface. It was determined that during the Schottky surface preparation and subsequent Schottky formation, a non-ideal processing step was inserted to reduce processing time. This step was the likely cause of the poor Schottky interface and the low yield on the wafers. Center patterns on most wafers showed the highest yield (Figure 29). A second diode lot B was planned to continue the effort on developing a Schottky diode process.

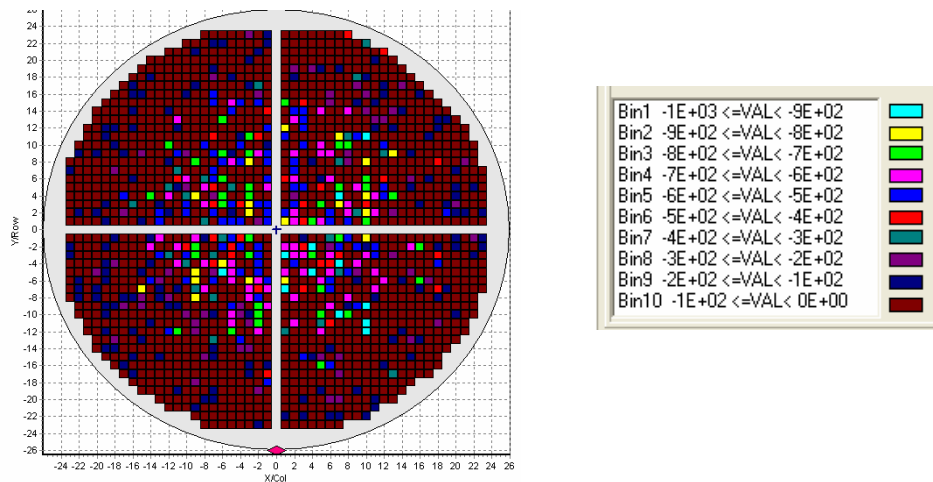


Figure 29: Wafermap of the blocking yield of 600V JBS diodes for Diode Lot A. The poor yield was identified as a misprocessing step during the Schottky contact formation.

2.3.6. Diode Lot B [1200V Diodes]

Objective: The Diode Lot B (Table 8) is intended to investigate aggressive new designs for JBS diodes with planar and etched channel regions. Simulations have shown that the addition of an etched channel (spreading) layer similar to the VJFET can both significantly reduce the electric field at the Schottky interface, and provide higher current density via reduced channel resistance and a resulting heavier doped drift region. Channel depth and width will be focused design variables in the JBS lot, as well as providing manufacturing statistics for larger area (3mm² active) JBS diodes.

Status: Diode lot B has progressed through the channel etch. Unfortunately, the new channel pattern caused some micromasking in the JBS p+ trench structure. As with the previous diode lot, it is unclear how these defects will affect final device performance since they do not appear in the active channel region. It was determined that this lot will continue processing through implantation and edge termination, unfortunately the micromasking prevented any results from this lot and a new lot for the next delivery order was planned.

Table 8: Epitaxy and Design Summary for 1200V JBS Diodes Lot B

Device	Drift	JBS Design	Channel Nd	Channel Y	Channel X
1200V JBS	9 μm /8E15	2.0 μm	2 μm /3E16	0 - 1 μm	2 μm -4 μm
1200V JBS	10 μm /7E15	2.0 μm	N/A	0 - 1 μm	1.5 μm -2.5 μm

3. TASK 2: PROCESS DEVELOPMENT

Process development tasks were targeted in several main areas including:

1. Source finger pattern, definition, and etch.
2. Edge termination definition and etch.
3. Frontside and backside Ohmic contact formation.

4. Gate isolation (planarization) process prior to final metal.

Each area was investigated and optimization tasks were performed to fabricate the devices reviewed in this report.

4. TASK 3: PRODUCIBILITY DEMONSTRATION

Lot 10 was the first producibility lot under Task 3. All wafers have been completed and tested with typical electrical parameters given in Table 9. Unfortunately, due to issues with the outsourced vendor, the planarization processing was a major cause of delay and yield loss. Although the aggressive design of a 3mm^2 device was expected to have a low percentage of yielding devices, we believe that the yield percentages could have been significantly higher if not for the poor processing.

Of the 6 wafers in the lot, only 3 could be used for working parts. Of those three wafers, the parts have been sorted in to groups, $BV > 600\text{ V}$ (43 devices) and $400 < BV < 600$ (100 devcies). We have diced and separated all of the 143 parts into gel-packs and are ready for assembly. A few devices were selected and packaged for post-dice testing with typical characteristics of yielding devices shown in Figures 30 and 31.

Table 9: Typical Measured Values of Packaged 3mm^2 Lot 10 VJFETs

Parameter	Typical Values	Conditions
V_p	-5V to -12V	V _{ds} = 1V
R_{on(sp)}	2.5 mΩ.cm ²	V _{gs} = 3V
I_{dss}	40A to 55A	V _{ds} = 10V
I_{Gs}	45mA to .9mA	V _{gs} = -30V

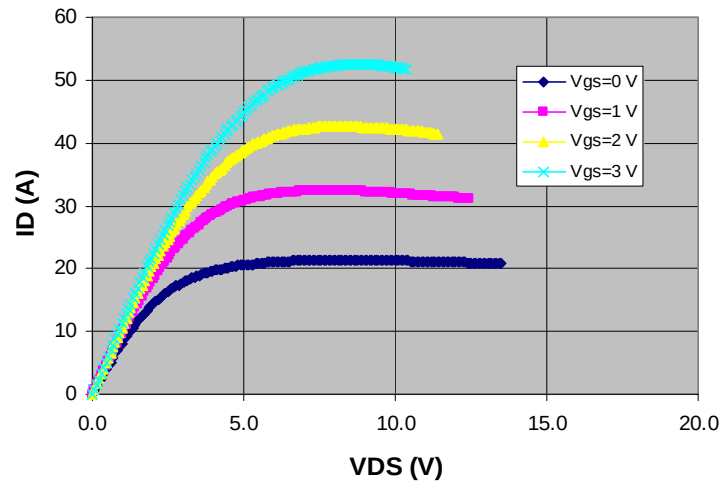


Figure 30: Typical I_D - V_{GS} curves of packaged lot 10 VJFETs with an active area of 3mm^2 .

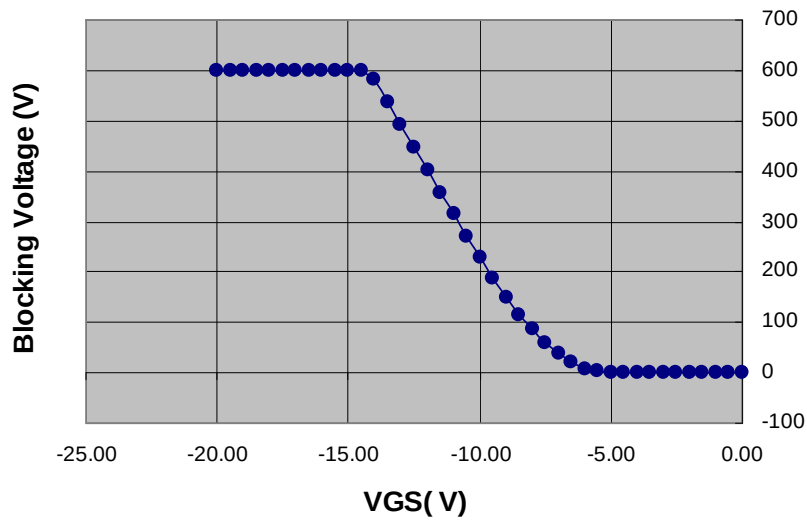


Figure 31: Typical blocking gain curve of the packaged Lot 10 VJFETs. Blocking gain curve was taken at $I_D = 200\mu\text{A}$.

Characterization of single SiC VJFET. A single 3 mm^2 (active area) SiC VJFET was assembled in a TO257 package. Figure 32 illustrates typical on-state DC characteristics of the 3 mm^2 SiC VJFET.

The $R_{\text{on-sp}}$ calculated in the linear region decreased from $3.18 \text{ m}\Omega\cdot\text{cm}^2$ at V_{GS} of 0 V to $2.56 \text{ m}\Omega\cdot\text{cm}^2$ at V_{GS} of 3 V. In Figure 32, forward current I_{DS} reaches 48.6 A at V_{DS} of 5.25 V and 57.1 A at V_{DS} of 9 V under V_{GS} of 3 V, which correspond to current density of 1620 A/cm^2 and 1903 A/cm^2 respectively.

Blocking characteristic of the SiC VJFET is shown in Figure 32 (b). Channel punch-through voltage is defined by the V_{DS} at which the drain leakage current reaches $200 \text{ }\mu\text{A}$ at a given V_{GS} . As shown in Fig. 3, the pinch-off voltage (V_{pin}) is measured at -12.2 V. The device blocking capability is limited by channel “punch-through” rather than dielectric breakdown (e.g., impact ionization), where the punch-through voltage is defined at a given V_{GS} by the V_{DS} at which $I_{\text{RDS}} = 200 \text{ }\mu\text{A}$. A blocking gain ($\Delta V_{\text{DS}}/\Delta V_{\text{GS}}$) of 54 is obtained at gate bias ranging from -13 V to -23 V and I_{RDS} of $200 \text{ }\mu\text{A}$.

An efficient gate control on the forward conduction of the SiC VJFET will require a robust and stable gate-source PN junction, meaning negligible gate-source leakage current (I_{RGS})

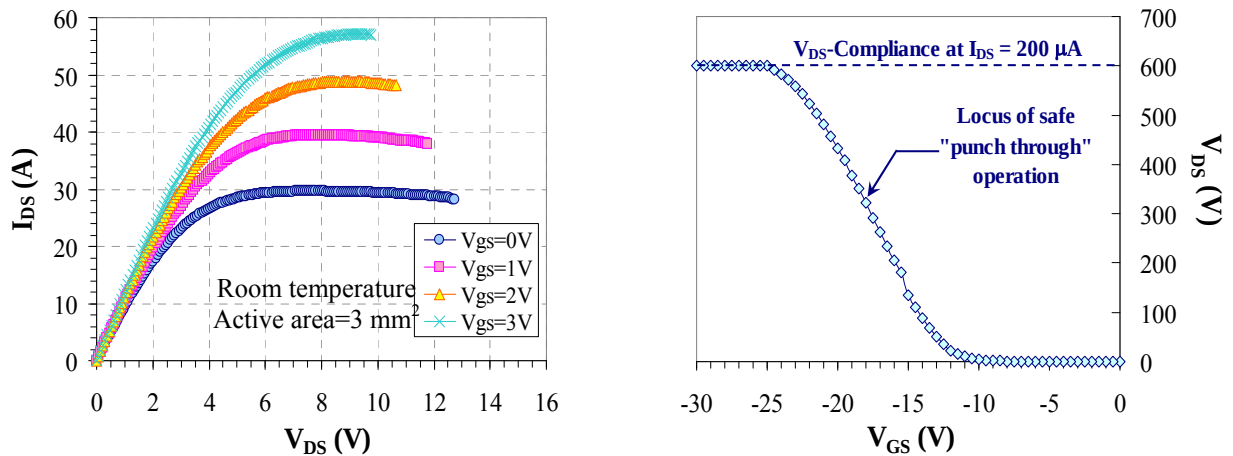


Figure 32: (a) Typical on-state conducting characteristics of a SiC VJFET. (B) Off-state blocking characteristics of a SiC VJFET.

under reverse biases. In, Figure 33, one can see that gate-source PN junction of the SiC VJFET is able to block up to 30 V at I_{RGS} less than 45 μA at room temperature, which is sufficient to provide a superior gate control over the operating bias range.

The device transient characteristic is evaluated by a simple internal gate resistance measurement. The internal gate resistance is estimated using a C-V meter with zero DC gate-to-source bias. The meter applies a 30-mV (RMS), 1-MHz AC test signal and the phase angle

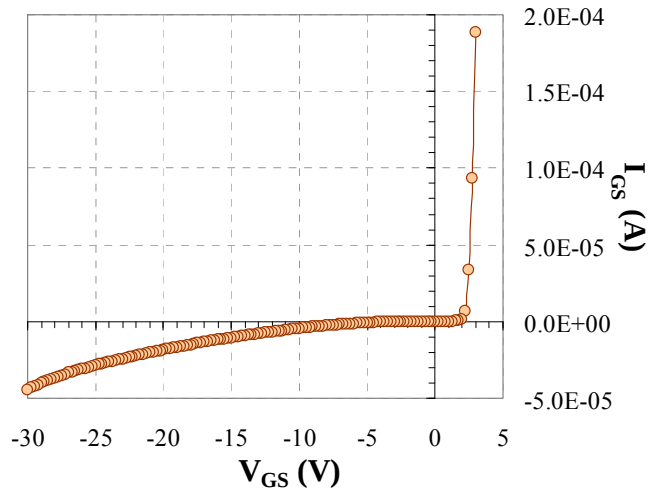


Figure 33: I-V characteristic of gate-source PN junction of the SiC VJFET at room temperature.

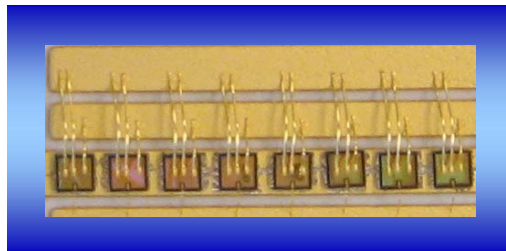


Figure 34: A photograph of eight-paralleled SiC VJFETs in a demonstration power module.

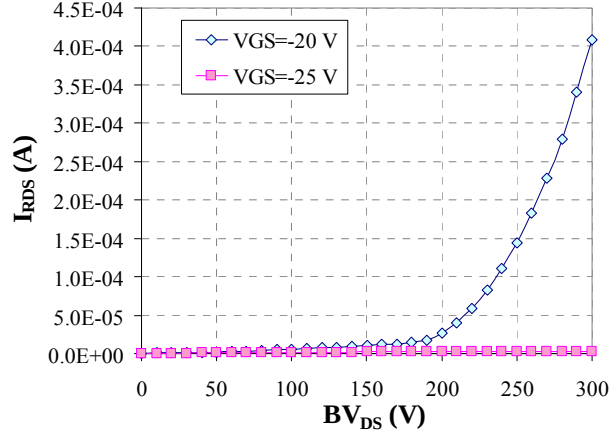


Figure 35: Reverse blocking of the eight-paralleled SiC VJFETs at V_{GS} of -20 V and -25

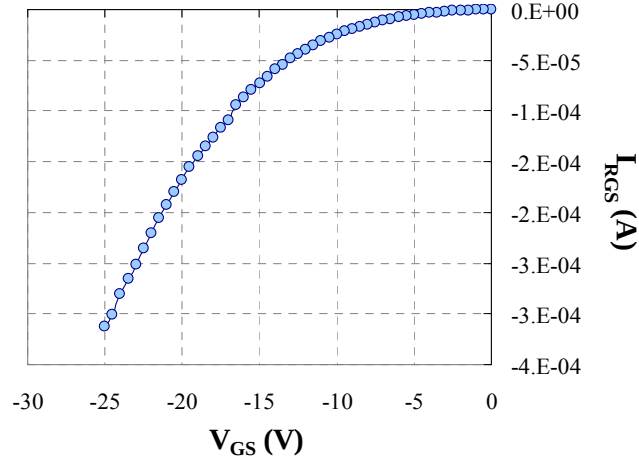


Figure 36: Reverse blocking capability of gate-source PN junction of the eight-paralleled SiC VJFETs.

is measured between the applied AC voltage and the induced AC current. This phase angle is resolved into a real and an imaginary impedance component using a lumped circuit model composed of a single resistance and capacitance in series. The internal gate resistance is then estimated from the real part of the impedance model. In this study, the estimated internal gate

resistance of the SiC VJFET (data not shown) indicates that the device is well suited for switching in a range of kHz to MHz.

High-temperature characterization of eight-paralleled, 600 V, 4H-SiC VJFETs. In order to demonstrate the use of SiC VJFETs for high-power applications, a high current, 600 V power module was fabricated by bonding multiple die in parallel until a desired high current rating was achieved. For this purpose, eight die that individual testing showed to have similar properties were bonded in a custom package, as shown in Figure 34. It was then tested for DC characteristics at room temperature and 175 °C.

As shown in Figure 37, total I_{RDS} of the eight-paralleled SiC VJFETs was measured at V_{GS} of -20 V and -25 V up to 50% of their full BV_{DS} . At BV_{DS} of 300 V, the total I_{RDS} are 409 μA and 3.1 μA at V_{GS} of -20 V and -25 V, respectively. Figure 36 shows that total I_{RGS} of gate-source PN junction of the eight-paralleled VJFETs is $\sim 310 \mu A$. The forward conduction shown in Figure 37 of the eight-paralleled VJFETs was characterized with a Tektronix Model 370 curve tracer in a pulsed mode using a 100- μs pulse width. A forward current of 361 A was achieved at V_{DS} of 5.25 V and V_{GS} of 3 V, which is equivalent to a current density of 1504 A/cm². The corresponding R_{ONSP} at V_{GS} of 3V in linear region is 2.8 m Ω .cm² at room temperature. Compared to the single die shown in Figure 32, a slight distortion of the current density from that of the individual die may be due to the current sharing.

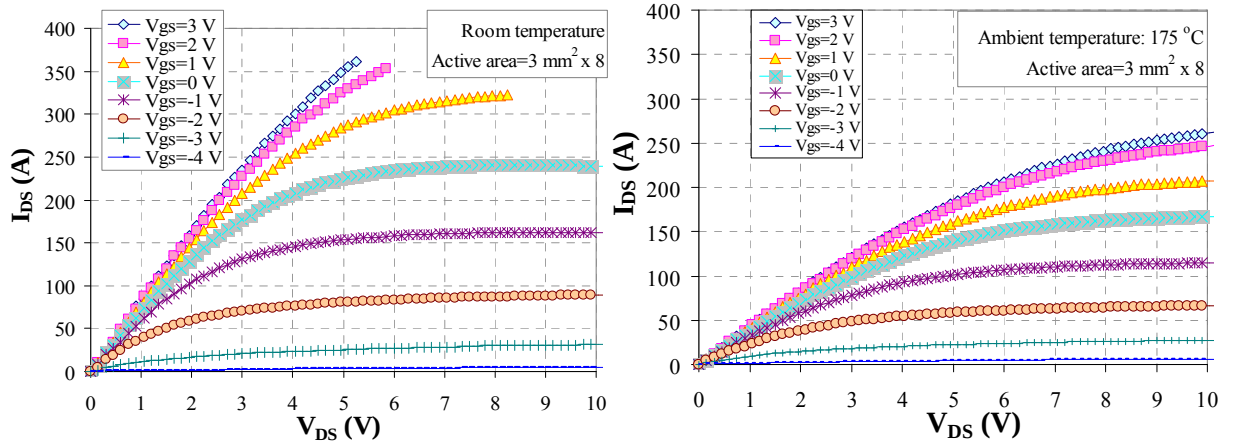


Figure 37: (a) Forward conduction of eight paralleled SiC VJFETs at V_{GS} of +3 V to -4 V with an interval of 1 V at room temperature. (b) Forward conduction of eight parallel SiC VJFETs at V_{GS} of +3 V to -4 V with 1 V interval at 175°C .

The eight-paralleled VJFETs were then heated and characterized at 175°C . The forward current reduced to 188 A at drain-source bias (V_{DS}) of 5.25 V and V_{GS} of 3 V. The total R_{ONSP} at V_{GS} of 3V in linear region increased to $5.35 \text{ m}\Omega\cdot\text{cm}^2$ at 175°C , which corresponds to a shift of $0.61\%/^\circ\text{C}$ from room temperature to 175°C .

4.1. PRODUCIBILITY LOTS

Over the last reporting period, there has been significant effort into growing epitaxy required for furthering the producibility demonstration past the initial results from the advanced devices in Task 1. Table 10 summarizes the epitaxy now available for wafer starts. The mask design is complete and the wafers are in queue for source finger etch. All devices are designed with 3mm^2 active area.

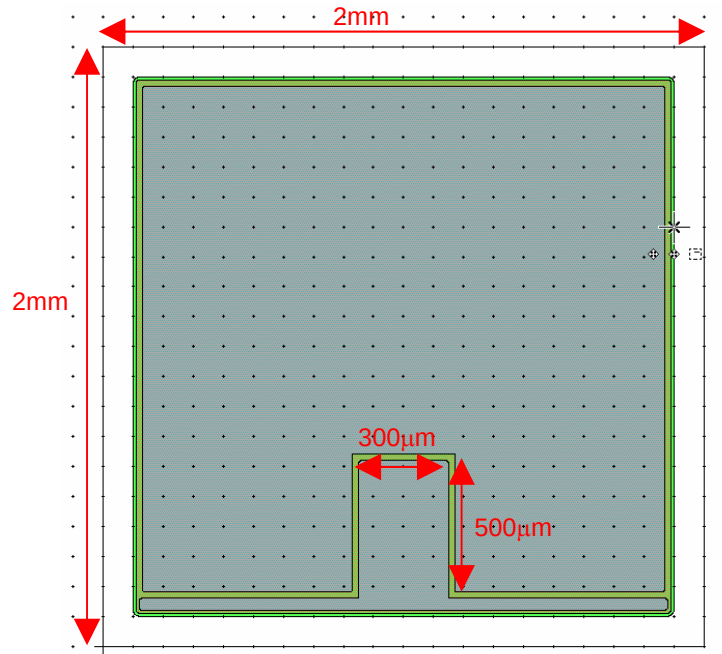


Figure 38: Die layout for producibility lots. Mesa size is 2mm x 2mm with an active area of 3mm².

Table 10: Producibility Lot Designs

Split	# Wafers	Source Cap	Channel	Drift
1	6	0.5µm / >1E19	3.0µm / 3E16	7.0µm / 1.3E16
2	6	0.5µm / >1E19	3.0µm / 3E16	7.0µm / 1.3E16
3	7	0.5µm / >1E19	3.0µm / 3E16	7.0µm / 1.3E16
4	7	0.5µm / >1E19	3.0µm / 3E16	7.0µm / 1.3E16
5	7	0.5µm / >1E19	2.0µm / 3E16	7.0µm / 1.3E16
6	7	0.5µm / >1E19	2.0µm / 3E16	7.0µm / 1.3E16
7	7	0.5µm / >1E19	3.0µm / 3E16	6.5µm / Graded
8	7	0.5µm / >1E19	1.3µm / 3E16	10.0µm / 1.3E16
9	7	0.5µm / >1E19	3.0µm / 3E16	10.0µm / 1.3E16

5. TASK 5: RELIABILITY EVALUATION

5.1. Introduction

Reliability of silicon carbide (SiC) devices is of critical importance in FET controlled devices such as VJFETs for high-power system applications. The inherent physical properties of SiC are well-suited for semiconductor electronic devices. SiC power FETs and diode rectifiers have been demonstrated to operate over higher voltage and temperature ranges, have superior switching characteristics, as well as have die sizes nearly twenty times smaller than correspondingly rated silicon-based devices [6]. This would enable large power system performance improvements. Among the SiC power devices, SiC JFETs are the only controlled turn on/off SiC device free from gate oxidation and high-temperature metal-semiconductor Schottky barrier reliability issues. With the vertical-channel structure, SiC VJFETs enable a higher packing density, lower on resistance, and easier to fabricate at reduced cost than power FETs having a pre-channel or lateral channel region [7]. In this work, we have studied high-temperature static and dynamic reliability of 600-V 4H-SiC VJFETs intended for commercial operations.

5.1.1. Definition of Failure

Initial reliability study from Lot 7 devices have used a very simple definition of failure: gate current reaching compliance. This has the virtue of simplicity, but does not meet industry standard failure definitions. The reliability literature on Si IGBTs suggests a more complete failure definition: 20% variation of any specified device parameter, or gate current rising above a specified value. Gate current is treated differently because in the ideal device, it tends toward zero. Specifying a percentage variation in a quantity tending toward zero is

asking for spurious behavior from a spec. For the purpose of initial analysis, we propose the following definition of device failure:

The device will be considered to have failed if any of the following criteria have been met:

- a. Drop in forward current of 20 % or more from initial value
- b. Drop in blocking voltage of 20 % or more from initial value
- c. Gate current under reverse bias reaches compliance (100 μA)

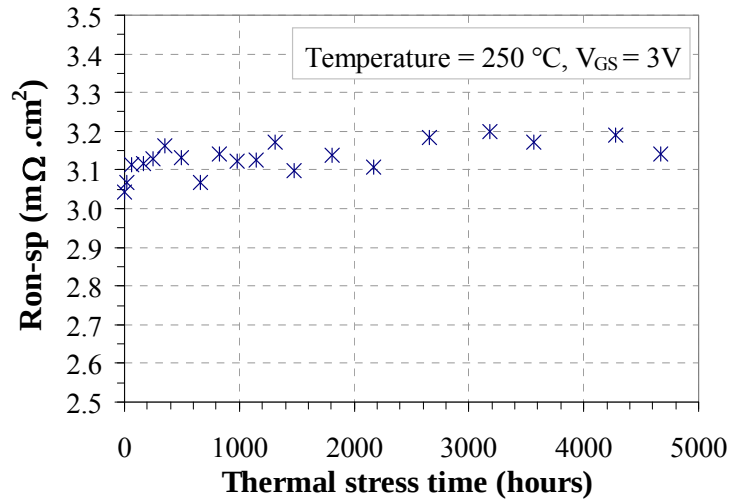
Ideally, a failure definition should include all parameters important to the use of a device in an application. In particular, we would like to have a gate current spec more stringent than compliance. Never the less, in the interest of circulating preliminary results within SemiSouth and MSU, we will use this definition for the present. We may revisit the raw data later on for additional analysis as needed.

5.1.2. Experiment and results

Critical transistor failure modes include thermal runaway that mostly affect bipolar junction transistors, contact migration, and thermal fatigue, which can eventually lead to a short circuit mode. In this study, three life test conditions have been conducted at temperatures up to 250 °C: (a) electrically unbiased thermal stress; (b) static high-temperature reverse bias; (c) dynamic lifetime switching test.

5.1.2.1. Unbiased thermal stress

The SiC VJFETs were thermally stressed in an oven at a constant temperature of 250 °C in air. The devices were brought to room temperature periodically for DC and switching characterizations. Figure 39 shows the specific-on resistance (R_{on-sp}) in linear region of a SiC VJFET at gate bias (V_{GS}) of 3 V under thermal stress for 4672 hours. The R_{on-sp} mainly remained unchanged with an average and median value of 3.13 m Ω .cm², indicating that the Ohmic contacts were stable and reliable after a long-term thermal stress. Figure 40 illustrates the switching performance of a SiC VJFET under thermal stress for 1728 hours. Total response time of the device increased from 36.2 ns to 47 ns after the initial 168 hours thermal



stress and then stayed around 45 ns up to 1728 hours thermal stress.

Figure 39: Forward DC conduction of the SiC VJFETs before and after 4672 hours thermal stress at 250 °C in air.

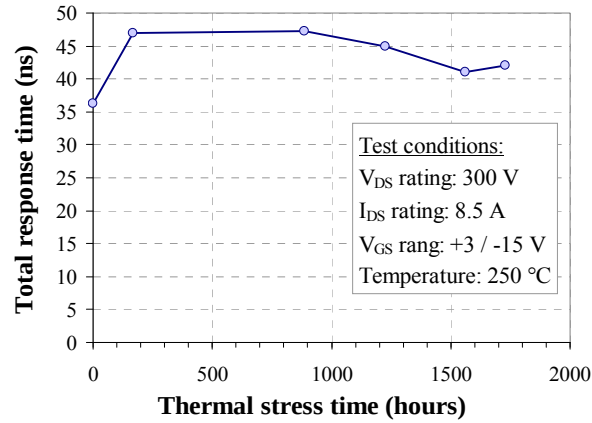


Figure 40: Switching performance of the SiC VJFETs thermal stress at 250 °C in air for 1728 hours.

5.1.2.2. High-temperature reverse bias (HTRB) test

HTRB is used to determine the effects of bias conditions and temperature over time. HTRB stresses the device in the blocking mode while at an elevated junction temperature in order to accelerate any blocking voltage degradation.

The primary failure mode for HTRB is a degradation of the breakdown characteristics. Such degradation is usually caused by the presence of foreign materials or ionic contamination, which migrates more quickly at high temperature under the applied field and alters the electric field-termination structure.

5.1.2.2.1. HTRB test set-up and typical results

HTRB test was performed to monitor the off-state drain-source leakage (I_{DS}) and gate-source leakage (I_{GS}) under 300-V drain-source reverse-bias (i.e.: 50% rated of device full blocking voltage) and V_{GS} of -20 V at 250 °C in air. As shown in Figure 41, the I_{DS} slightly decreased within the initial 400 hours HTRB test and then stayed below 5 μA up to 2278 hours. Meanwhile, the I_{GS} slightly increased within the first 130 hours HTRB test and then

stabilized between 20 ~ 50 μA up to 2278 hours. These results demonstrate the advantage of JFET over MOSFET by eliminating a concern of charge movement or trapping in the gate oxide of MOSFET during long-term high-temperature operation.

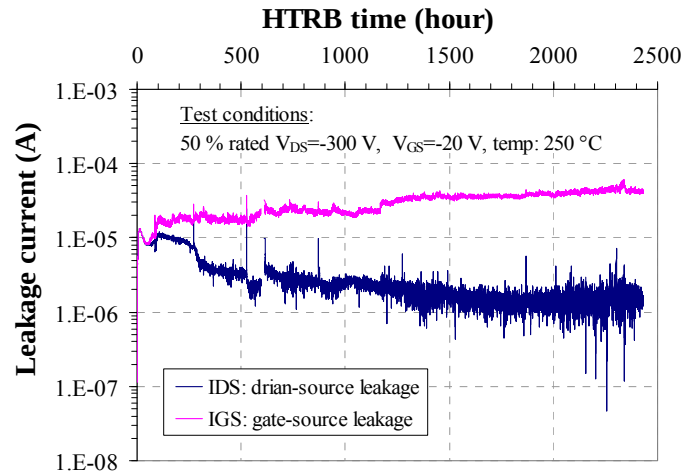


Figure 41: HTRB measurement of the SiC VJFETs at 50% rated V_{DS} of 300 V and V_{GS} of -20 V at 250 °C in air for 2278 hrs.

5.1.2.2.2. Weibull distributions (by Dr. Paul Martin)

Given the failure definitions in another section, we can summarize the results of the HTRB reliability test in a number of ways. The simplest is to report a median lifetime for each sample. Alternatively, we can characterize the life distribution of the sample and describe the parameters of that distribution. As we have stated earlier, this data is consistent with a Weibull distribution. It is also consistent with a lognormal distribution, and there is not enough data to distinguish objectively between the two fits. While a Weibull distribution is a standard in some fields (notably in the Si packaging reliability area) the lognormal distribution is the universal choice for compound semiconductor reliability. We are looking

at a sample of 7 devices from the CA wafer and 8 devices from the HK wafer. This is not a large sample. We believe it is premature to choose between the two distributions at this time. It is accepted practice to withhold judgment about the life distribution early in the development of a new technology.

For reference, the Weibull and Lognormal plots are shown below for the CA wafer. The Weibull plot shows a marginally superior fit, but the difference is small.

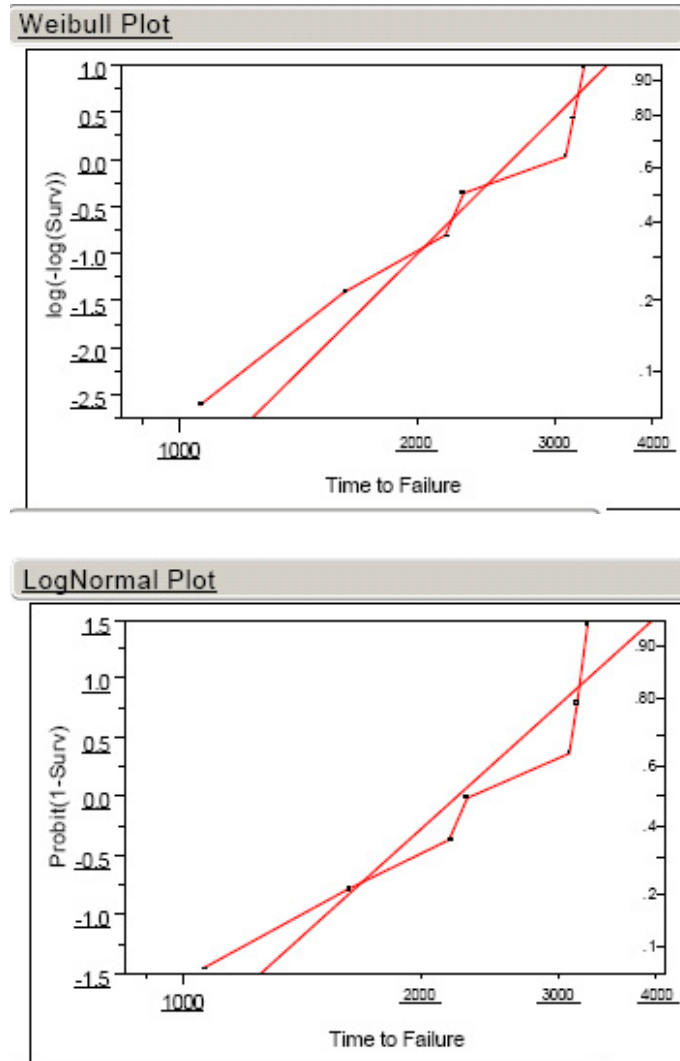


Figure 42: Weibull plots for the CA-01 wafer.

One convenient characteristic of the Weibull distribution is that one of the parameters has the dimensions of time, and is called the Weibull characteristic lifetime. This allows us to compare the available statistics as shown in Table 11.

Table 11. Lifetime Estimates

CA Median Life	CA Weibull Characteristic Lifetime	HK Median Life	HK Weibull Characteristic Lifetime
2279.9	2662	21.3	34.5

The median is a very robust statistic, in that it is insensitive to outliers. In the case of wafer CA, there are seven samples, and the median corresponds to the failure time of the fourth device. As it happens, the median life time is insensitive to our choice of failure definitions.

5.1.2.3. Lifetime switching measurement

An initial lifetime switching test has been conducted at room temperature. As seen in Figure 43, the device has been switching nearly 12,000 hours without a single failure. After the first several hours operation, case temperature of the SiC VJFET has been staying constant at 60 ~ 66 °C by device self-heating. Variations of the rise time (t_r) and fall time (t_f) are being kept within 23% from the beginning to now.

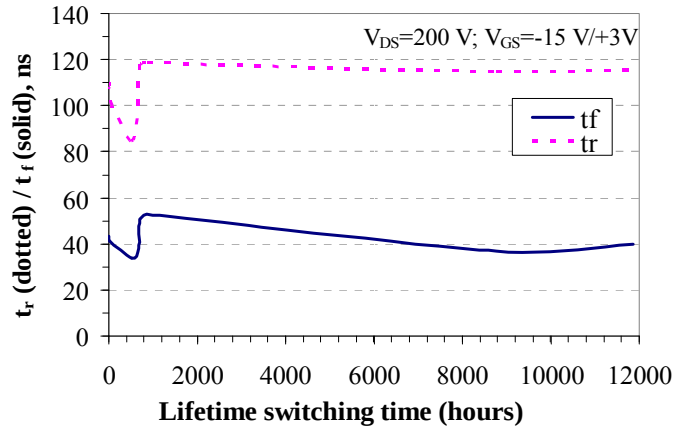


Figure 43: Rise time (t_r) and fall time (t_f) v.s. switching time of the 600-V SiC VJFET.

5.1.2.4. Failure Mechanisms

Three failure mechanisms were observed: increasing gate current, loss of drain-source blocking voltage, and decreasing forward current. Many devices exhibited multiple failure mechanisms. Failure mechanisms are summarized in Table 12. It should be noted that one HK device is still alive in the high temperature storage test, and has only recently shown any signs of change (a slight variation in gate leakage current, which is still quite low). This is the reason for the 50% entries in the HK storage row.

Table 12: Failure Mechanisms Observed.

Wafer	Gate Current Increase	Blocking Voltage Decrease	Forward Current Decrease
CA HTRB	71 %	29 %	43 %
HK HTRB	62 %	100 %	0 %
CA Storage	100 %	0 %	100 %
HK Storage	50 %	50 %	50 %
Epifet Storage	100 %	100 %	100 %

Another view of failure mechanisms is obtained by tracking the mechanism by which the device crosses the failure threshold. We call this the proximate cause of failure. This is summarized in Table 13. Please note that changes in the failure criterion will cause changes in Table 13, but not in Table 12.

Table 13: Proximate Cause of Failure

Wafer	Gate Current Increase	Blocking Voltage Decrease	Forward Current Decrease
CA HTRB	71 %	0 %	29 %
HK HTRB	25 %	75 %	0 %
CA Storage	50 %	0 %	100 %
HK Storage	0 %	0 %	50 %
Epifet Storage	0 %	0 %	100 %

The thermal storage differs from the HTRB test in one respect. While failure modes for the HTRB test were highly varied, all of the failed devices in thermal storage failed due to a drop in forward current. It is apparent from the comparison that application of bias adds additional failure modes to the device. Unfortunately, it is difficult to generalize with the small numbers of devices involved in the thermal storage test.

5.1.2.5. Extrapolation to useful life time

It is not possible to use this data to extrapolate a life time at operational temperature. For this purpose, it is necessary to perform a three temperature life test. This will allow extraction of activation energy for device failure, and extrapolation of accelerated failure rates to an expected life time at operating temperatures.

At present, we are equipped with a single oven for running HTRB tests. Running three temperature life tests serially in one oven consumes an unacceptable amount of time. We are looking at funding mechanisms which would allow us to construct at least two additional ovens. The funding challenge is not the oven itself, but the electronic instrumentation, ceramic circuit boards, relays, etc.

The fastest route to a three temperature life test would be to scale up the buck converter switching test to many devices at three temperatures. This does not replace the need for the HTRB test, since the buck converter places a different stress on the device, but it would be a useful test which is extremely relevant to at least one application.

5.2. ARFL “Bully” Reliability Study

5.2.1. Purpose of this study

The purpose of this study is to produce test data and relevant information to confirm that SemiSouth’s 600-V VJFETs meet the reliability requirements for market introduction. Based on the previous ARFL Lot 7 reliability study described in another section and limit of quality of the available devices for this study, the gate leakage current compliance for the HTRB test is modified to 370 μ A instead of 100 μ A defined in another section.

The test vehicle is “Bully-VJFETs” assembled into a TO-257 package and potted with a dielectric gel, which represents the device with 1 mm² active area in the family of 600-V, normally-on SiC VJFETs.

5.2.2. Description of stress test set-up

5.2.2.1. High Temperature Reverse Bias (HTRB) test set-up

The High Temperature Reverse Bias Test System (HTRB) is designed to source operating voltages and measures the resulting currents of 45 reverse biased Vertical Junction Field Effect Transistors (VJFET) for long periods at high temperatures. The system capabilities include: reverse bias gate to source voltage from 0 to -110 vdc, drain to source voltage from 0 to 1000 vdc, transistor operating temperatures from room temperature up to 300 °C, and continuous testing for up to 100 days (or 2,400 hours). System hardware consists of an oven to maintain the VJFETs at high temperature, a transistor test fixture built into the oven door to facilitate easy insertion and removal of transistors, and a data acquisition rack that houses instrumentation and a computer for controlling the test system. The test system software is written in Lab View and provides the system user interface, controls the test instrumentation, provides a method to store and edit test parameters, logs test data, and provides spreadsheet and charts for graphical data display in real time. **Table 14** below describes the test conditions, measured parameters, and failure criteria.

Table 14: HTRB test set-up:

Test Conditions	Measured Parameters	Failure Criteria
Temperature: 200 °C	$R_{DS(ON)} @ V_{GS}=+3 \text{ V}$	Exceeds > 20% shift
Drain-source bias: -480 V	$V_{GS} @ V_{DS}=600 \text{ V (BV gain)}$	Exceeds > 20% decrease
Gate-source bias: -20 V	$I_{RGS} @ -25 \text{ V}$	Exceeds > 5X increase (post/pre)

5.2.2.2. Thermal resistance measurement

Thermal resistance measurements of devices from the Bully lot were made by Analysis Tech, a company in Wakefield, Massachusetts which specializes in these measurements. The measurement technique follows the recommendations of the JEDEC standard JESD51-1, and was done in dynamic mode. The forward bias of the gate-source diode driven by a 20 mA current source was used as the temperature sensitive parameter. Prior to the measurement, a calibration curve is created for a single device by immersing the device in a dielectric oil bath to ensure thermal equilibrium, as shown in Figure 44. To measure the thermal resistance, the device is first placed on an air cooled heat sink with an embedded thermocouple contacting the back of the case. The device is clamped to the heat sink with a pneumatic clamp which ensures a constant clamping force even in the presence of thermal variations in the device dimensions.

A biasing network was then applied to the device as depicted in Figure 44b. In this configuration, the power dissipation of the device is determined by the value of the voltage applied at the V_{port} terminal. Both the V_{port} and the Sense Channel (Source and Sink) are electrically switched. During powering, the V_{port} is active and the Sense Channel is inactive. During junction temperature sensing, which lasts approximately 300 μs , the opposite is true. In other words, the device is heated with pulses of current applied between drain and source.

Between the heating pulses, the diode temperature is measured by applying 20 mA to the gate-source diode and measuring the forward voltage drop. The interruption is relatively short because the intent is to achieve a steady state condition. Nevertheless, some device cooling occurs during the interruption in the heating current. To account for this, the device temperature is measured at a series of delay times after the interruption of the heating pulse. The temperature is then extrapolated back to the instant when the heating pulse was interrupted.

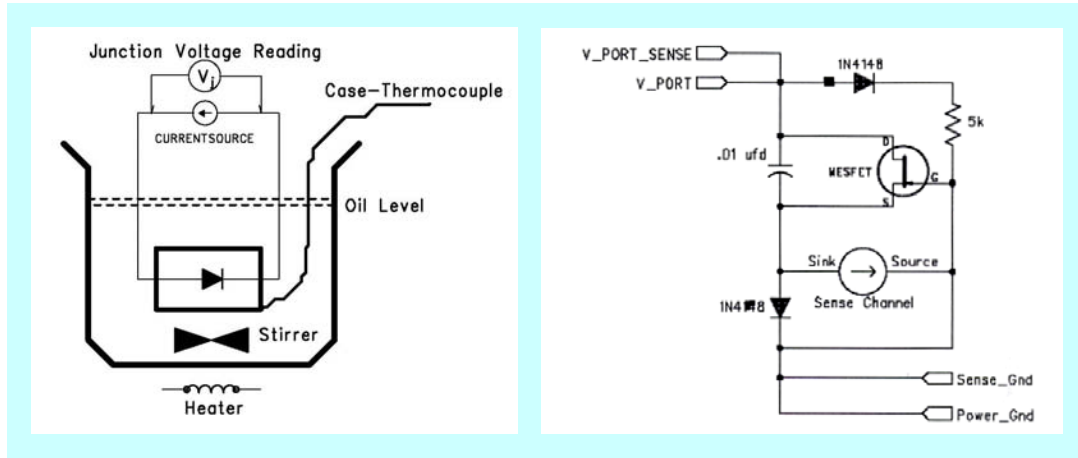


Figure 44: (a) Bath Method of Junction Calibration. (b) MESFET linear test method connections used for thermal resistance measurement of SiC VJFETs.

I-V characteristic of the gate-source diode was then measured as a function of temperature. The relationship between junction voltage and temperature is linear over a wide range in junction temperature. For a group of parts which are “identical” (in our case, this applies to parts of the same active area and source finger width) the calibration curves will have the same slope but different intercepts. This means that additional parts can be calibrated at a

single temperature point, and assigned a calibration curve with a unique intercept, but the same slope as the part which was extensively calibrated.

5.2.3. Stress test result

5.2.3.1. High Temperature Reverse Bias (HTRB)

There were 15 out of 32 selected parts past the initial 48 hours “burn-in” test at 200 °C. Among these 15 devices, 13 devices survived through the 1000 hours HTRB test. All failed devices were due to an increase of either gate-source or drain-source leakage current under the reverse biases at 200 °C.

For all “survived” devices, the data collected in **Table 15** show no significant shift in $R_{DS(ON-SP)}$ and BV Gain but about 75% reduction on the reverse gate-source leakage current (I_{RGS}). There are also no significant changes on the forward characteristics before and after 1000 hours HTRB stresses. An exemplary I-V characteristics measured from device #J388 before and after the 1000 hours HTRB stresses is shown in Figure 45.

Table 15: $R_{DS(ON-SP)}$, BV Gain, and I_{RGS} before and after 1000 hours HTRB stresses:

Device #	$R_{DS(ON-SP)}$ ($m\Omega \cdot cm^2$) at $V_{GS} = 3$ V			BV Gain at $I_{RDS} = 100$ μA			I_{RGS} (A) at $V_{GS} = 25$ V		
	Pre-stress	Post-stress	(Post-Pre)/Pre%	Pre-stress	Post-stress	(Post-Pre)/Pre%	Pre-stress	Post-stress	(Post-Pre)/Pre%
J387	1.868	1.758	-5.90%	-60.35	-64.25	6.47%	-4.76E-04	-8.10E-05	-82.98%
J388	1.789	1.744	-2.53%	-61.60	-62.03	0.70%	-2.61E-04	-4.05E-05	-84.49%
J407	1.801	1.707	-5.26%	-58.36	-59.05	1.19%	-2.22E-04	-6.14E-05	-72.37%
J408	1.831	1.762	-3.82%	-60.74	-64.36	5.96%	-2.79E-04	-6.04E-05	-78.38%
J409	1.811	1.691	-6.64%	-58.89	-61.72	4.80%	-3.69E-04	-7.23E-05	-80.40%
J416	1.693	1.729	2.10%	-62.09	-68.41	10.17%	-2.93E-04	-7.26E-05	-75.17%
J420	1.786	1.744	-2.32%	-67.15	-69.74	3.86%	-2.20E-04	-4.22E-05	-80.86%
J422	1.865	1.767	-5.28%	-66.14	-68.71	3.88%	-2.05E-04	-5.15E-05	-74.93%
J423	1.778	1.720	-3.29%	-48.53	-72.51	49.43%	-3.15E-04	-6.81E-05	-78.39%
J427	1.843	1.801	-2.26%	-68.99	-73.11	5.96%	-4.94E-04	-1.80E-04	-63.53%
J428	1.762	1.788	1.46%	-71.26	-71.83	0.80%	-3.34E-04	-6.22E-05	-81.40%
J430	1.890	1.777	-6.03%	-49.86	-46.99	-5.74%	-2.27E-04	-1.04E-04	-54.26%
J434	1.823	1.760	-3.41%	-54.76	-65.00	18.71%	-4.36E-04	-1.66E-04	-62.00%
J435	1.866	1.807	-3.13%	-67.28	-70.55	4.86%	-5.03E-04	-1.22E-04	-75.70%
Average	1.815	1.754	-3.31%	-61.14	-65.59	7.93%	0.00	0.00	-74.63%
Stdev.	0.052	0.034	2.60%	6.82	6.92	13.13%	0.00	0.00	8.85%

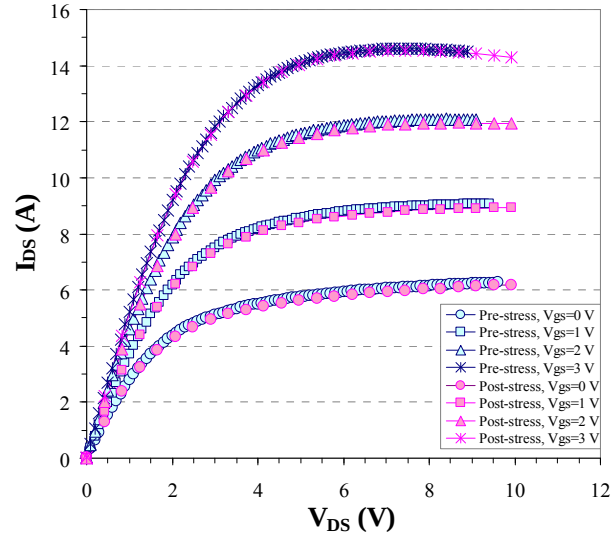


Figure 45: Forward characteristics of device #J388 before and after 1000 hours HTRB stresses.

Figure 46 shows the HTRB measurement of the device #J388 at 80% rated V_{DS} and V_{GS} at 200 °C in air for 1000 hours. After the first 150 hours stresses, both drain-source and gate-source reverse leakage current were stabilized and remained virtually unchanged.

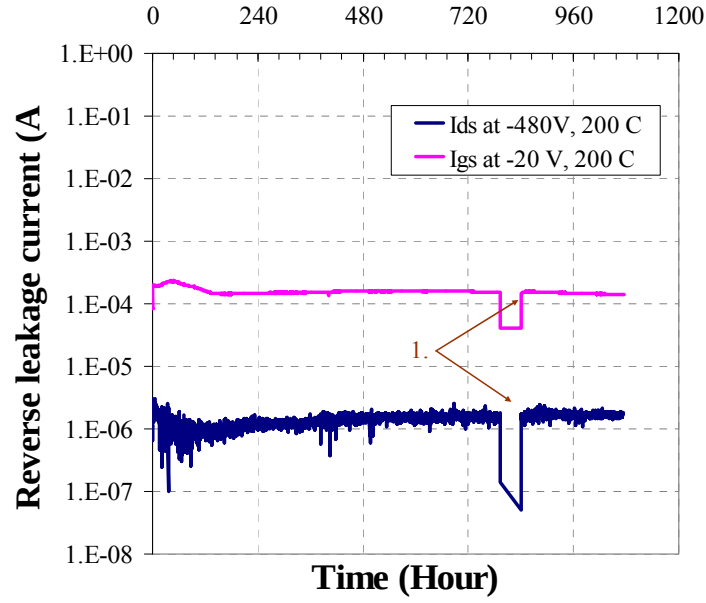


Figure 46: 9 HTRB measurement of the device #J388 at 80% rated V_{DS} of 480 V and V_{GS} of -20 V at 200 °C in air for 1000 hours. At point 1, the test was interrupted and restarted.

5.2.3.2. Internal gate resistance and capacitance estimates

To predict the device switching performance before, during, and after the 1000 hours HTRB stresses, the internal gate resistance (R_s) and capacitance (C_s) were estimated by simply measuring the gate-source two terminals with drain terminal floating. The data collected in **Table 16** show no significant shifts in R_s and C_s . Data for devices #427, 428, 430, 434, and 435 will be added in when available.

Table 16: Estimates of internal gate resistance and capacitance:

Device #	Rs (Ω)			Cs (pF)		
	0 hr	792.5 hrs	1000 hrs	0 hr	792.5 hrs	1000 hrs
J388	988	986	986	116	116	116
J407	1000	1009	1001	113	112	113
J408	951	961	939	118	118	118
J409	965	966	947	120	118	118
J416	814	815	785	133	130	132
J420	887	897	863	126	124	126
J422	783	792	770	137	135	136
J423	869	880	844	129	126	128

5.2.3.3. Thermal Resistance Measurement

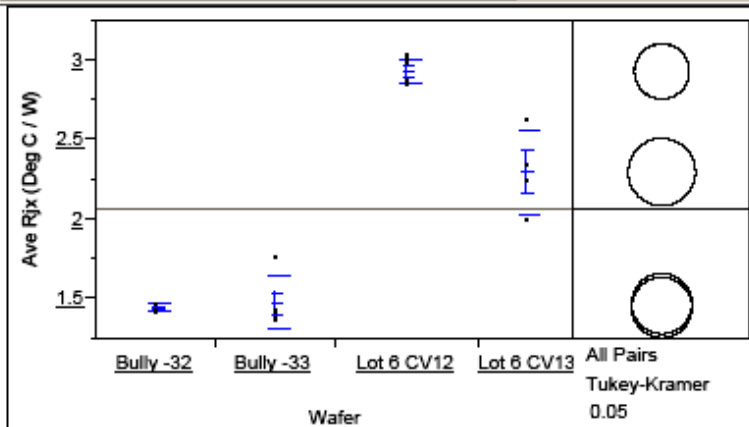
According to the data sheet provided by “Analysis Tech” in Figure 47, the average thermal resistance (R_{th}) measured on 10 devices sampled from two wafers is in the range of 1.4558 ± 0.012 °C/W, which is two times lower than the R_{th} measured from Lot 6 VJFETs fabricated about two years ago.

Sheet1- Fit Y by X

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Data Table=Sheet1

Oneway Analysis of Ave Rjx (Deg C / W) By Wafer



Excluded Rows 21

Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
Bully -32	5	1.44380	0.023952	0.01071	1.4141	1.4735
Bully -33	5	1.46780	0.165954	0.07422	1.2817	1.6739
Lot 6 CV12	6	2.92767	0.080656	0.03293	2.8430	3.0123
Lot 6 CV13	4	2.29425	0.263208	0.13180	1.8754	2.7131

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

q*	Alpha			
2.86102	0.05			
Abs(Dif)-LSD				
	Lot 6 CV12	Lot 6 CV13	Bully -33	Bully -32
Lot 6 CV12	-0.2453	0.3592	1.2026	1.2266
Lot 6 CV13	0.3592	-0.3004	0.5415	0.5655
Bully -33	1.2026	0.5415	-0.2687	-0.2447
Bully -32	1.2266	0.5655	-0.2447	-0.2687

Positive values show pairs of means that are significantly different.

Level	Mean
Lot 6 CV12 A	2.9276667
Lot 6 CV13 B	2.2942500
Bully -33 C	1.4678000
Bully -32 C	1.4438000

Levels not connected by same letter are significantly different

Level	- Level	Difference	Lower CL	Upper CL
Lot 6 CV12	Bully -32	1.483867	1.22661	1.741127
Lot 6 CV12	Bully -33	1.459867	1.20261	1.717127
Lot 6 CV13	Bully -32	0.850450	0.56545	1.135449
Lot 6 CV13	Bully -33	0.826450	0.54145	1.111449
Lot 6 CV12	Lot 6 CV13	0.633417	0.35918	0.907657
Bully -33	Bully -32	0.024000	-0.24470	0.292700

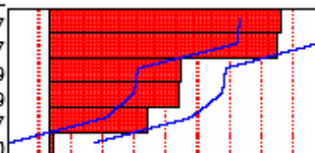


Figure 47: 10 Data sheet of thermal resistance results provided by “Analysis Tech”.

5.3. Summary

In summary, without any industrial standard and reference for the SiC VJFETs reliability, we have initialized three types of reliability tests to monitor the device performance during the environmental stresses, including HTRB, thermal storage, and life-time switching tests. In order to fully and more accurately evaluate the static and dynamic reliability of the SemiSouth's VJFETs, more stress tests (such as power-cycle, three temperature accelerated life-test, high-temperature switching life-test) should be considered as per availability of financial funding.

6. References

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