

SYNCHRONOUS IMPULSE RECONSTRUCTION (SIRE) RADAR SENSOR FOR AUTONOMOUS NAVIGATION

Marc A. Ressler, Lam H. Nguyen, Francois J. Koenig, and Gregory Smith
Sensors and Electron Devices Directorate
U. S. Army Research Laboratory
Adelphi, MD 20783

ABSTRACT

The Army Research Laboratory (ARL) has designed and fabricated an impulse-based, ultra-wideband (UWB) imaging radar to examine the utility of using a foliage-penetrating radar with other sensors to support autonomous navigation in robotic vehicles. This radar would also have application in mine detection and through-the-wall sensing. This proof-of-concept radar system employs a physical array of 16 receive antennas to provide the necessary aperture for sufficient cross-range resolution in the forward-looking geometry used in a robotic mission. Each antenna feeds a base-band receiver/digitizer that integrates the data from a number of radar pulses before passing it on to the personal computer (PC) based operator's console and display. The innovative ARL receiver design uses commercially available integrated circuits to provide a low-cost, lightweight digitizing scheme with an effective sampling rate of approximately 8 GHz. The design is extensible to allow for growth in the number of channels used and improvements in integrated circuit performance to eventually meet the expected unmanned ground vehicle combat pace. Using modules based on commercial off-the-shelf (COTS) components allows for continued expansion of capabilities of the system based on increasing capabilities of these components.

1. INTRODUCTION

The ability of our current and future forces to use unmanned systems increases their survivability. In addition, autonomous navigation systems will play a key role in the Army's Future Combat System as a force multiplier. A key element in defining the utility of these systems on the battlefield is their ability to perceive the environment that they are traversing. Most robotic "vision" systems are based on optical (video) or laser sensor systems. In combat and cross-country environments these systems have problems with fog and dust, as well as grass and foliage, blocking their sight lines to obstacles in their path. Interest has been expressed in adding a radar to augment the robotic-sensor suite to improve the ability to operate in obscured conditions. While short range penetration of dust and fog is typically not a problem for most radar systems, it is known that high-frequency microwave radiation does not penetrate foliage effectively. Rather, it is primarily

absorbed and scattered. It has been shown that the loss through foliage at frequencies at or above S-band is typically unmanageable for a practical radar system. However, *lower frequencies* do penetrate foliage and other media efficiently and offer the possibility of a new approach to this challenging military need. Low-frequency imaging radar offers the potential for dramatic new capabilities on the battlefield. In this paper, we discuss the development of such a radar to detect obstacles concealed behind foliage, as well as to detect surface and buried mines. In both cases, this technology offers the capability to satisfy autonomous navigation system requirements of the U.S. Army's Future Combat System. In addition, support of the Future Force is provided by the ability to "see the currently unseen," such as buried mines, foliage-concealed obstacles, and threats behind walls in urban environments.

2. SIRE RADAR SYSTEM

The radar is an ultra-wideband, impulse-based system. Down-range resolution is provided by the bandwidth of the transmitted monocycle pulse which occupies 300–3000 MHz. Range coverage for this implementation is designed to be 25 meters with an adjustable start point forward of the vehicle. A block diagram of the radar system is shown in figure 1. Since this is a forward-looking radar, normal synthetic aperture approaches to imaging won't work, so a physical aperture using 16 identical receive antennas is used. Each antenna feeds its own "receiver", in this case a base-band digitizing system based on low-cost COTS components. There are four receive channels per data acquisition card (Quad board), and a timing and control card to provide the necessary clock references. Data for all four channels is integrated on each acquisition card and assembled waveforms collected by a master controller. The six in-house designed boards are mounted in a modified VME chassis which provides power and cooling as well as low-speed data bus connectivity. A custom designed P2 backplane board supports critical timing signals. The data from the VME chassis, along with a GPS time tag, are passed to a personal computer (PC) which acts as the operator control and status display. Image processing is done with a back projection algorithm that allows a quick look at the scene ahead. However, radar data is continuously collected so that a horizontal two-dimensional synthetic aperture is formed. This allows off-line focusing of the data with the

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related GPS position information to yield estimates of target height as well as position, to identify potential obstacles as being negative (e.g. holes, ditches) or positive (e.g. tree stumps).

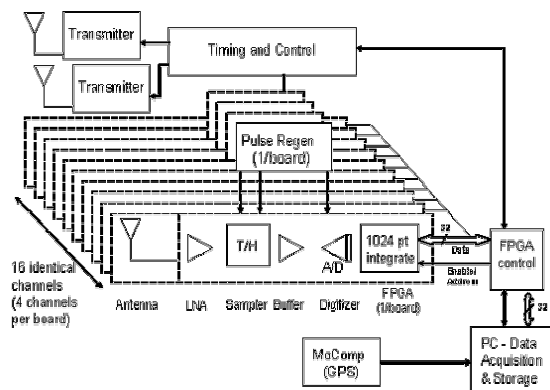


Figure 1. Block Diagram

2.1. Transmitters

The transmitters (fig. 2) are commercial mono-cycle impulse generators with a center frequency of approximately 950 MHz. The occupied bandwidth is 300 – 3000 MHz with an average power across the bandwidth of 5 mW to minimize the interference potential to other spectrum users. This provides just enough signal for the receiver assemblies to function properly.



Figure 2. Impulse Transmitter

2.2. Transmit Antenna

The transmit antennas (fig. 3) are TEM horns similar to those developed for the original ARL UWB synthetic aperture radar [Ressler and McCorkle, 1995, Ondrejka et al.] but reduced in size to better match the pulse spectrum of this radar. This family of antennas was chosen for early experimental stages as they provide good pulse fidelity along boresite and reasonably low reflected power [Robertson and Morgan, 1993, Shlager, et al., 1996]. The antennas are designed for a 200 Ω

characteristic impedance and are fed with an ARL designed 4:1 UWB balun (Patent #5,379,006). The mounting flanges on the antenna cover allow operation in either horizontal or vertical polarization.

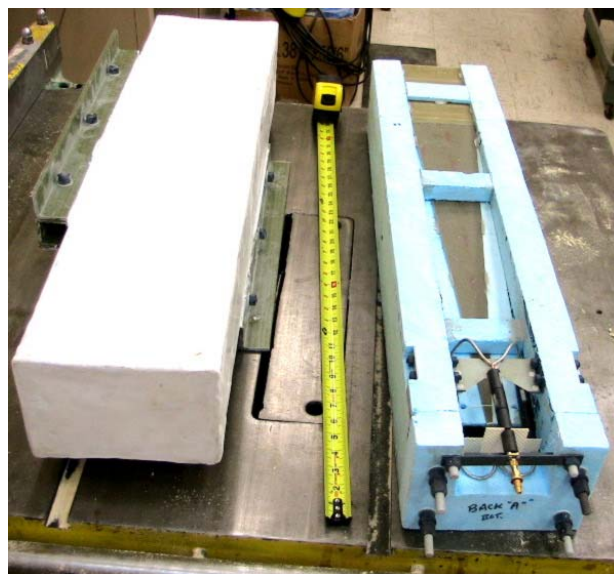


Figure 3. Transmit antenna and outer case

2.3. Receive Antennas

A more compact construction was desired for the receive antennas (fig. 4) to allow spacing antennas closer together (in either polarization) in a linear array. This is done to avoid grating lobes at higher frequencies when focusing the data. There was still a need for some directivity. A number of Vivaldi notch designs of varying sizes and material construction were tested. These are exponential slots at one end coupling the antenna to the incident field with a circular resonator at the other. The antenna feed is coupled through a perpendicular line that is terminated in a radial stub near the resonator. The selected design [Chio and Schaubert, 1999] was constructed from Duroid with a tapered stripline feed system that provides the necessary impedance transformation. SWR is below 3:1 for the 300 – 3000 MHz range.

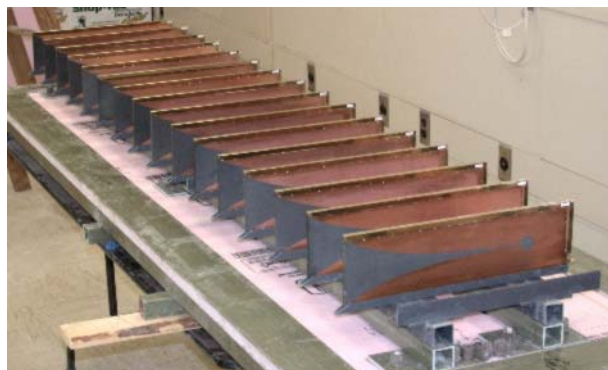


Figure 4. Partially assembled receive array

2.4. Timing and Control

The timing and control board is an ARL designed, six-layer printed circuit board fabricated on FR4 material. It resides in a 6U format, 8-slot VME card cage (fig.5). Figure 6 shows a block diagram of the circuit. Its operation can be described as a microcontroller interface for commands and control and a field programmable gate array (FPGA) for initiating precision radar timing. The microcontroller interface is a Stamp BS2p module which receives serial commands from the PC over an RS232 line. It interprets these commands for the FPGA by enabling up to 5 control lines going to the FPGA. Table 1 shows the list of available commands.

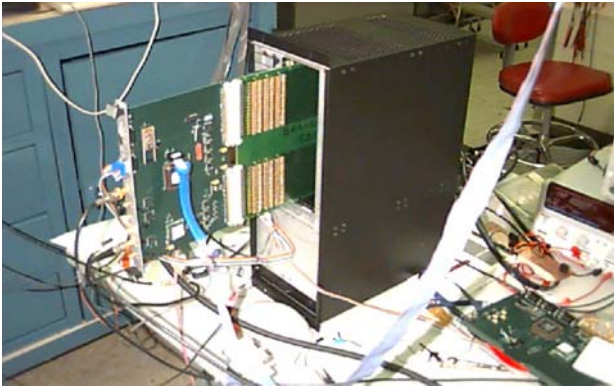


Figure 5. Timing and Control board under test in VME chassis

The heart of the timing circuit is the Altera EMP7160 84 pin FPGA. This device is considered low density (approximately 3000 gates) by today's standards of millions of gates but provides sufficient capacity for programming several complex state machines providing the timing signals.

One function of the FPGA is to trigger the transmitters at a pulse repetition frequency (PRF) of 1 MHz. To do this it provides a 125 ns trigger pulse for either the left transmitter or right transmitter, as determined by the control line from the stamp processor. The trigger pulse is repeated every microsecond to obtain the 1 MHz rate.

The FPGA must also provide a stable clock for sampling the radar return signal at an effective 8 GHz sampling rate. It accomplishes this by dividing down the 160 MHz reference clock to 40 MHz and sends it into a bank of three positive ECL (PECL) delay chips. These delay chips are programmed by the FPGA to provide a fine delay in steps of 130 ps. At each pulse repetition interval (PRI), the delay is incremented by 130 ps until 193 steps are complete. The 193 steps of 130 ps will cover the 25 ns real sampling period (40 MHz), giving the effective sampling rate of approximately 8 GHz. Typically, during the data collection, 1024 samples are taken at each of the fine delays to allow for coherent averaging of the data. Corrections have been designed

into the firmware of the FPGA to compensate for small differences in delay chip characteristics when switching between delay chips. Once the differential delay clock exits the bank of delay chips, it is buffered into four sets, one set per Quad board, and is sent to the P2 backplane. The signals will be used on the Quad boards to clock the track and hold and analog-to-digital converter (ADC).

In addition to the transmit triggers and the delay clock, the timing and control board must send a collect data signal to the Quad boards for synchronizing the Quad board FPGAs to the data taking sequence. A frame signal is sent which lasts for the duration of the data taking sequence consisting of all averaging and all clock delays of a single transmitter. A start accumulate signal is also sent repeatedly during the data taking frame to indicate on what clock cycle a sample should be collected into the Quad board FPGA. It compensates for the delay from the transmit signal's main bang to the desired receive signal's range gate. It also takes into account the 7 clock cycles of delay in the ADC pipeline processor. Initial tests with a fixed delay for the start accumulate showed that false triggerings could occur at the end of the 193 step delays due to the proximity in time of the next clock cycle's edge and the less than ideal signal slew rate. Hence, we added a delay chip into the path of the start accumulate signal to roughly correspond to the delay clock sent to the ADC.

Lastly, a pulse is sent to the Ashtec Z-Surveyor mobile GPS unit at approximately the middle delay in the 193 delay step sequence in order to trigger a time tag. Another Ashtec Z-Surveyor acts as the base station. GPS data is stored on memory cards in each of the units, and differential correction is done off-line. Image formation is done post-processing and uses the time tag to look up the final calculated radar position.

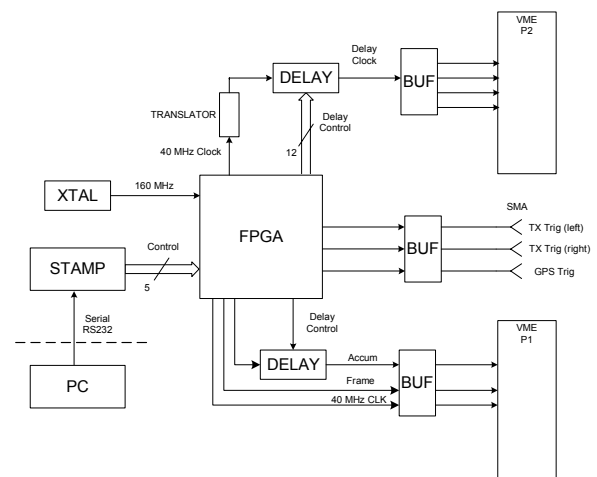


Figure 6. Timing and Control Board

The code for programming the Altera FPGA was written in VHDL using Altera's Quartus II design environment. It allows design entry, compilation, timing simulation and downloading, all in one package.

Command	Action	Radar Mode
00	Turn off Transmitter	Set up
01	Turn on Transmitter	Set up
02	Start collection using left TX with averaging	Normal, Active
03	Start collection using right TX with averaging	Normal, Active
04	Start RFI collection with no averaging	Normal, Passive
06	Start early collection using left TX with averaging	Main Bang BIT

The Quad board functions as the base-band receiver/digitizer and temporary storage of accumulated radar return pulses. ARL designed and laid out the eight-layer printed circuit board which was fabricated on Gtek material. The Gtek material is an improvement over the FR4 material in controlling trace impedances. A block diagram of the circuit is shown in figure 7. We see that there are four channels per board, requiring a total of four Quad boards for operating sixteen receive channels. Each channel consists of an Agilent wideband, low noise amplifier and a Rockwell Scientific dual high speed track and hold module. This is followed by an Analog Devices differential amplifier and an Analog Devices 12-bit 80 MHz ADC. The resultant 12 bits of digital data are applied to a Xilinx Spartan 3 FPGA. A single FPGA of about 400,000 gates will comfortably handle inputs from all four channels and store accumulated data in its internal block RAM. The block RAM operates in a dual port mode, allowing storage of the samples at a 40 MHz rate and clocking the data out of the FPGA at a 20 MHz rate, at the end of a frame. When the PC is ready to receive the data at the end of a frame, handshaking is performed between the PC and a master controller board which in turn will select the Quad boards, one at a time, to dump 32-bit wide, stored data samples onto the backplane. The master board will receive the data, buffer it and send it to the PC along with a synchronous 20 MHz data clock. Each Quad board will provide the PC with more than 5,400 samples of accumulated data per frame at a rate of about 3 frames per second. Each frame

Notable features of the Quad board design include 50-ohm impedance matching throughout the front end to minimize signal reflections and maintain sharp clock transitions and include equalized trace lengths (propagation delays) at the corresponding points across all four channels. Also, sub-nanosecond timing adjustments can be made on each board to maintain a desired relationship between the clocks for the two-stage track and hold module and the clock for the ADC. The adjustments are made with dip switches controlling PECL delay chips. One feature added for engineers debugging the data path without the aid of the PC is a 12-bit DAC for each channel. The reconstituted, sampled analog signal can be observed on an oscilloscope connected to an SMA output connector. Not shown in the block diagram is a flexible serial interface between Quad board FPGA's, master controller board FPGA and the PC. Using this interface, the PC can send reconfiguration commands to the FPGA's to accept a new number of step delays, pulses for averaging or samples per PRI, as often as each data collection frame.

1 of 4 Channels/Board

The diagram illustrates the architecture of the 1 of 4 Channels/Board. It features a signal path starting with a radar return, passing through an LNA (21 dB gain), a T/H block, a DIFF AMP (x2 gain), and a 12-bit ADC. The ADC outputs 12-bit ADC Data and is clocked by an ADC Clock. A DAC is also clocked by the ADC Clock and receives 12-bit data from the ADC. The T/H block is clocked by 4 T/H Clocks from a LOGIC block. The LOGIC block is connected to a DELAY block, which is in turn connected to a Dip SW. The BUF block is connected to the ADC Clock and the DELAY block. The BUF block is also connected to a DELAY block, which is connected to a Dip SW. The ADC CLK is connected to the FPGA. The FPGA receives 12-bit ADC1 Data, 12-bit ADC2 Data, 12-bit ADC3 Data, and 12-bit ADC4 Data. The FPGA outputs 32-bit Data to a BUF block, which is connected to a VME P1 interface. The BUF block also outputs 32-bit Data to a VME P2 interface. The VME P2 interface has request, ack, and enable signals. The VME P1 interface has ACCUM, FRAME, Data Out CLK, and FPGA CLK signals.

Figure 7 Quad Board Block Diagram

2.6. The Data Acquisition and Radar Control System

In this section we will briefly describe the computer that controls the radar operations. The hardware and software have been designed to satisfy the objectives of cost, migration, and transition. We employ a generic PCI bus computer that runs Windows XP operating system. The radar control software is written using open ANSI C programming language. It uses the National Instrument LabWindows/CVI real-time supporting libraries for the graphical user interface and multithreading. The main functions of the computer are: 1) interfacing with the timing and control (T/C) module, 2) interfacing with the Master FPGA module in the VME chassis, 3) interfacing with the GPS receiver, 4) acquiring digital radar data via the National Instrument 6534 high speed PCI data acquisition board, 5) streaming radar and GPS time tags onto the data storage device, 6) synchronizing all radar components, and 7) providing a graphical user interface to the radar operator.

Figure 8 shows that the software is partitioned into multiple threads: data acquisition thread, data archiving thread, graphical user interface thread, etc. The operating system can divide processing time on these threads so that they can run much more efficiently in parallel. For example, while the computer is waiting for the data acquisition cycle to complete by the data acquisition thread, the user interface thread can update plots of radar data and images on the screen, and the data archiving thread can stream previous data to data storage device.

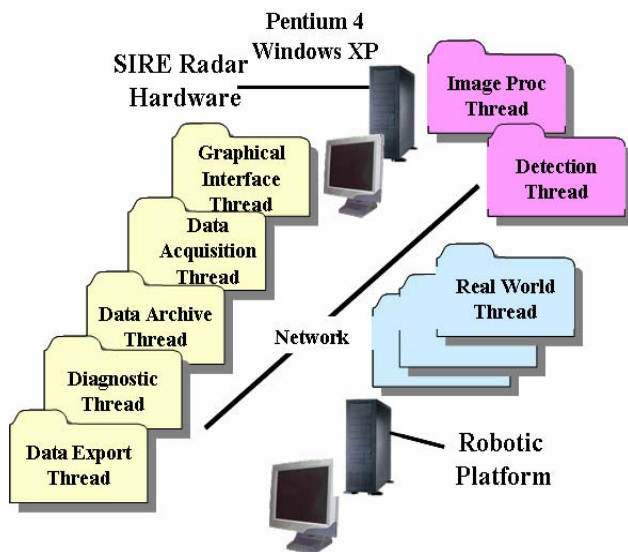


Figure 8. Partition of Software Threads

This approach offers several advantages. First, a single complicated problem can be divided into several simpler problems that cooperate to accomplish the requirements. Software feature can be extended by adding new threads instead of modifying existing codes. This multithreading approach will enable the system to

respond quickly to any event and provide services for the events within timing requirement. This also maximizes the CPU utilization since only threads that demand services will be granted sufficient CPU time. While multithreading offers many advantages on a single processor computer, it is absolutely necessary on a multiple processor computer.

As we mentioned above, the software has been designed to satisfy migration and transition. Our vision is that in the future the radar should be transitioned and integrated to the unmanned navigation system. Information from the UWB sensor such as SAR imagery, detected target locations are sent to the perception functions of the robotic platform. Radar processing functions such as image processing and target detection could reside on either platform.

The radar software operation can be summarized as follows. First, the computer sends commands to set up the FPGA acquisition module for a data acquisition cycle. It then sends commands to the timing and control module to start transmitting radar pulses using the left transmitter. The FPGA acquisition modules digitize, integrate, and interleave return radar signals. The digitized data from all 16 receivers are then packaged and send to the National Instrument high speed parallel board that interfaces with the host computer via the PCI bus. The time tag information from GPS receiver is also sent to the computer during this data acquisition cycle [Wong et al., 2003]. After the data for all 16 channels are digitized and integrated, the processing thread receives the data and performs tasks such as scaling, removing DC offset, converting to frequency domain, etc. and sends the processed data to the graphical user interface thread for presentation and also to the data archiving thread for data recording. After this, the data acquisition cycle repeats with the right transmitter.

Figure 9 shows the radar operator's main display/control panel. The x-y plot on the main panel shows the acquired data for a single receiving channel. This shows the signal level versus range (bottom x axis) or time (top x axis). The user can select which transmitter (left or right) and which receiving channel to display. The user can also select another option that automatically scans though all the channels and displays each of them in a different color. This feature allows the user to identify any bad receiving channel. Within the plot area, there are two cross-hair cursors that serve as a measuring tool. Each cursor indicates the x and y value of the data record at the location it points to. The display also indicates the x and y distances of the two cursor. This helps the user to measure the signal level as well as the ranges of targets of interest. The user can also zoom-in to examine a region of the plot defined by rectangular area forming by the two cursors.

Also in Figure 9, a separate window on the left side of the radar main control panel displays the radar phase history data as an image. Although this is not a focused

image (targets cannot be resolved in cross-range), it can show the targets' responses and their current ranges with respect to the radar.

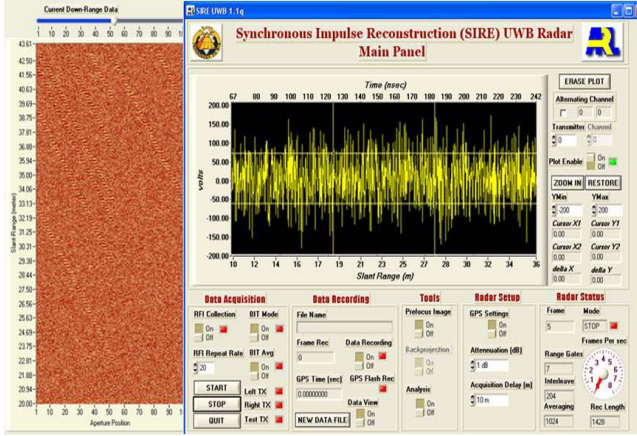


Figure 9. Main Operator Display

Figure 10 shows another window that displays more useful information. The false color plot on the right of Figure 10 displays the data for all 16 channels. This provides the user with a quick snapshot of the data quality across all channels. Using the upper plot window on the left of Figure 10, the user can select any two receiving channels and compare them in time domain. The frequency domain plots of the two selected channels are automatically computed and plotted on the second plot window. If the input signal to the system is a pure sinusoidal waveform, the software estimates its frequency and displays both the frequency responses of the reconstructed input waveform versus the theoretical sinusoidal one. This feature is particular helpful for our design engineers to fine-tune the radar acquisition timing so that the frequency response of the reconstructed input sinusoidal waveform closely match to that of the theoretical one.

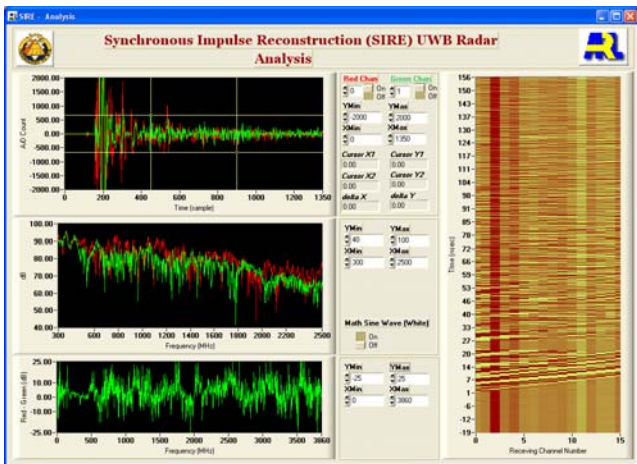


Figure 10. Another user interface panel

3. Configuration of Transmitter/Receiver Array Versus Cross-Range Resolution

The down-range resolution is a function of the signal bandwidth ($\Delta_r = \frac{c}{2B}$) where c is the speed of light and B is the bandwidth of the radar signal. For the forward-looking radar, we are more concerned with the cross-range resolution since we cannot generate a synthetic aperture in this direction. Thus, we have to construct a physical array of receivers in order to form a cross-range aperture. We have conducted a study to provide us with insights to configure our transmitter/receiver array to achieve a good cross-range resolution while minimizing the transmitting elements. In this work, we developed an analytical model that allows us to map the imaging geometry that consists of the locations of transmitters, receivers, and target into the spatial frequency domain [Nguyen and Soumekh, 2006]. This information gives us some insights to efficiently configure our transmitter/receiver array.

In this section, we present several simulation cases that correspond to the monostatic and some variations of bistatic configurations and compare the corresponding cross-range resolution. For each case, we generate a simulated range profile database and form the corresponding image using the backprojection algorithm [McCorkle and Nguyen, 1994]. We then compare the resolution of the point target from the images of various cases.

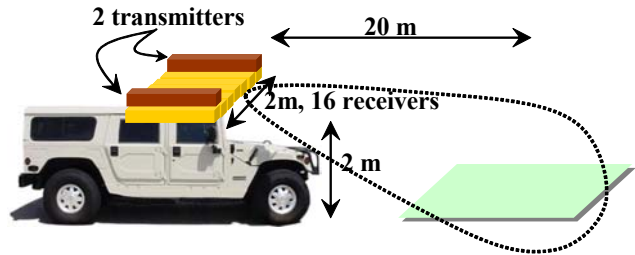


Figure 11. Typical imaging geometry implemented in ARL system

Figure 11 shows a typical forward imaging geometry. In our configuration, the aperture is constrained by the width of the vehicle, which is 2 m. Within the aperture size constraint, we can stack 16 receiving antennas. The height of the radar is 2m. The imaging area includes 5 point targets. The imaging center is located at 20 m from the radar. Later in this section we will compare target resolutions using imaging centers at various ranges. In this study, we only form imagery using a fixed range and thus the motion of the vehicle is not exploited. In practice, however, we form imagery using the physical aperture of the antenna array and the synthetic aperture (SAR) generated by the forward motion of the vehicle. This two-

dimensional aperture will give us not only the cross-range resolution (from physical aperture of the antenna array) but also the height resolution (from the forward motion) and thus results in a 3-dimensional image [Nguyen, et al., 2003a, Nguyen, et al., 2003b]. This approach also provides more integration to achieve a better signal-to-noise ratio in the resulting image. In this study, we are only concerned with the cross-range resolution of the target with respect to transmitter/receiver configurations and imaging geometry and thus the two-dimensional SAR image is sufficient. We have four simulation cases. The first simulation case is the bistatic configuration in which there is only 1 transmitter located at the middle of the receiving array of 16 elements. The second simulation case is the same as the first case except that the transmitter is located at one end of the receiving array. In the third simulation case, there are two transmitters and each one is located at one end of the receiving array. The fourth simulation case is the monostatic configuration with 16 transmitters and 16 receivers. Figure 12 shows the resulting backprojection images of the four simulation cases. In the bistatic cases with one transmitter (case 1 and 2), the target's cross-range resolution is the same for each case and worse than that from the monostatic case and the bistatic case with two transmitters (case 3 and case 4). In the latter two cases, the target's cross-range resolution is the same, which is about 1.2 m at 20 m range from the radar. Note that this is the cross-range resolution for a target at broadside to the receive array. For squinted targets, the cross-range resolution will get worse.

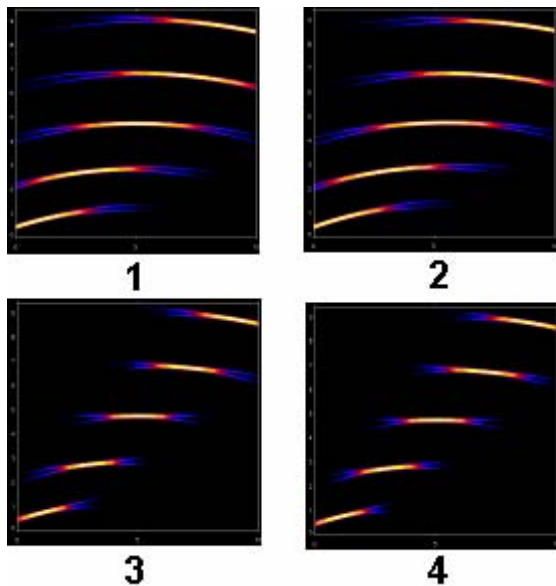


Figure 12. SAR images of five simulated targets using various configurations: 1) 1 transmitter at the middle of receiving array, 2) one transmitter at the end of the receiving array, 3) monostatic with 16 transmitters

and 16 receivers, 4) two transmitters at both ends of the array

The configuration of case 4 (two transmitters located at the ends of the receiver array) is implemented in our forward looking radar, giving us the best resolution while reducing the cost and complexity in our design.

We repeat the simulation with the bistatic configuration (with transmitters at both ends of the antenna array) using various ranges from radar to target. Figure 13 shows the cross-range resolution as a function of distance from radar to target.

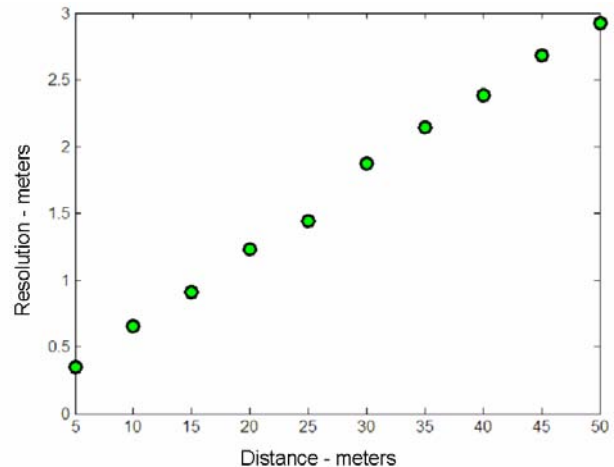


Figure 13. Cross-range resolution for a point target as a function of distance from radar to target

CONCLUSIONS

Initial testing of the radar system will be done using a Ford Expedition as the mobile platform (fig 14). The vehicle has an onboard 110 VAC system that can be operated from batteries if needed and an antenna support structure that will allow positioning the antenna at various locations with respect to the roof and front of the vehicle.



Figure 14. Early SIRE radar test configuration

Integrated radar data from all 16 channels will be collected and stored onboard the PC system with 3-D focusing of the data taking place offline. The differential GPS system will provide the positioning information needed to allow the data to be focused in a known coordinate system. This radar offers the capability to satisfy autonomous navigation system requirements of the FCS as well as providing the ability to see buried mines, foliage-concealed obstacles, and threats behind walls in urban environments. Its COTS-based design is modular in concept and provides a simple means to upgrading performance or number of receive channels. A simplified single channel version might be appropriate for a small UAV where data processing would be done at the ground station.

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