

A COTS-Based Replacement Strategy for Aging Avionics Computers

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This article describes a commercial off-the-shelf (COTS)-based form, fit, function, and interface replacement strategy for legacy avionics computers and embedded information systems that can reuse existing software code as is while providing a flexible framework for incremental upgrades and managed change. It is based on a real-time embedded software technology that executes legacy binary code on the latest generation COTS microprocessors. This scaleable technology, developed by TRW and sponsored in part by the Air Force Research Laboratory, demonstrates performance improvements of five to 20 times that of the legacy avionics computer that it replaces. It also promises a four-fold decrease in cost and schedule over rewriting the code, and provides a known, good starting point for incremental upgrades of the embedded flight software. Code revalidation cost and risk are minimized since the structure of the embedded code is not changed, allowing the replacement computer to be retested at the black-box level using existing qualification tests.

Military aircraft are active years longer than originally anticipated. The avionics computers on these aging aircraft are expensive to maintain due to parts obsolescence, and require additional processing and memory to handle changing requirements. As a result, old computer hardware needs to be replaced with newer, more capable microprocessor technology. However, incompatibility issues require that embedded software be rewritten. It is estimated that billions of upgrade-dollars could be saved if new computers could execute the old embedded code along with any new code to be added.

TRW has developed a generic commercial off-the-shelf (COTS)-based software technology called Reconfigurable Processor for Legacy Avionics Code Execution (RePLACE) that capitalizes on technology advances to eliminate costs associated with rewriting legacy software to execute on new hardware. This software allows a user to 1) replace obsolete computers with commercial processor-based hardware, 2) continue to use existing

operational flight plan (OFP) without modification, and 3) incrementally upgrade hardware and software to support new and modified capabilities. RePLACE COTS software allows Department of Defense (DoD) dollars to be spent on solving supportability and performance problems and adding new needed capabilities, rather than recapturing current capabilities in new hardware.

Figure 1 depicts using the COTS software to migrate from a current legacy avionics line-replaceable unit (LRU) to a new COTS-based replacement box (CRB). Typically, today's legacy avionics and embedded information systems are based on custom hardware and proprietary back-planes with an obsolete 16-bit instruction set. Little or no "modern" higher order language (HOL) support is available to support software for this equipment. In addition, these legacy systems are often limited in terms of throughput and memory.

A COTS-based, open-systems replacement strategy provides a low cost of entry strategy for COTS microprocessor tech-

nology insertion. Both the legacy instruction set architecture (ISA) as well as the new native ISA can be executed. Native code execution is supported by advanced HOLs such as Ada95 and C++. In addition, legacy code can execute much faster in the new hardware and utilize more memory than is available for needed upgrades.

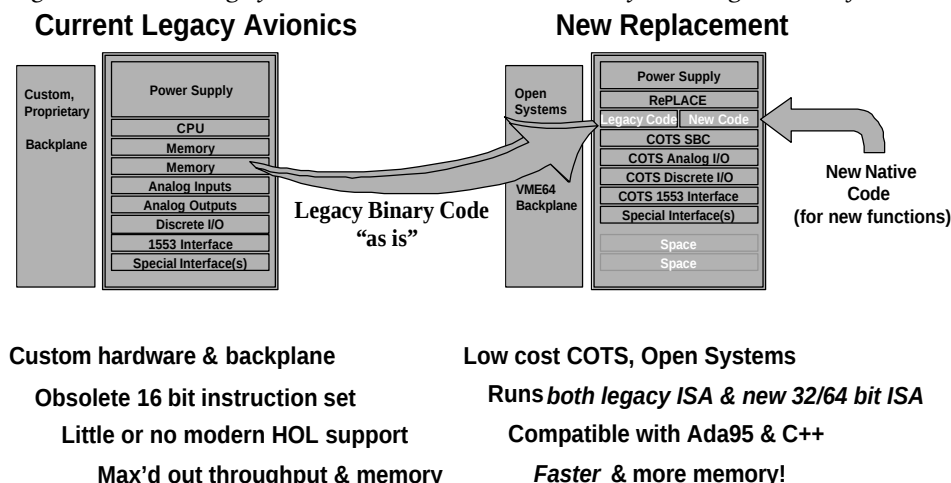
A software perspective of RePLACE is illustrated in Figure 2. Sitting on top of the COTS microprocessor and Portable Operating System Interface (POSIX)-compliant real-time operation system (RTOS) are two virtual machines: the legacy virtual machine and the native virtual machine. Within the legacy virtual machine space are four key software components: the legacy instruction set engine, the legacy OFP code binary image, the input/output (I/O) mapping software, and the virtual component environment (VCE).

The legacy instruction set engine contains unique cache-optimized code developed by TRW to execute the legacy binary OFP code. The I/O mapping software maps the new COTS interface devices to the legacy interface devices. The VCE allows for the efficient transition between the native and legacy virtual environments allowing the transfer of data and concurrent execution of both legacy and new native code.

The key features may be summarized as follows:

- Relies on using state-of-the-art COTS microprocessors and open system standards that improve both the legacy system's producibility and supportability.
- Runs legacy code from five to 20 times faster than the original legacy system by using a unique cache-optimized approach. This provides extra comput-

Figure 1: Current Legacy Avionics to a New COTS-Based by Utilizing COTS Software



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ing power for new functions. In addition, the performance of the legacy virtual machine is linearly scaleable with the performance of the COTS microprocessor technology that is being used. That is, as the internal clock speed of the microprocessor chip goes up, the legacy instruction/execution speed increases linearly.

- Makes the instruction set engine adaptable to diverse instruction set architectures, including, for example, MIL-STD-1750A, Z-8002, and AN/AYK-14A. This makes possible the replacement of multiple diverse legacy avionics LRUs with a common set of avionics hardware modules on a given platform or across different platforms.
- Provides I/O mapping software that exactly matches the new I/O COTS devices to the legacy I/O devices, providing a *drop-in* environment for the unmodified legacy OFP with little or no knowledge required of the original code.
- Executes both legacy and new native software concurrently in separate virtual spaces. This promotes incremental addition of new capabilities and gradual transition to new code.
- Provides instruction execution speed matching that can be initiated in critical sections of the OFP to provide legacy OFP timing adjustments for timing sensitive code.
- Allows practical real-time non-intrusive (RTNI) monitoring of legacy software built into the replacement avionics, dramatically enhancing the observability and testability of the embedded legacy software.

In order to illustrate the concurrent execution of legacy and native code in a RePLACE dual instruction set computer (DISC) environment, Figure 3 depicts the legacy code remaining in control while new software enhancements are introduced. On the far left are two time-lines showing the various rate groups processing tasks running in the legacy machine and in the CRB.

In the case of the CRB, the original rate groups are executed in a much shorter time frame within any given minor cycle. This leaves additional processor throughput at the end of each minor cycle to add new software running in the native ISA. Through the VCE context switch mechanism, referred to as a *thunk*, new native code can be introduced to replace existing legacy code or added to the existing legacy code.

Alternately, event flags can be set to augment the legacy code thread as illus-

trated. Note that legacy instruction execution speed matching can also be introduced for timing-sensitive code. In addition, the technology includes the capability to disable legacy code outputs without legacy OFP cognizance, providing a convenient mechanism to switch off functions in the legacy code without being intimately familiar with the legacy code structure. In all cases, the original legacy binary OFP code remains intact with *no* changes.

Another key component of the COTS software strategy is the availability of a source level, symbolic user console for system developers. A tool has been developed to facilitate the use of RePLACE in modern microprocessor technologies and is referred to as the virtual integration environment workstation, or VIEWstation. It is tightly integrated with the COTS native code integrated development environment and commercial tools that are selected to support new native code development.

VIEWstation is loosely integrated with the legacy code tools. It provides a source level, symbolic configurator tool to assist the software developers in mixing and matching legacy and native code; it also provides in-target debugging and RTNI monitoring of the legacy code. VIEWstation incorporates COTS graphical data analysis tools and an interactive symbol browser/editor. Examples of VIEWstation use include downloading and disassembling software binaries, displaying real-time debug and monitoring data, performing and displaying timing

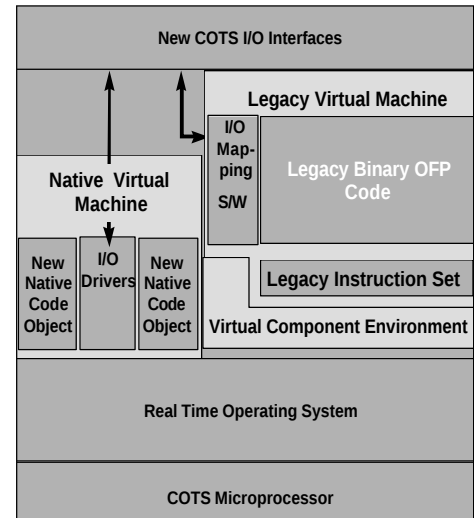


Figure 2: A Software Perspective of RePlace

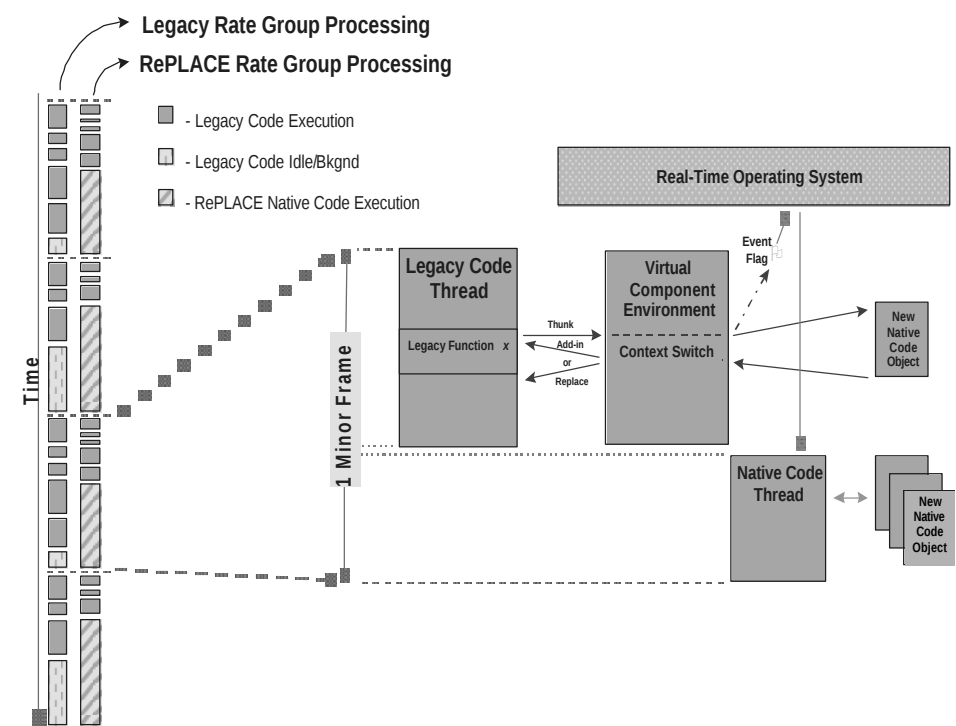
characteristics, creating and deleting events, and developing *add-in* code that is executed in response to specific user-specified events in the legacy code.

Results

Demonstrations of RePLACE executing legacy binary OFPs have been conducted in conjunction with AFRL for the following DoD aircraft subsystems:

- F-16 Heads-Up Display.
- F-16 Advanced Central Interface Unit (stores management processor).
- F-16 General Avionics Computer (fire control computer).
- AC-130H Gunship Mission Computer (SKC-3007A).
- C-17 Communication Control Unit.

Figure 3: New Software Enhancements Introduced to Legacy Code



- MH-60K Mission Computer (AP-102A).
- F-117 Mission Computer (AP-102A).

Comparisons of various alternatives to software adaptation are shown in Figure 4. The non-recurring costs for OFP development are, as would be expected, much higher for the case of an OFP rewrite. To a lesser extent, but still significant are the costs associated with an OFP rehost. This is because a rehost activity must still

Code revalidation costs are significant for all three approaches. However, these costs are minimized with RePLACE since the structure of the embedded code is not changed, allowing the replacement computer to be retested at the black-box level using the existing functional qualification tests. TRW has developed a set of analytical tools to support this type of tradeoff for different user scenarios.

Potential upgrade strategies using the COTS software cover a wide spectrum of upgrade possibilities. These include the introduction of a new ruggedized COTS replacement box for an existing legacy avionics LRU. It also includes the introduction of a new microprocessor replacement module for insertion into an existing avionics LRU. Finally, included is a tool to mitigate the inherent risks associated with introducing both new hardware and software into a platform at the same time.

Figure 5 illustrates determining the baseline of new COTS-based hardware with the legacy OFP as a first step in the process of adding new functionality into an existing platform. Tailoring the

The validation steps include validating the execution of the ISA within the new microprocessor, validating the I/O characteristics using the new microprocessor, and integrating and running acceptance tests of the legacy OFP with the new hardware.

RePLACE technology offers the DoD customer significant supportability, producibility, and performance improvements through the introduction of COTS-based state-of-the-art hardware; it maintains backward compatibility with existing OFPs while providing the means to affordably migrate to state-of-the-art hardware and software technology. The result is significant cost savings, substantial risk reduction, and incremental upgrade opportunities for future enhancements. It also requires no custom hardware – it is an embedded software technology that leverages off the latest in commercial processor technology.

The engine can be supplied with a turnkey lab-quality or ruggedized box, or with a set of open system COTS board-level products. Also, PC-based configuration, control, and monitoring software is available to provide setup, maintenance, and user interaction with the engine. Although conceived for on-board avionics computer replacement strategies, it is equally effective to other embedded computer applications such as command and control systems, automated test equipment, weapon system trainers, and integrated support environments. ♦

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graph LR
    subgraph Main_Flow [Main Integration Process]
        V1[Validate ISA w/ new COTS Hardware] --> D[Develop I/O Software]
        D --> V2[Validate DISC I/O w/ new Hardware]
        V2 --> I[Integrate Legacy OFP w/ new Hardware]
        I --> A[Acceptance Test Legacy OFP w/ new Hardware]
        A --> FT[Flight Test]
    end

    subgraph Inputs [Inputs]
        LITP[Legacy ISA Test Programs] --> V1
        NCH[New COTS Hardware] --> V1
        UC[User Console] --> V1
        LSTPT[Legacy System Performance Test Program] --> V2
        EIOTJ[Existing I/O Test Jig] --> V2
        LOFP[Legacy OFP] --> I
        EOFT[Existing OFP Test Environment] --> I
        FQTATP[FQT Acceptance Test Program] --> A
    end

    subgraph Demos [Demo Stages]
        ID[ISA DEMO]
        IOD[I/O DEMO]
        LOFD[Legacy OFP DEMO]
        ID --> IOD
        IOD --> LOFD
    end

    V1 --> ID
    V2 --> IOD
    A --> LOFD

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FCW.com

www.wargaming.net/Programming/69/Reengineering_index.htm

This is the Web site for Federal Computer Week magazine. Federal Computer Week is produced with emphasis on desktop, client/server, and enterprise-wide computing. A site search for Federal Computer Week turned up 226 results for legacy systems and legacy software articles.

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Reengineering

www.wargaming.net/Programming/69/Reengineering_index.htm

This Web site features a list of reengineering books along with links for additional information on the publication. Topics include workflow reengineering, analyzing outsourcing, building enterprise information architectures, systems information reengineering, reengineering software, and more.

The RENAISSANCE Web

www.comp.lancs.ac.uk/projects/RenaissanceWeb/index.html

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