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Sep 2008

S-MMICs: Sub-mm-wave Transistors and Integrated Circuits

Program Final Report, submitted to

Army Research Lab BAA DAAD19-03-R-0017
Research area 2.35: RF devices---Dr. Alfred Hung

Submitted by:

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Executive Summary

Transistor and power amplifier IC technology was developed under UCSB for the DARPA SWIFT program. SWIFT seeks to develop sub-mm-wave transistors and ICs to support 340 GHz-band imaging and radar systems. By program end, HBT power-gain cutoff frequencies were increased to 880 GHz, simultaneous with a ~5 V breakdown voltage. HBT layer structure designs and process flows, and initial 340 GHz power amplifier designs developed at UCSB were transferred to Teledyne Scientific. Teledyne Scientific then fabricated both transistors and ICs under the financial support of a separate DARPA program; results at TSC include a 2 mW power amplifier at 340 GHz.

Device technology development at UCSB included a number of significant accomplishments supporting the future development of sub-mm-wave transistors and integrated circuits, including all-dry-etched processes for reliable formation of ~128 nm feature size transistor emitters and ultra low resistivity contacts for the emitter and base contacts. These several features are critical in enabling transistor bandwidths to extend to the low THz regime.

Program Goals

S-MMIC Milestones				
Metric/Milestone	Unit	Program start March 1, 2006	Intermediate objective Q4 December 31, 2006	Phase 1 G/NG milestones Q7 December 31, 2007
Transistor				
scaling generation (emitter size)	nm	500	250	125
current-gain cutoff frequency ft	GHz	450	500	700
power-gain cutoff frequency fmax	GHz	490	700	1100
common base breakdown BVCBO	V	3.5	3.5	2.1
Monolithic Amplifier				
operation frequency	GHz	176	340 +/- 40	340 +/- 20
output power	mW	7.4	5	50
gain	dB	5	5	14
bandwidth	%	5	5	5
power-added efficiency	%	5	3	5
phase noise at 100 Hz offset	dBc/Hz	N/A	-38	-38

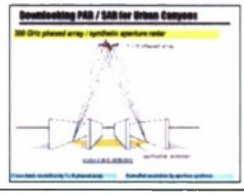


Figure 1: SWIFT Program Goals; technology for downlooking UAV radar.

Motivation / application

Sub-mm-wave systems in the 340 GHz-1000 GHz frequency range will support short-range to moderate range and high-resolution radar and imaging systems. The candidate system application (Figure 1) is a downlooking radar system for UAVs. The radar is in the form of a linear array arranged perpendicular to the UAV's direction of motion. Imaging of the ground in the direction of UAV motion is by standard aperture synthesis using the Doppler shift, while resolution of the ground in the direction perpendicular to UAV motion is using phased-array techniques. By using very short wavelength (sub-mm-wave radiation at 340 GHz), a round resolution of order 10 cm can be obtained with a ~ 10 meter array baseline (the UAV wingspan) with the UAV flying 1 km above the ground.

From these initial system specifications, and from a signal-noise ratio analysis, a UAV - based ground imaging system will be feasible given transmitter output power of order 50 mW/module (power-combining to be used between modules) and a receiver noise figure of order 5 dB.

In this particular program, a contract to UCSB under DARPA's SWIFT program, UCSB was contracted to develop base electronics technology for the 340 GHz transmitter , and hence the 18 month program goals were to develop a 340 GHz power amplifier with 50 mW output power. To obtain such circuit performance, wideband transistors are required; device development goals under the program therefore consisted of a 500 GHz

f_τ , 700 GHz f_{max} HBT at the 250 nm scaling generation, with a target date of Dec. 31, 2006, and of a 700 GHz f_τ , 1100 GHz f_{max} HBT at the 125 nm scaling generation, with a target date of Dec. 31, 2007, the phase 1 program end date.

Technology Status

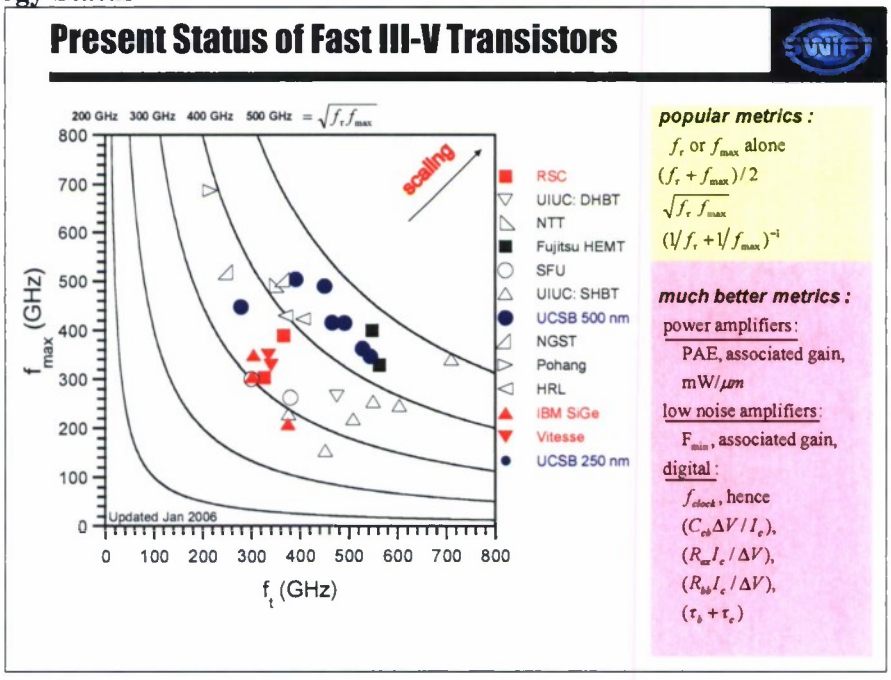


Figure 2: HBT Performance at Program Start, January 2006

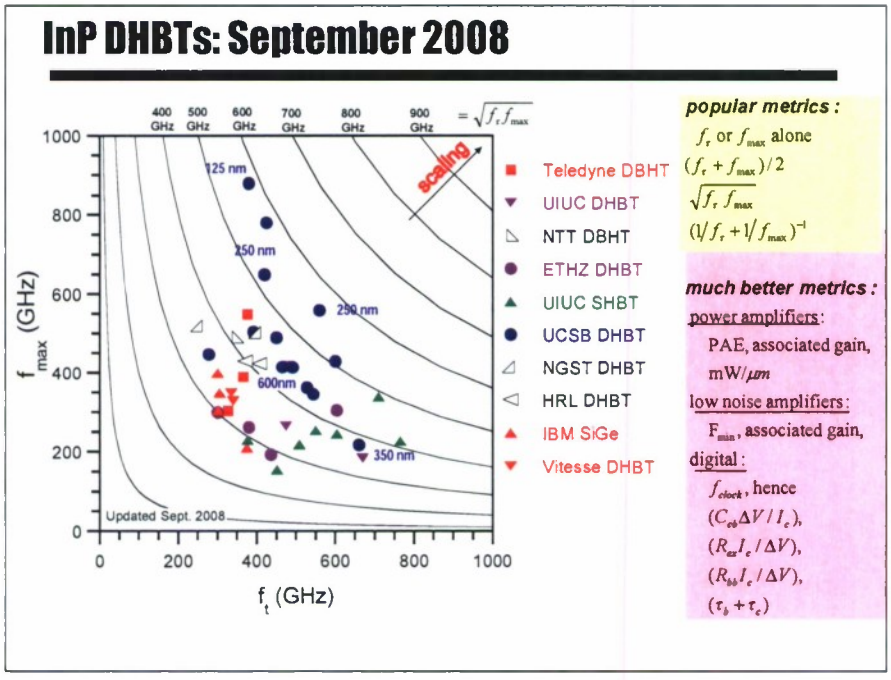


Figure 3: HBT Performance at final program review, September 2008. Note the change in ft, fmax axes.

Figure 2 and Figure 3 compare the performance of HBTs over the period January 2006 to September 2008. In this period, the HBT f_{max} has been increased from 500 to 900 GHz.

Transistor scaling laws

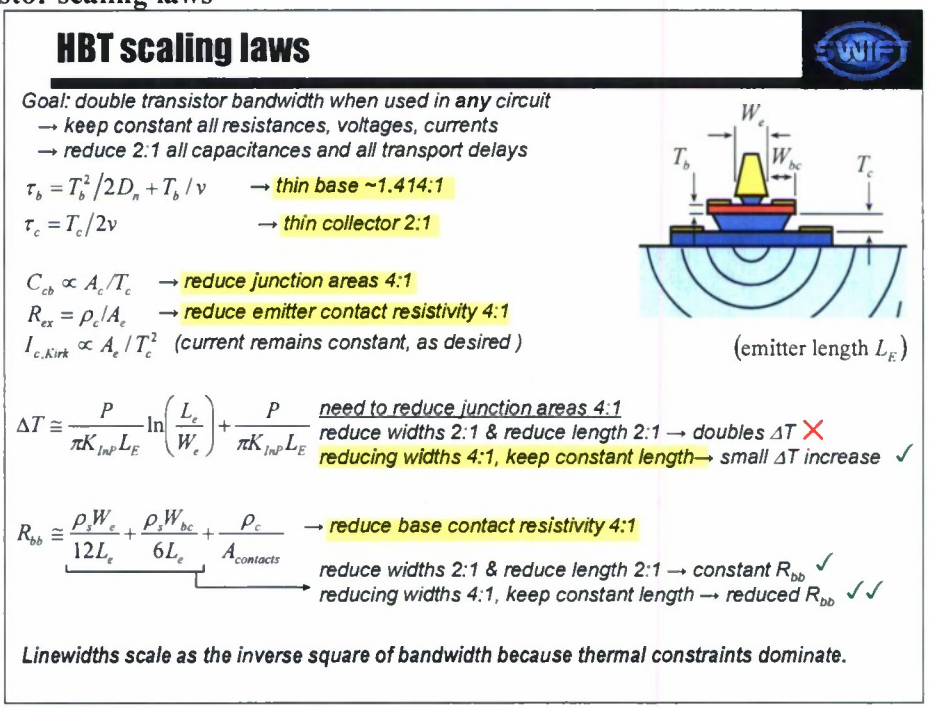


Figure 4: HBT Scaling Laws

Figure 4 illustrates HBT scaling laws. For each 2:1 increase in device bandwidth the collector layer must be thinned 2:1, the lithographic dimensions reduced 4:1, the current density increased 4:1 and the resistivities of the Ohmic contacts reduced 4:1. In addition to the challenges in developing fabrication processes which permit this rapid reduction in device dimensions, the underlying challenges are in the great difficulties faced in producing very low resistivity contracts, and in the difficulties faced in managing self-heating at such high current densities. Developed from the scaling laws of Figure 4, Figure 5 shows a scaling roadmap for mixed-signal HBTs. For sub-mm-wave HBTs such as needed in the SWIFT program, the scaling roadmap is similar except that collect thicknesses ~1.5:1 larger are employed, as this somewhat increases HBT f_{max}, albeit at some sacrifice in digital speed.

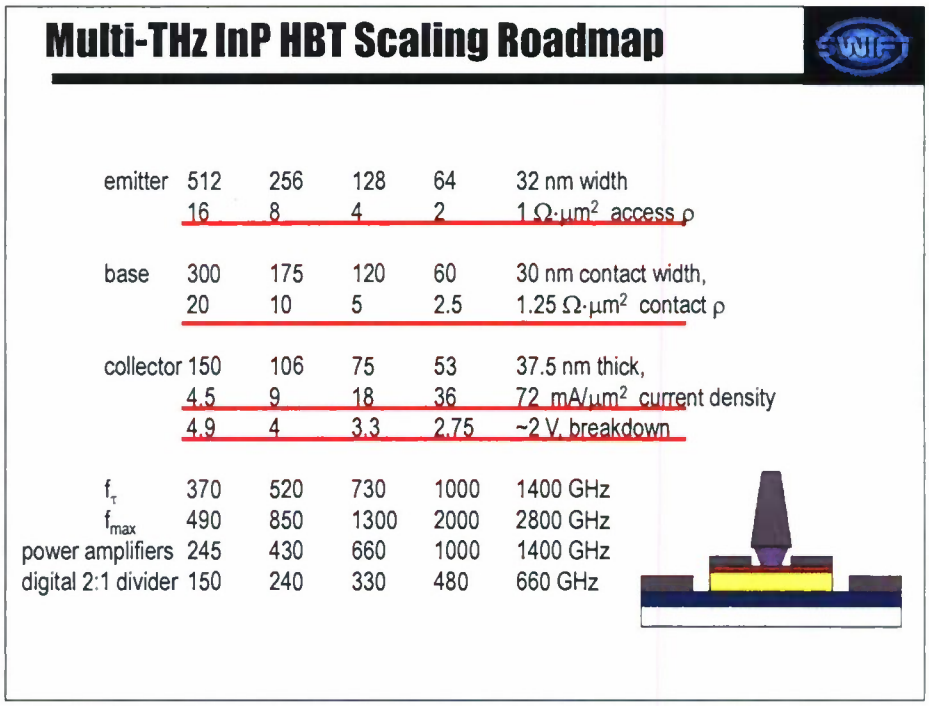


Figure 5 HBT Scaling Roadmap

256 nm generation

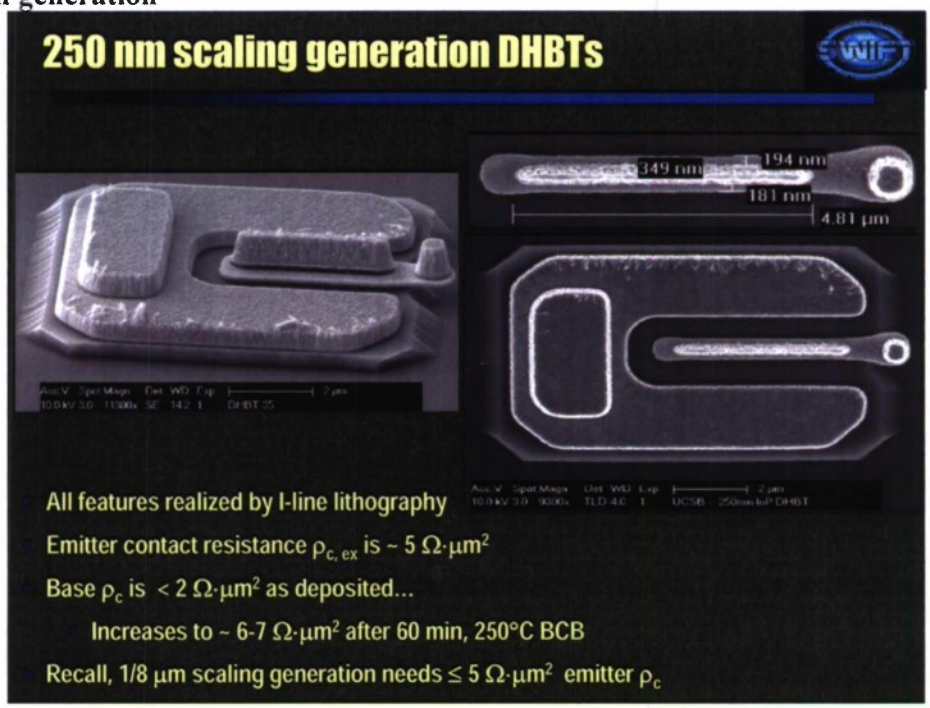


Figure 6: SEM Images of HBTs fabricated under SWIFT; 256 nm scaling generation.

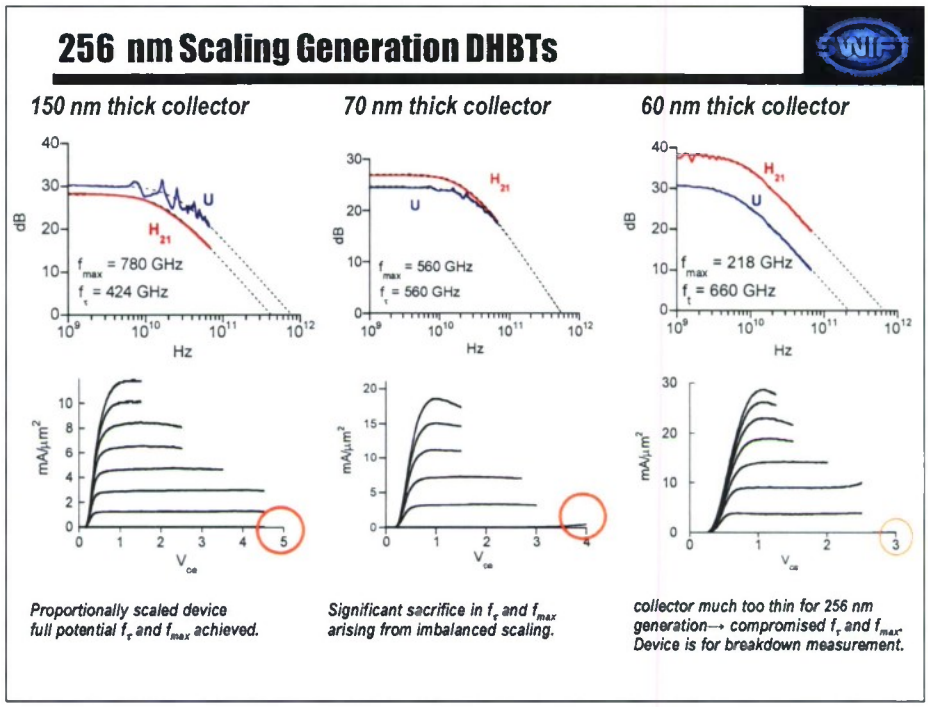


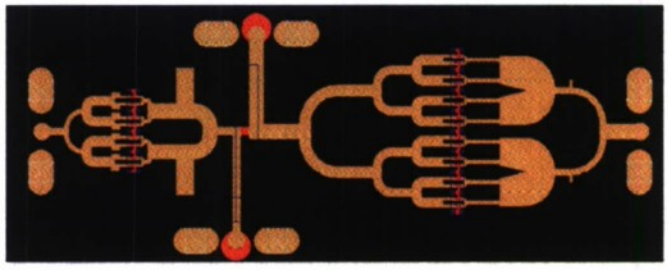
Figure 7: RF and DC parameters of HBTs at the 256 nm generation.

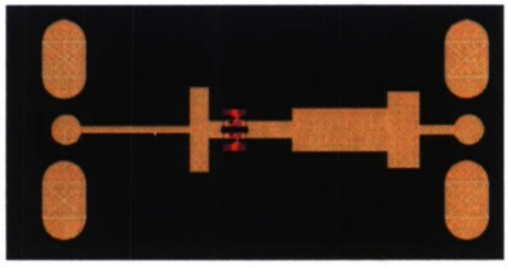
During the first 9 months of effort under SWIFT, HBTs were fabricated using standard mesa processes (Figure 6). Junction dimensions were reduced, epitaxial layers were made thinner, and contact resistivities were decreased. The results (Figure 7) included devices at 150 nm collector thickness with 780 GHz $f_{\max}$ and devices with 60 nm collector thickness showing 660 GHz f_τ .

HBT power amplifier development

Subsequent to the development of the 780 GHz $f_{\max}$ HBT at UCSB, power amplifier design was initiated. Mask designs included (Figure 8) versions of up to 60 mW saturated output power. These designs were not successfully fabricated at UCSB. Both IC designs and HBT process flows for the 256 nm scaling generation were therefore transferred from UCSB to Teledyne Scientific and Imaging Inc. (TSC), who subsequently fabricated lower-power versions of the design (Figure 9). An output power of 2 mW was obtained in a single-HBT design.

UCSB Amplifier Designs





- *8 to 16 finger two-stage design*
- *2 finger single-stage design*
- *Shown with large pad structures used for S-parameter measurements*
- *Two-stage design yields ~60 mW*
- *Small signal amp gives 7.2 dB*

Figure 8: Mask Layouts of 340 GHz power amplifiers designed at UCSB

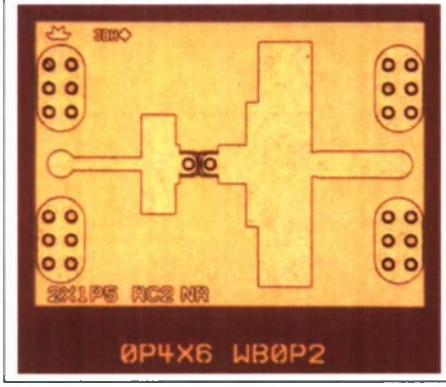
324 GHz Medium Power Amplifiers in 256 nm HBT

ICs designed by Jon Hacker / Teledyne

Teledyne 256 nm process flow-

Hacker et al, 2008 IEEE MTT-S

~2 mW saturated output power



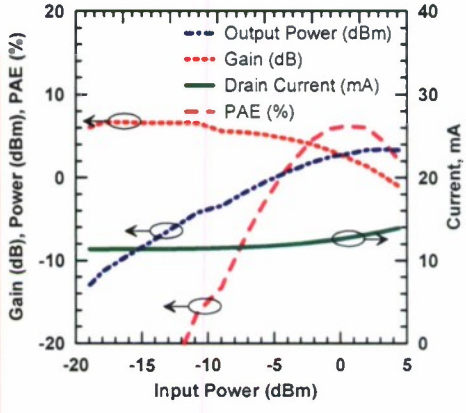


Figure 9: 2 mW 340 GHz TSC/UCSB power amplifier

Dry-Etched Emitter Technology: 256 nm generation

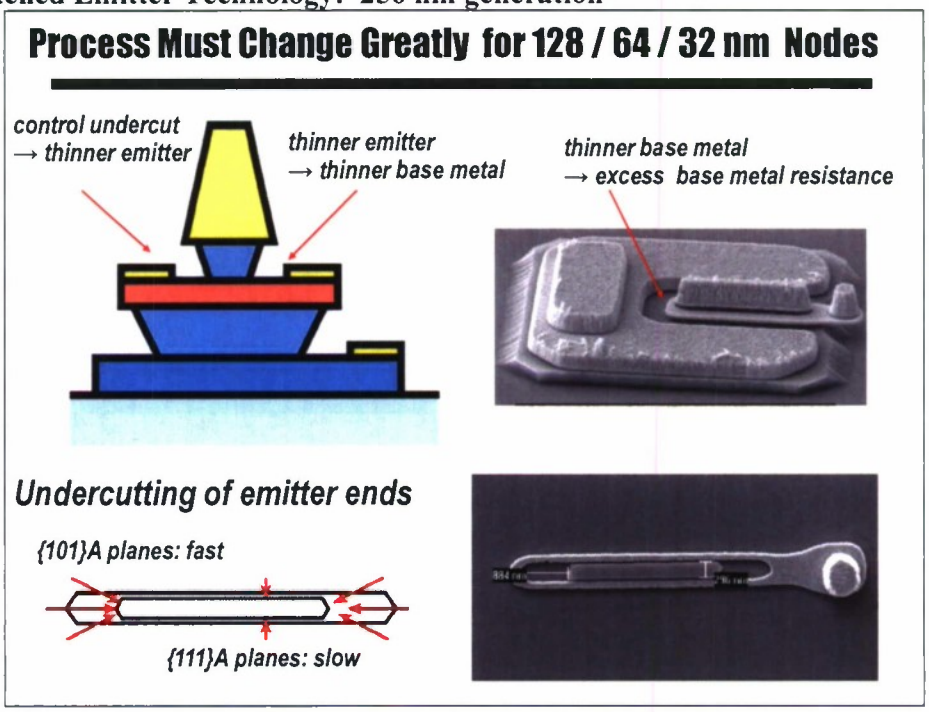


Figure 10: Difficulties faced in scaling HBT process flows to 128 nm & below.

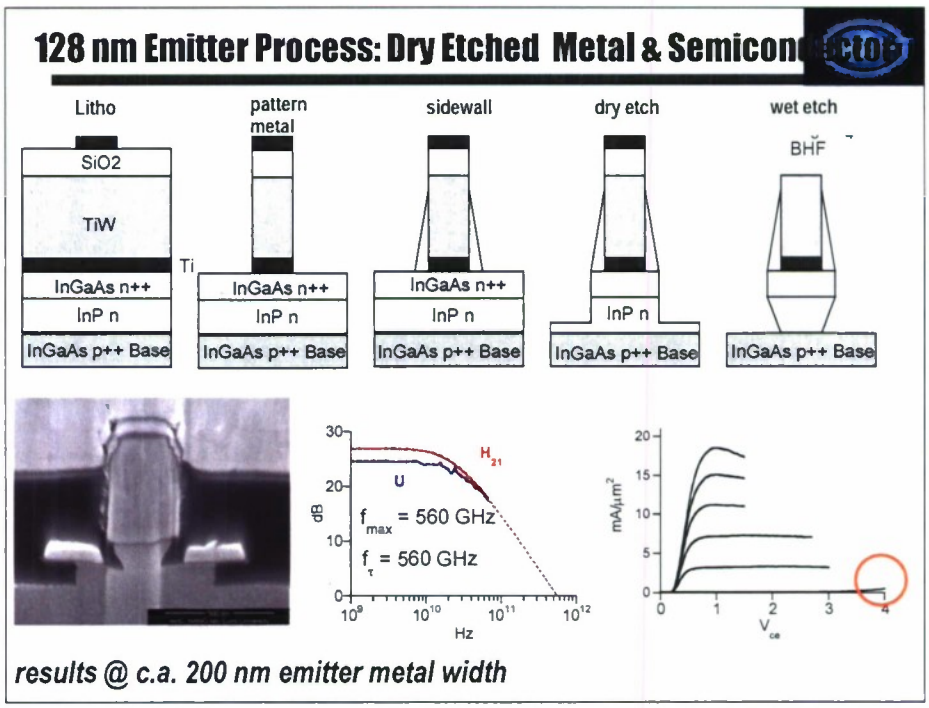


Figure 11: Dry-etched emitter process.

As shown in Figure 6, standard mesa and liftoff HBT processes can be used to build devices at 256 nm emitter feature size. At smaller sizes (Figure 10), two major difficulties arise. First, in making the emitter more narrow, emitter etch undercut must be reduced. This requires thinning the emitter, which (in a liftoff process) then requires thinning the base metal. High base metal access resistance then results from such thin metal layers, and the HBT f_{max} drops. A second difficulty arises from wet-etching the emitter. While the etch facets of InP allow the lateral etch rate to be low, reducing the lateral undercut on the emitter sides, facet effects result in very rapid undercutting of the emitter ends, particularly for very narrow emitters. For these reasons, wet etched and lifted-off processes were abandoned at the 128 nm generation.

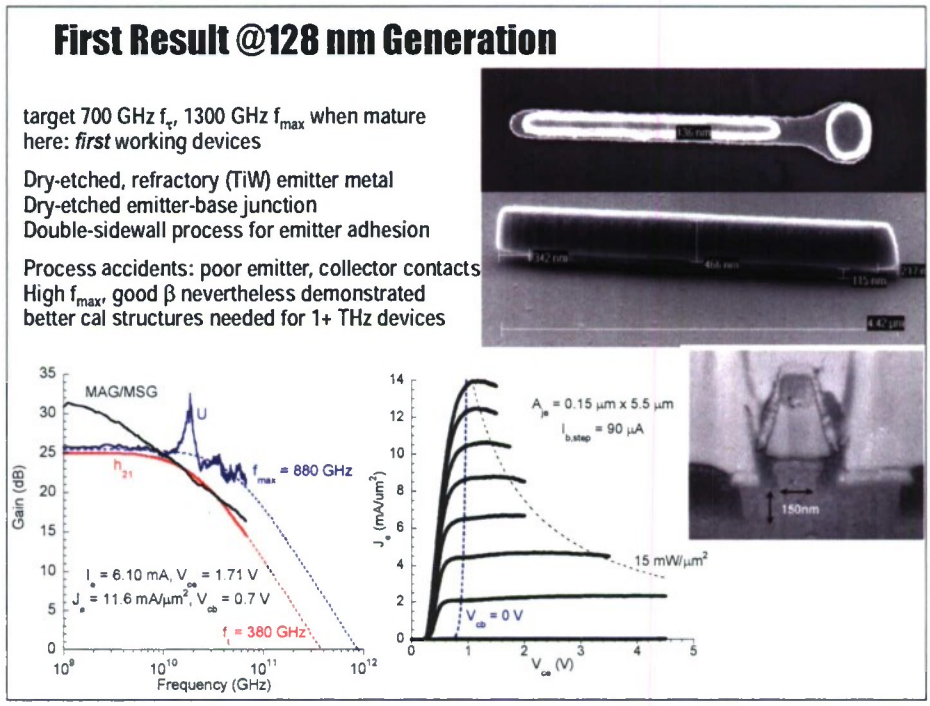


Figure 12: 128 nm scaling generation HBTs fabricated with dry-etched emitters.

A very large effort and investment was made under the SWIFT program to produce dry-etch emitter processes (Figure 11). It is necessary to dry etch both the emitter---so as to control etch undercut---and the emitter metal----so as to control the metal profile. A critical difficult in dry-etching the semiconductor is the accumulation of Indium Chloride on the etched surfaces. InCl is non-volatile, and interferes with subsequent processing. The developed processes used blanket-sputtered TiW refractory emitter metal, a metal which will remain stable at high current densities. The TiW metal is patterned by dry-etching. The emitter semiconductor is etched in an ICP-RIE system using Chlorine chemistry, with a combination of substrate heating and Argon sputtering used to drive off the InCl. Initial results of this process (Figure 11) produced HBTs with ~200 nm emitter feature size and 560 GHz f_τ and f_{max}. This was the first transistor of any type to have both cutoff frequencies simultaneously exceed 500 GHz.

Very recently, modified versions of the dry-etched emitter process flow have resulted in HBTs with 128 nm junctions and measured 880 GHz f_{max} (Figure 12).

Scaled Epitaxy

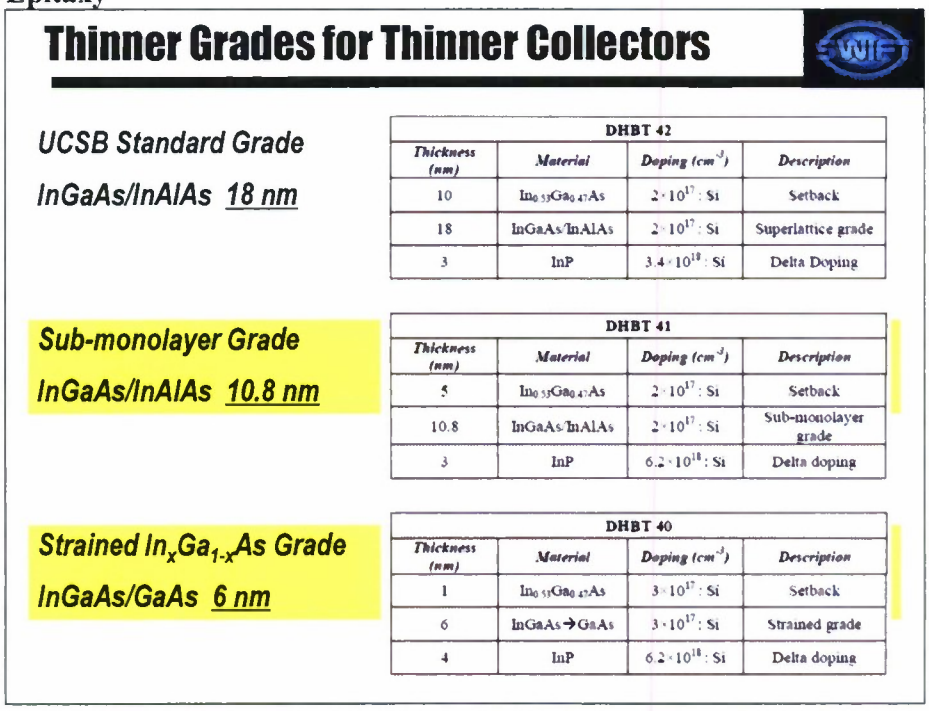


Figure 13 Revised collector grade designs for thinner epitaxial layers.

As collector layers are thinned for increased (f_τ , f_{max}) as per the scaling roadmap (Figure 5), the collector grade design must be revised (made thinner) so as to maintain the collector breakdown field. Revised collector designs with thinner grade layers were developed (Figure 13); these increased the measured low-current breakdown voltage by approximately 0.5 V (Figure 14). These layer designs were incorporated into the 560 GHz f_τ , 560 GHz f_{max} result of Figure 11

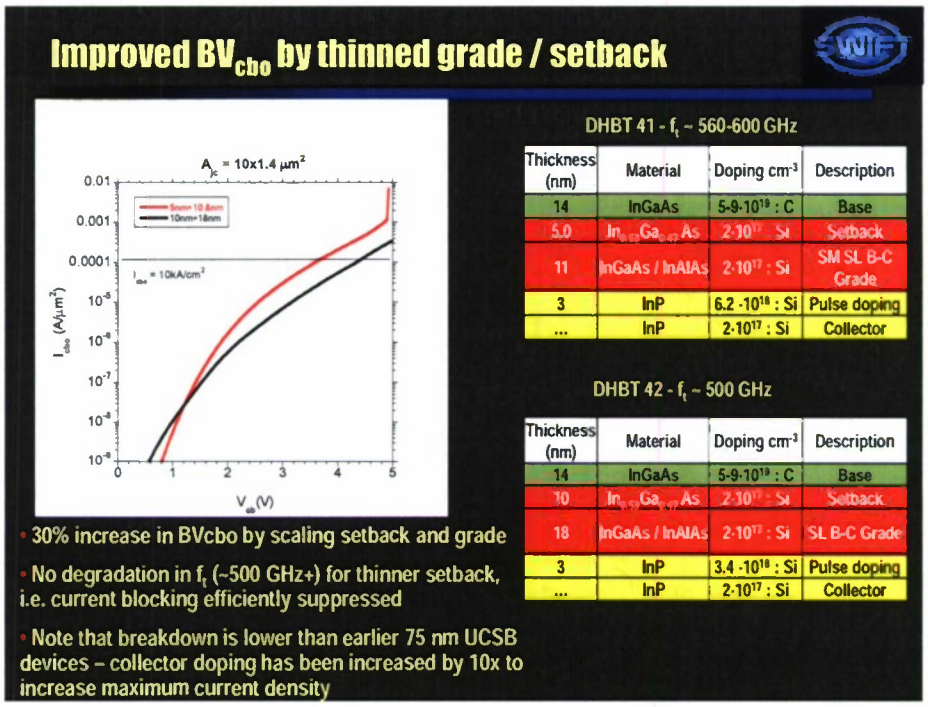


Figure 14: Measured improvement in breakdown voltage with thinned grade layers.

Conclusions

In the course of the SWIFT program HBT power gain cutoff frequencies were increased from 500 GHz to 880 GHz. This was accomplished by scaling the HBT from 500 nm feature size through 128 nm feature size, and demanded concurrent improvement in HBT process flows, low resistance emitter and base contacts, and revised epitaxial layer designs with thinner collector layers and thinner collector-base grades. Fundamental changes to the process flow were required in transitioning from the 256 nm to the 128 nm nodes, with the elimination of traditional liftoff and wet-etch processes and their replacement by blanket metal deposition (sputtering) and dry-etch processes, and the use of dielectric sidewalls to separate device electrodes. Development of these central process technologies was a major investment at UCSB made under support of the SWIFT program, and will enable further progress of HBT development to the sub-128-nm generations with associated multi-THz cutoff frequencies.