Patterning and Characterization Of Carbon Nanotubes Grown In a Microwave Plasma Enhanced Chemical Vapor Deposition Chamber

THESIS

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AFIT/GE/ENG/09-25

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Abstract

This research studies the growth of carbon nanotubes (CNT) from a nickel catalyst to be used on a field emission device. This thesis can be divided into three sections: the construction of a vacuum chamber for field emission testing, the design and fabrication of a triode structure to enable improved electron emission, and the pretreatment and growth of CNTs.

To experimentally test the field emission of CNTs, a vacuum chamber must attain a vacuum of at least 10^{-5} torr. Our vacuum chamber designed and built achieved a maximum, final pressure of 10^{-8} torr.

A triode structure was designed to pattern the CNTs to improve electron emission. A silicon wafer is used to fabricate the cathode and gate of the device while a quartz wafer is used as the anode. Through photolithography patterning of the gate, CNT growth occurs only in the defined locations.

To better understand CNT growth, a study was performed using a hydrogen pretreatment on sputtered and electroplated nickel catalyst on silicon at various thickness in a microwave plasma enhanced chemical vapor deposition to determine the effects of this pretreatment. Nickel catalyst of 50, 100, and 200 $\mathring{A}$ were treated with hydrogen and the formation of nano islands was achieved when using sputtered films. As the nickel catalyst thickness increases, the pretreatment time must also be increased to get favorable granule sizes and densities necessary for CNT growth. The 50 and 100 $\mathring{A}$ nickel samples granulated to 25 and 58 nm showed high growth densities while the 200 $\mathring{A}$ samples granulated to 180 nm showed marginal CNT growth. We also established the diameter of the multi walled CNTs grown correlated well to the size of the catalyst granules. The CNTs to be used in the triode design needed to be between 1.5 and 1.8 μm to avoid shorts between the gate and the CNTs. To achieve

this, CNTs with a length of 1.5 μm were successfully grown by flowing methane for exactly two minutes.

Acknowledgements

First I would like to thank my advisor Lt Col Coutu for his guidance and for supporting me through the completion of this thesis. I would also like to thank Maj Starman and Dr Collins for their advice during my fabrication hurdles. To the MEMS group thank you for answering my multiple questions.

Lastly, I would like to thank my wife and daugther for supporting and helping me during this time.

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List of Abbreviations

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LPCVD	Low-pressure Chemical Vapor Deposition	26
HF	Hydrofluoric Acid	26
Cr	Chromium	26
ALD	Atomic Layer Deposition	27
FET	Field Effect Transitor	30
ITO	Indium Tin Oxide	35
MPECVD	Microwave Plasma Enhanced Chemical Vapor Deposition	36
SiO_2	Silicon Dioxide	37
GFE	Government Furnished Equipment	40
CF	ConFlat	41
BOE	Buffered Oxide Etch	43
DIW	Deionized Water	43
RIE	Reactive Ion Etching	58
SEM	Scanning Electron Microscope	62

Patterning and Characterization Of Carbon Nanotubes Grown In a Microwave Plasma Enhanced Chemical Vapor Deposition Chamber

I. Introduction

Carbon nanotube (CNT) research is a hot topic in industry and academia due to CNTs incredible electrical and mechanical properties. CNT studies are being carried out in numerous application areas such as, field emitter displays (FED), heat dissipation elements, field effect transistors and many others.

One of the largest CNT application areas is FEDs. Currently the technology for displays include cathode ray tubes (CRTs), plasma displays, liquid crystal displays (LCD), and organic light emitting diode (OLED) displays. CRT displays are usually extremely heavy compared to all other displays and they are also limited in size. Plasma displays offer larger sizes, wide viewing angles and are flat but they also require lots of power to operate, suffer from burn-in and have a short life span. OLED displays are the newcomers to the market boasting low power consumption and wide viewing angles. OLED displays suffer from stability problems and have short life spans. CNT FEDs in comparison will consume less power than plasma displays since they will use the same phosphor as CRT displays but will not need the ionization step required for plasma displays. The weight of the display will be kept down since the cathode will be CNTs which are small and light weight. The CNTs will emit electrons thru a vacuum into the phosphorus screen. [1]

Vacuum microelectronics, a field in micro- and nanoelectronics, is the use of electrons in vacuum where the active element has dimensions on the order of tenth to hundredths of a micrometer [2]. Currently solid state electronics depend on electrons

and holes flowing thru some kind of conduction channel. With vacuum microelectronics, the ballistic motion of electrons in a vacuum will be used to increase the speed of transfer and lower power requirements, where ballistic motion is the movement of electrons in a medium with negligible electrical resistivity due to scattering. [2]

1.1 CNTs as Field Emitters

To be able to grow CNTs as field emitters, it is invaluable to first understand what factors affect field emission. Field emission is a quantum mechanics effect where electrons tunnel through matter into a vacuum. A combination of effects help electrons when tunnelling such as barrier narrowing as displayed in Figure 1.1. By combining both image forces and voltage, narrowing of the barrier makes it easier for electrons to tunnel and go from the cathode to the anode creating field emission.

1.2 Objective

The objective of this work is to build a triode structure containing a cathode, gate and anode to characterize field emission of CNTs. The cathode, CNTs in our case, will act as the electron emission source. To be able to extract the electrons, a voltage will be applied to the gate to create a voltage difference between the gate and cathode. The anode will accelerate the electrons to itself by having a higher potential than both the gate and cathode. This thesis effort can be divided into three sections:

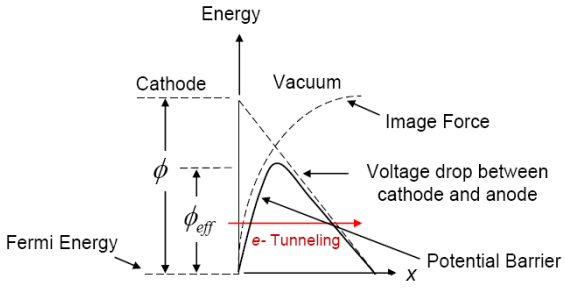


Figure 1.1: Idealized energy barrier at cathode-vacuum interface due to superposition of image forces and applied voltage between anode and cathode [3].

- Wafer Preparation
- CNT growth
- Experimental set up

1.2.1 Wafer Preparation. Two wafers were used during the fabrication of the triode structure. A silicon wafer was used as the cathode and gate while a quartz wafer was used as the anode structure.

Figure 1.2 illustrates the layers needed for the cathode and gate. A silicon wafer was used as the substrate for the cathode and gate due to its conductive nature. A titanium (Ti) layer 200 $\mathring{A}$ thick was sputtered as a diffusion barrier and adhesion layer for the 100 $\mathring{A}$ sputtered nickel (Ni) layer to be used as the catalyst for CNT growth. A 2 μm silicon dioxide layer was used as a dielectric between the gate and cathode. The gate material consisted of a 2500 $\mathring{A}$ thick layer of chromium. A gold layer, 5000 $\mathring{A}$ thick was used for flip chip bonding and wire bonding.

The quartz wafer used as the anode was patterned using photolithography. This was followed by a inductively coupled plasma reactive ion etching (ICP-RIE) process to give a 50 μm spacing between the anode and gate. The next step was to flip chip bond both wafers as shown in Figure 1.3. Quartz is used since it is a dielectric and it will not cause the gate and anode to short out. A gold layer, 1 μm thick, was

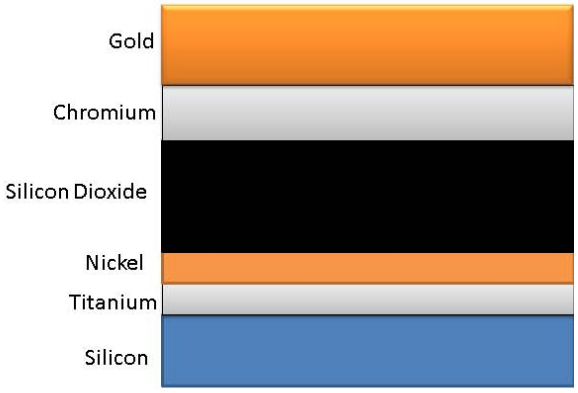


Figure 1.2: Layers needed to create the cathode-gate wafer.

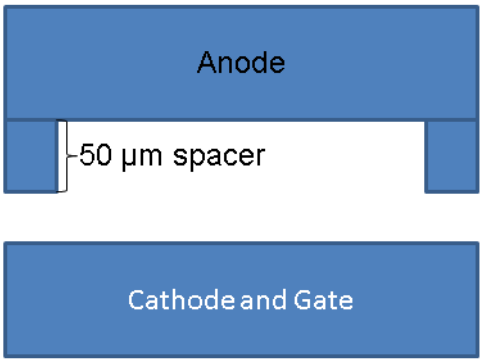


Figure 1.3: Illustration of anode wafer flip bonded to the cathode-gate structure.

evaporated or sputtered over the anode legs and bottom surface to act as a conducting surface and to aide with the adhesion during flip chip bonding.

1.2.2 CNT Growth. CNT growth takes place in a microwave plasma enhanced chemical vapor deposition system. The first step is to introduce H_2 to chemically react with the nickel and to create the conditions necessary for the formation of a plasma to granulate the nickel layer that acts as the catalyst for CNT growth. The microwave power is set to 400 watts at a temperature of 400 °C during the H_2 pretreatment. The time for pretreatment was varied and the nickel particles were studied to determine the optimum time needed for CNT growth. Both H_2 and CH_4 was used during the CNT growth. The ratio of H_2 to CH_4 was kept at 8:1 with a total flow of 135 sccm. The temperature during CNT growth is raised to 650 °C and to a microwave power of 1 kW. The time required for CNT growth to occur is between 60 and 120 seconds.

1.2.3 Experimental Set Up. The experimental set up consisted of the designing of a vacuum chamber, and setting up an electrical characterization test. Due to the outgassing of plastics, a typical printed circuit board can not be used. Instead, a sapphire wafer, a dielectric, was used as the board. Gold was deposited onto the wafer and then etched back to form the connection lines. A dual inline package with a cavity for a 1 cm^2 device was used to connect the wafer piece to the sapphire

wafer. The vacuum chamber, rated for at least 10^{-5} torr pressure, consist of eight high voltage electrical feedthroughs.

II. Background

In 1991 Sumio Iijima first saw images of a multi-walled carbon nanotubes (MWCNT) in a transmission electron microscope (TEM) [4]. In 1993 Sumio Iijima and Donald Bethune synthesized the first single-walled carbon nanotube (SWCNT) [4]. Since then the field of carbon nanotubes has exploded with different applications being studied everyday. To truly understand CNTs the following aspects need to be discussed:

- Structure of CNTs
- CNT fabrication techniques
- CNT properties
- Application of CNTs

2.1 Structure of Carbon Nanotubes

CNT structures vary depending on shape, size, and growth method. CNTs are divided into SWCNTs or MWCNTs, and further divided depending on the way the CNTs are rolled from a graphene sheet into zig-zag, armchair and helical.

2.1.1 Single-Walled Nanotubes. A SWCNT is a rolled up single walled layer of a graphene sheet (Figure 2.1) that ranges in diameter from 1 to 2 nm [5]. Diameters smaller than 1 nm have been created, but contain high stresses and require greater energy to produce [6].

There are no restrictions on the length of SWCNTs. Two important aspects of SWCNTs are derived from their geometry:

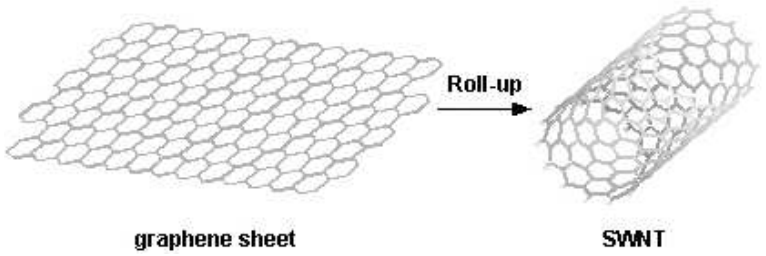


Figure 2.1: CNT Triode Fabrication [7]

1. All carbon atoms are arranged in a hexagonal shape. On SWCNTs, the tips are comprised of a pentagonal shape that will create better chemical reactivity [6].
2. Carbon to carbon bonds of SWCNTs are no longer planar making SWCNTs surfaces more reactive and encourages overlapping of energy bands that create specific electrical behavior, to be discussed in Section 2.3 [6].

2.1.2 Multi-Walled Nanotubes. MWCNTs are multiple graphene cylinders separated by a spacing of 0.34 nm [5] (Figure 2.2). Outer diameters of MWCNTs range between 2 to 25 nm and inner diameters range from 1 to 8 nm [5].

As with SWCNTs, MWCNTs do not have any restrictions on how long they can be grown. MWCNTs can be formed in three ways:

1. Concentric(c-MWCNT) [6]
2. Herringbone(h-MWCNT) [6]
3. Bamboo [6]

The c-MWCNT is the simplest form to visualize. It takes multiple SWCNTs with increasing diameters in the Russian-doll model shown in the inset of Figure 2.3. c-MWCNTs can also be visualized as a coaxial arrangement of SWCNTs. The number

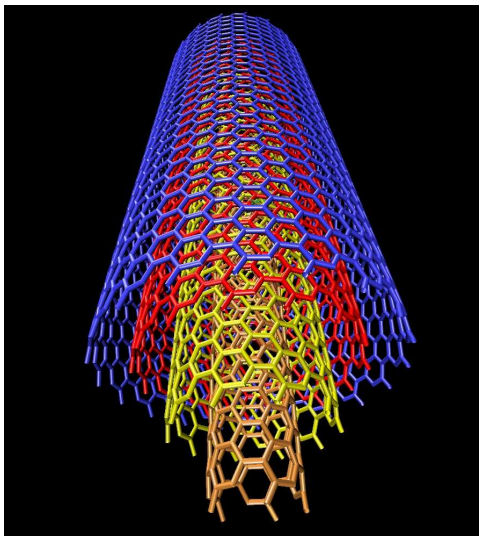


Figure 2.2: Multi-walled Carbon Nanotube [8]

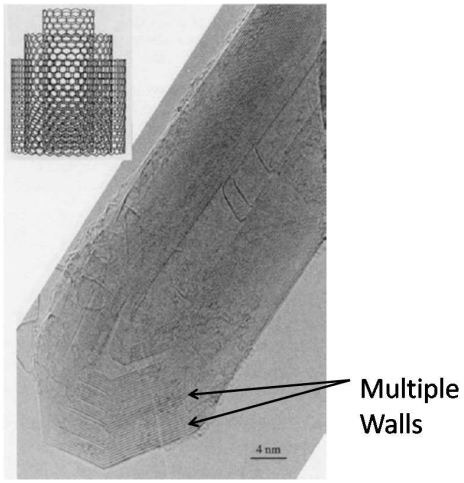


Figure 2.3: Transmission electron microscope Concentric Multi-walled Carbon Nanotube image. Insert in the upper left is a sketch of the Russian-doll-like display [6]

of walls can go from two (D-MWCNTs) to no limit. The distance between the tubes is approximately 0.34 nm closely matching the graphene sheet distance of 0.335 nm. [6]

Actual formation of the Herringbone MWCNTs is still under debate. One school of thought is that they are formed by folding the graphene sheet into multiple cylinders similar to a rolled up newspaper. Other scientist and engineers believe that they are formed by "stacking of independent, truncated-cone-like graphenes" [6]. Both groups agree the graphene sheet forms an angle to the axis of the nanotube varying dependent on the growth method used. When this angle reaches 90 degrees, the inner spacing between the CNTs collapses and is no longer a tube and it becomes a carbon fiber. [6]

The bamboo configuration can not exist by itself, but instead affect both c-MWCNT and h-MWCNT types as shown in Figure 2.4. In this configuration, the tube is not hollow throughout. Instead the tube is separated into individual hollow compartments similar to a bamboo. [6]

2.1.3 Helicity of Carbon Nanotubes. The helicity, or the way that the graphene sheet is rolled up to create CNTs, refers to three types of nanotubes:

- Armchair

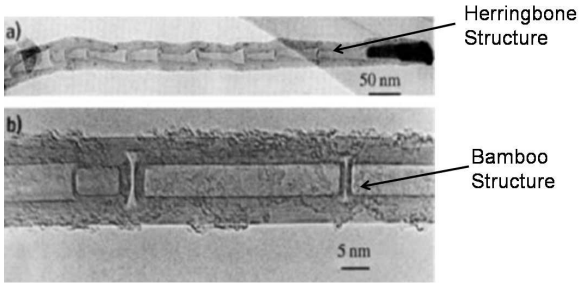


Figure 2.4: a) Transmission electron microscope of bamboo-herringbone-MWCNT image. b) Transmission electron microscope of bamboo-concentric-MWCNT image. [6]

- Zigzag
- Chiral

The different types of CNTs are derived from Bravais lattice vectors which satisfy the boundary conditions resultant from the mapping of a graphene sheet into a cylinder [5]. These vectors, called vectors of helicity C_h or Chiral vector, are defined by two primitive vectors and the angle of helicity θ as shown on Figure 2.5. In MWCNTs, each wall can have its own chiral vector but as a whole, the MWCNT does not have a chiral vector.

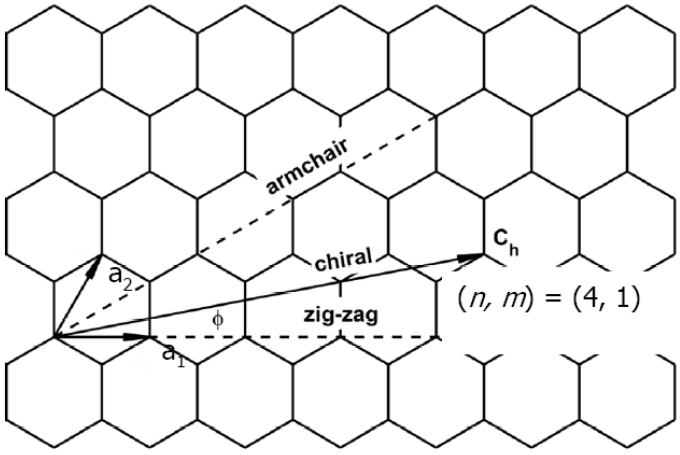


Figure 2.5: Scheme to derive the Chiral vectors and angle from a graphene sheet. [6]

Equation (2.1) shows the vector of helicity calculation and Equation (2.4) shows how to calculate the angle of helicity [6].

$$C_h = na_1 + ma_2 \tag{2.1}$$

where the unit vectors in the basal plane of a two dimensional lattice are

$$a_1 = \frac{a\sqrt{3}}{2}x + \frac{a}{2}y \tag{2.2}$$

$$a_2 = \frac{a\sqrt{3}}{2}x - \frac{a}{2}y \tag{2.3}$$

and

$$\cos\theta = \frac{2n+m}{2\sqrt{n^2+m^2+nm}} \tag{2.4}$$

where a=2.46 $\mathring{A}$, and n and m are the integers of the C_h vector considering unit vectors a_1 and a_2 [6]. The types of CNTs are defined as follows:

- Zigzag CNT need the vectors (n,m) to be (n,0) or (0,m) at $\theta = 0°$
- Armchair CNTs need the vectors (n,m) to be (n,n) at $\theta = 90°$
- Chiral CNTs need the vectors (n,m) to be (m,m) at $0° > \theta < 30°$. The vectors are determined by the way CNTs are rolled and formed.

  From the chiral vectors, the diameter of CNTs can be calculated by using [3]

$$D = (3^{\frac{1}{2}})a_{cc}(n^2+m^2+nm)^{\frac{1}{2}}(\mathring{A}) \tag{2.5}$$

where a_{cc} equals the distance between neighboring atoms found to be usually $1.41\mathring{A} \leq a_{cc} \leq 1.44\mathring{A}$ which equals the neighboring atom distance of graphite and C_{60} respectively [6]. The bandgap can also be calculated by using [3]

$$E_g = \frac{2y_o a_{cc}}{D}(eV) \tag{2.6}$$

where y_o is the carbon to carbon energy usually around 2.5 eV and D (length) is the tube diameter. Typical bandgaps for SWCNTs range from 10 meV to 1 eV [3].

2.2 Carbon Nanotube Fabrication Techniques

Multiple fabrication techniques have been studied for the formation of CNTs. One technique uses a catalyst metal as a precursor material for CNT growth while others do not use a catalyst. Basic steps for CNT growth from a metal catalyst are as follows:

- Placement of diffusion barrier if needed
- Placement patterning of the metal catalyst
- Annealing the metal catalyst

The main methods for growing CNTs are using an electrical arc reactor, laser ablation, surface decomposition, Chemical Vapor Deposition (CVD), or a Plasma Enhanced Chemical Vapor Deposition (PECVD) system.

2.2.1 Electrical Arc Discharge. Figure 2.6 shows an electric arc reactor. A potential of 20-25 V is applied across the cylindrical carbon electrodes which are 5-20 μm in diameter and separated by 1 mm at 500 torr of pressure with a flow of helium gas (inert gas). Carbon atoms are ejected from the positive electrode and form CNTs on the negative electrode. As the CNTs form, the positive electrode becomes shorter while the negative electrode adds carbon deposits. To produce a SWCNT, a catalyst metal has to be used, while MWCNTs can be created without using a catalyst. Typical SWCNTs have diameters of 1 nm to 5 nm and lengths up to 1 μm. MWCNTs fabricated by this method have inner diameters of 1 nm to 3 nm and outer diameters of approximately 10 nm.

2.2.2 Laser Ablation. In laser ablation systems (Figure 2.7), a pulsed laser is incident upon a graphite target, that contains small amounts of cobalt and nickel as catalysts. The target is placed inside a quartz tube containing argon gas and is heated

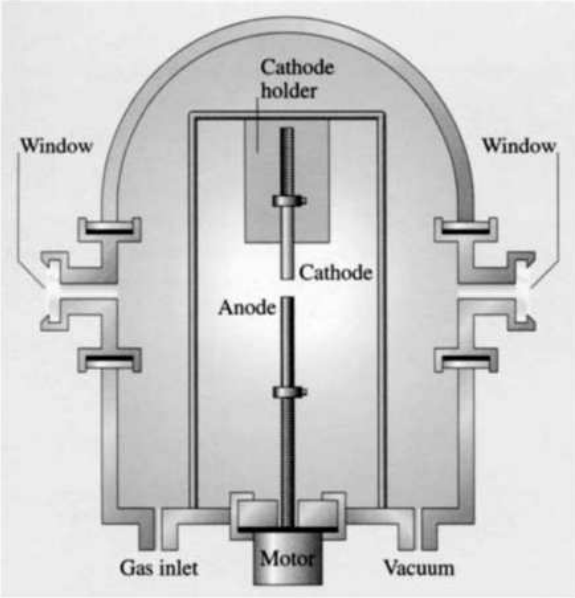


Figure 2.6: Sketch of an electric arc reactor. [6]

to 1200 °C. The pulsed laser hits the target evaporating carbon from the graphite. Carbon is then swept by argon from an area of higher temperature to an area of lower temperature. In the area of lower temperature, a water cooled copper collector collects the carbon that is being deposited as CNTs. Nominal CNTs of 10 nm to 20 nm in diameter and about 100 μm in length can be grown.

2.2.3 Surface Decomposition. In surface decomposition, a silicon carbide wafer is exposed to 1700 °C at 10^{-4} torr [3]. During decomposition, the silicon on the open wafer area (carbon face) is burned off and carried away by oxygen gas used in the process. Chemical reactions taking place are as follows [3]:

$$SiC(s) \rightarrow Si(g) \uparrow + C(s)$$

and/or

$$SiC(s) + \frac{1}{2}O^2 \rightarrow SiO(g) \uparrow + C(s)$$

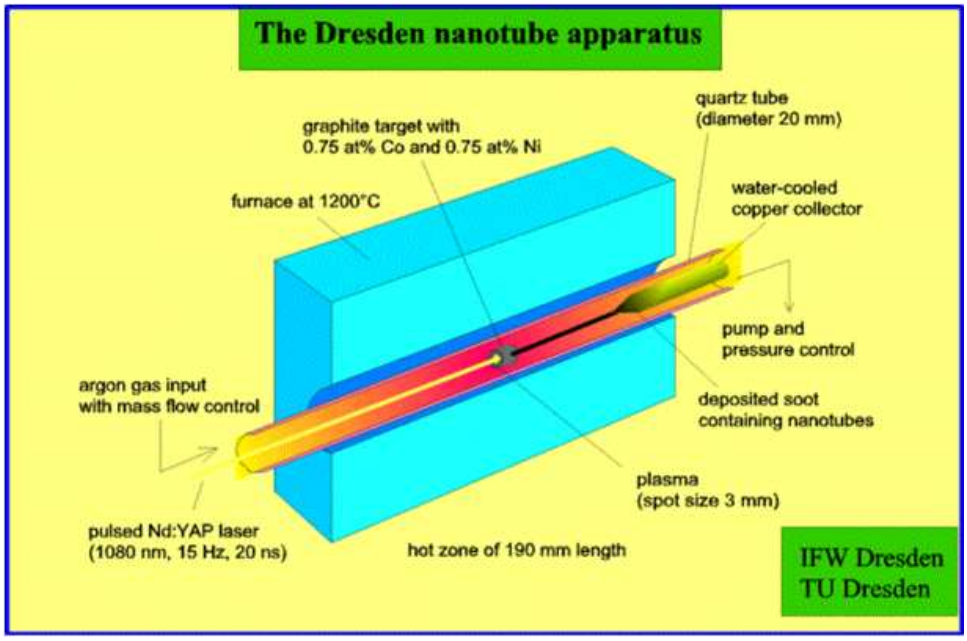


Figure 2.7: Sketch of an Laser Ablation System from the Institute for Solid State Research in Germany.

and/or

$$SiC(s) + CO(g) \rightarrow SiO(g) \uparrow + 2C(s)$$

The only thing left on the carbon side of the SiC wafer are SWCNTs as shown in Figure 2.8 .

2.2.4 Chemical Vapor Deposition (CVD) and Plasma Enhanced Chemical Vapor Deposition (PECVD). CVD and PECVD are the most widely used methods for growth of CNTs. Both methods involve decomposition of a hydrocarbon gas, for example methane (CH_4), which condenses on a cooler substrate containing metal. The growth process is as follows:

- Pretreatment of a catalyst at a lower temperature to granulate the metal layer.

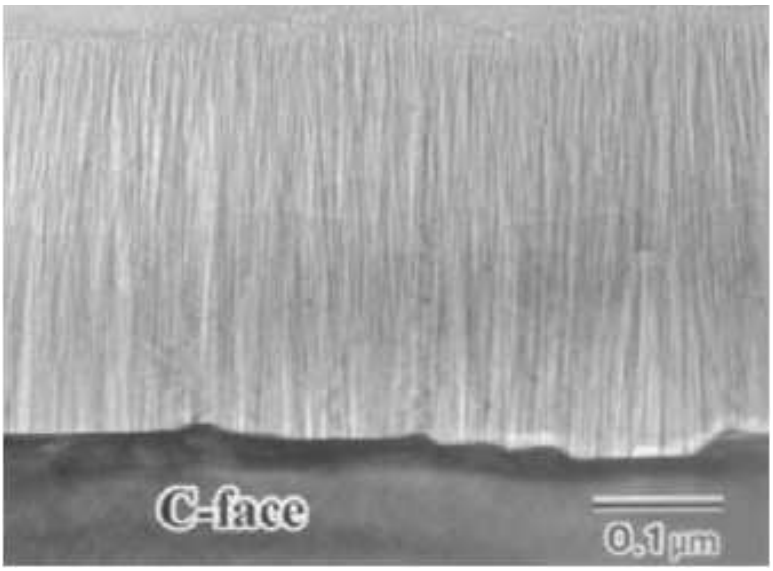


Figure 2.8: Transmission electron microscope image of a CNT film grown on the C-face of SiC [3]

- The size of granules determine if a SWCNT or MWCNT is produced. Hydrocarbon gasses interact with the metal catalyst and create an upward growth of CNTs (Figure 2.9).
- The metal catalyst does not stay on the surface of the CNT but travels to the tip of the CNT. This can be seen in the insert of Figure 2.10 as brighter spots on the tips.

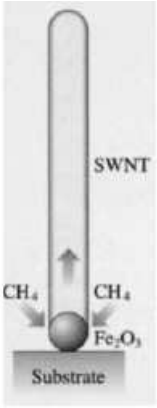


Figure 2.9: Growth of SWCNT from a metal catalyst [6]

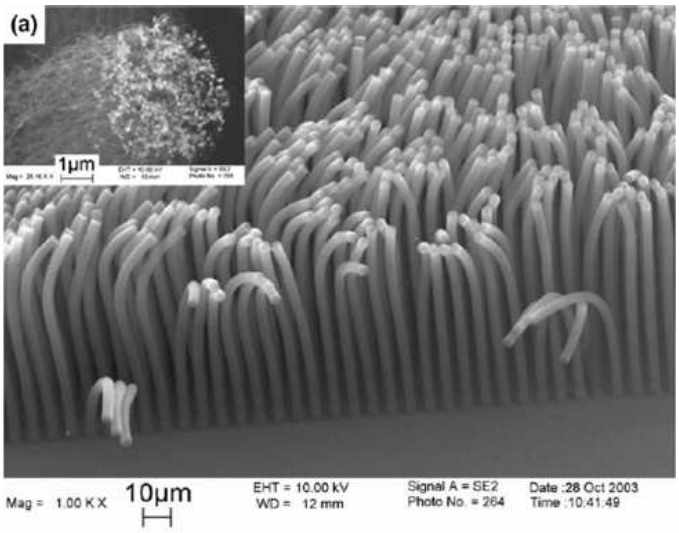


Figure 2.10: Growth of SWCNT from a metal catalyst using CVD. Insert shows bright spots due to the metal catalyst travelling to the tip. [9]

Figure 2.11 shows how a double CVD furnace acts to create CNTs. An inert gas flows from the low temperature oven to the high temperature oven. In the first oven, the hydrocarbon is produced and combines with the metal catalyst that is placed on a wafer on the high temperature oven to create CNTs [6]. Temperatures range between 550 °C to 900 °C.

Figure 2.12 shows the set up of a PECVD system. The addition of plasma allows the temperature to be kept lower, around 650 °C, in comparison to a CVD system. H_2 gas is used as a precursor gas to granulate the metal catalyst. Acetylene

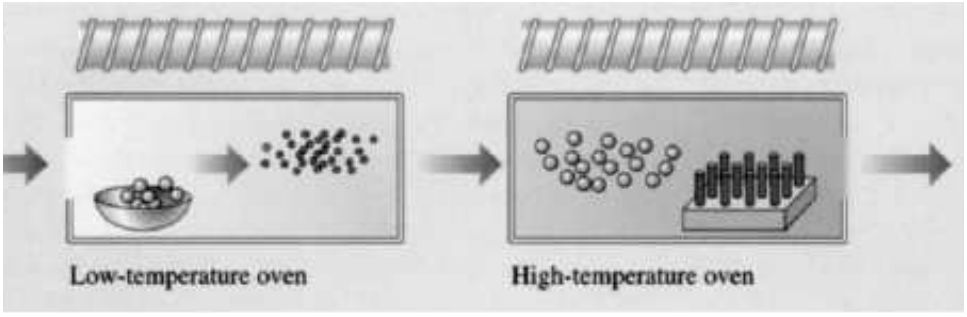


Figure 2.11: Sketch of a CVD double oven used for CNT growth. The first oven releases the hydrocarbon while the second promotes CNT growth [6]

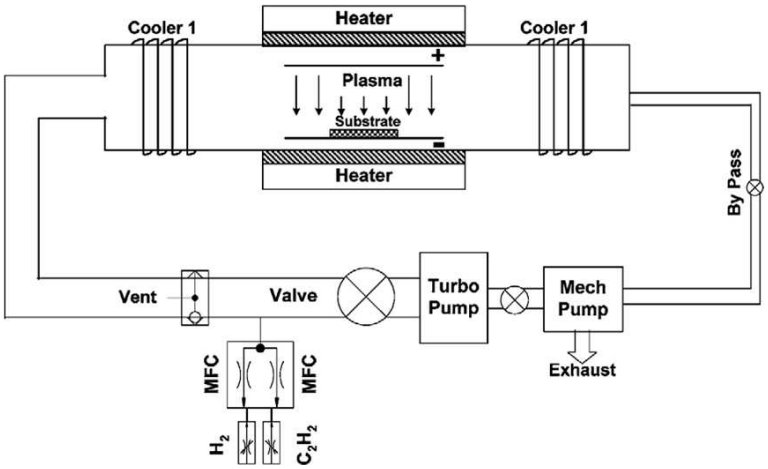


Figure 2.12: Sketch of a PECVD system [10]

(C_2H_2) is then used as the hydrocarbon for CNT growth. Plasma also affects CNT growth by making them grow vertical.

The four prominent methods for CNT growth using either CVD or PECVD methods and different structure fabrication methods found in literature will be discussed in the next section.

2.2.4.1 Controlled Density of Vertically Aligned Carbon Nanotubes in a Triode PECVD System. Lim [11] discusses the growth of CNTs that takes place in the PECVD system as shown in Figure 2.13. The PECVD system is arranged to have a triode configuration by adding a mesh located 10 mm from the substrate. The

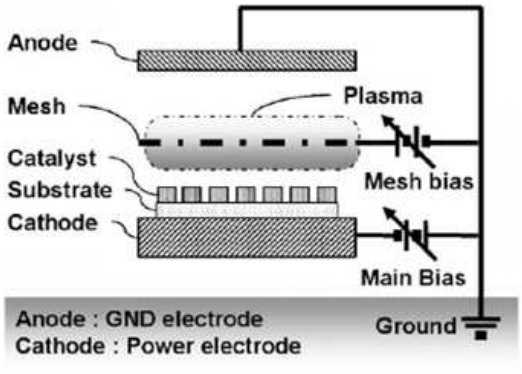


Figure 2.13: Triode PECVD System Schematic [11].

mesh has a hole size of 2 mm, pitch of 1 mm, and has a voltage swept from -300 V to 300 V. The substrate is kept at -600 V and the anode is grounded. The catalyst used is Ni, sputtered 30 nm thick and patterned with a method, not discussed, to yield 5 μm diameter disks. The catalyst is exposed to NH_3 and plasma for 2 minutes to granulate the Ni prior to CNT growth. Gases used for CNT growth are C_2H_2 (50 sccm), and NH_3 (50 sccm). The growth temperature was kept at 580 °C. CNT growth took place at a pressure of 2.66 mbarr (2 Torr) for 20 minutes. As shown in Figure 2.14, using a negative bias on the mesh, no CNT growth takes place due to electrostatic repulsion of charge species in the plasma. At 100 V, CNT length is 3 μm and if the mesh voltage is increased to 300 V, length increases to 5 μm with a density of 1.5 μm^2. The increase is attributed to the high supply of positive ions and the high electric field. No emission characteristics were discussed by Lim. [11]

There are three advantages to this process: no sophisticated techniques such as electronic beam lithography are needed, the length and density of CNTs can be varied by adjusting mesh bias voltage, and CNT growth is rapid.

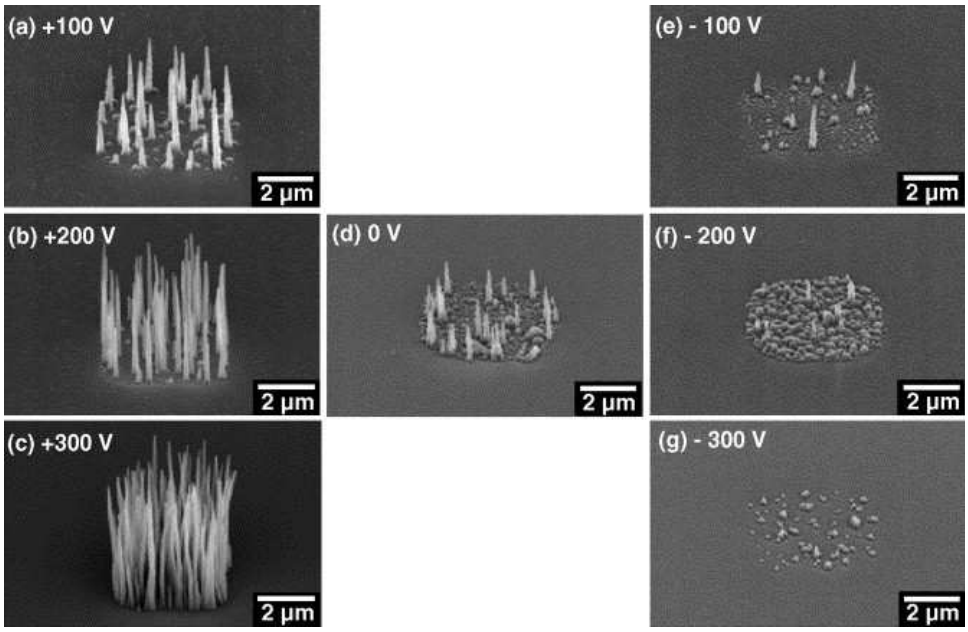


Figure 2.14: SEM images of CNTs grown with mesh bias voltage of 100 V (a),+200 V (b), +300 V (c), 0 V (d), -100 V (e), -200 V (f), -300 V (g) [11].

2.2.4.2 Growth of Vertically Aligned Arrays of Carbon Nanotubes for High Field Emission. D. Kim, et. al. [12] discusses two different methods to grow Multi-walled CNTs. All growth techniques use a highly n-doped Si substrate covered with a 10 nm thick TiN layer used as a diffusion barrier. The catalyst used is Ni and is sputtered approximately 7 nm thick. The substrate temperature for both methods is kept at 620 °C. The first method combines a hot wire CVD (HWCVD) with a dc PECVD system. A tungsten wire, 0.38 mm in diameter, is heated to approximately 1800 °C by flowing 13 amps. The tungsten wire is positioned approximately 15 mm from the cathode while the distance from the anode to the cathode is approximately 8 mm. The cathode is biased at -475 V as compared to the anode. A gas mixture of C_2H_2 for deposition and NH_3 with H_2 are used as etching gases to break up the Ni thin film sputtered into nanoparticles that originate CNT growth. The total gas flow rate is set at 100 sccm at a pressure of 1.5 Torr. The gas ratio of C_2H_2 to H_2 is 10% to 90% while the time needed is 15 minutes for MWCNT growth. CNTs grown were tangled and curled up making them a bad choice for CNT field emission.

The second method is to use the triode PECVD reactor discussed in Section 2.2.4.1 which produces CNTs that are vertically aligned. Patterning techniques are only conducted on the second method since these CNTs will yield a higher field emission. The two patterning techniques used are optical Ultra Violet (UV) lithography (1 μm resolution) and electron beam (EBL) lithography (50 nm resolution). In UV lithography, the dot pitch was set at 3.3 μm, 5 μm, and 10 μm for 1.6 μm Ni dots. From the 5 μm and 10 μm pitches, approximately 12 CNTs where observed on each dot with diverse diameters centered at 230 nm and an average length of 8.9 μm. The Ni dots are created by flowing NH_3 and H_2 as etching gasses. For e-beam lithography, the dot pitch was set at 2 μm, 3 μm and up to 8 μm to produce approximately 200 nm Ni dots. Only one MWCNT grows from Ni dots that are less than 200 nm [12]. The 2 μm pitch results demonstrated Ni dots of 260 nm with an average length of 4.2 μm (Figure 2.15).

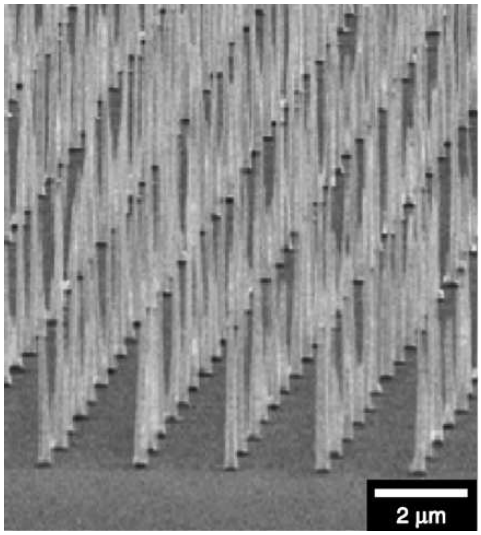


Figure 2.15: MWCNTs on Ni dots (260 nm in diameter). Dot pitch is 2 μm [12]

When a pitch of 2.8 μm is used, the Ni dot size is reduced to 180 nm. At this dot size average lengths are 3.8 μm with an average tip diameter of 45 nm with a base of 140 nm. The field emission current densities from the CNTs exceed 0.4 A/cm^2. Kim et al. believed that C_2H_2 being 50 % of the flow mass ratio led to an amorphous carbon deposition on the CNTs resulting in the low current density. One way to solve this problem would be to decrease C_2H_2 and increase NH_3. [12]

The advantages of these techniques are that the shape of the carbon nanotubes might increase the reliability of the CNT field emission array since once the taller CNTs erode, shorter CNTs take their place as sources of emission. The shape from this growth technique contributes to an equal E-field on all the CNTs. A disadvantage is the low current density of 0.4 A/cm^2 as compared to values discussed later. More tests are needed to prove that a different flow mass ratio would raise the current density.

2.2.4.3 Self-Aligned Carbon nanotubes for Field Emission Tip with Simple Process. A procedure for fabrication of a triode configuration CNT array is exposed by Eom [13] and displayed in Figure 2.16. The catalyst used in this process

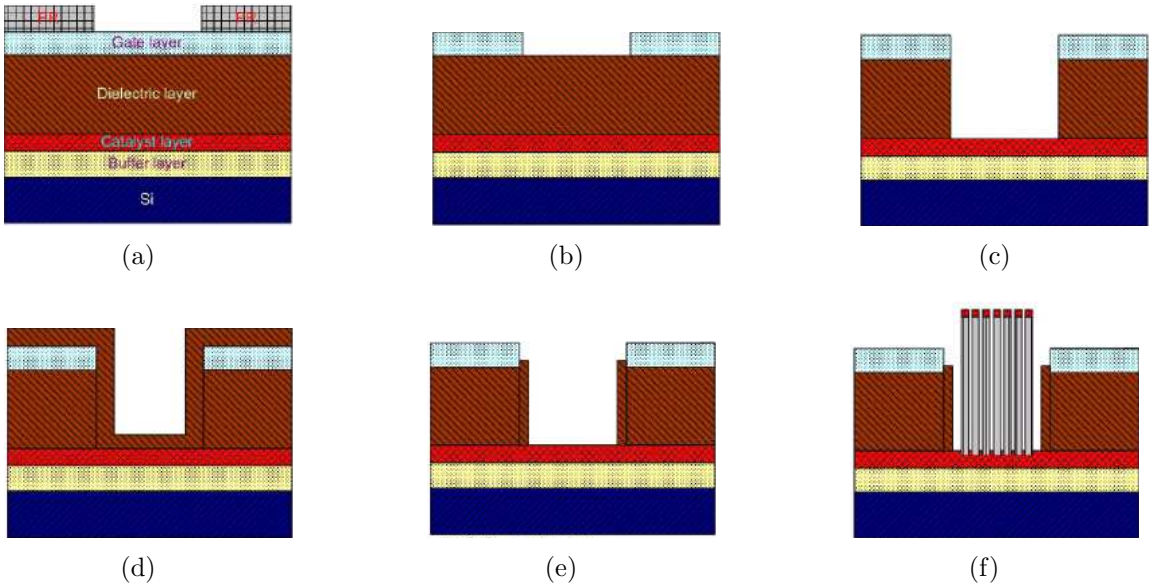


Figure 2.16: Process Flow for Eom Technique (a) Photo resist patterning. (b) Metal etching. (c) SiO_2 dry etching. (d) SiO_2 deposition. (e) SiO_2 dry etching. (f) CNTs growing. [13]

was Ni, sputtered 20 nm thick. Due to interactions of Ni with Si, a buffer layer of Ti, 50 nm thick, has to be sputtered before Ni. This is followed by depositing a 1 μm SiO_2 layer by PECVD and sputtering a 50 nm Cr layer to be used as the gate (Fig. 2.16 (a)). Patterning of the surface is done to be able to etch the Cr and SiO_2 until the catalyst is uncovered (Fig. 2.16 (b) and (c)). A second SiO_2 deposition and etching is done to decrease hole size (Fig. 2.16 (d)and (e)). Next, CNT growth takes place in a PECVD system with a gas flow of NH_3 at 40 sccm, C_2H_2 at 10 sccm, a temperature of 600 °C , and a pressure of 5.2 torr for 15 minutes (Fig. 2.16 (f)) [13]. The lengths of CNTs grown averaged approximately 1 μm in length.

The major advantage for this technique is simplicity of the fabrication process. Also, by depositing the second SiO_2 layer, a buffer layer is created to ensure no shorting can happen between the CNTs and the gate.

2.2.4.4 Field Emission Triode Amplifier Utilizing Aligned Carbon Nanotubes. Wong, et. al. [14] use techniques which consist of combining CVD to fabricate a gate structure then switching to MPCVD for growth of the carbon nan-

otubes. To prevent cathode-gate shorting, an over etched gate structure is used as displayed in the fabrication process in Figure 2.17. SiO_2 is grown by thermal oxidation to a thickness of $\sim$1.5 μm on a highly n-doped Si wafer (100). After the SiO_2 is grown, the wafer is moved into a CVD chamber for the deposition of an 0.8 μm polysilicon gate layer which is highly doped to obtain high conductivity. The next step is to etch the polysilicon and the oxide layer. Polysilicon is dry-etched by a mixture of SF_6 and O_2 at 150 mTorr while the oxide is wet-etched with BOE to obtain an undercut under the gate. For the growth of CNTs, a layer of Ti $\sim$20 nm thick, is deposited to act as a diffusion barrier. The catalyst is Ni, $\sim$5-10 nm thick. Both metals were sputtered by using a DC magnetron sputtering system set at 7 mTorr of Ar. For growth of vertically-aligned CNTs with a convex-shaped top, Ni is first pretreated with H_2 at 400 W microwave power and 400 °C. CNT growth occurs at 20 Torr with a substrate temperature of 650 °C, microwave power of 1 kW, and a gas flow ratio of CH_4 and H_2 at 1:8 with a total flow rate of 135 sccm. Vertical spacing between the edge of the CNT cathode and gate is 2 μm. Device characterization takes place at a base pressure of 10^{-6} Torr. The gate turn-on field for the device is measured at approximately 16.5 V/μm. A large anode current density of $\sim$1.2 mA/cm^2 is measured with a gate voltage of 46 V and an anode voltage of 300 V. [14]

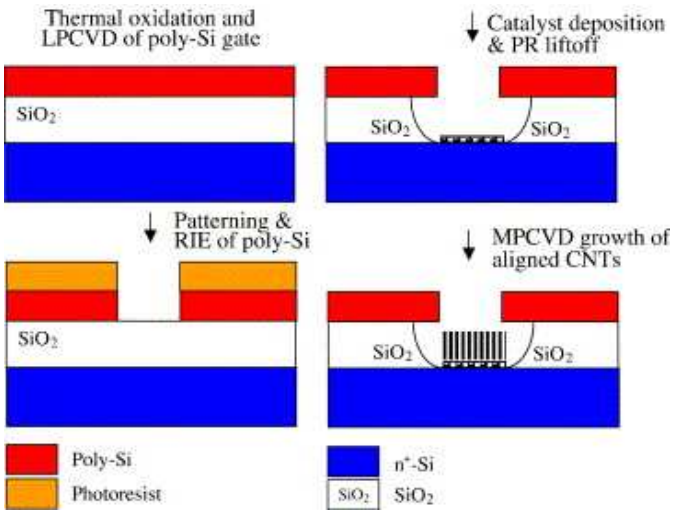


Figure 2.17: CNT Triode Fabrication [14]

The simplicity of this design is a major advantage of this process. Also, by undercutting the gate, the probability of gate-emitter shorting is decreased.

2.3 Carbon Nanotube Properties

The allure to use CNTs for a wide range of devices is due to the unique electrical and metallic properties they possess. Electrical properties of CNTs allow it to behave like a metallic or semiconducting material. Since CNTs are rolled sheets of graphene, it has band structures closely related to graphene. In Figure 2.18, a graphene's band structure crosses the fermi level at six points displaying the ability of CNTs to act as metallic or semiconductor structures. Whenever n-m=3i and i=0 or an integer in the chiral vector, it is a metallic CNTs, armchair CNTs are always metallic, if not it becomes a small gap semiconductor. Zigzag and chiral can be either metallic or semiconducting.

In Figure 2.19 it is shown how the graphene (a), metallic (b), and semiconducting (c) bands differ from each other. The metallic conduction and valence bands can be seen intersecting at different points like the graphene bands. The semiconducting bands have a gap at all intersections. These bands can be adjusted in minute movements with the help of an electric field. Figure 2.20 shows how by applying a small electric field across the band gap of a zigzag [17,0] (n-m=17 so we have a semiconducting CNT) CNT the gap decreases. The inset picture shows how a [18,0]

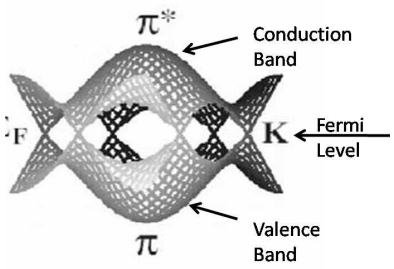


Figure 2.18: Band structure of graphene. Graphene's band structure crosses the fermi level six times. [3]

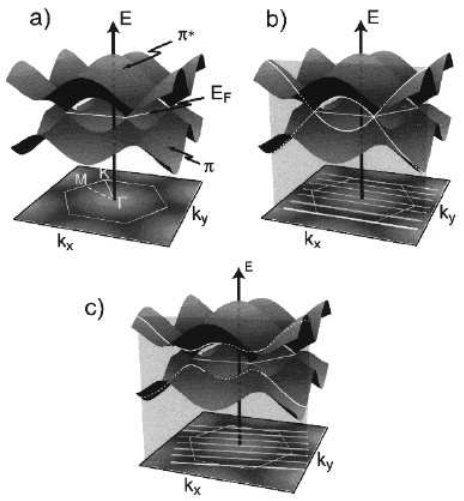


Figure 2.19: (a) Band structure of graphene, (b) metallic CNTs, (c) semiconducting CNTs (c) [15]

(n-m=18 so we have a metalic CNT) CNT has different band gaps depending on the electric field being applied.

The mechanical properties of CNTs also offer some novel device possibilities. CNTs have been found to have Young's Modulus of 1 TPa which is five times that of

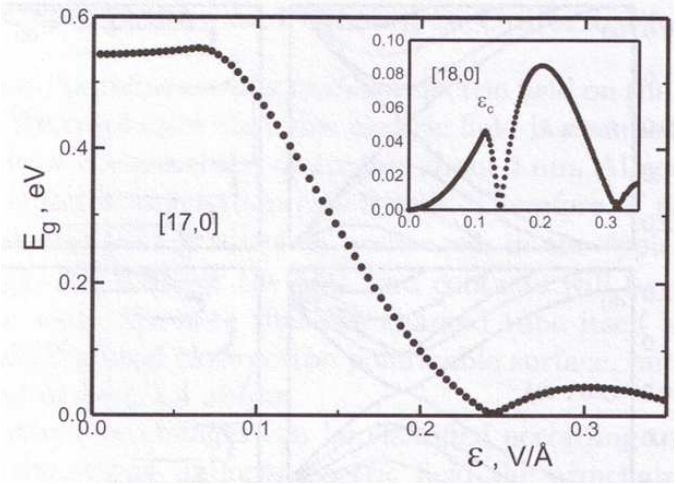


Figure 2.20: Band gap variation of a [17,0] (Semiconductor CNT) zigzag due to an electric field applied. As the electric field increases the band gap decreases. Inset: Band gap variation of a [18,0] (Metallic CNT) CNT due to an electric field. The band gap decreases and increases dependant on the field applied. [4]

steel. CNTs also have tensile strength of 45 GPa which is 20 times that of steel and strength to weight ratio 500 times greater than steel, aluminum and titanium [6]. One of the difficulties in using CNTs as mechanical devices is because there is no way to easily manipulate devices of a nanometer scale [16]. Other properties found in CNTs are high resistance to chemical substances, high thermal stability, able to operate in a vacuum and the use of its hollow structure as a composite for fuel cells.

2.4 Applications of Carbon Nanotubes

2.4.1 Mechanical Applications. The biggest obstacle in the application of CNTs as mechanical devices is size. Most electromechanical characterizations of CNTs have been done with the use of an atomic force microscope (AFM). The AFM is used to apply a force on a suspended CNT while measuring its electrical characteristics [17]. Studies have been done in the use of CNTs as mechanical elements for data storage, relays, oscillators, switches, and sensors [18]. Figure 2.21 has a matrix of possible CNT applications based on electrical, mechanical and optical transducers and their applications as sensors and actuators [18].

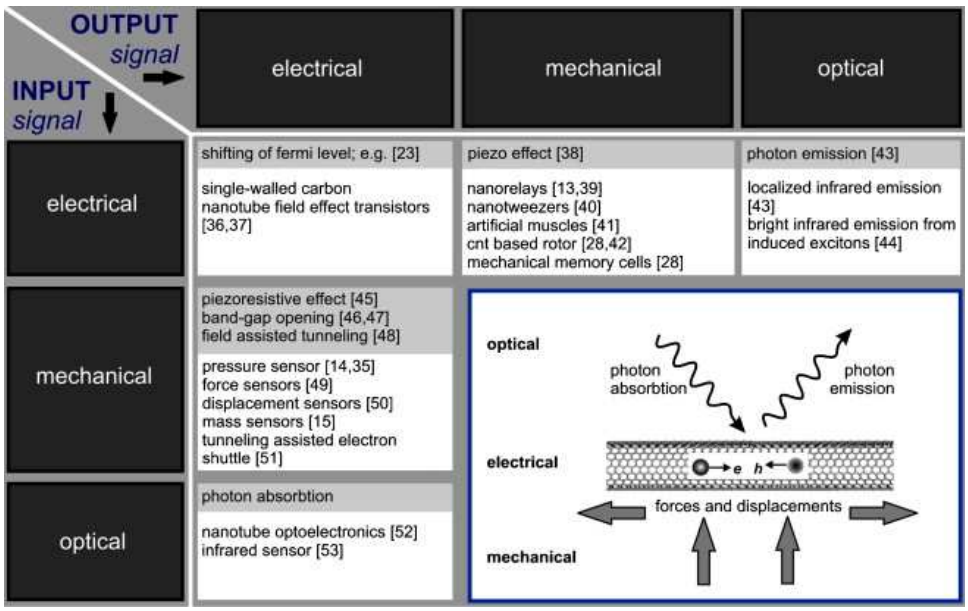


Figure 2.21: Matrix of possible CNTs applications based on electrical, mechanical and optical inputs and outputs. [18]

The fabrication of microelectromechanical systems (MEMS) devices can be divided into three categories:

- Surface Micromachining
- Bulk Micromachining
- Microforming

During surface micromachining the substrate is used only as a base to build the devices on. The material to be used is deposited on the wafer and then shaped by etching or lift off techniques. Bulk micromachining in comparison removes bulk sections of the substrate to create the devices. Microforming is comparable to surface micromachining where the devices are built on top of the substrate, however the thicknesses of the devices are greater than what we get in surface micromachining.

2.4.1.1 CNTs on PolyMUMPs. A. Jungen, et. al. proposes a method using PolyMUMPs to build a microelectromechanical test structure (Figure 2.22) to perform electromechanical studies on CNTs. The fabrication process is shown in Figure 2.23. The first step (Fig. 2.23 (a)) consists of spinning polymethyl methacrylate (PMMA), a positive resist, 400 nm thick over the 2 mm x 2 mm chip. Electron beam lithography followed by development with methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) at a ratio of 1:3 for 3 minutes is then used to clear a 2 μm area to place the catalyst metal for CNT growth. The catalyst is deposited as a droplet

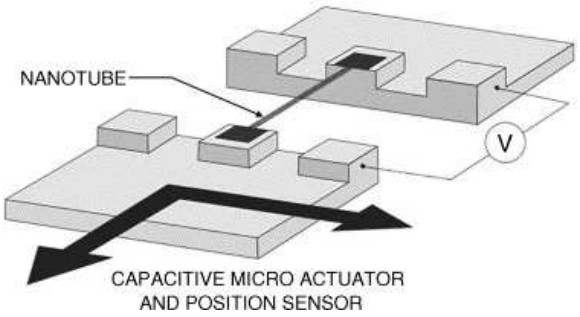


Figure 2.22: Proposed MEMS test structure to perform electromechanical studies of CNTs. [17]

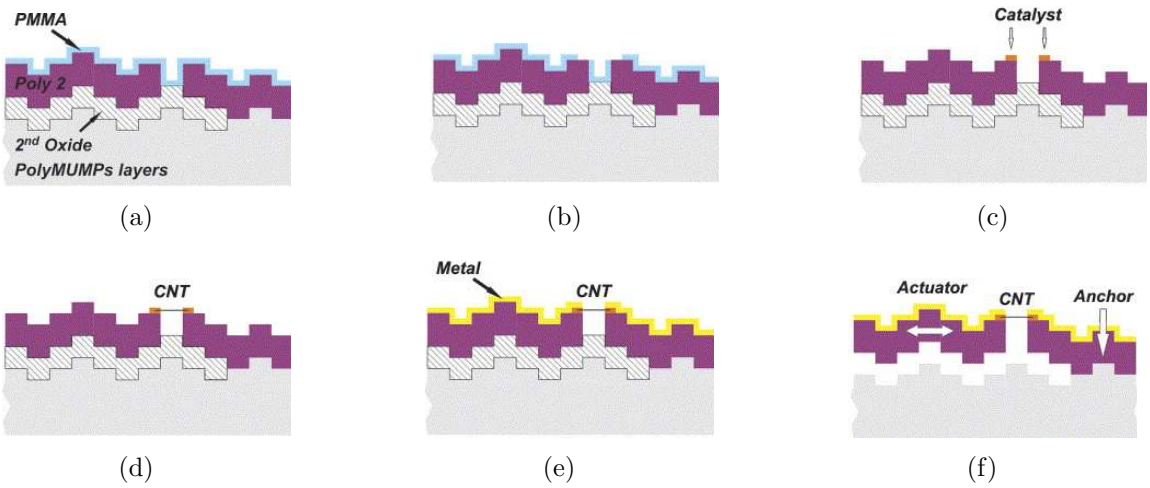


Figure 2.23: (a) Spin coating resulting in 400 nm thick resist. (b) Electron Beam Lithography followed by resist development MIBK:IPA 1:3 for 3 minutes. (c) Catalyst Deposition. (d) CNT growth using LPCVD reactor at 900 °C, for 10 minutes. (e) Metallization. (f) HF Release. [17]

consisting of iron nitride and methanol. The methanol is evaporated by placing the chip on a hot plate at 40 °C (Fig. 2.23 (b)). The PMMA is lifted off and completely removed by putting it in acetone under ultrasonic agitation (Fig. 2.23 (c)). CNT growth takes place in a low-pressure chemical vapor deposition (LPCVD) chamber at 900 °C for 10 minutes. Methane is introduced into the chamber at 100 mbar to interact with the iron and create CNTs (Fig. 2.23 (d)). The next step is to use e-beam lithography and lift off procedures to pattern a layer of Cr/Au used for electrical connections (Fig. 2.23 (e)). The last step involves releasing the MEMS structures using hydrofluoric acid (HF) (Fig. 2.23 (f)) [17].

Figure 2.24 shows the composition of the gold layer after it has been exposed to 900 °C during the CNT growth. The gold melted on the left side of the structure and might cause it to be attached to the substrate. The gold surface also appears to have an increased surface roughness. A way to alleviate this problem would be to use chromium (Cr) that has a melting temperature of 1907 °C instead of gold that has a lower melting temperature of 1064 °C [19]. Another issue with this process is that

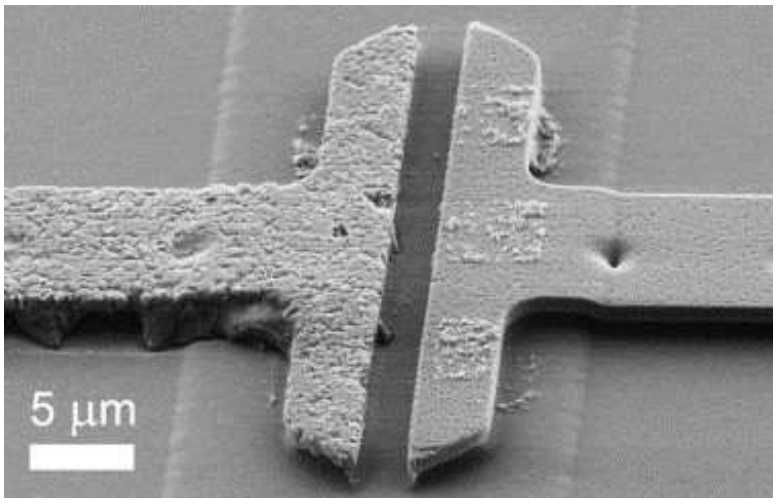
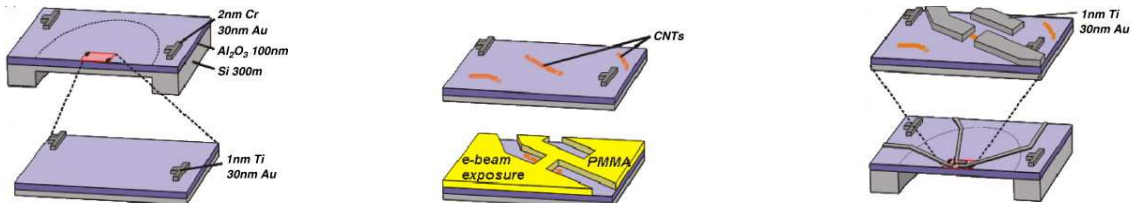


Figure 2.24: Defects on Gold layer after CNT growth in LPCVD reactor at 900 °C. [17]

the direction of CNT growth is random and only the CNTs that bridge the 2 μm gap will contribute to the MEMS structure. [17]

2.4.1.2 Membrane-based Electromechanical Transducer. Hierold, et. al. introduces a method to fabricate an electromechanical transducer that uses a SWCNT as an electromechanical piezoresistive transducer. A typical process flow for the integration of a pressure sensor using CNTs is shown in Figure 2.25. First a 100 μm thick alumina layer is deposited by atomic layer deposition (ALD) followed by the creation of global front side alignment markers made out off 30 nm of Au and 2 nm of



(a) (b) (c)

Figure 2.25: (a) 100 nm alumina is grown over Si substrate followed by global markers. The backside is aligned using the global markers and etched. Local markers are patterned by e-beam lithography. (b) CNTs are adsorbed on the alumina surface followed by contact electrode patterning by e-beam. (c) Physical vapor deposition is used to create contact electrodes. [18]

Cr. The global alignment markers are used to align the substrate for the back side dry etch process (Figure 2.25 (a)). The second step consists of making two local markers out of 1 nm Ti and 30 nm Au on top of the alumina layer as shown in Figure 2.25 (a). The local alignment markers will be used to find the relative position of the SWCNTs on the substrate. SWCNTs are then placed on a dodecylsulphate solution and spread over the alumina surface. The alumina surface adsorbs the dodecylsulphate solution leaving only the SWCNTs as shown in Figure 2.25 (b). EBL is then used to pattern the photoresist for the placement of contact electrodes (Figure 2.25 (b)). EBL is used due to the fact that no mask is needed and the CNT placement is random. The contact electrodes are formed by PECVD with 1 nm Ti and 30 nm Au followed by an annealing process to improve contact between the electrodes and the CNTs (Figure 2.25 (c)). The final step is to release the alumina membrane from the Si wafer (Figure 2.25 (c)). [18]

The end product of this process is shown in Figure 2.26. Pressure is applied on the alumina membrane, deposited using atomic layer deposition, causing it to be strained and it applies an axial stress on the SWCNT resulting in a piezoresistive effect. The SWCNTs first adhere to the membrane surface by van der Waals forces and are then physically and electrically clamped by the contact electrodes. When a differential pressure of 1.4 X 10^5 Pa is applied to the membrane it strains the SWCNT by 0.05 percent [18]. Strain on the SWCNT causes its resistance to increase resulting in a resistance vs pressure dependency. [18]

2.4.1.3 Suspended CNT Electromechanical Transducer. The process discussed in Section 2.4.1.2 can be used to create a suspended CNT transducer with two variations. The final membrane release etch is substituted and instead HF is used for the etching and release followed by drying in a CO_2 dryer. A device like the one in Figure 2.27 can be fabricated with the second method. The force applied to the device changes the resistance, due to the deformation of the CNT, and while voltage is kept constant, a change in current occurred. The change in current is directly related to

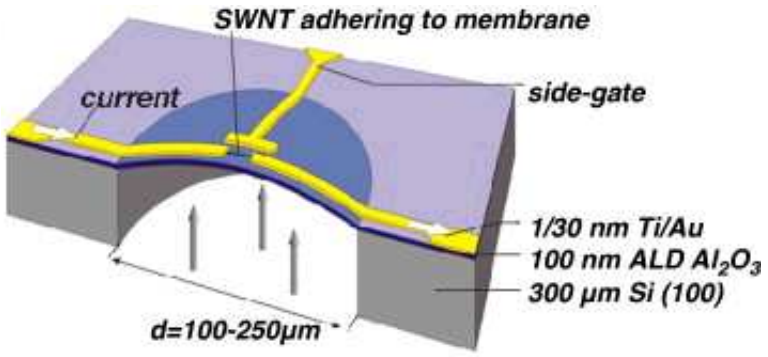


Figure 2.26: Illustration of membrane based electromechanical transducer. [18]

the pressure applied. The main difference between this method and the one discussed in Section 2.4.1.2 is that there is deformation at the tube instead of the membrane. Hierold, et. al. constructed the device in Figure 2.27 and applied pressure using the tip of an atomic force microscope and calculated the change in resistance by using $R = \frac{V}{I}$ (Figure 2.28). They measured a resistance around 300 kΩ with zero deflection and 5.5 MΩ when the nanotube was deflected 35 nm. [18]

2.4.1.4 Growth of CNTs on Microheaters. CNT growth takes place in temperatures between 650 °C and 1700 °C depending on the method used. The high temperatures would affect any type of CMOS device. To alleviate high temperature

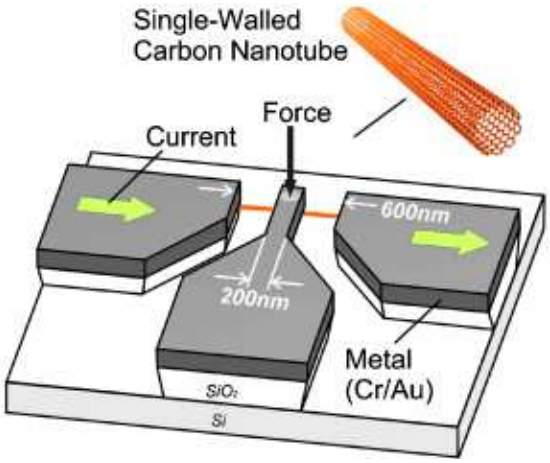


Figure 2.27: Illustration of a Suspended Electromechanical Transducer. [18]

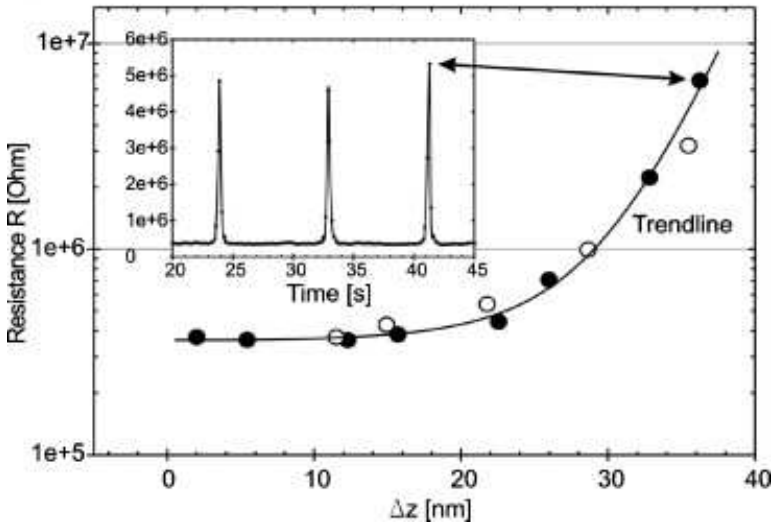


Figure 2.28: Electromechanical Measurements of a Suspended CNT Sensor. Resistance is plotted in a log scale vs change in z due to deflection. (•) indicates when the AFM is pushing down on the CNT and (◦) when the AFM is not applying a force on the structure. The inset demonstrates the reproducibility of resistance due to deflection. [18]

problems and amorphous carbon contamination Hierold, et. al. proposes a modified chemical vapor deposition growth method in which a microheater is used to heat the CNT catalyst while keeping the rest of the wafer at a lower temperature. The microheater to be used is depicted in Figure 2.29 (a). The microheater is to be placed inside a vacuum chamber where hydrogen and methane will be introduced for CNT growth (Figure 2.29 (b)). The combination of heat (temperatures up to 1200 K at the microheater are reported) and growth gasses will result in CNT growth (Figure 2.29 (c)). Hierold, et. al. reported that growth of small diameter nanotubes occurred in the hotter regions while bundles of single-walled and multi-walled CNTs was preferential to the colder regions (Figure 2.29 (d)).

2.4.2 Electrical Applications. The two main electrical applications of CNTs currently being studied are field emitters for displays and thruster applications and field effect transistors (FET).

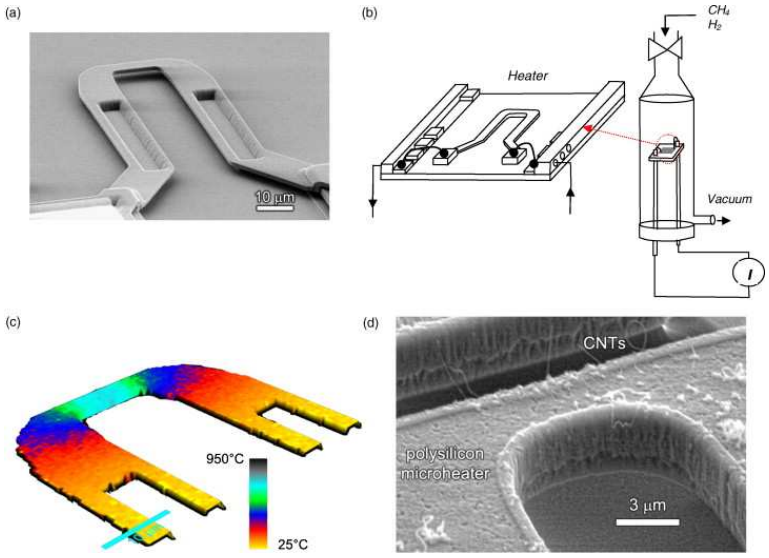


Figure 2.29: (a)Scanning electron microscope image of a microheater. (b) Diagram of CNT growth system using a microheater to supply the heat needed for CNT growth. (c) Temperature distribution of a microheater taken by confocal Raman scattering. (d) Grown CNTs on tips of microheaters. [18]

2.4.2.1 Field Emission. Field emission is the "primary mechanism by which electrical breakdown in a vacuum occurs" [20]. Fowler-Nordheim theory describes the effects of field emission on carbon nanotubes. Field emission, sometimes called cold emission, occurs by placing a strong electrical field close to the cathode, that has a sharp tip, to extract its electrons. This phenomenon is controlled by the voltage gradient between the cathode and anode, on a diode device, or gate on a triode device. [20]

The high electric field seen at the tips of the cathode causes a potential barrier narrowing effect as seen on Figure 2.30. When no voltage is being applied to the gate or anode, the potential barrier at the cathode vacuum interface is illustrated in Figure 2.30 (a). Image force is the force between two charges, in this case the force between the electron in the CNT and the positively charge particle representing an infinitely conducting sheet [3]. Figure 2.30 (b) illustrates the effects of the image force on the vacuum cathode interface. When a voltage is applied to the anode or

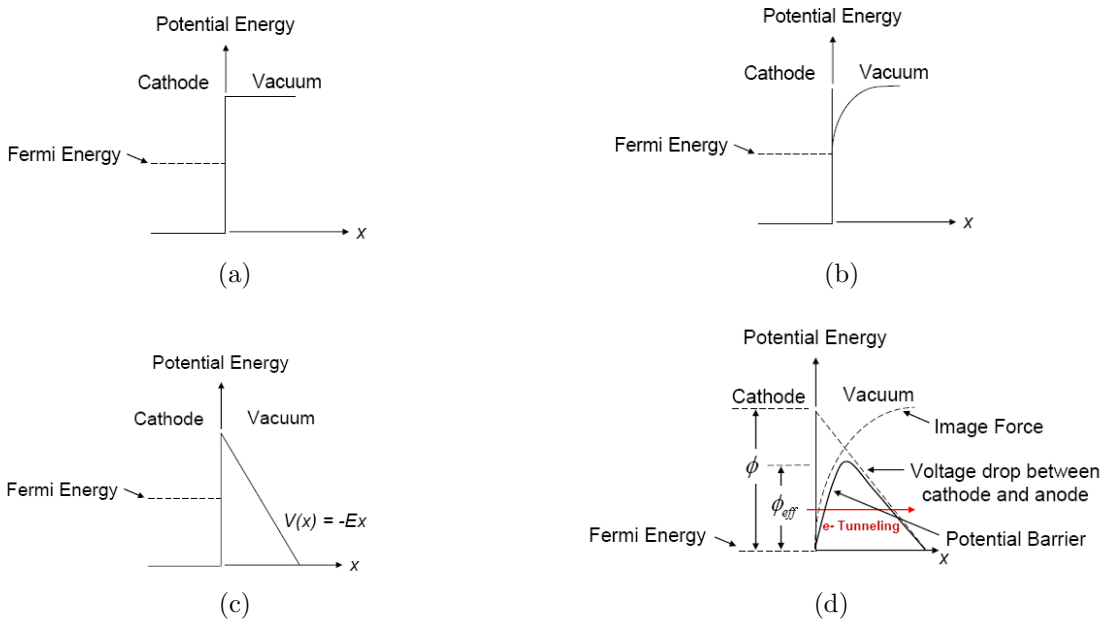


Figure 2.30: Figures of idealized energy barriers at cathode-vacuum interface. The x indicates distance from cathode to anode. (a) Ideal conditions no bias applied. (b) Image forces interacting with energy bands. (c) Effects with an applied voltage. (d) Superposition of imaging forces and applied voltage. [3]

gate, there is a lowering of the potential barrier as illustrated in Figure 2.30 (c). Figure 2.30 (d) illustrates the superposition of image forces and an applied voltage to the gate or anode. The result is a narrowing of the energy barrier promoting electron tunnelling from the cathode to a source with a positive potential. [3]

2.4.2.2 Fowler-Nordheim Theory. The metric used to measure how effective a field emitter is working is either current density or by the field enhancement factor. The following equations are derived from Fowler-Nordheim theory to calculate the current density J_{FE} with units of amps per area^2 [20]

$$J_{FE} = \frac{1.54 \times 10^{-2} F^2}{\phi t^2(y)} e^{\frac{-6.83 \times 10^9 \phi^{1.5} v(y)}{F}} \quad (A/m^2) \tag{2.7}$$

where ϕ is the work function of the emission tip, F is the electric field (V/m) at the cathode, and t(y) and v(y) are special tabulated functions of ϕ the work function and F where t(y) is generally slowly varying and equals unity as shown in Figure 2.31.

One of the difficulties when using Equation (2.7) is trying to calculate the area that is affected by the electric field. To overcome the area problem affected by the electric field (F) it can be rewritten as [20]

$$F = \beta \frac{V}{d} \quad (V/m) \tag{2.8}$$

where β is the field enhancement factor, V is voltage and d is the gap length between the cathode and anode or gate. Another part that is needed is to substitute J_{FE} by [20]

$$J_{FE} = \frac{I}{A} \quad (A/m^2) \tag{2.9}$$

where I equals the total measured emission current and A is the emission area [20]. By substituting Equation (2.8) and Equation (2.9) into Equation (2.7)

$$\left(\frac{I}{A}\right) = \left(\frac{1.54 \times 10^{-2} \beta^2 V^2}{\phi t(y)^2 d^2}\right) e^{\frac{-6.83 \times 10^9 \phi^{1.5} v(y) d}{\beta V}} \quad (A/m^2) \tag{2.10}$$

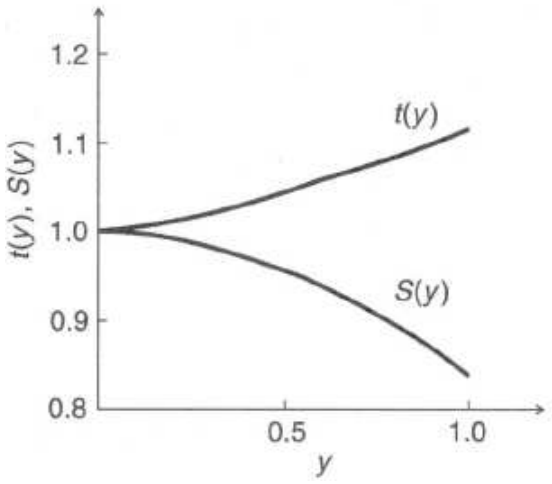


Figure 2.31: Behavior of t, a special tabulated function, as a function of y [2]

moving the A to the right side of the equation and V^2 to the left

$$\left(\frac{I}{V^2}\right) = \left(\frac{1.54 \times 10^{-2}\beta^2 A}{\phi t(y)^2 d^2}\right) e^{\frac{-6.83\times10^9\phi^{1.5}v(y)d}{\beta V}} \quad (A/V^2) \tag{2.11}$$

and taking the ln of both sides we get the following; [20]

$$\ln\left(\frac{I}{V^2}\right) = -\ln\left(\frac{\phi t(y)^2 d^2}{1.54 \times 10^{-2}\beta^2}\left(\frac{1}{A}\right)\right)\left(-\frac{6.83 \times 10^9 v(y)\phi^{1.5} d}{\beta}\left(\frac{1}{V}\right)\right) \tag{2.12}$$

Equation 2.12 can be used to calculate the emission area (A). Using field current measured as a function of voltage plotted on a log should result in a straight line where we can get β which will be the slope of the line. Once we have the slope, the only unknown of Equation 2.12 will be the emission area. [20]

In the literature for CNTs we usually see references to the enhancement factor β instead of the emission area A. The reason for this is that values of A that result lead to unrealistic results when applied to small cathodes like CNTs. This is most likely caused by insulating impurities encountered during testing [20]. To calculate β for CNTs the following equation is used [21]

$$\beta = 0.95B\phi^{3/2}d/b \tag{2.13}$$

where b is the slope of the F-N plot, ϕ is the work function of CNTs (4.5eV), d (length) is the distance between the anode and cathode, and B a constant is 6.87×10^7. [21]

Since the characterization of carbon nanotube field emission properties, CNTs have become a strong choice for future development of field emission devices [22]. Figures of merit include turn-on voltage which is the voltage at which a minimum current is measured at the anode, maximum current density or field from the device measured at the anode, tube/array spacing and arrangement of CNTs which include carpet or arrays. Figures of merit for these researches have been summarized in Table 2.1. From Table 2.1 it is clear that the way the array is arranged affects the maximum current density for the device under test. There are other aspects which

affect current density, an example is the type of configuration for the device. A diode configuration is constructed by applying a ground to the CNTs that are functioning as a cathode while applying a large voltage to the anode. Also, a triode configuration can be used in which the cathode is grounded, the gate has a positive voltage and the anode is set at a higher potential. For the triode configuration, the gate acts to extract the electrons at a lower potential and the anode is used to accelerate the electrons. The effects of differential potentials at the gate can be seen in Figure 2.32, 20 V on the left and 100 V at the right, helps to shape the electron trajectory into a tighter beam. Indium tin oxide (ITO) is commonly used as an anode due to its

Table 2.1: Figures of Merit from Multiple Papers

Author	Arrangement	Tube/Array Spacing	Turn-On Voltage or field	Max Current Density or Field
Wong [22]	Array 4 μm in diameter	20 μm	2.0 $V/\mu m$ at 1 $\mu A/cm^2$	100 $\mu A/cm^2$ at 3 $V/\mu m$
	Array 18 μm x 18 μm	12 μm	3.2 $V/\mu m$ at 1 $\mu A/cm^2$	30 $\mu A/cm^2$ at 5 $V/\mu m$
	Trenched Array 10 μm x 10 μm	20 μm	9 $V/\mu m$ at 1 $\mu A/cm^2$	100 $\mu A/cm^2$ at 20 $V/\mu m$
	Trenched Array 10 μm x 10 μm	50 μm	14 $V/\mu m$ at 1 $\mu A/cm^2$	70 $\mu A/cm^2$ at 27 $V/\mu m$
	Trenched Array 10 μmx 10 μm	100 μm	14 $V/\mu m$ at 1 $\mu A/cm^2$	100 $\mu A/cm^2$ at 25 $V/\mu m$
Huh [23]	Array		55 V	20μA at 100 V on the gate
Brunetti [24]	Carpet		40 V	0.85 μA at 115 V on the gate
Yu [25]	Array		2.8 $V/\mu m$	40 mA/cm^2
Wong [14]	Array		16.5 $V/\mu m$	1.2 mA/cm^2
Wong [26]	Array	20 μm	25 V	0.95 μA
Wong [27]	Array		2.93 $V/\mu m$	74 mA/cm^2
Li [21]	Array		4 $V/\mu m$ from onset	1 mA/cm^2 at 9.5 $V/\mu m$

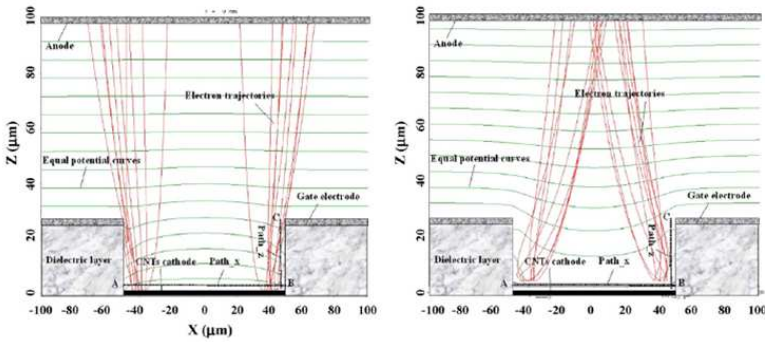


Figure 2.32: The left figure shows the electron trajectories with 20 V applied at the gate. The right figure shows a much tighter electron trajectory with 100 V applied to the gate [28].

transparent properties and conductivity. ITO's carrier concentration has to be kept low for it to keep its transparent characteristic.

Table 2.2 demonstrates how configuration, catalyst, and growth process can affect the maximum current density or field of the CNTs. The combination of a triode configuration and a Microwave Plasma Enhanced Chemical Vapor Deposition (MPECVD) growth process results in a higher current density.

Important electrical aspects extracted from the literature follow:

- MWCNTs are preferred for field emission due to robustness over SWCNTs.
- Bundles of CNTs will have a higher yield than single CNTs. A bundle of CNTs will be able to survive longer times compared to individual CNTs. As one CNT burns up a different CNT on the bundle will begin its field emission.
- When a multi walled CNT bundle shape is needed, PECVD is the preferred method. This is due to the attraction of the catalyst metals to the plasma that is being produced in the system. The plasma will guide the CNTs to grow vertically.
- Annealing of catalyst prior to CNT growth will shape the geometry of the bundle. By annealing the catalyst, nanoparticles of different dimensions and

Table 2.2: Device Configuration and Maximum Current Densities from Multiple Papers

Author	Configuration	Catalyst	CNT Growth Process	Max Current Density or Field
Wong [22]	Diode	Co	MPECVD	100 $\mu A/cm^2$ at 3 $V/\mu m$
	Diode	Co	MPECVD	30 $\mu A/cm^2$ at 5 $V/\mu m$
	Diode	Co	MPECVD	100 $\mu A/cm^2$ at 20 $V/\mu m$
	Diode	Co	MPECVD	70 $\mu A/cm^2$ at 27 $V/\mu m$
	Diode	Co	MPECVD	100 $\mu A/cm^2$ at 25 $V/\mu m$
Huh [23]	Triode	Fe	Thermal CVD	20μA at 100 V on the gate
Brunetti [24]	Triode	Fe	HWCVD	0.85 μA at 115 V on the gate
Yu [25]	Diode	Fe	CVD	40 mA/cm^2
Wong [14]	Triode	Ni	MPECVD	1.2 mA/cm^2
Wong [26]	Triode	Ni	MPECVD	0.95 μA
Wong [27]	Triode	Ni	MPECVD	74 mA/cm^2
Li [21]	Diode	Fe	CVD	1 mA/cm^2 at 9.5 $V/\mu m$

shapes are created. The particles on the edges create CNTs that are shorter compared to the center creating a convex shaped geometry.

2.4.2.3 Field Effect Transistor. CNTs are used to bridge two electrodes that act as the source and the drain while the CNT functions as the conduction channel. The CNT FETs can be either back gated or top gated. In back gated CNT FETs (Figure 2.33), van der Waals forces keep the CNTs attached to the two metal electrodes. Due to this type of connection, these devices do not achieve high drive currents or high transconductance. The back gated FET uses the silicon wafer as the gate. To isolate the gate and the CNT, a silicon dioxide (SiO_2) layer is deposited in between the CNT and the wafer.

In the top gated FET, a layer of SiO_2 is deposited on top of the wafer followed by the CNT. The SiO_2 acts to isolate the CNT and wafer as the two metal electrodes

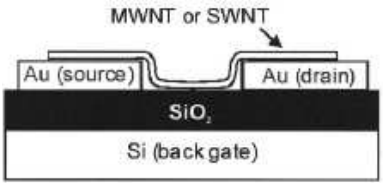


Figure 2.33: A MWCNT or SWCNT is used as the channel for conduction between two metal electrodes while the silicon wafer is used as the gate. Silicon dioxide is used to electrically isolate the gate, Si wafer, and the channel, CNT. [15].

are deposited over the CNT to act as the drain and source of the FET. This is followed by another SiO_2 layer to isolate the CNT, source and drain from the final metal to be deposited that will act as the gate. Thermal annealing is used to create a stronger bond between the CNT and the source and drain electrodes. Figure 2.34 shows the I_d-V_{gs} curves for a top gated CNT FET. The contact resistance for the top gated FET is 30 kΩ compared to the bottom gated FET resistance of $\geq$ 1 MΩ. Current also reaches the μA level and transconductance is 0.34 μS which is 200 times higher than one obtained from the back gated CNT FET [15]. As with standard FETs, time and research is needed to investigate more efficient ways to fabricate CNT FETs to improve the efficiency of these devices. [15]

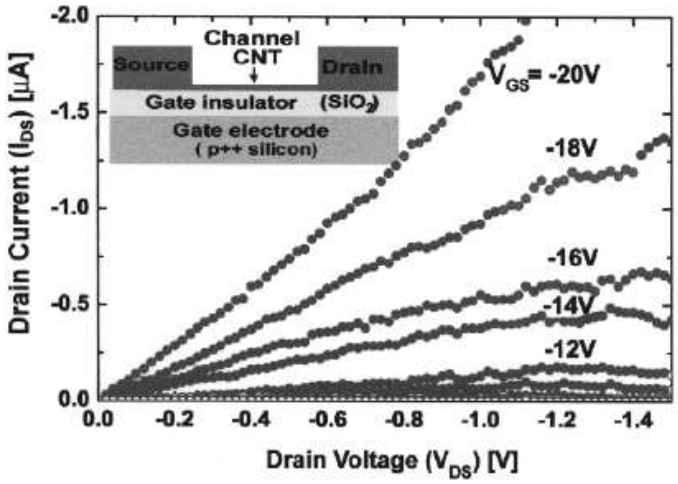


Figure 2.34: Output characteristics of a top gated CNT FET. [15].

2.5 Chapter Summary

This chapter provided a in-depth review of the structure of CNTs to include single wall and multi wall, a study of electrical arc discharge, surface decomposition and CVD methods for CNT growth, and the electrical and mechanical properties and applications of CNTs.

III. Design and Fabrication

The design and fabrication of CNT structures has to take many aspects into consideration not usually thought of when working in the micro world. First of all when it comes to the testing of CNT field emitters, an atmosphere of at least 10^{-5} torr is needed. CNTs differ when working with a carpet of catalyst that has not been shaped to one that has been. The design to be used also affects the maximum current density and the turn on voltage of the device being tested.

3.1 Field Emission Testing

3.1.1 Vacuum Chamber. CNT field emitters need to be characterized under vacuum. To be able to accomplish this at AFIT a system had to be purchased that fit the following characteristics:

- Vacuum system (chamber, load lock, flanges, and pumps) capable of sustained operation at 10^{-9} torr pressure.
- The main vacuum chamber must have:
  - A minimum of eight flanges (ports) on the main vacuum chamber. Unused ports must be adequately capped or used as viewports.
  - At least one 8" flange for possible interfacing with a government furnished equipment (GFE) ion pump.
  - A minimum of eight electrical feedthroughs that are rated for greater than 500 volts and ensure the transport of current in the range of picoamps up to a few amps.
  - A minimum of 2 viewports oriented on the center of the chamber.
  - Ability to accommodate a 2.8" $\times$ 2.8" $\times$ 2" sample volume in the center of the chamber.
  - A dry vacuum pump able to pump from 1×10^{-3} to 1×10^{-6} torr in less than 60 min and achieve an ultimate pressure of at least 10^{-9} torr. A GFE

rough pump, capable of reaching to 10^{-3} torr, will be provided with KF25 connection for main chamber roughing.

  - Ability to vent or open chamber without shutting down pumps that provide high vacuum.

- Pressure measurement system capable of measuring and displaying pressure from atmosphere to 10^{-9} torr in any and all chambers.
- The ability and equipment needed to vent any and all chambers.
- High vacuum/high voltage rated electrical cables to connect all eight feedthrough pins to reliable push connections on the sample mount. Thus, these cables must be able to span the longest internal chamber distance. Connections will be provided by bidder. GFE sample mount will have push connections to the sample platform which will be "fastened" inside the main chamber.
- All components must be able to be assembled without welding.

A survey of companies available to accommodate these requirements resulted in Kurt J. Lesker as the only company that was able to supply the needed materials in time to build a suitable system for field emission. The parts list is included in Appendix A. To achieve the required pressure, ConFlat (CF) flanges had to be used. A CF flange uses a knife-edge under the flanges flat surface to cut into a soft metal gasket and create a seal. Figure 3.1 illustrates a schematic of the vacuum system components needed to fulfill all requirements. Four gate valves are needed to isolate different components in the system. Three of these gate valves were used in the main vacuum chamber to isolate the main vacuum chamber from the load lock, isolate the venting valve and isolate the turbo pump. The last gate valve is used to isolate the load lock and its turbo pump. By isolating the turbo pumps from the main chamber and load lock venting to atmosphere can take place while the turbo pumps are left running. To be able to measure from atmosphere to 10^{-9} torr, two different kinds of gauges need to be used. A convection gauge is used to measure from atmosphere to 10^{-3} torr. Two gauges were installed; one in the main vacuum chamber and one in

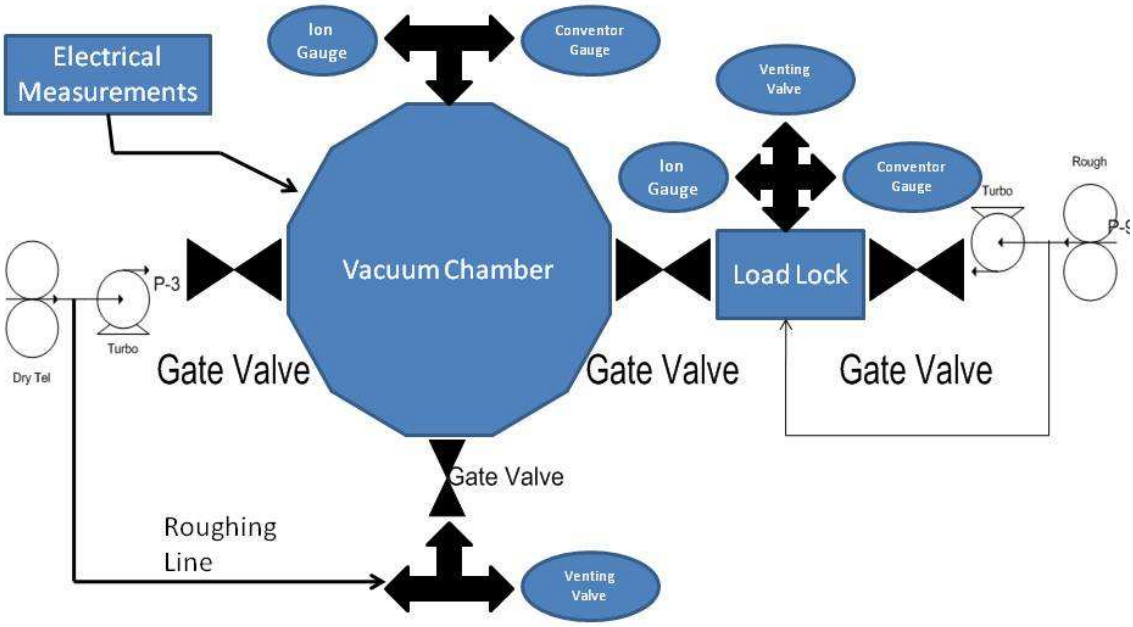


Figure 3.1: Illustration of Vacuum system components.

the load lock. To measure from 10^{-3} torr to 10^{-9} torr two ion gauges were purchased and installed in the main chamber and load lock. To be able to achieve a pressure of at least 10^{-6} torr, a turbo pump and rough pump combination are needed. Rough pumps are used to bring the chamber and load lock from atmosphere to 10^{-3} torr and also to back up the turbo pumps. Turbo pumps are to be always operated at a minimum inlet pressure of 10^{-3} torr and have a outlet pressure of at least 10^{-2} torr. By having the rough pump backing up the turbo, the 10^{-2} torr outlet pressure is achieved. When designing the field emission test chamber, inline valves were placed on the outlets of the rough pumps to be able to only rough out the vacuum chamber or load lock, back up the turbo pumps or to do both roughing and backing of the turbo pumps. Due to the high voltages needed in a field emission testing, mini high voltage connectors will be used that are rated to voltages up to 5 kV.

3.1.2 Electrical Connections. To connect the device under test to voltage supplies located outside of the chamber, a circuit board had to be created. Due to the vacuum environment needed to conduct testing, commercial printed circuit

boards that are made out of polymers could not be used. Instead a sapphire wafer was used to create the printed circuit board needed. The process follower is located in Appendix B. A pre-metal dip of the wafer in a buffered oxide etch (BOE) is accomplished to remove impurities on the wafer. Shipleys 1818 photoresist, a positive photoresist, is then spun over the wafer at 500 rpm for the first 10 seconds to help spread it out over the entire wafer surface followed by a spin at 4000 rpm for 30 seconds to thin the photoresist to get the desired thickness. Nominal thickness for 1818 using this method is approximately 1.8 μm. To be able to get a pattern unto the photoresist a two step process is used:

- Using the EVG 620 mask aligner and a mask created using the layout in Figure 3.2, UV rays strike the photoresist where it is not covered by the mask, making the photoresist susceptible to development. The UV rays hit the photoresist for 3 seconds.
- The second step is to use a developer consisting of deionized water (DIW) and Shipleys 351 developer at a ratio of 5:1. The wafer is spun at 500 rpm for the development time of 60 seconds immediately followed by a DIW rinse to stop the development process.

A plasma asher is then used to remove any left over organic material. A gold layer id deposited 5000 $\mathring{A}$ thick and patterned. The gold is then etched by using a gold etchant TFA sold by Transene company that etches at a rate of 28 $\mathring{A}$/sec. Only areas not covered by the photoresist are etched leaving the pattern shown in Figure 3.2.

3.2 Triode Structure Fabrication

The device that was fabricated consisted of two different wafers. A silicon wafer was used to create the cathode and gate structure. A quartz wafer was used to create the anode.

3.2.1 Anode Fabrication. The anode and gate needed to be separated by at least 50 μm. This was to be accomplished by using a quartz wafer, a dielectric,

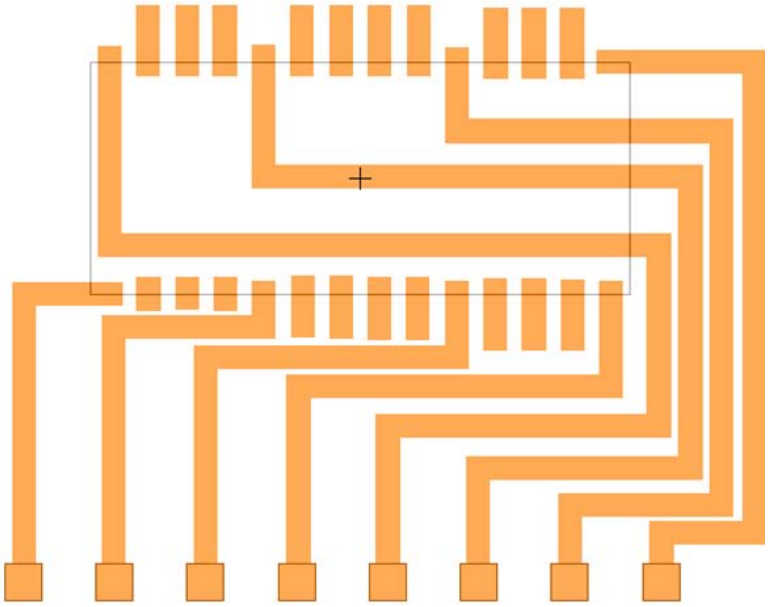


Figure 3.2: Layout of Printed Circuit Board created in L-Edit.

and etching 50 μm using ICP-RIE followed by the deposition of gold on the bottom surface as shown in Figure 3.3.

The process follower is located in Appendix C. The process follows the same principles as the PCB fabrication. The difference is that instead of adding materials we are subtracting some of the bulk substrate material, a process refereed to as bulk micromachining.

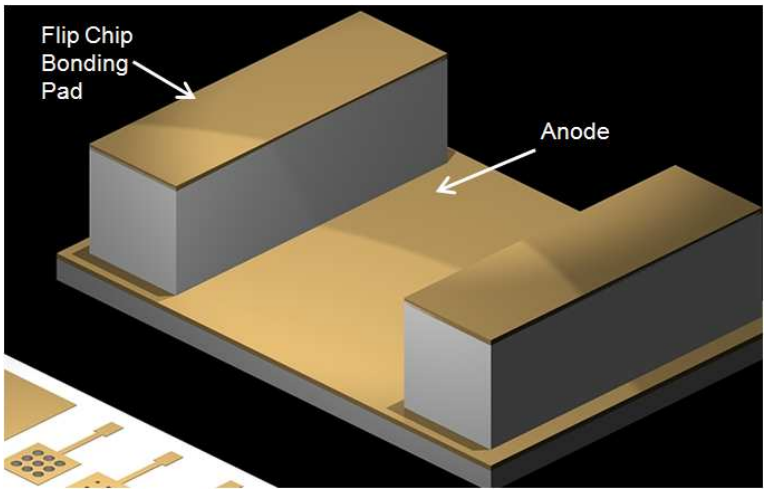


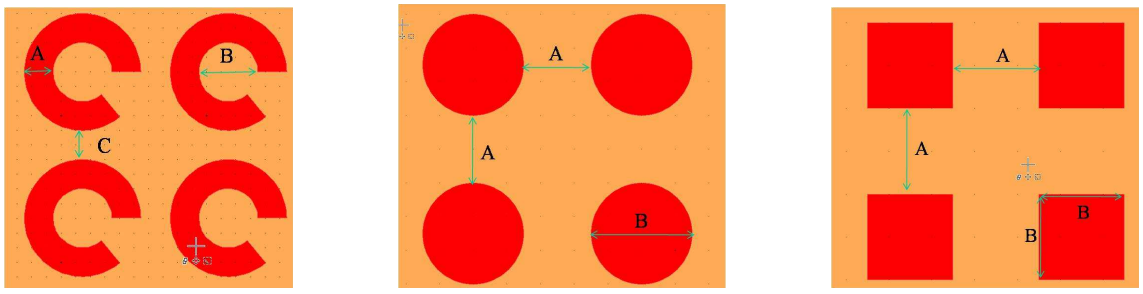
Figure 3.3: Anode design.

3.2.2 Cathode and Gate Fabrication. The cathode and gate were fabricated by laying various layers of metals and dielectrics on a silicon wafer, followed by a sequence of etch backs and finally the growth of the CNTs.

The layer structures that were used are as follows:

- A Titanium layer 200 $\mathring{A}$ thick was sputtered as a diffusion barrier and adhesion layer for the 100 $\mathring{A}$ sputtered Nickel layer that acts as the catalyst for CNT growth. The nickel film needs to be thin so that it can be broken up into nano size islands during the CNT growth process.
- A 2 μm silicon dioxide layer was used as a dielectric between the gate and cathode. The electric breakdown of silicon dioxide is greater than 1×10^7 V/cm in thermal oxides and as low as 1×10^6 V/cm in CVD oxides.
- The gate material, Chromium 2500 $\mathring{A}$ thick, will not be affected by hydrofluoric acid which is used during the etch back process followed by a 5000 $\mathring{A}$ thick gold layer that will be used for flip chip bonding and wire bonding.

Three masks were designed using L-Edit and then purchased from Photosciences Corp. to create the desired gate structures. The array mask contains circles, squares and a toroid array as seen in Figure 3.4. Studies performed by Wong [22] demonstrated how the patterning of CNTs affects turn on voltage, current density and growth time. When Wong used a circular pattern, 4 μm diameter circles spaced 20 μm apart,



(a) (b) (c)

Figure 3.4: Arrays to be fabricated. A, B, and C values can be found in Table 3.1. (a) Toroid. (b) Circles. (c) Squares.

the circle array had a lower turn on voltage and higher current density that a CNT carpet [22]. Wong also demonstrated that the growth rate of CNTs when patterned was lower than just growing a carpet on the whole wafer. This study led to the design for AFIT's array mask. Wong demonstrated that by decreasing the array spacing and shaping the CNT bundles, more efficient CNT arrays can be fabricated. Figure 3.5 shows how a 10 $\times$ 10 μm square array with different spacing affects not only the early voltage but also the maximum current density. The array mask fabricated for AFIT has array spacings of 1, 2 and 3 μm to take advantage of this discovery. Wong also noticed the shape of the pattern has an effect on current density and early voltage as seen on Figure 3.6. It is shown that circular arrays having a 4 μm diameter proved to have higher current density than a 18 $\times$ 18 μm square array. For a more accurate comparison AFITs array mask has circle diameters of 1, 2 and 3 μm and squares that have 2 $\times$ 2 μm and 3 $\times$ 3 μm dimensions. The third shape to be incorporated has a toroid like structure. With this shape we will see the CNTs grow taller in the middle of the C channel causing a line of CNT emitters instead of a concentrated point in

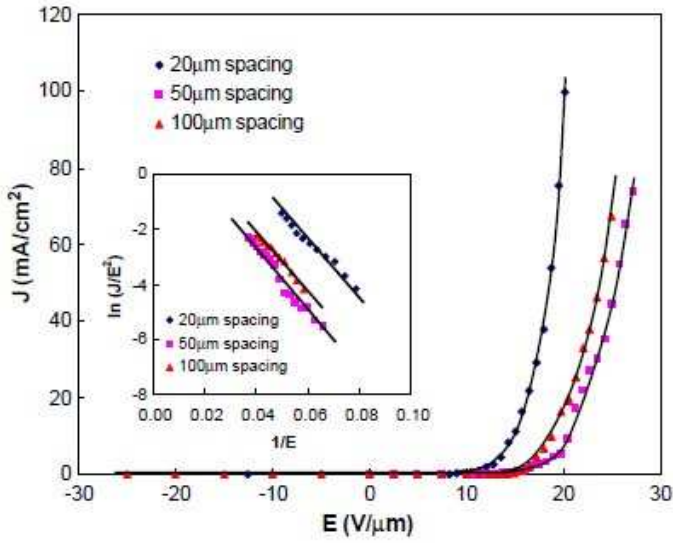


Figure 3.5: Effects on current density due to spacing on a 10 $\times$ 10 μm square array. Inset is the F-N plots of the emission data. [22]

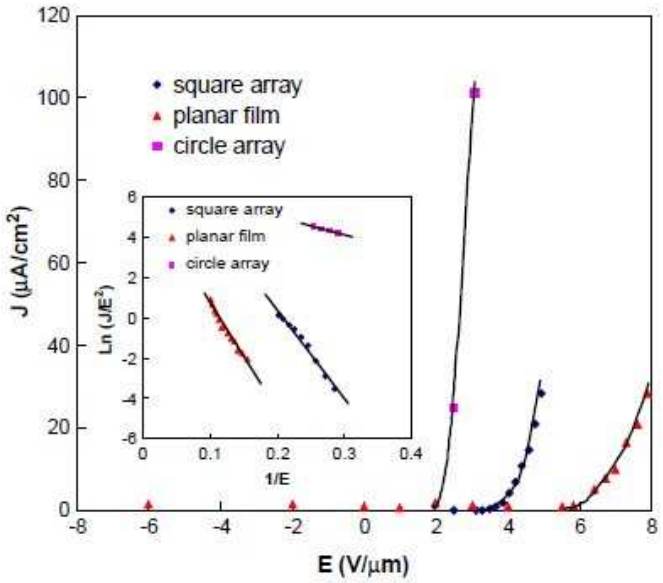


Figure 3.6: Effects on current density due to patterning of CNT arrays into a 4 μm diameter circle array, 18 $\times$ 18 μm square array and a planar film with no patterning. Inset is the F-N plots of the emission data. [22]

the center as with the square and circle arrays. The dimensions and spacings are as shown in Table 3.1 and referenced on Figure 3.4.

The second mask, Figure 3.7, was used to create the gates, flip pads and the electrical bonding pads for the triode structure. The package where this structure will be mounted is manufactured to accept a 1 cm $\times$ 1 cm wafer. As seen from Figure 3.7 the device to be manufactured will be 0.990 cm $\times$ 0.980 cm to be able to fit into the prefabricated package. To facilitate in the flip chip bonding process, the flip chip bonding pads dimension are 700 μm $\times$ 8000 μm. The vacuum chamber was built to accommodate eight electrical connections, one connection will be used as a ground, one for the anode and six connections are left to individually power six separate gates. These gates will have different arrays to be tested without having to take the sample out of the vacuum chamber.

The third mask, Figure 3.8, will be used to create bonding pads for a ground connection. A fourth mask will have to be manufactured to be able to etch the

Table 3.1: Array types, sizes and dimensions for the array mask as shown in Figure 3.4.

Array Type	Array Size	A (μm)	B (μm)	C (μm)
Toroid	200 × 200	2	4	2
	222 × 222	2	4	1
	181 × 181	2	4	3
	333 × 333	1	2	2
	400 × 400	1	2	1
	286 × 286	1	2	3
Circles	500 × 500	2	2	Not Applicable
	666 × 666	2	1	Not Applicable
	400 × 400	2	3	Not Applicable
	666 × 666	1	2	Not Applicable
	1000 × 1000	1	1	Not Applicable
	500 × 500	1	3	Not Applicable
	400 × 400	3	2	Not Applicable
	500 × 500	3	1	Not Applicable
	333 × 333	3	3	Not Applicable
	333 × 333	4	2	Not Applicable
	400 × 400	4	1	Not Applicable
	286 × 286	4	3	Not Applicable
Squares	500 × 500	2	2	Not Applicable
	666 × 666	1	2	Not Applicable
	400 × 400	3	2	Not Applicable
	400 × 400	2	3	Not Applicable
	500 × 500	1	3	Not Applicable
	333 × 333	3	3	Not Applicable

0.5 μm gold layer for wire bonding and flip chip bonding pads. Figure 3.9 illustrates

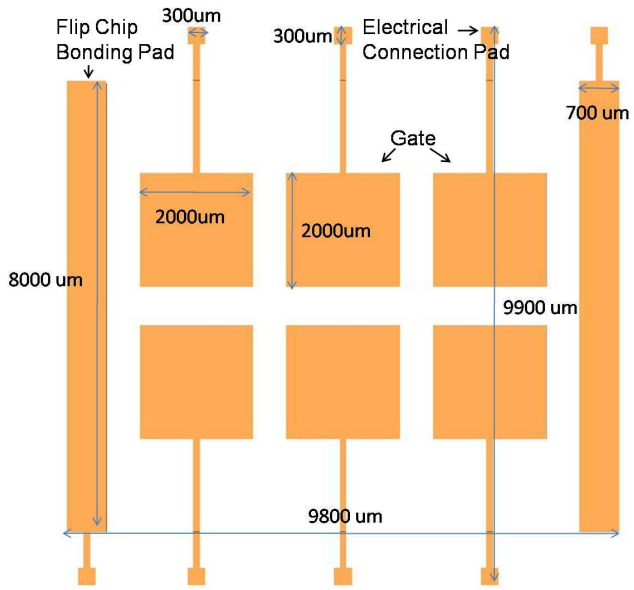


Figure 3.7: Design and dimensions of AFITs gate mask.

the fabrication steps to create the cathode and gate. The process follower to fabricate the device is located in Appendix D.

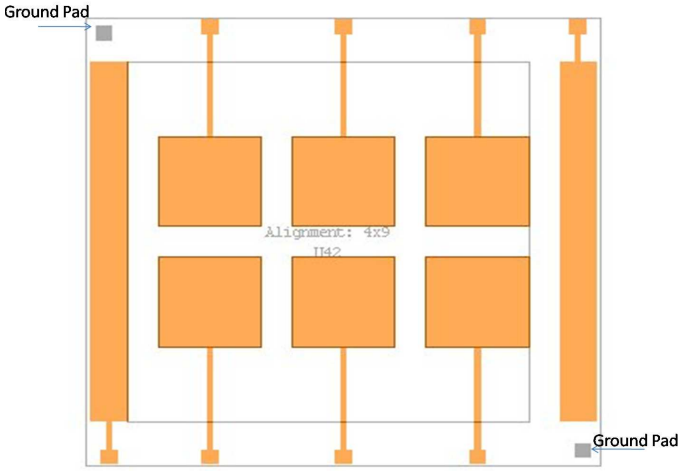


Figure 3.8: Design of AFITs gate mask in regards to the gate mask.

3.3 CNT Growth

CNT growth took place in an ASTeX 1500 watt MPECVD system own by AFRL/RZ. The growth process occurs due to two separate chemical processes. The first process goes in and breaks up the catalyst, nickel in our case, into small size particles. These particle sizes determine the diameter of the CNT to be grown. The

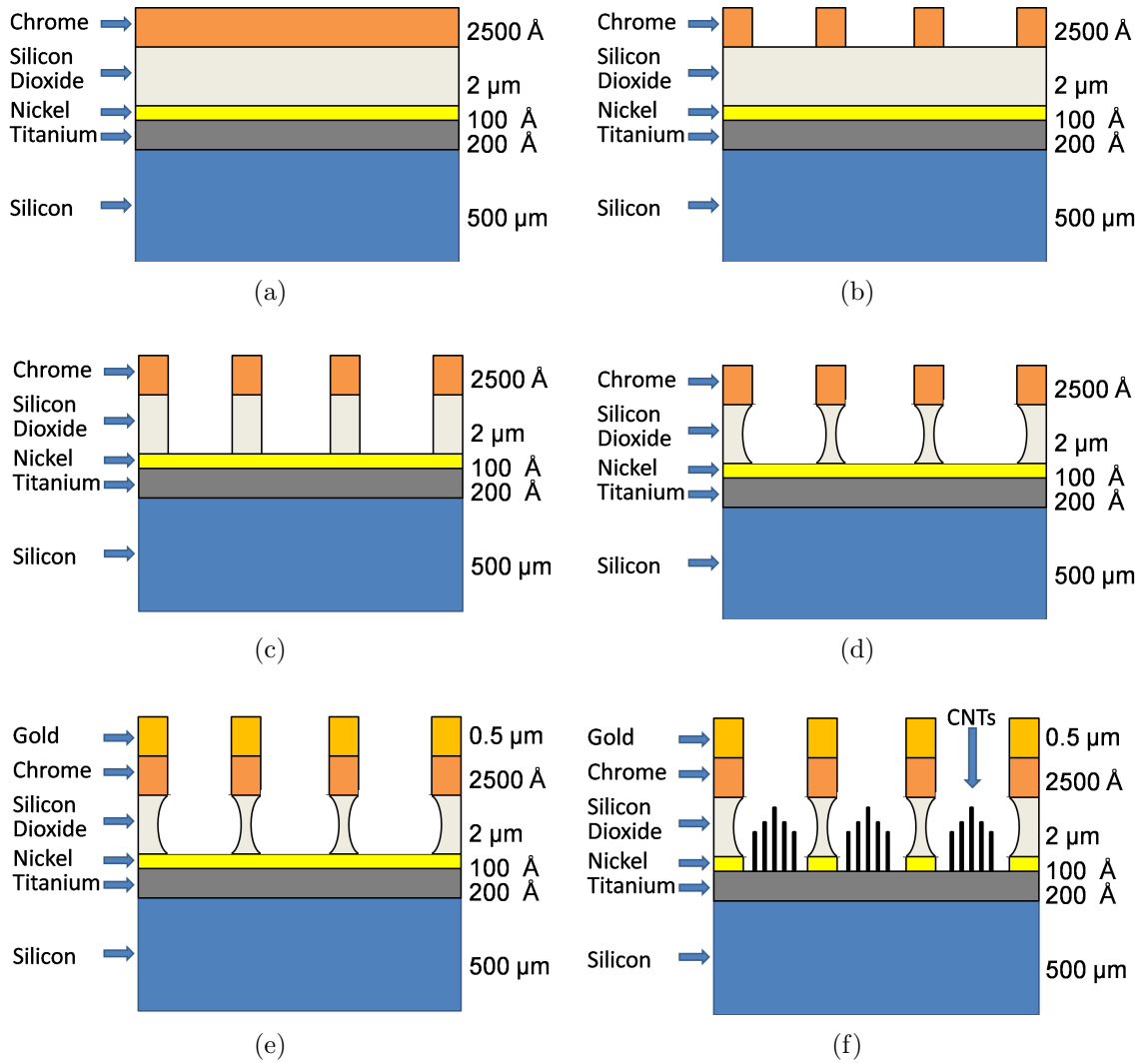


Figure 3.9: Fabrication Process Flow for the Cathode-Gate Wafer. (a) Materials to be deposited and their thicknesses. (b) The first step is to etch the chrome using CR-14 a chrome wet etchant. (c) This is followed by the etching of the SiO_2 through a RIE process. (d) A BOE is then used to isotropically etch the SiO_2. (e) A gold layer is deposited and then etched so that it appears only over the bond pads. (f) The full wafer is introduced into a MPECVD chamber for CNT growth.

second process introduces a hydrocarbon, methane in our case, that combines with the catalyst nickel to induce CNT growth. The MPECVD system can be seen in Figure 3.10.

The system can be divided into vacuum components, microwave components and stage components. The vacuum components include a small vacuum chamber, rough pump able to reach 10^{-3} torr, a convection gauge that measures the pressure between the chamber and pump, and a baratron gauge that measures the vacuum in the chamber and is not affected by any of the gasses used for CNT growth. The convection gauge is controlled by a 340 vacuum controller shown on the top left of Figure 3.10. The baratron gauge controller shown on the left of Figure 3.10 sends the baratron gauge reading to the butterfly valve controller seen on the right of Figure 3.10. To set the desired pressure the butterfly valve controller is set to auto and the desired pressure is set on the set point dial. This will send a signal to the butterfly valve between the chamber and pump to open and close accordingly to maintain the

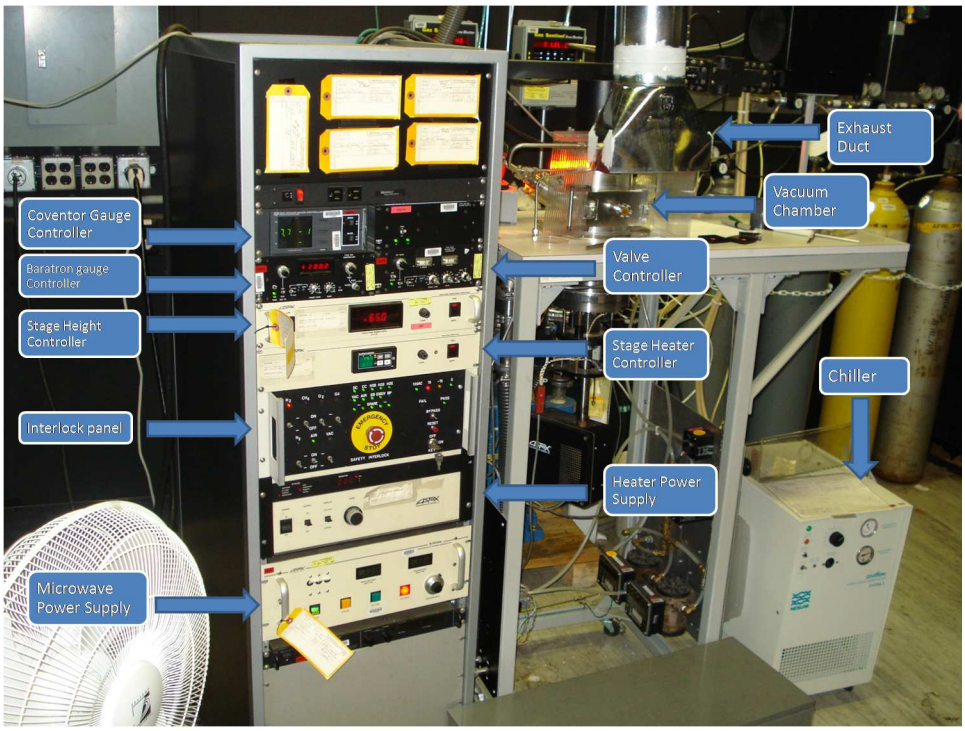


Figure 3.10: AFRL/RZ MPECVD System.

optimal pressure. The stage components include a height controller, motor, and a heating group that is comprised of an RF power supply for heating, thermocouple to measure the temperature of the wafer and a temperature controller. The microwave components include the magnetron, wave guide, a water chiller, two separate tuners and a microwave power supply. To be able to tune the plasma, the height of the stage needs to be taken into account and the two tuners (a fine tuner and a rough tuner) need to be tuned so that the reflective power is between two and six watts. Appendix E specifies the procedures for operating the MPECVD system and Appendix F contains a schematic with electrical, gas and RF connections.

There are many safety aspects to consider when operating this system. The safety interlock panel seen in Figure 3.11 helps mitigate some of the safety concerns when operating the MPECVD system. To be able to operate the system, all four power indicator lights need to be on and all status lights on the middle of the panel with the exception of the BP light, BP stands for bypass, need to be on. Table 3.2 matches the status lights on the interlock panel to devices on the MPECVD system. One of the main safety additions to the MPECVD system was the modification of the exhaust vent over the chamber opening as seen in Figure 3.10. The system is purged with hydrogen and nitrogen before it is opened to evacuate any free flowing CNTs in the chamber. In the unlikely event that there are still free CNTs in the chamber, the exhaust flow will trap and vent them out of the building.

Figure 3.11: AFRL/RZ MPECVD system interlock panel.

Table 3.2: Interlock panel status lights matched to components on the MPECVD system.

Status Light	Device	Troubleshooting
SC and CC	Water Chiller	Chiller on and water turned on
H2B, H2S, H2E	Hydrogen and Methane Sensors	Hydrogen or Methane leak
VAC	VAC Switch on Interlock panel	Not operating
AIR	Air Switch on Interlock panel	Check switch on interlock panel and air solenoid on pump
EB	Not in use	Not in use
EMGY	Emergency Stop on Interlock panel	Turn Emergency Stop Knob
BP	286 Bypass Switch on Interlock panel	Bypass switch is pressed

For the CNT growth, a pretreatment of the nickel catalyst was done by flowing hydrogen at 135 sccm, a substrate temperature of 400 °C and 400 watts from the microwave power supply. The time needed for the pretreatment varies depending on the size of the catalyst particle needed and thickness of the catalyst. For the growth, the hydrogen flow is decreased to 120 sccm and the power of the microwave power supply is increased to 1000 watts while keeping the reflective power between two and six watts. After reaching the required power, the temperature is increased to 650 °C followed by flowing methane at 15 sccm. The time needed for growth and pretreatment is also affected if using a patterned or unpatterned substrate. The reason for this is that the plasma and gasses for chemical interactions have a harder time reaching the catalyst inside the patterned structures. The time needed for the patterned structures is higher than the one for unpatterened structures.

3.4 Chapter Summary

This chapter covered the design and fabrication of a vacuum system and a sapphire PCB board for the testing of CNTs as field emitters. It also covered the design and fabrication of the triode structure to include a silicon wafer as the gate-cathode and a quartz wafer to be used as the anode. Finally the equipment and procedure for CNT growth were discussed.

IV. Results

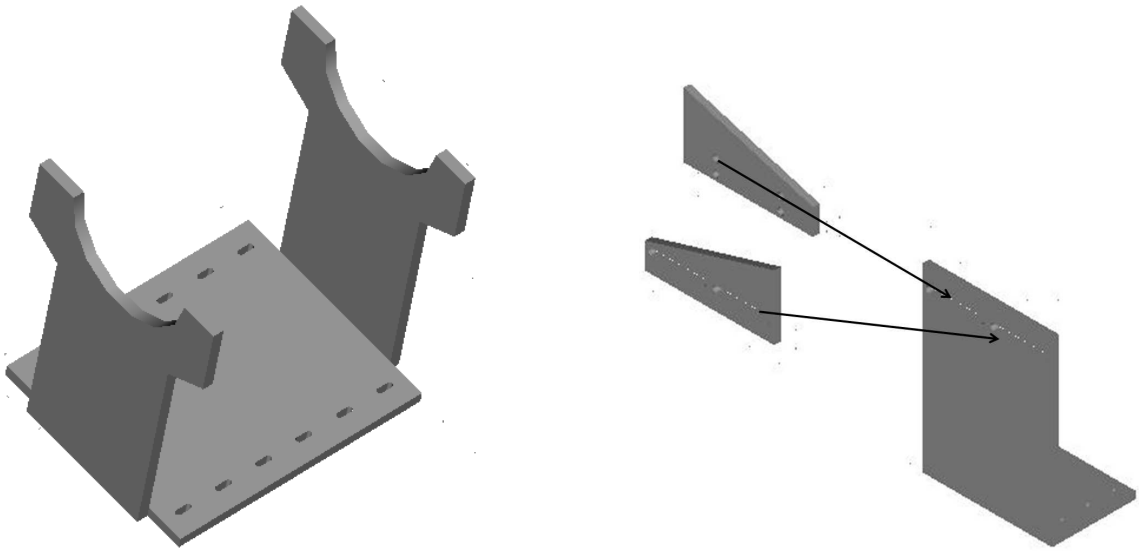
This chapter describes the results obtained from the fabrication and design of a vacuum chamber for field emission testing, the fabrication of a triode structure for CNT growth, the pretreatment of nickel for the growth of CNTs and finally the growth of CNTs with and without patterning.

4.1 Field Emission Testing

4.1.1 Vacuum Chamber. The 12" diameter sphere bought from Kurt J. Lesker has four 8" flanges, two 6" flanges, one $4\frac{1}{2}$" flange, and four $2\frac{3}{4}$" flanges. All flanges where secured following the specifications from the manufacturer:

- 8", 6", $4\frac{1}{2}$" CF flange bolts are tighten to 15 ft.-lbs.
- $2\frac{3}{4}$" CF flange bolts are tighten to 12 ft.-lbs.

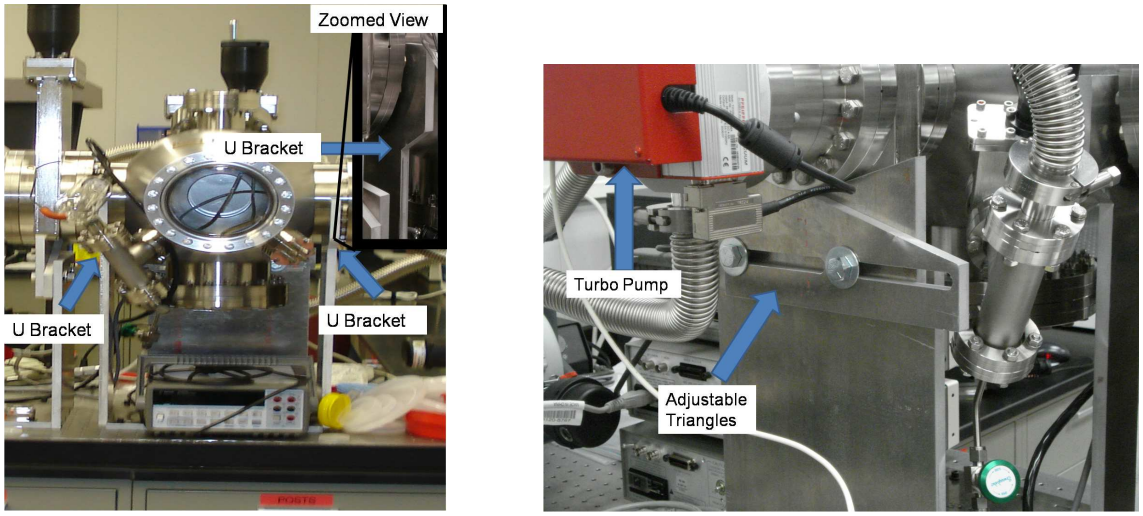
To attach the turbo molecular pump, ion gauge, and convection gauge to the load lock, the main chamber needed to be elevated by 15 inches. The brackets seen in Figure 4.1 were fabricated to elevate and stabilize the chamber. The elevation brackets were fabricated out of $\frac{1}{2}$" aluminum and was designed to let two of the 8 inch ports rest over the u-shaped posts. Figure 4.2(a) shows the chamber once it is elevated and the inset picture demonstrates how the chamber rests on the U shaped brackets. The base plate was fabricated with 0.75 inch diameter holes spaced 2 inches apart to be able to be attached to an optical table. Once the chamber was elevated, the stabilization brackets are used to stabilize the load lock that is attached to one of the 8" ports on the main chamber and the turbo pump that is attached to the main chamber. The stabilization brackets were designed to be adjustable from $14\frac{1}{2}$" up to $15\frac{1}{2}$" with the use of two triangles as seen in Figure 4.2(b). Once the chamber was elevated, nitrogen lines where run into the venting valves to return the chamber back to atmosphere from high vacuum conditions. The chamber was pumped down and achieved a final pressure of 10^{-8} torr.



(a) (b)

Figure 4.1: Chamber fabricated for elevation and stabilization (a) Elevation Bracket. (b) Stabilization Bracket.

4.1.2 Electrical Connections. To be able to power up the triode device, three electrical signals are needed:



(a) (b)

Figure 4.2: Chamber elevated on U and L brackets. (a) Shows chamber elevated on U brackets. The inset picture shows how the chamber rests on the U brackets. (b) L brackets with adjustable brackets.

- The cathode, substrate in this case, needs to receive a ground signal.
- The gate needs to have a high enough voltage to extract the electrons from the CNT tips for field emission.
- The anode needs to be set at a higher potential than the gate to be able to accelerate the electrons and be able to measure current to calculate the CNTs field emission.

The vacuum chamber built was designed to accept eight electrical connections through miniature high voltage plugs. Connectors rated for high vacuum conditions will be used to connect the outside equipment to the sample puck receiver combination illustrated in Figure 4.3 available from MDC vacuum products. The sample puck is configured to have a heating dish that will take two of the available seven connections or it can be rewired to have seven electrical connections and no heater.

The triode structure fabricated is under 1 cm $\times$ 1 cm so that it is able to fit in a ceramic package with a 1 cm $\times$ 1 cm cavity. The package is a dual inline configuration and contains up to 28 pins for outside connections. A wafer shown in Figure 4.4 was fabricated to attach the ceramic package that contains the triode structure to the sample puck. Field emission testing needs to be done in a vacuum so a normal printed circuit boards can not be used, instead a sapphire wafer was used. The connection lines where achieved by evaporating gold 5000 $\mathring{A}$ thick onto the wafer,

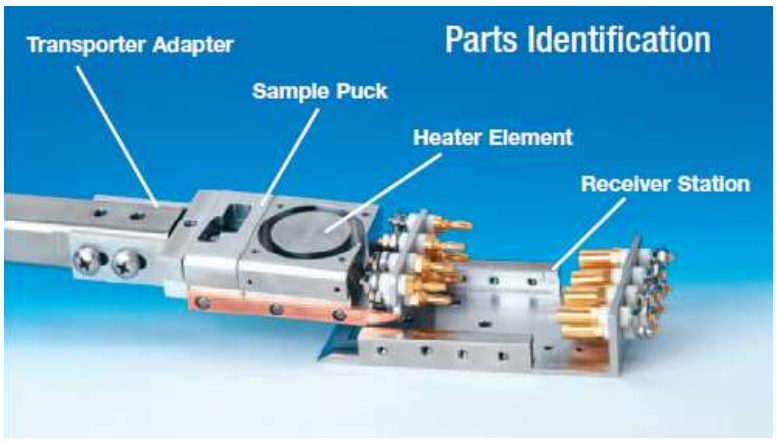


Figure 4.3: MDC Transferable Test Station.

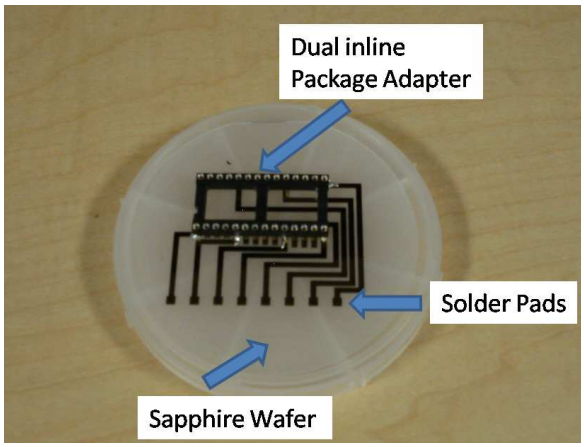


Figure 4.4: PCB board and dual inline package adapter .

followed by patterning, and finally etching off the excess gold with the gold etchant TFA. To be able to quickly connect and disconnect ceramic packages, a dual inline to surface mount adapter was used. By using the adapter, we do not have to solder a new package every time we want to test a new structure. The surface mount adapter was then soldered onto the sapphire wafer using indium solder, a solder that will not outgas in vacuum applications.

4.2 Triode Structure Fabrication

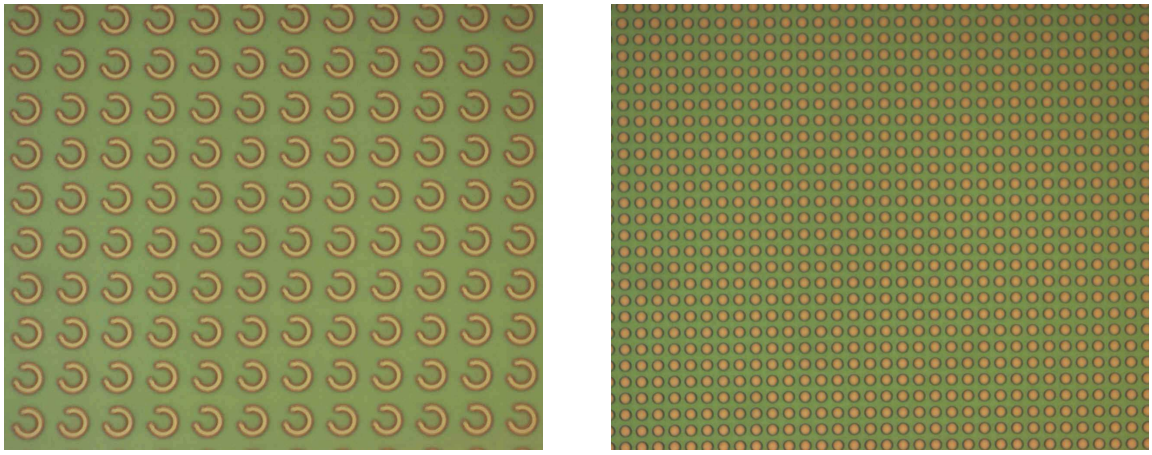
4.2.1 Anode Fabrication. To fabricate the anode structure, inductively coupled plasma reactive ion etching is used to get 50 μm and straight sidewalls. To be able to use ICP-RIE, a combination of photoresist and a nickel mask, 3000 $\mathring{A}$ thick, is needed to protect the underlaying structure. The first wafer etched used only a reactive ion etching (RIE) process and reached 10 μm. To be able to attain the desired 50 μm, an RIE system combined with an inductively coupled plasma source that will allow a faster etch rate of the material without destroying the mask material needed to be used but at the time the anode was fabricated the ICP-RIE system was not operational. The wafer is then diced and followed by an evaporation of Ti 200 $\mathring{A}$ thick to act as an adhesion layer, and a gold layer 5000 $\mathring{A}$ thick to be used for bonding. Evaporation is used to limit the amount of gold deposited on the sidewalls. Excess gold on the sidewall of the anode structure would cause some of the electrons to be

diverted to the sides and increase the chance of the gate and anode shorting and will increase the gate current leakage.

4.2.2 Cathode and Gate Fabrication. To fabricate the gate-cathode combination, a silicon wafer had the following layers added to it:

- A 200 $\mathring{A}$ Ti layer was sputtered for adhesion and to act as a diffusion barrier between the silicon wafer and the Ni layer.
- A 100 $\mathring{A}$ Ni layer was sputtered to act as the catalyst for CNT growth. The CNTs will act as the cathode of the device.
- A 2 μm SiO_2 layer is deposited by PECVD to act as a dielectric between the gate and cathode.
- A 2500 $\mathring{A}$ Cr layer is used as the gate of the device.

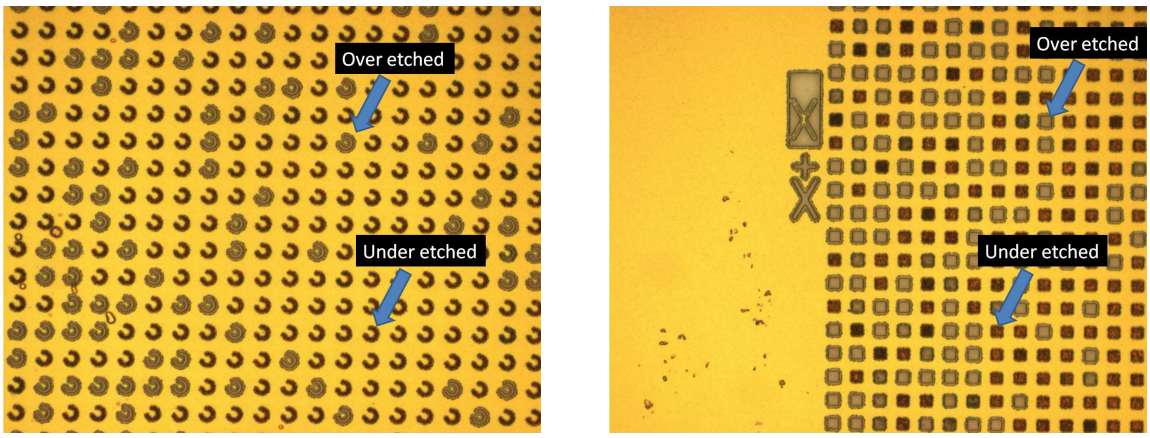
To be able to achieve good definition for the small size features on the gate arrays, we used 1805 photoresist with a thickness of approximately 0.5 μm. As seen in Figure 4.5 good sidewall definition and clear features where achieved using the process described in Appendix D. Originally a layer of gold between 2500 $\mathring{A}$ and 5000 $\mathring{A}$ thick was going to be deposited after our Cr layer and later etched to create a good surface for bond pads. An etch study was done to determine the effects of TFA, a gold etchant sold by Transene company on the small dimension to be used for the array in our cathode gate structure. As seen on Figure 4.6(a) and (b), the gold etchant did not etch at a constant rate, causing the final result to be either over etched or under etched. The sidewall definition needs to be maintained since the metal layer will act as a mask during the RIE and buffered oxide etch of the silicon dioxide. In comparison, the chrome etchant, CR-4 sold by CYANTEK company created constant etch rates and excellent sidewall definition as seen in Figure 4.7. It was decided to add a gold layer after the array has been created and then etch off all the gold but the gold over the wire bonding pads and flip chip bonding pads. A separate mask was designed for the gold layer and it is shown in Chapter V.



(a) (b)

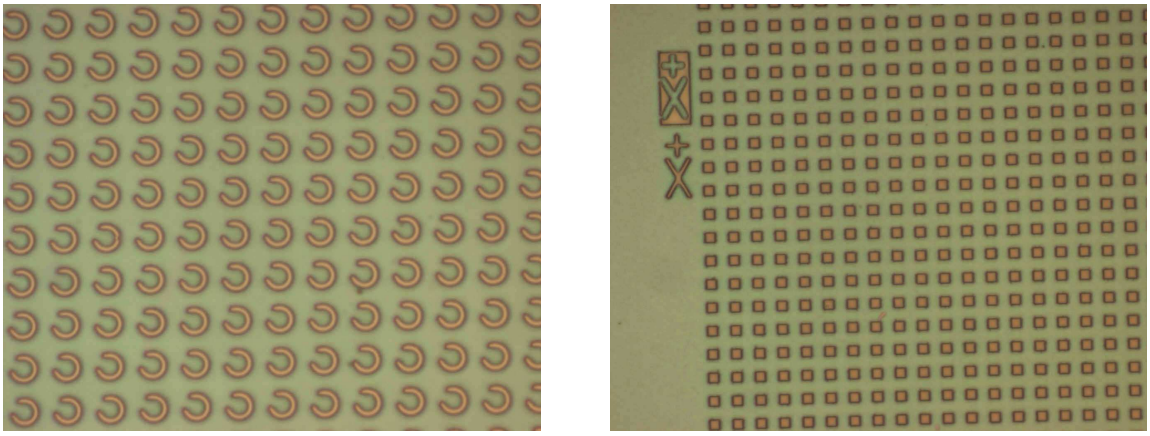
Figure 4.5: Array mask transferred onto the substrate using 1805 photoresist exposed for 3 seconds and developed for 30 seconds. (a) Torroid array. (b) Square array.

To be able to get CNTs to grow in this structure the catalyst layer needs to be exposed. After the chrome is etched, the SiO_2 layer was dry etched with a gas combination of CF_4 at 40 sccm and O_2 at 3 sccm for 40 minutes. After this process, it appeared that the top of the nickel surface still had some left over SiO_2 and was also contaminated with an unknown substance. The next step was to etch some of



(a) (b)

Figure 4.6: Gold layer 2500 $\mathring{A}$ wet etched for 36 seconds. Wet etchant did not provide a constant etch rate.



(a) (b)

Figure 4.7: Chrome layer 2500 $\mathring{A}$ wet etched for 153 seconds. Wet etchant provided a constant etch rate.

the SiO_2 sidewalls using a buffered oxide etchant to reduce the chances of having the cathode and gate short. After this step, the unknown substance on top of the nickel was still present keeping the buffered oxide from etching any of the left over SiO_2 on the top of the nickel. Several methods to include ashing, BOE, HF, CR-4 and using 1165 a lift off resist stripper were tried to remove the unknown black substance with no success.

4.3 CNT Growth

To achieve CNT growth using a catalyst, it is first necessary to pretreat the catalyst, a process that granulates the catalyst into nano size islands, followed by a growth process that adds a hydrocarbon gas, methane in our case.

The pretreatment of the catalyst is accomplished at a lower temperature and microwave power than the one needed for CNT growth. The pretreatment helps in the creation of isolated nanoislands that promote CNT growth [26]. It has also been discovered that the diameter of the Ni particles correspond to the diameter of the CNTs being grown [26]. The time needed to create the right size catalyst without affecting the density of the catalyst particle is dependant on the thickness of the catalyst being used. Wafers with 200 $\mathring{A}$ of Ti and Ni thickness and deposition methods

shown in Table 4.1 were subjected to H_2 pretreatment to try to determined what is the best pretreatment time for the formation of CNTs. The times for the pretreatment where set to 3.5, 5 and 7 minutes. During one of the 3.5 minute pretreatment cycles the MPECVD systems RF detector went out causing the reflective power not to be measured. Due to this, the plasma took longer to strike, leaving the sample with flowing H_2 and at a substrate temperature of 400° C for an extra 3 minutes, extending the pretreatment to 6.5 minutes. The process used to get these measurement is as follows:

- MPECVD chamber is pumped down to 10 torr.
- H_2 is flowed into the chamber at 135 sccm.
- Temperature is set to 400° C.
- Plasma is ignited. Once the plasma is ignited the time starts. The plasma usually starts around 300 W and it takes 10 seconds to reach 400 W. The pressure is moved to 20 torr during the pretreatment and growth.
- The timer stops once the microwave power is turned off.
- The granule sizes were approximated using Scanning Electron Microscope (SEM) images from three different locations on the wafer.

From Table 4.1, we can see that when the nickel thickness increases, so does the size of the granules. It is also shown that evaporated films tend to have smaller granule sizes than sputtered samples. This is due to the fact that evaporated particles have less kinetic energy than sputtered particles [29] and are easier to break up during the pretreatment process. The evaporated 50 $\mathring{A}$ 3+3.5 minute sample flipped upside down during the pumping down of the MPECVD chamber so it did not get any form of pretreatment so all the nickel was still present. The evaporated 100 $\mathring{A}$ 3+3.5 minute sample had no nickel left on it. Since it was actually pre-treated for about 6.5 minutes, it matches closely to our 7 minute case where all the nickel granules are not visible.All other granule sizes on the 6.5 minute samples are close to the 7 minute case.

Table 4.1: Granule sizes of different nickel thicknesses and deposition methods treated for different times.

Treatment Time	Evaporated or Sputtered	Nickel Thickness ($\AA$)	Granule Size (nm)	Notes
3.5 Minutes	Evaporated	50	30	N/A
	Evaporated	100	45	N/A
	Evaporated	200	75	N/A
	Sputtered	50	35	N/A
	Sputtered	100	50	N/A
	Sputtered	200	80	N/A
5 Minutes	Evaporated	50	20	N/A
	Evaporated	100	45	N/A
	Evaporated	200	100	N/A
	Sputtered	50	25	N/A
	Sputtered	100	58	N/A
	Sputtered	200	180	N/A
3 Minutes + 3.5 Minutes with out plasma	Evaporated	50	0	Upside Down
	Evaporated	100	0	N/A
	Evaporated	200	35	N/A
	Sputtered	50	25	N/A
	Sputtered	100	35	N/A
	Sputtered	200	50	N/A
7 Minutes	Evaporated	50	0	No Ni
	Evaporated	100	0	No Ni
	Evaporated	200	40	N/A
	Sputtered	50	40	N/A
	Sputtered	100	50	N/A
	Sputtered	200	60	N/A

If the nickel catalyst is pretreated for to much time the nickel nano size islands will begin to conglomerate creating islands with larger areas not suitable for CNT growth. This is a reason why the pretreatment time is a crucial step in the CNT growth process.

Figure 4.8 shows an example of one of the pictures taken by the SEM to determined the size of the nickel catalyst after pretreatment. Three different areas of the wafer where examined and an average size for the catalyst was determined. Apart from the size of the catalyst, another important consideration to take is the density of the nickel catalyst left on the wafer. The density will become an important factor during the growth of vertically aligned CNTs.

Figures 4.9, 4.10,and 4.11 illustrate SEM images of the effects of a five minute pretreatment on different thickness of nickel catalyst. As the thickness of the nickel catalyst layer increases, the diameter of the nickel particles also increase. It is also seen that the evaporated samples have smaller diameter particles compared to the sputtered samples. To get a good vertical carpet of CNTs, it is necessary to have a high density of nickel particles attaining high Van der Waals forces.

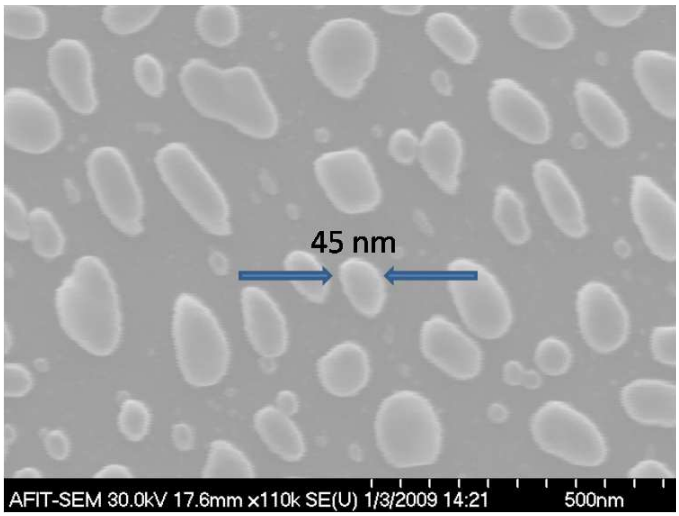
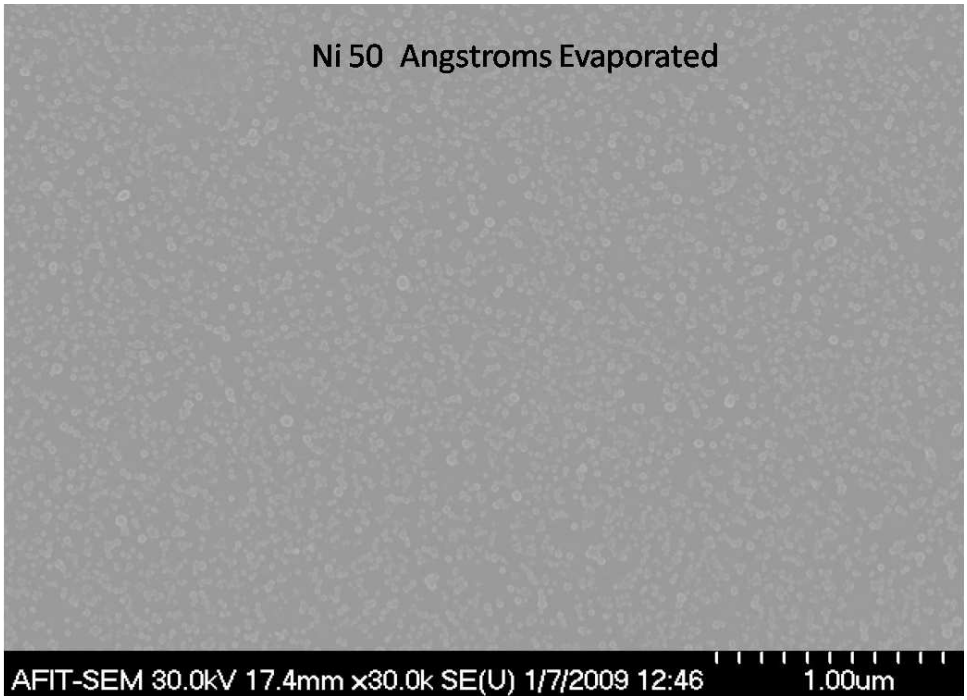
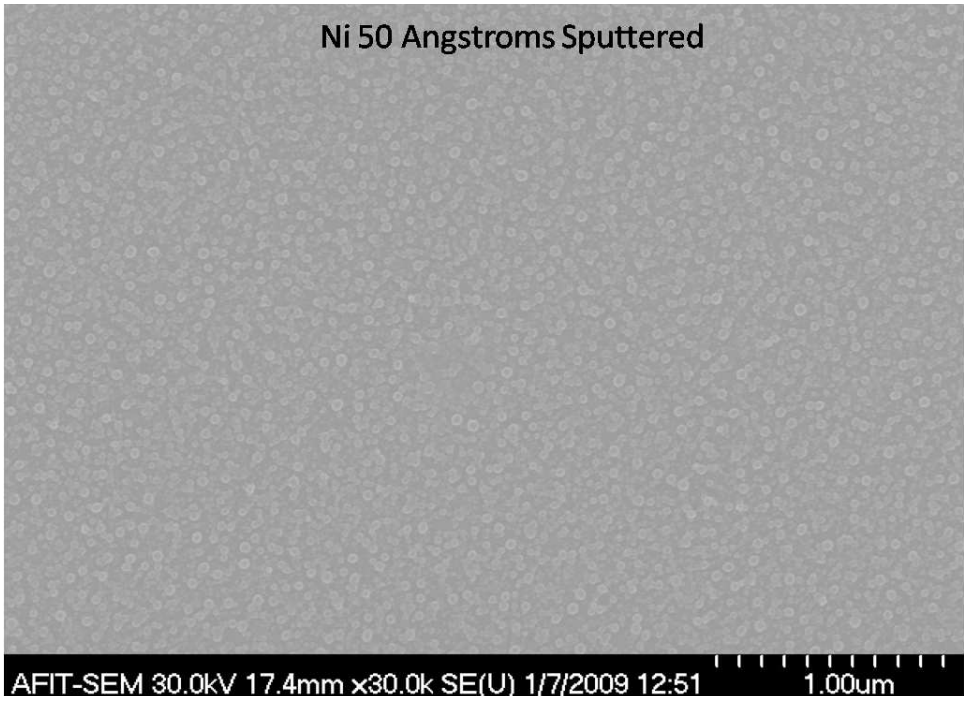


Figure 4.8: Evaporated Ni 100 $\mathring{A}$ thick pre-treated for 5 minutes.

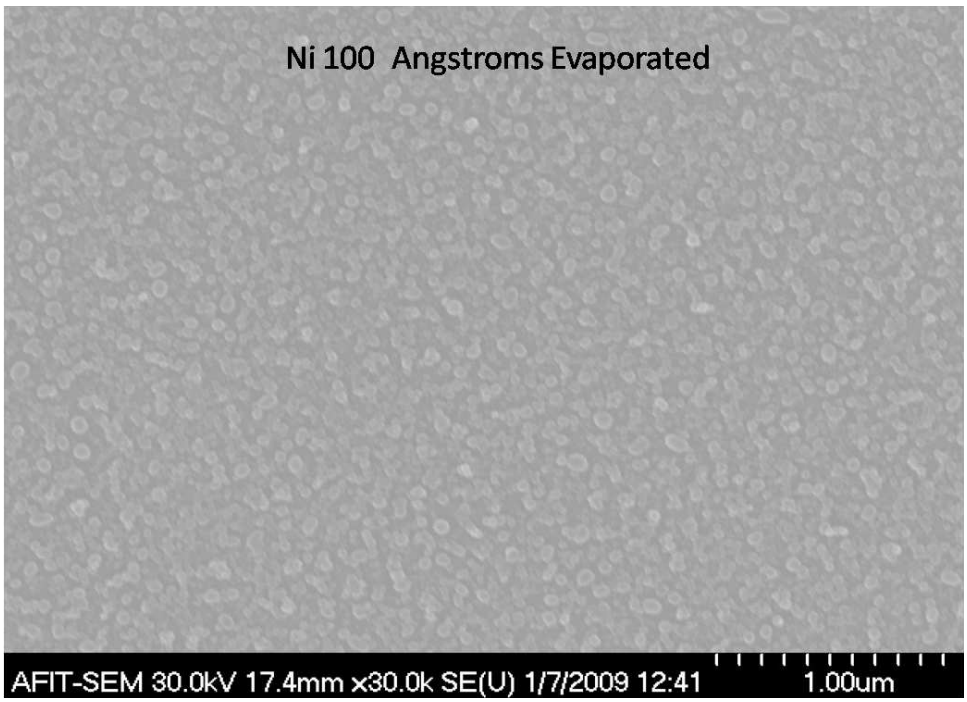


(a)

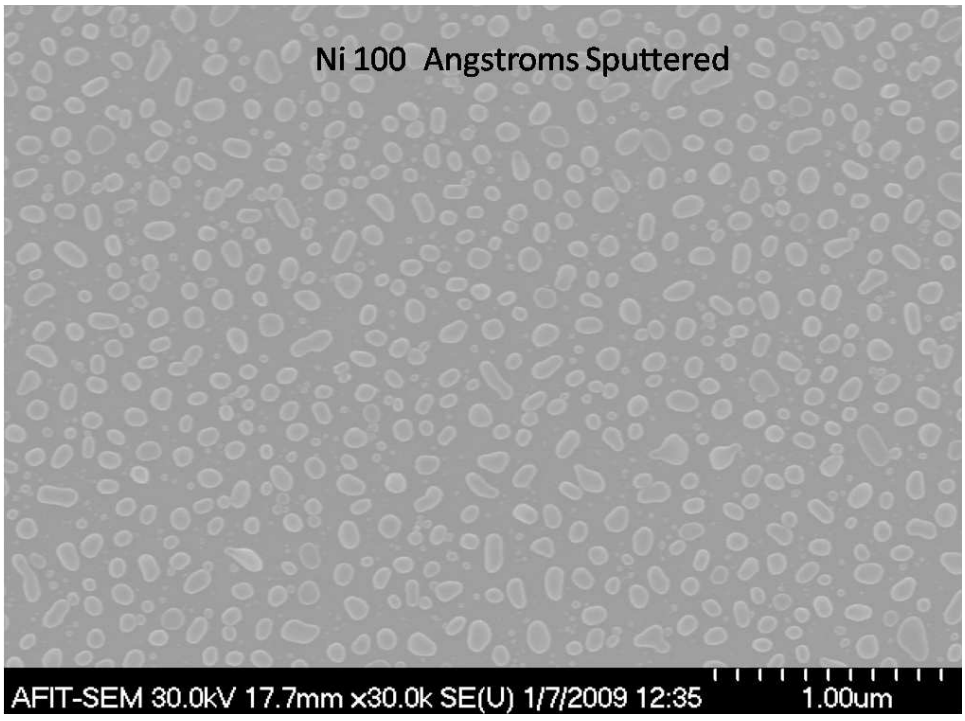


(b)

Figure 4.9: 5 Minute Pretreatment of 50 $\mathring{A}$ of Nickel. Small diameter granules are present. (a) Evaporated nickel. (b) Sputtered nickel.

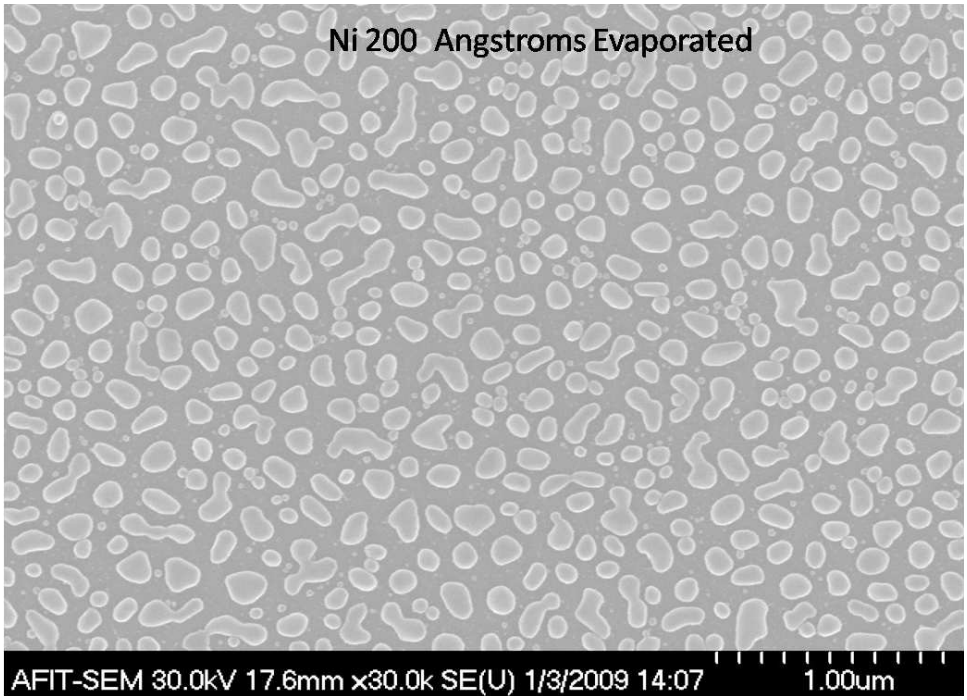


(a)

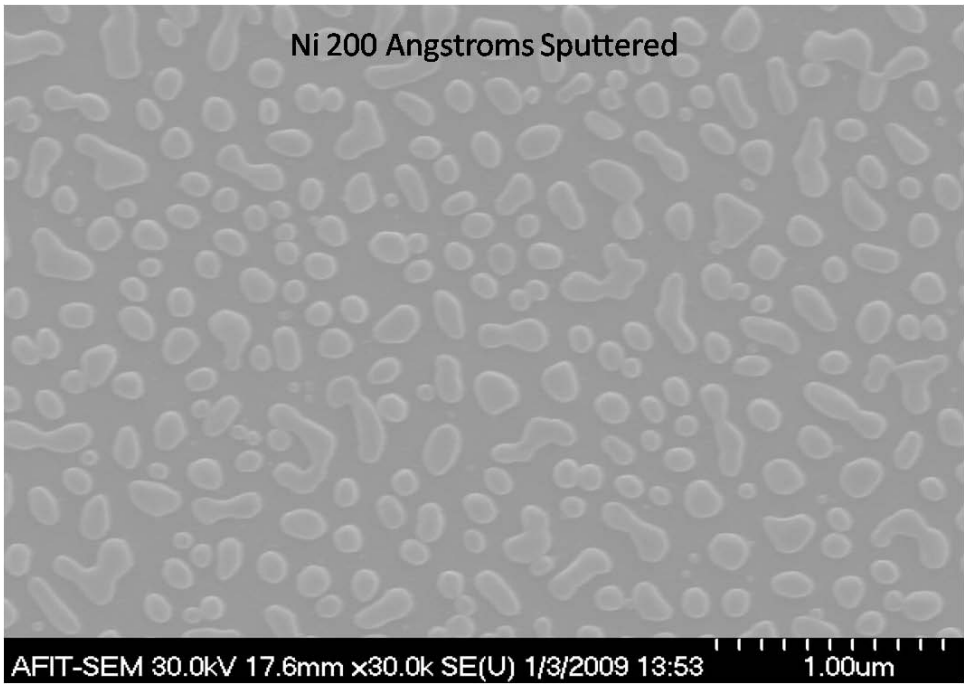


(b)

Figure 4.10: 5 Minute Pretreatment of 100 $\AA$ of Nickel. Sputtered nickel shows good granule size and good formation of nano islands. (a) Evaporated nickel. (b) Sputtered nickel.



(a)



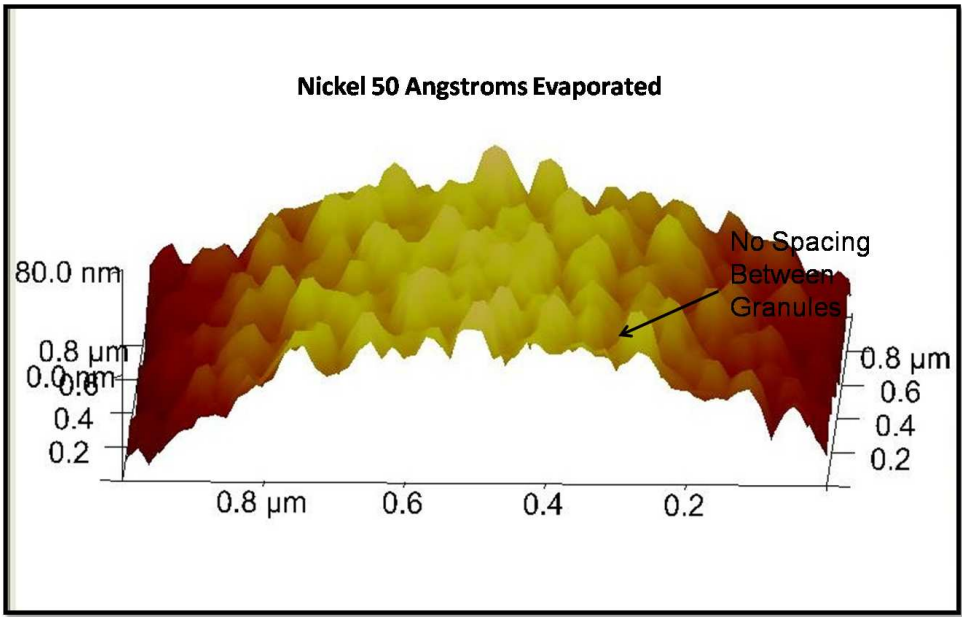
(b)

Figure 4.11: 5 Minute Pretreatment of 200 $\AA$ of Nickel. Sputtered sample shows cleaner breaks between nickel islands. (a) Evaporated nickel. (b) Sputtered nickel.

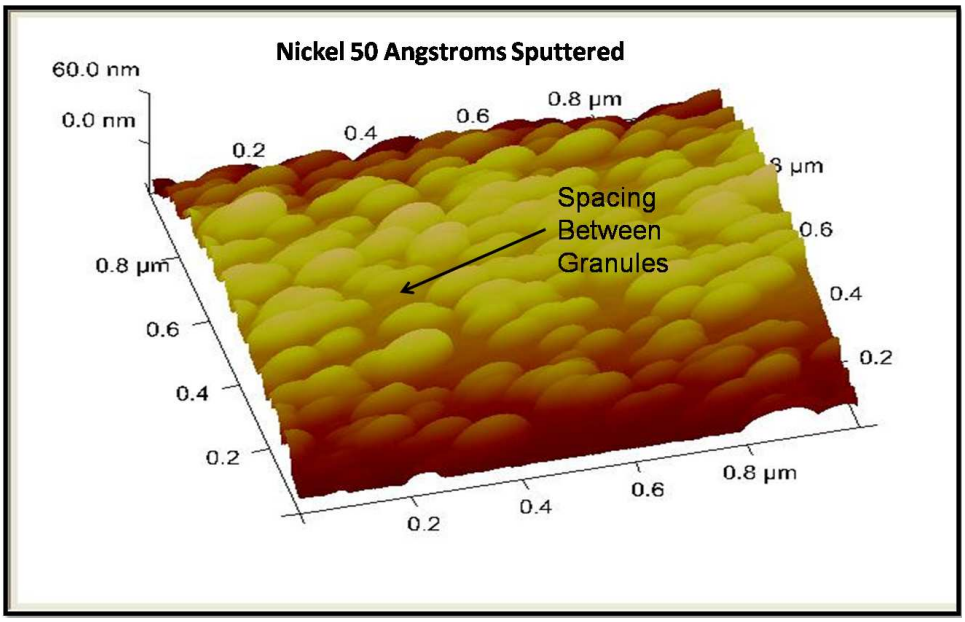
From Figure 4.9, we can see that the 50 $\mathring{A}$ nickel catalyst was granulated into small diameter nickel granules. Figure 4.10(b) shows a good density of catalyst and nickel catalyst size. Figures 4.11 (a) and (b) shows bigger diameter catalyst that will not function as well for CNT growth as demonstrated later in this section. The same six samples of Figures 4.9, 4.10, and 4.11 where subjected to an AFM measurements to determine the size of the catalyst. Tapping mode is used for the AFM measurements since it does not destroy the surface being tested and preserves the AFM tips for multiple uses in comparison to full contact mode. Two imaging modes are used to image the surfaces.

- Height Mode: The oscillation amplitude of the cantilever that contains the AFM tip is measured by the use of a laser and a diode detector. This type of measurement gives us the height of the catalyst granules under test. One of the disadvantages of this method is when there exists large height differences, the smaller structures are not recorded.
- Phase Mode: During phase mode, both the amplitude of the cantilever through the laser measurement and the drive signal from the piezoelectric driver are compared. The phase lag between both signals is used to determined the topographical aspects of the surface under test making it an extremely precise measurement. Advantages of this measurement is that it gives us finer features between grain boundaries on our granulated catalyst and it is not affected by height differences.

Height mode measurements can be seen in Figures 4.12, 4.13, and 4.14.

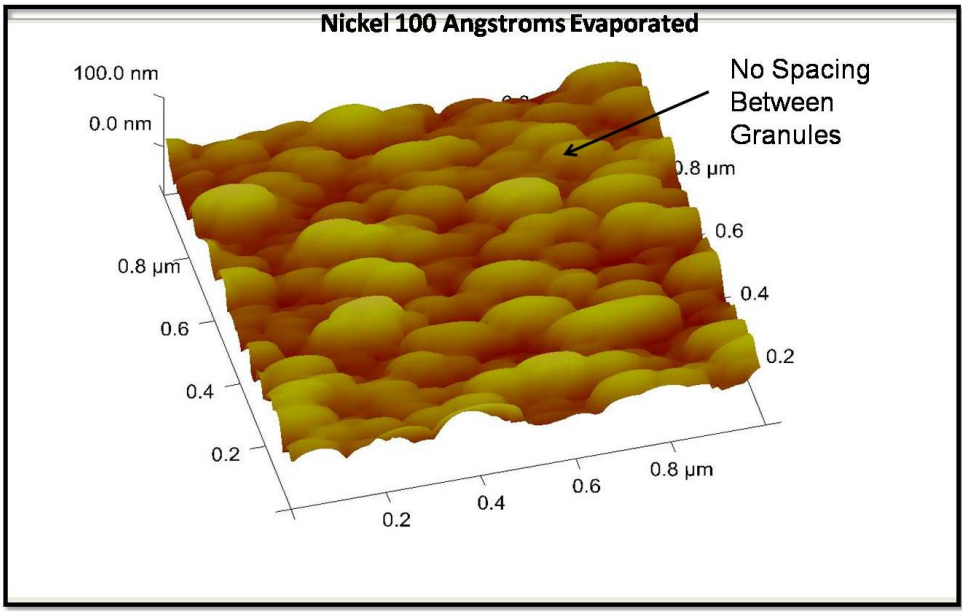


(a)

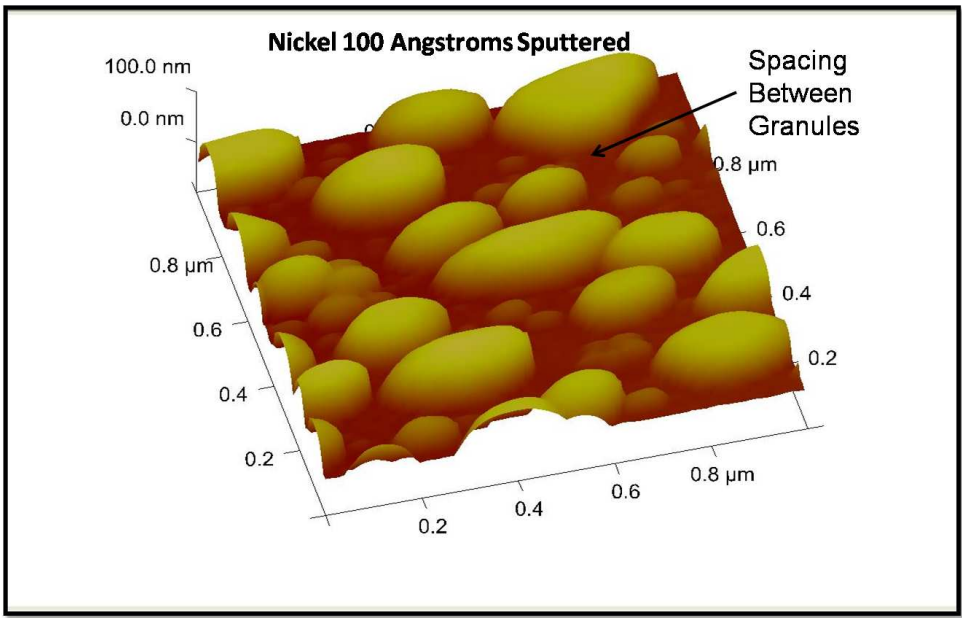


(b)

Figure 4.12: AFM Height Measurement 5 Minute Pretreatment of Nickel. (a) Evaporated Ni 50 $\mathring{A}$ thick. (b) Sputtered Ni 50 $\mathring{A}$ thick.

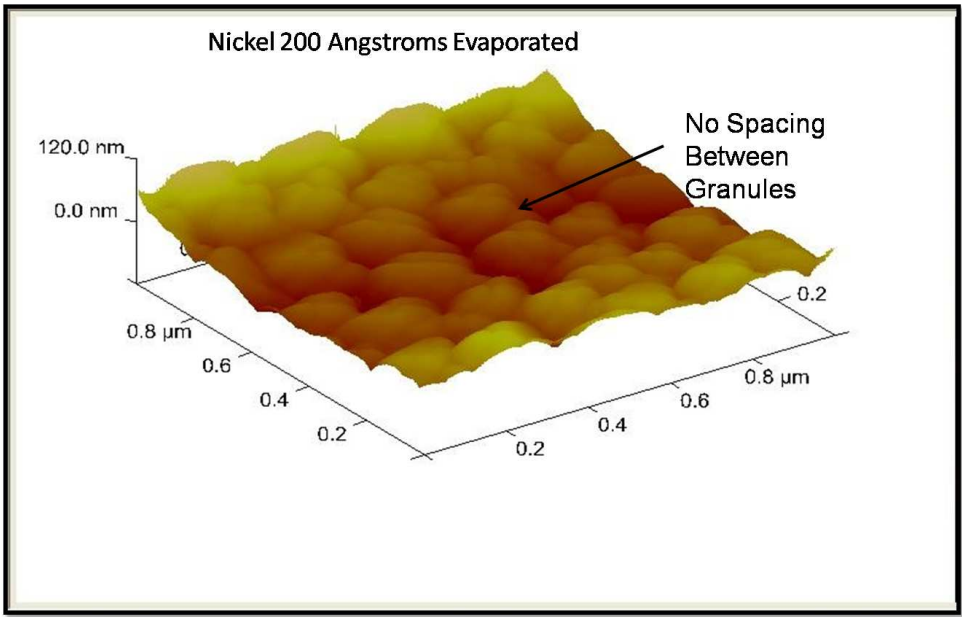


(a)

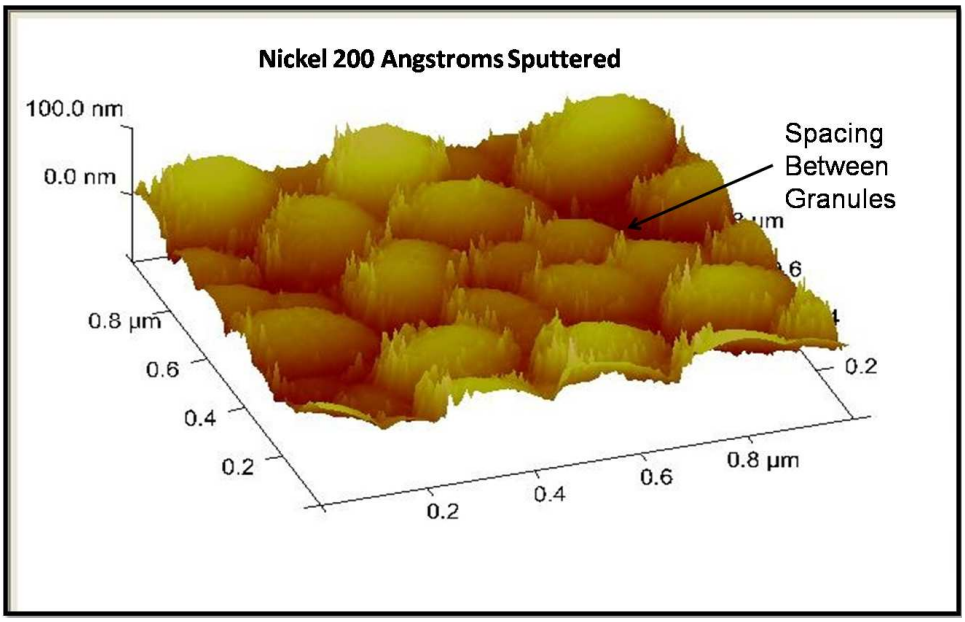


(b)

Figure 4.13: AFM Height Measurement 5 Minute Pretreatment of Nickel. (a) Evaporated Ni 100 $\mathring{A}$. (b) Sputtered Ni 100 $\mathring{A}$ thick.



(a)



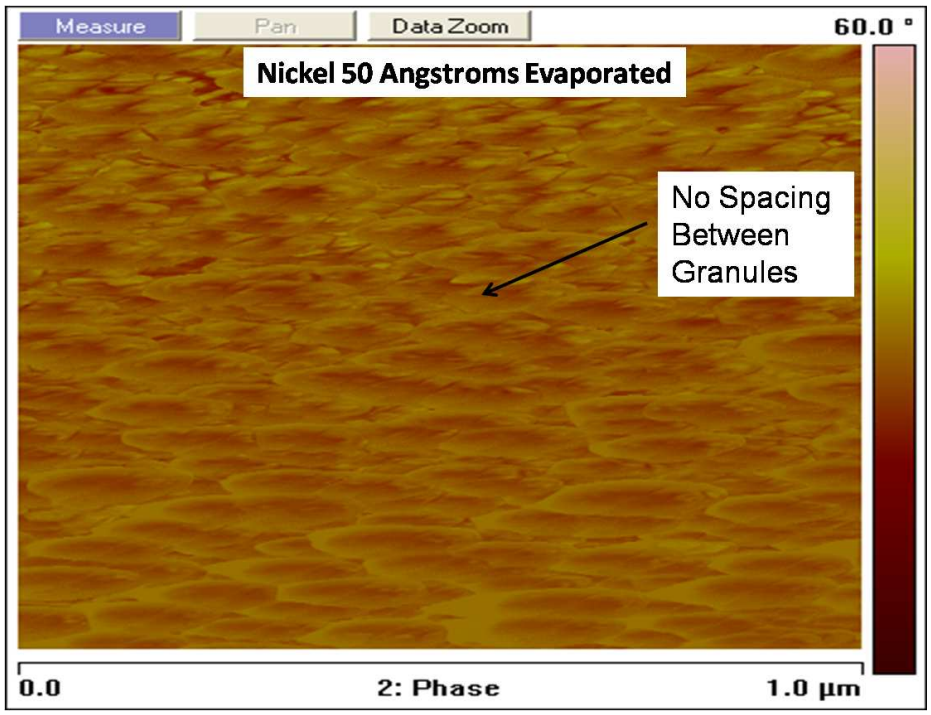
(b)

Figure 4.14: AFM Height Measurement 5 Minute Pretreatment of Nickel. (a) Evaporated Ni 200 $\mathring{A}$ thick. (b) Sputtered Ni 200 $\mathring{A}$ thick.

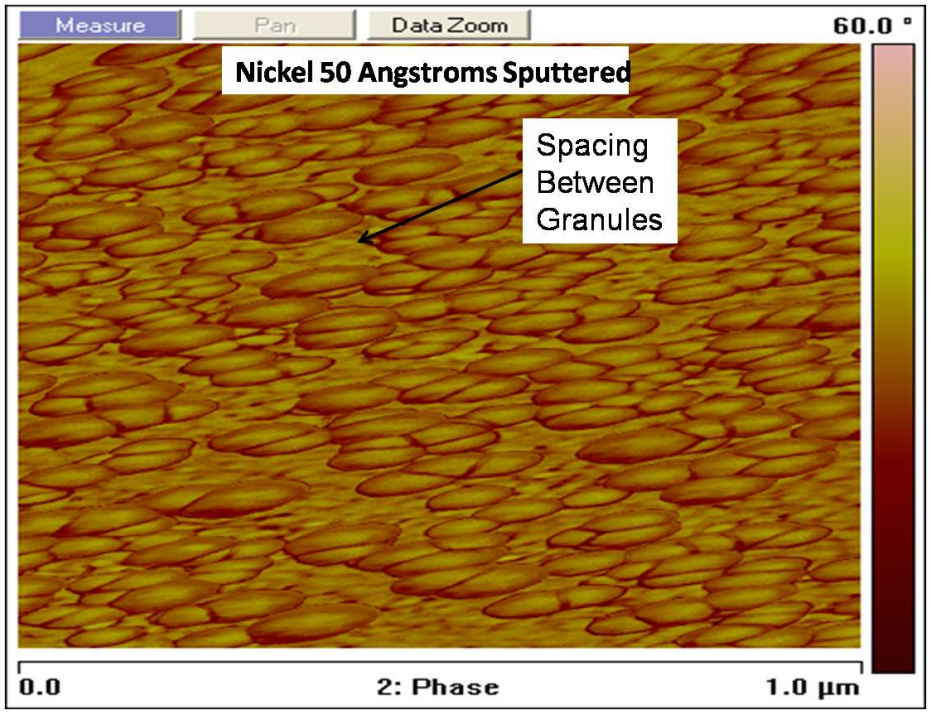
From the AFM height measurements, we get a fast measurement of the height and size of the granulated nickel particles. Both of the 50 $\mathring{A}$ samples shown in Figures 4.12(a) and 4.12(b) can be seen to have small size diameter granules and to have a heavy density of granules compared to the 100 $\mathring{A}$ sputtered sample in Figure 4.13(b). For CNT growth, we need the nickel to form nickel islands and from Figures 4.13 (a) and 4.14(a) we can tell that the 100 $\mathring{A}$ and 200 $\mathring{A}$ evaporated samples seem to have no spacing between their granules. CNT growth will not happen as easily and with the same density on the evaporated samples compared to the sputtered samples.

To be able to tell the exact boundary of the granulated particles, a phase measurement was taken of the same six samples and it is shown in Figures 4.15, 4.16, and 4.17. The 50 $\mathring{A}$ evaporated sample in Figure 4.15(a) creates granules of the right size but they are still attached to each other creating a problem for CNT growth. The 50 $\mathring{A}$ sputtered sample in Figure 4.15(b) show granulation of the catalyst and the formation of separate nickel islands. The phase measurement shows us that for both the 100 $\mathring{A}$ and 200 $\mathring{A}$ evaporated films in Figures 4.16(a) and 4.17(a) the granules are in tight approximation with each other and not really forming nickel islands. The 100 $\mathring{A}$ sputtered film in Figure 4.16(b) shows distinct nickel islands of different diameters. Any extra pretreatment to this sample would just break up the islands into smaller islands creating better conditions for CNT growth. The 200 $\mathring{A}$ sputtered film in Figure 4.17(b) shows that this sample still needs more pretreatment time to be able to create smaller islands for CNT growth.

After the granulation of the catalyst has been accomplished the MPECVD systems is adjusted to promote the growth of CNTs. Van der Waals forces between CNTs combined with the microwave power from the MPECVD system creates an optimum environment for vertical CNT growth. When changing from a pretreatment mode to a growth mode, the H_2 flow is reduced to 120 sccm from 135 sccm followed by an increase of substrate temperature to 650° C, microwave power of 1000 watts and CH_4 flow of 15 sccm.

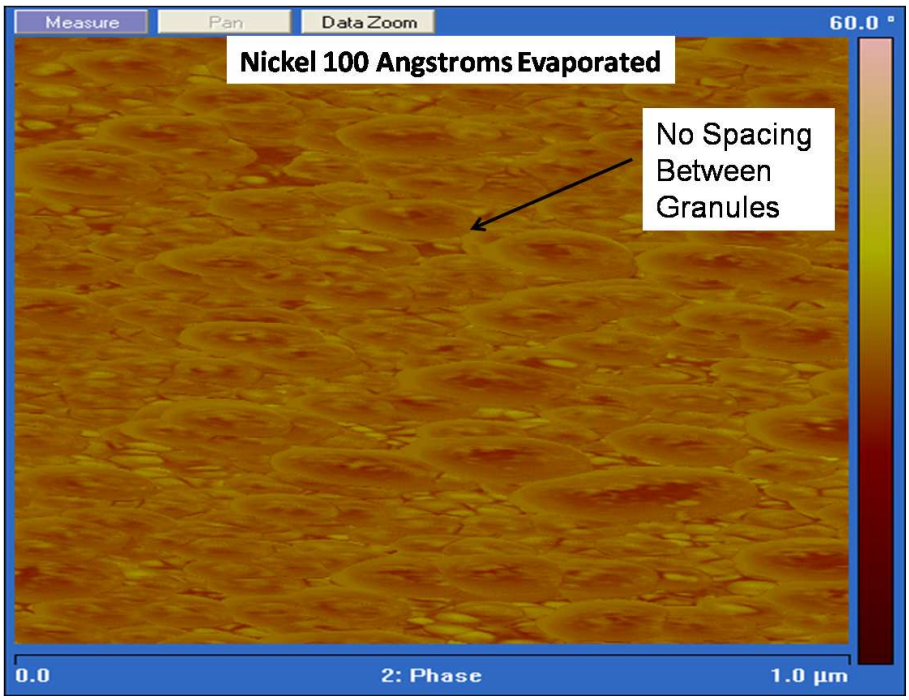


(a)

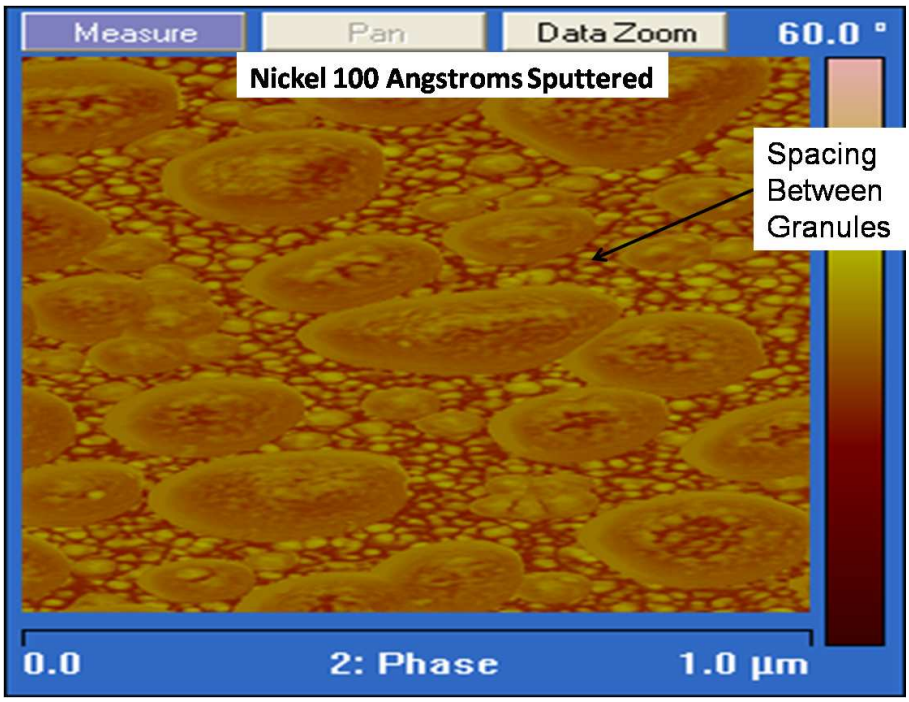


(b)

Figure 4.15: AFM Phase Measurement 5 Minute Pretreatment of Nickel (a) Evaporated Ni 50 $\mathring{A}$ has good granule size but no good separation between granules. (b) Sputtered Ni 50 $\mathring{A}$ is starting to separate and form nano islands.

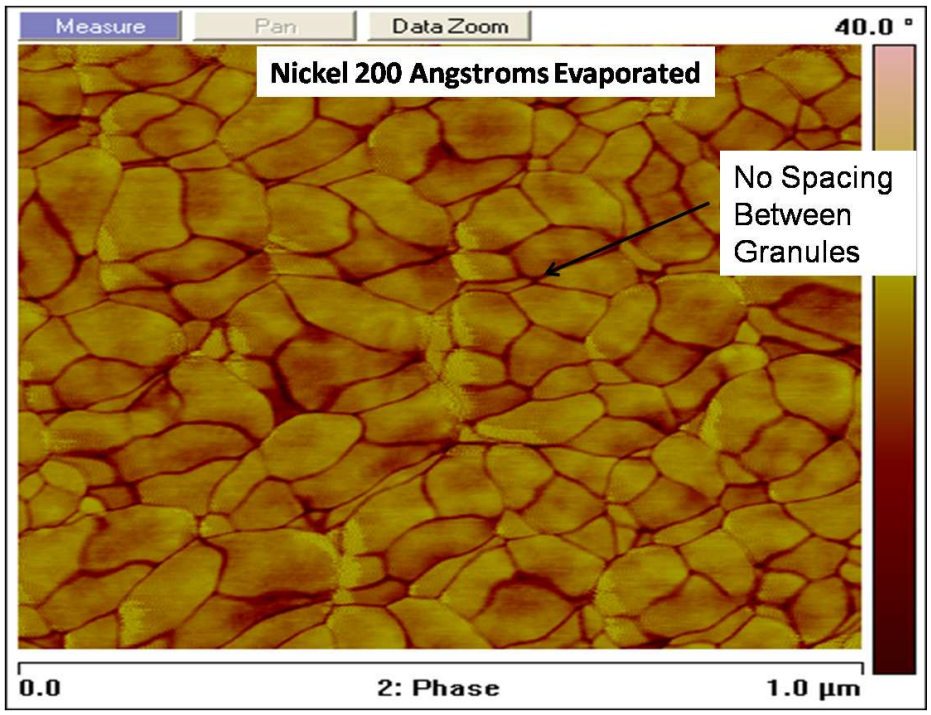


(a)

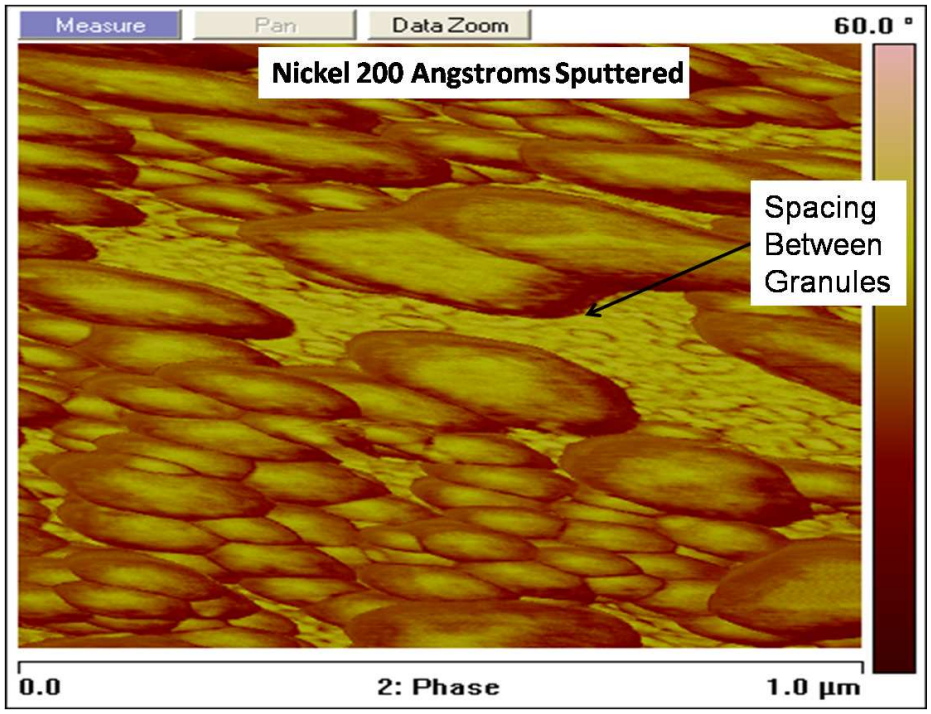


(b)

Figure 4.16: AFM Phase Measurement 5 Minute Pretreatment of Nickel. (a) Evaporated Ni 100 $\mathring{A}$. There is no separation between granules. (b) Sputtered Ni 100 $\mathring{A}$. Good granule size and separation.



(a)



(b)

Figure 4.17: AFM Phase Measurement 5 Minute Pretreatment of Nickel. (a) Evaporated Ni 200 $\mathring{A}$. There is no separation between granules. (b) Sputtered Ni 200 $\mathring{A}$. Needs more pretreatment to create smaller granule islands.

The time it takes to change from pretreatment to growth is normally from one minute to 1.5 minutes. By keeping the MPECVD system at this level for two minutes, we got a CNT growth of approximately 1.5 μm measured using AFITs AFM and shown in Figure 4.18.

During the time that the systems substrate temperature and microwave power for the system is being brought up to CNT growth parameters, the nickel catalyst is still being pretreated. The samples seen in Figure 4.19 were subjected to a 5 minute pretreatment followed by a 2 minute growth. The exact time line is as follows:

- At 35 seconds the plasma ignited.
- From 35 seconds to 5 minutes and 35 seconds the pretreatment took place.
- From 5 minutes and 35 seconds to 6 minutes and 53 seconds, the substrate temperature and microwave power were increased to get CNT growth.

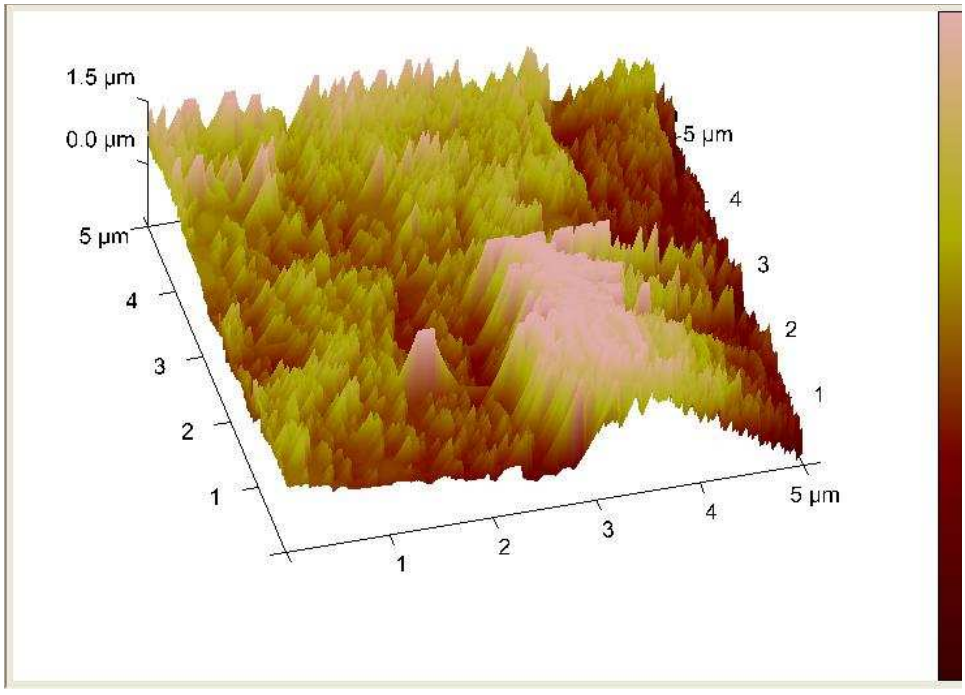
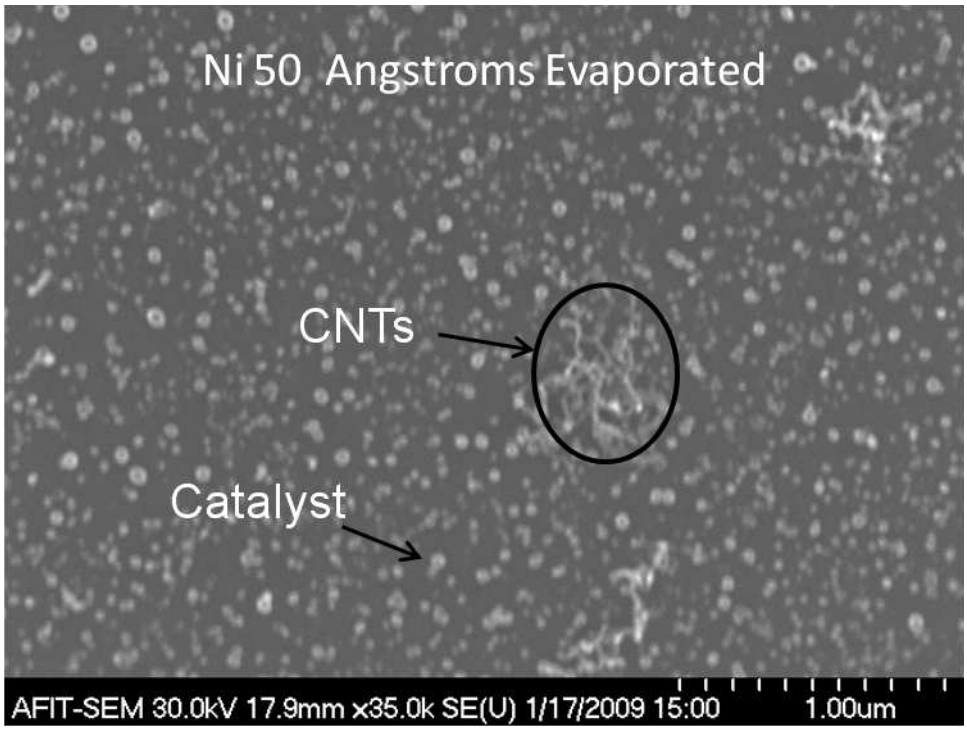


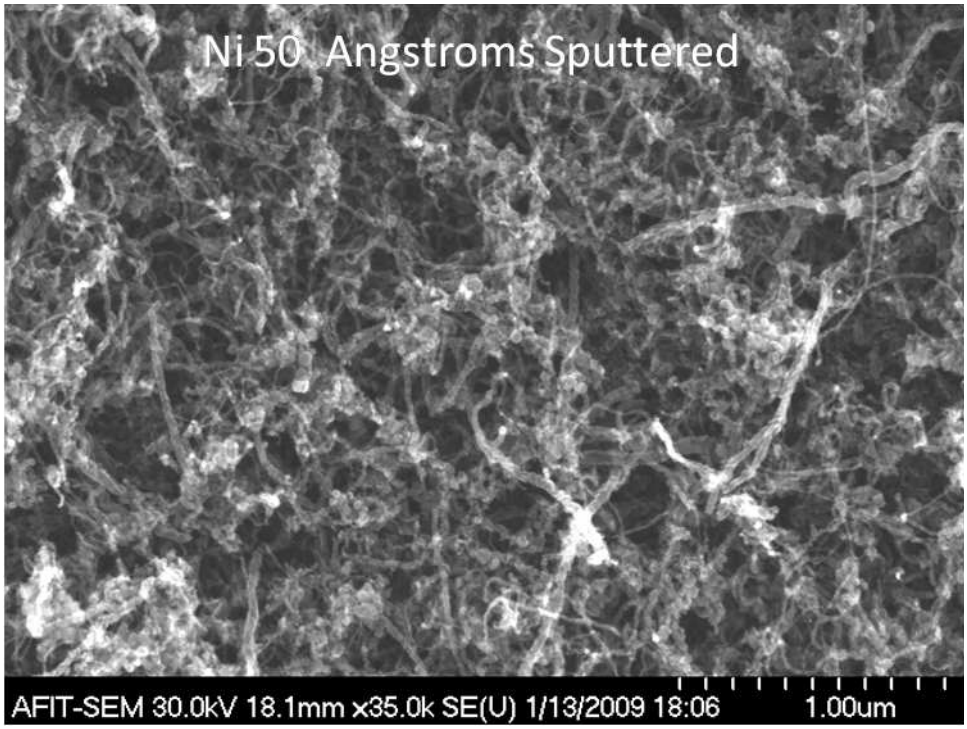
Figure 4.18: AFM height measurement of CNTs from sputtered Ni 100 $\mathring{A}$ thick pre-treated for 5 minutes and grown for 2 minutes.

- Growth took place from 6 minutes and 53 seconds to 8 minutes and 53 seconds giving us 2 minutes of growth time.

From the time line above, we can see that the samples were pretreated for an extra minute and 18 seconds. During this time the granule size continued to decrease or if it reached a minimum size it started to conglomerate into larger nickel granules. From Figures 4.19, 4.20, and 4.21 we can see how CNT growth was minimal on the evaporated samples and CNT growth was exponentially better on the sputtered samples. During evaporation, the metal film laid down is softer and it does not embed itself as deep as the sputtered films on the lower layer, in our case Ti, due to the use of less kinetic energy. The AFM phase measurements also showed that evaporated films tend to have granules that are closer together making it harder for the growth of CNTs. We can also see that between the three sputtered films, the 50 $\mathring{A}$ sample in Figure 4.19(b) has a more dense carpet and its CNTs are smaller in diameter than the 100 $\mathring{A}$ and 200 $\mathring{A}$ sputtered Ni films seen in Figures 4.20(b) and 4.21(b). This makes sense with our pretreatment study since the catalyst size for the thinner films had a smaller diameter, it follows that the CNTs from this films will also have smaller diameters. Smaller diameter catalyst on sputter films also bring higher density as seen on Figures 4.12, 4.13, 4.14, 4.15, 4.16, and 4.17. When we look closely at Figure 4.21(b), we can see that some of the catalyst can still be seen on the substrate indicating that the thicker nickel needs more pretreatment time to break up into smaller size particles to get a smaller diameter CNT and a higher density of CNTs.

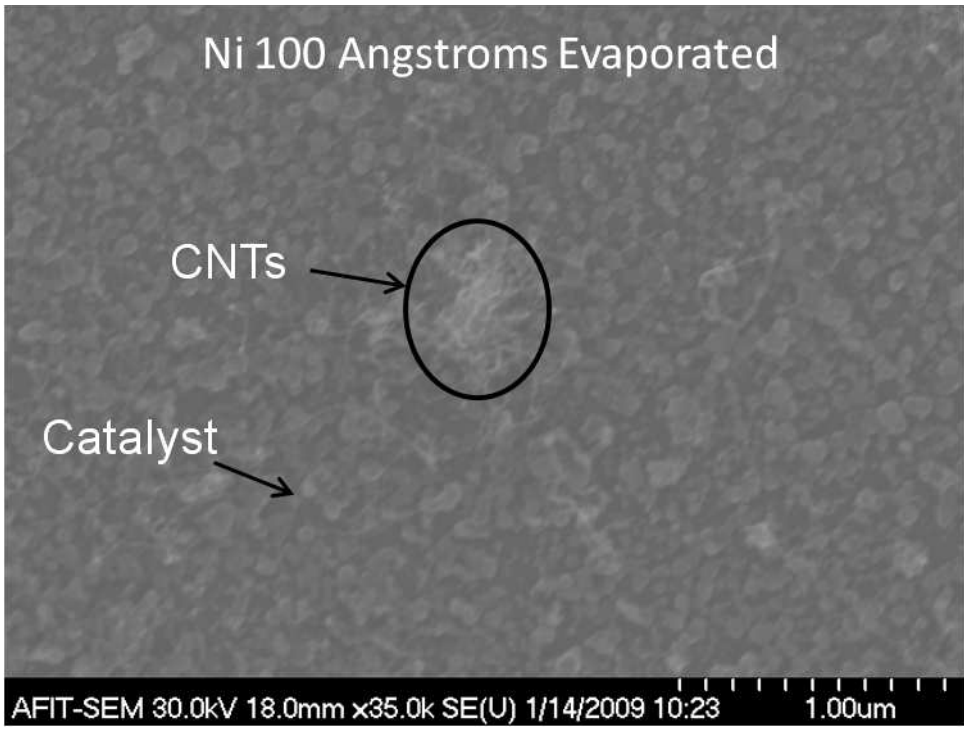


(a)

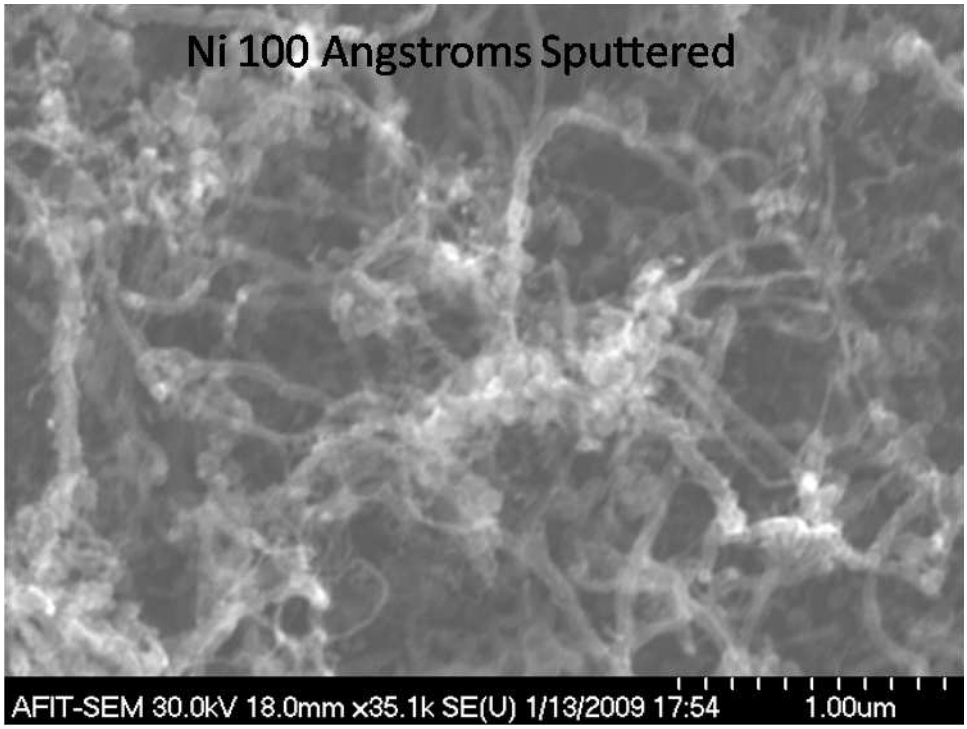


(b)

Figure 4.19: SEM figure of CNT grown for 2 minutes and pretreated for 5 minutes. (a) Evaporated Ni 50 $\mathring{A}$ thick had barely any growth. (b) Sputtered Ni 50 $\mathring{A}$ thick had excellent growth.

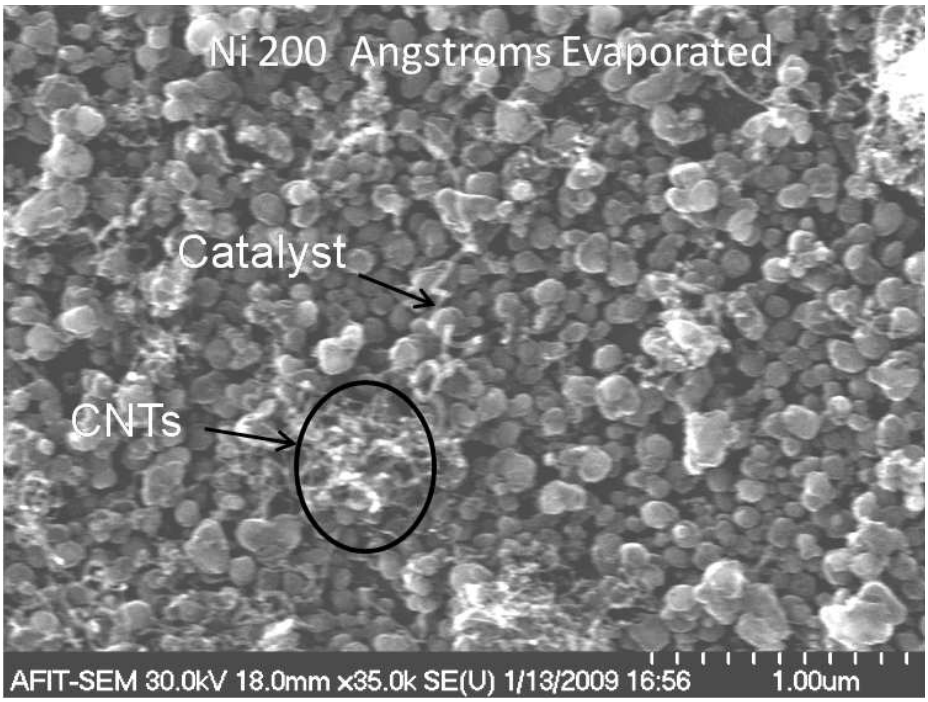


(a)

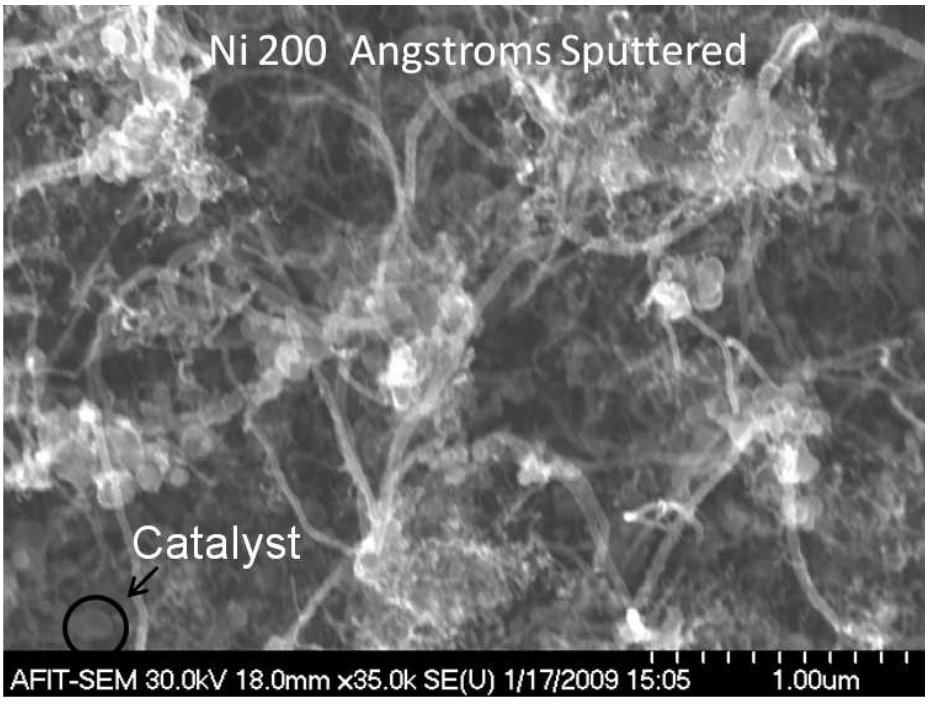


(b)

Figure 4.20: SEM figure of CNT grown for 2 minutes and pretreated for 5 minutes. (a) Evaporated Ni 100 $\mathring{A}$ thick had barely any growth. (b) Sputtered Ni 100 $\mathring{A}$ thick had excellent growth.



(a)



(b)

Figure 4.21: SEM figure of CNT grown for 2 minutes and pretreated for 5 minutes. (a) Evaporated Ni 200 $\mathring{A}$ thick minimal growth. (b) Sputtered Ni 200 $\mathring{A}$ thick had growth but some large nickel granules can be seen in the surface.

The next step in the process is to try to grow CNTs into a patterned surface. The cathode-gate structure from Section 4.2.2 will be used to pattern the CNTs. CNTs are expected to grow inside the different patterns designed and also inside the 300 μm windows that where used in the alignment process. The thin SiO_2 layer and the unknown substance on top of the nickel was still present when we introduced the samples into the MPECVD chamber. During the pretreatment, some of the unknown substance and SiO_2 created some problems by protecting the nickel and not letting it granulate to form dense CNTs. Figure 4.22 shows how the SiO_2 that is left over on one of the 4 μm circle patterned covers the nickel, but some of the CNTs are still able to grow. To try to clear the unknown substances, one device was subjected to HF for 20 seconds. The HF completely destroyed all the gate structure but it was able to clean some of the SiO_2 off the wafer as seen on Figure 4.23(a). The center of the 4 μm circle still had minimal CNT growth since apparently the unknown substance was thickest at this point. On the same wafer, the 3 μm circles did not have any of its circles cleared enough to grow any CNTs. We did get growth on the perimeter of the circles as seen on Figure 4.23(b). The circle diameter difference was enough to cause CNTs either to grow or not to grow on the patterned devices. On the 4 μm case, the HF was able to etch down deeper so it did not attack the sidewalls as much as it

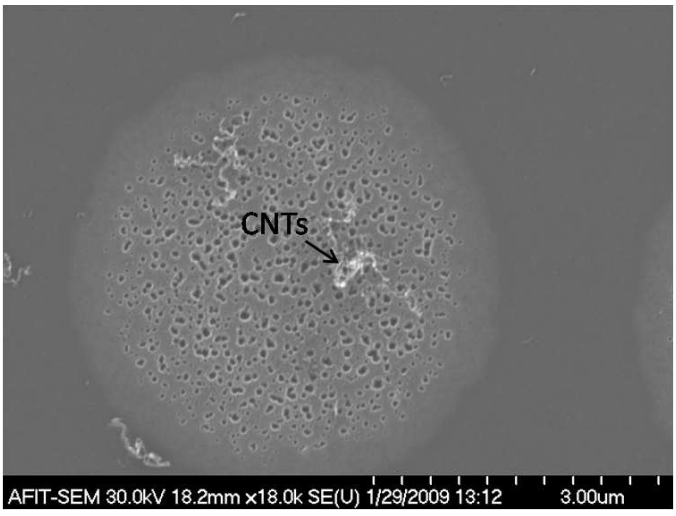
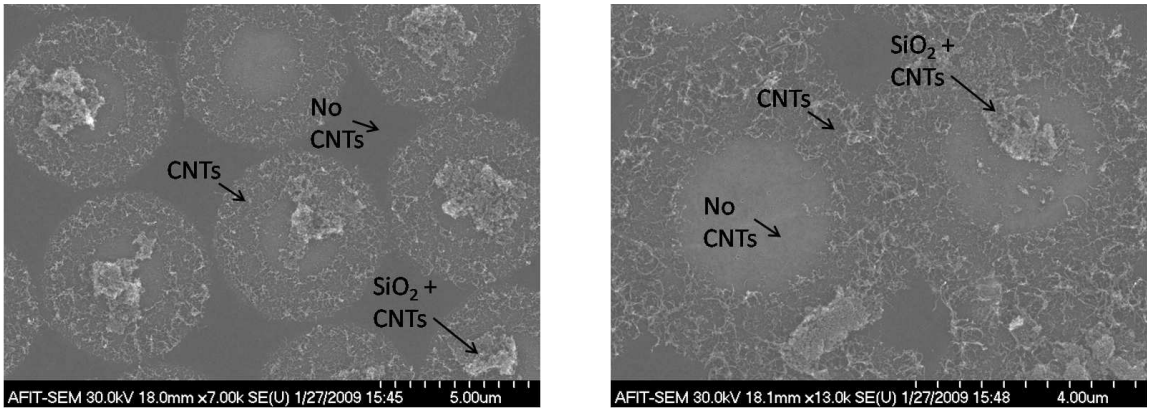


Figure 4.22: Patterned Growth Through SiO_2.



(a) (b)

Figure 4.23: HF treated patterned growth. (a) HF treated patterned growth on 4 μm circle. The center of the circle still contains some of the unknown substance and SiO_2. (b) HF treated patterned growth on 3 μm circle. The circle still has a thick SiO_2 layer so no CNTs grow in the middle but multiple CNTs are able to grow on the perimeter.

did on the 3 μm case were the thickness of the unknown substance in addition to the SiO_2 left more HF reactants to attack the sidewalls and not loose the rate it etches going down. A note to make is that the wafer was not agitated when placed in the HF container. A second wafer was subjected to a BOE etch for 1.5 minutes. The excess time was able to clear some of the left over SiO_2 and the unknown substances. All the gate structures were destroyed on this wafer. The purpose of the BOE etch was to decrease the growth of CNTs on the edges of the structure to be built. Figure 4.24 shows how the CNTs did not grow as tall on the edges of a 300 μm window. This will help in preventing cathode and gate shorting and also increase the efficiency of the CNT emitters by getting most of the electrons from the middle of the structure. Once the middle CNTs burn up the ones in the sides that are lower and are affected less by the electric field from the gate will act as the new electron emitters.

4.4 Chapter Summary

This chapter discussed the results of the fabrication and testing of the vacuum chamber to be used for CNT field emission testing. The constant etch rate of CR-4 was

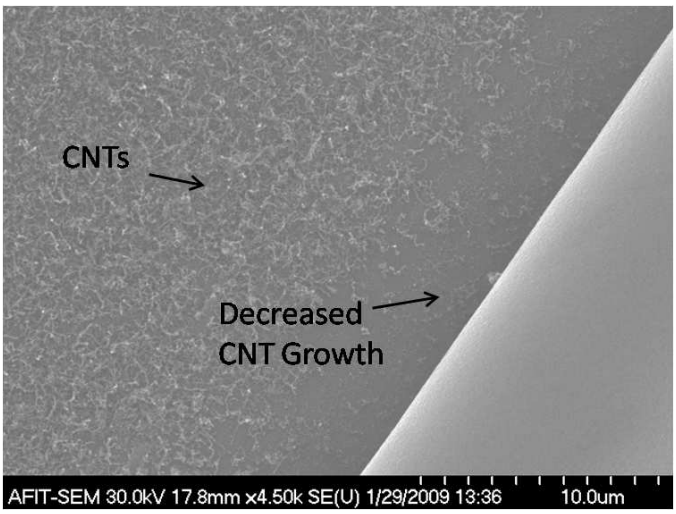


Figure 4.24: Growth of CNTs after BOE etch. CNT growth is confined to the middle of the structure decreasing the chance of cathode to gate shorting and increasing emitter efficiency.

discussed in comparison to the non constant etch rate of TFA during the fabrication of the cathode-gate structure. The pretreatment time for the granulation of the nickel catalyst was studied to be able to attain CNT growth.

V. Conclusions and Recommendations

The research presented in this thesis pertains to the gowth of CNTs for field emission. It included the fabrication of a system for field emission testing, fabrication of a integrated triode structure and the growth of CNTs from a nickel catalyst utilizing a MPECVD system.

5.1 Field Emission Testing Structure

The chamber used for field emission testing has been completed with the exception of the electrical connections from the chamber into the device. The sample puck to facilitate this connection will have to be attached to the chamber and connections will have to be made from the sample puck to the MHV connection on the chamber and from the sample puck to the sapphire PCB board.

5.2 Triode Structure

The triode structure suffered some setbacks during the fabrication process. The lack of ICP during the RIE limited the depth that we were able to etch onto the quartz wafer creating a 10 μm anode gate spacing compared to the 50 μm depth desired.

The original design called for a gold layer to be deposited down right after the chrome layer on the cathode gate structure to help with the adhesion of the gold wire during wire bonding and also to facilitated the bonding during flip chip bonding. The original idea was to use the array and gate masks to pattern the gold layer. During fabrication we found that the gold etchant did not have a constant etch rate and with our small size features this method would not work. A separate mask had to be designed and is shown in Figure 5.1 to add a gold layer just to the pads. The process would require us to deposit the gold as a last step after all the etching for the cathode-gate structure has been completed. The next step would be to use 1818 photoresist to cover the pad structure as seen on Figure 5.1 to protect the gold from the gold etchant. The gold etchant would remove the gold from all other areas leaving gold only on the wire bonding pads and the flip chip bonding pads.

The RIE process used to remove the 2 μm thick layer of SiO_2 left an unknown substance on top of the nickel layer that interferes with the CNT pretreatment and growth process. HF, BOE and ashing have been used to try to remove this substance with small or no success. A possibility is that since the photoresist used for the gate array was to thin to completely protect the chrome surface, some contamination might have occurred on the etched surfaces. AFRL/RY currently uses 1813 photoresist, a resist that is thicker than 1805 but thinner than 1818, both photoresists currently used at AFIT. 1813 would be thin enough to afford the resolution needed for the array mask and might be thick enough to be able to protect our gate better than the 1805 photoresist was able to attain.

5.3 CNT Growth

Sputtered Ni catalyst demonstrated to be a better choice for the growth of CNTs due to its clean formation of nano islands when compared to evaporated films. We showed how we where able to grow a high density carpet of CNTs on sputtered nickel catalyst of different thicknesses. The CNTs did grow vertically but the tips usually

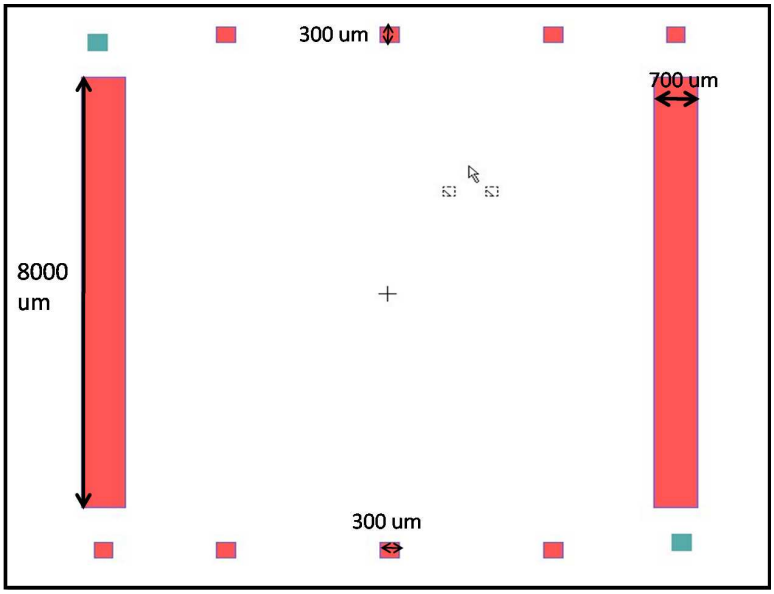


Figure 5.1: Mask designed for the addition of gold to flip chip bonding and wire bonding pads.

did not reach the verticality we where looking for. To be able to get a more vertically aligned CNT substrate, biasing during CNT growth needs to be used. By biasing the substrate, usually around -500 volts, the nickel catalyst is not only being attracted by the plasma energy but the negative bias is repelling the nickel particle.

5.4 Future Work

An important aspect of field emission is the placement of the carbon nanotubes in an array to get better field emission. We have demonstrated how we get patterned CNTs by placing a sheet of nickel down followed by other material to cover the nickel that we do not want to have CNTs grown on. A different method to achieve this would be to place the nickel catalyst in the areas where we would like the CNTs to grow only. This can be done with the help of EBL at a high cost and we would have to design the mask to use for this method. Another alternative is to use self assembled nanospheres or colloids to create the pattern for our nickel layer. Dr. Bayraktaroglu from AFRL/RY has investigated the effects of these colloids and how they can be used to create patterns of metal nanoparticles on a substrate. Figure 5.2 demonstrates how the process would work to get Ni catalyst only on selected areas. First the colloids are self assembled followed by evaporation of the nickel catalyst on the surface. Previously we have discussed how evaporated films do not create the nanoislands needed for CNT growth but in this case, no pretreatment would be needed to create these islands since the nickel film would already be deposited into nanosize islands. The next step would be to remove the excess nickel and colloids finishing with the pattern seen in Figure 5.2.

5.5 Contributions

This research has contributed the following advancements:

- The characterization of evaporated and sputtered films after a H_2 pretreatment in a MPECVD system using SEM and AFM images to determine the optimal pretreatment time for CNT growth.

- This is the first time at AFIT that CNTs have been grown from a metal catalyst.
- The design of a triode configuration in which a quartz wafer, the anode, is to be flip chip bonded to a silicon wafer, the cathode and gate, to obtain field emission from CNTs.
- The design and fabrication of a testing chamber at AFIT for field emission.

5.6 Conclusions

The ability to grow CNTs was demonstrated in a carpet form and also when patterned. Different thicknesses and methods of nickel deposition where investigated and it was discovered that sputtered films tend to work better for CNT growth due to their formation of nano islands of nickel. The next step is to perfect the vertical

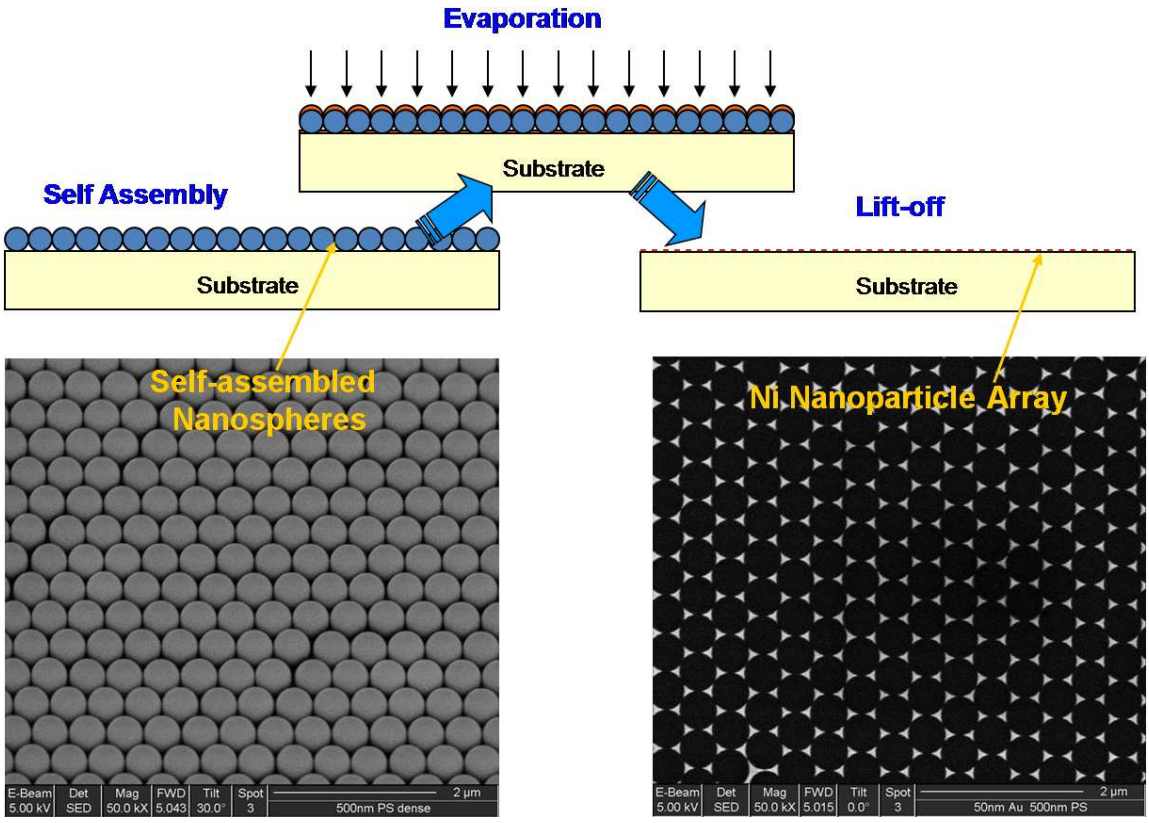


Figure 5.2: We first start with the aligned colloids over the surface where we want CNTs to grow. We then evaporate the metal over the colloids. When the colloids are removed we get Ni only over the areas where we want CNT growth [30].

growth of CNTs followed by the testing of these devices and record their field emission properties.

Appendix A. Kurt J. Lesker Parts List

Line	Quantity	U/M	Item Number	Description
1	1	EA	SP1200S	SPHERE,12" STANDARD,304SS DWG #CHA-05700 R.G
2	4	EA	F0275X000N	FLANGE,UHV,SS,BLANK,FXD,2.75" OD
3	1	PK	GA-0275	GASKET, COPPER, 2-3/4" FLANGE, 1.895"OD,1.451"ID,10/PKG
4	2	EA	HBS25028138	HEX B,N,&W SET,(25)1/4-28X1.38 FOR 2-1/8 AND 2-3/4" FLANGES
5	1	EA	F0450X000N	FLANGE,UHV,SS,BLANK,FXD,4.50" OD
6	1	PK	GA-0450	GASKET, COPPER, 4-1/2" FLANGE 3.243"OD,2.506"ID,10/PKG
7	1	PK	HBS31224200	HEX B,N,&W SET,(25)5/16-24X2.0 FOR 4-1/2, 4-5/8, 6NR FLANGES
8	2	EA	F0600X000N	FLANGE,UHV,SS,BLANK,FXD,6"OD
9	1	PK	GA-0600	GASKET, COPPER, 6" FLANGE, 4.743"OD,4.006"ID 10/PKG
10	2	PK	HBS31224225	HEX B,N,&W SET,(25)5/16-24 X 2-1/4 FOR 6R,6-3/4",8"FLANGES

Line	Quantity	U/M	Item Number	Description
11	2	EA	F0600X400N	FLANGE,UHV,SS,BORED,FXD,6"OD, 4"C-BORE
12	2	EA	VPZL-600	VIEWPORT,ZERO-LENGTH,KOVAR SLEEVE, 6" UHV
13	2	PK	HBS31224200	HEX B,N,&W SET,(25)5/16-24X2.0 FOR 4-1/2, 4-5/8, 6NR FLANGES
14	1	PK	VZCUA100	GASKET,ANNEALED,CU,FOR 6"OD UHV FLANGE,5/PKG
15	4	EA	F0800X000N	FLANGE,UHV,SS,BLANK,FXD,8"OD
16	2	PK	GA-0800	GASKET, COPPER, 8" FLANGE, 6.743"OD,6.007"ID,10/PKG
17	4	PK	HBS31224225	HEX B,N,&W SET,(25)5/16-24 X 2-1/4 FOR 6R,6-3/4",8"FLANGES
18	2	EA	F0800X600N	FLANGE,UHV,SS,BORED,FXD,8"OD, 6"C-BORE
19	2	EA	VPZL-800	VIEWPORT, ZERO-LENGTH, SS, 5-3/8" VIEW AREA, 8" FLANGE
20	2	PK	HBS31224225	HEX B,N,&W SET,(25)5/16-24 X 2-1/4 FOR 6R,6-3/4",8"FLANGES

Line	Quantity	U/M	Item Number	Description
21	1	PK	VZCUA150	GASKET,ANNEALED,CU,FOR 8"OD UHV FLANGE,5/PKG
22	2	EA	SG0600MCCF	GATE BONNET,8"UHV
23	2	PK	HBK31224175	HEX BOLT KIT FOR 8"&10" TAPPED FLANGES, (25) 5/16-24X1.75
24	1	EA	SG0400MCCF	GATE BONNET,6"UHV
25	1	PK	HBK31224125	HEX BOLT KIT,3-3/8,4-1/2,4-5/8 6"TPD FLG,(25)5/16-24 X 1.25
26	1	EA	LLC-PLNR4	LOAD LOCK VESSEL,PLANER FOR 100MM WAFER DWG# A0022144 R.B *** No Cancel No Return Item ***
27	1	PK	GA-0450	GASKET, COPPER, 4-1/2" FLANGE 3.243"OD,2.506"ID,10/PKG
28	1	PK	HBS31224200	HEX B,N,&W SET,(25)5/16-24X2.0 FOR 4-1/2, 4-5/8, 6NR FLANGES
29	1	EA	F0275XQF25	ADAPTER,SS,2-3/4"UHV FLANGE TO QF25 FLANGE

Line	Quantity	U/M	Item Number	Description
30	1	EA	QF25-100-SRV	CENTERING RING,SS,QF25,VITON
31	1	EA	QF16-075-SRV	CENTERING RING,SS,QF16,VITON O-RING,3/4"
32	1	EA	QF25-100-CS	CLAMP,SS,QF25,MACHINED,1"
33	1	EA	QF16-075-CS	CLAMP,SS,QF16,MACHINED, 1/2" & 3/4"
34	1	EA	QF16-075-SB	FLANGE,BLANK,SS,QF16
35	1	EA	C-0275	CROSS,4-WAY,SS,1.5" TUBE OD, 2-3/4" UHV,2.46" "A" DIM
36	1	PK	GA-0275	GASKET, COPPER, 2-3/4" FLANGE, 1.895"OD,1.451"ID,10/PKG
37	1	EA	HBS25028138	HEX B,N,&W SET,(25)1/4-28X1.38 FOR 2-1/8 AND 2-3/4" FLANGES
38	1	EA	PM016207AU	CENTERING RING,W/SCREEN,ANTI-SLIP DN63 ISO-K/ISO-KF PUMPS *** No Cancel No Return Item ***
39	1	EA	P4564309ZE	CABLE,110V,POWER CABLE FOR CONTROLLER *** No Cancel No Return Item ***

Line	Quantity	U/M	Item Number	Description
40	1	EA	PMZ01253	AIR COOLING,TMH/U071 *** No Cancel No Return Item ***
41	1	EA	QF63-SAVR	CENTERING RING,QF63,SS INNER, AL OUTER,VITON O-RING
42	6	PK	QF-LDC-CS1	CLAMP,FOR ISO FLANGE,STEEL, DOUBLE CLAW,QF63-QF250,EACH
43	1	EA	SG0250MVIK	GATE VALVE,SS,2.50",MANUAL, VITON BONNET,ISO 63-K *** No Cancel No Return Item ***
44	1	EA	QF25XQF16C	REDUCING FULL NIPPLE,CONICAL, SS,QF25 TO QF16
45	1	EA	ED-A72601906	PUMP,MECHANICAL,XDS10,115V,1P 50/60HZ
46	1	EA	ED-A50507000	LINE CORD,PUMP,USA/JAPAN, FITS XDS PUMPS *** No Cancel No Return Item ***
47	1	EA	ED-A50597000	SILENCER,EXHAUST,FOR XDS5 & XDS10 PUMPS *** No Cancel No Return Item ***
48	1	EA	QF25-100-C	CLAMP,ALUMINUM,QF25,CAST 1"

Line	Quantity	U/M	Item Number	Description
49	1	EA	QF25-100-SRV	CENTERING RING,SS,QF25,VITON
50	1	EA	QF16-075-T	TEE,SS,QF16 FLGS,3/4"OD TUBE, "A"-1.57"
51	2	EA	SA0075MVQF	RT ANGLE VALVE, SS, QF16 FLG, MANUAL, 3/4" PORT, VIT SEALED
52	2	EA	MHT-QF-A36	FLEX HOSE,SS,36"OAL,QF16 FLGS, 3/4"ID,.006"WALL
53	2	EA	IFTMG042033	INST F/T,MHV,GRNDED,5KV,(4) .094"SS COND,3A,2.75"UHV *** No Cancel No Return Item ***
54	2	PK	FTASSC094	CONNECTOR,PUSH ON TO .094" PIN 15A,UP TO .050"WIRE,10/PKG
55	8	EA	FTAMHV	ELECT CONNECTOR, TYPE MHV, FITS RG-59U COAX CABLE *** No Cancel No Return Item ***
56	2	EA	F0275X4SWG	ADAPTER FITTING, 2-3/4"CF TO 1/4" SWAGELOK
57	2	EA	SS-4H	VALVE,SHUT-OFF,"H" SERIES, MODEL H,1/4"SWAGELOK
58	1	EA	KJL6600C	ION GAUGE CONTROLLER,115/220V 4 CONVECTION

Line	Quantity	U/M	Item Number	Description
59	1	EA	G100F	GAUGE TUBE,B-A,KOVAR,1" ON 2-3/4"FLANGE,IRIDIUM FILAMENT
60	2	EA	KJL912164	CONVECTION TUBE,SS,2.75"UHV FLG
61	1	EA	KJLIGCCV10	CABLE, CONVECTION 10FT LONG, FOR USE WITH KJL2200 KJL4500 & KJL6600 CONTROLLERS *** No Cancel No Return Item ***
62	2	EA	KJLIGC10G	CABLE,ION GAUGE,GLASS TUBE, 10FT LONG,FOR USE WITH KJL2200 KJL4500 & KJL6600 CONTROLLERS
63	1	EA	PMP03666	TURBO PUMP,TMU262,220L/S,6"UHV CONTROLLER ON-BOARD *** No Cancel No Return Item ***
64	1	EA	P4564309ZE	CABLE,110V,POWER CABLE FOR CONTROLLER *** No Cancel No Return Item ***
65	1	EA	PMZ01252	AIR COOLING,TMH/U261 *** No Cancel No Return Item ***
66	1	EA	PM016315	SPLINTER SHIELD,TURBO 6" UHV INLET *** No Cancel No Return Item ***

Line	Quantity	U/M	Item Number	Description
67	2	EA	VZTL	THREAD LUBRICANT 1oz TUBE
68	2	EA	VZGRT	GASKET REMOVAL TOOL
69	2	EA	FTACBL25BB36	CABLE,COAX,1/4",3000V,15A,36" OAL, "B" TERMINATION BOTH ENDS *** No Cancel No Return Item ***
70	1	EA	XTEMP	*** PART NUMBER WILL BE: PMP03655 *** No Cancel No Return Item ***
71	1	EA	VXLRPH024M	LIN'R R&P TR'SP'TER HIGH STAB 24"TRVL,4-1/2"UHV,MAGIDRIVE DWG #LRP-5461 R.5 *** No Cancel No Return Item ***
72	1	EA	F0275XQF25	ADAPTER,SS,2-3/4"UHV FLANGE TO QF25 FLANGE
73	2	EA	SA0100MVQF	RT ANGLE VALVE, SS, QF25 FLG, MANUAL, 1" PORT, VITON SEALED
74	1	EA	QF25-100-T	TEE,SS,QF25 FLGS,1"OD TUBE, "A"-1.97"
75	1	EA	MHT-QF-B36	FLEX HOSE,SS,36"OAL,QF25 FLGS, 1"ID,.006"WALL

Line	Quantity	U/M	Item Number	Description
76	8	EA	QF25-100-SRV	CENTERING RING,SS,QF25,VITON
77	8	EA	QF16-075-SRV	CENTERING RING,SS,QF16,VITON O-RING,3/4"
78	8	EA	QF25-100-CS	CLAMP,SS,QF25,MACHINED,1"
79	8	EA	QF16-075-CS	CLAMP,SS,QF16,MACHINED, 1/2" & 3/4"
80	2	EA	T-0275	TEE, SS, 2.46"A, 1.5"OD, 2.75" FLANGE
81	1	PK	GA-0275	GASKET, COPPER, 2-3/4" FLANGE, 1.895"OD,1.451"ID,10/PKG
82	1	EA	HBS25028138	HEX B,N,&W SET,(25)1/4-28X1.38 FOR 2-1/8 AND 2-3/4" FLANGES
83	1	EA	SG0150MVCF	GATE VALVE,SS,1.50",MANUAL, VITON BONNET,2.75"UHV
84	1	EA	G100F	GAUGE TUBE,B-A,KOVAR,1" ON 2-3/4"FLANGE,IRIDIUM FILAMENT
85	1	EA	KJLIGCCV10	CABLE, CONVECTION 10FT LONG, FOR USE WITH KJL2200 KJL4500 & KJL6600 CONTROLLERS *** No Cancel No Return Item ***

Appendix B. Process Follower PCB

Wafer	Purpose	Mask	Process	Print Date
	CNTS	*PCB*	PCB	

Init.	Process Step	Notes	Date Time
	INSPECT WAFER: □ Note any defects	**Start Date** **Start Time**	
	PRE-METAL DIP: □ 30 sec dip (1:10) BOE:DI Water □ 3x DI Water rinse □ Dry wafer with nitrogen on clean texwipes		
	METAL DEPOSITION: □ Evaporate 200 Å Ti / 5000Å Au or sputter 200 Å Ti / 10000Å Au		
	SOLVENT CLEAN: □ 30 sec acetone rinse at 500 rpm □ 20 sec isopropyl rinse at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	BAKE: □ 2 min 110 °C Hot plate bake		
	1818 COAT: □ Flood wafer with 1818 □ 10 sec spin at 500 rpm, ramp=200 □ 30 sec spin at 4000 rpm, ramp=200 □ 75 sec 110°C hot plate bake □ Use acetone to remove 1818 on backside		
	EXPOSE 1818 with PCB MASK: □ ☐No alignment □ ☐3.0 sec exposure on EVG 620		
	1818 DEVELOP: □ 60 sec develop with 351:DI Water (1:5) at 500 rpm □ 30 sec DI Water rinse at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: □ ☐Place wafer flat towards top of microscope □ ☐Inspect wafer pattern □ ☐Check Lithography : □ ☐Open □ ☐Clean □ ☐Sharp Definition		
	MEASURE: □ Measure photoresist step height in three locations Top _____ Middle _____ Bottom _____		
	ASHER DESCUM □ 2 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	ETCH METAL: □ Etch gold using gold etcher TFA. Rate is 28 Å/sec □ Rinse wafer in DI water □ Visually inspect for metal removal □ 30 sec spray with acetone bottle at 500 rpm □ 30 sec spray with isopropyl alcohol at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	ASHER DESCUM □ 4 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	INSPECT WAFER: □ Inspect for resist removal under microscope		
	MEASURE: □ Measure step height in three locations Top _____ Middle _____ Bottom _____	***Finish Date*** ***Finish Time***	

Appendix C. Process Follower Anode

Wafer	Purpose	Mask	Process	Print Date
	CNTS	*ANODE*	ANODE	

Init.	Process Step	Notes	Date Time
	INSPECT WAFER: □ Note any defects on Quartz wafer	**Start Date** **Start Time**	
	PRE-METAL DIP: □ 30 sec dip (1:10) BOE:DI Water □ 3x DI Water rinse □ Dry wafer with nitrogen on clean texwipes		
	METAL DEPOSITION: □ Evaporate 1000Å Cr or sputter 1000Å Cr		
	SOLVENT CLEAN: □ 30 sec acetone rinse at 500 rpm □ 20 sec isopropyl rinse at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	BAKE: □ 2 min 110 °C Hot plate bake		
	1818 COAT: □ Flood wafer with 1818 □ 10 sec spin at 500 rpm, ramp=200 □ 30 sec spin at 4000 rpm, ramp=200 □ 75 sec 110°C hot plate bake □ Use acetone to remove 1818 on backside		
	EXPOSE 1818 with PCB MASK: □ ☐No alignment □ ☐3.0 sec exposure on EVG 620		
	1818 DEVELOP: □ 60 sec develop with 351:DI Water (1:5) at 500 rpm □ 30 sec DI Water rinse at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: □ ☐Place wafer flat towards top of microscope □ ☐Inspect wafer pattern □ ☐Check Lithography : □ ☐Open □ ☐Clean □ ☐Sharp Definition		
	MEASURE: □ Measure photoresist step height in three locations Top _____ Middle _____ Bottom _____		
	ASHER DESCUM □ 2 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	ETCH METAL: □ Etch Cr using Cr-4 etcher. Rate is 22 Å/sec □ Rinse wafer in DI water □ Visually inspect for metal removal		
	ETCH QUARTZ WAFER □ Etch Quartz using HF. Rate is ___ Å/sec □ Rinse wafer in DI water □ Measure step height in three locations for 50 micrometers Top _____ Middle _____ Bottom _____		

Wafer	Purpose	Mask	Process	Print Date
	CNTS	*ANODE*	ANODE	

	REMOVE PHOTORESIST ☐ 30 sec spray with acetone bottle at 500 rpm ☐ 30 sec spray with isopropyl alcohol at 500 rpm ☐ Dry with nitrogen at 500 rpm ☐ Dry wafer with nitrogen on clean texwipes		
	ASHER DESCUM ☐ 4 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	INSPECT WAFER: ☐ Inspect for resist removal under microscope		
	MEASURE: ☐ Measure step height in three locations Top _____ Middle _____ Bottom _____		
		Finish Date **Finish Time**	

Appendix D. Process Follower Cathode-Gate

Wafer	Purpose	Mask	Process	Print Date
	CNTS	*Array, Gate, Ground*	Cathode-Gate	

Init.	Process Step	Notes	Date Time
	INSPECT WAFER: ☐ Note any defects on Si wafer	**Start Date** **Start Time**	
	PRE-METAL DIP: ☐ 30 sec dip (1:10) BOE:DI Water ☐ 3x DI Water rinse ☐ Dry wafer with nitrogen on clean texwipes		
	DEPOSITION: ☐ Sputter 200 Å Ti ☐ Sputter 100 Å Ni ☐ Deposit 2 µm of SiO_2 by PECVD ☐ Evaporate 2500Å Cr or sputter 2500Å Cr		
	SOLVENT CLEAN: ☐ 30 sec acetone rinse at 500 rpm ☐ 20 sec isopropyl rinse at 500 rpm ☐ Dry with nitrogen at 500 rpm ☐ Dry wafer with nitrogen on clean texwipes		
	BAKE: ☐ 2 min 110 °C Hot plate bake		
	1805 COAT: ☐ Flood wafer with 1805 ☐ 10 sec spin at 500 rpm, ramp=200 ☐ 30 sec spin at 4000 rpm, ramp=200 ☐ 75 sec 110°C hot plate bake ☐ Use acetone to remove 1805 on backside		
	EXPOSE 1805 with Array MASK: ☐☐No alignment ☐☐3.0 sec exposure on MA6		
	1805 DEVELOP: ☐ 30 sec develop with 351:DI Water (1:5) at 500 rpm ☐ 30 sec DI Water rinse at 500 rpm ☐ Dry with nitrogen at 500 rpm ☐ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: ☐☐Place wafer flat towards top of microscope ☐☐Inspect wafer pattern ☐☐Check Lithography : ☐☐Open ☐☐Clean ☐☐Sharp Definition		
	MEASURE: ☐ Measure photoresist step height in three locations Top _____ Middle _____ Bottom _____		
	ASHER DESCUM ☐ 2 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	ETCH METAL: ☐ Etch Cr using Cr-4 etcher. Rate is 22 Å/sec (153 Seconds) ☐ Rinse wafer in DI water ☐ Visually inspect for metal removal		

	ETCH SiO_2 (Dry Etch) ☐ 42 minute etch using RIE and the following Gasses • CF_4 at 40 sccm • O_2 at 3 sccm ☐ Rinse wafer in DI water ☐ Measure step height in three locations Top _____ Middle _____ Bottom _____		
	ETCH SiO_2 (Wet Etch) ☐ Etch SiO_2 using BOE. Rate is 490 nm/min Etch for 15 seconds ☐ Rinse wafer in DI water ☐ Visually inspect for Dielectric removal		
	REMOVE PHOTORESIST ☐ 30 sec spray with acetone bottle at 500 rpm ☐ 30 sec spray with isopropyl alcohol at 500 rpm ☐ Dry with nitrogen at 500 rpm ☐ Dry wafer with nitrogen on clean texwipes		
	ASHER DESCUM ☐ 4 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	INSPECT WAFER: ☐ Inspect for resist removal under microscope		
	MEASURE: ☐ Measure step height in three locations Top _____ Middle _____ Bottom _____		
	SOLVENT CLEAN: ☐ 30 sec acetone rinse at 500 rpm ☐ 20 sec isopropyl rinse at 500 rpm ☐ Dry with nitrogen at 500 rpm ☐ Dry wafer with nitrogen on clean texwipes		
	BAKE: ☐ 2 min 110 °C Hot plate bake		
	1805 COAT: ☐ Flood wafer with 1805 ☐ 10 sec spin at 500 rpm, ramp=200 ☐ 30 sec spin at 4000 rpm, ramp=200 ☐ 75 sec 110°C hot plate bake ☐ Use acetone to remove 1805 on backside		
	EXPOSE 1805 with Gate MASK: ☐☐Align so all array shapes fit inside large square pads ☐☐3.0 sec exposure on MA6		
	1805 DEVELOP: ☐ 30 sec develop with 351:DI Water (1:5) at 500 rpm ☐ 30 sec DI Water rinse at 500 rpm ☐ Dry with nitrogen at 500 rpm ☐ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: ☐☐Place wafer flat towards top of microscope ☐☐Inspect wafer pattern ☐☐Check Lithography : ☐☐Open ☐☐Clean ☐☐Sharp Definition		
	MEASURE: ☐ Measure photoresist step height in three locations Top _____ Middle _____ Bottom _____		
	ASHER DESCUM ☐ 2 min, 75 W, 400 sccm O_2, LFE Barrel Asher		

	ETCH METAL: □ Etch Cr using Cr-4 etcher. Rate is 22 Å/sec □ Rinse wafer in DI water □ Visually inspect for metal removal		
	REMOVE PHOTORESIST □ 30 sec spray with acetone bottle at 500 rpm □ 30 sec spray with isopropyl alcohol at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	ASHER DESCUM □ 4 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	INSPECT WAFER: □ Inspect for resist removal under microscope		
	MEASURE: □ Measure step height in three locations Top _____ Middle _____ Bottom _____		
	SOLVENT CLEAN: □ 30 sec acetone rinse at 500 rpm □ 20 sec isopropyl rinse at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	BAKE: □ 2 min 110 °C Hot plate bake		
	1805 COAT: □ Flood wafer with 1805 □ 10 sec spin at 500 rpm, ramp=200 □ 30 sec spin at 4000 rpm, ramp=200 □ 75 sec 110°C hot plate bake □ Use acetone to remove 1805 on backside		
	EXPOSE 1805 with Array MASK: □☐Align using alignment marks provided □☐3.0 sec exposure on MA6		
	1805 DEVELOP: □ 30 sec develop with 351:DI Water (1:5) at 500 rpm □ 30 sec DI Water rinse at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: □☐Place wafer flat towards top of microscope □☐Inspect wafer pattern □☐Check Lithography : □☐Open □☐Clean □☐Sharp Definition		
	MEASURE: □ Measure photoresist step height in three locations Top _____ Middle _____ Bottom _____		
	ASHER DESCUM □ 2 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	ETCH SiO_2 (Wet Etch) □ Etch SiO_2 using BOE. Rate is 490 nm/min. Etch for 4.1 minutes □ Rinse wafer in DI water □ Visually inspect for Dielectric removal		
	REMOVE PHOTORESIST □ 30 sec spray with acetone bottle at 500 rpm □ 30 sec spray with isopropyl alcohol at 500 rpm □ Dry with nitrogen at 500 rpm □ Dry wafer with nitrogen on clean texwipes		

	ASHER DESCUM ☐ 4 min, 75 W, 400 sccm O_2, LFE Barrel Asher		
	INSPECT WAFER: ☐ Inspect for resist removal under microscope		
	MEASURE: ☐ Measure step height in three locations Top _____ Middle _____ Bottom _____		
		Finish Date **Finish Time**	

Appendix E. MPECVD Procedures

The following is the procedures to operate the MPECVD system:

Safety requirements

- Safety goggles must be worn while operating equipment.
- Microwave system will be check monthly to insure no radiation leakage.
- Hydrogen and methane sensors to be inspected by PMEL.

Start Up

1. Set Sample In chamber.
2. Annotate H2 reading on exhaust line.
3. Bring Chamber to desired Vacuum, for pretreatment and CNT growth 20 Torr.
4. Turn on H_2, N_2 and CH_4 bottles.
5. Turn on Water supply (Yellow Handle).
6. Turn on Chiller.
7. Turn on Interlock Panel.
8. Turn on air switch on interlock panel.
9. Make sure all lights on interlock are on with the exception of the BP(by-pass) light.
10. Turn on stage height controller and set height to 65.
11. Turn on temperature controller and set desired temperature.
12. Turn on stage heating RF power supply and turn on (Once this is done you should see temperature rising on the temperature controller display).
13. Turn on Microwave power supply.
14. Set H_2 at 135 sccm, Temperature to 400 °C and microwave power to 400 W for desired time.

15. Set H_2 and CH_4 with a flow ratio of 1:8 with total flow of 135 sccm, temperature at 650 °C, Microwave power of 1 kW for desired time.

    Shut Down

1. Shut down plasma and microwave transmitter.
2. Turn off CH_4 flow.
3. Shut down RF stage heater power supply.
4. Set H_2 to 300 sccm to cool down stage to 30 °C and to flush out system of any loose CNTs. H_2 is used for cooling since it has been used during the complete process and it will not interact with the heated substrate. This usually takes about 20 minutes.
5. Turn H_2 Flow off.
6. Turn on N_2 flow to get all H_2 out of chamber. Once the exhaust sensor reads the H_2 value as noted on step 2 off start up close the gate valve from the pump.
7. Bring chamber to atmosphere.
8. Purge chamber.
9. Take out sample.
10. Close chamber door.
11. Turn off N_2 flow. Open gate valve so chamber pumps down to desired pressure.
12. Turn off H_2, N_2 and CH_4 bottles.
13. Turn off air.
14. Turn off temperature controller.
15. Turn off Stage height controller and interlock panel.
16. Turn off chiller and water supply.

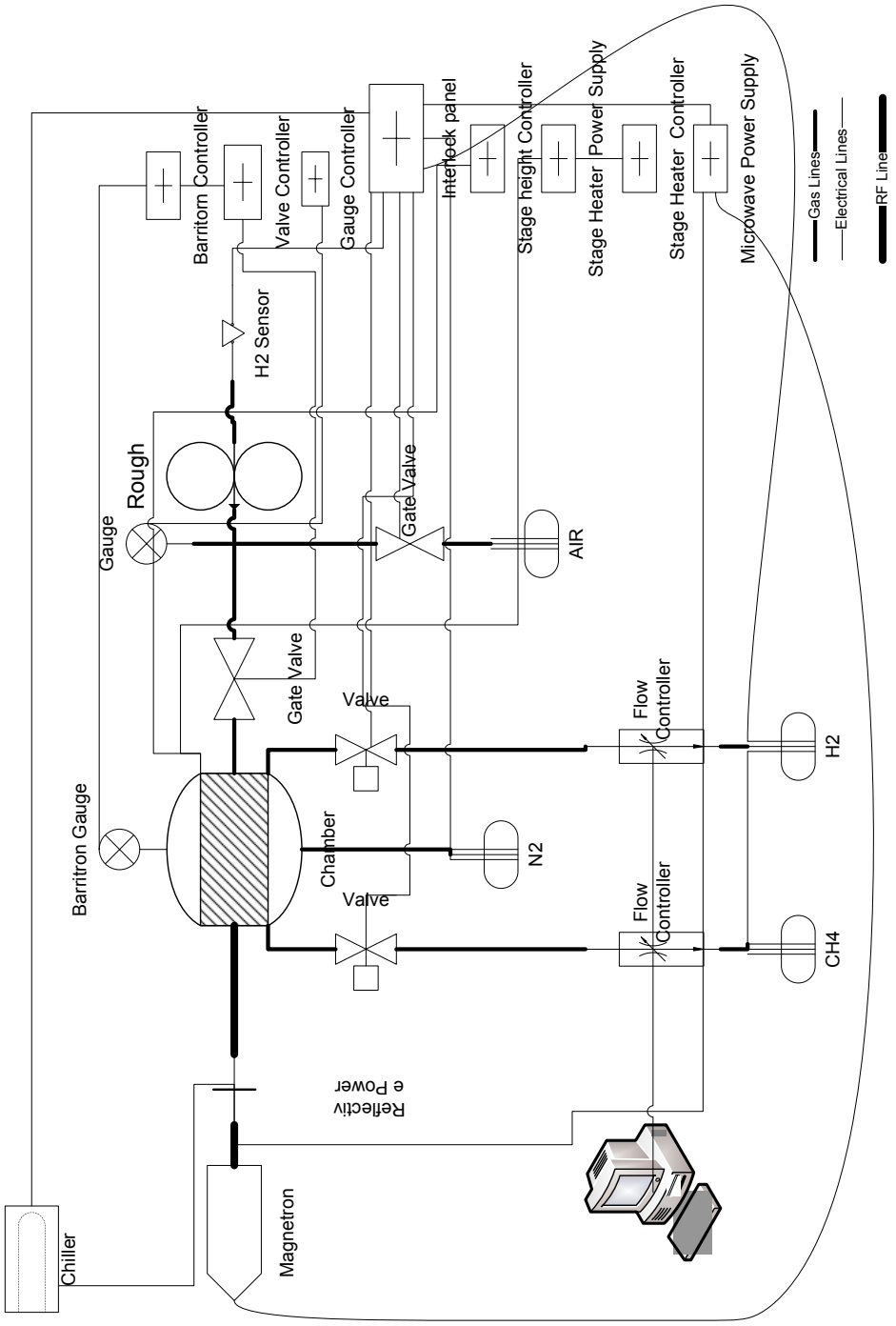


Figure F.1: AFRL/RZ MPECVD System Schematic.

Bibliography

1. Z. Yaniv, "Furthering the hdtv revolution - the cnt fed display."
2. G. Fursey, *Field Emission in Vacuum Electronics*. Kluwer Academic/Plenum Publishers, 2005.
3. M. C. Pochet, "Characterization of the field emission properties of carbon nanotube film formed on silicon carbide substrate by surface decomposition," Master's thesis, Air Force Institute of Technology, 2006.
4. S. Rotkin and S. Subramoney, *Applied Physics of Carbon Nanotubes*. Springer-Verlag New York, NY, USA, 2005.
5. H. S. Nalwa, *Nanostructured Materials and nanotechnology*. Academic Press San Diego, California, USA, 2002.
6. B. Bhushan, *Springer Handbook of Nanotechnology*. Springer-Verlag New York, NY, USA, 2004.
7. C. M. Lieber, July 2008.
8. A. Rochefort, July 2008.
9. M. J. Bronikowski, "Cvd growth of carbon nanotube bundle arrays," *Carbon,*, vol. 44, pp. 2822–2832, 11 2006.
10. J. Koohsorkhi, Y. Abdi, S. Mohajerzadeh, H. Hosseinzadegan, Y. Komijani, and E. A. Soleimani, "Fabrication of self-defined gated field emission devices on silicon substrates using pecvd-grown carbon nano-tubes.," *Carbon*, vol. 44, no. 13, pp. p2797 – 2803, 20061101.
11. S. H. Lim, K. C. Park, J. H. Moon, H. S. Yoon, D. Pribat, Y. Bonnassieux, and J. Jang, "Controlled density of vertically aligned carbon nanotubes in a triode plasma chemical vapor deposition system," *Thin Solid Films,*, vol. 515, pp. 1380–1384, 12/5 2006.
12. D. Kim, S. H. Lim, A. J. Guilley, C. S. Cojocaru, J. E. Boure, L. Vila, J. H. Ryu, K. C. Park, and J. Jang, "Growth of vertically aligned arrays of carbon nanotubes for high field emission," *Thin Solid Films,*, vol. 516, pp. 706–709, 1/15 2008.
13. B. Eom, "Self-aligned carbon nanotubes for field emission tip with simple process," 2006. ID: 1.
14. Y. M. Wong, W. P. Kang, J. L. Davidson, B. K. Choi, W. Hofmeister, and J. H. Huang, "Field emission triode amplifier utilizing aligned carbon nanotubes," *Diamond and Related Materials,*, vol. 14, pp. 2069–2073, 0 2005.
15. P. Avouris, "Carbon nanotube electronics," *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1772–1783, 2003. doi: pmid:.

16. J. J. Brown, J. W. Suk, G. Singh, A. I. Baca, D. A. Dikin, R. S. Ruoff, and V. M. Bright, "Microsystem for nanofiber electromechanical measurements," *Sensors and Actuators A: Physical*, vol. In Press, Corrected Proof, pp. –, 2008.

17. A. Jungen, C. Stampfer, J. Hoetzel, V. M. Bright, and C. Hierold, "Process integration of carbon nanotubes into microelectromechanical systems," *Sensors and Actuators A: Physical,*, vol. 130-131, pp. 588–594, 8/14 2006.

18. C. Hierold, A. Jungen, C. Stampfer, and T. Helbling, "Nano electromechanical sensors based on carbon nanotubes," *Sensors and Actuators A: Physical,*, vol. 136, pp. 51–61, 5/1 2007.

19. M. Jackson, "Crc handbook of chemistry and physics," 2001.

20. R. Boxman, D. Sanders, and P. Martin, *Handbook of Vacuum Arc Science and Technology - Fundamentals and Applications*. William Andrew Publishing/Noyes, 1995.

21. J. Li, W. Lei, X. Zhang, B. Wang, and L. Ba, "Field emission of vertically-aligned carbon nanotube arrays grown on porous silicon substrate," *Solid-State Electronics,*, vol. 48, pp. 2147–2151, 12 2004.

22. Y. M. Wong, W. P. Kang, J. L. Davidson, B. K. Choi, W. Hofmeister, and J. H. Huang, "Array geometry, size and spacing effects on field emission characteristics of aligned carbon nanotubes," *Diamond and Related Materials,*, vol. 14, pp. 2078–2083, 0 2005.

23. Y. Huh, J. Y. Lee, J. H. Lee, T. J. Lee, S. C. Lyu, and C. J. Lee, "Selective growth and field emission of vertically well-aligned carbon nanotubes on hole-patterned silicon substrates," *Chemical Physics Letters,*, vol. 375, pp. 388–392, 7/3 2003.

24. F. Brunetti, "Flip-cathode design for carbon nanotube-based vacuum triodes," *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 111–113, 2008. doi: pmid:.

25. W. J. Yu, Y. S. Cho, G. S. Choi, D. J. Kim, Y. H. Song, and J. H. Lee, "A stable high power carbon nanotube field-emitter device," *Diamond and Related Materials*, vol. 13, pp. 1017–1021, 0 2004.

26. Y. M. Wong, W. P. Kang, J. L. Davidson, B. K. Choi, W. Hofmeister, and J. H. Huang, "Fabrication of aligned convex cnt field emission triode by mpcvd," *Diamond and Related Materials*, vol. 15, pp. 334–340, 0 2006.

27. Y. M. Wong, W. P. Kang, J. L. Davidson, and J. H. Huang, "Carbon nanotubes field emission integrated triode amplifier array," *Diamond and Related Materials*, vol. 15, pp. 1990–1993, 0 2006.

28. L. Wei, X. Zhang, C. Lou, and Z. Zhu, "Influence of charge deposition in a field-emission display panel," *Applied Surface Science,*, vol. 254, pp. 2096–2101, 1/30 2008.

29. C. Harper, *Electronic Materials and Processes Handbook*. McGrawHill, 2005.

30. B. Bayraktaroglu, "How to get more out of nanotechnology," AFRL/RY, 2009.

Index

The index is conceptual and does not designate every occurrence of a keyword. Page numbers in bold represent concept definition or introduction.

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14. ABSTRACT This research studies the growth of carbon nanotubes from a nickel catalyst to be used on a field emission device. A triode structure was created to be able to patterned the CNTs to improve the emission of electrons. Studies are performed on the effects of hydrogen pretreatment on nickel catalyst of different thicknesses and deposition methods on a silicon substrate and how it will affect the growth of carbon nanotubes using microwave plasma enhanced chemical vapor deposition. The treated catalyst granule size and density was determined optically through scanning electron microscope images and atomic force microscope measurements. It was discovered that sputtered catalyst needs a longer pretreatment than evaporated catalyst. As expected, the pretreatment time must be increased as the catalyst thickness increases to get granule sizes and densities favorable for carbon nanotube growth. We also established the size of the catalyst granules correlated to the diameter of the multi walled CNTs grown. We determined the catalyst can be over treated causing catalyst conglomeration that result in poor CNT growth. The CNTs diameter was determined optically through scanning electron microscope images.

15. SUBJECT TERMS

carbon nanotubes, field emission, microwave plasma enhanced chemical vapor deposition

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