

# Switching Requirements for Stacked Blumleins Commutated by Individual Switches

Matthew T. Domonkos

Air Force Research Laboratory, Directed Energy Directorate, 3550 Aberdeen Ave. SE  
Kirtland AFB, NM 87117

**Abstract** - Stacked Blumlein lines with solid dielectric potentially offer a compact pulsed power system for a variety of applications by combining the energy storage, voltage scaling, and pulse forming functions into a single device. By stacking the lines physically, not simply electrically, the line is made more compact because adjacent lines share electrodes. This design does not lend itself to the use of a single switch to commutate the stacked line, and multiple switches are far simpler to implement. The switch jitter and electrical characteristics strongly influence the performance of the line and the stresses on the dielectric. This paper explores the effects of switch jitter, inductance, the resistive decay during closure, and the closed-state resistance on the output pulse and dielectric stresses for stacked Blumlein lines using SPICE simulations. The impact of switch operation on the necessary dielectric strength and the quality of pulse is presented. The suitability of various switch technologies to meet the performance requirements is also discussed.

## I. INTRODUCTION

Rep-rate and compact pulsed power generator design seeks a balance between size, robustness, and pulse quality. Many pulsed power loads are designed for a single operating voltage and operate poorly outside of their nominal envelope. Consequently, laboratory pulsed power systems are typically tuned to deliver a relatively constant voltage over a desired duration [1,2,3]. When attempting to package the pulsed power into a compact form, engineers face the challenges of maintaining the pulse shape, preventing breakdown in the compact architecture, and to a lesser extent, rejecting waste heat in high duty rep-rated systems.

Commercially available power supplies are generally limited to less than 100-kV, and a Marx topology, a pulse transformer, or some combination of both is used to scale the voltage above 100-kV [4]. For compact pulse generators, the Marx topology is more commonly used since it reduces sub-system count by combining the energy storage and power scaling sub-

systems [4,5]. Voltage scaling is an essential function of compact pulsed power systems since the system size is strongly driven by the storage voltage [2]. Modest pulse shaping can be accomplished with Marx banks by the inclusion or reduction of inductance between stages. Typically large rep-rate systems will incorporate a pulse forming line (PFL) to shape the pulse. While PFLs deliver very high quality voltage flat-tops to matched loads, they seldom lend themselves to compact designs. Solid dielectric pulse forming lines have the potential to store pulse energy, and the PFL may also be stacked similarly to a Marx bank to facilitate voltage scaling of the output [4,6]. For common polymer insulators with dielectric constants less than five, the resulting PFL can be quite long.

Advances in solid dielectrics have presented new opportunities to exploit the attractive features of solid pulse forming lines [7]. While there are many variants on the Blumlein even within the general categories of coaxial and planar, a planar geometry consisting of alternating layers of electrodes and dielectric, hereafter a vertically stacked Blumlein (VSB), has some desirable packaging features relative to other designs. The price for the simplified packaging is that each stage of a stacked Blumlein must be switched independently.

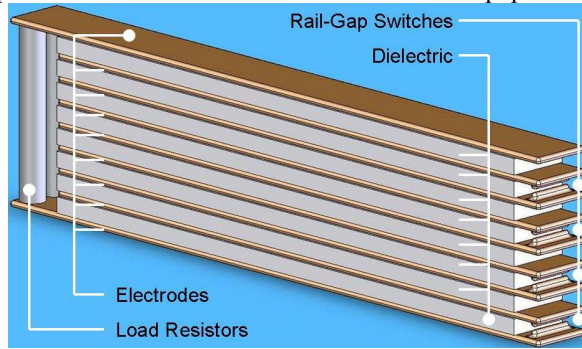
This paper describes switching of vertically stacked Blumleins. The general ways in which switch jitter, inductance, and resistive decay affect the operation of the Blumlein is discussed. SPICE circuit simulations are presented to better describe the impact of realistic switches on the output from a Blumlein. Next, the impact of non-ideal switching on the performance and lifetime of a vertically stacked Blumlein is addressed. A brief discussion of the switch technologies appropriate for this type of Blumlein is included. Finally, the major conclusions of this paper are summarized.

## II. EFFECTS ON BLUMLEIN OPERATION

A vertically stacked Blumlein consists of planar transmission line elements arranged so that adjacent stages share an electrode, as shown in Figure 1. Depending on the dielectric and the length of the line, the relevant pulse lengths range from a few ns to a few

| Report Documentation Page                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                    |                                     |                                         | Form Approved<br>OMB No. 0704-0188       |                                 |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-------------------------------------|-----------------------------------------|------------------------------------------|---------------------------------|
| Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number. |                                    |                                     |                                         |                                          |                                 |
| 1. REPORT DATE<br><b>01 MAY 2006</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                    | 2. REPORT TYPE<br><b>N/A</b>        |                                         | 3. DATES COVERED<br><b>-</b>             |                                 |
| 4. TITLE AND SUBTITLE<br><b>Switching Requirements for Stacked Blumleins Commutated by Individual Switches</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                    |                                     |                                         | 5a. CONTRACT NUMBER                      |                                 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                    |                                     |                                         | 5b. GRANT NUMBER                         |                                 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                    |                                     |                                         | 5c. PROGRAM ELEMENT NUMBER               |                                 |
| 6. AUTHOR(S)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                    |                                     |                                         | 5d. PROJECT NUMBER                       |                                 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                    |                                     |                                         | 5e. TASK NUMBER                          |                                 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                    |                                     |                                         | 5f. WORK UNIT NUMBER                     |                                 |
| 7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)<br><b>Air Force Research Laboratory, Directed Energy Directorate, 3550 Aberdeen Ave. SE Kirtland AFB, NM 87117</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                    |                                     |                                         | 8. PERFORMING ORGANIZATION REPORT NUMBER |                                 |
| 9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                    |                                     |                                         | 10. SPONSOR/MONITOR'S ACRONYM(S)         |                                 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                    |                                     |                                         | 11. SPONSOR/MONITOR'S REPORT NUMBER(S)   |                                 |
| 12. DISTRIBUTION/AVAILABILITY STATEMENT<br><b>Approved for public release, distribution unlimited</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                    |                                     |                                         |                                          |                                 |
| 13. SUPPLEMENTARY NOTES<br><b>See also ADM001963. IEEE International Power Modulator Symposium (27th) and High-Voltage Workshop Held in Washington, DC on May 14-18, 2006, The original document contains color images.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                    |                                     |                                         |                                          |                                 |
| 14. ABSTRACT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                    |                                     |                                         |                                          |                                 |
| 15. SUBJECT TERMS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                    |                                     |                                         |                                          |                                 |
| 16. SECURITY CLASSIFICATION OF:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                    |                                     | 17. LIMITATION OF ABSTRACT<br><b>UU</b> | 18. NUMBER OF PAGES<br><b>4</b>          | 19a. NAME OF RESPONSIBLE PERSON |
| a. REPORT<br><b>unclassified</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | b. ABSTRACT<br><b>unclassified</b> | c. THIS PAGE<br><b>unclassified</b> |                                         |                                          |                                 |

hundred ns for compact systems. The center electrode of each stage is charged to  $V_{CH}$ , and each stage is commutated by a switch. The switch closure sends a wave,  $-V_{CH}$  in magnitude, down half of a stage toward the load. When the wave reaches the load at time  $t=\tau$  ( $\tau$  is the transit time), it is partially reflected and transmitted to the load and the other lines. The result is waves traveling along all the lines back toward the switch end of the line. The waves seeing the short circuit of a closed switch are inverted when they are reflected, while those seeing the open circuit are merely reflected. At time  $t=3\tau$ , the waves arrive at the load again and cancel if the line is perfectly matched. Stacked Blumlein operation with ideal switches and a matched resistive load delivers a square voltage flat-top with a magnitude equal to the number of stages times the charge voltage and a duration of  $2\tau$ . In reality, the switches will have jitter, inductance, a finite rate of commutation, and some residual resistance when closed. Loads of interest generally include inductance, capacitance, and non-linear behavior, however, peculiarities of the load are not treated in this paper.



**Figure 1** - Schematic Illustration of a Four-Stage Vertically Stacked Blumlein with Notional Rail-Gap Switches and Load Resistors

The vertically stacked Blumlein levies several requirements on the switch operation: 1) the triggering jitter between the switches should be small, 2) the inductance should be small compared to the stage inductance, 3) the resistive decay time should be small compared to the pulse length, and 4) the closed-state resistance should be small compared to the stage impedance. The switch-to-switch trigger jitter must be small compared to the pulse length to preserve most of the performance of the line. Additionally, the switch-to-switch trigger jitter must be small compared to the time required to breakdown the dielectric at expected field stresses induced by the jitter. Inductance in the switch causes the output voltage to be rounded off, reducing the quality of the flat-top. Both the resistive decay time and the closed-state resistance decrease the performance of the line by slowing the voltage rise across the load and consuming some of the stored energy. The effects

of switch performance on Blumlein operation are elaborated below.

Switch trigger jitter alters both the output voltage and the stresses on the dielectric in the line. Jitter results in temporally staggered wave fronts in the lines. Only when all of the waves have reached the load will the output voltage stack to the desired value of  $n \cdot V_{CH}$  where  $n$  is the number of stages. Consequently, the duration of the voltage flat-top is reduced by the spread in the switch trigger times. The switch trigger jitter also leads to over-voltage conditions on the dielectric. Given that a goal of compact pulsed power design is to minimize insulation margins, switch jitter adversely impacts system size. Figure 2 shows the normalized voltage within a four-stage stacked Blumlein. The voltage is normalized to the charge voltage, and the time is normalized to the one-way transit time for the line. The switching for each of the four lines is separated temporally, causing mismatches in the lines, and hence, undesirable voltage excursions at the load end. The line whose switch triggers last experiences the greatest voltage extremes. As the waves initially approach the load end of the line, the last line to trigger experiences a voltage of

$$V_{\tau} = \left(1 + \frac{n-1}{2n}\right) V_{CH} \quad 1$$

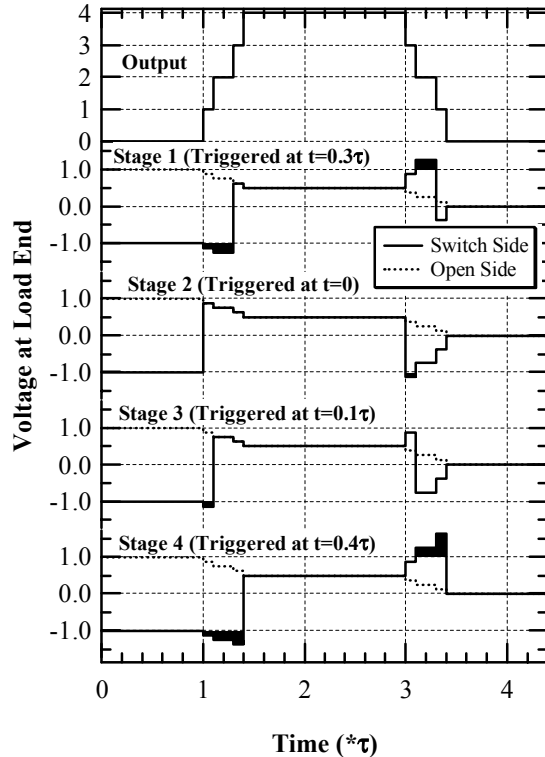
Similarly, after the waves complete their roundtrip to the switch end of the line, the line whose switch triggered last experiences a voltage of

$$V_{3\tau} = -\left(\frac{1}{2} + \frac{3(n-1)}{2n}\right) V_{CH} \quad 2$$

The resulting upper and lower limits of voltage experienced by a stage are plotted in Figure 3. For purely resistive loads, reduction of the number of stages helps to minimize the margin of dielectric strength required. While the reflected and transmitted waves will continue to transit the line in the lossless case considered here, realistic losses will dampen the transients associated with those waves. Consequently, late-time transients are not considered here.

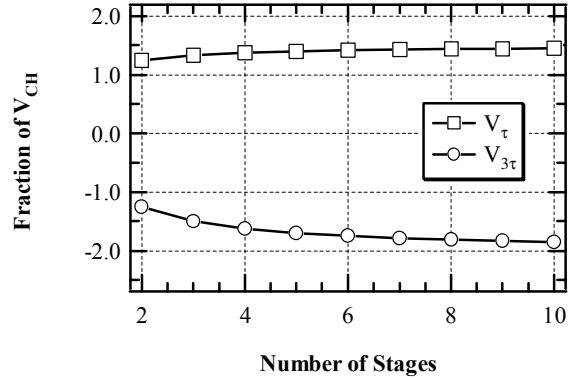
In order to evaluate the effects of inductance and resistance in the switch, SPICE simulations were employed. A two-stage model is depicted in Figure 4. An inductor is shown in series with the switch, while the closed-state resistance is imbedded in the switch model. The simulations presented in this paper all consider a four-stage line. The inductance in common pulsed power switches can be limited to a few tens of nH. As a rough design guide, the switch inductance should be small compared to the stage inductance. The stage inductance,  $L_{st}$ , is plotted as a function of transit time for several values of stage impedance,  $Z/2n$ , in Figure 5. For most switch options, its inductance will influence the pulse shape significantly for lines with

transit times below 50 ns and low stage impedance. The effect of the switch inductance on the output pulse is depicted in Figure 6. The voltage ramp is damped and the flat-top duration is reduced. The effects of switch inductance on the output, similar to switch trigger jitter, also drive the design of vertically stacked Blumleins toward minimization of the number of stages, in this case primarily to preserve output quality. One unintended benefit of switch inductance is that it will dampen the severity of the voltage transients induced by the switch trigger jitter, thereby protecting the dielectric.

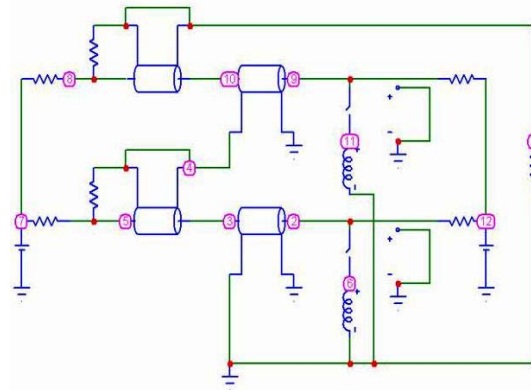


**Figure 2 - Four Stage Stacked Blumlein Response with Specified Switch Trigger Jitter (Shaded Regions Indicate Voltage Excursions Beyond the Charge Voltage)**

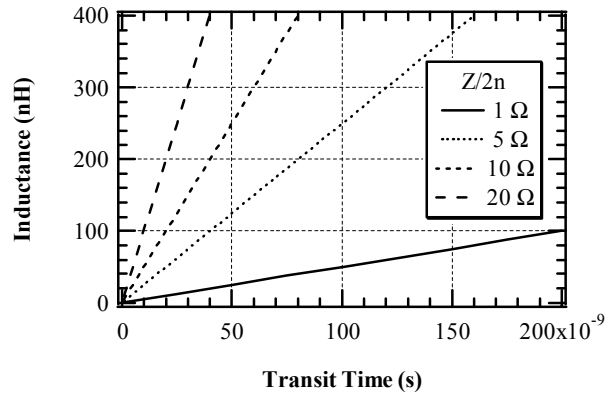
The resistive decay during commutation of the switches and the closed-state resistance of the switches both reduce the quality of the output voltage pulse. The resistive decay serves to decrease the slope of the wave front launched by the switch commutation. This effect is similar to the inductance in the switch, and can be minimized by ensuring that the commutation time is much less than the transit time of the line. The closed-state resistance of most switches is already much less than that of a Blumlein stage. Consequently, the primary impact of the switch closed-state resistance is to reduce the output voltage. The design goal is to ensure that the switches consume a small fraction of the stored energy.



**Figure 3 - Maximum Voltages Experienced within the Stacked Blumlein with Individually Commutated Switches as a Function of the Number of Stages**



**Figure 4 - SPICE Model of a Two-Stage Blumlein**



**Figure 5 - Line Inductance Dependence on Transit Time and Line Impedance (Switch Inductance Is Especially Critical for sub-50 ns Transit Times)**

### III. CONSEQUENCES FOR BLUMLEIN LIFE

Solid dielectric failure is dependent upon the electric field and weakly dependent upon the volume [8]. Both dependencies are statistical. Additionally, the DC breakdown strength of dielectrics is generally less than that under pulse conditions. Consequently, the charge rate for the Blumlein must be considered when determining the dielectric strength margins. Provided the DC strength is within a few percent of the pulsed

strength, examination of Figure 3 reveals that the stresses applied during the discharge of a vertically stacked Blumlein drive the design of the insulation.

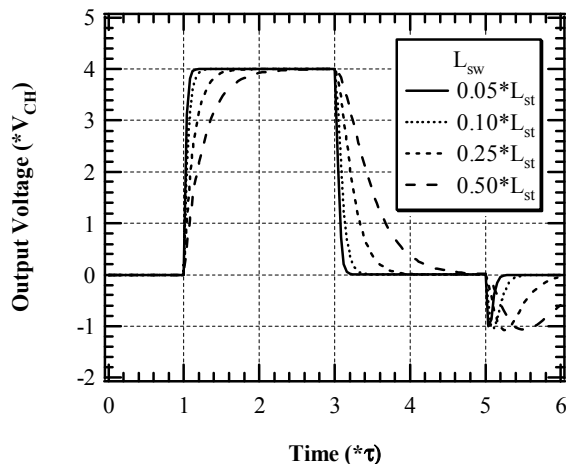


Figure 6 - Effect of Switch Inductance on the Quality of the Output Voltage Pulse

Defects, contaminants or voids, in large scale dielectrics, are largely responsible for the volume dependence of the effective dielectric strength. The volume of dielectric in a Blumlein is a function of both energy storage and insulating margin. Consequently the dielectric volume is independent of the number of stages. The volume effect of the dielectric strength may be mitigated while decreasing the line length by the use of a polymer-ceramic composite. The polymer matrix helps to minimize voids, and nano-scale ceramic particles give the material a relatively high dielectric constant while also minimizing the size of any voids in the material.

In order to calculate the shot life of a Blumlein based on dielectric failure, a detailed circuit simulation must be combined with a prediction of the field concentration points within the line and a model or empirical database of the dielectric strength. The calculation must be probabilistic in order to capture the statistical nature of the dielectric breakdown and the switch operation.

#### IV. SUITABLE SWITCH TECHNOLOGIES

Gas gap switches have long been the choice for pulsed power applications, and their ability to commutate within a few ns or quicker makes them well suited for vertically stacked Blumleins. Care must be exercised in minimizing the switch jitter, though electrically and optically triggered switches have demonstrated jitter of less than 2 ns [9]. Minimization of the inductance in gas gap switches can be accomplished through high pressure operation with small gaps or the use of rail electrodes. Rail-gap switches generally require currents exceeding tens of kA or exotic gas mixtures in order to generate a low inductance multi-

channel discharge. Gas mixtures usually contain a gas that emits strongly in the ultraviolet to promote photoionization. Jitter can be minimized with gas mixtures if adjacent switches can illuminate each other, capitalizing on photoionization. Switch jitter also scales inversely with the charge rate.

Several solid-state switch technologies are also suitable for Blumlein operation in various regimes and offer very low jitter and long life operation. Photoconductive solid state switches (Si, GaAs) are suitable for applications up to a few ns. Longer duration pulses may be compatible with MOSFETs or IGBTs provided the stage voltage is a few kV at most. Several optically triggered semiconductor technologies currently in development may be suitable for long pulse operation above 10 kV per stage [10].

#### V. CONCLUSIONS

The impact of switch performance on the operation of vertically stacked Blumleins was examined. Switch trigger was found to have the most severe impact on the output quality and the necessary insulation margin in the line. Switch inductance was identified as a critical design issue for lines with transit times of less than 50 ns. Blumlein performance and lifetime considerations were discussed along with suitable switch technologies.

#### REFERENCES

- [1] T. C. Grabowski, C. W. Gregg, D. Trujillo, *et al.*, "Refurbishment of the ETDL Rep-Rate Pulse Generator at AFRL," Proc. from the 15th IEEE International Pulsed Power Conf., Monterey, CA, 2005.
- [2] M. Buttram, "Some Future Directions for Repetitive Pulsed Power," *IEEE Transactions on Plasma Science*, Vol. 30, No. 1, Feb. 2002, pp. 262-266.
- [3] J. A. Casey, F. O. Arntz, M. P. J. Gaudreau, M. A. Kempkes, "Solid-State Marx Bank Modulator for the Next Linear Collider," *2004 IEEE International Power Modulator Conference*.
- [4] W. C. Nunnally, "Critical Component Requirements for Compact Pulse Power System Architectures," *2004 IEEE International Power Modulator Conference*.
- [5] J. R. Mayes, M. G. Mayes, and M. B. Lara, "A Compact MV Marx Generator," *2004 IEEE International Power Modulator Conference*.
- [6] F. Davanloo, J. L. Koriath, D. L. Borovina, R. K. Krause, *et al.*, "Stacked Blumlein Pulse Generators," *1996 IEEE Power Modulator Conference*.
- [7] M. T. Domonkos, P. J. Turchi, J. V. Parker, T. C. Grabowski, C. W. Gregg, C. E. Roth, and K. Slenes, "A Ceramic Loaded Polymer Blumlein Pulser for Compact, Rep-Rated Pulsed Power Applications," Proc. from the 15th IEEE International Pulsed Power Conf., Monterey, CA, 2005.
- [8] J. C. Martin, *J. C. Martin on Pulsed Power*, T. H. Martin, A. H. Guenther, and M. Kristiansen, Ed., Plenum Press, New York, 1996.
- [9] J. Alexander, Sandia National Laboratories, Albuquerque, NM, private communication, Feb. 2006.
- [10] D. M. Weidenheimer and D. Giorgi, "Technological Breakthroughs in Light-Activated Thyristors for Pulsed Power," *2004 IEEE International Power Modulator Conference*.