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14. ABSTRACT

We report large-seale integration of nanowires for heterogeneous, multi-funetional eireuitry that utilizes both the sensory and eleetronic funetionalities of single erystalline nanomaterials. Highly ordered and parallel arrays of optieally aetive CdSe nanowires and high mobility Ge/Si nanowires are deterministieally positioned on substrates, and eonfigured as photodiodes and transistors, respectively. The nanowire sensors and eleetronie deviees are then interfaeed to enablc an all-nanowire eireuitry with on-ehip integration, eapable of deteeting and amplifying an optieal signal with high sensitivity and preeision. Notably, the proeess is highly reproducible and sealable with a yield of ~80% funetional eireuits, therefore, enabling the fabrieation of large arrays (i.e., 13x20) of nanowire photosensor eireuitry with image sensing funetionality. The ability to interfaee nanowire sensors with integrated eleetronics on large seales and with high uniformity presents an important advanee toward the integration of nanomaterials for sensor applieations.

15. SUBJECT TERMS

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a. REPORT	b. ABSTRACT	c. THIS PAGE			Ali Javey
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All Nanowire Integrated Sensor Circuitry

Final Report
Reporting Period: 10/16/07 – 04/28/08

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Problem statement and objective

Semiconductor nanowires (NWs) are an exciting class of new materials that have recently received significant attention due to their unique chemical, physical, and electrical properties, and have been proposed as the building blocks for various technological applications. For example, they are ideal materials for sensor applications with high sensitivity to the environment due to their miniaturized dimensions and high surface area to volume aspect ratio. Furthermore, they have been shown to exhibit high carrier mobility, and they can be readily assembled on any substrate, making them ideal for various high performance electronic applications. While single devices with sensor or transistor functionality have been demonstrated based on nanowires, to this day, an integrated circuit that combines and incorporates the two functional elements together for an all nanowire circuit has not yet been demonstrated. Exploring and successfully demonstrating such an integrated circuit is essential for further progress of the field and potential large scale integration of nanowire materials in high performance electronics. The purpose of this project was to integrate nanowire-based light sensors with NW-FETs on a single chip for electrical detection and amplification of a white light signal using an all nanowire circuitry, taking advantage of our recently developed nanowire printing technology for large-scale assembly of parallel arrays of nanowires at well defined locations on the substrates and with high uniformity.

Results and achievements

We were able to successfully demonstrate the exact replica of the proposed all-integrated nanowire sensor arrays with high yield and uniformity, capable of proof of concept imaging capability. This is the first time that an all-integrated circuitry utilizing both the sensor and transistor functionalities of nanowires has been experimentally demonstrate and this work may pave the way for the development of a wide range of technological applications, for instance sensor tapes, with profound interest to the military and battle-field surveillance.

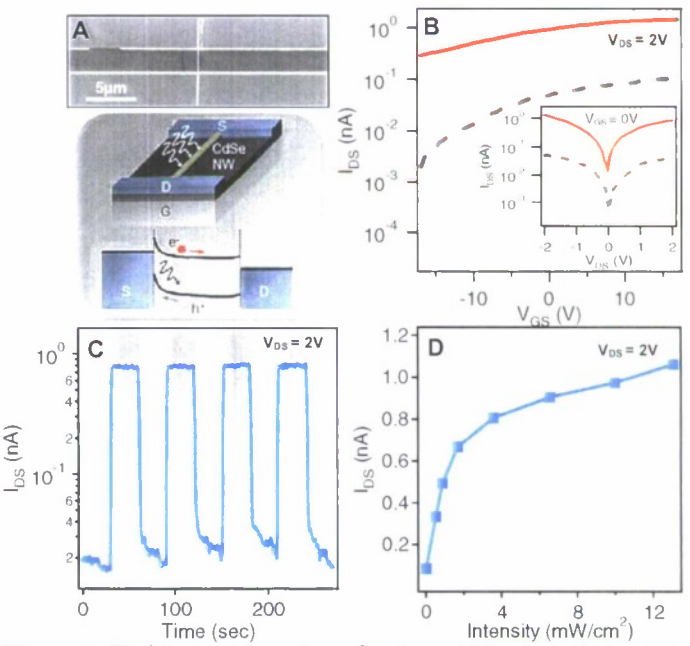


Figure 1. Highly sensitive, direct band-gap NW photodiodes. (A) SEM (top), schematic (middle), and the band diagram (bottom) of a CdSe NW photodetector with Ni/Pd Schottky S/D contacts. (B) I_{DS}-V_{GS} and I_{DS}-V_{DS} (inset) curves of a representative CdSe NW device before (dashed, gray line) and after (solid, red line) white light illumination, exhibiting ~100x current modulation. (C) Transient of a single CdSe NW device with an illumination intensity of 4.4mW/cm^2. (D) Illumination intensity dependent measurements of a CdSe NW device, showing a nonlinear behavior.

In this work, direct band gap CdSe NWs were used as a model system for the optical sensor elements, capable of detecting visible light with high sensitivity. To implement CdSe NWs as optical sensors, Schottky devices were fabricated by contacting the NWs with high work function Ni/Pd (5/45 nm) source (S) and drain (D) electrodes (Fig. 1A). NWs were grown intrinsically without any intentional doping using the previously reported vapor-liquid-solid process, and as expected they exhibited *n*-type behavior (Fig. 1B) due to their surface Fermi level pinning. From photoluminescence measurements, a band gap of ~1.76eV was extracted, which is consistent with the reported bulk value, and is indicative of stoichiometric composition. The electrical characteristic of a representative CdSe NW Schottky device is shown in Fig. 1B. The device exhibits large dark resistance R_{dark}~140GΩ due to the Schottky barriers at the S/D interfaces that severely limit the carrier injection from the metal into the chemically intrinsic

semiconductor NWs. Upon white light illumination (halogen light source, 4.4 mW/cm^2), a drastic decrease of ~100x in the device resistance (R_{light}~2GΩ) is observed which is attributed to the efficient electron/hole photogeneration and field-induced carrier separation in CdSe NWs (Fig 1A).

To further characterize the CdSe NW photosensors, transient and illumination intensity dependent measurements were performed. Time resolved photo-response measurements were conducted for multiple illumination cycles as depicted in Fig. 1C. Each photo-response cycle consists of three transient regimes – a sharp rise (τ~0.7 sec), steady state and sharp decay (τ~0.7 sec). Importantly, a nearly identical response is observed for multiple cycles which demonstrates the robustness and reproducibility of the NW optical sensors. The illumination power dependence of the photoresponse is shown in Fig. 1D, exhibiting two distinct regimes with the transition intensity of ~2mW/cm^2. This nonlinear photoresponse has also been previously reported in other NW photodetectors, and has been attributed to the charge-trapping and recombination processes due to the dominant surface states in the forbidden gap of NWs.

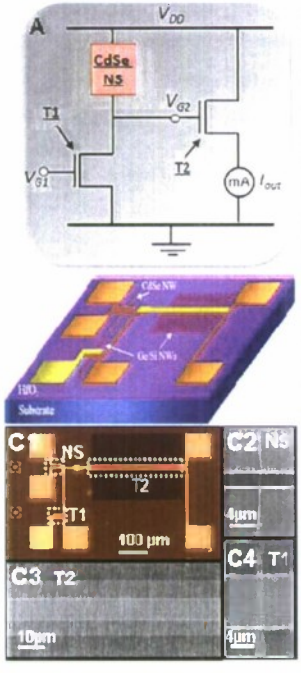


Figure 2. Heterogeneous NW assembly for an all integrated, sensor circuitry. (A) Circuit diagram for the all-nanowire photodetector, with high mobility Ge/Si NW FETs (T1 and T2) amplifying the photoresponse of a CdSe nanosensor. (B) Schematic of the all-nanowire optical sensor circuit based on ordered arrays of Ge/Si and CdSe NWs. (C1) An optical image of the fabricated NW circuitry, consisting of a CdSe nanosensor [NS, (C2)] and two Ge/Si core/shell NW FETs [T2 and T1, (C3)-(C4)] with channel widths ~300 μm and 1 μm, respectively. Each device element within the circuit can be independently addressed for dynamics studies and circuit debugging.

While the miniaturized nanosensor elements, such as the CdSe NW photodetectors shown here, provide high sensitivity to the environment with high spatial resolution, they are inherently limited to low signal amplitude (i.e., current), and therefore require an eventual signal amplification via electronic circuitry to enable effective data processing. To date, this important requirement has not yet been addressed. Here, we report direct, on-chip amplification of the nanosensor signal using an all NW circuitry without any external wiring. The schematic, SEM and optical images of a fabricated all-nanowire circuit is shown in Fig. 2, consisting of three active device elements – (i) optical nanosensors (NS) based on either a single or parallel arrays of multiple CdSe NWs, (ii) a high resistance FET (T1) based on parallel arrays of 1-5 Ge/Si core/shell NWs, and (iii) a low resistance buffer FET (T2) with the channel consisting of parallel arrays of ~2000 NWs. The all-nanowire circuitry utilizes T1 to match the output impedance of the NS in a voltage divider configuration. Once the illumination-dependent NS current is translated into potential V_{G2}, the output current of T2 is modulated according to its transfer characteristics, resulting in ~5 orders of magnitude amplification of the NS current signal.

To enable the successful fabrication of the all-integrated, heterogeneous NW circuitry, it is essential to assemble highly regular NW arrays with high uniformity at well defined locations on the substrate. Recently, we have developed a contact printing technology for direct transfer of highly ordered and aligned NW arrays on various receiver substrates with high reproducibility over large areas. In this approach, a dense "lawn" of single crystalline NWs with controlled composition is first grown on a growth substrate using the vapor-liquid-solid process, followed by the transfer of NWs to a receiver substrate by a directional sliding. Prior to the printing process, the receiver substrate is coated with a photolithographically patterned resist layer which enables for patterned NW assembly upon resist removal in acetone. We incorporated this assembly approach for enabling the fabrication of the all-nanowire sensor circuitry. First, highly aligned CdSe and Ge/Si NW arrays were assembled at pre-defined locations on a Si/SiO_2 (50 nm, thermally grown) substrate using a two-step printing process. Ni/Pd S/D electrodes were then patterned on NW arrays followed by atomic layer deposition (ALD) of 8-9nm thick HfO_2 film as the high-κ gate diclectric. Finally, the HfO_2

layer was selectively etched in hydrofluoric acid at the bonding pads and vias, and the top gate electrodes (Ni/Pd) were patterned on Ge/Si NWs while simultaneously forming the vias between the two metal layers. Figure 2C shows an optical microscopy image of a fabricated circuit and scanning electron microscopy (SEM) images of each individual component, clearly demonstrating the highly ordered NW positioning and the on-chip integration. The achieved NW alignment is highly desirable for high performance and highly uniform transistor and sensor arrays.

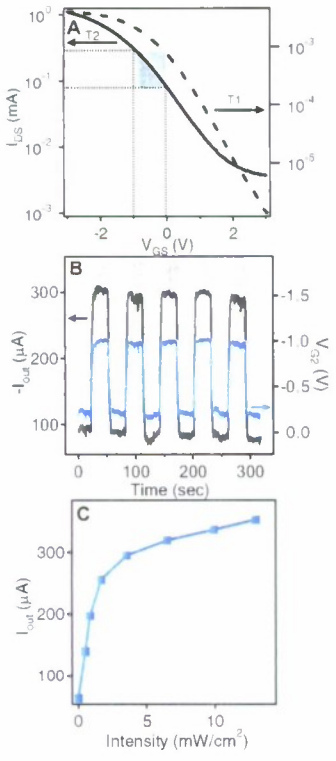


Figure 3. All-integrated NW sensor circuitry. (A) Transfer characteristics of parallel array Ge/Si NW FETs with channel width of ~1μm (dash line, T1) and ~300 μm (solid line, T2) with V_{DS}=3V. The blue box represents the active operation regime in which the photosensor circuit is being operated. (B) Circuit output current (blue curve) and voltage divider output voltage (grey curve) response to light illumination (4.4 mW/cm^2). (C) Light intensity dependent measurement of the circuit output current.

The all-nanowire photosensor circuits were measured at both the single device component and circuit levels in order to characterize their operational performance. Figure 3A shows the transfer characteristics of T1 and T2, both exhibiting clear *p*-type switching characteristics with I_{ON} ~4μA and 1mA, respectively. Ge/Si NW FETs were found nonresponsive to white light illumination which guaranteed no undesired interference. For the circuit level operation, the operating bias, V_{DD} was maintained at -3V for all measurements. The gate electrode for T1 was biased at V_{G1} = 3V (corresponding to R_{T1} =1-2GΩ) in order to match the output impedance of the CdSe NS. The output signal of a circuit for multiple white light illumination cycles (4.4mW/cm^2) is depicted in Fig. 3B, showing an average dark and light currents of ~80μA and ~300μA, respectively. Importantly, this output current is quantitatively consistent with the value that is estimated based on the circuit layout and the electrical properties of the single device components. The output current of the circuit can be estimated from the transfer characteristics of T2 and the output voltage of the voltage divider, which is also the input to T2. The output of the voltage divider, V_{G2} can be estimated as

$$V_{G2} = V_{DD} \times \frac{R_{T1}}{R_{T1+}R_{NS}}$$

, corresponding to V_{G2}~ -0.02V and -1.11V for dark and light ($R_{NS\text{-}dark}$~140 GΩ and $R_{NS\text{-}light}$~2 GΩ, Fig. 1B) scenarios, respectively, which is in good agreement with the measurements (blue curve, Fig. 3B). The V_{G2} swing defines the operation regime of T2 as depicted in the transfer characteristics (Fig. 3A). This operation regime corresponds to an output current swing of 87-310μA, consistent with the measured values and the PSpice modeling.

To further demonstrate the versatility of our approach, we fabricated large arrays (i.e. 13x20) of the all-nanowire circuits on a chip (Fig. 4A), and measured the photoresponse of each individual circuit element. It was found that ~80% of the circuits demonstrated successful photoresponse operation as depicted in the failure analysis map (Fig. 4B). The functional circuits exhibited a mean photocurrent of ~420 μA with a standard deviation of ±165 μA. The reasonably small circuit to circuit variation arises from the uniformity of the assembled nanowire arrays. The three major causes for circuit failure were (i) fabrication defects (i.e., poor metal lift-off and gate dielectric breakdown), (ii) failed CdSe printing, and (iii) weak photoresponse from CdSe NWs (i.e., defective NWs) which represent ~10%, 5% and 5% of the fabricated circuits accordingly. The high yield of the operational circuits with high level of complexity proves the potential of the NW technology and our parallel array assembly approach for large-scale sensor and electronic

integration. In future, this yield can be further enhanced through NW synthesis and fabrication processing optimization.

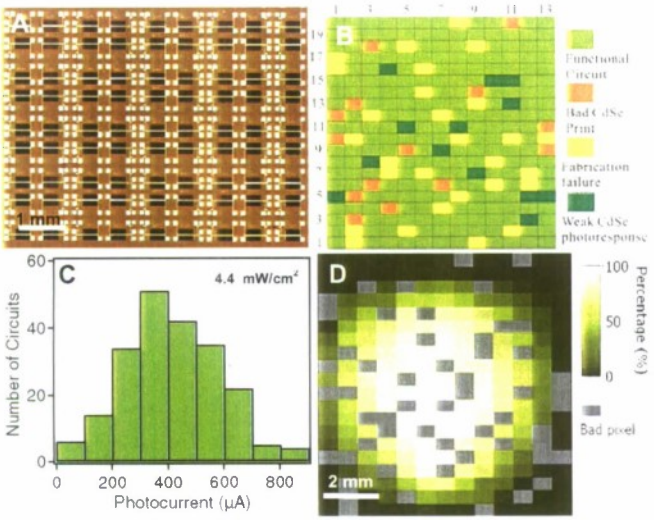


Figure 4. Large-scale and heterogeneous integration of NWs for image sensing. (A) Optical image of an array of all-nanowire photodetector circuitry with each circuit element serving as an independently addressable pixel. (B) A defect analysis map showing the functional and defective NW photodetector circuit elements. (C) A histogram of the photocurrent for all functional circuit elements of the fabricated array. (D) An output response of the circuit array, imaging a circular light spot. The contrast represents the normalized photocurrent, with the gray pixels representing the defective sites.

The large NW circuit matrix can readily function as an image sensor. To demonstrate this feasibility, as a proof of concept, a halogen light source was focused and projected onto the center of the matrix. The output current was measured for each individual working circuit and digitized into a 0-100 scale with "0" and "100" representing the maximum and minimum measured intensity, respectively. Each of the circuits was regarded as a pixel and the measured intensity levels of the circuits were incorporated into a 2-D plot to generate a contrast map shown in Fig. 4D. The contrast map clearly demonstrates the spatial intensity variation from the center to the outer edge of the circuit matrix, precisely matching the intensity profile of the projected light source, thus showing a preliminary imaging function with an all-nanowire circuit array. In future, significant down-scaling of the pixel size can be achieved by reducing the feature size (for instance, channel length and width) of the Ge/Si NW FETs and the metal interconnects.

In summary, the large-scale assembly of NWs for heterogeneous, sensor circuitry with on-chip integration was demonstrated. For the first time, the sensory and electronic functionalities of NWs have been interfaced through heterogeneous integration of direct band gap CdSe NWs and high mobility Ge/Si NWs. Active elements consisting of both single and parallel arrays of NWs were incorporated to enable the circuit operation, involving 5 orders of magnitude current amplification of the nanosensors' signal. Importantly, by using parallel arrays of NWs as the active component of each device, the reliability and uniformity was significantly enhanced, therefore, enabling a reliable large-scale integration path for the demonstration of an image sensor. In the future, the process can be expanded to other optically-active NWs, which combined with the scaling of the fabricated devices may enable high resolution, and multi-color imaging. This work not only demonstrates the nanowire device integration at an unprecedented scale, but also illustrates and presents a novel system based on printed NW arrays that may enable a number of technological applications utilizing NWs as the building blocks.

Future work:

Our main objective is to develop a versatile fabrication technology for printable sensor tapes that can be utilized for real-time battle-field survallience needed in today's urban warfare. To achieve such sensor tapes, 4 main modules need to be developed: sensor, electronics, wireless component, and battery/energy source. To date, we have addressed the first two needs. The next step is to develop the wireless and energy components based on printed nanowire arrays to be incorporated with the nanowire sensor circuitry. Our group is currently exploring novel routes for addressing these needs and developing a fully integrated sensor tapes based on crystalline nanowires.

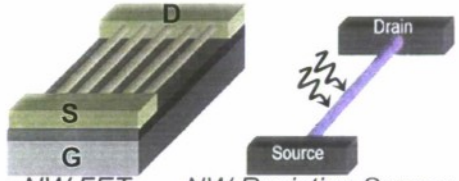
Publications resulted from this seedling

- Z. Fan, J. C. Ho, Z. A. Jacobson, H. Razavi, A. Javey, "Large Scale, Heterogeneous Integration of Nanowire Arrays for Image Sensor Circuitry", *Proceedings of the Notionol Acodemy of Sciences (PNAS)*, 2008, in press, DOI: 10.1073/pnas.0801994105. This work has been covered by various news agencies, including New Scientist and Science Daily.

All Nanowire Integrated Sensor Circuitry

PI: Ali Javey, Electrical Engineering and Computer Sciences, UC Berkeley

STATUS QUO

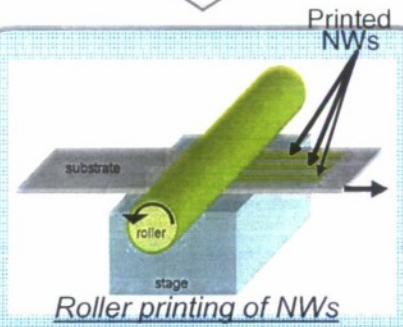


NW FET *NW Resistive Sensor*

Nanowires (NWs) can be configured into individual transistor and sensor devices

- *Large scale integration has not been shown.*
- *No heterogeneous integration for an all nanowire sensor circuit has yet been demonstrated*

NEW INSIGHTS



Roller printing of NWs

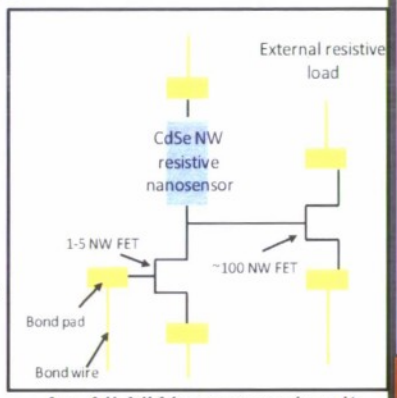
Our newly developed contact printing technology enables large-scale assembly of NWs with high uniformity

Heterogeneous integration can be achieved by printing various types of NW materials on substrates

ACHIEVEMENT

MAIN ACHIEVEMENT:

Demonstrate the first all nanowire sensor circuitry where various nanowire device configurations are integrated together in order to enable a new functionality. As a proof of concept, we will build a nanowire optical sensor.



An All NW sensor circuit

HOW IT WORKS:

A CdSe nanowire resistive nanosensor acts as an optical sensor element. The signal from this device is amplified by using an all nanowire circuitry that incorporates a single NW FET and a parallel array multi-NW FET.

QUANTITATIVE IMPACT

Developing a completely new technology for printable , high performance, multi-functional, and heterogeneous nano-enabled circuitry.

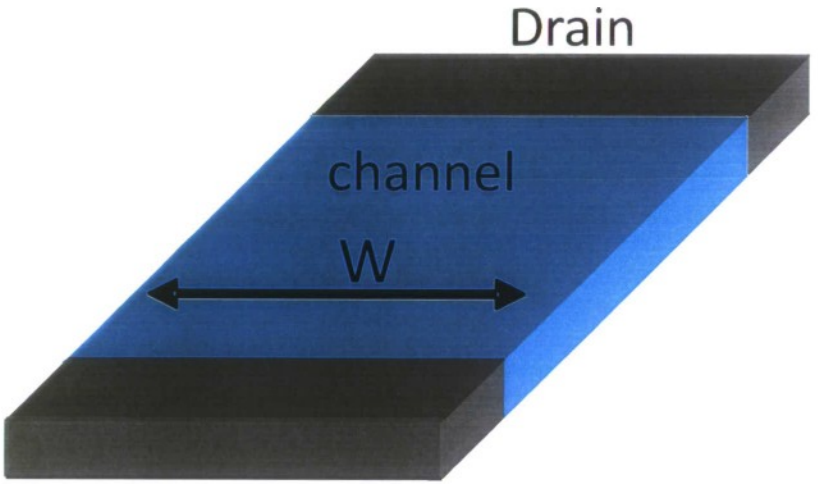
The strategies developed in this project can lead the way to large-scale integration of nanowires for electronics.

END-OF-PHASE GOAL

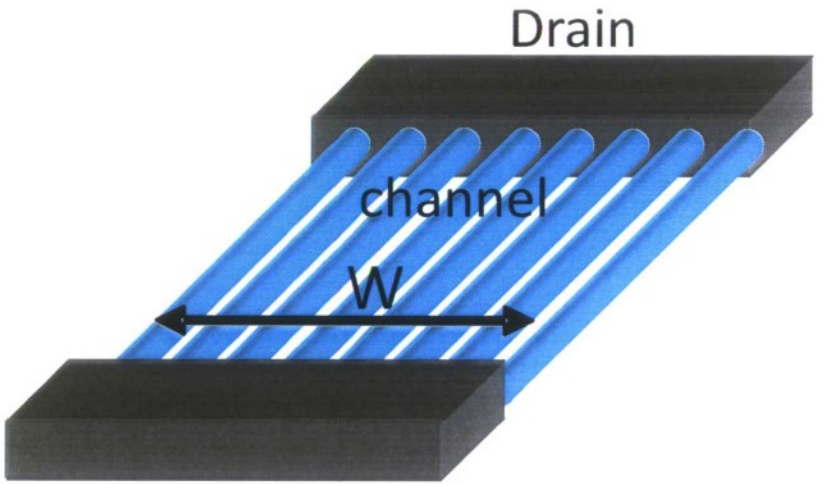
- Integrate two different types of nanowire materials for multi-functional operation on a single chip-5-6 m.
- Demonstration of nanowire sensor circuit– 5-6 mo.
- Technical report describing the design and performance of an all nanowire sensor circuit

This project can lead the way to the large-integration of nanowires for various electronic applications.

Parallel Array Assembly of NWs for Electronics and Sensors



Planar Device

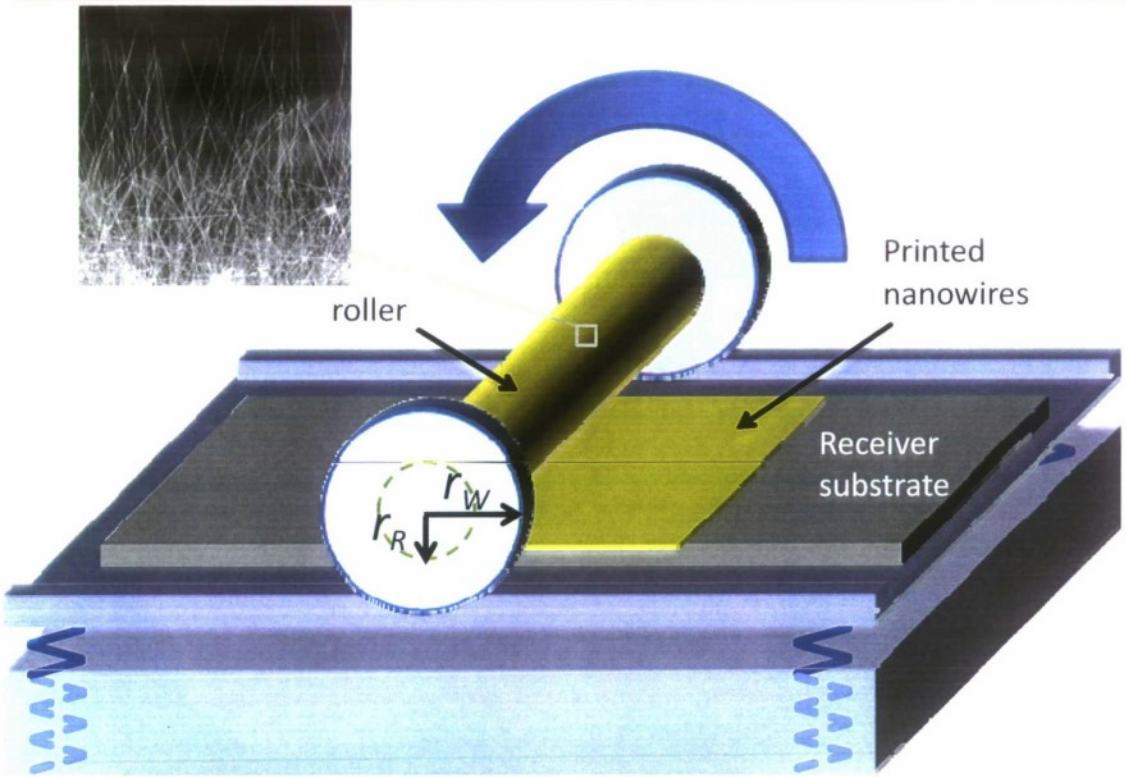


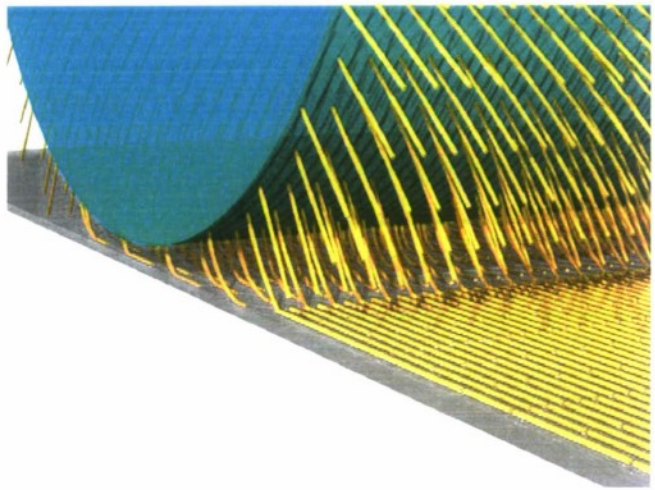
Parallel Array NW Device

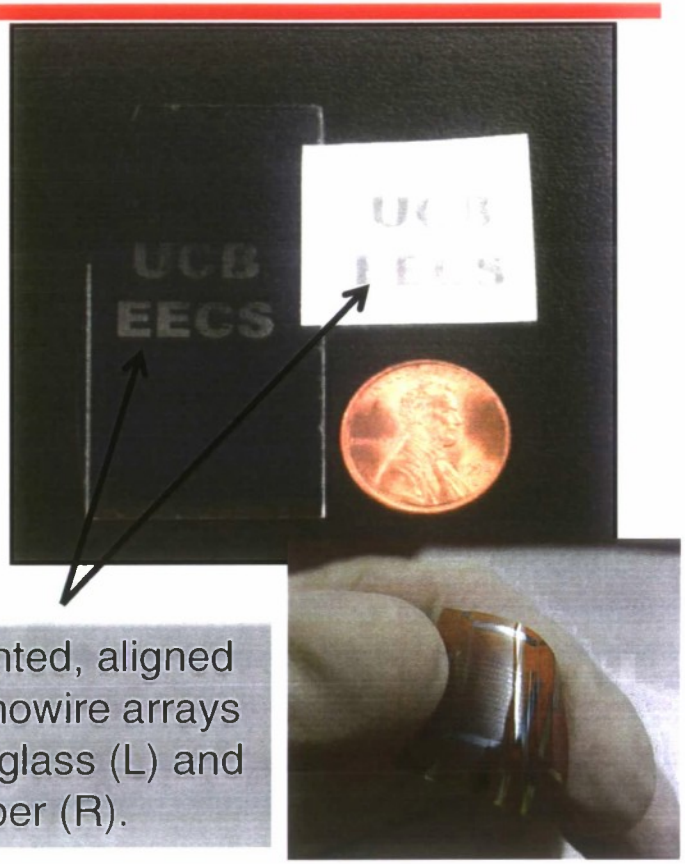
Nanowire Assembly Requirements:

- -Well Aligned
- -Tunable Density
- -Clean
- -Scalable

Roll Printing of NWs







Printed, aligned nanowire arrays on glass (L) and paper (R).

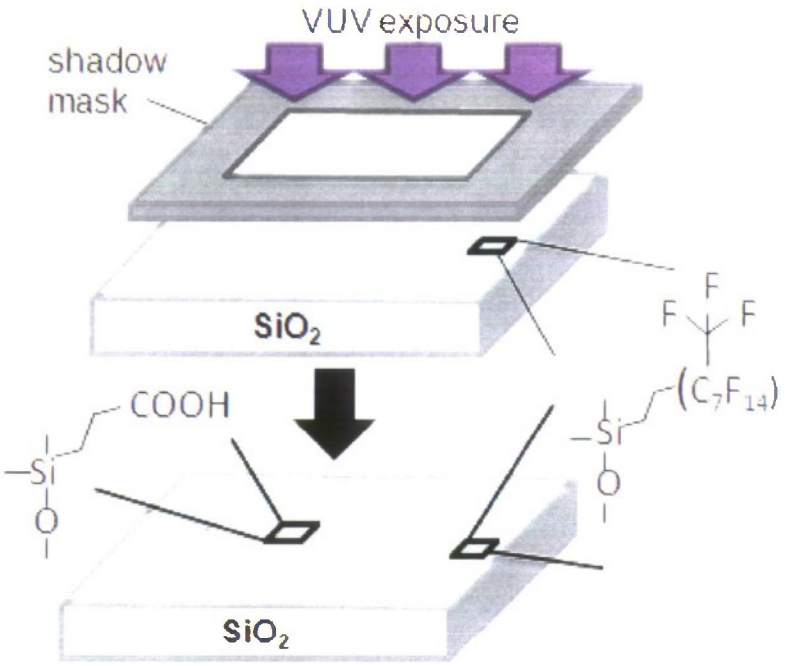
❖Nanowires are first grown on a roller and are then transferred to the desired receiver substrate by a roll printing process. The transferred nanowires are aligned in the direction of rolling.

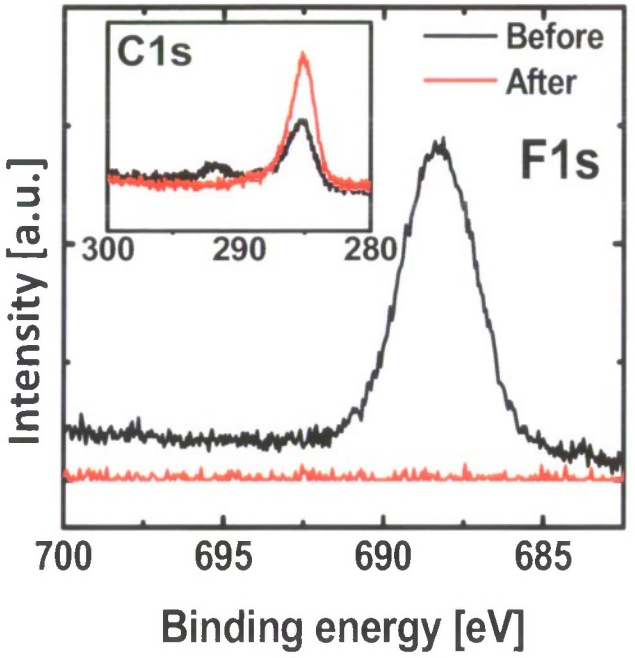
❖A shear motion is applied in conjunction with the rolling motion.

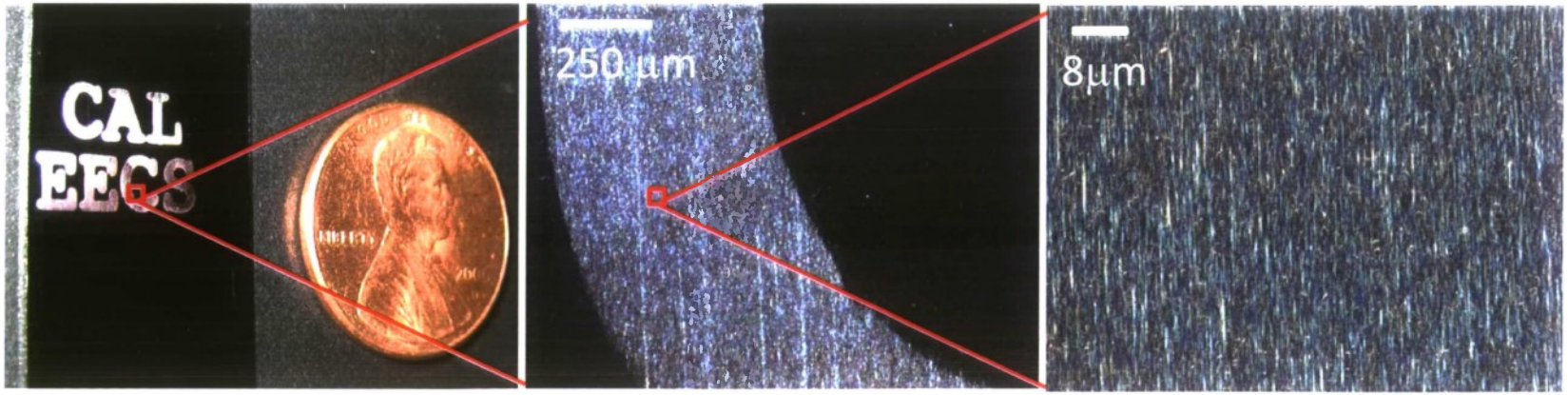
❖Applicable for a wide range of NW materials.

Yerushalmi, et al. Applied Physics Letters, 2007.

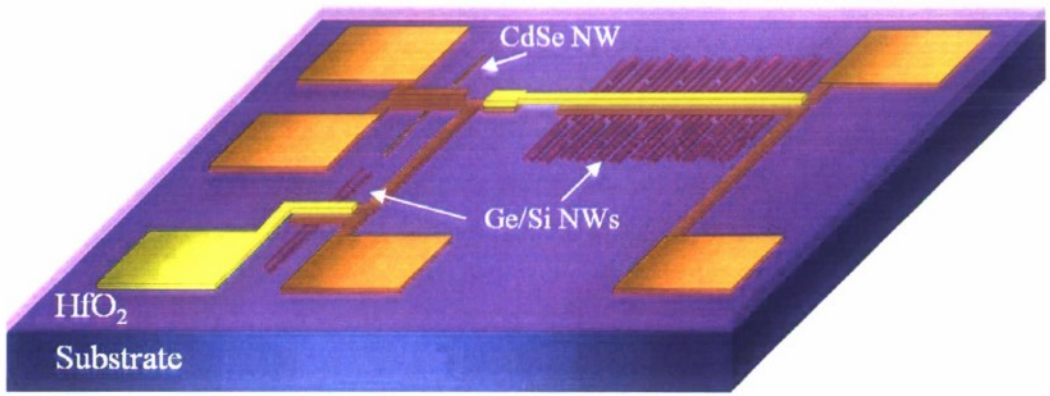
Monolayer Resist for Patterned Printing

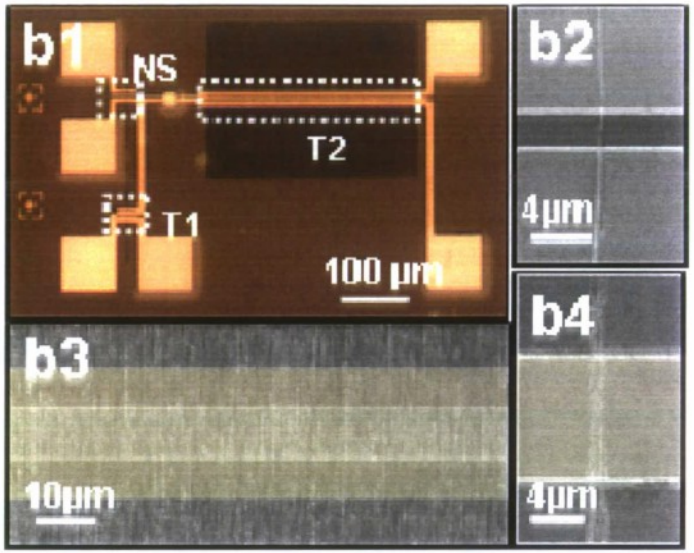






Heterogeneous NW Integration

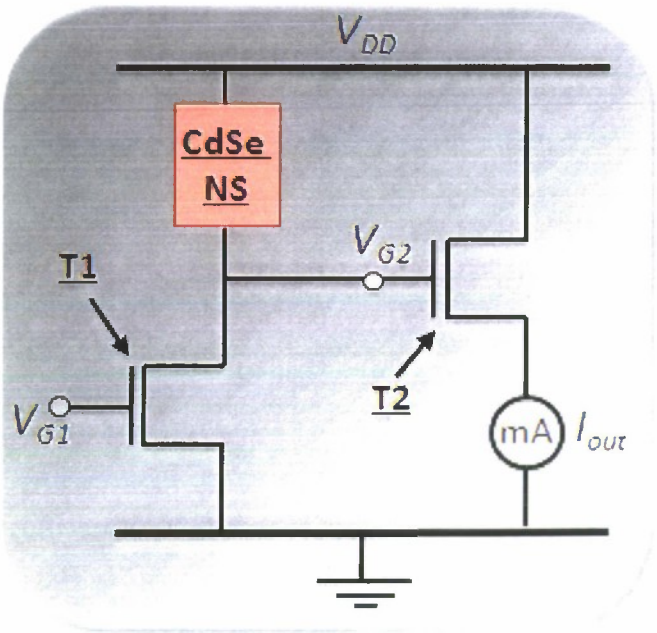




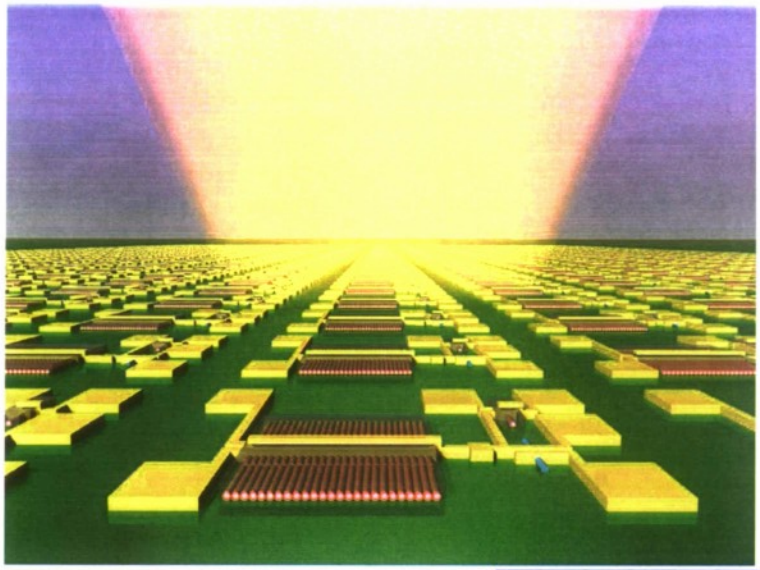
❖ Heterogeneous integration of high mobility Ge/Si NWs with optically active CdSe NWs.

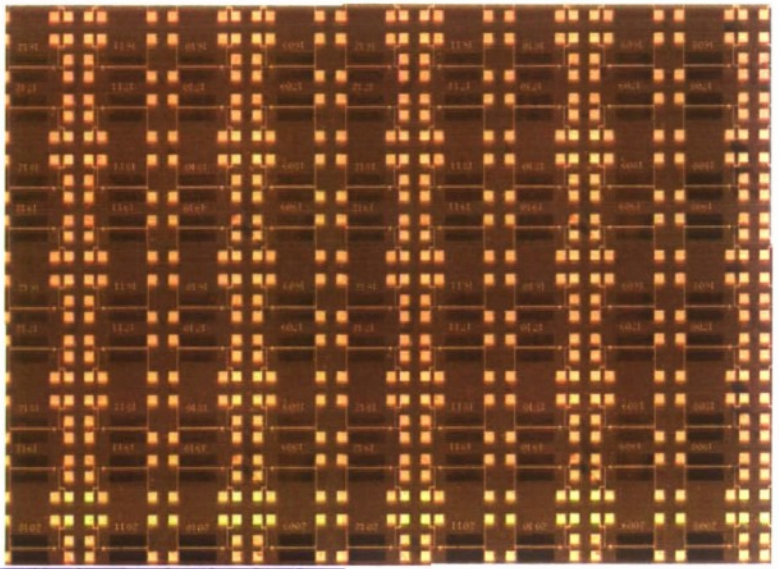
❖ Nanowires are assembled in two printing steps.

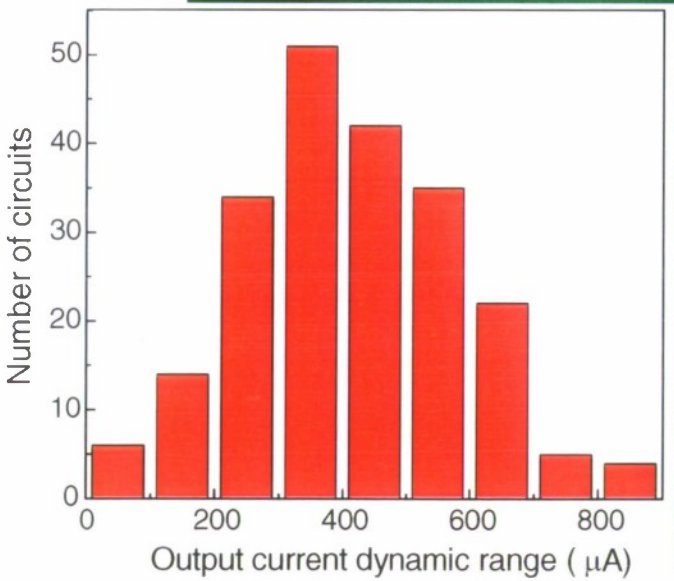
Z. Fan, et al, PNAS, 2008.

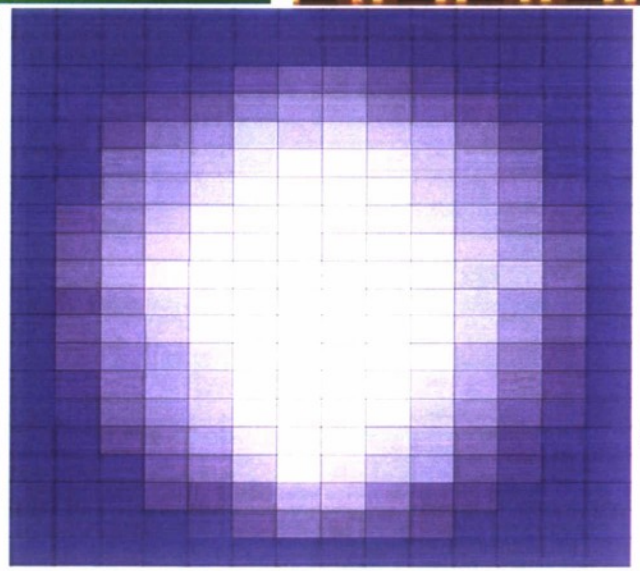


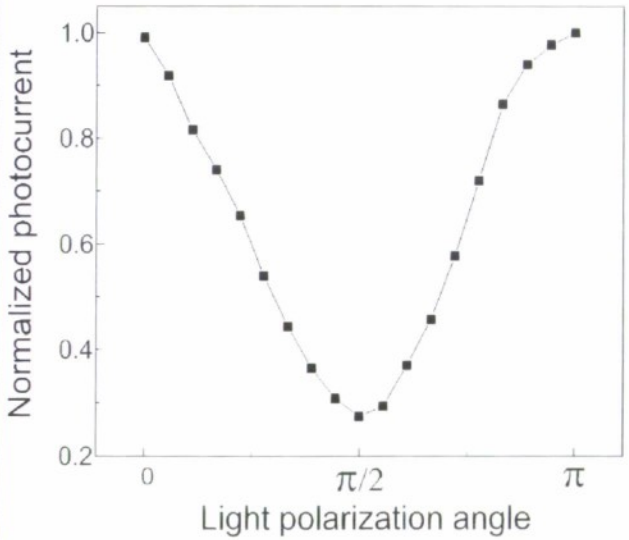
Heterogeneous NW Integration











Proof of concept imager: large NW arrays can be integrated into functional circuitry with high uniformity over large areas