System Impact of Pulsed Power Loads on a Laboratory Scale Integrated Fight Through Power (IFTP) System

B. Cassimere, C. Rodríguez Valdez, S.Sudhoff, S. Pekarek,
B. Kuhn, D. Delisle, and E. Zivi

***Abstract*— Pulsed power weaponry is being considered for inclusion in future warships. In this work, the effects of pulsed power weaponry on a power distribution and propulsion system are demonstrated in the context of a physical system known as the Naval Combat Survivability Testbed. It is shown that, as expected, when using an integrated fight through power (IFTP) architecture, the pulsed power load results in a disturbance on the generation ac bus; but it has no effect on the zonal ac busses. The use of propulsion coordination is also investigated.**

***Index Terms*—power electronics, power systems, pulsed power, transient behavior**

I. Introduction

THE use of pulsed power weaponry such as rail guns is being considered for inclusion in future warships. In this work, the effects of such weaponry on the power distribution and propulsion system are demonstrated in the context of a physical system – the Naval Combat Survivability Testbed depicted in Fig. 1. As can be seen, this testbed utilizes an Integrated Fight Through Power (IFTP) architecture. This laboratory scale system has a total generation capacity of 60 kW. The system is meant to be a resource for researchers in Naval power and propulsion systems and has no proprietary components or controls.

This work begins with a system description of the principal system components. Next, a detailed description of the pulsed power load will be set forth. This load has two parts. The first part is a controlled rectifier which serves to charge the second part of the load – a capacitor bank. This capacitor bank could be used to drive a rail gun. Since the laboratory system does not include a rail gun, a capacitor emulator system is used to emulate the bank and rail gun. This emulator will also be described in detail. The final part of the system description will be of a simple control to coordinate the pulsed power load and propulsion system.

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B. Cassimere, C. Rodriguez, S.D. Sudhoff, and S.P. Pekarek are with Purdue University, West Lafayette, IN 47907, USA (e-mail: sudhoff@purdue.edu).

B. Kuhn is with SmartSpark Energy Systems (e-mail: B.Kuhn@smartsparkenergy.com)

D. Delisle, is with Naval Sea Systems Command, (e-mail: DelisleDE@navsea.navy.mil).

E. Zivi is with the U.S. Naval Academy, (e-mail: zivi@usna.edu).

After the system description, a collection of experimental studies demonstrating the effects of the pulse power load on the NCS Testbed will be presented. It is shown that while the pulsed power load does impact the generation ac bus, the zonal ac busses are undisturbed.

II. System Description

Fig. 1 depicts the Naval Combat Survivability Testbed. This system consists of a 59 kW generator, a 37 kW propulsion motor, a 15 kW (total load) three zone zonal distribution system, and a 18 kW peak power pulsed power load.

In this system a turbine emulator / governor acts as the prime mover (PM) for the system. Physically, the turbine emulator is implemented using a 120 kW 4-quadrant speed-controlled dynamometer. The prime mover acts on a 59 kW 3-phase wound rotor synchronous machine with a brushless excitation system. The nominal output of the generator is 560 V, l-l, rms. Details on the synchronous machine are set forth in [1,2], on the brushless exciter in [3,4], and on the voltage regulator and prime mover in [5].

In Fig. 1, the generation bus can be seen to supply the port bus of the distribution system through power supply PS-1, the pulsed power load PP, and the propulsion drive PD. The most significant load on the system is the propulsion drive. In this system, the propulsion drive consists of a rectifier, dc link, and inverter fed induction motor which is connected to a load emulator. The power level of the propulsion load is 37 kW, or about 63 % of the maximum system generation. Fig. 2 depicts the propulsion drive topology. Fig. 3 depicts the top layer of the control. Therein, the propulsion drive has two modes, a speed control mode and a torque mode. The speed control is a simple PI based control. In the speed control mode, the principal output is a desired torque $T_{e,sc}$. The torque command to the drive is then selected between the torque reference $T_{e,ref}$ (in torque mode) and the speed control desired torque $T_{e,sc}$ (in speed mode) yielding the torque command T_e^*. An adaptive maximum torque per amp control (AMTPA) determines a current and slip frequency commands based on the torque command. The current command is limited, and a synchronous current

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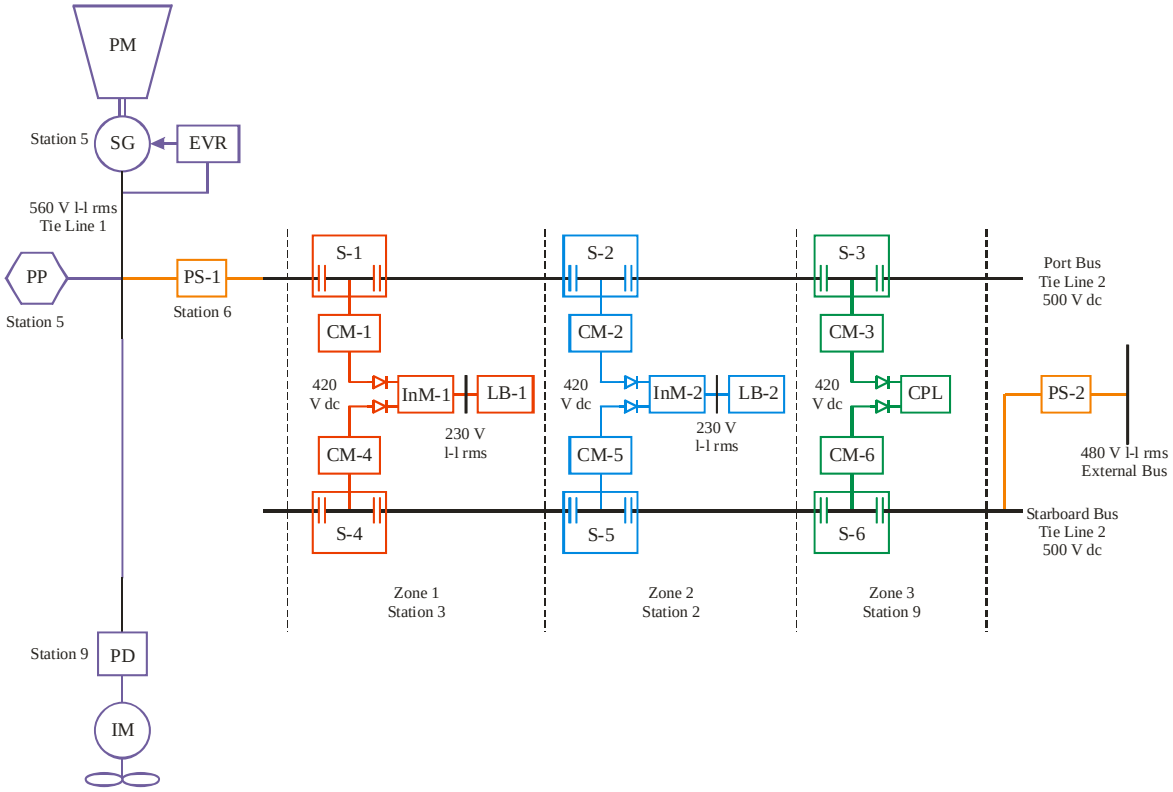

Fig. 1. Naval Combat Survivability Testbed.

regulator (SCR) is used in conjunction with a delta modulator to control the inverter switching devices in such a way that the desired current is obtained. The control also utilizes an on-line rotor resistance estimator. Details on the induction machine are set forth in [6-7], on the adaptive maximum torque per amp control in [8], on the adaptive rotor resistance estimator in [9], and on the synchronous current regulator and delta modulator in [10].

As depicted in Fig. 1, the dc power distribution system port bus is fed by power supply PS-1. This is a controlled rectifier based unit designed for an output voltage of 500 V dc, and has a continuous rating of 15 kW. Sectionalizers S-1, S-2, and S-3, connect converter modules CM-1, CM-2, and CM-3 to the port bus. Each converter module has a continuous rating in excess of 5 kW and has an output voltage of 420 V dc (unloaded) to 400 V (at 5 kW). The situation is identical on the starboard bus, though the power supply (PS-2) is fed from the utility rather than the generation bus.

From Fig. 1, it can be seen that the zone 1 inverter module (InM-1) is supplied by converter modules CM-1 (port bus) and CM-4 (starboard) bus through or-ing diodes. Because of the droop controls present on the converter modules, if both the port and starboard bus are active, then the load will be shared between the busses. The output of inverter module InM-1 is three-phase 230 V l-l rms ac. This bus supplies load bank 1 (LB-1), a 5 kW resistive load. Zone 2 is similar to Zone 1. In Zone 3, a generic constant power load is used in place of the inverter module. Details on the dc power distribution components are set forth in [11].

III. PULSED POWER LOAD

The objective of this paper is to study the system effects of pulsed power loads. In this paper, this will take the form of a power converter which is used to charge an (emulated) dc capacitor bank from the ac system bus. Based on very crude scaling of anticipated platforms to the Naval Combat Survivability Testbed, the pulsed power charging network is required to store a peak energy of 200 kJ; in the present system it is assumed that 128 kJ are extracted from the capacitor bank per event. The peak pulse rate for this load will be approximately 6 cycles per minute (though the first charge cycle takes longer since there is no initial charge).

The power converter topology used for the pulsed load is depicted in Fig. 4. As can be seen, a transformer line-commutated converter is used to charge the energy storage capacitor C_{stg}. Once the capacitor becomes charged to the desired point, the pulsed load discharges the capacitor.

The highest level of the pulsed power control is the charge / discharge control shown in Fig. 5. The inputs to this control are a command to charge the capacitor, e_c^* (high to charge), a command to discharge, e_d^* (high to discharge), the filtered voltage across the energy storage capacitor, v_{cf}, and the minimum capacitor voltage at which firing is allowed, v_{c2}^*. The outputs of this control are the actual charging status, e_c (high to charge), and actual discharge status, e_d (high to

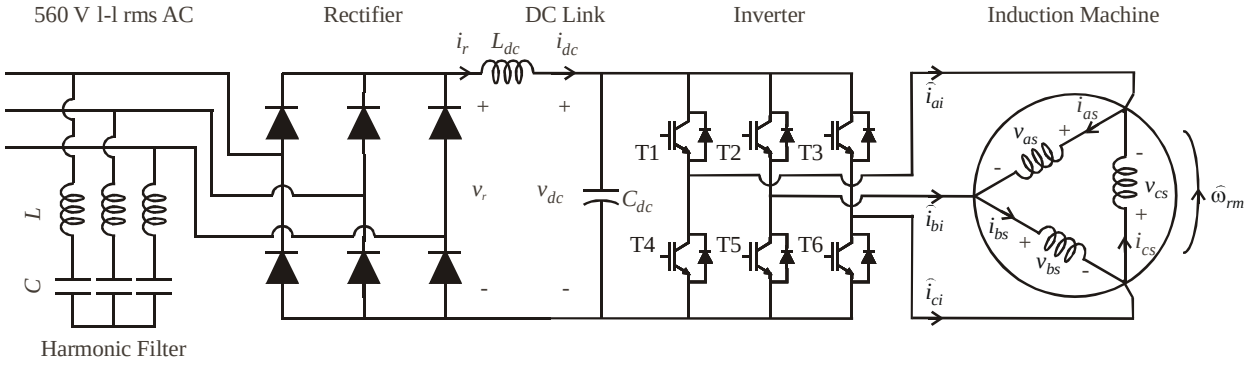

Fig. 2. Propulsion Drive.

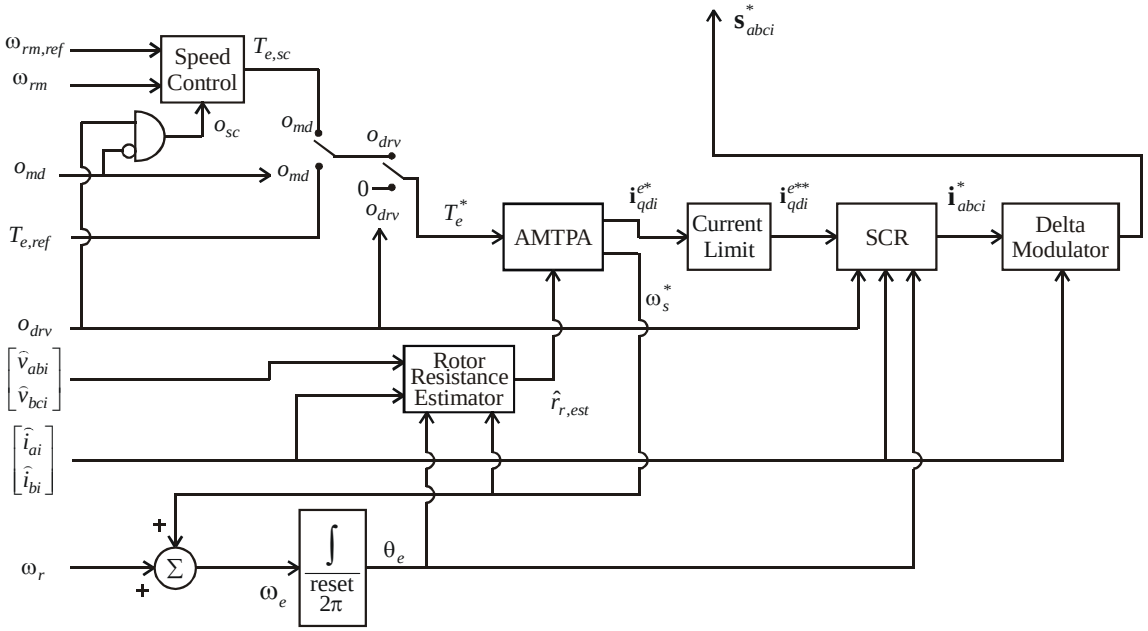

Fig. 3 Propulsion Drive Control.

discharge).

Provided that a discharge sequence is not underway, setting e_c^* high will cause the charge status, e_c, to go high, whereupon the capacitor will be charged. If the energy storage capacitor voltage is above the threshold and e_d^* goes high (indicating a request for discharge), or e_d^* is already high and the filtered capacitor voltage becomes greater than the minimum firing voltage, v_{c2}^*, then e_{ds} will immediately go high to indicate that a discharge sequence has been initiated. On the rising edge of this signal two pulses are generated. The first of these has a duration of t_{dc}, the time interval over which charging is disabled. The second of these has a duration of the total discharge cycle t_{dc} less the time required to physically discharge the capacitor t_{dis}. The result is that the charge status e_c goes low for the entire discharge cycle of length t_{dc} and e_d goes high (and the actual discharge occurs)

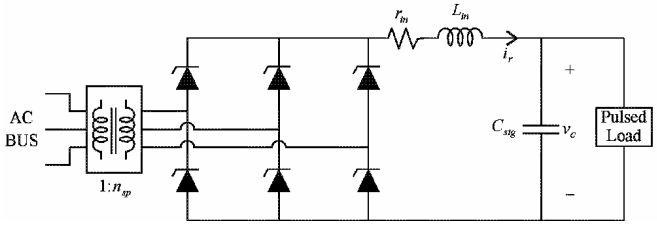

Fig. 4. Pulsed Power Charger Topology

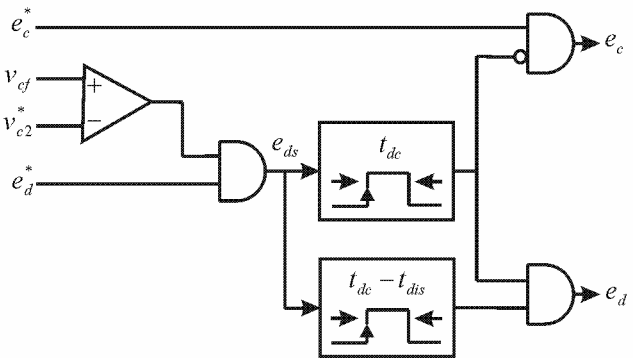

Fig. 5. Charge / Discharge Control

during the last t_{dis} of the discharge interval of length t_{dc}.

The next level of the control is the synthesis of a capacitor current command i_c^*. This control is diagrammed in Fig. 6. The basic philosophy of the control is to charge the capacitor as rapidly as possible subject to a peak capacitor current limit, i_{cmax}, and a peak power limit, P_{cmax}. Inputs to the control are the target final capacitor voltage, v_{c1}^*, the measured capacitor voltage, $\hat{v}_c$, and the charge status, e_c. As can be seen, the measured capacitor voltage is first filtered by a simple low pass filter with time constant τ_{inf} and then subtracted from the command. The voltage error is then multiplied by a proportional gain K_{sf} and limited to a dynamic limit i_{climit}, which is calculated so as to insure both the power and peak current limit will be observed.

The commanded capacitor current is then the filtered output (time constant of τ_{of}) of either this gain/limiter (if e_c is high) or zero (if e_c is low).

The gain K_{sf} is selected to be large enough that the limit is almost always in effect until the point where v_{cf} becomes very close to v_{c1}^*; after this point the capacitor voltage approaches the target voltage asymptotically. For this reason, the target voltage, v_{c1}^*, is slightly higher than the minimum voltage to fire, v_{c2}^*.

The objective of the next level of the control is to insure that the capacitor current accurately tracks the desired current. Fig. 7 shows the current control. In this case, the inputs to the control are the capacitor current command, i_c^*, the measured rectifier current, $\hat{i}_r$, and the filtered capacitor voltage, v_{cf}. The output of the control is the cosine of the phase delay of the load commutated converter, $\cos\alpha$. The basic strategy of this control is the formulation of a rectifier voltage command, v_r^*, which is essentially equal to the output of a PI control operating on the current error (the difference between the capacitor current command i_c^* and the filtered rectifier current i_r, which is in turn equal to the capacitor current during the charge cycle) plus a feed-forward term equal to the filtered capacitor voltage. This command is then translated to a phase delay by dividing by the nominal rectifier voltage and limiting. Note that when the limits are in effect the integrator of the PI control is prevented from integrating in order to prevent integrator wind up. Parameters of the pulsed power charging circuit and controls are listed in the Appendix.

IV. CAPACITOR EMULATOR

The capacitor emulator is depicted in Fig. 8. This circuit is designed to replace the energy storage capacitor of the charging circuit. It allows the amount of energy that needs to be physically stored by the system to be drastically reduced. In addition, it allows the energy stored to be rapidly discharged with moderate currents. Using the capacitor emulator, energy is continually dissipated. The main design goal of the capacitor emulator is to make the charging circuit behave exactly as if the full energy storage capacitor was in place.

The capacitor emulator circuit's first element is a physical capacitance which is a fraction γ of the capacitance to be emulated, C_{emu} (which is the desired storage capacitance C_{stg}). Next, a boost stage regulates the energy leaving the storage capacitor, C_{emu}. It dumps the energy from the emulator capacitor into the intermediate buck-boost capacitor, C_{bb}. Note that there is a power supply connected to the emitter of the boost IGBT, v_k. This power supply provides a negative bias voltage such that even when the voltage in the emulator capacitor is zero, the boost circuit has control capability over the current in the boost inductor, L_{boost}. With this power supply is a capacitor, C_k, and a diode to provide a current conduction path if the power supply fails to avoid negatively charging C_k.

The intermediate energy storage capacitor, C_{bb} separates the boost circuit from a buck circuit. The energy stored in this capacitor is discharged by the buck circuit into the load resistor, R_{load}.

The boost circuit controller is depicted in Fig. 9. Therein, the inputs to the control are the current into the storage capacitor, i_{cin} and the storage capacitor voltage, v_c. Both of these quantities are initially low pass filtered with a time constant of τ_{bbf}. The output of the controller is the

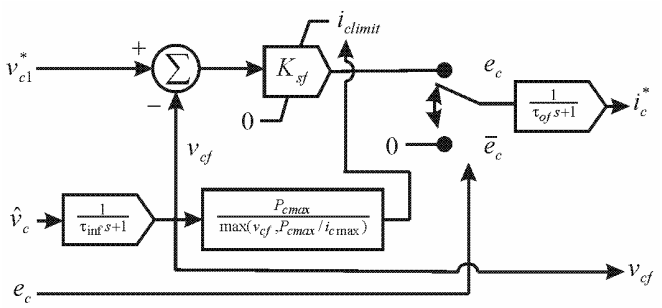

Fig. 6. Current Command Synthesizer

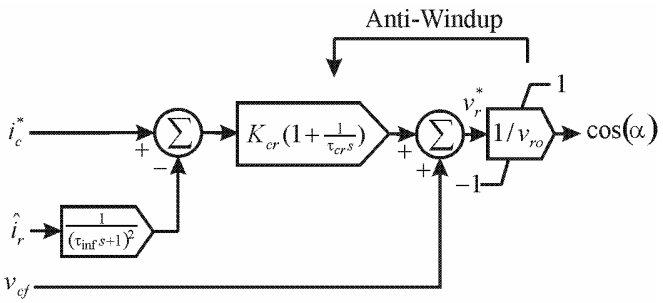

Fig. 7. Current Control.

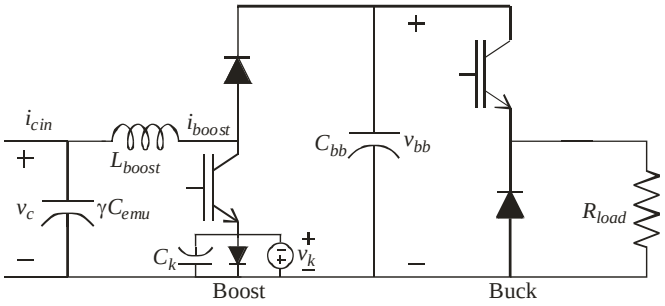

Fig. 8. Capacitor Emulator.

commanded current of the boost inductor, i^*_{boost}. The primary basis of the control is a feed-forward of the capacitor input current which is multiplied by the capacitor reduction factor $(1-\gamma)$. To this, a correction factor is added. This correction factor is formed by integrating the current into the capacitor and dividing it by the estimated capacitance of the full capacitor. This gives the expected value of the capacitor voltage. Then, this value is subtracted from the actual capacitor voltage and multiplied by a gain factor, K_{vc} and then added to the feed-forward term. After a discharge event, the output of the integrator is set to the remaining voltage in the capacitor to start the next cycle. The gating signal for the boost IGBT is generated using a hysteresis controller with a hysteresis level of Δi_{boost}.

The buck circuit's control is shown in Fig. 10. Nominally, the voltage in the intermediate energy storage capacitor is regulated to be twice the voltage in the main energy storage capacitor. This allows the boost circuit to operate with a nominal duty cycle of 50%. In this manner, voltage hysteresis is utilized with a hysteresis level of Δv_{bb}. The commanded voltage, v^*_{bb} is generated by bounding the value of $2v_c$ between Δv_{bb} and $v_{bb,max}$. The voltage hysteresis control operates in a similar manner as a current hysteresis controller. The buck switch is turned on if v_{bb} exceeds v^*_{bb} by Δv_{bb} and is turned off when v_{bb} is less than $v^*_{bb} - \Delta v_{bb}$.

The parameters used for the capacitor emulator control are listed in the Appendix.

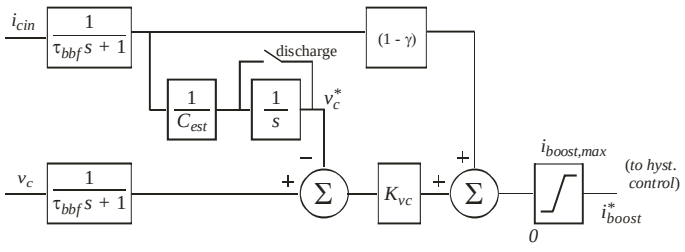

Fig. 9. Capacitor Emulator Boost Control.

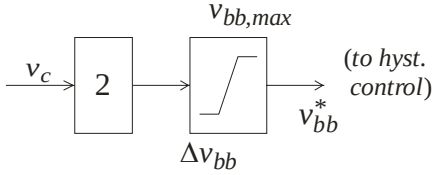

Fig. 10. Capacitor Emulator Buck Control.

IV. PROPULSION COORDINATION

It will be shown that coordinating propulsion and pulsed power loads can reduce the system impact of pulsed power loads. A control algorithm to provide such coordination is depicted in Fig. 11. Therein, inputs are the mechanical rotor speed of the propulsion drive, ω_{rm}, the torque command to the propulsion drive, T^*_e, and the effective instantaneous power command into the pulsed power load, P^*, which is equal to the commanded capacitor current, i^*_c, times the filtered measured capacitor voltage, v_{cf}. Based on these quantities a modified torque command, T^{**}_e, for the propulsion drive is produced such as to keep the overall system power requirements constant, subject to a maximum torque perturbation $\Delta T_{e,mx}$ and that the final torque command has to be positive. For the studies to be considered, $\Delta T_{e,mx}$ was set equal to the maximum allowed torque command of 200 Nm.

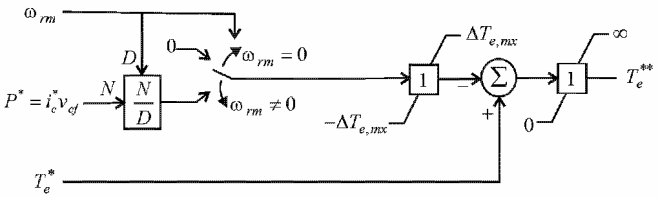

Fig. 11. Propulsion Coordination Control

V. SYSTEM PERFORMANCE

In this section, the system performance under pulsed loading conditions is examined. Two principal studies will be performed. Common features of the study are that each zone will be loaded to 5 kW, and that the propulsion drive will be operating at full speed (1800 rpm) and full torque (200 Nm). In the studies presented, it is assumed that the starboard bus is faulted, so that the situation represents a damaged scenario. An additional feature of the studies will be that a 200 kJ charge cycle is used. Recall that the pulsed power load normally starts from a non-zero capacitor voltage, and that a discharge will remove 128 kJ. In this study, the initial capacitor voltage is 0 (so 0 kJ stored) and will be charged to

200 kJ; and this amount of energy will be fully discharged. As a result, the charge cycle will be longer than normal.

Variables to be depicted are as follows:

$v_{ab,sg}$ Line-to-line synchronous generator voltage (V)

$i_{a,sg}$ A-phase synchronous generator voltage (V)

$i_{fde,sg}$ Brushless exciter field current (A)

$i_{r,pp}$ Pulsed power rectifier current (A)

$i_{a,pp}$ A-phase pulsed power current (A)

$v_{c,pp}$ Pulsed power energy storage capacitor voltage (V)

$i_{a,pd}$ A-phase propulsion drive current (A)

$v_{dc,pd}$ DC link propulsion drive voltage (V)

$v_{dc,pb}$ DC voltage on port bus (V)

$v_{dc,im1}$ DC voltage at input to inverter module 1 (V)

$v_{ab,im1}$ Line-to-line output voltage at inverter module 1 (V)

Fig. 12 depicts the system performance in the absence of propulsion coordination. In assessing the waveforms, the pulsed power capacitor voltage waveform, v_{cp}, is particularly useful as it can be used to mark the progress of the charging cycle. In Fig. 12, it can be seen that the generator voltage profile remains flat, with the exception of at the beginning and end of the charge cycle. It can also be seen that the generator current also remains almost flat – although it does increase slightly. The fact that only a slight increase occurs is a result of the fact that the input current is almost constant. However, despite this the power out of the synchronous machine is not since the power factor of the pulsed power load starts out very low and then increases as the capacitor voltage increases. The next trace is the brushless exciter field current. Again, the disturbance is most pronounced at the beginning and end of the study. The pulsed power rectifier current, $i_{r,pp}$, can be seen to be essentially constant over until the end of the charge cycle where it starts to decrease because of the power limit in the pulsed power control. Observe that the ripple decreases as the capacitor voltage increases (and firing delay decreases). The next trace is the a-phase pulsed power current which is closely associated with the pulsed power rectifier current. The capacitor voltage $v_{c,pp}$ can be seen to increase nearly linearly until near the end of the charge cycle when the pulsed power power limit comes into play.

The propulsion drive current a-phase current $i_{a,pd}$ and dc link voltage $v_{dc,pd}$ are almost unaffected by the charging of the pulse power load (recall that in this study propulsion co-ordination is off), although a minor disturbance is evident at the beginning and end of the study. The propulsion drive torque $T_{e,pd}$ is completely unaffected by the pulsed power load.

The next traces depict the performance of the pulsed power load on the dc distribution system. As can be seen, there is a minor disturbance in the port bus voltage at the

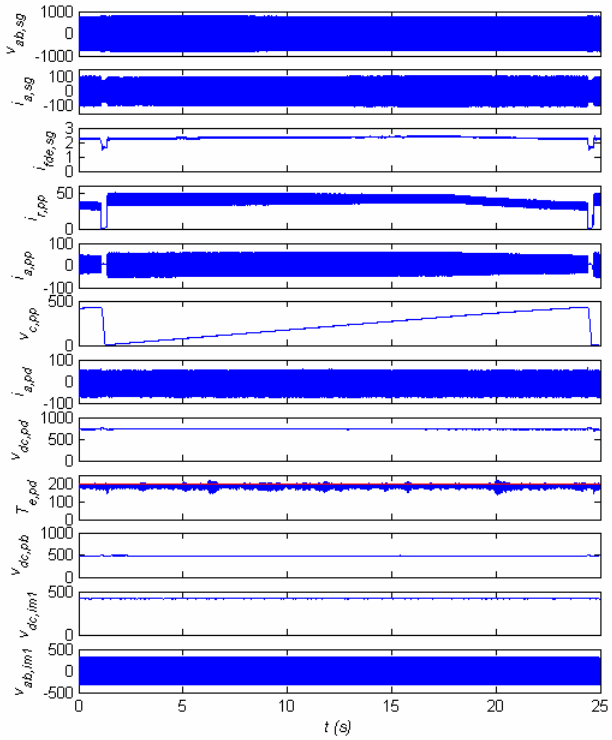

Fig. 12. Study 1 results.

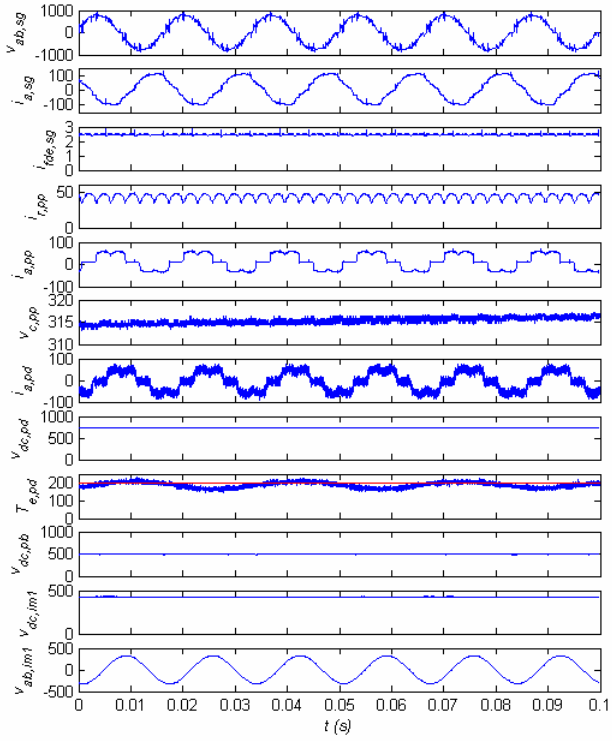

Fig. 13. Study 1 results – expanded time scale.

beginning and end of the charge cycle. However, this disturbance does not propagate to the dc voltage at the input to the inverter module $v_{dc,im1}$ nor to the ac output of the inverter module, $v_{ab,im1}$, as would be expected.

Fig. 13 depicts and expanded view of all of the waveforms at the point wherein the pulsed power capacitor voltage is approximately 315 V. One unexpected feature in the waveforms is an approximately 30 Hz oscillation in the propulsion drive torque. The torque transducer has only recently been added to the system and the cause of this torque variation has not been identified. It may be associated with the dynamometer speed control rather than the system.

Figs. 14-15 depict the system performance for the same conditions, but in this study (Study 2) propulsion coordination is used. Many of the trends are similar, but there are some differences. First, the generator current and brushless exciter current are always less than in Study 1 wherein propulsion coordination is not used. A second difference is that in this study, the propulsion drive current and torque are, as one would expect, highly influenced by the pulsed power charging cycle. Unfortunately, the principal benefit of propulsion coordination, that is real power load leveling, would require showing either the synchronous machine torque or power; these signals were not available at the time this paper was prepared, but will be recorded in the future.

APPENDIX – PULSED POWER PARAMETERS

TABLE I
PULSED POWER TRANSFORMER PARAMETERS

Parameter	Value	Description
$L_{\ell p}$	0.222 mH	primary leakage inductance
r_p	0.100 Ω	primary resistance
L_m	2.321 H	magnetizing inductance
$L_{\ell s}$	0.222 mH	secondary leakage inductance
r_p	0.100 Ω	secondary resistance
n_{sp}	0.786	secondary to primary turns ratio

TABLE II
PULSED POWER PASSIVE PARAMETERS

Parameter	Value	Description
L_{in}	11 mH	input inductor series inductance
r_{in}	0.1 Ω	input inductor series resistance
C_{es}	2.02 F	energy storage capacitance

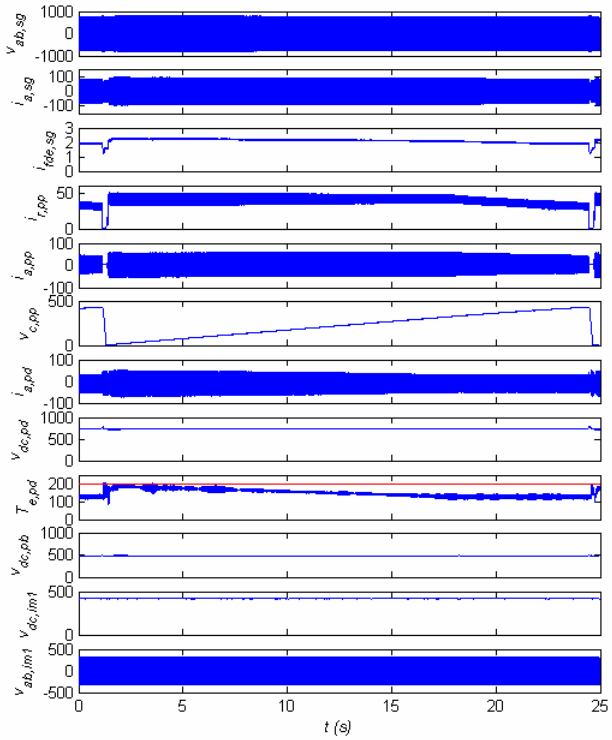

Fig. 14. Study 2 results.

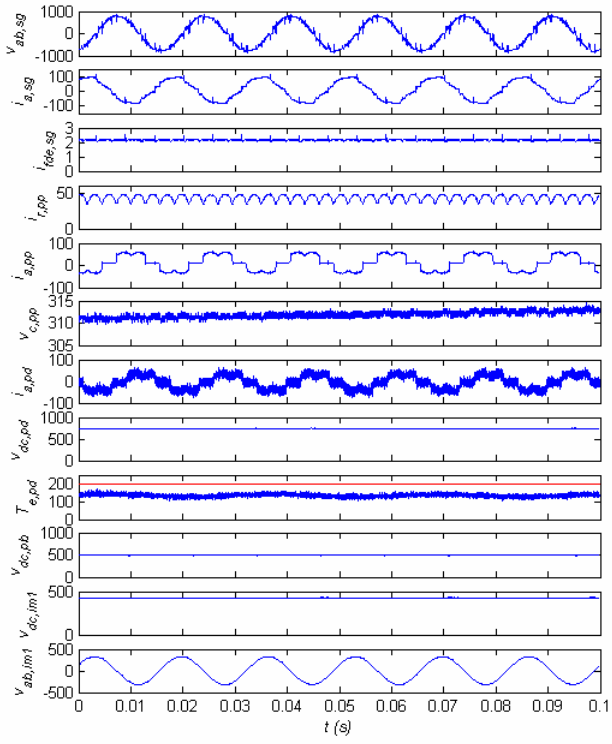

Fig. 15. Study 2 results – expanded time scale.

TABLE III
CHARGE/DISCHARGE AND CAPACITOR CURRENT CONTROL PARAMETERS

Parameter	Value	Description
v_{c1}^*	450 V	target capacitor charging voltage
v_{c2}^*	445 V	minimum capacitor firing voltage
P_{cmax}	13.52 kW	maximum allowed power into storage capacitor
i_{cmax}^*	40.52 A	maximum allowed current into storage capacitor
t_{dis}^*	0.2 ms	time over which storage capacitor is discharged
t_{dc}^*	0.25 ms	time of discharge cycle
τ_{inf}^*	0.79 ms	time constant of input filter
τ_{of}^*	5.0 ms	time constant of output filter
K_{sf}^*	13.35	current forward gain

TABLE IV
CAPACITOR EMULATOR PARAMETERS

Parameter	Value	Description
C_{est}	2.02 F	estimated value of full capacitance
γ	0.01	capacitor reduction factor
l_{boost}	0.5 mH	inductor for boost circuit (100A)
R_{load}	33.3 Ω	load resistance (18kW)
C_{bb}	500 µF	intermediate storage capacitor
v_k	-24 V	startup voltage
C_k	930 mF	startup capacitor
K_{vc}	20 A/V	gain for boost current control
$i_{bost,max}$	100 A	current limit for boost control
Δi_{boost}	2.67 A	boost current hysteresis level
$v_{bb,max}$	750 V	maximum voltage for C_{bb}
Δv_{bb}	25 V	voltage hysteresis level
τ_{bbf}	31.8 µs	input filter time constant
i_{dis}	60.0 A	inductor current during discharge

REFERENCES

[1] D.C. Aliprantis, S.D. Sudhoff, B.T. Kuhn, "A Synchronous Machine Model with Saturation and Arbitrary Rotor Network Representation," accepted for *IEEE Transactions on Energy Conversion.*

[2] D.C. Aliprantis, S.D. Sudhoff, B.T. Kuhn, "Experimental Characterization Procedure for a Synchronous Machine Model with Saturation and Arbitrary Rotor Network Representation," accepted for *IEEE Transactions on Energy Conversion.*

[3] D.C. Aliprantis, S.D. Sudhoff, B.T. Kuhn, "A Brushless Exciter Model Incorporating Multiple Rectifier Modes and Praisach's Hysteresis Theory," accepted for *IEEE Transactions on Energy Conversion.*

[4] D.C. Aliprantis, S.D. Sudhoff, B.T. Kuhn, "Genetic Algorithm Based Parameter Identification of a Hysteresis Brushless Exciter Model," accepted for *IEEE Transactions on Energy Conversion.*

[5] D.C. Aliprantis, "Advances in electric machine modeling and evolutionary parameter identification," Ph.D. dissertation, Purdue University, West Lafayette, IN, Dec. 2003 (Appendices C and D).

[6] S.D. Sudhoff, P.L. Chapman, B. T. Kuhn, D. Aliprantis , "An Advanced Induction Machine Model for Predicting Inverter-Machine Interaction," *IEEE Transactions on Energy Conversion*, Vol. 17, No. 2, June 2002, pp. 203-210]

[7] Chunki Kwon, Scott D. Sudhoff, "A Genetic Algorithm Based Induction Machine Characterization Procedure," 2005 International Electric Machines and Drives Conference, San Antonio, Texas, May 15-18, 2005.

[8] Chunki Kwon, Scott D. Sudhoff, "An Adaptive Maximum Torque Per Amp Strategy," 2005 International Electric Machines and Drives Conference, San Antonio, Texas, May 15-18, 2005

[9] Chunki Kwon, Scott D. Sudhoff, "An On-line Rotor Resistance Estimator for Induction Machine Drives," 2005 International Electric Machines and Drives Conference, San Antonio, Texas, May 15-18, 2005

[10] P.C. Krause, O. Wasynczuk, S.D. Sudhoff, *Analysis of Electric Machinery*

[11] B. P. Loop, "Estimating Regions of Asymptotic Stability of Nonlinear Systems with Applications to Power Electronics Systems," Ph.D. dissertation, Purdue University, West Lafayette, IN, May 2005.