Chip-scale Photonics

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Microsystems Technology Symposium

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Standard Form 298 (Rev. 8-98)
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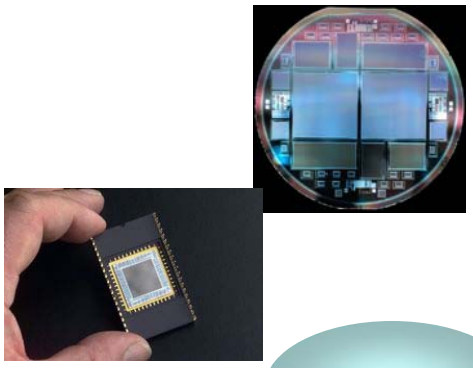
Photonic information/energy processing

What do we do now with photons?

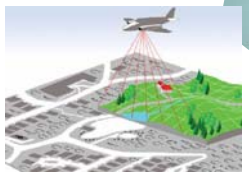


Photonic Time Domain Processing

Compute, Process

Display

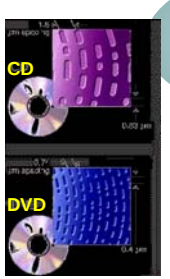
Sense



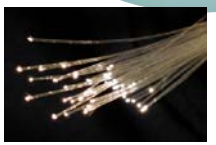
Photonics

Energize

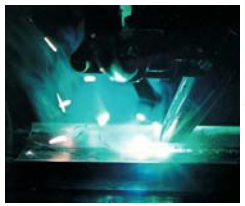
Store



Transport



Actuate



Medical Applications

Laser Welding

Photonics at the Chip level

Many functions require complex circuits structures that may benefit from *chip-scale* fabrication techniques.

- **Exploit benefits of precise material growth techniques**
- **Achieve maximum performance, yield, and circuit complexity**
- **Combine multiple functions on single chip**
- **Provide means to "get close" to Silicon**
- **Leverage advantages of lithographic design and fabrication for SCALABILITY in future generations**

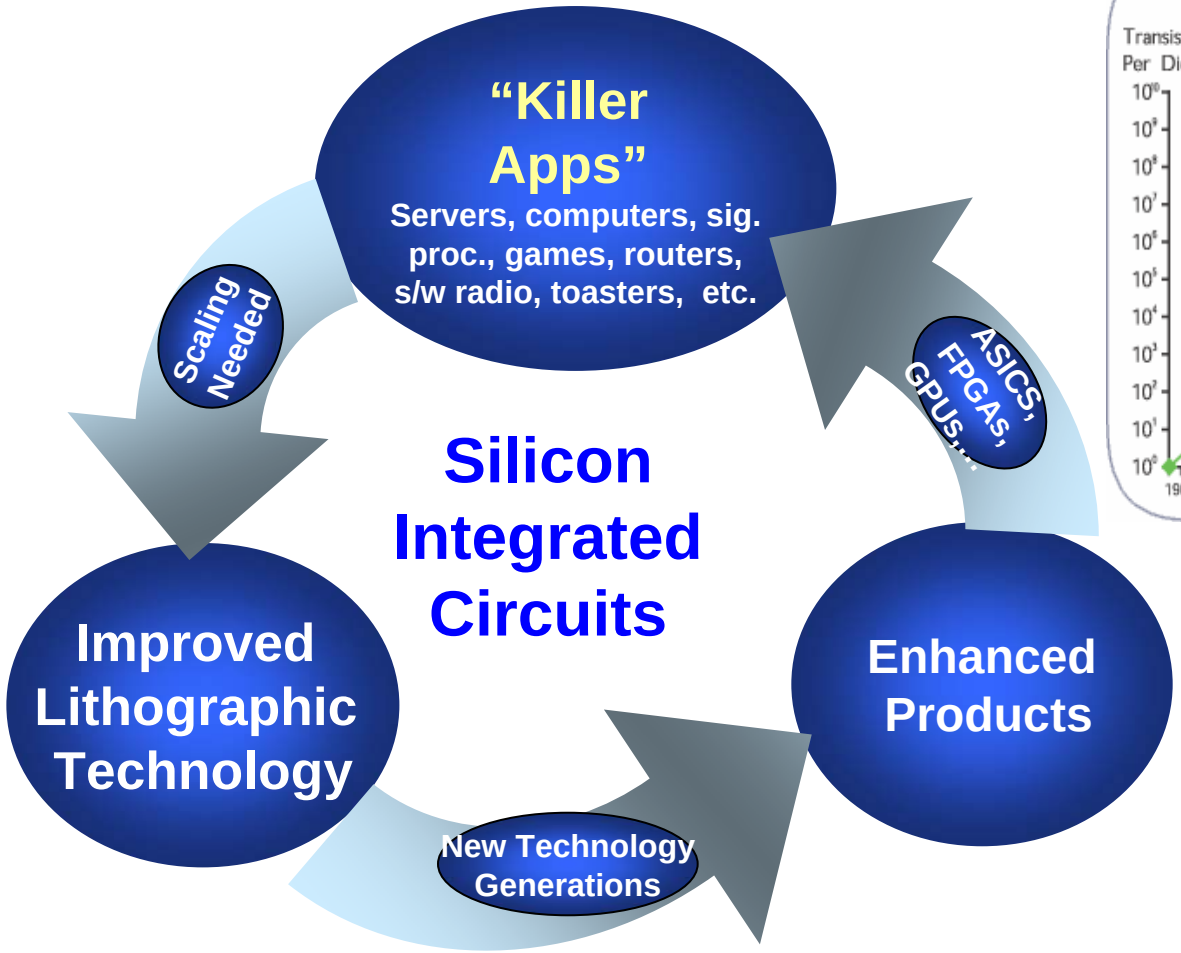
But ….

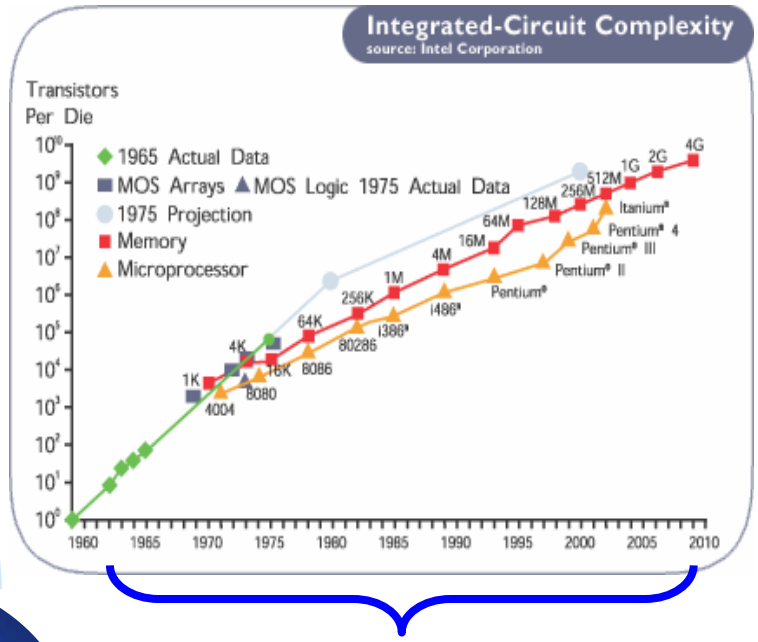
- **Make sure advantages are real**
  - **Use solid metrics to connect technology and system parameters**
- **Compete with, or "help," Silicon with great trepidation!**

The vicious (but lucrative) cycle of Si scaling

Lithography opened path to Scaling:

- **Sustained value-added cycle due to IP that is magnified by use of technology platform**

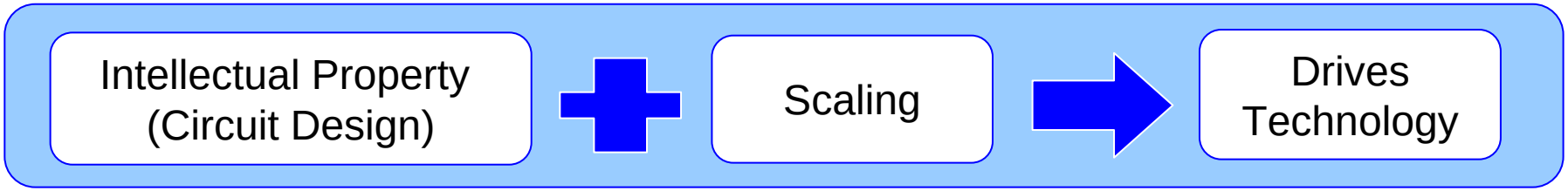




~45 years of exponential scaling!

Photonics' "tentative" start at chip-scale scaling ….

Litographic Scaling in Photonics



So….Will Photonics have an IC-driven scaling pathway?

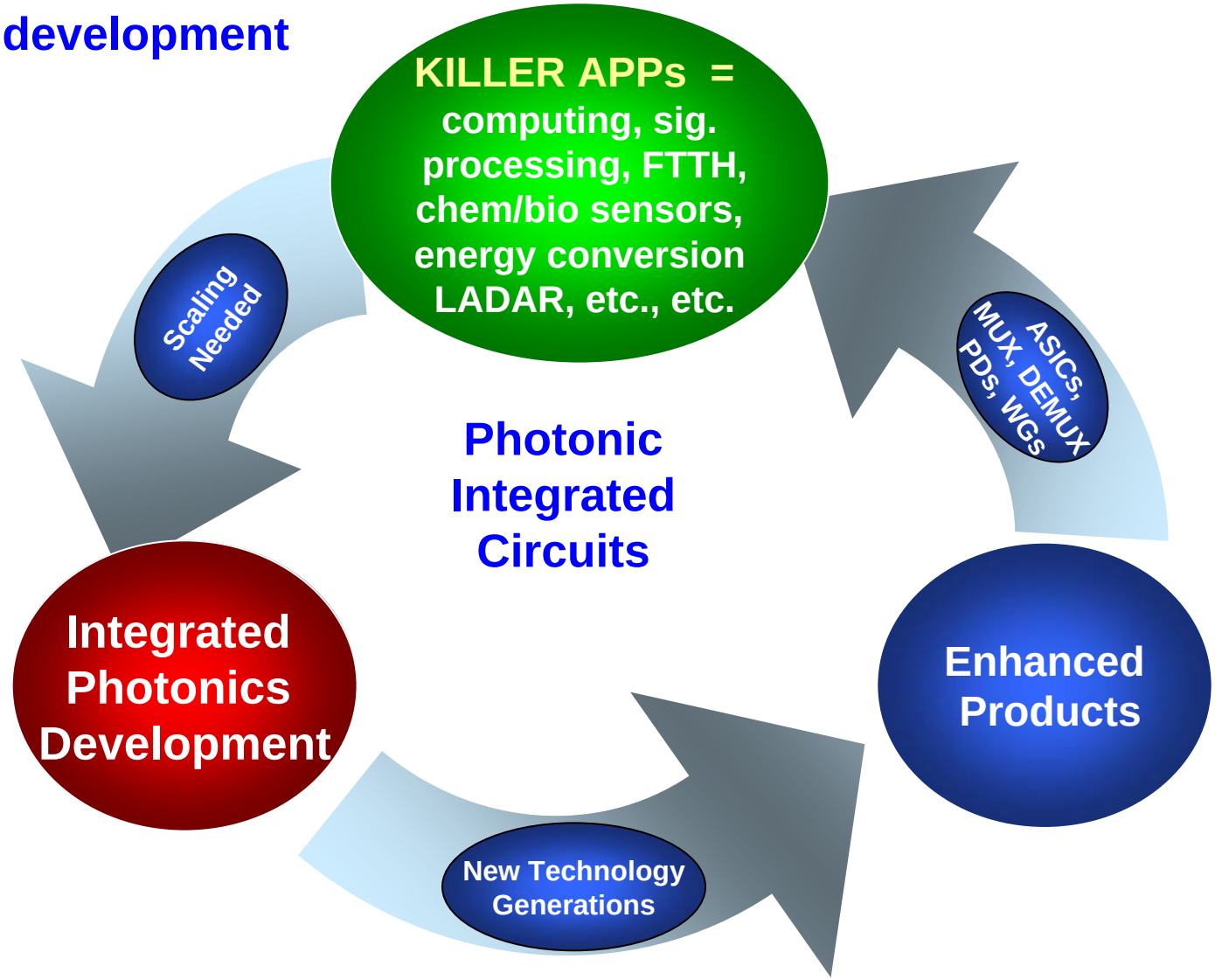
- **Can we leverage the telecom investment and focus on chip-scale applications to drive technology?**
- **Which Integrated Photonics platforms will emerge?**
- **How close to the photonic "information density" limits can we get?**

AND… Can we go… BACK TO THE FUTURE ???

- **Analog optical signal processing –** that is ***scalable*** and ***programmable***.
- **Optical interconnects –** to ***enable*** Silicon scaling
- **Optical digital computing –** as ***complement*** to Silicon
- **Computational Sensing –** but with ***integrated flat form-factor*** optics.

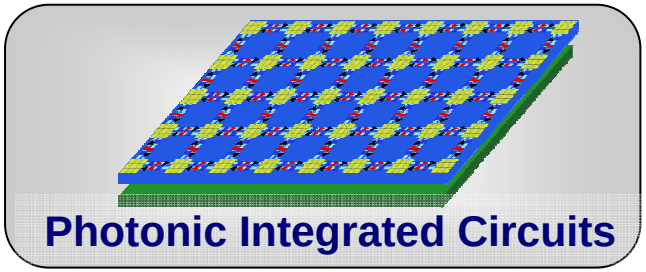
Approach: Enrich the "Killer App" domain

… to spur PIC development

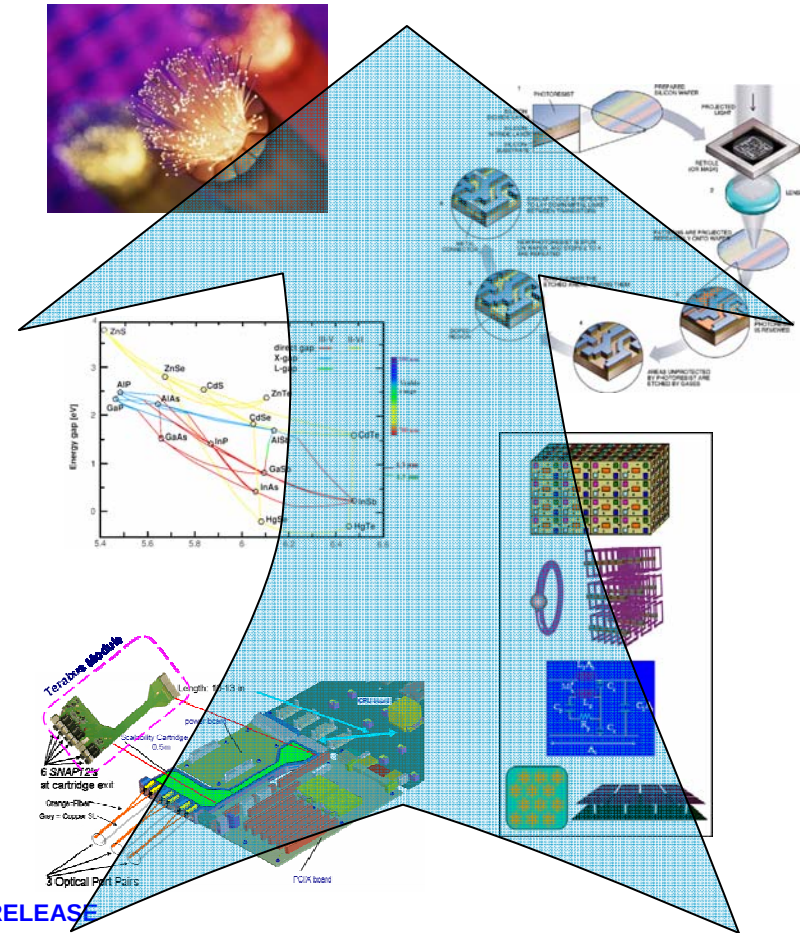


Photonics Value Proposition

How do we get there?



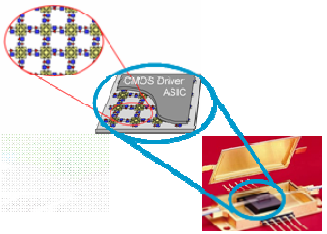
- Leverage **3 decades+** of FO technology and related devices (e.g. non-linear optics), but for non-transport functions
- Leverage **4 decades+** of lithography-based chip technology
  - What are the PIC technology platforms?
- Expand **5 decades+** of band-gap engineering
- Employ “Magic Meta-Materials” based on photonic/ phononic/ electronic/ plasmonic engineered materials
- Exploit a PIC’s natural match at interface to outside (photonic) world



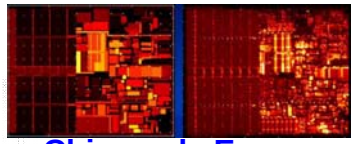
PICs enable the future

µ-LADAR

Montage



PhASER



Chip-scale Energy scavenging?

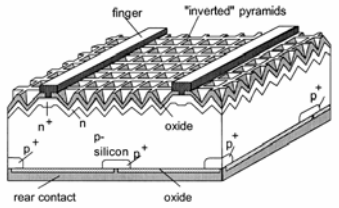
Compute, Process

Display

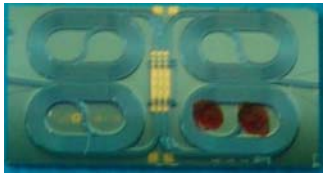
Sense

Photonics

Energize



Chip scale solar cell



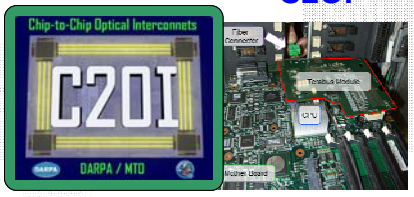
DOD-N Optical Buffer

Store

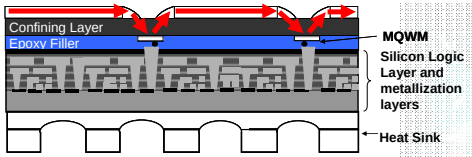
Transport

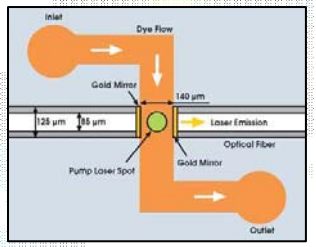
Actuate

C2OI



Intra-chip OI





µ-opto-fluidics

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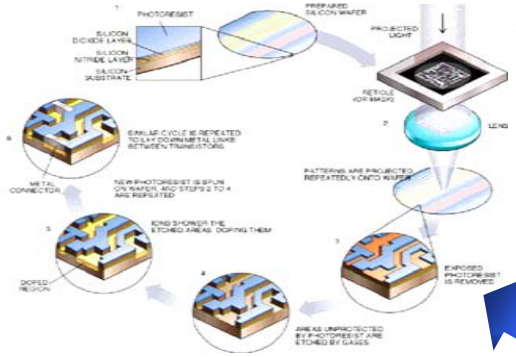
The PIC Payoff

Old: "*finger-fab*" Photonics

New: "*foundry-fab*" Photonics



Many Killer Applications

Fab-less PIC design

Technology Scaling