DESIGN OF A GIGABIT OPTICAL NETWORK INTERFACE CARD

AND

LAYOUT METHODOLOGY FOR HIGH-VOLTAGE DRIVERS IN LARGE ARRAYS FOR MODULATORS AND MEMS DEVICES

by

Premanand Chandramani

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DEDICATION

To my parents,

Whose endless love and support have inspired my achievements

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ABSTRACT

High-speed optical data links enable local area networks (LANs) that operate at data rates above 10Gbps. Various networks, protocol and switch architectures have been proposed that use these links. The optical network interface card (ONIC) is an important component for demonstrating efficient application of these architectures. In this paper, we describe the design of a programmable ONIC that interfaces a 12-channel gigabit parallel optical link module with a 64-bit/66-MHz PCI computer bus. Hardware programmability (using FPGAs) enables the ONIC to efficiently implement different communication protocols. For hardware testing, the ONIC hardware was programmed for bit error rate (BER) analysis. In continuous operation at 8Gbps for 30 days through a 1-meter fiber, no errors occurred. For application testing, a custom ONIC software driver was developed. We used this driver to demonstrate message passing between applications running on two ONIC-equipped servers. The ONIC design provides a low-cost solution that can be readily adapted for application and device specific requirements. The use of ONIC in a free-space optical switch system is described in the dissertation.

A layout methodology for high-voltage smart-pixel ICs that can integrate, high-voltage circuits and low-voltage high-density VLSI circuits with a one dimensional/two dimensional array of modulators and MEMS devices. This layout methodology is compatible with the existing CAD tools enabling the automation of placement and routing tasks. This layout methodology was applied to a high-voltage driver IC with 256 individual high-voltage driver cells to drive a one-dimensional

array of 256 Spatial Light Modulator devices. The IC was designed and fabricated using AMS 0.8um high-voltage CXZ process in a wafer run and has about 210,000 transistors. This IC has been designed to be flip-chip integrated with GaAs Multiple-Quantum-Well SLM devices. This high-voltage driver IC has the largest numbers of high-voltage drivers integrated on to a single VLSI IC compared to any commercially available driver ICs. For testing the driver performance and process variance across the array in each ASIC, the output of every eighth driver in the array was brought out to a bond pad. Also present in this dissertation is the test strategy used to test these ICs electrically at wafer level.

Chapter 1

INTRODUCTION

The use of photons to move information is making rapid strides in terms of research and development and is looked upon as the future technology of the communication world. On a networking level the undisputed trend is higher speed. The increased use of fiber optic links to get that extra speed supports that trend. High-Speed digital chips with low power consumption continue to flow out of semiconductor industry and the optical component industry has matched them with optoelectronic devices with improved performance.

Popular communication networking systems such as Wide Area Networks (WAN), Local Area Network (LAN) [1], Personal Area Network (PAN) [2], and Storage Area Network (SAN) has a unique place in market today. Of these the LAN and SAN have a brighter spot in networking. These networks interconnect large disk arrays to servers and other systems through gigabit optical data links. High-Speed optical data links enable LAN that operates at data rates above 10Gbps. In SAN the speed has been increased up to 2.125Gbps.

On the other hand the research community is coming up with new networks, protocols and switch architectures for computational intensive application that have wide range of commercial and defense related interests. The Optical Network Interface Cards (ONIC) are the gateways of communication between compute nodes in such a network for efficient demonstration of their applications. More and more optical communication modules, with varying speed and bandwidth

are available commercially. With the architectures and their applications changing, a generic architecture of the ONIC is needed for future researchers. The generic architecture of the ONIC and how future designers can readily adapt it is the first subject of this dissertation.

On the other front optoelectronic devices such as modulators and Micro Electro Mechanical Systems (MEMS) find immense use in both commercial and defense related applications. Designing and fabricating these devices in large arrays with tight pitch is possible now and the Complementary Metal Oxide Semiconductor (CMOS) Integrated Circuits (IC) to drive these devices must be able to match these advancements. A well-defined and tested CMOS IC layout methodology needs to be in place to do this. The CMOS design approach becomes more stringent when the optoelectronic devices need higher operating voltage ranges. A lot of high-voltage driver IC is available commercially. However, they don't have large number of drivers and they cannot be adapted for applications where the optoelectronic devices needed to be attached on top of active silicon. So, a custom CMOS solution that can be readily adapted and modified to suit the optoelectronic device array and application needs to be designed. This included the driver circuitry for the devices and the processing logic operating at a much lower voltage. A layout methodology needs to be defined to partition the IC with the high-voltage cells and low-voltage cells isolated and optimized separately on the same IC.

The second subject of this dissertation is the proposed layout methodology for such a high-voltage driver IC. Also, it describes the design methodology applied to a high-voltage CMOS driver IC that can drive up to 50Volts to drive modulators. This procedure has been developed as the result of designing custom ICs whose size range

from a few thousand transistors to 220,000 transistors and their functions range from driver/receiver chips to high-speed scanner IC with 768 modulators and 85Kbits of Random Access Memory (RAM). They make use of custom cells and standard cells from the vendor libraries. This layout methodology includes partitioning of the design at the voltage level and integrating mixed-signal analog and digital circuits.

1.1 Dissertation Organization

Chapter 2 provides some background information on ONIC design methodology and high-voltage driver IC layout methodology to provide some context and help the reader understand the motivation behind the designs.

Chapter 3 covers the ONIC design methodology and design implementation targeting a certain application and the results.

Chapter 4 covers the layout methodology of the high-voltage driver IC and its implementation on to a driver IC targeting a certain application. It also explains the test setup and the results from the design implementation.

The conclusions of applying the ONIC architecture and high-voltage driver layout methodology to designs and what future designers can do to improve are discussed in chapter 5.

Chapter 2

BACKGROUND INFORMATION AND MOTIVATION

2.1 Optical Network Interface Card (ONIC)

Various very short-reach (VSR) optical data links that operate at data rates of 10Gb/s (Gigabits per second) and beyond are now becoming available as commercial products [3], [4], [5]. Various network, protocol and switch architectures that utilize these links have been proposed [6], [7], [8]. Example network architecture is shown in Figure 2.1.

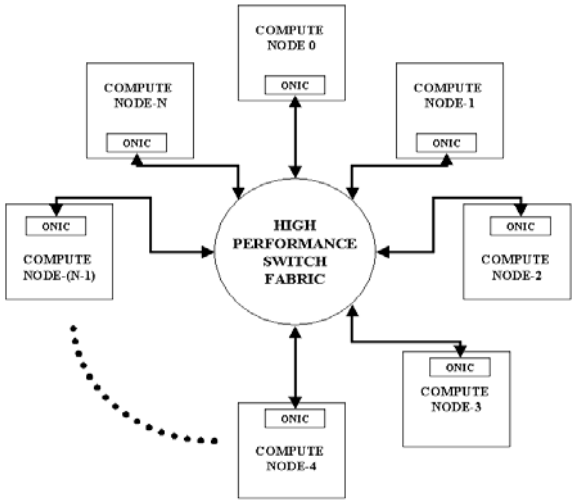


Figure 2.1 Network architecture with 'N' compute nodes interconnected in a switch fabric through ONIC

It uses VSR optical data links to interconnect multiple compute nodes through a central switch. In order to efficiently utilize the increased bandwidth capability of VSR optical data links, these network architectures use new communication protocols rather than relying on legacy based such as ATM, Ethernet, or HIPPI [9], [10], and [11]. The ONIC is an important instrument for demonstrating efficient application of these new architectures. The purpose of the ONIC is to interface a standard computing node, such as a workstation or an embedded processor, with a VSR optical data link. On the hardware front, the ONIC converts slow, wide-parallel and clock-synchronous data streams (typically used in chip-level computer interconnection) to narrow gigabit-speed data streams with embedded clock information (typically used in VSR optical data links). The ONIC hardware often contains First-In First-Out (FIFO) memory storage to buffer incoming and outgoing network data for flow control. On the software front, the ONIC includes software drivers to provide communication and flow control between the hardware, application running on the computing node and the custom network protocol used by the network that is being demonstrated.

This dissertation work describes the design of a programmable ONIC that interfaces a 12-channel, gigabit parallel optical link module [12] and [13] with a 64-bit/66-MHz Peripheral Component Interface (PCI) bus [14]. The adoption of PCI bus allows our ONIC design to be used in widely available PCI-based workstation and server computers. Hardware programmability is achieved using Field Programmable Gate Array (FPGA) integrated circuits. This enables our ONIC design to efficiently implement different network protocols. Although the current ONIC design uses a specific VSR optical data link hardware, it can be readily modified to support other

types of optical data links. The ONIC design was originally developed to demonstrate a specific network architecture that used free-space optical interconnection inside the switch fabric [6]. However, the novelty of the design is that it provides a low-cost network interface solution that can be readily modified by other researchers for network protocol and optical device specific requirements. The following paragraphs compare the ONIC approach described in this dissertation with existing ONIC implementations and provide justification for the approach followed.

Commercially available ONICs use custom integrated circuits and/or network processor chips to implement specific network protocols [15] and [16]. They cannot keep up with the 10-100 Gigabit data rates available with VSR optical data links. Finally, commercial ONICs use proprietary designs and cannot be modified to use new VSR optical link hardware. These attributes make commercial ONICs unusable for experimenting with new network architectures and VSR optical data links. On the other hand, a ONIC has been previously demonstrated that used custom-made integrated circuits to implement a specific network protocol [17]. While this approach successfully demonstrated the new network protocol proposed by its authors, it is difficult to modify this design because of the high cost and extensive knowledge required for the design of custom integrated circuits.

References [7] and [18] describe a network architecture demonstration that used a ONIC design similar to the one being proposed in this dissertation. This ONIC design also used FPGAs and Serializer De-Serializer chips (SERDES) that can be reconfigured to support various network protocols. However, it employed a proprietary memory-bus interface to connect the optical link with the computing node. While a memory bus interface permits higher bandwidth communication between the

processor and the optical link, our PCI-based ONIC supports a broad range of computing hardware from a multitude of computer manufacturers. Future modifications of the ONIC design can use the emerging PCI bus extensions to achieve higher communication bandwidth than that possible with existing 64-bit/66-MHz PCI standard [19]. Finally, more work was done at the software driver level to demonstrate application-level message passing between computing nodes interconnected using ONICs.

2.2 High-Voltage Driver for Optoelectronic Devices

Recent advancements in research and development of Spatial Light Modulators (SLM) and Micro Electro Mechanical Systems (MEMS) devices find use in various applications such as optical correlators for optical processing, optical beam steering for avionic counter measures and input/output devices for memory systems [20] and [21]. The application requirements and technological advancements have enabled the devices to be designed and fabricated in large one-dimensional/two-dimensional arrays with increasingly shorter pitch between them. These requirements have pushed for very compact driver solution but with high-voltage drive capability. Commercially available high-voltage driver ICs only has a limited number of drivers in them and multitudes of these devices have to be used when driving huge arrays of Modulators and MEMS devices. Custom Complimentary Metal Oxide Semiconductor (CMOS) Very Large Scale Integrated (VLSI) circuit design is best suited for large arrays and compact solution.

Application demands for compact solution with little or no electrical parasitics or losses poses a challenge in using commercially available driver ICs. Also when the device array is large trying to drive them externally almost becomes

impossible with the number of electrical Input and Output (I/O) pads needed. On the other hand hybridization of the optical device on top of the active silicon helps in achieving optical device arrays in tighter pitch, larger array size and with less interconnects capacitances.

Technological advancements have enabled hybrid integration of VLSI ICs with two-dimensional arrays of Multiple Quantum Well (MQW) based Modulators, Photodetectors, Vertical Cavity Surface Emitting LASER (VCSEL), SLMs and MEMS devices [22] and [23]. These advancements will enable to integrate VLSI Integrated Circuits (IC) with millions of transistors and thousands of optical Input/Output operating at high-speed for various computing and switching applications. The important aspect in integration of the VLSI IC with millions of transistors with optoelectronic and MEMS devices is the efficient method of VLSI circuit layout methodology. The ability to integrate optoelectronic device arrays with optimized, high-density VLSI layout of RAMS and datapaths has been demonstrated by an efficient layout methodology. The optoelectronic devices used in these systems were low-voltage devices and so was possible to design VLSI circuits in deep sub-micron processes. With the above mentioned constraints a CMOS process technology that can support high voltage ranges and also smaller feature size needs to be chosen.

An efficient layout methodology is proposed in this dissertation to design and layout high-voltage drivers and the supporting digital logic. This needs to be done in a way so as to have both the high-voltage cells and low-voltage cells on the IC and still be able to partition and place them without breaking any design rules or cause fatalities to the driver IC. The proposed driver IC layout is explained in chapter 4. To verify the proposed layout methodology the design was implemented on a 1D array of

256 high-voltage drivers to be flip-chip bonded with a 1D array of 256 modulators. The IC integrated with the modulators will be used to steer Infra-Red (IR) beams for avionic countermeasures applications. The IC was fabricated in a wafer run using Austria Micro Systems (AMS) high-voltage CXZ process [24] and probe tested electrically.

Chapter 3

GIGABIT OPTICAL NETWORK INTERFACE CARD

The Optical Network Interface Card is an important instrument in demonstrating efficient application of architectures where high-speed optical data-links at data rates above 10Gbps are necessary. The purpose of the ONIC is to interface a standard computing node, such as a workstation or an embedded processor, with a VSR optical data link. On the hardware front, the ONIC converts slow, wide parallel and clock-synchronous data streams (typically used in chip-level computer interconnects) to narrow gigabit-speed data streams with embedded clock information (typically used in VSR optical data links). The ONIC hardware often contains First-In First-Out (FIFO) memory storage to buffer incoming and outgoing network data for flow control. On the software front, the ONIC includes software drivers to provide communication and flow control between the hardware, application running on the computing node and the custom network protocol used by the network that is being demonstrated.

3.1 ONIC Architecture

The architecture of the ONIC was developed in two phases. The first phase was to design prototype hardware with no compute node interface and high-speed electrical network interface. This evaluation prototype hardware was called Optical Network Interface Board (ONIB). The second phase was to design prototype hardware with the compute node interface and all optical network interfaces. A

generic architecture as the base for any ONIC design was developed to suit application requirements. The ONIC architecture developed at University of Delaware is shown in Figure 3.1. It is a PCI based Network Interface Card (NIC). It has a high-end re-configurable chip such as an FPGA that is programmed with the network protocols. The network interface of the ONIC is through an N-channel gigabit parallel optical link modules to transmit and receive data. The FPGA sends and receives the parallel data from the compute server to the optical modules through a set of SERDES. The SERDES converts the parallel data to high-speed. Serial data suitable for the optical module and recover the data and clock from the optical receive module.

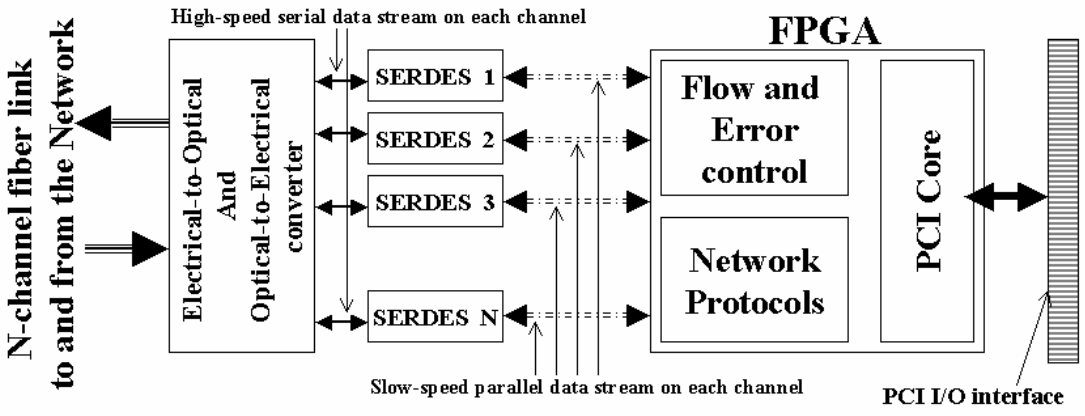


Figure 3.1 Generic Architecture of an Optical Network Interface Card (ONIC)

3.2 Optical Network Interface Board (ONIB)

The ONIB was designed to develop and test the protocols to be performed in the application. This was based on the generic architecture of an Optical NIC. However, the ONIB does not interface with any compute nodes. It has a high-speed

electrical interface. The architecture of the ONIB is shown in Figure 3.2. It has two Xilinx VIRTEX XCV1000 FPGAs. Each FPGA has 1 million system gates. One FPGA is to generate and transmit data. The second FPGA is to receive and process the received data. Each FPGA has two banks of Zero Bus Turnaround (ZBT) SRAM and the total memory capacity of the four banks combined is 8Mb (256k x 32bits). These SRAM are for buffering the transmit data and received data. The FPGA interfaces to three four channel SERDES S2065S from AMCC.

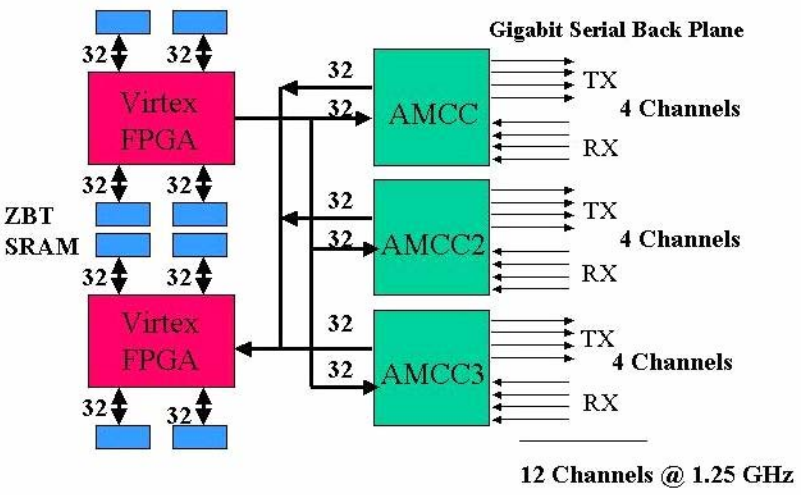


Figure 3.2 Architecture of Optical Network Interface Board (ONIB)

Each AMCC interface to both the transmit FPGA and receive FPGA through a 32bit synchronous line running at 100MHz each. Of each 32bit lines to the SERDES 8bits are assigned to every high-speed differential channel. Each AMCC can transmit and receive high-speed data at up to 1.25Gbps rate. The SERDES does 8b/10b encoding of the data when transmitting and 8b/10b decoding when receiving the data. The high-speed data to and from the SERDES is through MMCX connectors.

The ONIB was designed and fabricated using FR-4 based 8-layer PCB in January 2000. Many prototypes were fabricated for test and demonstration purposes. Figure 3.3 shows a picture of the fabricated and fully assembled ONIB.

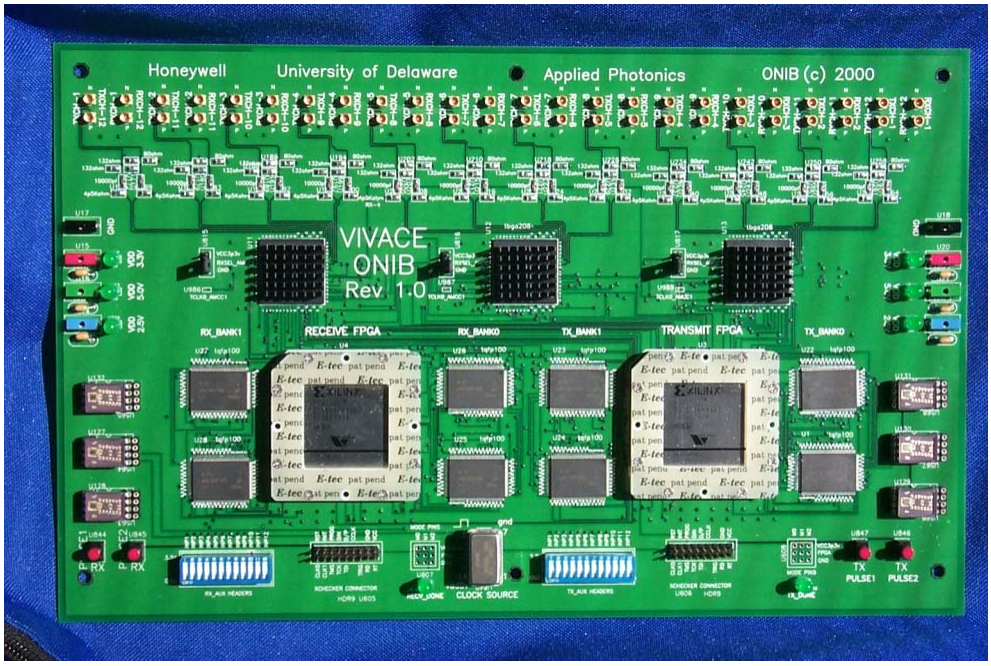


Figure 3.3 Picture of the fabricated Optical Network Interface Board (ONIB)

3.2.1 Optical Data Link modules

The optical data link to the ONIB is through two sets of 12-channel parallel optical data link modules. The optical data transmission is through a optical module that has a 1-Dimenisonal (D) array of 12 VCSELs. The Optical data reception is through an optical module that has a 1D array of 12 Photodetectors. The optical modules are mounted on two separate PCB with electrical interface through MMCX connectors. The transmit module and receive modules interface each other through a

12-channel optical fiber link. Each channel in the optical module has been tested to run greater than 1Gbps data rate. The ONIB interfaces to one optical transmit and one optical receive module for a full duplex connection between two ONIB to establish communication. With full duplex connection between two ONIBs the total bandwidth is greater than 24Gbps. This bandwidth is after 8b/10 encoding of the transmitted data. The optical data link modules with a parallel fiber link between them are shown in Figure 3.4.

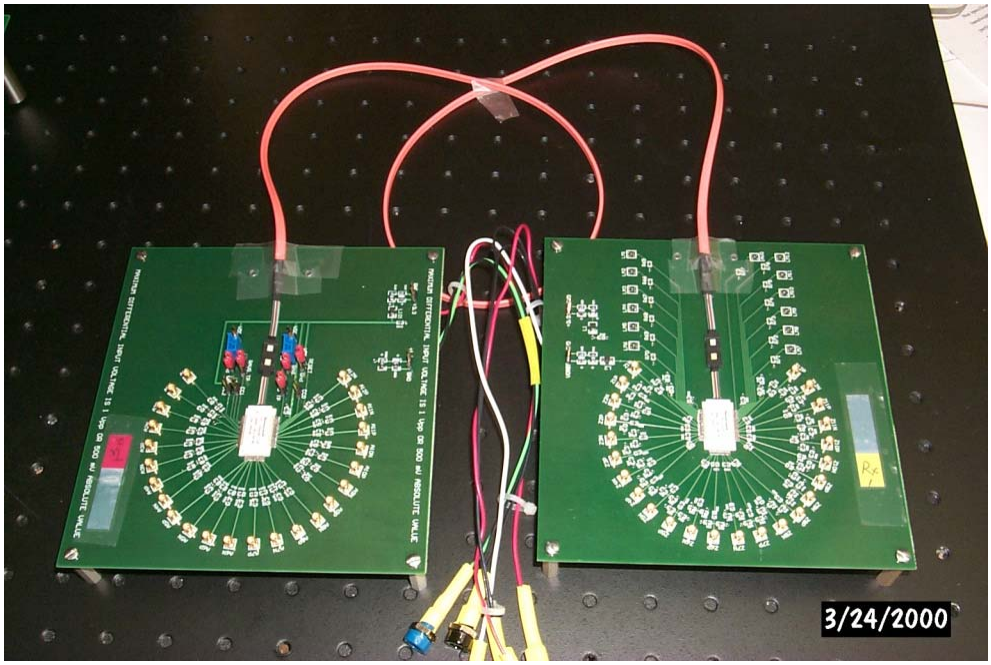


Figure 3.4 Twelve-channel Optical Transmit and Receive Data Link Modules

3.2.2 ONIB to ONIB Interface Demonstrator System

A demonstrator system was setup to interface two ONIBs through a 12-channel optical fiber link. The system setup is shown in Figure 3.5.

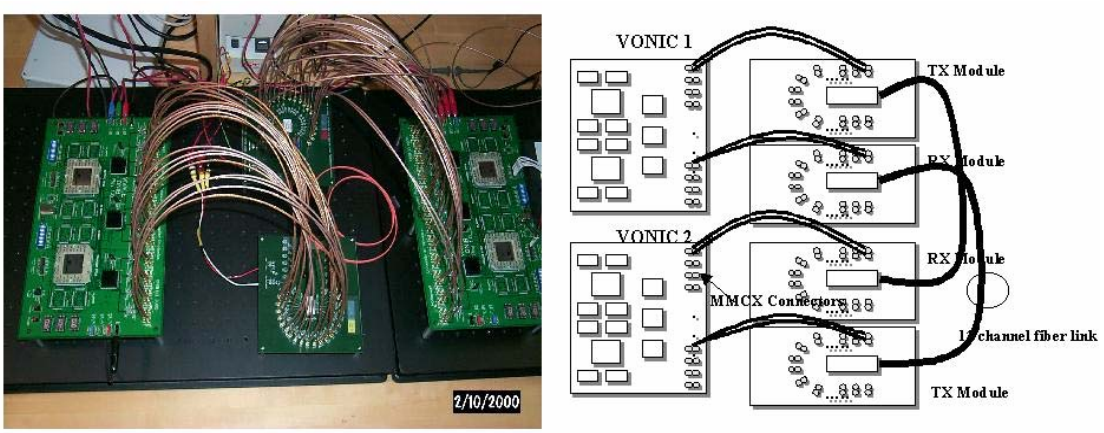


Figure 3.5 ONIB to ONIB Interface Demonstrator System using the 12-channel Optical Data Link

The schematic on the right of Figure 3.5 shows the system setup. Each ONIB is connected to one optical transmit and one optical receive module. The ONIB are connected to the transmit module and receive module through co-axial cables with MMCX connectors. The transmit module and receive module are connected to each other through two sets of 12-channel fiber ribbon. The picture of the system setup is shown on the left of Figure 3.5. It shows only one-way communication from one ONIB to the other. Since the high-speed lines are differential signals, the co-axial cables for establishing the two-way communication are clustered and difficult to debug. Even though the system was demonstrated for two-way communication as in the schematic of Figure 3.5, only one-way communication is shows to make the picture simple.

A link integrity test was performed to test the interface between the ONIB hardware. An algorithm for generating and transmitting the data was developed. Another algorithm to receive and process the data was developed.

Transmit Algorithm:

The algorithm for transmitting the data is configured onto the transmit FPGAs on both the ONIBs. The transmitting state machine is

State 1: Reset all three SERDES and run them at channel lock mode. This is done to synchronize all three SERDES and run them of a single clock source.

State 2: Run transmit test on all three SERDES separated by one clock cycle interval. The one clock cycle interval is to make sure there is no cross talk between the four channels in a single SERDES.

Transmit Test Program:

Step 1: Transmit synchronization characters K28.5 simultaneously on all four channels of each SERDES.

Step 2: Transmit 8-bit digital signature on every channel separated by one clock cycle interval. This indicates to the receiving ONIB that the data flowing immediately after the digital signature is real data.

Step 3: Transmit 8-bit Pseudo Random Bit Pattern (PRBS) test data on every channel separated by one clock cycle interval. It is a 255 non-repeating pattern generated using an 8-bit Linear Feedback Shift Register (LFSR) on the FPGA.

Receiver Algorithm:

The algorithm for receiving the data is configured onto the receive FPGAs on both the ONIBs. The receive algorithm is

State 1: Watch for error status bit for each SERDES and update the error counter to assess the bit error rate of the optical channel.

State 2: Report error if loss of synchronization occurs for each SERDES.

State 3: Run the test program.

Receiver test Program

Step 1: Establish word boundary in each data stream. This is done from the K28.5 characters transmitted by the transmit ONIB.

Step 2: Wait for the digital signature. Once digital signature is received it indicates that the data bits following the signature are real data.

Step 3: Receive and check the PRBS data received on each channel. This is done by starting an 8-bit LFSR with the same seed value as the transmit data and comparing the received data. Report any errors by asserting an error status bit and the error counter keeps track of the total errors.

On continuous operation of the demonstrator system with two ONIBs communication to each other a bit error rate was reported in the order of 10^{-16}. All twelve channels (full duplex) were tested at 900Mbps. The system was tested and verified for establishing sync between the transmit ONIB and receive ONIB at 1Gbps on all twelve channels. Figure 3.6 shows the oscilloscope snapshot of the data at 1Gbps rate in one of the channels.

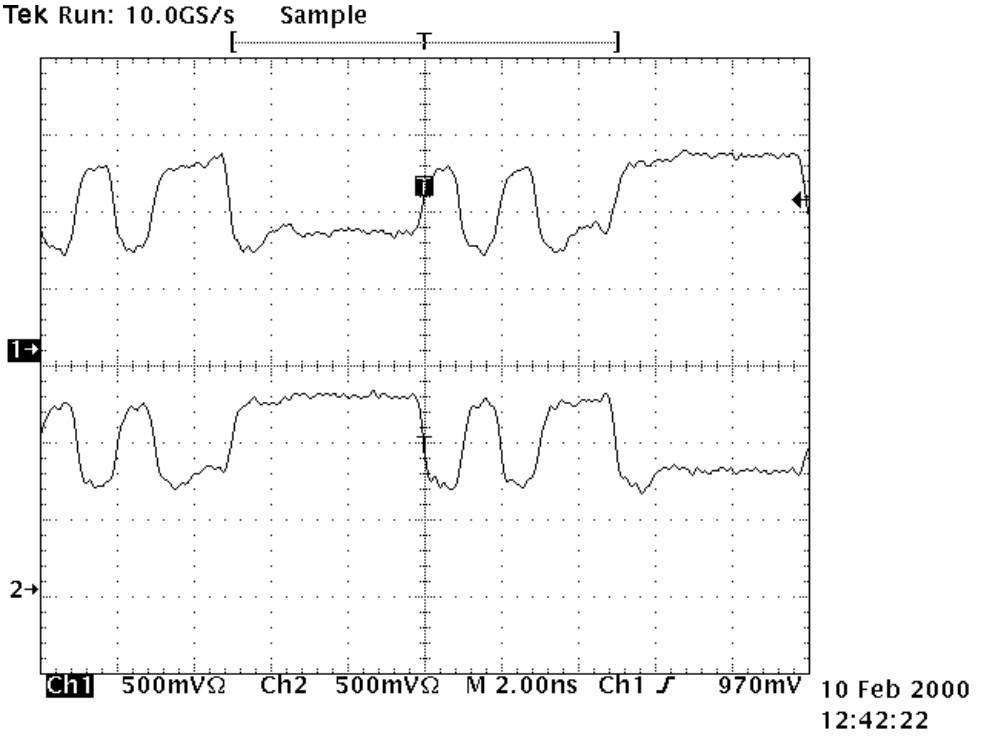


Figure 3.6 Oscilloscope snapshot of one of the channels transmitting data at 1Gbps data rates

3.3 Optical Network Interface Card (ONIC) design

The ONIC was designed using the generic architecture described in section 3.1. The schematic if the ONIC is shown in Figure 3.7. The communication between the ONIC hardware and the compute node is through the fast-wide PCI 64-bit/66MHz interface. The theoretical maximum bandwidth of the bi-directional PCI performance is 4.22Gbps half duplex. This was done as the PCI interface is widely used and the only option available to interface a NIC to a compute node when the card was designed [25], [26] and [27].

In the heart of the ONIC is an FPGA that has the network protocol and acts like a network processor. The advantage is it has the protocol defined by the user. The FPGA on the ONIC is a high-performance VIRTEX XCV1000 from Xilinx [28]. This FPGA is similar to the one used on ONIB. The whole network protocol can be implemented on to the FPGA and gives greater flexibility in modifying it. Parts of the FPGA resources on the ONIC were devoted to Xilinx PCI core. This is required for establishing communication between the ONIC and the compute node to which it will be plugged. The ONIC uses only one FPGA for handling both transmitting and receiving of the data.

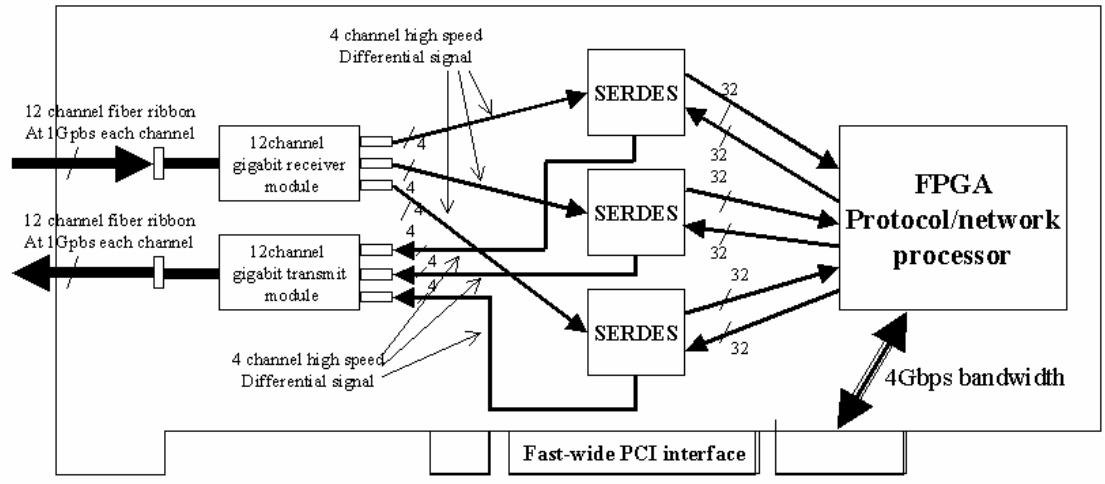


Figure 3.7 Schematic view of the components in the Optical Network Interface Card (ONIC)

The data from the FPGA goes to three AMCC S2065 quad channel serial back-plane SERDES. Each SERDES has a 32-bit slow speed input and output channels and four high-speed differential inputs and outs. Each of these high-speed

input and output channels can operate between 0.7Gbps and 1.4Gbps. The data to and from the compute server to the SERDES is fro the FPGA through the 32 input and 32 output data lines running between 70Mbps and 130Mbps. The SERDES on the transmit side does the 8b/10 encoding of the data. It generated K28.5 synchronization characters to establish communication with the destination node.

The high-speed differential signals from the three SERDES connect to a 12-channel gigabit parallel optical link driver and receiver module from Honeywell Technology Center. Unlike the ONIB the optical modules are placed on the Optical Network card itself. Each optical module couples to a 12-channel parallel fiber link. Each channel of this link has been demonstrated at 1.06Gbps giving the full composite parallel link a full-duplex bandwidth of 24Gbps. With the 8b/10 encoding/decoding of the data done by the SERDES at the transmitting and receiving ONIC to maintain signal integrity, the real full-duplex data bandwidth is approximately 20Gbps for each compute node the ONIC is attached to. The data from the optical receive modules is sent to the SERDES. The SERDES does data decoding, clock recovery and synchronization on the received data. The ONIC does not have any external memory as in the ONIB. The protocol uses the memory available on the FPGA for flow control.

The ONIC was fabricated using a standard copper and FR-4 PCB fabrication process. The PCB has eight layers of routing with full and split power planes. A picture of the fabricated ONIC hardware with all the components soldered to it in Figure 3.8. The PCI bus is designed to provide power to the PCI cards plugged into it. However the ONIC draws more power than the PCI bus can sustain. The three SERDES on the ONIC draws close to 10 watts of power. Hence the ONIC is powered

externally fro the compute server power supply. The isolation of power from the PCI bus ensures reliable power from the compute server without affecting the ability to add other system components on the PCI bus. The ONIC has onboard DC/DC converters to regulate the power to various components in it. The FPGA needs two power supplies: 3.3Volts for the FPGA I/Os and 2.5 Volts for the FPGA core logic. The SERDES also require 3.3Volts but draw more current than the FPGA. With this requirement three DC/DC converter circuits were implemented on the ONIC. The first power supply is to regulate FPGA 3.3Volts. Second DC/DC converter is to regulate FPGA 2.5Volts and the third to regulate 3.3Volts power supply for the SERDES and Optical link modules. All the three power supplies are generated from the 5Volts power supply of the compute server.

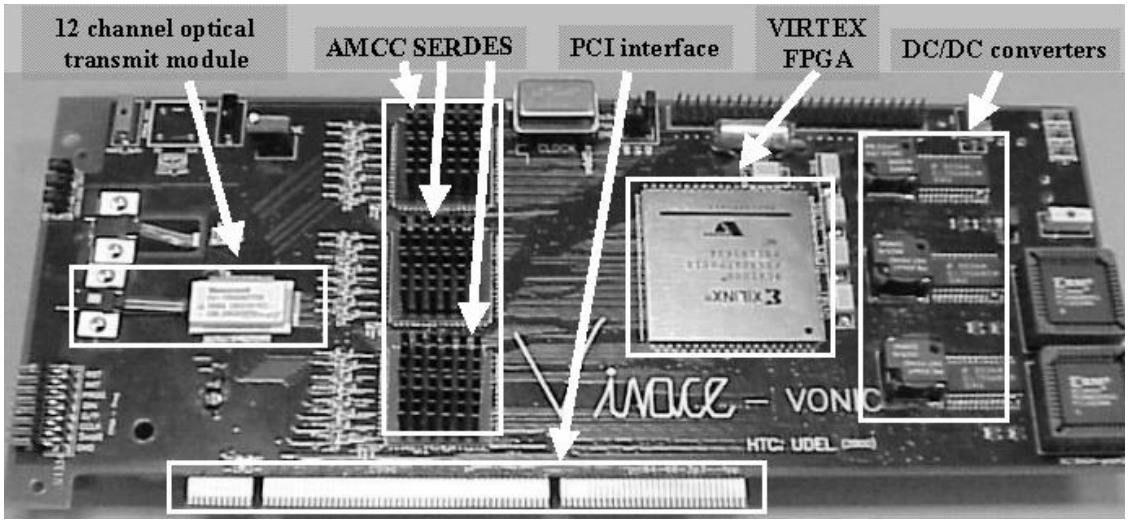


Figure 3.8 Prototype Optical Network Interface Card (ONIC) hardware with the whole card assembled

The parallel optical driver and receiver modules are located on either side of the ONIC. The transmit module is shown in Figure 3.8. The receiver module is attached on the other side of the ONIC and the fiber link comes through a cut out on the card. Differential transmission lines run from the SERDES to the optical transmit and receive modules. These lines are 50ohm impedance matched and they are located only on the outer layer of the ONIC. This was done to avoid multiple vias and the inherent problems associated with vias in transmission lines [29]. Figure 3.9 is a snapshot of the high-speed traces on the ONIC.

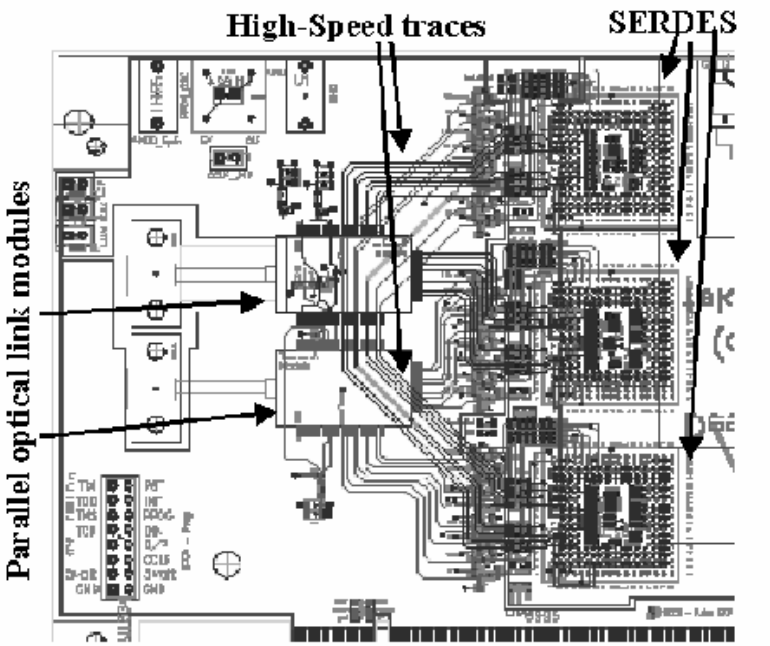


Figure 3.9 Snapshot of the 50ohm impedance matched transmission lines from the SERDES to the parallel optical link modules

3.4 Programming of the ONIC hardware

The design flow for the FPGA on the ONIC is described in this section. The design starts with a description of the protocol functional requirements. The functionality is then modeled using Very High Speed Integrated Circuits (VHSIC) Hardware Descriptive Language (VHDL) [30]. The design is further converted to register Transfer Level code. A behavioral simulation of the VHDL model is performed to validate functionality. On completion of the simulation, the VHDL model is synthesized to a netlist using tools from Synopsys. During synthesis the VHDL model is targeted towards the FPGA on the ONIC. This determines the resources that will be used on the FPGA and the timing. Once a netlist is generated it is simulated to verify functionality. Fig. 3.10 shows the steps involved in programming the FPGA with the protocols and IP core. Upon validation a bit file is generated for programming the FPGA. The bit file is loaded into a Programmable Read Only Memory (PROM) on the ONIC through a Joint Test Action Group (JTAG) interface [31]. Once the PROM is loaded with the bit file, it can be used to program the FPGA multiple times with the same functionality. When a new functionality needs to be implemented the steps described above are followed and the PROM is loaded with the new bit file.

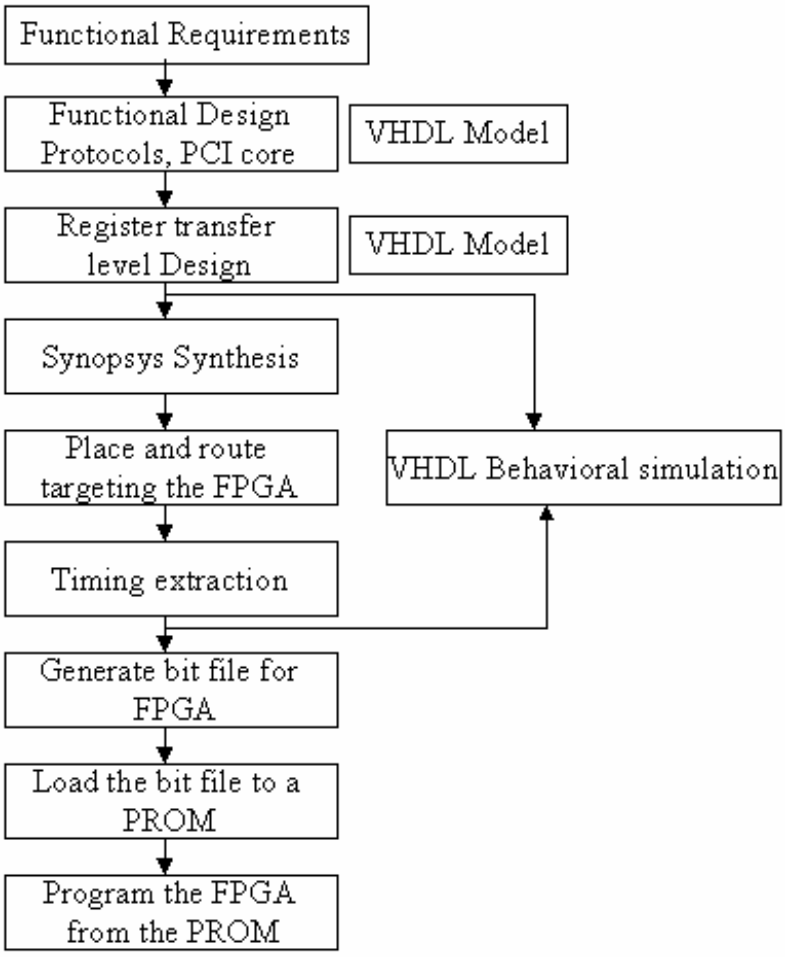


Figure 3.10 Design flow steps for the FPGA on the ONIC hardware

3.5 Test and results on the ONIC

The ONIC hardware was tested in two phases. A link integrity test for Bit Error Rate (BER) analysis and a message passing application was run to test the ONIC hardware. These tests were conducted by sending synchronization characters followed by a digital signature (data starting point). This is followed by the real data.

3.5.1 Link Integrity Test

The link integrity test was performed on the ONIC hardware for BER analysis. Initially, ONIC loop-back test was performed. Only one ONIC was used in this test. The parallel fiber ribbon from the transmitting optical module is looped back to the optical receiver module. The fiber ribbon was 1meter in length. The ONIC was plugged into the PCI bus of a compute server.

The FPGA of the ONIC was programmed with the test protocols and the PCI core. A 32-bit Linear Feedback Shift Register (LFSR) was used to generate Pseudo Random Bit Stream (PRBS). All three SERDES on the ONIC are controlled by the FPGA. Two of the three SERDES were run in sync with each other. The third SERDES was not used in the test. The K28.5 character for data synchronization between the two ONICs was sent on all four channels of each SERDES. After sending the K28.5 characters, an 8-bit digital signature was sent. This was followed by the same PRBS on both SERDES delayed from one another by a clock cycle. This data is encoded by the SERDES and sent to the optical modules. The data is then sent through the fiber-ribbon and is received by the receiver module. Figure 3.11 shows the steps involved in the link integrity test.

The data goes to the receiver optical module and is converted to electrical signals and sent to the SERDES. The SERDES waits for the K28.5 characters and when it recognizes the characters it synchronizes onto the oncoming data. The SERDES performs data decoding, recovers the clock from the data and sends them to the FPGA. The FPGA establishes the word boundary in the data stream from the K28.5 characters. It waits for the digital signature. As soon as the FPGA sees the digital signature it starts an LFSR with the same seed as the transmit LFSR. It compares the oncoming data with its LFSR data. A status bit gets asserted when an

error occurs. An error counter keeps track of the error from each SERDES. It also reports error on loss of synchronization in any of the SERDES. Fig. 3.12 shows a scope snapshot of the data through one of the high-speed channels at 1Gbps. The error count is communicated back to the compute server through the PCI interface and is continuously updated. The test was run for 30 days and we encountered no errors. The total bandwidth of optical data communication in this test was 8Gbps.

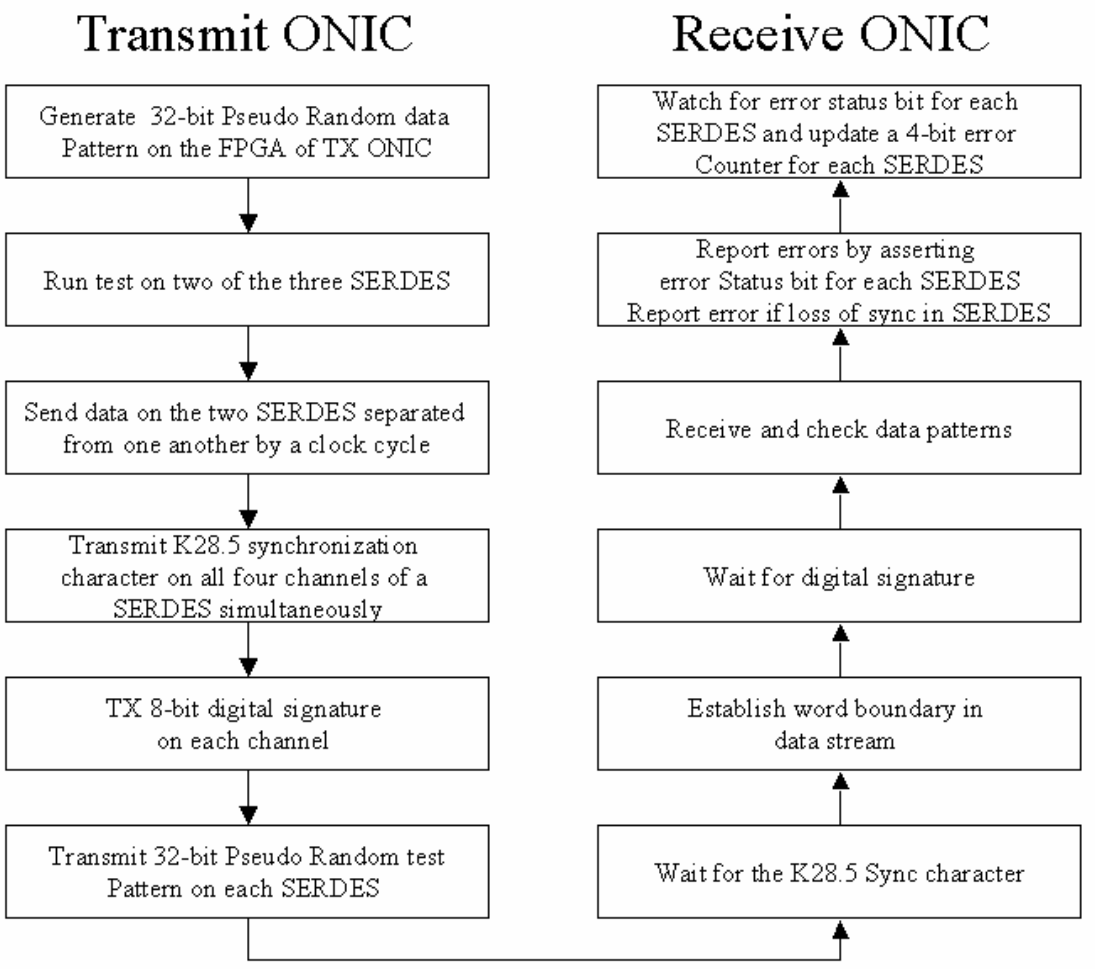


Figure 3.11 Steps involved in the link integrity test on the ONIC

The same test was repeated with two ONIC plugged onto two compute servers. One ONIC acts as the transmitter and the second ONIC as the receiver. The protocols were separated and the transmitting ONIC was programmed with the PCI core and the transmission protocol. The receiver ONIC was programmed with the PCI core and the receiver protocol. The length of the fiber ribbon used in this test was 1 meter. The test was run for 2 hours without any errors.

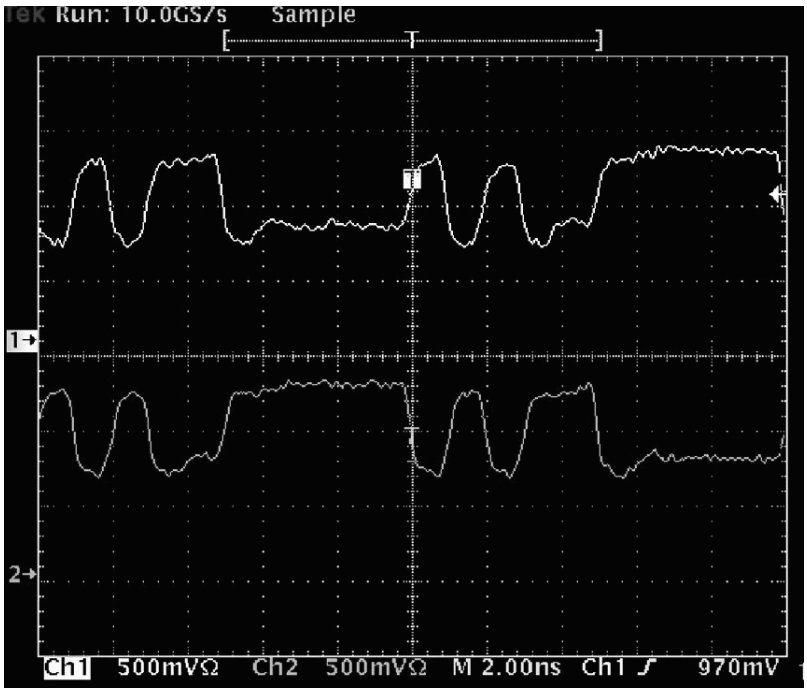


Figure 3.12 Scope snapshot of the data through one of the high-speed channels at 1Gbps

5.5.2 Message Passing Application

A message passing demonstration was performed to test application level communication between two ONICs plugged into the PCI bus of two compute servers.

They were connected to each other through a 12-channel fiber-link. Fig. 3.13 shows a picture of the two servers with ONIC hardware.

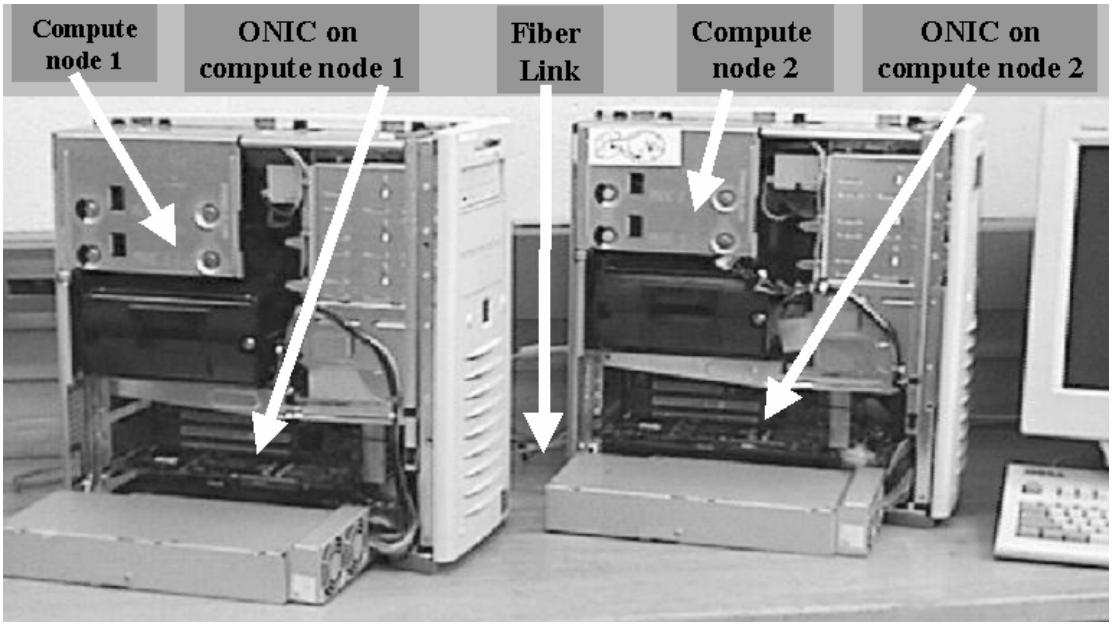


Figure 3.13 Message passing application running between two servers with ONIC hardware connected through a parallel optical fiber link

A custom software driver was written for the application to communicate with the PCI core on the ONIC FPGA through the PCI bus. The device driver was developed for Windows NT 4.0. The server uses the driver function calls to communicate with the ONIC.

The application itself was simply the transmission of characters typed on the keyboard of one compute server to another. To start the transmission the compute server announces to the ONIC to establish communication. The ONIC in turn, sends K28.5 characters to establish the link and continues to send K28.5 characters to

maintain the link. Each keyboard stroke is recognized by the driver, assigned a unique address (even if it is repeated) and sent to the ONIC through the PCI interface. The FPGA on the ONIC is programmed to recognize each character with its unique address. It sends it repeatedly to the SERDES until the next character with a different address is received for transmission. The SERDES 8b/10b encodes the data and sends it over the fiber link to the second compute server. Since the data bandwidth is very small compared to the bandwidth available, only one SERDES was used in this test. Figure 3.14 shows the steps involved in the message passing application test.

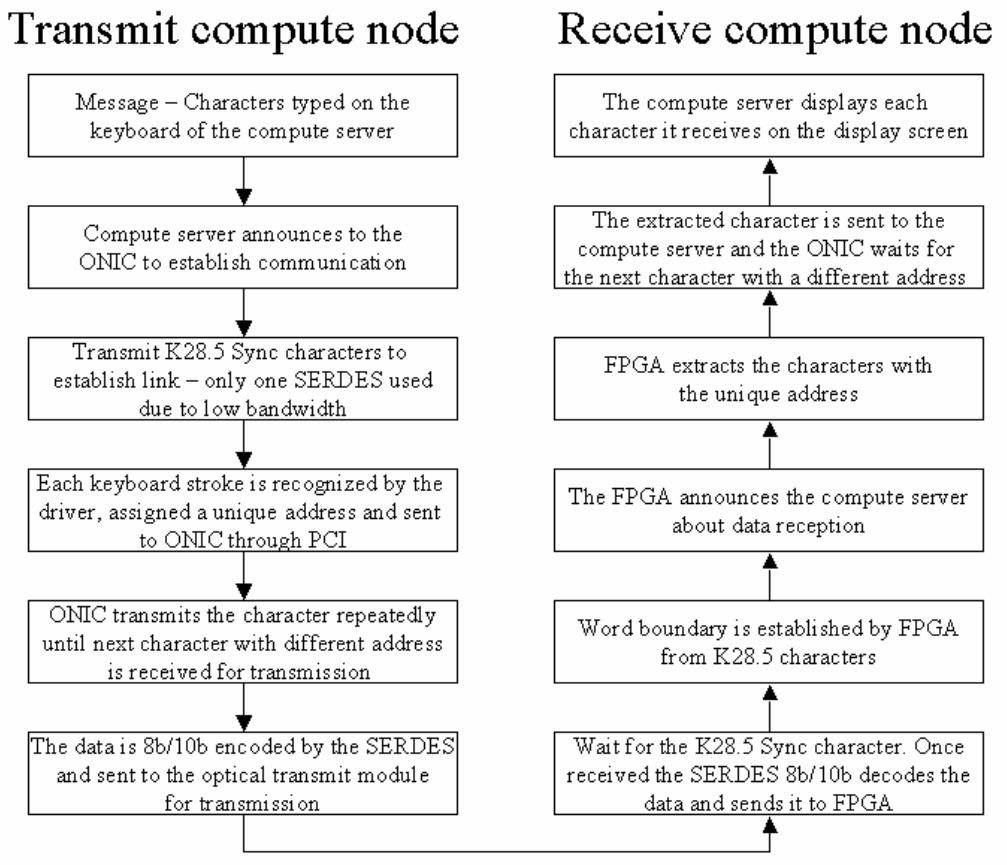


Figure 3.14 Steps involved in the message passing application test

The SERDES on the ONIC of the receiving compute server, 8b/10b decodes the data received. It recognizes the K28.5 characters sent to it and establishes a word boundary. The FPGA then waits for the data. As soon as it receives a new character with a unique address, it is sent to the compute server. The ONIC continues to monitor the received data. It sends the next character only when its address is different from the previous character received. Both the message sent and received was displayed on the respective display screens of the compute servers. With only one SERDES used in the test the application was run at 4Gbps bandwidth using only four channels in the 12-channel fiber ribbon.

3.6 Application of ONIC

VIVACE program stands for VCSEL based Interconnects in VLSI Architectures for Computational Enhancement. This is a Defense Applied Research Projects Agency (DARPA) funded VLSI Photonics program [32], [33] and [34]. This program is aimed at building a high bi-section bandwidth, free-space optically interconnected switch and to demonstrate it in a system of multiple compute servers in close physical proximity running a Message Passing Interface (MPI) based distributed algorithm.

The VIVACE demonstrator system will consist of eight compute servers interconnected by a high-speed Free-Space Optically Interconnected (FSOI) switch fabric [6], [35], [36], [37] and [38]. The system however can be scaled up to 128 nodes using the same design. Figure 3.15 shows the VIVACE system concept.

The heart of the VIVACE system is the FSOI switch built on a Multi-Chip Module (MCM) that will consist of a 4x4 array of VLSI CMOS chips heterogeneously integrated with large-scale 2D VCSEL/Photodetector (PD) array [13] and [22]. A

prototype FSOI switch fabric was built and demonstrated as part of the Free-space Accelerator for Switching Terabit Networks (FAST-Net) system [39]. Figure 3.16 shows the FAST-Net switch assembly.

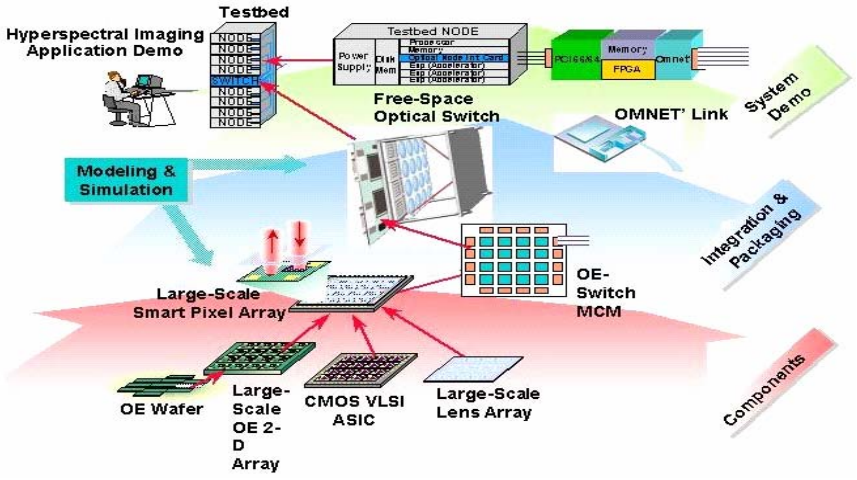


Figure 3.15 VIVACE system concept

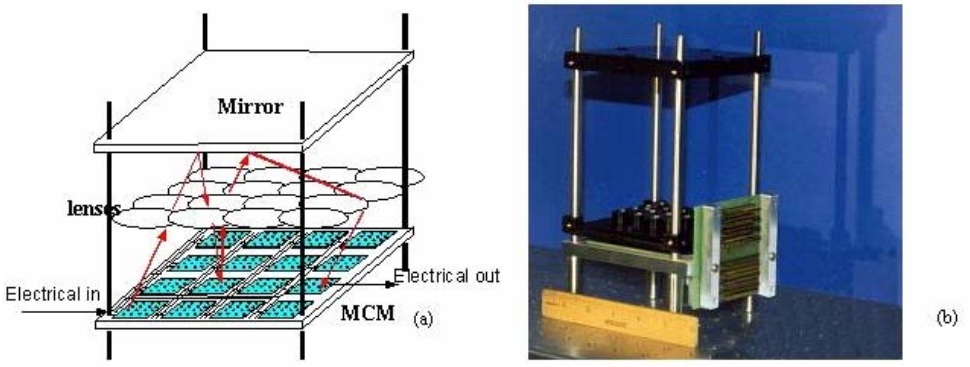


Figure 3.16 FastNet switch assembly. (a) Shows the Free Space Optical Interconnect (FSOI) switch concept, (b) Prototype FastNet FSOI switch assembly

The switch takes advantage of the tremendous bandwidth available through free-space for communication and utilizes high-density parallel gigabit optical links to communicate with the switch I/O ports. The capacity of the switch prototype is up to 128 ports. The bi-directional throughput of each port is from 2.12Gbps up to 12Gbps. The 128-port switch requires 16 2D smart-pixel chips (32 x 32 arrays of VCSEL/Photodetector pairs) for a total switch matrix size of 128 x 128. This amounts to a total bi-section bandwidth of 1.69Tbps (Tera bits per second) of the free-space interconnected switch [32].

Each of the compute servers in the VIVACE system will be interconnected with the FSOI switch though the ONIC using the parallel gigabit optical links. Custom protocols are being developed to communicate between the compute servers and the switch fabric. Figure 3.17 shows the schematic view of the VIVACE protocols.

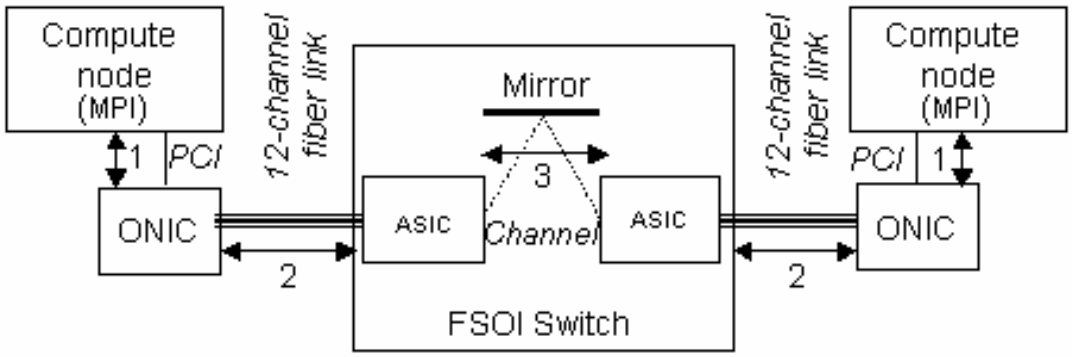


Figure 3.17 Schematic view of the VIVACE Protocol with communication from one compute node to another through the FSOI switch fabric

The protocols were developed for communication between the compute server and the ONIC, ONIC and the switch, switch and ONIC and from ONIC to the compute server. Also, foreseeing interconnecting more compute servers, communication between nodes on different switches was also considered. The protocols for intra-switch and inter-switch communication are not explained in this paper. The data received by the ONIC from the server through the PCI bus is at 64-bits/66MHz data rate. The FPGA on the other end of the ONIC communicates with the three SERDES on a 96-bit wide bus for data transmission and reception at 100Mb/s rate. The bandwidth discrepancy is fixed by using FIFO logic to convert the 64-bit data to 96-bit data and vice-versa. A flow control algorithm is being implemented to monitor the status of the FIFO and communicate to the transmitting ONIC to regulate the transmission accordingly. This helps in error control and data loss. The functions implemented on the FPGA are shown in Figure 3.18. The communication between the nodes is through a three-phase protocol.

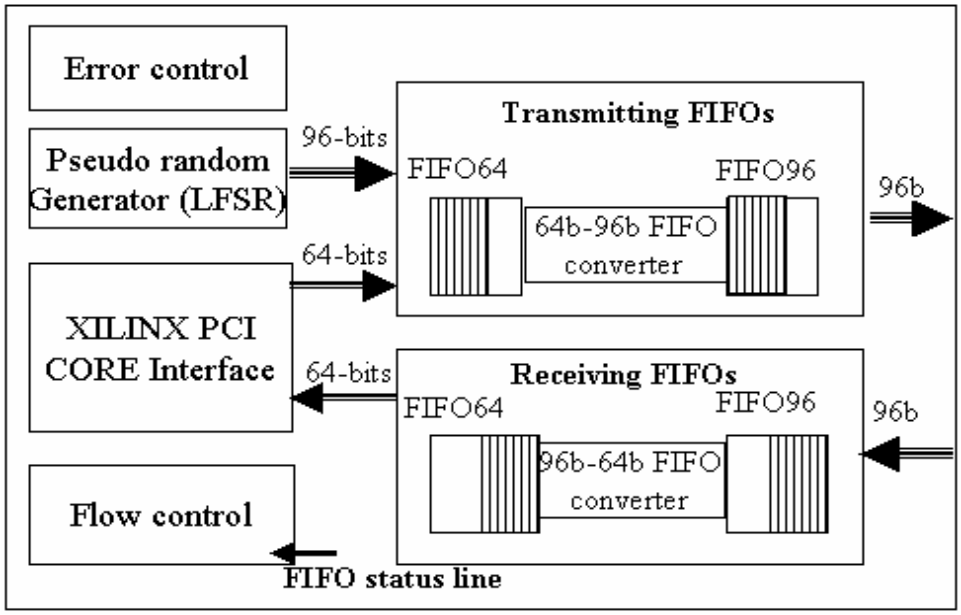


Figure 3.18 Functions implemented on the FPGA of the ONIC

3.6.1 Communication request protocol

In phase 1 Node A wants to establish communication with Node B to send a message. Node A initiates this communication by the sending a MPI call from the application. A control block with MPI TAG and MPI priority without the address of the application data (address 0) is created on the MPI memory of Node A. MPI then sends header information with the message length, memory address and the destination address to the ONIC. The ONIC examines the header and determines that there is no application data. It then reads the control block created in the MPI memory. The ONIC sends the header with the destination address, address where the message is to be written, source switch ID and port on source switch. It first transmits the header followed by the control block with the cyclic redundancy check (CRC) checksum. This request message negotiates through the switch and arrives at the destination node.

Figure 3.19 gives a schematic view of the communication between the nodes and the data format.

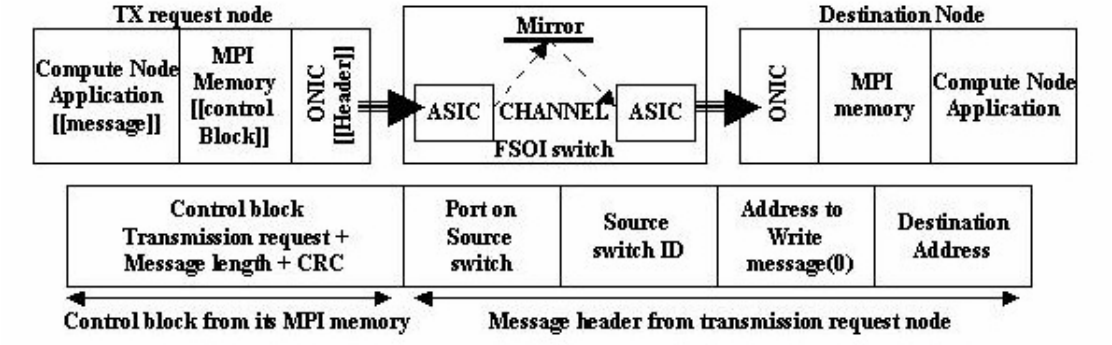


Figure 3.19 Communication request from Transmission request node to the destination node through the ONIC and FSOI switch

3.6.2 Communications response protocol

In phase 2 the ONIC on Node B receives the header followed by the control block. The header is examined by the ONIC and determines the message to be a communication request. It also does a CRC checksum on the received data. It then Direct Memory Access (DMA) writes the control block into the compute server MPI memory. The MPI determines that the message is a request and also destination address is necessary for transmission. It keeps track of the control blocks received to determine if the data associated with it was received. The MPI on Node B then waits for its application to send a control block to match the received control block. The MPI creates a control block for response with permission to transmit or no-transmit of data for the request from Node A. It creates a header and sends it to the ONIC. The

ONIC examines the header and determined that the message is without data and DMA reads the control block from the MPI memory. It then sends the header followed by the control block with a CRC checksum. Figure 3.20 gives a schematic view of the communication acknowledgement protocol.

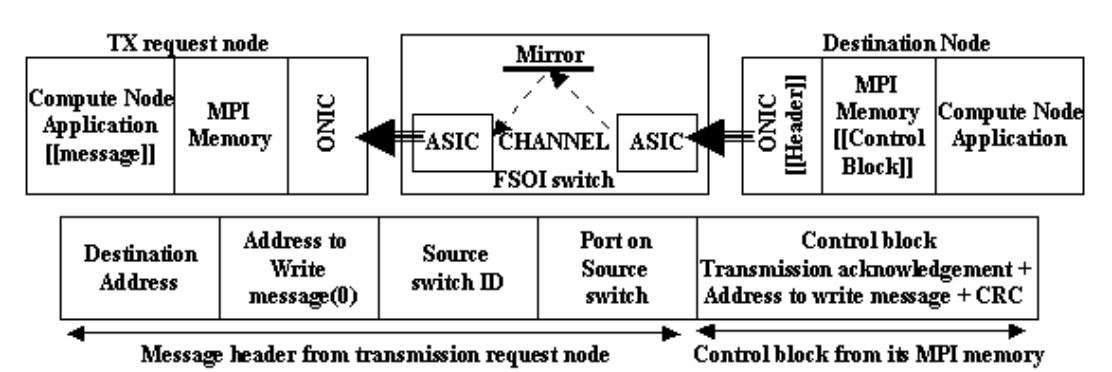


Figure 3.20 Communication response from the destination node to the transmission request node through the ONIC and FSOI switch

3.6.3 Message transmission protocol

During phase 3 the message negotiates through the switch and is received at the ONIC in the transmission request node, Node A. The ONIC examines the header to determine if there is data following the header. If not it DMA write the control message following the header to the MPI memory of Node A. The MPI examines the control block and finds it to be a response message. It matches it with the initial control message sent for transmission request. If the response is an acknowledgement for transmission request with the address for the message, the MPI creates a new control block to send the long application message. It discards the

previous control block and creates new header information with the address where the data needs to be written on the destination application memory.

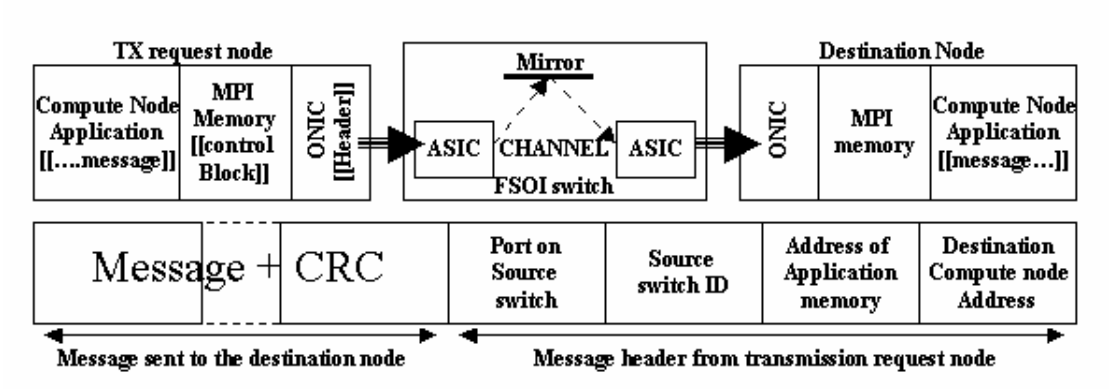


Figure 3.21 Message transmission protocol where the Transmission request node send the message to the destination node

The MPI memory in Node A's DMA, writes the header and control block to the ONIC. The ONIC examines the header and modifies it to include the destination address, address to write the memory, source switch ID and port on source switch. It now sends the header followed by the application data DMA read from Node A along with CRC checksum. The message arrives at the ONIC of Node B. The ONIC examines the header and the MPI memory writes the data to Node B application memory. The control block associated with this received message is discarded. Figure 3.21 shows the communication protocols involved in phase 3. Node A waits for a predetermined time and if it sees no response it assumes the message reached the destination node.

Chapter 4

LAYOUT METHODOLOGY OF HIGH-VOLTAGE DRIVERS FOR MODULATORS AND MEMS DEVICES

Optoelectronic devices are now designed and fabricated in large one-dimensional and two-dimensional arrays. They are then integrated on top of active silicon. The important aspect in integration of the VLSI IC with millions of transistors with optoelectronic and MEMS devices is the efficient method of VLSI circuit layout methodology. With the maturing of hybridization techniques the integration of optoelectronic devices on top of VLSI IC is becoming very popular. In the case of SLMs they are attached to silicon IC by flip-chip bonding process.

The process of placing the optoelectronic devices on top of active silicon is to reduce the interconnect capacitance associated between the transmitter/receiver circuitry to the optoelectronic devices. This inherently reduces the overall power consumption of interconnects, between the VLSI IC and the optoelectronic devices. This has become more necessary as the application demands have increased the speed of data processing to gigabit data rates.

Traditionally, the layout approach for designing a VLSI IC for optoelectronics based application is to create a smart-pixel cell. A smart-pixel cell is comprised of the Optical devices such as VCSELs, Photodetectors, MEMS or modulators, the optical driver/receiver circuitry and the electronic processing circuitry. This is then replicated in a one-dimensional or two-dimensional pattern to form a smart-pixel array [40], [41] and [42].

Application demands and a simpler system design have driver the optoelectronic devices to the fabricated using a rectangular array with a fixed pitch both vertically and horizontally. Then based on this application demand the smart-pixel array is replicated in the array. The approach for random placement and routing of the smart-pixel cells has not been considered in this research work, as the random approach might not fully utilize all the available smart-pixel cells in the IC.

Creating smart-pixel cells and smart-pixel array is very well suited for bit-serial processing of data. This however is not very effective when designing highly optimized RAM cells and bit-parallel datapath logic. The optimized cells do not use standard cells or regular routing in them. Changing the optimized designs to get the smart-pixel layout becomes a cumbersome task and would result in increased routing congestion and non-uniform timing. The problem becomes even more difficult as the optoelectronic arrays use a fixed pitch both horizontally and vertically.

SLM and MEMS devices for optical correlation and optical beam steering require high-voltage drivers with ranges up to 100Volts [43]. State-of-the-art CMOS process technologies have very small operating voltages. This poses a challenge in using low-voltage high-speed, deep sub-micron VLSI circuits. So, a sub micron process that can handle higher voltage ranges and also supports low voltage digital logic has to be used in designing the VLSI circuits.

4.1 Optical Device integration to Photonic ICs

The steps involved in designing and fabricating a smart-pixel IC is shown in Figure 4.1. The design process happens in two phases. First phase is the design and fabrication of the VLSI IC and the optoelectronic device array. The optoelectronic devices are fabricated according to application specifications and operation

characteristics needed for the application. This is the OE device array shown in Figure 4.1. The VLSI IC is designed according o the optoelectronic device pitch and device operation specifications. For every optoelectronic device the respective transmitter/receiver circuitry and processing circuitry is assigned and placed at the proximity where the devices will be attached. Next the contact point where the optoelectronic devices will be attached is specified in top layer metal with passivation opening on the VLSI IC. They are called area pads. In some application where micro lenses are needed they are designed and fabricated separately.

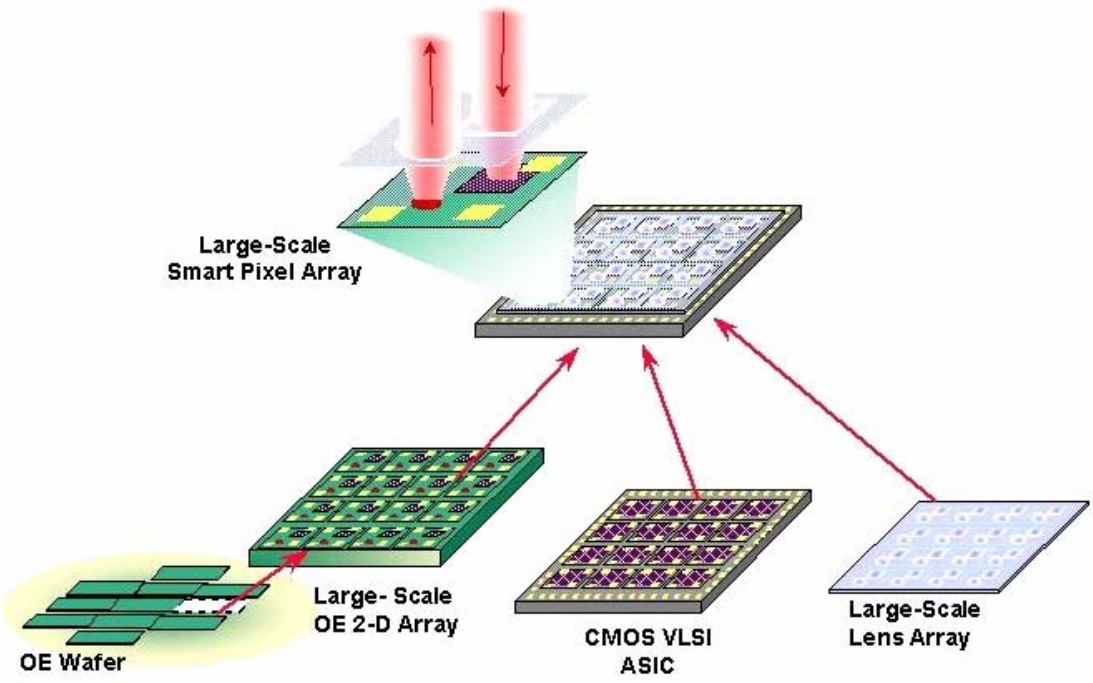


Figure 4.1 Steps involved in integration of VLSI IC with optoelectronic devices

The second phase is the integration of the optoelectronic devices to the VLSI IC. An example of how the optoelectronic devices are attached to silicon is

shown in Figure 4.2. Here the optoelectronic devices are attached to the VLSI IC by flip-chip integration process. As a first step in integration solder/Indium bumps are laid on the area-pads of the VLSI IC. Then the optoelectronic device array is flip-chip attached to the VLSI IC to complete the smart-pixel IC. The picture in Figure 4.2 shows the IC designed and fabricated as part of the FastNet program. The small bright lights in an array format from the IC are the VCSELs lasing.

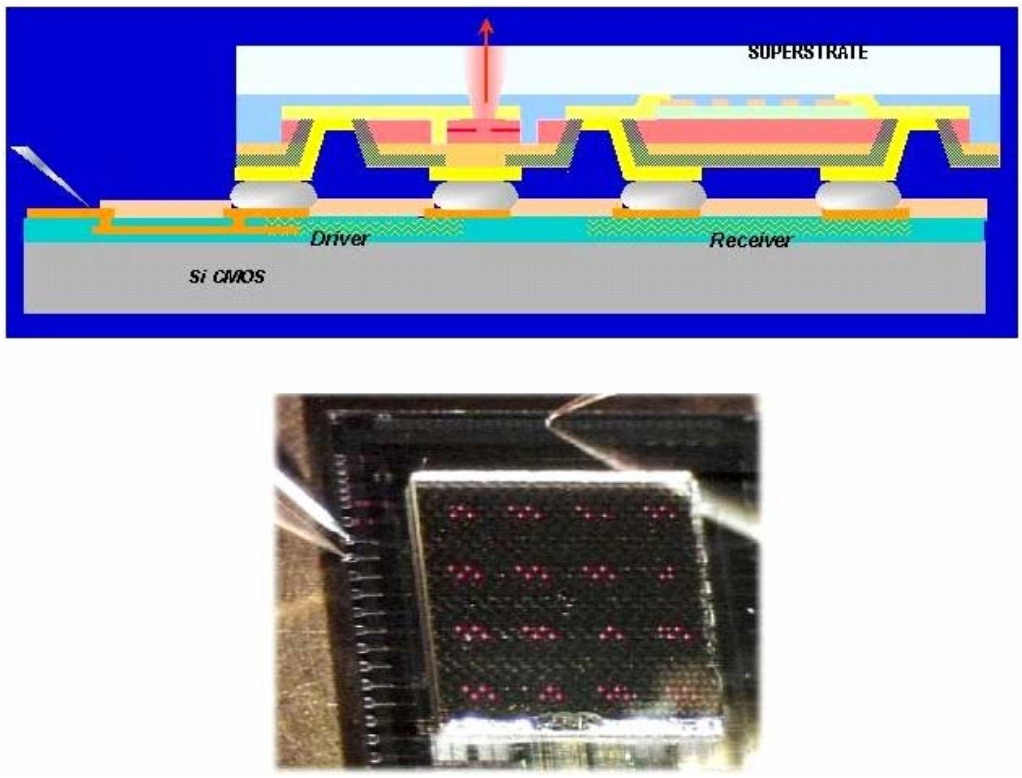


Figure 4.2 Flip-chip integration process, where the optoelectronic devices are fabricated separately and then flip-chip attached on top of VLSI IC with driver, receivers and processing logic

4.2 Layout Methodology

From the previous section it is very evident that the most important aspect is the efficient VLSI IC layout methodology. Recent advancements have enabled hybrid integration of VLSI ICs with two-dimensional array of MQW based modulators, Photodetectors, VCSELs and MEMS devices. These advancements will enable to integrate VLSI ICs with millions of transistors and thousands of optical input/output operating at high-speed for various computing and switching applications.

The ability to integrate optoelectronic device arrays with optimized, high density VLSI layout of RAMs and datapath elements is very important. Effective layout smart-pixel layout methodologies were proposed and were tested in implementing Photonic page buffers [40]. Typically these VLS circuits use datapath layout style that creates a regular row and column structure.

An example layout style is shown in Figure 4.3. Here the smart-pixel array of two types of circuit (VCSEL driver and Photodetector receiver) and are replicated in a two-dimensional array. It implements a 4 x 4 cluster with eight smart-pixels in each cluster. The optoelectronic devices were flip-chip attached to the VLSI IC. This chip had minimum processing logic and was placed and optimized at the bottom of the smart-pixel array [39].

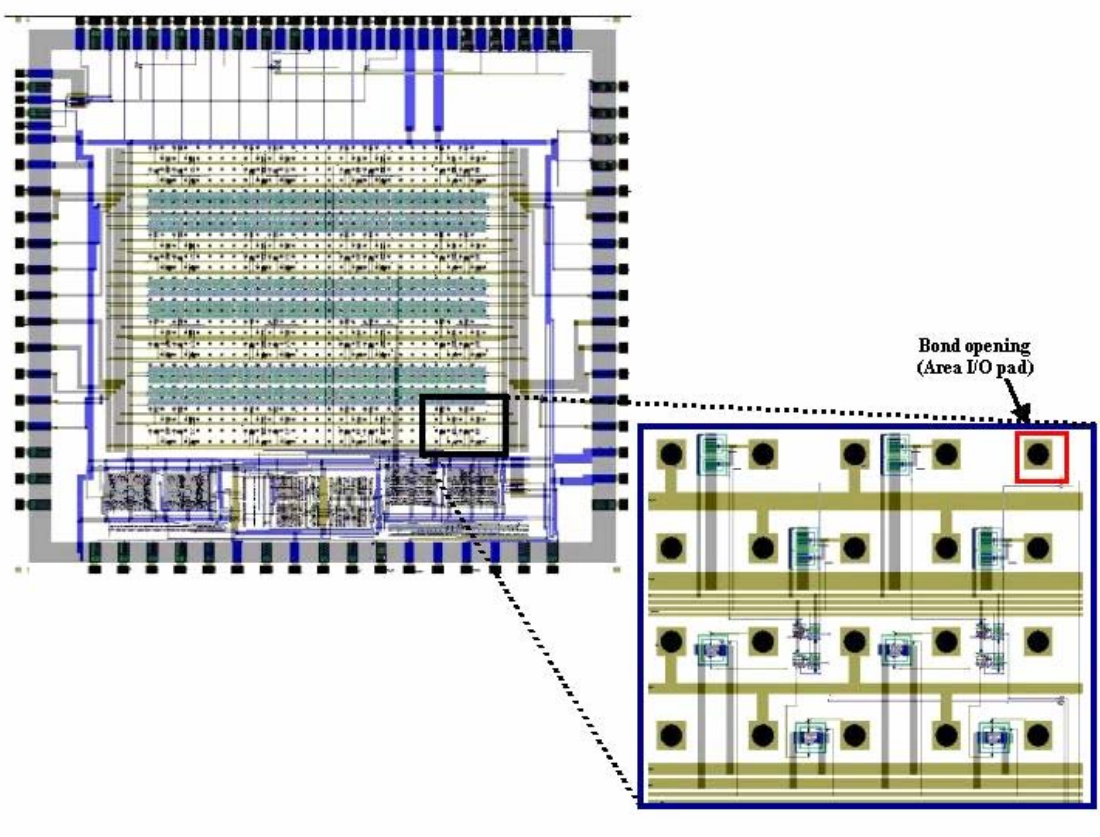


Figure 4.3 Example of a smart-pixel layout style where two types of circuit are replicated in a two-dimensional array is shown. The layout implements a 4 x 4 array of cluster with eight smart-pixels in each cluster. The optoelectronic devices were attached by flip-chip integration process

Another example layout is a high-speed CMOS scanner chip designed for it to be flip-chip bonded with MQW modulators. This chip includes an 85Kbit SRAM used as optical buffers and to scan data out through modulators at high translation speeds of up to 100MHz scan rates. The application of the design is analogous to the print head of a LASER printer for electro-photographic printing at high scan rates. The whole design can be viewed as a Photonic buffer module with the data entering

the IC electrically and scanned out optically. Although MQW modulator technology has been demonstrated over 1GHz modulation with 4096 I/Os. This particular design approach will be electrically limited by electrical parasitics. Figure 4.4 shows the layout of the CMOS scanner chip [44].

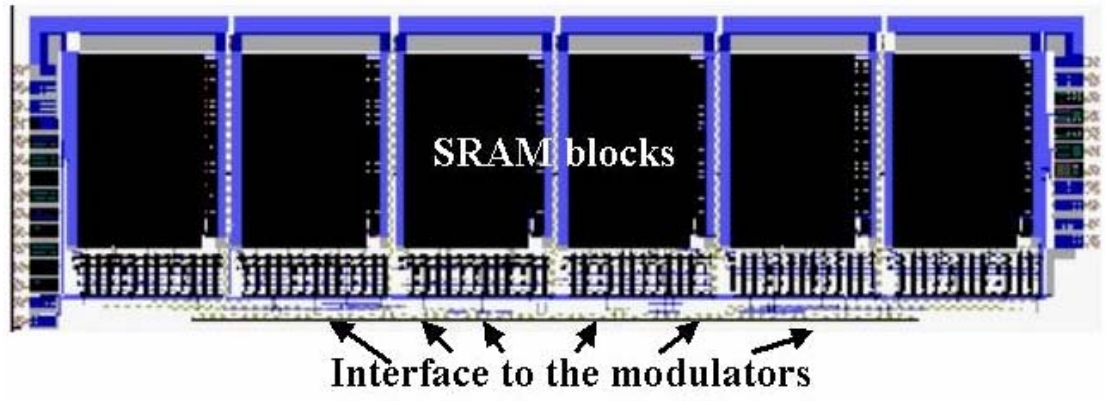


Figure 4.4 CMOS scanner chip designed for it to be flip-chip attached with 768 MQW modulators

The design has the SRAM block occupying the whole IC and the interface to the modulators is at the edge of the chip. The electrical parasitics is due to the long interconnect between the SRAM block and the interface to the modulators. Typically these VLSI circuits use a datapath layout style that creates a highly regular row and column structure. The datapath layout style is preferred for multi-bit processing circuits. These circuits achieve uniform timing for all the bits in a word and minimize routing congestion. Partitioning this circuit to fit the conventional smart-pixel array layout would result in non-uniform timing and increased routing congestion. Also the examples mentioned so far are operating at smaller voltage levels.

The proposed layout methodology is for designing large scale high-voltage smart-pixel IC that can efficiently integrate the optoelectronic devices to both high-density VLSI layout such as register based RAM, RAM, bit-parallel datapath and high-voltage circuits. This method allows the core logic of the chip such a RAM, datapath and driver circuitry (both low-voltage and high-voltage circuits) to be placed and optimized separately [40] and [45]. This method allows the optoelectronic device array to be placed directly over active silicon with the corresponding high-voltage driver circuitry.

The layout methodology is shown in Figure 4.5. Here the one-dimensional or two-dimensional high-voltage driver array structure is placed at the center of the IC. The array of the high-voltage driver array is called the High-voltage Photonic Driver Module (HPDM). The core logic is placed around the HPDM. With this approach the HPDM and the VLSI core logic are placed and optimized separately. Also the electrical interconnect between the core logic and HPDM is purely digital signals and can be buffered based on their respective lengths. The CMOS VLSI IC layout with this method is very effective for large high-voltage driver array driving optical devices. With this proposed layout approach future researchers can design custom VLSI layout for large optoelectronic device arrays top suit their application.

The layout methodology was applied to design and layout of a high-voltage CMOS driver IC to drive a one-dimensional array of 256 SLMs. The driver IC is targeted for Avionics Countermeasures application where a one-dimensional array of SLM devices is used for infrared rays beam steering application. A test chip was designed and fabricated prior to this IC for various circuit characterizations.

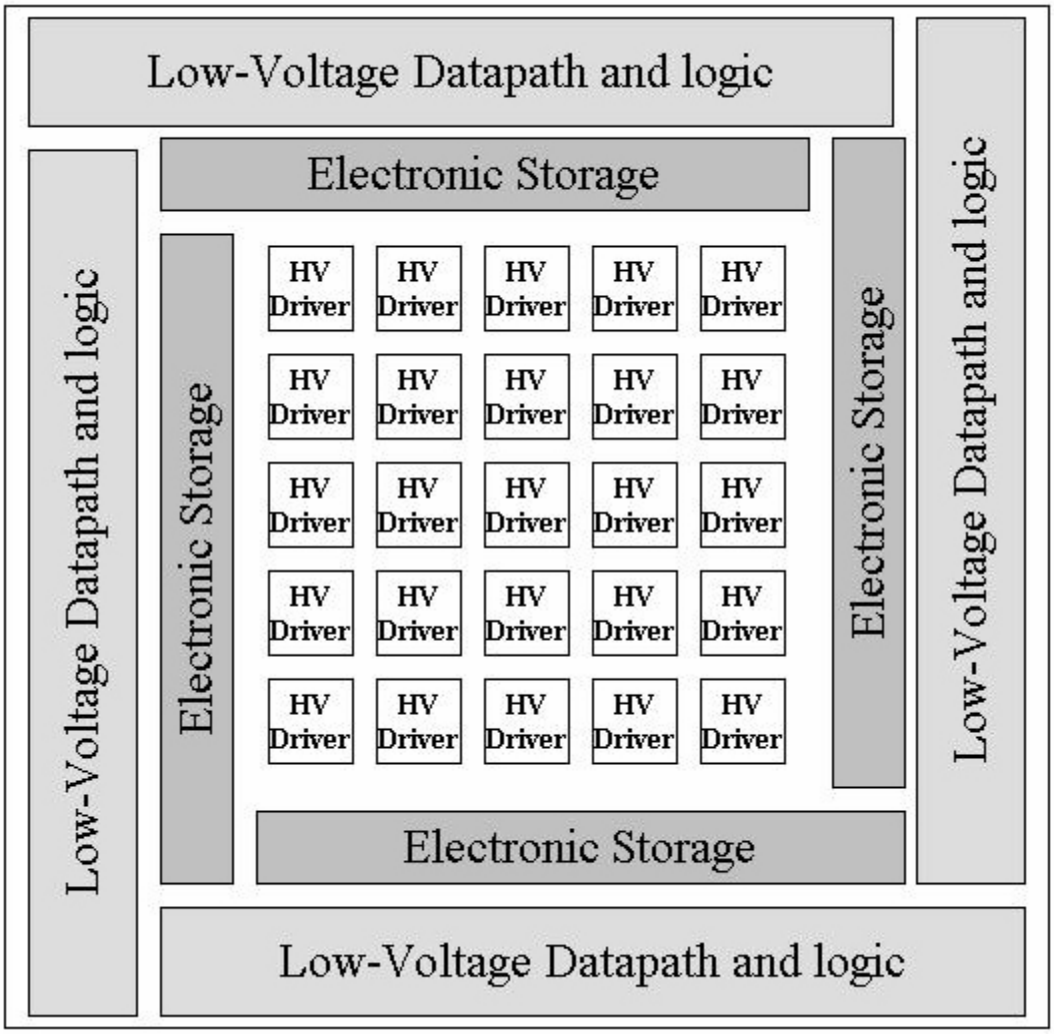


Figure 4.5 Layout Methodology for high-voltage drivers to drive MEMS and SLM devices

4.3 Application requirements of high-voltage driver IC

The high-voltage driver IC had to be designed with the following application requirements. Each driver cells needs to be able to generate arbitrary waveform and a CMOS integrated solution to reduce the overall size of the driver. The

output voltage range should be up to 50Volts with drive speeds in 10's of KHz. The driver IC should have 256 individual high-voltage drivers to drive one-dimensional array of 256 SLM devices arranged in a 13um pitch. The output of each driver needs to drive an area pad output that is 4mm in length. The challenges that are inherent with design requirements are the need for high-voltage drivers using CMOS. The high-voltage CMOS process requires larger feature size instead of using deep submicron CMOS processes.

4.4 High-Voltage CMOS test IC

The test chip was designed to build three high-voltage driver channels using standard library cells on a single VLSI IC. The chip was designed using 0.8um Austria Micro Systems (AMS) high-voltage (CXZ) CMOS process [24]. The size of the IC is 2.858mm x 3.65mm. Figure 4.6 shows the design of the test chip and the design of the high-voltage driver.

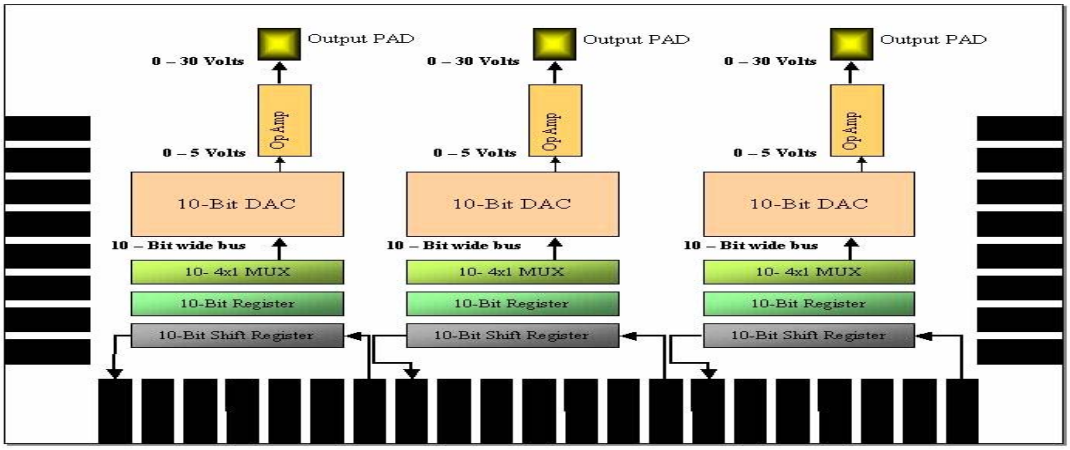


Figure 4.6 High-voltage CMOS driver IC and its functional blocks

Each driver cell is comprised of a 10-bit Digital to Analog (DAC) converter and an operational amplifier and drives an output up to 30volts. A 10-bit shift register is used to load the DAC input electrically on chip. A secondary set of shift registers is used to store the previous input of the DAC until a new input is loaded. All the components are from the standard library of cells from AMS. Figure 4.7 shows the DAC and the high-voltage operational amplifier. The dimensions of the DAC and operational amplifier are 185,000 μm^2 and 29,000μm^2.

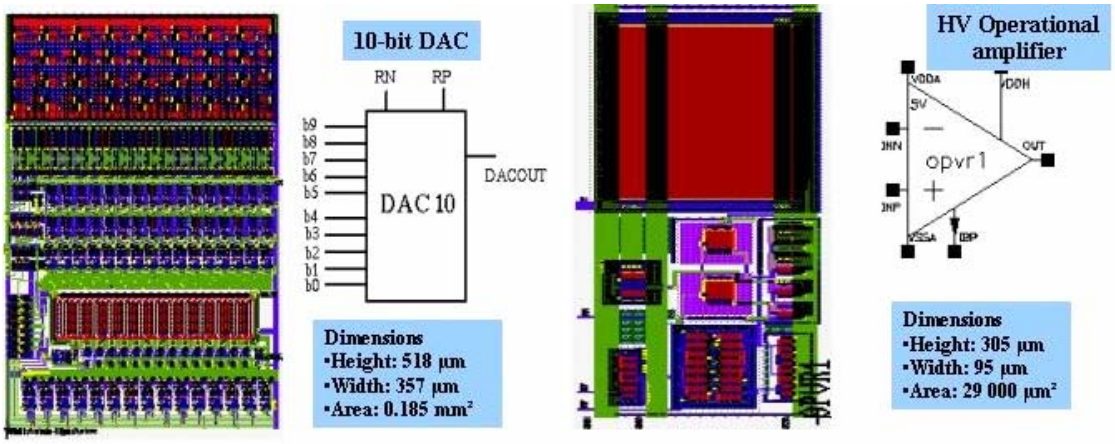


Figure 4.7 Layout of the DAC and the operational amplifier from the standard cell library

The layout and the fabricated high-voltage test IC are shown in Figure 4.8. Individual cells in the IC were tested and characterized. However, using the standard cells based driver posed a limitation when 256 of these drivers need to be arranged together and the maximum output range attainable is 30Volts. This is far less than the requirements of the application. So, a custom driver solution was designed to drive the SLM device array.

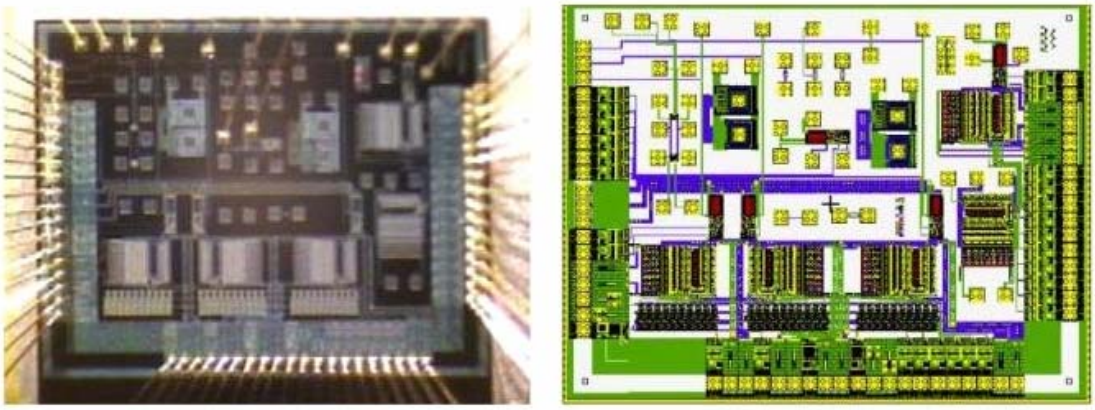


Figure 4.8 Picture of the fabricated high-voltage test chip is on the left of the figure. The layout of the IC is shown on the right of the figure

4.5 High-Voltage driver IC

The high-voltage driver IC was designed using the proposed design methodology with custom high-voltage driver. The IC was designed using AMS 0.8um CMOS (CXZ_ high-voltage process. It was designed so the drivers in the IC can be tested and characterized electrically before the SLM devices can be integrated with the VLSI IC [46].

4.5.1 High-Voltage driver design

Each high-voltage driver circuit is comprised of an 8-bit current DAC followed by a low-voltage current mirror circuit and then a high voltage section to drive the optical devices. The schematic of the driver is shown in Figure 4.9. Four versions of the driver were designed as listed in Table 4.1.

Table 4.1 Design versions of the High-Voltage driver

Driver Version	Maximum Voltage Swing	Current Draw by the driver	Load Capacity	Maximum speed of operation	Power consumption at maximum speed
50Volts	40Volts	0.5mA	5pF	125KHz	20mW
25volts	20Volts	0.5mA	5pF	250KHz	10mW
25Volts	20Volts	0.5mA	5pF	125KHz	5.0mw
12Volts	10Volts	0.5mA	5pF	125KHz	2.5mW

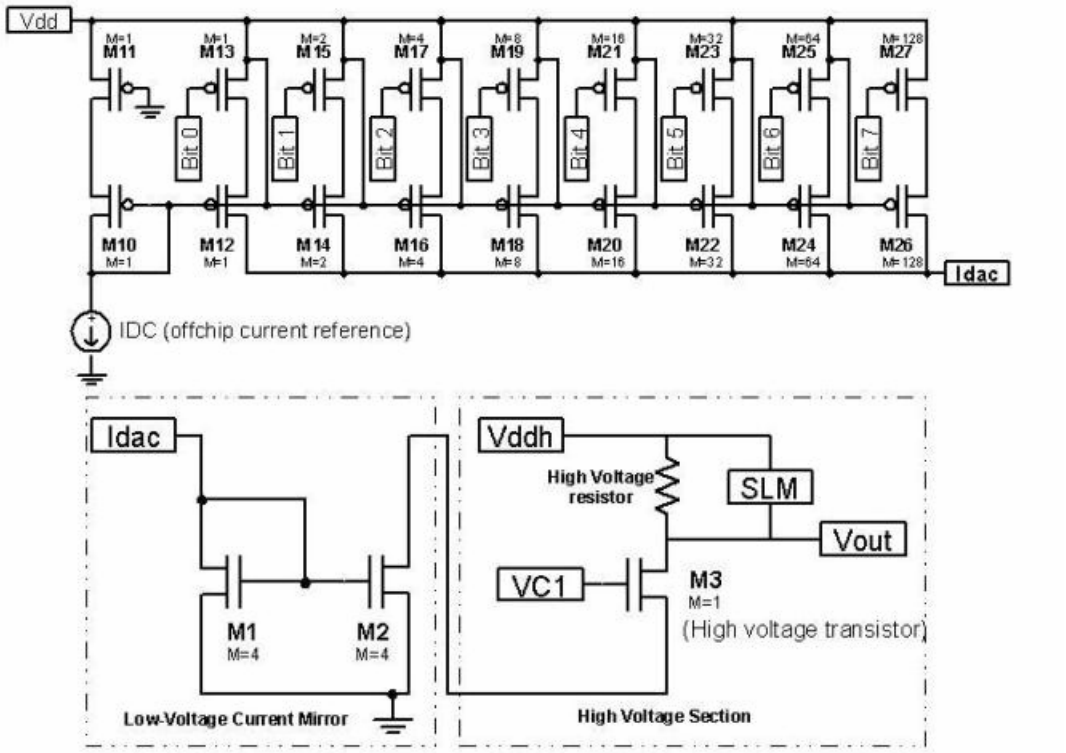


Figure 4.9 Generic Schematic of the high-voltage driver circuit. The 8-bit current DAC with off-chip reference current and the low-voltage current mirror followed by the high voltage section

The interface to the driver is an 8-bit digital input (bit 0 … bit 7) shown in the figure 4.9. The DAC uses 5Volts power supply. A 2uA off-chip reference current is provided as input to the DAC. Based on the digital input pattern the DAC multiplies the reference current input. The resultant current is available at the output Idac. This is then provided to the low-voltage current mirror. Based on the size and number of transistors in M1 and M2 the current is multiplied or divided to meet the output voltage requirements. The current output from the low voltage section is connected to the source of the high-voltage transistor M3. The high-voltage transistor gate is a cascode control input tied to 5Volts. Hence the transistor is always turned on. Turning off the gate input to M3 turns off the high-voltage transistor and any input to the optoelectronic device connected to it. The drain of the transistor M3 is connected to the high-voltage supply through a high-voltage resistor.

The current modulated by the DAC based on the 8-bit input pattern flows through the low-voltage current mirror and through the high-voltage transistor M3. This current through the high-voltage resistor defines the drop across the resistor and the resulting high-voltage output at Vout. The SLM device is a voltage steered device and is substituted with a capacitance of 5pF in value for simulation purposes. As mentioned in table 1 the four versions of the driver were designed and simulated to verify performance. The driver schematics and their respective simulation results are shows in the following figures.

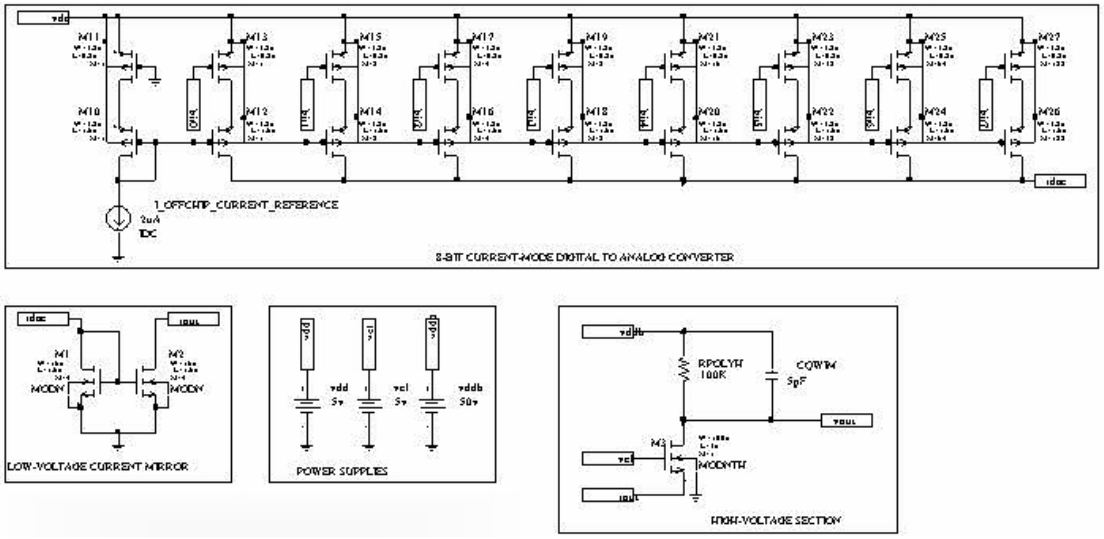


Figure 4.10 Schematic of the 50Volts driver

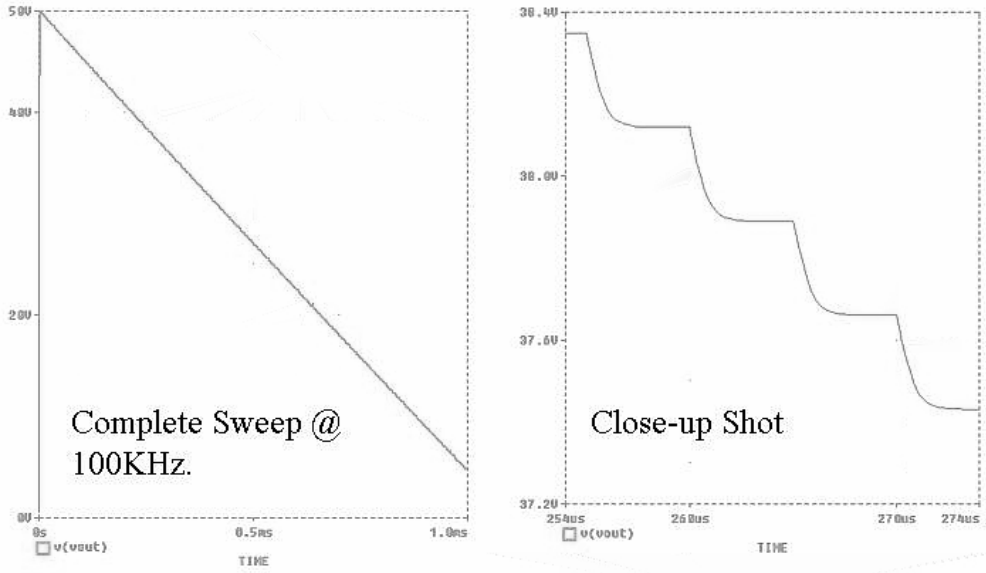


Figure 4.11 Simulation results of the 50Volts driver. The trace on the left is the complete sweep of the driver from 0Volts to 50Volts at 100 KHz. The simulation results on the right are the voltage step size with the change in the digital input sweep

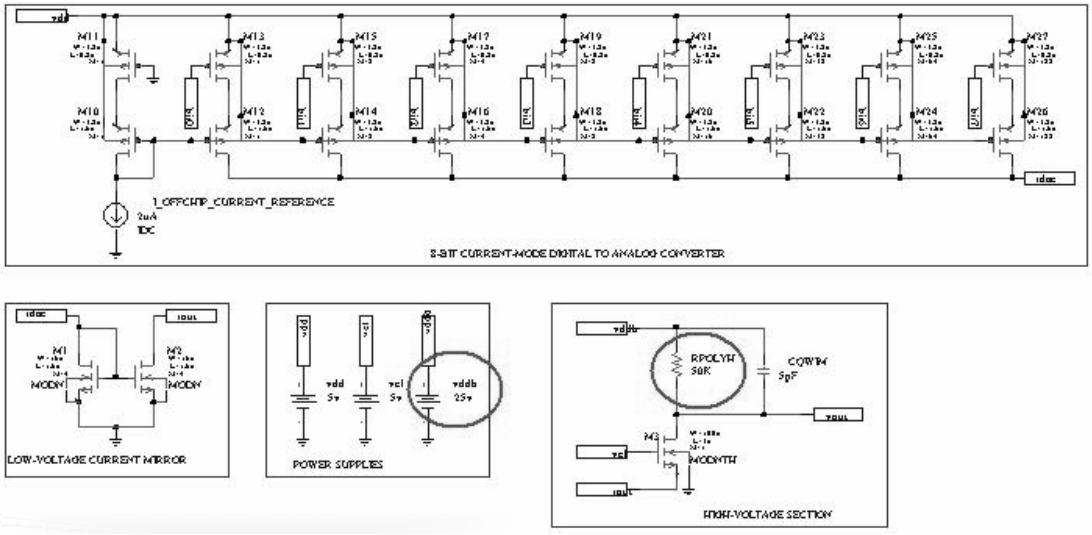


Figure 4.12 Schematic of the 25Volts driver with speed up to 250 KHz

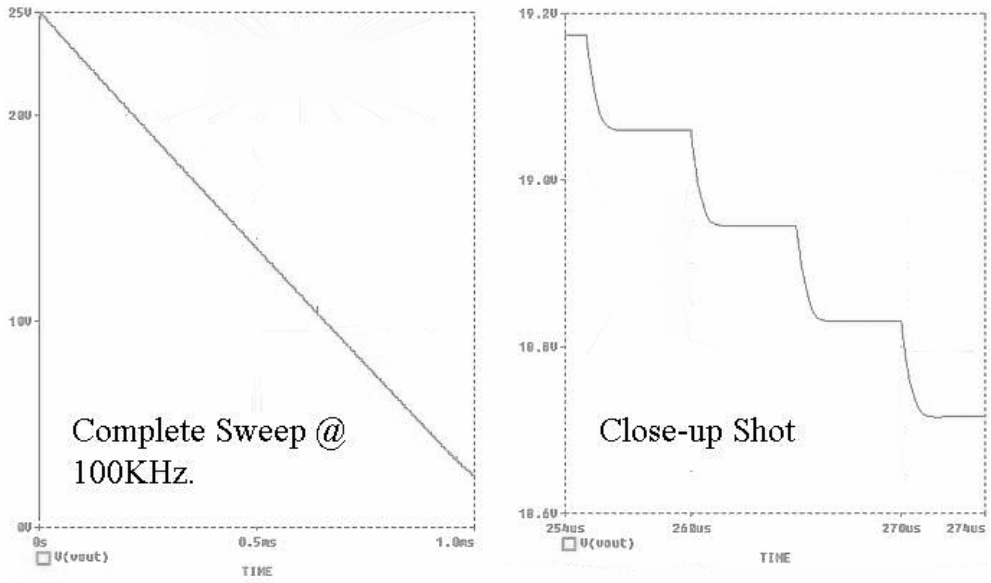


Figure 4.13 Simulation results of the 25Volts driver. The trace on the left is the complete sweep of the driver from 0Volts to 25Volts at 100 KHz. The trace on the right is the voltage step size with the change in the digital input sweep

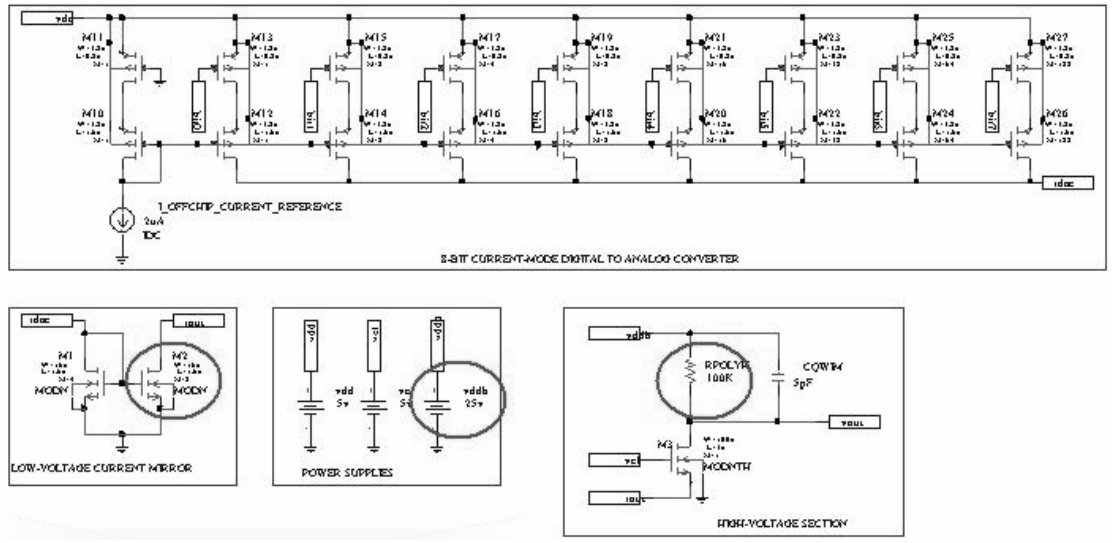


Figure 4.14 Schematic of the 25Volts driver with speed up to 125 KHz

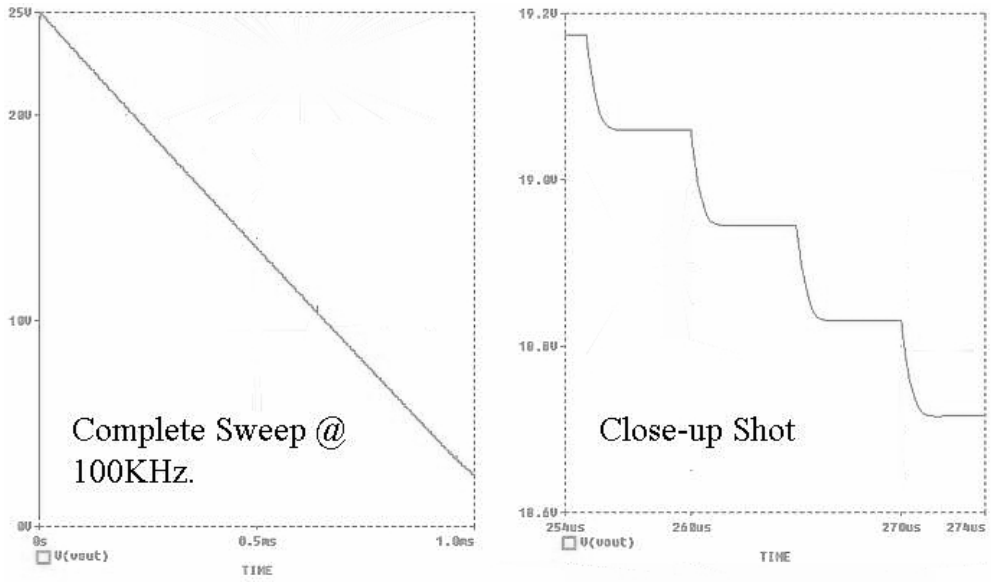


Figure 4.15 Simulation results of the 25Volts driver circuit are shown. The trace on the left is the complete sweep of the driver from 0Volts to 25Volts at 100 KHz. The trace on the right is the voltage step size with the change in the digital input sweep

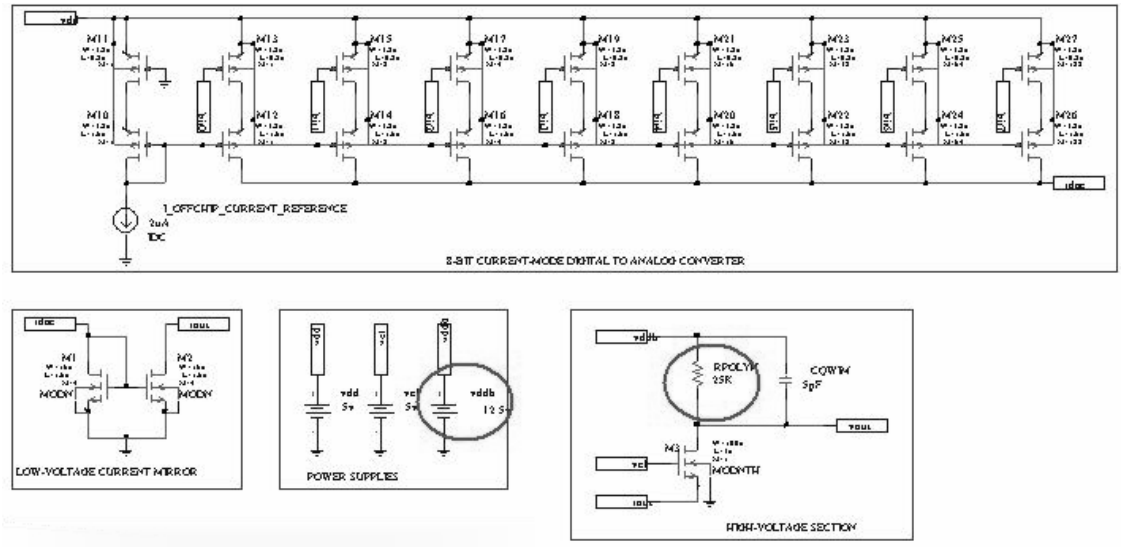


Figure 4.16 Schematic of the 12Volts driver with speed up to125KHz

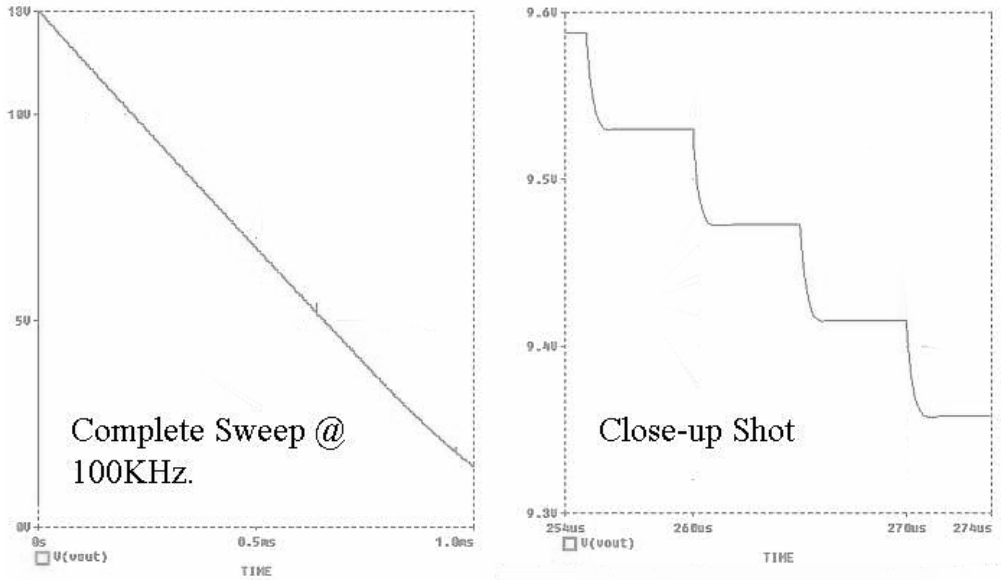


Figure 4.17 Simulation results of the 12Volts driver circuit are shown. The trace on the left is the complete sweep of the driver from 0Volts to 12Volts at 100 KHz. The trace on the right is the voltage step size with the change in the digital input sweep

4.5.2 Architecture of the driver IC

The high-voltage driver IC was designed based on the proposed layout methodology. Four versions of the driver were implemented on four different IC. This defined the maximum operating range of the driver IC. The application requirements for the electrical interface to the optoelectronic devices were considered in the architecture of the IC. The electrical contacts for each optoelectronic devices was a 4mm long top layer metal with passivation opening on top of it at regular intervals. The width of the metal structure was 7μm. A 1-D array of 256 of these metal lines was laid out with a pitch of 13μm.

The next step was to layout the high-voltage driver. Since the device pitch requirement was 13um an optimum height for the high-voltage driver was considered and the driver layout to fit under the long metal traces. This was done to reduce the interconnect capacitance between the driver and the optoelectronic device attached to the driver. With the driver cell optimized to fit under the metal trace the smart-pixel driver cell was in place.

The digital input to the 8-bit DAC was brought into the IC using an 8-bit shift register chain. D type registers with reset were chosen from the standard cell library for the shift-register chain. Eight registers were allocated to each driver. In addition to the eight registers another set of eight storage registers were allocated to each driver to store the previous value until a new value is scanned in to the shift register chain. Then the output from the 8-bit storage register is tied to the 8-bit digital input of the DAC.

The height of the register from the standard cell library was more than three times the height of the high-voltage driver cell. This was certainly a limitation in providing the input to the driver fro the shift-register and the storage registers. To reduce the interconnect wiring a novel approach was done. The high-voltage drivers were staggered in placement under the long metal traces. The scheme is shown in Figure 4.18.

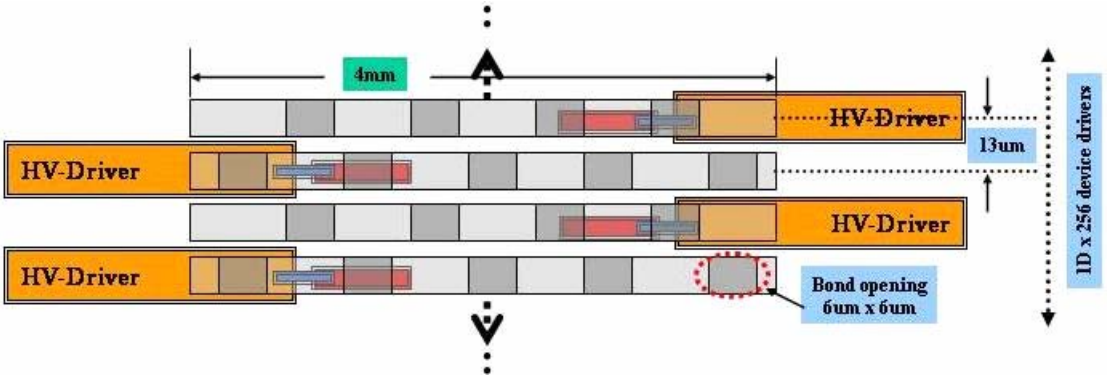


Figure 4.18 Layout of the high-voltage drivers with staggered placement under the top layer metal with 6μm x 6μm bond opening at regular intervals. The drivers are driven from left and right alternating

The high-voltage drivers are staggered I such a way that they have to be driver from wither side of the array. From the figure the first driver from the top of the array is driven from the right side and the second driver from the left is driven from the left side. Even with this scheme the height mismatch between the driver and the register was large. Re-designing the register to match the driver height was not considered, as it may not have the same performance as an optimized standard cell. As a compromise the shift registers and the storage registers for three drivers were arranged in a single row of cells. The layout scheme and the layout of the rows are shown in Figure 4.19.

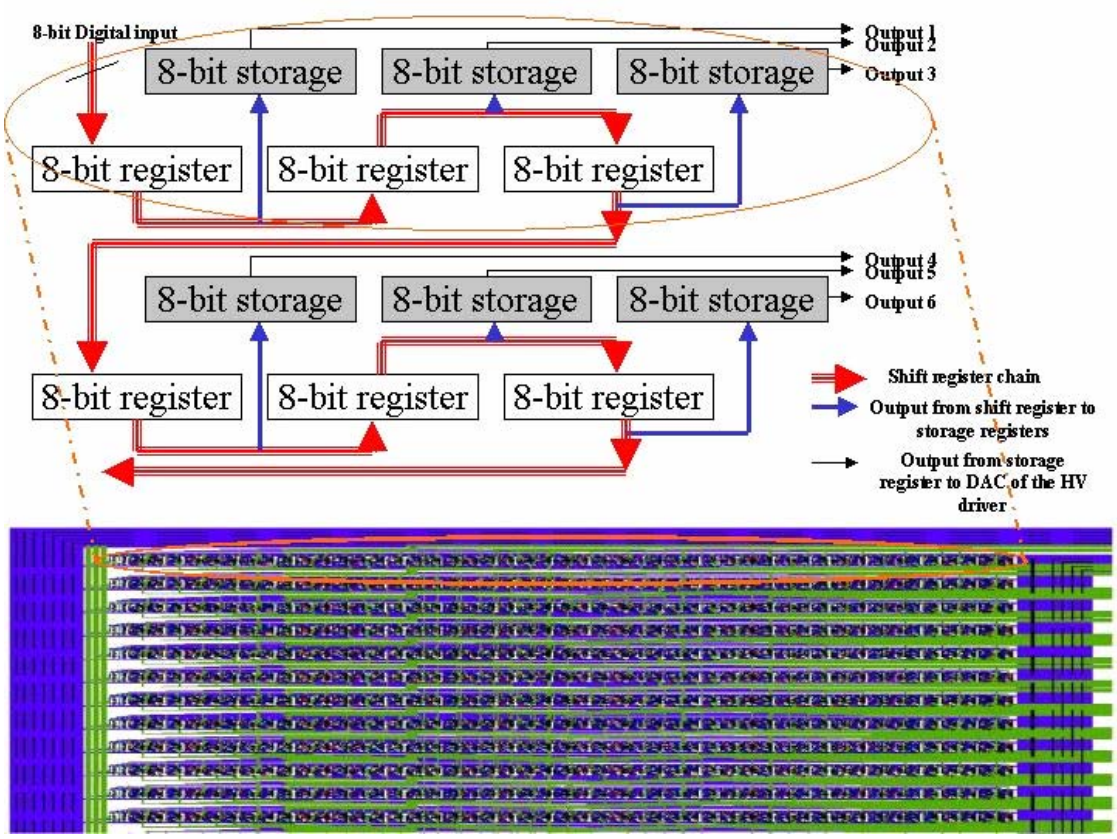


Figure 4.19 Layout scheme for the shift register chain and the storage registers

In the figure, the 8-bit digital data enter and goes to the first 8-bit register. The shift register is an 8-bit wide shift register of size 128. The way the data enter the chain and flows is shown in the figure. After 128 clock cycles the new set of data input to the high-voltage driver is available in the shift register chain. The storage registers are controlled by a load signal. At the end of the 128 clock cycles the load signal is asserted high and the values available in the shift register chain is loaded on to the storage registers. These values are for the drivers driven from left side. Similarly another set of 8-bit wide shift register chain of 128 and storage registers provide input values to the drivers from the right side. Thus in 128 clock cycles and

one load cycle the input to all 256 drivers can be scanned in. Also the input value that enters the chain is for the last driver and the last input value entering the shift register chain is for the first driver. The architecture of the driver IC is shown in Figure 4.20.

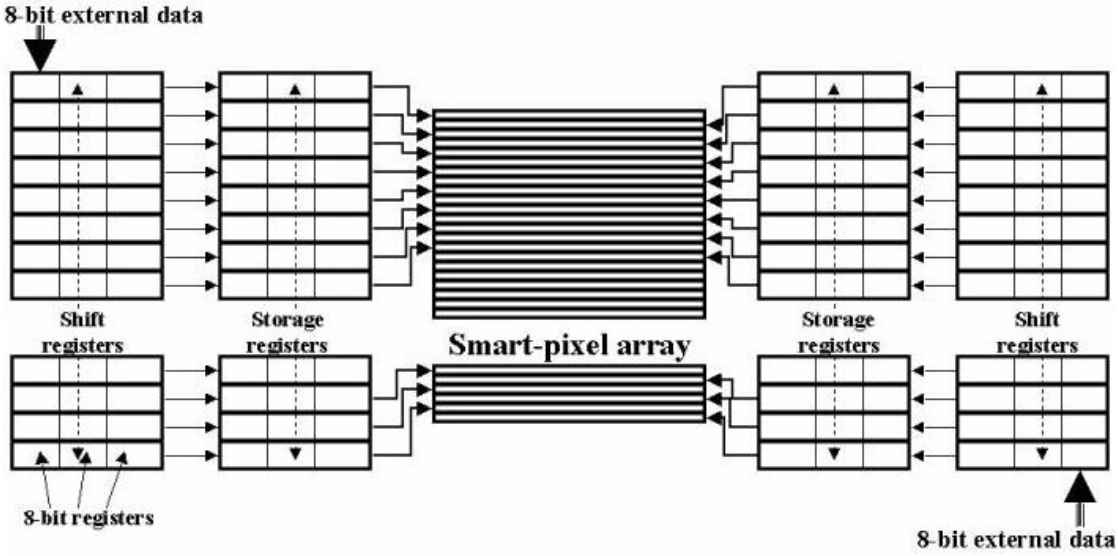


Figure 4.20 Architecture of the driver ASIC is shown with the smart-pixel array in the center. The storage and shift registers are on either side of the smart-pixel array

4.5.3 Layout and fabrication of the high-voltage driver IC

The IC was designed using AMS 0.8micron high-voltage CXZ process. The IC was laid out and designed for it to be flip-chip bonded with SLM devices. The application requirement was to have the IC tested fully electrically before optoelectronic devices are attached to it. This is to make sure the uniformity of the driver performance across the 1-D driver array is good.

To test the IC electrically, the output of every eight driver in the array was brought out to a probe pad. The size of the probe pad is the same as the size of the bond-pad at the periphery of the IC. This made up for 15 probe pads on either side of the IC. Also the digital outputs of the shift register chain were brought out to probe pads to verify that the chain is working. Figure 4.21 shows the edge of the IC where the probe pads are located for the high-voltage outputs and the digital outputs.

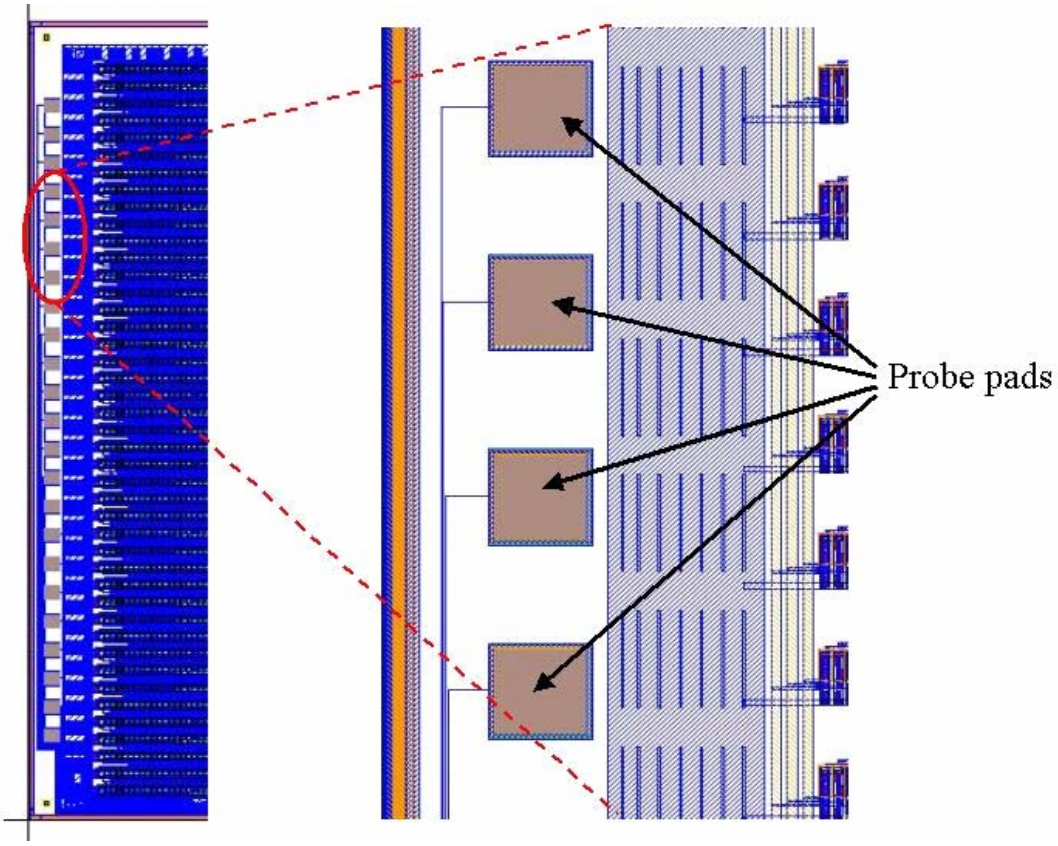


Figure 4.21 Probe pads on the edge of the IC to electrically probe the driver output using a probe card mounted on a probe station

The electrical input, control signals and the power supply pads were located at the top and bottom part of the IC. The input signals include the 8-bit digital input for the shift-register chain, digital clock, digital load and the digital reset mirrored on top and bottom edges of the IC. This is to provide input and control the drivers on either side of the smart-pixel array. A list of the pin assignments on the IC is given in Table 4.2.

Table 4.2 List of the Input, Output and power pads on the high-Voltage driver IC

PAD NUMBER	PAD DESCRIPTION	AMS PAD TYPE	VOLTAGE RATING	CURRENT RATING	INPUT CAPACITANCE IN
1	Digital core ground	PP03P*	Ground		
2	Periphery VSS	PP05P*	Ground		
3	Periphery VDD	PP06P*	5 volts		
4	Digital core VDD	PP04P*	5volts		
5	Digital Input 7	IB15P*			1.829
6	Digital Input 6	IB15P*			1.829
7	Digital Input 5	IB15P*			1.829
8	Digital Input 4	IB15P*			1.829
9	Digital Input 3	IB15P*			1.829
10	Digital Input 2	IB15P*			1.829
11	Digital Input 1	IB15P*			1.829
12	Digital Input 0	IB15P*			1.829
13	IDC	IOA2P*		2uA	3.8
14	DAC gate input	IOA2P*	Ground[*1]		3.8
15	Digital VDD for DAC	PP04P*	5 volts		
16	Ground for LVCM**	IOA2P*	Analog ground		3.8
17	HV transistor gate input	IOA2P*	5 volts[*2]		3.8
18	SLM device ground	PP03P*			

PAD NUMBER	PAD DESCRIPTION	AMS PAD TYPE	VOLTAGE RATING	CURRENT RATING	INPUT CAPACITANCE IN
19	Periphery VSS	PP05P*			
20	Periphery VDD	PP06P*			
21	High Voltage power pad	PP50*	50 volts		3.0
22	High Voltage power pad	PP50*	50 volts		3.0
23	Digital clock input	IB15P*			
24	Digital input LOAD	IB15P*			
25	Digital input RESET	IB15P*			
26	SLM device ground	PP03P*			
27	Periphery ground	PP05P*			
28	Periphery VDD	PP06P*			
29	HV transistor gate input	IOA2P*	5 volts[*2]		3.8
30	Ground for LVCM	IOA2P*	Analog ground		3.8
31	Digital VDD for DAC	PP04P*	5 volts		
32	DAC gate input	IOA2P*	Ground[*1]		3.8
33	IDC	IOA2P*		2 uA	3.8
34	Digital VDD	PP04P*	5 volts		
35	Digital VDD	PP04P*	5 volts		
36	Digital VSS	PP03P*	ground		
37	Digital VSS	PP03P*	ground		
38	Digital output DRT-0	Bare pad**			
39	Digital output DRT-1	Bare pad**			
40	Digital output DRT-2	Bare pad**			
41	Digital output DRT-3	Bare pad**			
42	Digital output DRT-4	Bare pad**			
43	Digital output DRT-5	Bare pad**			
44	Digital output DRT-6	Bare pad**			

PAD NUMBER	PAD DESCRIPTION	AMS PAD TYPE	VOLTAGE RATING	CURRENT RATING	INPUT CAPACITANCE IN
45	Digital output DRT-7	Bare pad**			
46	Analog output of Modulator 247	Bare pad**			
47	Analog output of Modulator 221	Bare pad**			
48	Analog output of Modulator 213	Bare pad**			
49	Analog output of Modulator 187	Bare pad**			
50	Analog output of Modulator 179	Bare pad**			
51	Analog output of Modulator 153	Bare pad**			
52	Analog output of Modulator 145	Bare pad**			
53	Analog output of Modulator 119	Bare pad**			
54	Analog output of Modulator 111	Bare pad**			
55	Analog output of Modulator 85	Bare pad**			
56	Analog output of Modulator 77	Bare pad**			
57	Analog output of Modulator 51	Bare pad**			
58	Analog output of Modulator 43	Bare pad**			
59	Analog output of Modulator 17	Bare pad**			
60	Analog output of Modulator 1	Bare pad**			
61	Digital core ground	PP03P*	Ground		
62	Periphery VSS	PP05P*	Ground		
63	Periphery VDD	PP06P*	5 volts		
64	Digital core VDD	PP04P*	5volts		
65	Digital Input 7	IB15P*			1.829
66	Digital Input 6	IB15P*			1.829

PAD NUMBER	PAD DESCRIPTION	AMS PAD TYPE	VOLTAGE RATING	CURRENT RATING	INPUT CAPACITANCE IN
67	Digital Input 5	IB15P*			1.829
68	Digital Input 4	IB15P*			1.829
69	Digital Input 3	IB15P*			1.829
70	Digital Input 2	IB15P*			1.829
71	Digital Input 1	IB15P*			1.829
72	Digital Input 0	IB15P*			1.829
73	IDC	IOA2P*		2uA	3.8
74	DAC gate input	IOA2P*	Ground[*1]		3.8
75	Digital VDD for DAC	PP04P*	5 volts		
76	Ground for LVCM**	IOA2P*	Analog ground		3.8
77	HV transistor gate input	IOA2P*	5 volts[*2]		3.8
78	SLM device ground	PP03P*			
79	Periphery VSS	PP05P*			
80	Periphery VDD	PP06P*			
81	High Voltage power pad	PP50*	50 volts		3.0
82	High Voltage power pad	PP50*	50 volts		3.0
83	Digital clock input	IB15P*			
84	Digital input LOAD	IB15P*			
85	Digital input RESET	IB15P*			
86	SLM device ground	PP03P*			
87	Periphery ground	PP05P*			
88	Periphery VDD	PP06P*			
89	HV transistor gate input	IOA2P*	5 volts[*2]		3.8
90	Ground for LVCM	IOA2P*	Analog ground		3.8
91	Digital VDD for DAC	PP04P*	5 volts		
92	DAC gate input	IOA2P*	Ground[*1]		3.8
93	IDC	IOA2P*		2 uA	3.8
94	Digital VDD	PP04P*	5 volts		

PAD NUMBER	PAD DESCRIPTION	AMS PAD TYPE	VOLTAGE RATING	CURRENT RATING	INPUT CAPACITANCE IN
95	Digital VDD	PP04P*	5 volts		
96	Digital VSS	PP03P*	ground		
97	Digital VSS	PP03P*	ground		
98	Digital output DRT-0	Bare pad**			
99	Digital output DLT-1	Bare pad**			
100	Digital output DLT-2	Bare pad**			
101	Digital output DLT-3	Bare pad**			
102	Digital output DLT-4	Bare pad**			
103	Digital output DLT-5	Bare pad**			
104	Digital output DLT-6	Bare pad**			
105	Digital output DLT-7	Bare pad**			
106	Analog output of Modulator 26	Bare pad**			
107	Analog output of Modulator 34	Bare pad**			
108	Analog output of Modulator 60	Bare pad**			
109	Analog output of Modulator 68	Bare pad**			
110	Analog output of Modulator 94	Bare pad**			
111	Analog output of Modulator 102	Bare pad**			
112	Analog output of Modulator 128	Bare pad**			
113	Analog output of Modulator 136	Bare pad**			
114	Analog output of Modulator 162	Bare pad**			
115	Analog output of	Bare pad**			

PAD NUMBER	PAD DESCRIPTION	AMS PAD TYPE	VOLTAGE RATING	CURRENT RATING	INPUT CAPACITANCE IN
	Modulator 170				
116	Analog output of Modulator 196	Bare pad**			
117	Analog output of Modulator 204	Bare pad**			
118	Analog output of Modulator 230	Bare pad**			
119	Analog output of Modulator 238	Bare pad**			
120	Analog output of Modulator 256	Bare pad**			

The four versions of the IC were designed and fabricated as part of a wafer run. The four ICs were arranged to fit into a wafer reticle of 19.4mm x 19.4mm with a small test chip. The layout of one of the IC is shown in Figure 4.22.

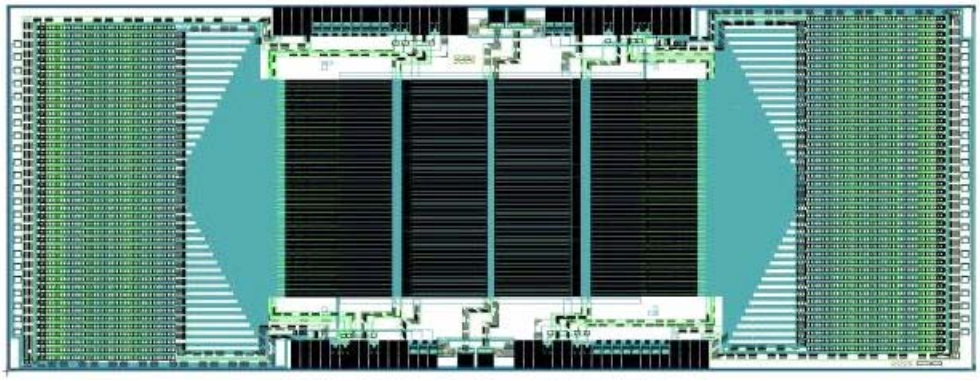


Figure 4.22 Layout snapshot of the high-voltage driver IC with a 1-D array of 256 drivers

The design and layout of the IC was done using VIRTUOSO manual layout tool from CADENCE IC tool suite. A database of the various components on

the driver IC was done separately. A hierarchical design approach was done to reduce repetition of any changes needed in base cells. Also this proved to be an easy approach in designing the four driver ICs as the only difference between each IC was the driver cell itself and the rest of the logic was the same. The database was duplicated four times and the driver cell replaced to the target 12Volts, 25Volts and 50Volts driver output.

Each chip was systematically simulated before being submitted for fabrication. Hspice software was used to simulate the various cells of the IC. A full chip simulation was not possible as we did not have simulation tools to support such a large IC and a step-by-step approach to do a hierarchical simulation was performed. To reduce complexity in the power supply, inputs and controls to the chip the driver array laid out in a staggered manner gave an opportunity to divide the IC into two identical parts. The input, controls and power pins were duplicated. This was also done to facilitate easy probe testing of the IC at wafer level, as the probe cards available were smaller in dimension compared to the size of the driver IC. The size of each driver IC was approximately 13mm x 5.7mm. Scribe lines were drawn around the IC as per the fabrication rules and the four versions of the IC were arranged in the manner shown in Figure 4.23 to form the reticle of a wafer. A small test chip was also designed to drive MEMS devices off-chip.

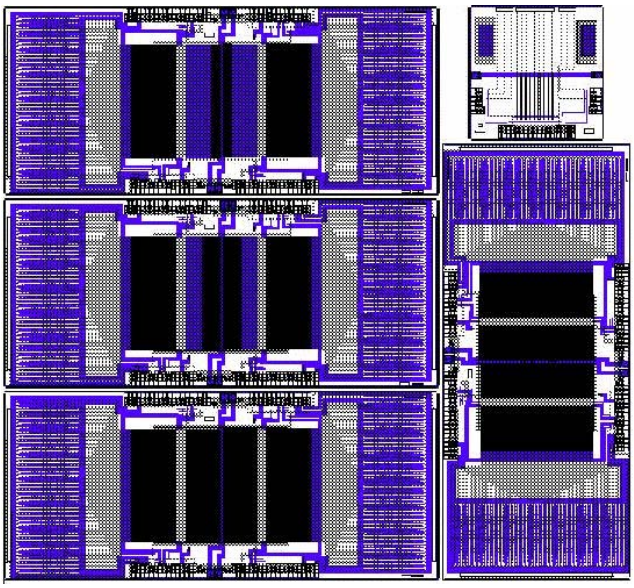


Figure 4.23 Wafer reticle with four versions of the driver IC and a test chip

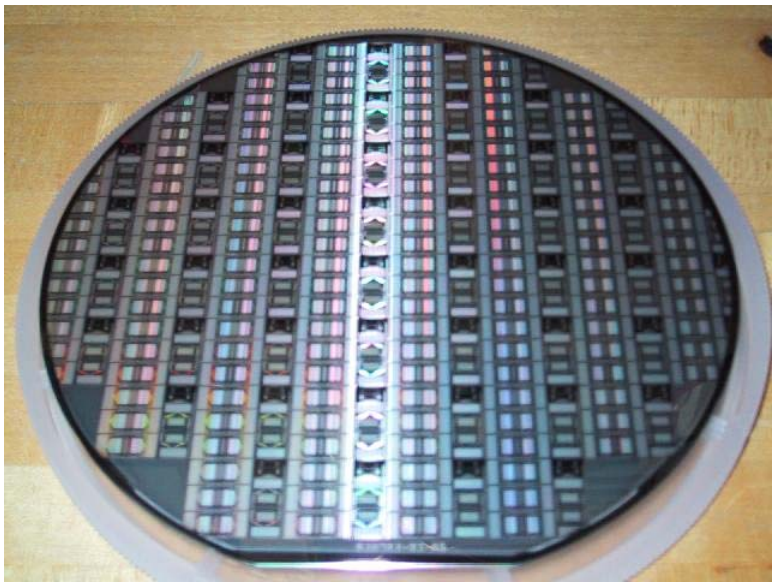


Figure 4.24 Picture of the fabricated driver ICs at wafer level

The design was submitted for fabrication in March 2002. The fabrication process was to deliver 6 wafers with three guaranteed wafers. The wafers were received back in May 2002 with five wafers. Two wafers were used to test the flip-chip bonding process before the electrical test of the IC was performed. The picture of the fabricated wafer is shown in Figure 4.24.

4.6 Testing and results

A semi-automatic testing of the IC electrically at wafer level was done using Labview software. A probe card was ordered and the probes in it were custom assembled to match the driver IC I/O footprint. The probe card was mounted on a probe station to probe the IC at wafer level. The various equipments used were the PC with Labview software installed, Tektronix pattern generator, various power supplies and power reading meters. All the equipment used in the test was connected to the PC through GPIB cables and each instrument was assigned a unique address.

The Tektronix pattern generator was programmed with the complete set of input patterns that need to be provided to the chip. All the possible 256 combinations using a 8-bit input starting from “00000000” to “11111111” was written to separate files. Labview program was done to send a stimulus to the pattern generator to generate patterns as soon as the IC is ready for probing. This prompts the pattern generator to send the first pattern 128 times with the clock and at the end of 128 cycles assert the load signal for the chip to load the new test pattern. The equipments used in the test were not optimized to do at-speed test and so input patterns were loaded one at a time. At any given test instance only one pattern was loaded to all the drivers. Figure 4.25 shows the picture of the lab setup used to do the probe testing of the wafer.

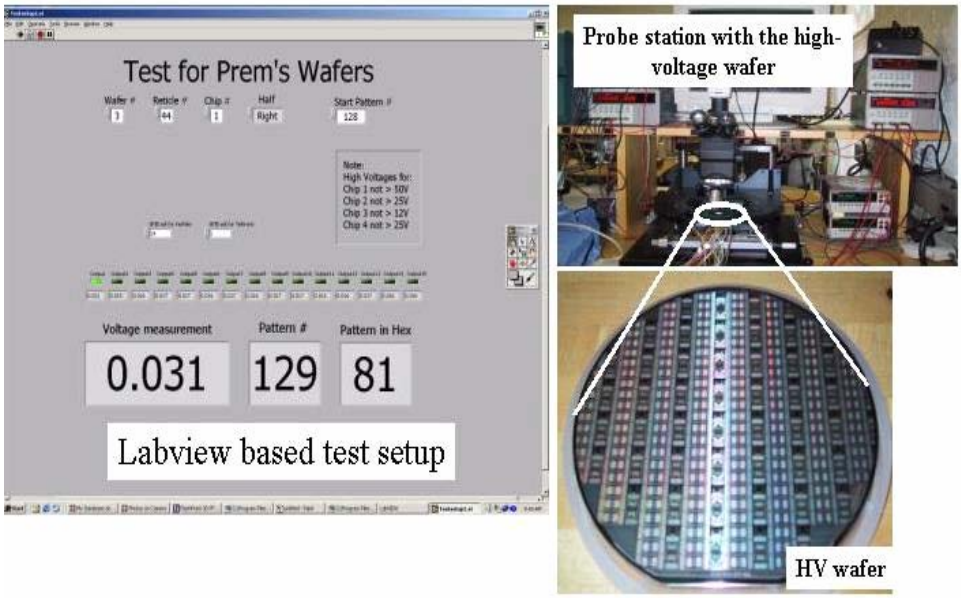
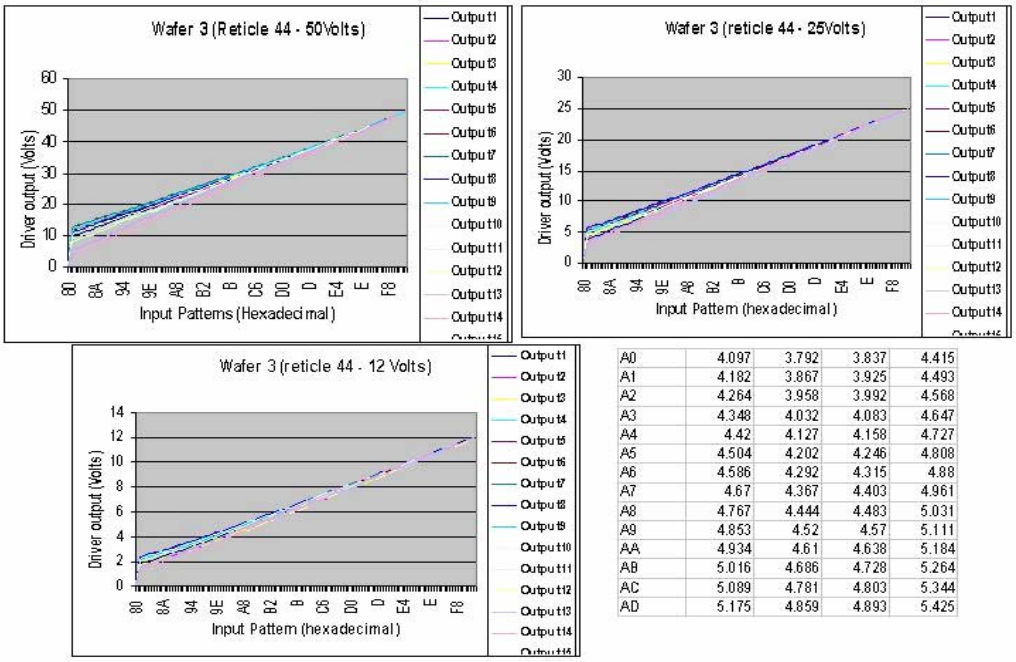


Figure 4.25 Semi-automated test setup to test the driver IC electrically with the wafer mounted on a probe station. A probe card mounted on the probe station probes the wafer. On the left of the figure is the test panel interface written using Labview software to define the various test parameters and to monitor the response from the wafer probing

An interface to control the wafer testing was done using the Labview program as well. Shown in Figure 4.25 is the test panel written for the semi-automated test. To begin the test, the wafer is placed on the probe station over the vacuum chuck. This hold the wafer when probing is done. Then the probe card is brought down slowly until the probes touch the pads on the IC. Once contact is made, the details of the IC are entered in the Labview test panel. The information required is the reticle site, the version of the IC that is probed, the maximum voltage output, the first pattern to start with and the last pattern to end the test. Also the test can be performed with input digital patterns in descending order. Even though the driver is rated for a certain

high-voltage maximum it can be operated at or below its rated maximum voltage range.

Once all the necessary input conditions are entered the Labview program starts the test with all the drivers in reset state. The pattern generator with the start stimulus from Labview sends the first input pattern to the probe card. Also the clock is sent along with the data. Once the new set of data is loaded in to the shift register, the load signal is asserted high. This loads the data to the storage registers. With the new input data the driver output is modulated. The output response from every eight drivers is available with the probe card. This data comes back to the Labview program and the values are noted. This way the stimulus and response are noted for each test pattern and also a profile of the response from each driver across the array. A whole wafer was tested with their maximum rated voltages and all the possible test patterns. The test results for one of the reticle is given in Appendix A. Figure 4.26 shows the test results for all the four versions of the driver ICs in one of the reticle. Also the driver IC was stress tested to check as to the maximum voltage range of operating beyond the rated maximum operating voltage range. The version of the chip with its maximum output range of 50Volts was stress. The response of the driver IC was very good until 60Volts (20% more than the maximum rated voltage range of the process). The response of the driver chip across the array is shown in Figure 4.27.



A0	4.097	3.792	3.837	4.415
A1	4.182	3.867	3.925	4.493
A2	4.264	3.958	3.992	4.568
A3	4.348	4.032	4.083	4.647
A4	4.42	4.127	4.158	4.727
A5	4.504	4.202	4.246	4.808
A6	4.586	4.292	4.315	4.88
A7	4.67	4.367	4.403	4.961
A8	4.767	4.444	4.483	5.031
A9	4.853	4.52	4.57	5.111
AA	4.934	4.61	4.638	5.184
AB	5.016	4.686	4.728	5.264
AC	5.089	4.781	4.803	5.344
AD	5.175	4.859	4.893	5.425

Figure 4.26 Electrical probe testing results of reticle 44 in one of the wafers marked 3. Shown are the drivers operating at 50Volts, 25Volts and 12Volts. Also an inset shows the test pattern input and responses from four of the drivers

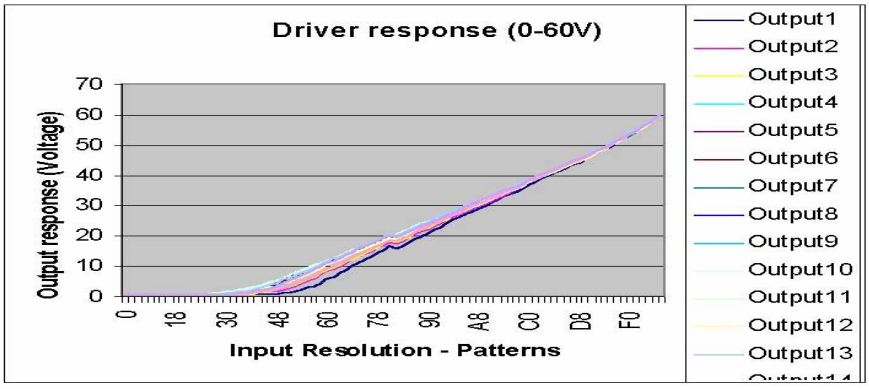


Figure 4.27 Electrical stress testing of the wafer at 20% more than the maximum rated voltage range of the fabrication process

The testing results of the whole wafer are shown in Figure 4.28. The rectangles marked in dark grey are good ICs and the rectangle marked in transparent red are bad ICs. Apart from the reticles at the edge of the wafer the total yield of the wafer was more than 90%. The chips were termed good for integration with SLM devices whose operation was satisfactory with the probe testing and the response of the drivers.

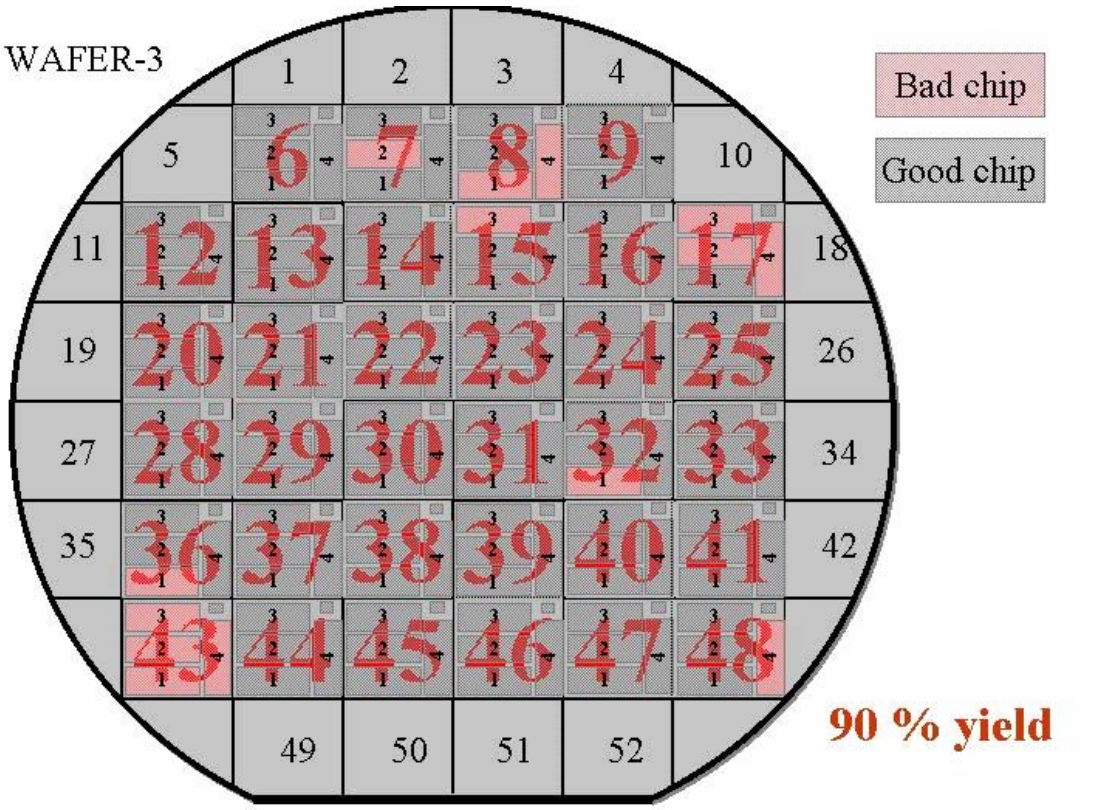


Figure 4.28 Test results of the whole wafer yield after electrically tested using the semi-automated test process

Chapter 5

CONCLUSIONS

5.1 ONIC

A novel design approach for a programmable ONIC, that interfaces to a parallel optical data link with a computer interface has been proposed. This design approach is very simple with a generic design for designing and fabricating a ONIC with FPGA, SERDES, parallel optical link modules and a standard compute system interface such as PCI. The design approach was applied to design a programmable ONIC that interfaces a 12-channel, gigabit parallel link module (each channel running at 1.25Gbps) and with a 64-bit/66MHz PCI computer bus. Several prototypes were developed to demonstrate VIVACE architecture that uses free space optical interconnects inside the switch fabric.

The ONIC hardware was designed in two stages to test the new FPGAs and hg-speed interface electrically with the optical modules located in a separate PCB. This was used for protocol development. The second generation ONIC was with all the components in the generic architecture designed according to PCI card standards. Two prototype ONIC were plugged onto PCI bus of two compute workstations and link integrity test and message passing application were performed. The test setup and results were presented in chapter 3. The compute node interface of PCI 64-bit/66MHz was driven by extensive availability of core logic, documentation and support. Also,

the standards are well defined and compute systems motherboards are designed with PCI bus interface.

The communication test performed between two ONIC installed onto two compute nodes worked as expected with links working at or above 1Gbps. The results show that the ONIC has high performance and high programmability compared to other commercially available. While the ONIC design technique lays a promising foundation for efficient optical network interconnection, it can be readily modified and adapted to support new protocols and optical data link technologies.

5.1.1 Suggestions for future study and improvement

The ONIC hardware that was designed and built for VIVACE system was done with the components available during the design phase. However there are many modifications that can be adapted to make the ONIC more powerful. Recently high performance compute node interfaces such as Infiniband [47] and PCI-X [48] are commercially available are software cores and chips designed to handle these protocols. The ONIC can be modified to provide higher communication bandwidth. PCI-X doubles the maximum bandwidth of 4Gbps of the ONIC with PCI interface to 8Gbps. These changes would involve extensive knowledge and studies of how the new interfaces work and once familiar can be easily adapted.

The first-generation ONIC used VIRTEX XCV1000 type FPGA devices from Xilinx. The second generation ONIC, however used only one VIRTEX XCV1000 FPGA device to control and process all the protocols. This FPGA had the PCI core and all the ONIC protocols in it. Also it used the slow-speed interface to communicate with the SERDES to send and receive the optical high-speed data. Recently VIRTEX FPGA with 24 individual SERDES circuits is commercially

available. They can operate at data rates from 622Mbps to 3.125Gbps. They also have POWER PC multiprocessor cores. With these new and efficient features the latest VIRTEX FPGA can simplify ONIC design as it reduces the PCB wiring between the SERDES and FPGA.

Newly available network processors support 10Gbps network bandwidth and software programmability [49]. But they cannot scale to 3.125Gbps * 24 = 75Gbps which is the total bandwidth achievable by the new VIRTEX II pro FPGA [50]. Thus FPGA based ONIC approach continues to be a good approach for demonstrating new network architecture and new VSR optical link technologies.

5.2 High-Voltage drivers for MEMS and modulators

A novel design methodology to design and build large arrays of high-voltage drivers for 1D and 2D arrays of modulators and MEMS devices was proposed. Application such as optical correlation for optical processing, optical beam steering and input and output devices for memory systems require large 1D and 2D array of optical devices such as MEMS and modulators. Most importantly hybrid integration of optoelectronic devices onto CMOS VLSI circuits becomes necessary. The added complexity arises when these optical devices need to be driven by higher voltages than normal CMOS processes in the order of 10s of volts. Hybrid integration of optoelectronic devices on top of active circuits gives greater flexibility for VLSI IC designers.

The design methodology was implemented on a high-voltage driver IC designed to drive a 1D array of 256 modulators for optical beam steering to be used in Avionic counter measures applications. Also the driver IC was designed to be flip-chip bonded with the modulators. The design aspect and results were presented in

chapter 4. The IC was also designed for it to be electrically tested before the devices were flip-chip integrated on to it. Four versions of the driver IC we re implemented with varying voltage ranges of up to 50Volts and varying maximum speed of operation. The driver designs were implemented taking into account the interconnect capacitance between the driver and the device and the capacitance induced by the optoelectronic devices as well. The driver IC were designed and fabricated as part of a wafer run using AMS 0.8um CXZ high-voltage process. A semi-automated test procedure was devised to test the driver IC at wafer level using Labview software. Every eighth driver output was brought to an external pad to be probe tested using the automated process. This verified if the whole driver array had a uniform performance. The yield of the wafer in terms of driver IC in good operating condition and uniform performance was very high. The results are given in chapter 4. The driver wafer was sent to the vendor to be diced and flip-chip attached with modulator devices.

This design approach and design implementation example shows that it is efficient and effective when designing optoelectronic device arrays that need high voltage of operation. This methodology can be adapted by designers designing high-voltage driver IC for optoelectronic devices with little or no changes to the core logic and still don’t have to sacrifice performance of the optoelectronic devices.

5.2.1 Adaptability and improvements

The proposed design approach is compatible with existing VLSI CAD tools and research needs to be conducted to make the whole process of placement and routing of the drivers and core logic in an automated fashion. Although the driver IC was designed for 1D array of devices it can be easily modified and adapted for a 2D array of devices. The size of the IC can however be dramatically improved when the

operating voltage of the devices are reduced leading to using sub-micron CMOS process with more metal layer for interconnections.

Appendix A

ELELCTRICAL PROBE TESTING RESULTS FOR DRIVER IC WITH MAXIMUM OUTPUT RANGE OF 50VOLTS

Pattern	O/P1	O/P2	O/P3	O/P4	O/P5	O/P6	O/P7	O/P8	O/P9	O/P10	O/P11	O/P12	O/P13	O/P14	O/P15
7F	0.08	0.086	0.087	0.084	0.092	0.094	0.094	0.095	0.094	0.093	0.092	0.09	0.088	0.083	0.079
80	8.016	10.89	9.055	8.357	10.52	9.565	10.28	8.084	9.084	9.656	9.141	8.847	6.735	5.836	7.56
81	8.337	11.19	9.381	8.492	10.83	9.88	10.56	8.384	9.414	9.971	9.448	9.163	7.066	6.169	7.91
82	8.667	11.54	9.685	8.963	11.1	10.17	10.87	8.691	9.661	10.27	9.751	9.455	7.368	6.472	8.212
83	8.988	11.82	9.994	9.107	11.4	10.47	11.14	8.967	9.97	10.57	10.05	9.767	7.693	6.805	8.555
84	9.338	12.15	10.27	9.22	11.68	10.71	11.43	9.29	10.23	10.78	10.37	10.09	8.062	7.16	8.909
85	9.667	12.43	10.57	9.91	11.98	11.01	11.7	9.573	10.54	11.09	10.66	10.4	8.384	7.473	9.246
86	9.975	12.77	10.87	10.05	12.23	11.29	12	9.877	10.79	11.37	10.97	10.69	8.696	7.784	9.553
87	10.3	13.06	11.19	10.42	12.54	11.61	12.28	10.17	11.12	11.7	11.28	11.01	9.038	8.133	9.918
88	10.69	13.37	11.44	10.67	12.81	11.92	12.5	10.43	11.4	12	11.6	11.41	9.376	8.552	10.28
89	11.01	13.66	11.76	10.62	13.12	12.23	12.78	10.72	11.71	12.31	11.91	11.72	9.717	8.887	10.63
8A	11.34	14.01	12.06	11.28	13.37	12.51	13.09	11.04	11.97	12.61	12.22	12.03	10.03	9.193	10.94
8B	11.65	14.29	12.39	11.21	13.69	12.84	13.38	11.33	12.29	12.93	12.52	12.35	10.37	9.532	11.3
8C	12.01	14.62	12.68	11.4	13.98	13.09	13.68	11.68	12.58	13.16	12.85	12.68	10.75	9.901	11.66
8D	12.32	14.9	12.98	11.83	14.28	13.4	13.95	11.97	12.9	13.46	13.16	12.99	11.08	10.24	12.01
8E	12.65	15.25	13.29	12.1	14.55	13.69	14.27	12.28	13.15	13.76	13.48	13.29	11.4	10.54	12.32
8F	12.98	15.53	13.61	12.57	14.86	14.01	14.55	12.57	13.47	14.07	13.78	13.6	11.72	10.87	12.65
90	13.29	15.73	14.03	12.9	15.21	14.32	14.88	13.05	13.79	14.53	14.06	13.94	11.99	11.43	12.98
91	13.62	16.03	14.35	12.88	15.51	14.63	15.15	13.33	14.11	14.83	14.36	14.24	12.31	11.75	13.31
92	13.94	16.36	14.64	13.07	15.76	14.9	15.46	13.64	14.35	15.12	14.67	14.55	12.62	12.07	13.62
93	14.25	16.64	14.96	13.66	16.07	15.23	15.74	13.94	14.68	15.45	14.98	14.87	12.97	12.42	14
94	14.57	16.95	15.22	13.83	16.35	15.47	16.03	14.27	14.96	15.69	15.33	15.22	13.37	12.8	14.38
95	14.86	17.21	15.52	13.94	16.66	15.79	16.31	14.57	15.28	16.01	15.64	15.54	13.72	13.15	14.75
96	15.18	17.55	15.82	14.15	16.92	16.07	16.62	14.89	15.55	16.3	15.95	15.85	14.03	13.45	15.04
97	15.51	17.85	16.15	14.45	17.24	16.4	16.91	15.18	15.87	16.62	16.25	16.15	14.34	13.75	15.34
98	15.93	18.19	16.43	14.77	17.52	16.71	17.15	15.44	16.15	16.91	16.56	16.52	14.66	14.16	15.69
99	16.26	18.47	16.74	15.33	17.83	17.04	17.41	15.74	16.47	17.23	16.88	16.85	15.02	14.52	16.06
9A	16.56	18.81	17.03	15.19	18.09	17.32	17.73	16.07	16.74	17.54	17.21	17.18	15.36	14.86	16.4
9B	16.86	19.09	17.34	15.58	18.4	17.65	18.03	16.37	17.07	17.86	17.52	17.5	15.71	15.2	16.76
9C	17.19	19.4	17.62	15.77	18.67	17.89	18.32	16.7	17.35	18.1	17.86	17.84	16.09	15.58	17.13
9D	17.49	19.67	17.91	16.14	18.98	18.2	18.59	17	17.67	18.41	18.17	18.17	16.45	15.94	17.5
9E	17.79	20	18.21	16.48	19.24	18.49	18.91	17.32	17.94	18.72	18.5	18.48	16.76	16.25	17.81
9F	18.1	20.28	18.52	16.87	19.54	18.81	19.18	17.61	18.27	19.03	18.79	18.79	17.1	16.58	18.15
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
A0	18.63	20.43	18.9	16.87	20.01	18.89	19.63	17.81	18.68	19.29	18.95	19.08	17.29	17.17	18.53

A1	18.95	20.73	19.23	17.47	20.34	19.22	19.91	18.09	19	19.61	19.24	19.38	17.61	17.47	18.85
A2	19.3	21.1	19.54	17.43	20.61	19.51	20.23	18.42	19.25	19.89	19.54	19.66	17.9	17.75	19.12
A3	19.63	21.39	19.86	18.01	20.92	19.83	20.51	18.7	19.57	20.2	19.83	19.96	18.21	18.05	19.43
A4	19.98	21.71	20.16	17.68	21.23	20.09	20.82	19.03	19.84	20.41	20.15	20.27	18.58	18.39	19.76
A5	20.31	22.01	20.49	18.37	21.55	20.42	21.11	19.33	20.17	20.72	20.46	20.58	18.9	18.71	20.09
A6	20.64	22.36	20.81	18.57	21.81	20.7	21.42	19.65	20.42	21.04	20.78	20.89	19.2	18.99	20.36
A7	20.96	22.65	21.13	18.89	22.13	21.03	21.71	19.94	20.74	21.34	21.07	21.19	19.53	19.3	20.69
A8	21.35	22.96	21.37	18.9	22.4	21.34	21.93	20.23	21.05	21.64	21.4	21.57	19.86	19.73	21.07
A9	21.67	23.24	21.69	19.11	22.7	21.66	22.21	20.53	21.37	21.95	21.7	21.89	20.21	20.07	21.4
AA	21.98	23.57	21.99	19.46	22.96	21.94	22.52	20.84	21.62	22.25	22.01	22.19	20.52	20.37	21.7
AB	22.3	23.86	22.3	20.14	23.28	22.27	22.81	21.14	21.96	22.57	22.32	22.51	20.85	20.71	22.04
AC	22.62	24.17	22.58	20.23	23.56	22.51	23.1	21.49	22.24	22.81	22.66	22.84	21.24	21.07	22.39
AD	22.93	24.44	22.89	20.31	23.87	22.84	23.39	21.79	22.56	23.11	22.96	23.15	21.57	21.4	22.73
AE	23.24	24.78	23.19	20.67	24.13	23.12	23.7	22.1	22.82	23.41	23.27	23.45	21.88	21.69	23.02
AF	23.53	25.05	23.49	21.04	24.43	23.43	23.97	22.39	23.15	23.72	23.58	23.76	22.21	22.02	23.35
B0	23.85	25.26	23.92	21.39	24.79	23.76	24.32	22.89	23.48	24.19	23.88	24.1	22.49	22.59	23.66
B1	24.17	25.54	24.24	21.53	25.1	24.08	24.6	23.19	23.8	24.49	24.18	24.41	22.82	22.91	24
B2	24.48	25.88	24.55	22.14	25.36	24.38	24.91	23.5	24.05	24.78	24.48	24.7	23.12	23.19	24.27
B3	24.79	26.15	24.85	22	25.66	24.69	25.19	23.8	24.37	25.1	24.78	25	23.44	23.51	24.6
B4	25.12	26.46	25.13	22.57	25.95	24.94	25.49	24.13	24.65	25.32	25.12	25.32	23.81	23.87	24.94
B5	25.43	26.74	25.45	22.89	26.26	25.27	25.77	24.44	24.97	25.63	25.41	25.63	24.14	24.19	25.26
B6	25.74	27.08	25.74	22.85	26.53	25.56	26.09	24.75	25.24	25.93	25.73	25.93	24.45	24.48	25.56
B7	26.06	27.36	26.07	23.44	26.84	25.88	26.37	25.06	25.56	26.25	26.04	26.24	24.79	24.81	25.89
B8	26.42	27.66	26.31	23.39	27.1	26.19	26.61	25.33	25.86	26.55	26.36	26.63	25.12	25.23	26.24
B9	26.71	27.93	26.61	23.53	27.41	26.51	26.88	25.63	26.18	26.87	26.67	26.94	25.46	25.55	26.57
BA	27.02	28.27	26.91	24.2	27.67	26.81	27.21	25.96	26.45	27.17	26.98	27.25	25.77	25.85	26.85
BB	27.33	28.54	27.23	24.29	27.98	27.13	27.49	26.25	26.77	27.49	27.29	27.56	26.1	26.17	27.19
BC	27.66	28.86	27.51	24.73	28.28	27.38	27.78	26.6	27.05	27.71	27.62	27.88	26.47	26.52	27.53
BD	27.95	29.14	27.81	25.08	28.58	27.7	28.07	26.89	27.38	28.03	27.93	28.18	26.8	26.84	27.85
BE	28.26	29.47	28.11	25.04	28.85	28	28.38	27.21	27.64	28.32	28.23	28.48	27.1	27.13	28.13
BF	28.56	29.74	28.42	25.51	29.15	28.31	28.66	27.51	27.96	28.63	28.53	28.78	27.43	27.45	28.45
C0	29.05	30.16	28.99	26.19	29.34	28.67	29.23	27.85	28.48	29.14	28.86	29.22	27.91	28.02	29.3
C1	29.36	30.43	29.3	26.38	29.65	29	29.5	28.14	28.81	29.45	29.16	29.53	28.23	28.33	29.62
C2	29.67	30.77	29.6	26.49	29.91	29.28	29.82	28.47	29.06	29.74	29.47	29.82	28.53	28.62	29.9
C3	29.96	31.04	29.91	27.01	30.22	29.61	30.1	28.76	29.39	30.06	29.77	30.12	28.86	28.94	30.22
C4	30.29	31.35	30.19	28.37	30.51	29.85	30.41	29.1	29.67	30.28	30.11	30.44	29.22	29.28	30.55
C5	30.59	31.62	30.5	27.98	30.82	30.18	30.69	29.4	29.99	30.6	30.41	30.75	29.55	29.6	30.87
C6	30.89	31.96	30.79	28.38	31.08	30.47	31.01	29.73	30.25	30.9	30.72	31.05	29.86	29.89	31.15
C7	31.19	32.23	31.1	28.68	31.39	30.79	31.29	30.02	30.58	31.21	31.02	31.35	30.19	30.21	31.47
C8	31.54	32.53	31.34	28.46	31.65	31.1	31.52	30.3	30.87	31.52	31.35	31.73	30.52	30.61	31.81
C9	31.84	32.8	31.66	28.14	31.97	31.43	31.8	30.6	31.2	31.83	31.65	32.04	30.84	30.92	32.12
CA	32.15	33.14	31.96	29.33	32.23	31.72	32.12	30.92	31.47	32.13	31.96	32.34	31.15	31.21	32.4
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
CB	32.44	33.41	32.26	29.59	32.54	32.05	32.4	31.22	31.79	32.44	32.26	32.65	31.47	31.52	32.72
CC	32.76	33.72	32.54	29.97	32.82	32.3	32.7	31.56	32.07	32.67	32.59	32.96	31.84	31.86	33.04
CD	33.06	33.99	32.85	30.46	33.13	32.62	32.98	31.86	32.39	32.98	32.89	33.26	32.16	32.17	33.36

CE	33.36	34.32	33.15	30.13	33.4	32.92	33.31	32.19	32.66	33.28	33.21	33.55	32.46	32.46	33.64
CF	33.66	34.6	33.45	30.66	33.71	33.24	33.59	32.49	32.99	33.59	33.51	33.86	32.79	32.78	33.96
D0	33.97	34.8	33.88	31.08	34.07	33.57	33.95	33	33.32	34.06	33.81	34.21	33.06	33.33	34.26
D1	34.28	35.07	34.19	30.67	34.38	33.91	34.23	33.3	33.65	34.38	34.12	34.51	33.39	33.64	34.58
D2	34.57	35.41	34.5	31.18	34.65	34.2	34.56	33.63	33.91	34.68	34.44	34.81	33.69	33.93	34.86
D3	34.87	35.68	34.8	31.92	34.96	34.53	34.84	33.93	34.24	35	34.74	35.12	34.02	34.25	35.18
D4	35.19	36	35.08	32.08	35.25	34.78	35.14	34.28	34.53	35.22	35.08	35.43	34.39	34.59	35.5
D5	35.49	36.27	35.4	32.04	35.57	35.12	35.43	34.58	34.86	35.54	35.38	35.74	34.72	34.9	35.82
D6	35.8	36.61	35.7	32.37	35.83	35.42	35.76	34.92	35.13	35.85	35.7	36.04	35.02	35.19	36.1
D7	36.1	36.88	36.01	32.75	36.15	35.75	36.05	35.22	35.47	36.17	36.01	36.34	35.35	35.5	36.42
D8	36.46	37.19	36.26	33.08	36.43	36.07	36.3	35.51	35.77	36.48	36.34	36.74	35.69	35.91	36.75
D9	36.76	37.47	36.58	32.96	36.74	36.41	36.58	35.81	36.1	36.8	36.65	37.04	36.02	36.22	37.08
DA	37.07	37.81	36.89	33.18	37.02	36.71	36.92	36.15	36.37	37.1	36.97	37.35	36.32	36.51	37.35
DB	37.37	38.09	37.2	33.71	37.34	37.05	37.21	36.46	36.72	37.42	37.28	37.66	36.66	36.83	37.68
DC	37.7	38.41	37.49	34.11	37.64	37.31	37.52	36.82	37.01	37.66	37.63	37.98	37.03	37.17	38.01
DD	37.99	38.69	37.81	34.61	37.96	37.65	37.82	37.13	37.35	37.99	37.93	38.29	37.37	37.49	38.33
DE	38.3	39.04	38.12	35.08	38.24	37.96	38.16	37.47	37.62	38.3	38.26	38.6	37.68	37.78	38.61
DF	38.61	39.32	38.44	35.37	38.56	38.3	38.45	37.78	37.97	38.63	38.57	38.91	38.01	38.1	38.93
E0	39.22	39.55	38.9	35.75	39.13	38.47	38.98	38.05	38.47	38.96	38.79	39.26	38.26	38.74	39.35
E1	39.53	39.83	39.22	35.94	39.45	38.82	39.29	38.38	38.82	39.29	39.1	39.58	38.6	39.06	39.68
E2	39.84	40.18	39.54	36.11	39.74	39.13	39.63	38.73	39.1	39.61	39.43	39.89	38.92	39.36	39.97
E3	40.15	40.47	39.87	36.55	40.06	39.48	39.93	39.04	39.45	39.94	39.75	40.2	39.26	39.68	40.29
E4	40.48	40.8	40.16	37.09	40.38	39.75	40.26	39.41	39.76	40.19	40.11	40.53	39.64	40.04	40.63
E5	40.8	41.09	40.49	37.28	40.72	40.1	40.57	39.74	40.11	40.52	40.43	40.85	39.99	40.36	40.96
E6	41.12	41.45	40.82	38.03	41	40.42	40.92	40.09	40.39	40.84	40.76	41.17	40.31	40.66	41.24
E7	41.43	41.74	41.15	38.26	41.34	40.78	41.23	40.42	40.75	41.19	41.08	41.49	40.65	40.99	41.57
E8	41.82	42.07	41.42	38.1	41.64	41.13	41.5	40.73	41.08	41.52	41.44	41.9	41.01	41.41	41.93
E9	42.14	42.36	41.76	38.33	41.98	41.5	41.81	41.06	41.44	41.86	41.77	42.23	41.36	41.74	42.27
EA	42.47	42.72	42.09	38.79	42.28	41.82	42.18	41.43	41.74	42.19	42.11	42.55	41.69	42.05	42.56
EB	42.79	43.03	42.43	39.32	42.63	42.2	42.49	41.77	42.11	42.54	42.45	42.88	42.04	42.38	42.89
EC	43.14	43.37	42.74	39.33	42.96	42.48	42.84	42.16	42.43	42.8	42.82	43.23	42.44	42.75	43.24
ED	43.46	43.67	43.09	40.18	43.31	42.86	43.16	42.5	42.81	43.15	43.16	43.56	42.8	43.09	43.59
EE	43.8	44.05	43.43	40.99	43.62	43.2	43.53	42.87	43.11	43.49	43.51	43.89	43.14	43.4	43.88
EF	44.13	44.35	43.79	41.5	43.97	43.58	43.86	43.22	43.49	43.85	43.85	44.22	43.51	43.74	44.23
F0	44.5	44.59	44.29	40.95	44.4	43.98	44.29	43.83	43.9	44.39	44.21	44.62	43.82	44.37	44.58
F1	44.84	44.9	44.66	41.33	44.77	44.38	44.63	44.19	44.29	44.76	44.57	44.96	44.19	44.72	44.93
F2	45.18	45.29	45.01	41.34	45.09	44.73	45.01	44.58	44.61	45.11	44.93	45.3	44.54	45.04	45.23
F3	45.52	45.6	45.38	41.89	45.46	45.14	45.36	44.95	45.01	45.48	45.29	45.64	44.92	45.4	45.59
F4	45.9	45.97	45.72	41.8	45.82	45.45	45.73	45.38	45.36	45.76	45.68	46.02	45.35	45.79	45.95
F5	46.24	46.29	46.1	42.79	46.2	45.86	46.09	45.75	45.77	46.14	46.05	46.37	45.74	46.15	46.32
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
F6	46.6	46.69	46.47	43.12	46.53	46.23	46.5	46.17	46.11	46.51	46.43	46.72	46.11	46.48	46.63
F7	46.96	47.02	46.86	44.15	46.92	46.65	46.86	46.56	46.53	46.9	46.8	47.07	46.5	46.85	47
F8	47.39	47.39	47.18	44.29	47.27	47.06	47.17	46.93	46.92	47.28	47.21	47.54	46.92	47.33	47.4
F9	47.75	47.73	47.58	45.13	47.67	47.5	47.54	47.33	47.36	47.68	47.59	47.89	47.33	47.71	47.78
FA	48.13	48.14	47.98	45.6	48.02	47.9	47.97	47.77	47.72	48.06	47.98	48.26	47.72	48.06	48.1

FB	48.5	48.49	48.39	45.94	48.43	48.34	48.36	48.18	48.18	48.47	48.37	48.62	48.15	48.44	48.49
FC	48.9	48.88	48.76	46.09	48.82	48.69	48.77	48.67	48.58	48.77	48.81	49	48.64	48.86	48.88
FD	49.27	49.23	49.19	46.27	49.24	49.15	49.17	49.1	49.06	49.2	49.2	49.36	49.09	49.25	49.27
FE	49.65	49.66	49.6	47.04	49.6	49.56	49.62	49.57	49.47	49.6	49.61	49.71	49.52	49.61	49.61
FF	50	50	50	47.37	50	50	50	50	50	50	50	50	50	50	49.99

Appendix B

ELECTRICAL PROBE TESTING RESULTS FOR DRIVER IC WITH MAXIMUM OUTPUT RANGE OF 25VOLTS

Pattern	O/P1	O/P2	O/P3	O/P4	O/P5	O/P6	O/P7	O/P8	O/P9	O/P10	O/P11	O/P12	O/P13	O/P14	O/P15
7F	0.098	0.103	0.104	0.086	0.108	0.11	0.11	0.11	0.109	0.108	0.106	0.104	0.102	0.097	0.092
80	3.192	3.32	4.349	4.392	5.456	5.661	4.213	5.287	4.763	4.648	4.589	4.065	3.787	3.26	3.118
81	3.353	3.485	4.508	4.287	5.623	5.826	4.369	5.44	4.914	4.777	4.741	4.063	3.782	3.253	3.117
82	3.533	3.655	4.685	4.609	5.767	5.958	4.511	5.566	5.057	4.926	4.868	4.354	4.096	3.54	3.397
83	3.697	3.823	4.834	4.842	5.93	6.122	4.655	5.72	5.206	5.054	5.026	4.344	4.092	3.536	3.395
84	3.919	3.97	5.026	4.701	6.051	6.232	4.814	5.876	5.34	5.225	5.2	4.677	4.403	3.846	3.72
85	4.069	4.132	5.172	5.012	6.208	6.394	4.967	6.033	5.494	5.36	5.352	4.674	4.404	3.855	3.731
86	4.256	4.299	5.334	5.161	6.349	6.518	5.106	6.159	5.635	5.515	5.488	4.979	4.727	4.174	4.06
87	4.427	4.472	5.489	5.078	6.509	6.685	5.256	6.317	5.794	5.652	5.648	4.974	4.726	4.182	4.067
88	4.605	4.644	5.638	5.186	6.647	6.841	5.424	6.422	5.914	5.799	5.807	5.291	5.045	4.582	4.432
89	4.752	4.797	5.78	5.676	6.797	7.003	5.57	6.58	6.069	5.938	5.969	5.293	5.051	4.596	4.445
8A	4.931	4.957	5.939	5.421	6.936	7.129	5.707	6.704	6.212	6.098	6.104	5.597	5.379	4.926	4.789
8B	5.074	5.115	6.079	5.724	7.085	7.282	5.861	6.862	6.367	6.227	6.266	5.599	5.388	4.942	4.807
8C	5.281	5.244	6.261	5.899	7.203	7.392	6.01	7.017	6.498	6.402	6.438	5.938	5.696	5.259	5.143
8D	5.423	5.403	6.4	6.154	7.355	7.554	6.155	7.168	6.657	6.534	6.606	5.949	5.707	5.273	5.164
8E	5.596	5.561	6.552	5.972	7.491	7.679	6.293	7.297	6.801	6.696	6.745	6.248	6.036	5.605	5.511
8F	5.746	5.717	6.695	6.134	7.644	7.842	6.446	7.451	6.954	6.829	6.905	6.244	6.034	5.604	5.511
90	5.944	5.948	6.881	6.283	7.788	7.953	6.56	7.521	7.081	6.993	6.945	6.626	6.361	5.889	5.852
91	6.097	6.11	7.029	6.417	7.939	8.114	6.708	7.678	7.236	7.125	7.108	6.626	6.364	5.897	5.865
92	6.275	6.268	7.182	6.708	8.081	8.241	6.856	7.804	7.38	7.289	7.246	6.939	6.702	6.233	6.21
93	6.413	6.42	7.317	6.612	8.229	8.401	7.001	7.963	7.539	7.429	7.411	6.94	6.707	6.241	6.221
94	6.622	6.561	7.507	7.115	8.347	8.511	7.155	8.12	7.669	7.596	7.584	7.277	7.015	6.563	6.563
95	6.772	6.717	7.65	6.928	8.488	8.663	7.293	8.27	7.82	7.723	7.732	7.267	7.009	6.555	6.561
96	6.953	6.885	7.809	7.059	8.641	8.798	7.444	8.401	7.961	7.878	7.866	7.564	7.326	6.875	6.885
97	7.125	7.061	7.972	7.245	8.803	8.964	7.599	8.556	8.123	8.012	8.034	7.559	7.325	6.873	6.887
98	7.318	7.239	8.126	7.365	8.948	9.132	7.773	8.662	8.249	8.16	8.182	7.872	7.64	7.277	7.241
99	7.47	7.406	8.278	7.426	9.104	9.292	7.924	8.822	8.408	8.299	8.353	7.877	7.644	7.286	7.251
9A	7.651	7.565	8.432	7.539	9.246	9.42	8.069	8.95	8.554	8.463	8.493	8.184	7.98	7.617	7.596
9B	7.79	7.721	8.574	7.956	9.398	9.584	8.22	9.109	8.713	8.605	8.656	8.184	7.981	7.623	7.609
9C	8.002	7.862	8.761	7.928	9.521	9.699	8.376	9.27	8.847	8.774	8.835	8.527	8.296	7.941	7.948
9D	8.153	8.024	8.914	7.973	9.68	9.861	8.53	9.431	9.007	8.911	8.988	8.526	8.29	7.941	7.949
9E	8.347	8.194	9.079	8.082	9.827	9.996	8.678	9.559	9.156	9.071	9.13	8.826	8.623	8.273	8.283
9F	8.502	8.364	9.231	8.387	9.985	10.16	8.831	9.719	9.317	9.206	9.293	8.827	8.624	8.276	8.293
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
A0	8.593	8.527	9.436	8.58	10.17	10.26	9.1	9.88	9.446	9.448	9.348	9.11	8.988	8.656	8.619

A1	8.744	8.691	9.584	8.543	10.32	10.42	9.251	10.04	9.607	9.59	9.518	9.112	8.995	8.669	8.635
A2	8.916	8.853	9.734	8.725	10.46	10.56	9.395	10.18	9.752	9.751	9.656	9.422	9.33	8.998	8.976
A3	9.066	9.013	9.883	9.007	10.62	10.72	9.543	10.33	9.911	9.89	9.821	9.425	9.335	9.006	8.984
A4	9.269	9.146	10.07	8.952	10.74	10.83	9.707	10.5	10.05	10.07	9.992	9.765	9.651	9.328	9.326
A5	9.42	9.31	10.22	9.401	10.9	11	9.859	10.65	10.21	10.2	10.16	9.766	9.652	9.331	9.336
A6	9.606	9.479	10.38	9.216	11.04	11.13	10.01	10.79	10.36	10.37	10.3	10.08	9.985	9.664	9.671
A7	9.752	9.641	10.53	9.562	11.2	11.29	10.16	10.94	10.52	10.51	10.47	10.08	9.992	9.67	9.683
A8	9.939	9.812	10.68	9.674	11.34	11.46	10.34	11.06	10.65	10.66	10.63	10.4	10.31	10.07	10.04
A9	10.09	9.981	10.83	9.966	11.5	11.63	10.49	11.22	10.81	10.8	10.8	10.4	10.32	10.08	10.05
AA	10.27	10.14	10.99	9.761	11.65	11.76	10.64	11.35	10.96	10.97	10.93	10.71	10.65	10.41	10.38
AB	10.42	10.31	11.14	10.16	11.8	11.93	10.8	11.51	11.13	11.11	11.1	10.71	10.65	10.42	10.4
AC	10.63	10.45	11.33	10.13	11.93	12.04	10.96	11.67	11.26	11.28	11.28	11.05	10.97	10.74	10.74
AD	10.78	10.62	11.47	10.49	12.08	12.21	11.11	11.84	11.42	11.42	11.45	11.05	10.97	10.75	10.74
AE	10.95	10.78	11.63	10.31	12.23	12.33	11.26	11.97	11.58	11.59	11.59	11.36	11.3	11.07	11.09
AF	11.11	10.94	11.78	10.55	12.39	12.5	11.42	12.13	11.74	11.73	11.75	11.36	11.31	11.08	11.09
B0	11.3	11.16	11.96	10.67	12.53	12.62	11.54	12.21	11.87	11.9	11.81	11.76	11.65	11.38	11.44
B1	11.45	11.33	12.11	10.75	12.69	12.79	11.7	12.37	12.04	12.04	11.98	11.76	11.66	11.39	11.45
B2	11.63	11.49	12.27	10.85	12.84	12.92	11.85	12.5	12.19	12.21	12.12	12.07	11.99	11.72	11.79
B3	11.78	11.65	12.42	11.2	12.99	13.09	12	12.67	12.35	12.35	12.29	12.08	12	11.73	11.8
B4	11.98	11.79	12.61	11.51	13.12	13.2	12.17	12.83	12.49	12.53	12.47	12.42	12.32	12.05	12.14
B5	12.14	11.95	12.76	11.67	13.27	13.37	12.32	13	12.65	12.67	12.64	12.42	12.31	12.05	12.15
B6	12.31	12.12	12.92	11.74	13.42	13.5	12.47	13.13	12.81	12.83	12.78	12.73	12.66	12.39	12.49
B7	12.46	12.28	13.07	11.64	13.58	13.67	12.63	13.29	12.97	12.98	12.95	12.73	12.66	12.39	12.5
B8	12.64	12.46	13.22	11.88	13.73	13.84	12.81	13.41	13.1	13.14	13.11	13.06	12.98	12.8	12.85
B9	12.79	12.62	13.37	11.81	13.88	14.01	12.97	13.57	13.27	13.28	13.28	13.06	12.99	12.81	12.86
BA	12.97	12.79	13.53	11.96	14.03	14.14	13.12	13.71	13.43	13.45	13.42	13.37	13.32	13.13	13.2
BB	13.12	12.96	13.68	12.5	14.19	14.31	13.28	13.87	13.59	13.59	13.59	13.37	13.33	13.14	13.21
BC	13.32	13.09	13.86	12.66	14.31	14.43	13.44	14.04	13.73	13.77	13.77	13.72	13.65	13.47	13.55
BD	13.47	13.26	14.01	12.61	14.47	14.6	13.6	14.2	13.9	13.91	13.94	13.72	13.65	13.47	13.56
BE	13.65	13.42	14.17	12.92	14.62	14.73	13.75	14.34	14.05	14.09	14.09	14.03	13.99	13.81	13.9
BF	13.8	13.59	14.32	12.71	14.78	14.9	13.91	14.5	14.22	14.22	14.25	14.04	14	13.81	13.9
C0	14.23	13.98	14.5	12.82	15.05	15.06	14.06	14.87	14.37	14.43	14.5	14.39	14.29	14.32	14.32
C1	14.39	14.15	14.65	13	15.21	15.22	14.23	15.04	14.54	14.57	14.67	14.39	14.29	14.33	14.33
C2	14.57	14.31	14.81	13.11	15.36	15.36	14.38	15.18	14.69	14.74	14.82	14.7	14.63	14.65	14.67
C3	14.72	14.48	14.96	13.64	15.52	15.53	14.54	15.35	14.86	14.88	14.99	14.71	14.63	14.66	14.67
C4	14.92	14.62	15.15	13.8	15.64	15.65	14.7	15.51	15	15.07	15.17	15.05	14.95	14.98	15.01
C5	15.07	14.78	15.3	13.95	15.81	15.82	14.86	15.68	15.17	15.21	15.34	15.05	14.96	14.99	15.02
C6	15.25	14.95	15.46	13.84	15.95	15.96	15.02	15.81	15.33	15.38	15.49	15.37	15.3	15.32	15.36
C7	15.4	15.12	15.61	14.15	16.11	16.13	15.18	15.98	15.5	15.52	15.66	15.37	15.3	15.32	15.36
C8	15.58	15.29	15.77	13.95	16.26	16.3	15.36	16.1	15.63	15.69	15.82	15.69	15.63	15.73	15.72
C9	15.73	15.46	15.92	14.17	16.43	16.47	15.53	16.27	15.8	15.83	15.99	15.7	15.63	15.74	15.73
CA	15.91	15.63	16.08	14.61	16.57	16.61	15.68	16.41	15.96	16	16.14	16.01	15.97	16.07	16.06
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
CB	16.06	15.8	16.23	14.75	16.74	16.78	15.85	16.57	16.13	16.15	16.31	16.01	15.97	16.07	16.07
CC	16.27	15.94	16.42	14.92	16.86	16.9	16.01	16.75	16.27	16.33	16.49	16.36	16.29	16.39	16.41
CD	16.42	16.11	16.58	14.71	17.02	17.07	16.18	16.91	16.44	16.47	16.67	16.36	16.3	16.4	16.41

CE	16.6	16.27	16.74	14.8	17.17	17.21	16.33	17.05	16.6	16.64	16.81	16.68	16.64	16.73	16.75
CF	16.75	16.44	16.89	15.15	17.34	17.38	16.5	17.22	16.77	16.79	16.99	16.68	16.64	16.73	16.75
D0	16.95	16.68	17.08	15.52	17.49	17.51	16.63	17.31	16.92	16.97	17.05	17.09	16.99	17.03	17.1
D1	17.1	16.85	17.24	15.55	17.66	17.68	16.79	17.47	17.09	17.12	17.22	17.08	16.99	17.04	17.1
D2	17.28	17.02	17.4	15.72	17.81	17.82	16.96	17.62	17.25	17.29	17.37	17.4	17.33	17.36	17.44
D3	17.43	17.19	17.55	15.53	17.97	17.99	17.12	17.78	17.42	17.44	17.54	17.4	17.34	17.36	17.44
D4	17.64	17.33	17.74	15.71	18.1	18.11	17.29	17.95	17.56	17.62	17.73	17.75	17.66	17.69	17.78
D5	17.79	17.5	17.9	16.11	18.26	18.29	17.46	18.13	17.74	17.77	17.9	17.75	17.66	17.69	17.78
D6	17.97	17.67	18.06	16.1	18.41	18.42	17.62	18.26	17.89	17.94	18.05	18.07	18.01	18.02	18.12
D7	18.12	17.84	18.21	16.27	18.57	18.6	17.78	18.44	18.07	18.09	18.22	18.07	18.01	18.02	18.12
D8	18.31	18.02	18.37	16.56	18.72	18.77	17.97	18.56	18.21	18.25	18.39	18.4	18.34	18.43	18.48
D9	18.46	18.19	18.53	16.39	18.89	18.95	18.14	18.73	18.38	18.4	18.56	18.4	18.34	18.44	18.48
DA	18.64	18.36	18.69	16.77	19.04	19.09	18.29	18.87	18.54	18.57	18.71	18.72	18.69	18.77	18.82
DB	18.79	18.53	18.85	16.78	19.21	19.26	18.46	19.04	18.72	18.72	18.89	18.72	18.69	18.77	18.82
DC	19	18.67	19.04	16.85	19.33	19.38	18.64	19.21	18.87	18.91	19.07	19.07	19.02	19.09	19.15
DD	19.15	18.84	19.19	17.78	19.5	19.56	18.81	19.39	19.04	19.06	19.25	19.07	19.02	19.1	19.16
DE	19.33	19.02	19.36	17.88	19.65	19.7	18.97	19.53	19.21	19.23	19.39	19.38	19.36	19.42	19.49
DF	19.49	19.19	19.51	18.11	19.82	19.87	19.13	19.7	19.38	19.38	19.57	19.39	19.36	19.43	19.5
E0	19.61	19.4	19.77	18.35	20.04	20.01	19.47	19.91	19.56	19.67	19.67	19.72	19.78	19.85	19.86
E1	19.76	19.57	19.92	18.71	20.21	20.19	19.64	20.08	19.73	19.82	19.84	19.72	19.78	19.85	19.87
E2	19.95	19.74	20.09	18.82	20.36	20.33	19.8	20.22	19.9	20	19.99	20.03	20.13	20.18	20.2
E3	20.1	19.92	20.24	18.79	20.53	20.51	19.97	20.4	20.07	20.15	20.16	20.04	20.13	20.18	20.2
E4	20.31	20.06	20.44	18.94	20.65	20.63	20.15	20.57	20.23	20.34	20.35	20.39	20.46	20.5	20.54
E5	20.46	20.23	20.59	18.98	20.82	20.81	20.32	20.75	20.4	20.49	20.53	20.39	20.46	20.51	20.54
E6	20.64	20.41	20.76	19.28	20.98	20.95	20.48	20.89	20.57	20.66	20.68	20.71	20.8	20.84	20.87
E7	20.79	20.58	20.91	19.16	21.16	21.14	20.68	21.08	20.77	20.84	20.88	20.73	20.83	20.86	20.9
E8	21	20.79	21.1	19.4	21.32	21.32	20.87	21.21	20.91	21.01	21.05	21.06	21.16	21.27	21.25
E9	21.16	20.96	21.25	19.5	21.49	21.5	21.05	21.39	21.1	21.16	21.23	21.07	21.16	21.27	21.26
EA	21.34	21.14	21.42	19.77	21.64	21.64	21.21	21.53	21.26	21.34	21.38	21.38	21.51	21.6	21.59
EB	21.49	21.31	21.57	19.78	21.8	21.82	21.39	21.7	21.44	21.49	21.56	21.39	21.51	21.61	21.59
EC	21.7	21.46	21.77	19.73	21.93	21.95	21.57	21.89	21.6	21.68	21.75	21.74	21.84	21.93	21.93
ED	21.85	21.64	21.93	20.21	22.1	22.12	21.74	22.06	21.78	21.84	21.93	21.74	21.85	21.93	21.93
EE	22.04	21.81	22.1	20.36	22.26	22.26	21.91	22.21	21.95	22.02	22.08	22.06	22.2	22.26	22.26
EF	22.19	21.99	22.26	20.42	22.43	22.44	22.09	22.38	22.13	22.17	22.26	22.06	22.19	22.26	22.27
F0	22.39	22.24	22.46	20.87	22.59	22.58	22.24	22.48	22.29	22.37	22.33	22.48	22.56	22.57	22.62
F1	22.55	22.42	22.62	21.15	22.76	22.76	22.42	22.66	22.47	22.52	22.51	22.49	22.57	22.57	22.62
F2	22.73	22.6	22.79	21.29	22.92	22.9	22.59	22.8	22.64	22.7	22.67	22.81	22.92	22.9	22.95
F3	22.88	22.78	22.95	21.64	23.09	23.08	22.76	22.98	22.83	22.86	22.84	22.81	22.92	22.91	22.95
F4	23.1	22.93	23.15	21.82	23.22	23.2	22.95	23.16	22.99	23.05	23.03	23.16	23.25	23.23	23.29
F5	23.25	23.11	23.31	21.92	23.39	23.38	23.13	23.34	23.17	23.21	23.22	23.16	23.25	23.24	23.29
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
F6	23.43	23.29	23.48	22.1	23.54	23.53	23.3	23.49	23.35	23.39	23.38	23.49	23.6	23.56	23.63
F7	23.59	23.48	23.64	22.26	23.71	23.71	23.49	23.66	23.54	23.55	23.55	23.49	23.61	23.57	23.63
F8	23.78	23.67	23.81	22.32	23.87	23.89	23.69	23.8	23.69	23.73	23.74	23.82	23.95	23.98	23.98
F9	23.94	23.86	23.96	22.42	24.04	24.07	23.88	23.98	23.88	23.89	23.92	23.83	23.95	23.99	23.98
FA	24.12	24.05	24.14	22.61	24.2	24.21	24.05	24.13	24.06	24.08	24.08	24.15	24.3	24.32	24.32

FB	24.28	24.24	24.3	22.68	24.37	24.39	24.24	24.31	24.25	24.24	24.26	24.15	24.31	24.32	24.32
FC	24.5	24.39	24.5	22.91	24.5	24.51	24.43	24.49	24.42	24.45	24.46	24.51	24.64	24.65	24.66
FD	24.66	24.59	24.67	23.02	24.68	24.69	24.62	24.67	24.62	24.62	24.65	24.51	24.65	24.66	24.66
FE	24.84	24.79	24.84	23.27	24.83	24.83	24.81	24.82	24.8	24.82	24.81	24.84	25.01	25.01	25
FF	25.01	25.01	25.01	23.46	25.01	25.01	25.01	25.01	25.01	25.01	25.01	24.84	25.01	25.01	25

Appendix C

ELECTRICAL PROBE TESTING RESULTS FOR DRIVER IC WITH MAXIMUM OUTPUT RANGE OF 12VOLTS

Pattern	O/P1	O/P2	O/P3	O/P4	O/P5	O/P6	O/P7	O/P8	O/P9	O/P10	O/P11	O/P12	O/P13	O/P14	O/P15
7F	0.045	0.05	0.051	0.058	0.055	0.058	0.057	0.058	0.057	0.057	0.055	0.053	0.051	0.047	0.043
80	1.87	2.274	2.177	2.342	2.402	2.615	2.415	2.579	2.604	2.308	2.279	1.86	1.926	1.493	1.498
81	1.932	2.336	2.242	2.401	2.458	2.672	2.479	2.634	2.665	2.366	2.341	1.919	1.985	1.558	1.567
82	1.998	2.393	2.306	2.466	2.521	2.741	2.535	2.698	2.725	2.43	2.398	1.983	2.056	1.624	1.626
83	2.059	2.458	2.369	2.523	2.579	2.798	2.598	2.755	2.789	2.489	2.463	2.044	2.119	1.69	1.696
84	2.134	2.522	2.42	2.602	2.637	2.857	2.66	2.814	2.844	2.559	2.533	2.122	2.189	1.76	1.771
85	2.197	2.588	2.485	2.662	2.694	2.915	2.725	2.875	2.909	2.617	2.597	2.185	2.249	1.828	1.843
86	2.265	2.646	2.551	2.727	2.759	2.985	2.782	2.938	2.971	2.684	2.657	2.251	2.322	1.896	1.904
87	2.33	2.711	2.616	2.786	2.817	3.043	2.846	2.997	3.036	2.745	2.724	2.314	2.384	1.965	1.977
88	2.408	2.783	2.69	2.853	2.895	3.097	2.893	3.067	3.097	2.811	2.777	2.385	2.459	2.056	2.065
89	2.473	2.847	2.759	2.912	2.956	3.157	2.959	3.128	3.165	2.872	2.843	2.449	2.524	2.124	2.138
8A	2.543	2.908	2.826	2.979	3.022	3.229	3.02	3.192	3.23	2.943	2.904	2.516	2.597	2.196	2.202
8B	2.609	2.976	2.893	3.041	3.084	3.291	3.088	3.258	3.296	3.002	2.972	2.582	2.664	2.27	2.278
8C	2.687	3.044	2.946	3.126	3.147	3.356	3.153	3.323	3.358	3.079	3.048	2.664	2.735	2.341	2.359
8D	2.753	3.112	3.015	3.187	3.211	3.419	3.222	3.389	3.427	3.14	3.116	2.728	2.801	2.415	2.434
8E	2.825	3.176	3.085	3.255	3.28	3.496	3.286	3.46	3.498	3.212	3.178	2.798	2.876	2.486	2.5
8F	2.892	3.246	3.157	3.323	3.345	3.56	3.357	3.524	3.57	3.278	3.249	2.865	2.944	2.561	2.575
90	2.956	3.343	3.233	3.405	3.434	3.637	3.447	3.59	3.634	3.332	3.338	2.919	3.009	2.607	2.642
91	3.026	3.418	3.305	3.471	3.501	3.704	3.52	3.659	3.707	3.398	3.414	2.988	3.076	2.684	2.72
92	3.098	3.486	3.379	3.547	3.574	3.783	3.587	3.73	3.778	3.473	3.479	3.058	3.156	2.758	2.787
93	3.169	3.561	3.454	3.616	3.645	3.849	3.661	3.8	3.85	3.541	3.557	3.128	3.226	2.833	2.865
94	3.254	3.636	3.514	3.708	3.712	3.919	3.734	3.868	3.916	3.625	3.639	3.216	3.303	2.909	2.951
95	3.326	3.711	3.591	3.773	3.782	3.985	3.807	3.937	3.988	3.694	3.717	3.287	3.377	2.986	3.03
96	3.405	3.781	3.667	3.854	3.858	4.063	3.875	4.011	4.059	3.77	3.782	3.363	3.459	3.064	3.098
97	3.477	3.857	3.746	3.919	3.928	4.131	3.95	4.081	4.131	3.841	3.861	3.436	3.534	3.142	3.178
98	3.574	3.938	3.831	3.997	4.016	4.192	4.004	4.157	4.202	3.922	3.925	3.52	3.619	3.24	3.278
99	3.65	4.013	3.909	4.065	4.085	4.258	4.079	4.227	4.273	3.993	4.003	3.593	3.697	3.322	3.364
9A	3.731	4.084	3.986	4.144	4.16	4.337	4.148	4.3	4.346	4.07	4.069	3.673	3.783	3.403	3.435
9B	3.807	4.16	4.065	4.212	4.231	4.404	4.223	4.369	4.419	4.139	4.149	3.75	3.857	3.488	3.523
9C	3.898	4.236	4.127	4.31	4.3	4.473	4.296	4.439	4.483	4.224	4.233	3.844	3.94	3.571	3.615
9D	3.975	4.311	4.204	4.379	4.369	4.54	4.37	4.508	4.557	4.294	4.312	3.919	4.016	3.658	3.702
9E	4.056	4.383	4.284	4.456	4.445	4.618	4.441	4.58	4.628	4.373	4.379	4	4.101	3.739	3.776
9F	4.133	4.46	4.361	4.526	4.514	4.688	4.517	4.65	4.701	4.442	4.457	4.076	4.176	3.828	3.865
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
A0	4.238	4.556	4.414	4.559	4.6	4.808	4.603	4.794	4.771	4.516	4.498	4.193	4.251	3.95	4.005

A1	4.316	4.631	4.492	4.629	4.674	4.875	4.677	4.862	4.847	4.589	4.577	4.271	4.329	4.036	4.091
A2	4.396	4.702	4.571	4.706	4.746	4.955	4.748	4.936	4.919	4.667	4.646	4.35	4.415	4.118	4.167
A3	4.473	4.776	4.649	4.777	4.818	5.024	4.822	5.005	4.994	4.737	4.723	4.427	4.492	4.203	4.255
A4	4.563	4.854	4.71	4.869	4.887	5.094	4.896	5.077	5.058	4.821	4.807	4.522	4.574	4.292	4.349
A5	4.642	4.93	4.791	4.938	4.958	5.161	4.971	5.147	5.132	4.892	4.888	4.598	4.65	4.375	4.436
A6	4.722	5.001	4.867	5.016	5.034	5.242	5.041	5.22	5.205	4.971	4.954	4.679	4.736	4.459	4.51
A7	4.798	5.078	4.946	5.084	5.106	5.31	5.116	5.291	5.281	5.038	5.034	4.755	4.812	4.544	4.598
A8	4.892	5.159	5.034	5.162	5.195	5.37	5.172	5.369	5.351	5.122	5.097	4.839	4.901	4.651	4.705
A9	4.97	5.236	5.111	5.233	5.267	5.439	5.248	5.44	5.423	5.192	5.177	4.914	4.976	4.739	4.792
AA	5.052	5.307	5.191	5.31	5.342	5.519	5.318	5.514	5.497	5.274	5.245	4.996	5.061	4.822	4.865
AB	5.128	5.383	5.27	5.382	5.415	5.586	5.393	5.584	5.572	5.342	5.324	5.071	5.135	4.905	4.953
AC	5.22	5.46	5.331	5.474	5.483	5.658	5.469	5.656	5.636	5.429	5.409	5.166	5.22	4.99	5.046
AD	5.297	5.536	5.411	5.547	5.553	5.728	5.545	5.726	5.712	5.498	5.489	5.241	5.298	5.077	5.133
AE	5.377	5.609	5.489	5.623	5.63	5.807	5.615	5.801	5.784	5.578	5.556	5.324	5.383	5.161	5.207
AF	5.453	5.684	5.567	5.693	5.702	5.876	5.692	5.872	5.859	5.649	5.636	5.398	5.456	5.244	5.293
B0	5.527	5.791	5.652	5.783	5.798	5.959	5.79	5.942	5.928	5.709	5.731	5.463	5.533	5.303	5.372
B1	5.604	5.868	5.732	5.854	5.871	6.027	5.868	6.013	6.002	5.781	5.81	5.539	5.608	5.386	5.458
B2	5.684	5.939	5.812	5.934	5.948	6.109	5.938	6.087	6.076	5.861	5.88	5.619	5.693	5.469	5.529
B3	5.761	6.017	5.891	6.002	6.021	6.178	6.013	6.159	6.151	5.931	5.958	5.697	5.77	5.555	5.616
B4	5.852	6.093	5.952	6.098	6.09	6.248	6.09	6.233	6.218	6.017	6.042	5.792	5.854	5.638	5.708
B5	5.928	6.166	6.031	6.17	6.161	6.319	6.169	6.302	6.293	6.087	6.123	5.866	5.928	5.722	5.795
B6	6.01	6.239	6.112	6.248	6.24	6.399	6.238	6.377	6.368	6.169	6.193	5.947	6.014	5.806	5.868
B7	6.085	6.315	6.19	6.319	6.311	6.468	6.315	6.449	6.443	6.237	6.271	6.023	6.089	5.891	5.953
B8	6.181	6.399	6.277	6.399	6.402	6.53	6.373	6.531	6.515	6.322	6.337	6.11	6.179	5.998	6.06
B9	6.26	6.476	6.359	6.469	6.472	6.601	6.451	6.6	6.589	6.394	6.416	6.186	6.254	6.083	6.146
BA	6.341	6.547	6.439	6.548	6.552	6.681	6.522	6.675	6.663	6.474	6.485	6.265	6.34	6.165	6.218
BB	6.416	6.624	6.518	6.617	6.625	6.751	6.6	6.748	6.74	6.545	6.565	6.341	6.415	6.249	6.303
BC	6.508	6.701	6.58	6.712	6.696	6.823	6.676	6.821	6.805	6.632	6.65	6.436	6.5	6.334	6.396
BD	6.585	6.779	6.659	6.788	6.767	6.894	6.753	6.893	6.88	6.701	6.73	6.513	6.575	6.418	6.479
BE	6.665	6.851	6.74	6.867	6.847	6.975	6.825	6.967	6.956	6.783	6.8	6.595	6.66	6.502	6.552
BF	6.742	6.928	6.821	6.938	6.919	7.045	6.902	7.04	7.032	6.854	6.879	6.67	6.736	6.583	6.637
C0	6.86	7.001	6.892	6.97	6.966	7.121	6.973	7.077	7.165	7.005	6.972	6.825	6.922	6.679	6.778
C1	6.936	7.078	6.971	7.041	7.039	7.191	7.051	7.149	7.241	7.078	7.051	6.901	6.999	6.762	6.863
C2	7.019	7.15	7.052	7.122	7.119	7.273	7.122	7.225	7.316	7.159	7.122	6.981	7.082	6.845	6.935
C3	7.093	7.229	7.13	7.194	7.193	7.344	7.201	7.296	7.392	7.231	7.201	7.058	7.16	6.929	7.02
C4	7.184	7.305	7.194	7.288	7.263	7.416	7.279	7.37	7.458	7.317	7.288	7.154	7.243	7.014	7.111
C5	7.263	7.382	7.274	7.358	7.336	7.487	7.356	7.443	7.535	7.389	7.367	7.23	7.32	7.097	7.195
C6	7.344	7.454	7.355	7.442	7.415	7.569	7.427	7.52	7.609	7.471	7.438	7.311	7.404	7.178	7.268
C7	7.42	7.531	7.434	7.513	7.488	7.64	7.507	7.591	7.687	7.542	7.517	7.387	7.479	7.263	7.352
C8	7.517	7.615	7.524	7.592	7.58	7.703	7.566	7.674	7.759	7.626	7.584	7.473	7.569	7.37	7.457
C9	7.593	7.693	7.605	7.665	7.653	7.775	7.646	7.745	7.835	7.698	7.664	7.55	7.645	7.453	7.541
CA	7.675	7.766	7.685	7.742	7.734	7.856	7.717	7.823	7.911	7.781	7.734	7.631	7.731	7.535	7.614
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
CB	7.75	7.844	7.765	7.816	7.807	7.929	7.797	7.895	7.988	7.852	7.815	7.708	7.806	7.618	7.697
CC	7.842	7.921	7.829	7.914	7.879	8.001	7.874	7.968	8.055	7.94	7.901	7.803	7.89	7.703	7.787
CD	7.919	7.998	7.91	7.985	7.952	8.073	7.953	8.041	8.131	8.011	7.981	7.88	7.966	7.785	7.871

CE	8	8.071	7.99	8.067	8.032	8.155	8.026	8.119	8.208	8.094	8.053	7.962	8.051	7.867	7.941
CF	8.077	8.147	8.071	8.139	8.107	8.227	8.106	8.192	8.284	8.166	8.133	8.038	8.126	7.952	8.026
D0	8.151	8.258	8.162	8.233	8.209	8.314	8.21	8.267	8.358	8.232	8.234	8.104	8.205	8.009	8.103
D1	8.227	8.336	8.243	8.306	8.283	8.385	8.29	8.34	8.434	8.303	8.314	8.18	8.28	8.093	8.187
D2	8.309	8.409	8.323	8.388	8.363	8.468	8.364	8.418	8.512	8.386	8.385	8.259	8.366	8.174	8.257
D3	8.385	8.488	8.405	8.458	8.437	8.541	8.443	8.491	8.587	8.458	8.466	8.336	8.441	8.258	8.341
D4	8.477	8.564	8.469	8.559	8.51	8.615	8.52	8.565	8.656	8.547	8.553	8.433	8.525	8.343	8.43
D5	8.553	8.642	8.549	8.631	8.584	8.687	8.601	8.64	8.733	8.62	8.633	8.51	8.6	8.425	8.514
D6	8.634	8.716	8.631	8.712	8.665	8.771	8.675	8.716	8.81	8.701	8.705	8.591	8.685	8.507	8.585
D7	8.71	8.794	8.713	8.785	8.74	8.842	8.754	8.79	8.887	8.775	8.787	8.667	8.762	8.589	8.668
D8	8.806	8.879	8.804	8.864	8.833	8.907	8.815	8.875	8.962	8.862	8.854	8.754	8.851	8.695	8.772
D9	8.883	8.955	8.884	8.937	8.907	8.981	8.895	8.948	9.039	8.935	8.935	8.831	8.927	8.779	8.855
DA	8.964	9.029	8.968	9.02	8.988	9.063	8.969	9.026	9.116	9.018	9.006	8.913	9.013	8.86	8.925
DB	9.04	9.108	9.048	9.091	9.064	9.136	9.049	9.1	9.194	9.089	9.087	8.988	9.09	8.944	9.008
DC	9.133	9.186	9.112	9.192	9.139	9.211	9.128	9.176	9.262	9.178	9.174	9.085	9.173	9.028	9.097
DD	9.209	9.264	9.194	9.266	9.213	9.284	9.209	9.25	9.341	9.252	9.257	9.162	9.248	9.11	9.18
DE	9.291	9.338	9.276	9.347	9.295	9.368	9.284	9.329	9.417	9.335	9.327	9.244	9.333	9.192	9.25
DF	9.367	9.416	9.358	9.421	9.369	9.441	9.363	9.402	9.495	9.408	9.409	9.319	9.409	9.274	9.332
E0	9.491	9.532	9.432	9.474	9.479	9.586	9.475	9.571	9.588	9.503	9.469	9.461	9.504	9.417	9.486
E1	9.567	9.61	9.514	9.547	9.554	9.659	9.555	9.645	9.667	9.577	9.551	9.537	9.58	9.499	9.569
E2	9.649	9.684	9.596	9.63	9.636	9.744	9.63	9.724	9.745	9.659	9.623	9.619	9.665	9.58	9.639
E3	9.725	9.762	9.679	9.703	9.711	9.817	9.712	9.799	9.822	9.734	9.705	9.696	9.741	9.663	9.722
E4	9.817	9.841	9.743	9.802	9.786	9.893	9.791	9.875	9.892	9.823	9.794	9.794	9.825	9.747	9.81
E5	9.893	9.919	9.826	9.877	9.863	9.966	9.874	9.95	9.971	9.896	9.876	9.87	9.901	9.83	9.893
E6	9.974	9.994	9.908	9.959	9.945	10.05	9.948	10.03	10.05	9.98	9.949	9.952	9.986	9.91	9.962
E7	10.05	10.07	9.99	10.03	10.02	10.13	10.03	10.1	10.13	10.05	10.03	10.03	10.06	9.993	10.04
E8	10.15	10.16	10.08	10.12	10.12	10.19	10.09	10.19	10.2	10.14	10.1	10.12	10.15	10.1	10.15
E9	10.22	10.24	10.17	10.19	10.19	10.27	10.18	10.27	10.28	10.22	10.18	10.19	10.23	10.18	10.23
EA	10.31	10.31	10.25	10.27	10.28	10.35	10.25	10.35	10.36	10.3	10.25	10.28	10.31	10.26	10.3
EB	10.38	10.39	10.33	10.35	10.35	10.43	10.33	10.42	10.44	10.38	10.34	10.35	10.39	10.35	10.38
EC	10.47	10.47	10.4	10.45	10.43	10.5	10.41	10.5	10.51	10.47	10.42	10.45	10.47	10.43	10.47
ED	10.55	10.55	10.48	10.52	10.51	10.58	10.5	10.57	10.59	10.54	10.51	10.53	10.55	10.51	10.55
EE	10.63	10.62	10.57	10.61	10.59	10.66	10.57	10.65	10.67	10.62	10.58	10.61	10.63	10.59	10.62
EF	10.71	10.7	10.65	10.68	10.67	10.74	10.66	10.73	10.75	10.7	10.66	10.69	10.71	10.68	10.7
F0	10.78	10.82	10.74	10.78	10.77	10.83	10.77	10.81	10.82	10.77	10.77	10.76	10.79	10.73	10.78
F1	10.86	10.89	10.83	10.85	10.85	10.9	10.85	10.89	10.9	10.85	10.85	10.83	10.87	10.82	10.86
F2	10.94	10.97	10.91	10.94	10.94	10.99	10.93	10.97	10.98	10.93	10.93	10.92	10.95	10.9	10.93
F3	11.02	11.05	11	11.01	11.01	11.06	11.01	11.04	11.06	11.01	11.01	10.99	11.03	10.98	11.01
F4	11.11	11.13	11.06	11.11	11.09	11.14	11.09	11.12	11.13	11.1	11.1	11.09	11.11	11.06	11.1
F5	11.19	11.21	11.15	11.19	11.17	11.22	11.18	11.2	11.21	11.17	11.18	11.17	11.19	11.15	11.18
Pattern	**O/P1**	**O/P2**	**O/P3**	**O/P4**	**O/P5**	**O/P6**	**O/P7**	**O/P8**	**O/P9**	**O/P10**	**O/P11**	**O/P12**	**O/P13**	**O/P14**	**O/P15**
F6	11.27	11.28	11.23	11.27	11.25	11.3	11.26	11.28	11.29	11.26	11.26	11.25	11.27	11.23	11.25
F7	11.34	11.36	11.32	11.35	11.33	11.38	11.34	11.36	11.37	11.33	11.34	11.33	11.35	11.31	11.33
F8	11.44	11.45	11.41	11.43	11.43	11.45	11.41	11.44	11.45	11.43	11.41	11.42	11.44	11.42	11.44
F9	11.52	11.53	11.5	11.51	11.51	11.52	11.49	11.52	11.53	11.5	11.5	11.5	11.52	11.5	11.52
FA	11.6	11.6	11.58	11.59	11.59	11.61	11.57	11.6	11.61	11.59	11.57	11.58	11.6	11.58	11.59

FB	11.67	11.68	11.67	11.67	11.67	11.68	11.66	11.68	11.69	11.66	11.66	11.66	11.68	11.67	11.67
FC	11.77	11.76	11.74	11.77	11.75	11.76	11.74	11.76	11.76	11.76	11.75	11.76	11.76	11.75	11.76
FD	11.84	11.84	11.82	11.85	11.83	11.84	11.83	11.84	11.84	11.83	11.83	11.84	11.84	11.83	11.84
FE	11.92	11.92	11.91	11.93	11.92	11.93	11.91	11.92	11.92	11.92	11.91	11.92	11.93	11.92	11.91
FF	12	12	12	12.01	12	12	12	12	12	12	12	12	12	12	12

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