0.5-μm CMOS Orthogonal Encoding Readout Cell for Active Imaging Systems

Jorge A. Garcia, *Student Member, IEEE*, William Lawler, Nicholas Waite, and Fouad Kiamilev, *Member, IEEE*

***Abstract*—We propose a novel continuous-time simultaneous-readout scheme for active imaging systems based on orthogonal modulation of photodetector signals. The superimposed-continuous-time approach presented here differs from the conventional scheduled-discrete-time scheme in that the photodetector signals are summed in a common bus and read concurrently. We show how that our proposed architecture may be advantageous, particularly in applications where bandwidth requirements for a time-multiplexed scheme are highly demanding. The active readout cell presented here is the kernel of the proposed orthogonal encoding architecture. We describe the cell operation principle, its properties and major design challenges. A 0.5-μm CMOS test chip has been fabricated to demonstrate functionality of the readout architecture. Test results show it to be a viable option for highly-integrated active imaging systems.**

***Index Terms*—Active imaging readout circuits, focal plane arrays, laser radar imaging systems, three-dimensional (3-D) imaging systems.**

I. Introduction

DESIGN of readout circuits for infrared imaging systems is increasingly challenging due to larger format photodetector arrays with smaller pixels, coupled with requirements for higher sensitivity and lower power dissipation. Traditional readout techniques involve photocurrent-to-voltage conversion at the cell level by means of an integrating capacitor as in the case of buffered direct injection (BDI), capacitive transimpedance amplifier (CTIA), or current mirrored direct injection (CMDI) [1]. Once the signals have been converted to voltage domain, time-multiplexing circuitry is used to transfer the discrete-time voltages to a single serial output [2]. To mitigate the effects of sampling noise at the integrating capacitors, techniques such as correlated double sampling (CDS) and auto-zeroing have been thoroughly studied and successfully implemented [3]–[7]. With smaller pixels, one of the obvious limitations becomes the size of the integration capacitor per readout cell, which is closely related to the amount of storable charge and sampling noise. Additionally, larger format arrays require that the electronics multiplexing the discrete-time cell voltages operate at faster speeds for a given frame rate. For active imaging systems with moderately large detector arrays, the bandwidth requirements of the readout integrated circuit may become prohibitive, forcing alternative ways of reading out the photodetector currents.

One possibility has been explored in [8]–[10], where current-mode signals are time-multiplexed similar to the voltage readout case, and a per-row current-to-voltage amplifier is used to deliver discrete-time voltages. While relaxing the scalability constraints by eliminating the integration capacitor per cell, this option is not practical for active imaging systems that require sampling of ac photocurrent signals, because the current-mode time-multiplexing scheme does not integrate the optical signal during the time interval a given readout cell is not selected, resulting in loss of readout efficiency.

The alternative we propose consists of a current-mode, continuous-time scheme for reading out the photo charges. By modulating the photocurrents with orthogonal carriers in the active readout cell, signals from an entire row are read simultaneously without loss of optical power. The current-to-voltage amplifier is removed from the cell and shared by an entire row. We illustrate how, for a 32×32 active imaging system under study at Army Research Laboratory, the orthogonal encoding architecture presented here leads to significant relaxation of the circuit bandwidth in comparison to the conventional time-multiplexing scheme. To compensate for the noise added by the cell electronics, we describe how the orthogonal encoding approach exhibits spectrum-shaping properties that can be used to reduce low-frequency noise. The active readout cell presented in this paper is the core of the proposed scheme. We describe its implementation details and major design challenges.

To verify functionality of the proposed readout architecture, a 0.5-μm complementary metal-oxide-semiconductor (CMOS) test chip containing prototype circuits for the active readout cells has been fabricated. The test system is completed by an off-chip, discrete-component current-to-voltage amplifier and a printed circuit board interface that allows us to perform electrooptical verification.

Section II presents the proposed readout architecture, its properties and design challenges. Section III describes the active readout cell implementation in detail. Section IV shows the results for the test prototype and Section V is devoted to conclusions.

II. Proposed Readout Integrated Circuit Architecture

A. System-Level Description

Fig. 1 shows a block diagram of the proposed readout architecture. The continuous-time currents from the photodetectors

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J. A. Garcia, N. Waite, and F. Kiamilev are with the Electrical Engineering Department, University of Delaware, Newark, DE 19716 USA (e-mail: garcia@ee.udel.edu; kiamilev@udel.edu; waite@ee.udel.edu).

W. Lawler is with the Army Research Laboratory, Adelphi, MD 20783 USA (e-mail: wlawler@arl.army.mil).

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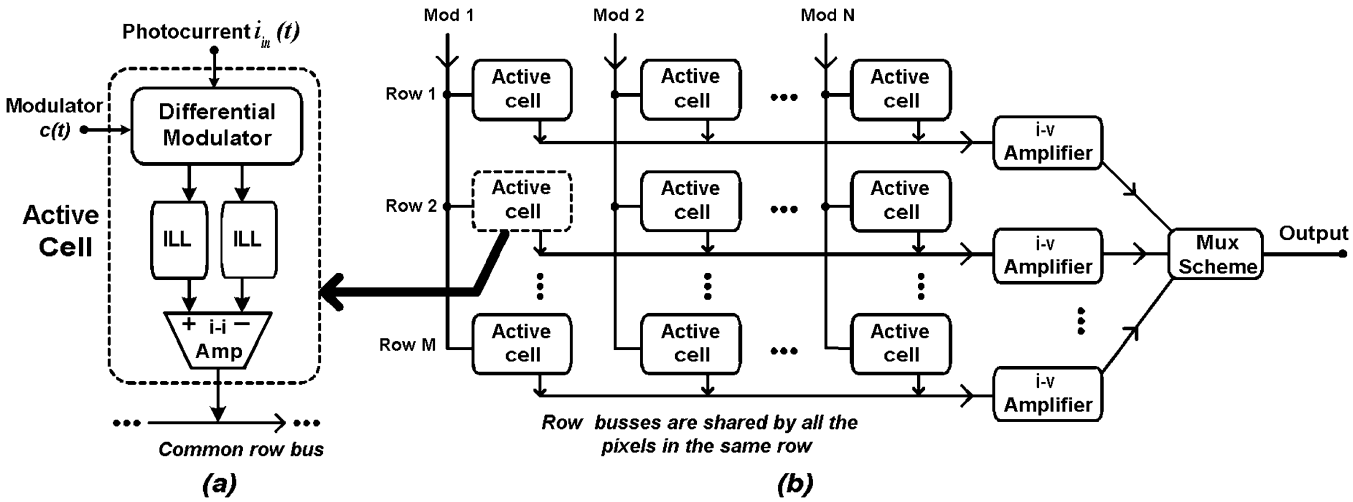

Fig. 1. Readout integrated circuit architecture. (a) Readout cell block diagram. (b) System block diagram.

are modulated by orthogonal signals in a column-wise manner in the active cells, and then added in the per-row common busses. Next, the added current signals are driven to an array of current-to-voltage converters that provide additional voltage gain. At the last stage, the amplified signals are fed to a multiplexer block to generate a single data stream output.

The orthogonality principle referred to here has been exploited in wireless multiuser communications [11], [12] For the active imaging architecture implemented in this paper, the multiuser scheme of preference is code-division multiple-access (CDMA) using pseudorandom (pn) sequences. The main reason for this choice is that generation of pn-sequences is simple, and their properties are well understood and documented [13], [14]. A potential drawback is that pn-sequences are not perfectly orthogonal, but they can be designed to meet a specific error criterion determined by the overall system noise budget [12], [13].

The novelty of our readout architecture resides in the use of orthogonal signals that multiply the cell photocurrents on a per column basis, thus allowing all signals from the same row to be read concurrently. The superimposed-continuous-time approach differs from the conventional scheduled-discrete-time scheme in that all photodetectors are read out simultaneously. Hence, the proposed solution may prove advantageous for applications where time-multiplexing bandwidth requirements would be highly demanding.

B. Potential Advantages

Consider, for example, an active imaging system with a 32×32 photodetector array of 20.6-MHz-bandwidth signals for a buried mine detection application under study at the Army Research Laboratory. The system is to be implemented using frequency-modulated/ continuous-wave laser radar (FM/cw LADAR) technology [15]–[17] with a chirp signal that serves as the receiver local oscillator and repeats every 0.1 s (10 Hz). An analog-to-digital (A/D) converter is implemented at the end of each row. For the CDMA architecture presented in this paper, each of the 32 pn-sequences should be designed with 1024 transitions, commonly called chips, so that cross talk amongst cells is held sufficiently low [12]. We achieve that by generating one code as a 32 768-b sequence of transitions and 32 delayed replicas of it, one for each column. Hence, the code rate for the chirp's 10-Hz repetition-rate is 10 Hz $\times$ 1024 (transitions or chips/cell) $\times$ 32 cells/row $=$ 327.7 kchips/s. The operation bandwidth of the row A/D, however, depends on the frequency contents of the summed row signals. Since the active imaging bandwidth (20.6 MHz) is much larger than the code rate (327.7 kHz), the bandwidth of the encoded signals remains below 21 MHz. Therefore, we conclude that for the CDMA readout the A/D converter bandwidth needs to be 21 MHz $\times 2$ (Nyquist-rate sampling) $=$ 42 Msamples/s. In contrast, the conventional time-multiplexing scheme requires a total A/D conversion bandwidth of 20.6 MHz (active signal bandwidth) $\times 2$ (Nyquist-rate sampling) $\times 32$ cells/row $=$ 1.318 Gsamples/s, a much more difficult requirement that places severe limits on the scalability of a time-multiplexed readout system.

One further benefit of orthogonal signal coding is that it can be used to shape the low-frequency noise of the succeeding electronics. A qualitative representation is shown in Fig. 2. In the cell encoding process, the photocurrent signal spectrum of bandwidth B is spread over the code bandwidth B_C [Fig. 2(a)]. As shown in top of Fig. 2(b), the thermal and $1/f$ noise (corner frequency f_n) of the subsequent electronics add to the spectrum and are then band-limited by the row amplifiers to approximately the code bandwidth B_C. After demodulation, the signal spectrum is collected back to its original band B whereas the noise spectrum gets spread over the code bandwidth [bottom of Fig. 2(b)]. A low-pass filter with cutoff frequency B, as shown in Fig. 2(c), can be used to recover the signal spectrum while minimizing the electronics $1/f$ noise.

The main challenge for the proposed architecture is to provide an efficient implementation of the active readout cell. The cell's purpose is to encode the incoming photocurrent signal, while adding low electronic noise and providing high injection efficiency. Additionally, for the self-mixing metal-semiconductor-metal (MSM) detectors used in the test prototype, it is essential that the readout cell provide virtual ground for the photodetector.

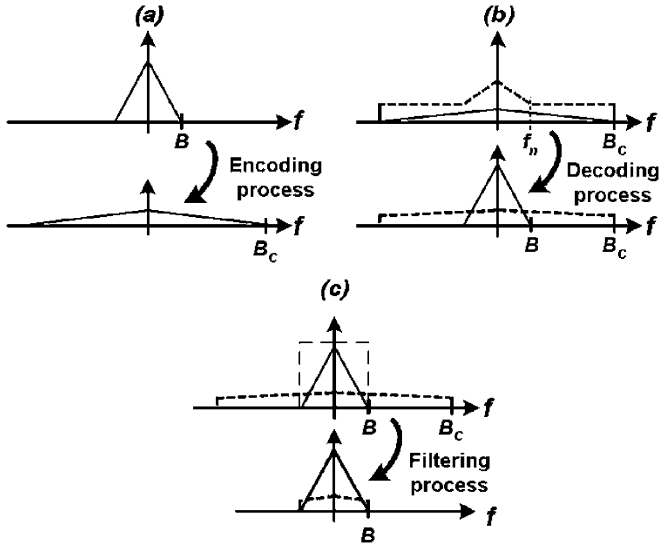

Fig. 2. Power spectral density of (a) photodetector signal (top) and encoded signal with code bandwidth B_C (bottom). (b) Output of amplifier with bandwidth B_C and $1/f$ corner frequency f_n (top) and decoded signal (bottom). (c) Output of low-pass filter with cutoff frequency B.

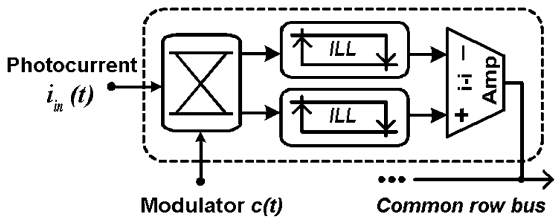

Fig. 3. Readout cell block diagram.

III. Active Readout Cell Implementation

Fig. 3 shows the block diagram of the readout cell topology. The first block, a *differential modulator*, consists of a cross-coupled array of CMOS switches that multiply the incoming photocurrent $i_{\rm in}(t)$ by the modulating signal $c(t)$.

At each modulator output, a *current locked loop* (ILL) circuit ensures near-zero MSM detector bias and virtual ground regulation while coupling the impedance of the photodetector to the next module. The last block, a *differential current amplifier*, is designed to provide current gain and high output impedance to couple the single-ended output of the cell to the common bus.

A. Differential Modulator

The circuit in Fig. 4 has been used as an analog multiplier [18], [19] and as square wave modulator in high frequency, low noise chopper amplifiers [20]. Its function here is two-fold: on the one hand, it modulates the photocurrent input with a signal from an orthogonal set, and on the other hand, it spreads the photodetector signal spectrum before amplification occurs so that the noise shaping techniques described previously can be used to improve the signal-to-noise ratio of the overall cell.

One of the difficulties with the modulator in Fig. 4 is the charge injection effect introduced at the output by the modulated switching transistors. Much effort has been devoted toward minimizing the effect of switching noise for a variety of applications [21]. Unfortunately, the complexity of such schemes is

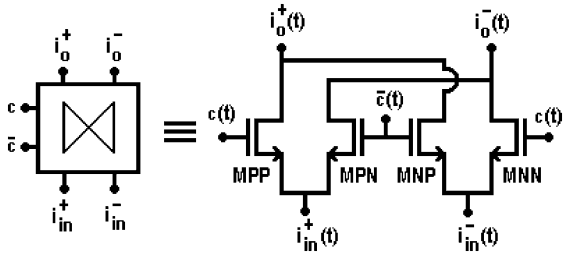

Fig. 4. Differential modulator, symbol, and transistor level circuit.

impractical for the rather simple architecture required for scalability and low-power consumption of active imagers.

Provided transistor and threshold voltage mismatches are minimized, the differential nature of the modulator presented here causes equal charge injection from the modulating signal into both arms of the output. In addition, assuming low photocurrent amplitude at the circuit input, the modulator's injection noise can be treated as signal independent [22], [23]. Then, the circuit's complementary structure ensures that the charge injection produced by the switching of MPP and MNP on $i_o^+(t)$ is replicated over $i_o^-(t)$ by the switching of MNN and MPN. The injected signal in the modulating process becomes common-mode noise that can be cancelled in the succeeding differential to single-ended amplifier stage.

The photodetector readout cell implementation presented in this paper uses a single-ended photocurrent input, but for the sake of generality, we derive here the expressions for a differential input. Let $i_{\rm in}^+(t)$ and $i_{\rm in}^-(t)$ be the current inputs to the modulator; if $c(t)$ and $\overline{c}(t)$ are the modulating signals, with $\overline{c}(t)$ the inverted version of $c(t)$, the differential modulator outputs are

$$\begin{aligned} i_o^+(t) &= i_{\rm in}^+(t)\cdot c(t) + n_c + i_{\rm in}^-(t)\cdot c(t) + n_{\overline{c}} \\ i_o^-(t) &= i_{\rm in}^+(t)\cdot \overline{c}(t) + n_{\overline{c}} + i_{\rm in}^-(t)\cdot c(t) + n_c \end{aligned} \tag{1}$$

where n_c and $n_{\overline{c}}$ represent the signal-independent, time-invariant charge injections introduced by the modulating signals $c(t)$ and $\overline{c}(t)$, respectively. The previous derivation assumes that transistor and threshold voltage mismatches are negligible. From (1), the output differential current $i_{od}(t)$ becomes

$$i_{od}(t) = i_o^+(t) - i_o^-(t) = \left[i_{\rm in}^+(t) - i_{\rm in}^-(t)\right]\cdot\left[c(t) - \overline{c}(t)\right] \tag{2}$$

which is, under ideal charge injection cancellation conditions, the differentially modulated signal.

Both the multiplying signals and transistor sizes are selected to minimize the charge injection terms n_c and $n_{\overline{c}}$, and to ensure that injection noise will be common to both outputs. The modulating signals are designed so that the channel charge accumulation in the switching transistors is minimized. Here, we choose $c(t)$ as a dc level added to a time-varying signal with sufficient amplitude to turn on and off the transistor switches, and the complementary $\overline{c}(t)$ as the inverted oscillating signal around the same dc value. To guarantee low switching noise, transistor sizes are optimized for minimum gate capacitance.

Although in (2) we assumed a differential input current, the result holds for single-ended inputs with $i_{\rm in}^-(t)$ equal to zero. Thus, under signal-independent charge injection and negligible transistor mismatch conditions, the differential modulator

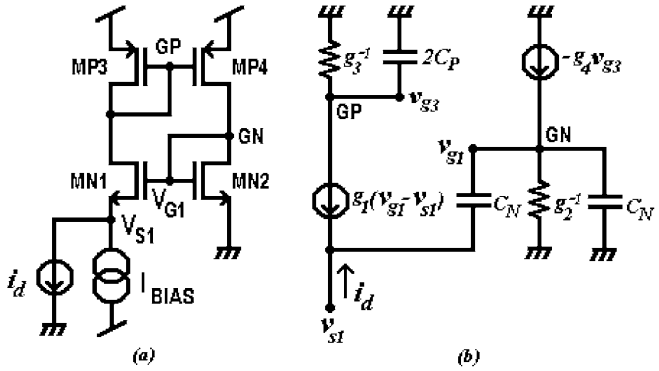

Fig. 5. (a) ILL circuit. (b) Small-signal equivalent.

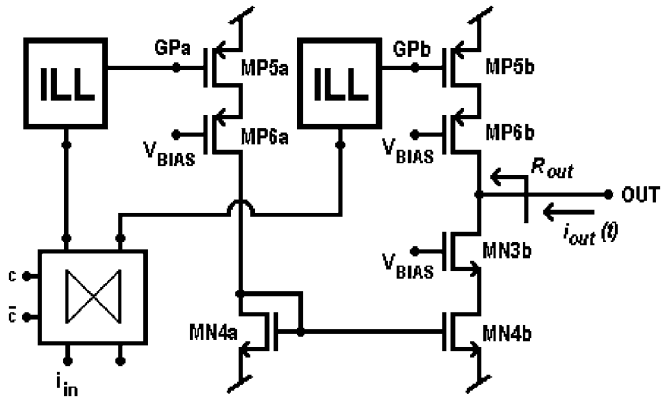

Fig. 6. Differential current amplifier schematic.

makes the injected charge appear as common-mode noise, and the differential to single-ended operation carried out by the *differential current amplifier* cancels the switching noise.

B. Current Locked Loop (ILL)

The ILL architecture shown in Fig. 5(a) has been successfully used to collect photodetector currents from passive infrared (IR) sensors [2], [8], [9]. The high injection efficiency, near-zero detector bias and low static power consumption, make the ILL ideally suited for passive readout applications. This section evaluates the circuit topology for active imaging applications. We study the dc and ac properties of the ILL architecture including its feedback nature and stability characteristics.

1) Dc Characteristics: For dc analysis, the current i_d in Fig. 5(a) is not considered. Transistor MN1 transfers the input bias current $I_{\rm BIAS}$ to the current mirror MP3–MP4. The drain current of MP4 is driven to the diode-connected transistor MN2 that converts it back to a gate voltage V_{G1}. Provided MP3-MP4 and MN1-MN2 are closely matched, the dc gate-source voltage of the n-type transistors will be approximately equal (assuming their threshold voltages are the same) and consequently $V_{S1} \approx 0$.

Previous work [9] shows the dc source voltage V_{S1} is a function of transistor geometries and threshold voltage mismatches across the silicon wafer, and is given by

$$V_{S1} = \frac{K_P}{K_N}\Delta V_{TP} + \Delta V_{TN} \tag{3}$$

where K_P, K_N are geometrical constants and V_{TP}, V_{TN} are the threshold voltages of p-type and n-type transistors, respectively. Reasonably low threshold mismatches ensure dc operation points close to zero (in the low millivolt range), making this biasing structure a good candidate for photodetection applications that require virtual ground regulation.

2) Feedback Nature and Input Voltage Regulation: Analyzing the feedback loop behavior and stability conditions for the ILL structure is key to determine its performance as an active photoreceiver amplifier.

For an ac input i_d, the cascode transistor MN1 and the current mirror MP3–MP4 are the error sensing elements whereas the transconductor MN2 is the feedback actuator. If the input current i_d increases, the MN1 source voltage decreases by v_{s1} to accommodate the current variation; the change in MN1 current is mirrored by MP3–MP4 and converted by MN2 into a change in gate potential v_{g1}. Proper sizing of the transistors guarantees a voltage gain $|v_{g1}/v_{s1}|$, so the gate rather than the source of MN1 accomplishes the voltage variation corresponding to the input current change. The higher increment of v_{g1} in turn forces the source potential v_{s1} back to its original value, thus providing detector virtual ground regulation for dc and low frequency operation.

This operation principle applies only to current source inputs, and provided the transistor sizes yield a negative v_{g1}/v_{s1} gain, the circuit operates under negative feedback and regulates the input voltage. If v_{g1} fails to counteract the input voltage change, the system enters positive feedback region and v_{s1} drops until the circuit fails to regulate the virtual ground. In our case, the unregulated input unbalances the mixing process at the MSM photodetector.

The equivalent small signal circuit for the ILL architecture is shown in Fig. 5(b), with $g_m >> g_{ds}$ for all transistors, and lumped capacitors C_N and $2C_P$, with $C_N \approx C_{GS\text{-}N1} = C_{GS\text{-}N2}$ and $C_P \approx C_{GS\text{-}P4} = C_{GS\text{-}P3}$.

Using Kirchoff's current law at nodes G_P and G_N we get

$$-v_{g3}(g_3 + 2sC_P) = g_1(v_{g1} - v_{s1})$$

and

$$-g_4 v_{g^3} + sC_N v_{s1} = v_{g1}(g_2 + 2sC_N). \tag{4}$$

Eliminating v_{g3} yields the voltage gain relationship

$$\frac{v_{g1}}{v_{s1}} = \frac{-g_1 g_4 + sC_N(g_3 + 2sC_P)}{(g_2 + 2sC_N)(g_3 + 2sC_P) - g_1 g_4}. \tag{5}$$

At dc and low frequencies, (5) becomes

$$\left.\frac{v_{g1}}{v_{s1}}\right|_{\rm lowfreq.} = \frac{-g_1 g_4}{g_2 g_3 - g_1 g_4} = \frac{-\gamma}{1-\gamma}, \text{ with } \gamma = \frac{g_1 g_4}{g_2 g_3}. \tag{6}$$

Hence, for $\gamma < 1$, the voltage gain is negative and the circuit operates under negative feedback conditions, successfully providing virtual ground at the source of MN1. The factor γ derived above is key to the proper operation of the circuit. The transistors must be sized so that in the expression for γ in (6) the numerator is always slightly smaller than the denominator.

3) Input Impedance: Photodetector readout circuits require a very low input impedance to maximize injection efficiency. Conventional readout pixel architectures accomplish low-input impedance by providing a voltage regulated cascode transistor

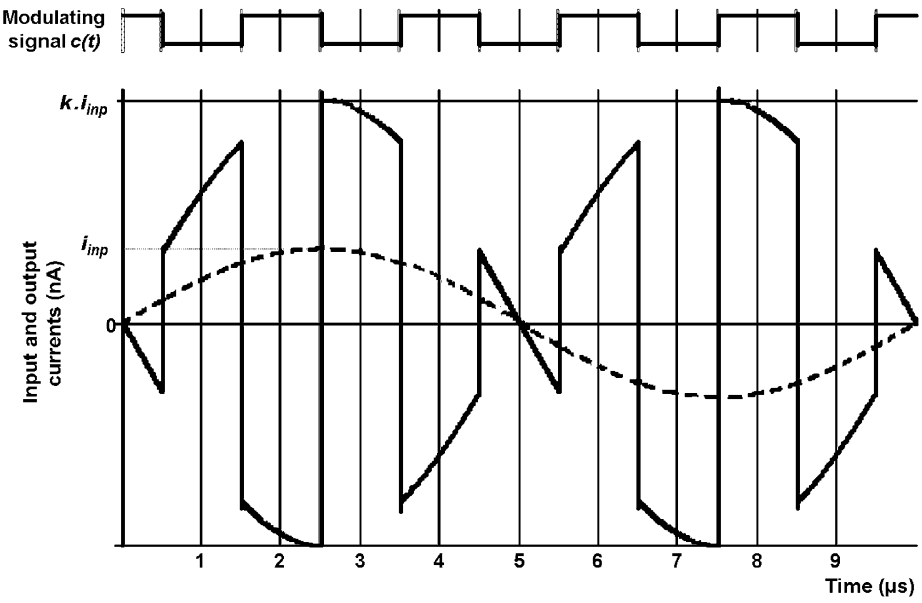

Fig. 7. Qualitative representation of the photocurrent modulation process.

input as in the buffered direct injection case or by providing a virtual ground using an amplifier in negative feedback configuration [24].

In the ILL circuit, the low input impedance is accomplished by negative feedback around transistor MN1. Using a test input voltage v_{s1} at the source of MN1, the input current i_d is given by

$$i_d = -(v_{s1} - v_{g1})(g_1 + sC_N) \tag{7}$$

and combining (7) and (5), we get the expression for the input impedance

$$Z_{\text{in}} = \frac{v_{s1}}{i_d} = \frac{(g_2 + 2sC_N)(g_3 + 2sC_P) - g_1 g_4}{(g_1 + 2sC_N)(g_2 + sC_N)(g_3 + 2sC_P)}. \tag{8}$$

At low frequencies, (8) comes

$$Z_{\text{in}}|_{\text{lowfreq.}} = \frac{1}{g_1}(1 - \gamma). \tag{9}$$

Evidently, the negative feedback effect is present in (9) where, as the factor γ approaches unity, the input impedance tends to zero, maximizing the injection efficiency. For the high frequency regime, the two zeroes in (8) generate an increment in the value of the impedance, corresponding to the region where the ILL circuit fails to work as a photocurrent amplifier (an indicator of the end of negative feedback regime and the beginning of unstable operation.)

For a particular operation bandwidth, it is necessary to engineer the values of the transconductors and capacitors so that negative feedback and, consequently, high injection efficiency and virtual ground regulation are guaranteed over the frequency range of interest. Due to the third-order denominator in (9), at very high frequencies, the input impedance approaches zero.

C. Differential Current Amplifier

As shown in Fig. 6, the current mirrors MP5a and MP5b amplify the outputs from each ILL circuit. To perform differential to single-ended conversion, one of the branches is passed through the current mirror MN4a, MN4b–MN3b and then subtracted from the other. The resulting single-ended signal corresponds to an amplified version of the modulated photocurrent. Transistor MN3b is used to minimize channel-length modulation on MN4b and to improve its output impedance. Transistors MP6a and MP6b are used to minimize channel-length modulation effects on the mirror transistors MP5a, MP5b and to further boost the output impedance of the amplifier. The low frequency output impedance R_{out} of the circuit is the parallel of the n-type and p-type cascode output impedances

$$R_{\text{out}} = (1 + g_{m6b} r_{06b}) r_{05b} // (1 + g_{m3b} r_{03b}) r_{04b}. \tag{10}$$

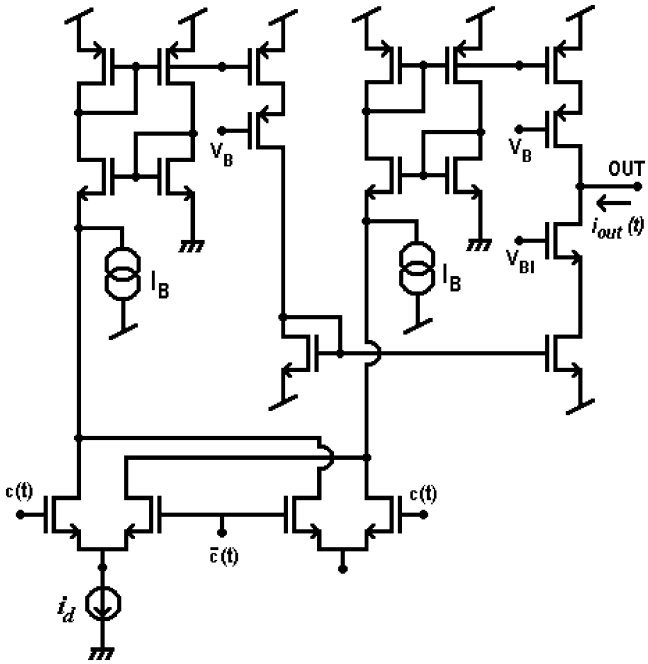

Fig. 8. Simplified schematic of the active readout cell.

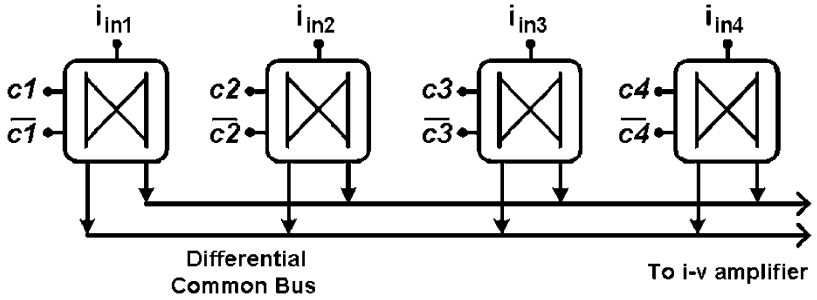

Fig. 9. Four-element encoding array with a common output bus. Each cell contains the circuit of Fig. 8.

As mentioned in Section III-A, this scheme cancels the common-mode switching noise introduced by the differential input modulator so the single-ended output current becomes

$$i_{\text{out}}(t) = k \cdot \left[i_{\text{in}}^{+}(t) - i_{\text{in}}^{-}(t)\right] \cdot \left[c(t) - \overline{c}(t)\right] \qquad (11)$$

where k is the transistor ratio between MP5 (a or b) and p-type transistors of the ILL circuit. Fig. 7 shows a qualitative representation of a modulated output current. The input is a sinusoidal current signal with peak amplitude i_{inp} and the modulating signal $c(t)$ is the square waveform shown on top. Fig. 8 shows a simplified schematic of the active readout cell.

IV. Verification and Test Results

We have fabricated a CMOS test chip to verify the circuit designs and to demonstrate orthogonal readout cell encoding. The chip has been mounted onto a custom circuit board and operated successfully with electrical test signals. In a proof-of-principle experiment, we have demonstrated that the readout encoding architecture functions in agreement with the theory presented earlier.

In this section, we discuss the readout chip layout, the test configuration, and present the measured results that validate the circuit designs and architecture.

A. Readout Test Chip and Printed Circuit Board Interface

The readout integrated circuit (ROIC) test chip was fabricated in a 0.5-μm, 5-V process that has feature sizes appropriate for full-scale chips. The integrated circuit contains test cells for the differential modulator of Fig. 4, the current locked loop of Fig. 5(a), and several small 1-D arrays of encoding cells.

The ILL test cell was biased with a 100-nA current and functions as expected, with a low-frequency unity gain and the input maintained within 5 mV of ground level, showing regulation of the virtual ground input node. Low bias current is important for low noise and low power dissipation, as the cell may have application in low to medium density focal plane arrays.

The modulators of Fig. 3 were laid out such that only the i_{in}^{+} inputs connect to wire bond pads, assuring zero input current for the minus terminal. Fig. 9 shows the 1×4 element array of encoding cells used for testing. Each of the cells contains the circuit schematic shown in Fig. 8.

The code inputs for each cell are brought in from off chip so that the clocking signals can be optimized for minimum charge injection during modulator switching. Through experiments with simple square-wave modulation signals, optimal clock levels were determined to be 1.35 and 0.9 V for the ON and OFF switch conditions, respectively. These levels straddle the threshold voltages of the switching transistors, which have increased due to the body effect caused by the -2.5-V level of V_{SS}. There are a total of eight code inputs for the four-cell array. The output of each cell is summed on a common bus with the other cell outputs and lead off chip for amplification.

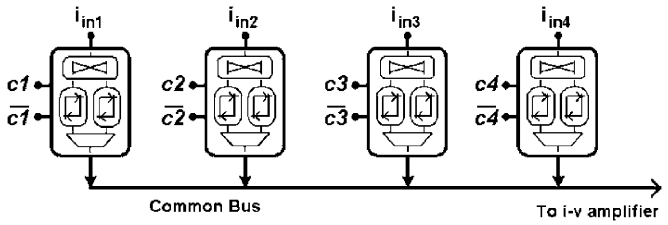

Fig. 10. Test board configured for electrical inputs. The test chip is mounted in the center of the board and wire bonded to PCB traces and planes.

The CMOS die is glued and wire-bonded to a custom printed circuit board (pcb). This chip-on-board layout allows the readout chip to interface with laboratory signal sources or with MSM photodetector elements. Fig. 10 shows the test board configured for electrical testing. The code modulation signals and electrical test input signals are brought onto the board via coaxial ribbon cables at the top and bottom edges of the board, respectively. We used a laboratory voltage signal generator followed by a large (10 MΩ) on-board series resistor to emulate a current source detector element.

Since the encoders act as current buffers with close to unity gain, the output current is very low. The board contains 10 two-stage ac-coupled amplifiers that provide a 500-kHz bandwidth with approximately 40 MΩ transresistance gain for the chip output current waveforms.

B. Experimental Verification of Roic Architecture

For simple verification of the architecture, we constructed the system shown in Fig. 11. The experiment was designed to demonstrate encoding of two independent input waveforms, their summation on the common bus, and their decoding off chip to show recovery of the original signals.

Pseudorandom codes for two channels were programmed into a digital pattern generator and from there fed into a programmable signal-conditioning instrument for level shifting and amplitude control. For simplicity, we used pn-codes of 63 b length and repeated the code four times for each set of data. The encoding signals were generated from a 50-kHz clock. Channel 2 code was simply an 8-b time-shifted version of the code used for channel 1. Although these codes are not truly orthogonal,

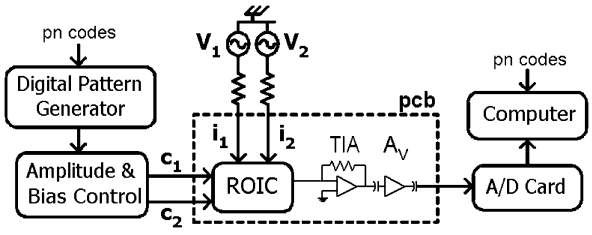

Fig. 11. Configuration of the two-channel verification experiment.

they do offer sufficient channel-to-channel isolation and are easy to implement. Two laboratory signal generators connect to the inputs of channels 1 and 2 of the readout array of Fig. 9 to provide independent current sources. The source for channel 1, V_1, was set to produce a 1-kHz sinusoid with 200-mV peak amplitude, that with the series resistor creates a 20-nA input sinusoidal current. The source for channel 2, V_2, was set at 3 kHz, also with 200-mV amplitude. The encoded and summed currents from the readout test chip are amplified off chip and digitized at the code clock rate with a data acquisition card in the computer.

The digitized composite signal from the ROIC bus is shown in left side of Fig. 12(a). The signal is composed of the two encoded sinusoids, noise added by the readout circuits, and channel-to-channel cross talk from the encoding process. The frequency spectrum of the composite signal (right) shows how the input signal energy has been spread over the code bandwidth due to the ROIC encoding process.

Fig. 12(b) corresponds to the decoded version of channel 1. The frequency spectrum (right) clearly shows that the 1 kHz component has been recovered. Similarly, for Fig. 12(c), the composite waveform was multiplied by the code for channel 2, resulting in a 3-kHz signal, clearly visible in the frequency domain.

Frequency-domain analysis is important because actual detection takes place in the frequency domain in many of the anticipated applications of this technique. The best theoretical signal-to-noise ratio (SNR) in the frequency domain should be approximately equal to the square root of the number of bits of the pn-code times the square root of the number of code repetitions [25]. For this experiment, the best theoretical SNR is $2 \cdot \sqrt{63}$ or 15.9. From the data of Fig. 12(b) and (c), we calculate the signal-to-noise ratio in the frequency domain as the ratio of the peak signal to the standard deviation of the noise floor. For channel 1, the calculated SNR is 11.8 (49.2 peak and 4.18 standard deviation) and for channel 2, it is 10.7 (45 peak and 4.22 standard deviation). These are satisfactory results for this proof-of-principle experiment considering that only few of the important system parameters have been optimized. The theoretical best value of 15.9 is based on cross talk noise due to code nonorthogonality, and does not consider electronic noise from the ROIC. In particular, we believe one of reasons for disagreement is that the $1/f$ noise from the electronics is significant and the code-rate used in the experiment is not high enough to take advantage of the noise shaping techniques presented before. For a particular application, we would employ noise-reduction circuits and fully exploit the readout architecture properties. Overall, the results verify the applicability of code modulation to readout circuits.

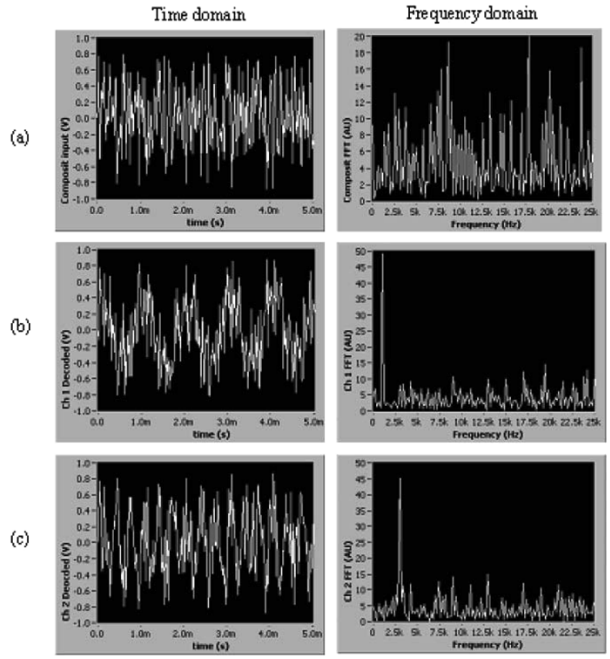

Fig. 12. Digitized ROIC output data. (a) Composite signal. (b) Decoded signal for channel 1. (c) Decoded signal for channel 2.

V. Conclusion

We have presented a novel readout scheme for active 2-D imaging systems. Depending on system requirements, our encoding architecture may be a stronger choice than a TDMA readout architecture. We obtained satisfactory results for the proof-of-principle experiment presented in this paper. A negative feature of the encoding readout technique is cross talk noise due to nonideal code orthogonality that is not present in TDMA readouts. However, the cross talk noise can be reduced by increasing the length of the code.

We think the encoding readout technique can also be advantageous for passive imaging systems, particularly systems such as longwave (8–12 μm) infrared imagers where there is a very large background flux. In longwave TDMA readout circuits, the high background flux may saturate the in-pixel integration capacitor(s), which can not be made large due to area constraints. In a passive encoding readout scheme, the integration capacitors would be located at the end of each row, where more chip area is available. Another promising application for the encoding technique is high-speed passive imaging, particularly for applications that do not require extremely high amplitude resolution.

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Jorge A. Garcia (S'99) was born in Bogotá, Colombia, in 1973. He received the B.S. degree in electronic engineering from Pontificia Universidad Javeriana (PUJ), Bogotá, in 1996. He is currently working toward the Ph.D. degree in the CMOS VLSI Research for Optoelectronics Group, Department of Electrical Engineering, University of Delaware, Newark.

From 1996 to 1998, he was an Instructor Professor in the areas of analog and digital electronics with the Electronical Engineering Department, PUJ. In 1999, he joined AANETCOM, Inc., in the area of signal processing applications for high-speed data transmission. During 2000 and 2001, he was a Mixed Signal Designer of integrated circuits for broadband communications with PMC-Sierra, Inc. His research interests include CMOS and bipolar mixed-signal integrated circuit design for high-speed data transmission, optical receivers, and readout integrated circuits for infrared imaging systems.

William Lawler joined the Army Research Laboratory (ARL), Adelphi, MD, in 1991. He is a currently a Member of the Laser Radar Team in the EO/IR Techlology Branch, ARL. His research interests include readout integrated circuits and CCD image sensors.

Nicholas Waite is currently a student in the Electrical Engineering Department, University of Delaware, Newark.

Fouad Kiamilev (M'92) is currently a Professor with the Computer Engineering Department, University of Delaware, Newark. Prior to joining the University of Delaware, he was on the Faculty of the University of North Carolina, Charlotte (1992–1999). He has published 32 journal papers and coauthored six patents and numerous conference papers. His research group is engaged in research and development of hybrid and integrated circuits related to optical sensors, communication, and information processing.