REPORT DOCUMENTATION PAGE	*Form Approved* *OMB No. 0704-0188*

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
05-04-2010	Final	09-08-2008 to 03-09-2010

4. TITLE AND SUBTITLE
Ultra-Low Power Radios for Ad-Hoc Sensing Networks

5a. CONTRACT NUMBER
W31P4Q-08-1-0011

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Alyssa Apsel

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Cornell University
373 Pine Tree Rd, EHP
Ithaca NY 14850-2820

8. PERFORMING ORGANIZATION REPORT NUMBER
OSP 56484

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Defense Technical Information Center
ATTN: DTIC-O (Technical Reports Database)
8725 John J. Kingman Road, STE 0944
Ft. Belvoir, VA 22060-6218

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approval for public release; distribution is unlimited.

20100511133

13. SUPPLEMENTARY NOTES

14. ABSTRACT
This report describes progress towards the development of radio networks with ultra-low power requirements in the range of self-powered systems and networking capabilities that are both scalable and ad-hoc. As indicated in the following sections we have achieved many of our projected milestones including demonstration of record breaking low power transmitter and receiver front ends that are robust, CMOS compatible, process tolerant, and FCC compliant at less than 20uW. At the same time, we encountered significant challenges in the design and demonstration of timing and synchronization blocks. While we were able to demonstrate synchronization of more than two radios with jitter levels better than 0.1 percent proposed, we realized that circuit level improvements needed to be initiated to demonstrate the level of timing certainty of which the system is ultimately capable. As a result of this first year of effort, we have learned many key lessons and are forging a path forward to a network of radios capable of duty cycled operation with power levels an order of magnitude lower than any comparable system shown to date and with scalability previously not considered possible in other radio networks.

15. SUBJECT TERMS
Low Power, UWB, Impulse Radio, Ad-hoc Networks

16. SECURITY CLASSIFICATION OF: a. REPORT	b. ABSTRACT	c. THIS PAGE	17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
U	U	U	UU	7	Alyssa Apsel

19b. TELEPHONE NUMBER *(Include area code)*
607-255-3962

Ultra Low Power For Ad-Hoc Sensing Networks
W31P4Q-08-1-0011 (UNCLASSIFIED)

Final Report
Reporting period – 9/8/08-3/9/10

Sponsored by:
Defense Advanced Research Projects Agency (DOD) Microsystems Technology Office

Issued by:
U.S. Army Contracting Command, Aviation & Missile Command Contracting Center
under Grant No. W31P4Q-08-1-0011

Technical Agent:
U.S. Army RDECOM, Aviation & Missile Research, Development & Engineering Center

Name of Contractor: Cornell University
PI: Alyssa Apsel, Technical Point of Contact
Business Address: Electrical and Computer Engineering
Cornell University
412 Phillips Hall
Ithaca, NY 14853
Phone: 607-255-3962
Date of contract: 9/8/08-3/9/10

Abstract:

This report describes progress towards the development of radio networks with ultra-low power requirements in the range of self-powered systems and networking capabilities that are both scalable and ad-hoc. The work described here covers the period from Septemeber, 2008 to March, 2009. As indicated in the following sections we have achieved many of our projected milestones including demonstration of record breaking low power transmitter and receiver front ends that are robust, CMOS compatible, process tolerant, and FCC compliant at less than 20uW. At the same time, we encountered significant challenges in the design and demonstration of timing and synchronization blocks. While we were able to demonstrate synchronization of more than two radios with jitter levels better than 0.1 percent proposed, we realized that circuit level improvements needed to be initiated to demonstrate the level of timing certainty of which the system is ultimately capable. As a result of this first year of effort, we have learned many key lessons and are forging a path forward to a network of radios capable of duty cycled operation with power levels an order of magnitude lower than any comparable system shown to date and with scalability previously not considered possible in other radio networks.

Project Background:

The original basis for this project was to develop a fundamentally new method for the design of a miniature, low power, low cost, radio node capable of self organization and communication within an ad-hoc network. The integrated radio transceiver combined with a backend processor in a single networkable node offers unique network scalability and record low power levels that will enable applications that are not possible with any existing sensor node platform. One unique feature of this radio, is that the proposed integrated microchip can be mass produced in a CMOS process without a costly external crystal such that the network formed by a set of homogenous nodes is robust to network changes or node failure. These characteristics enable formation of reliable, inexpensive ad-hoc networks with group intelligence and long-lifetimes.

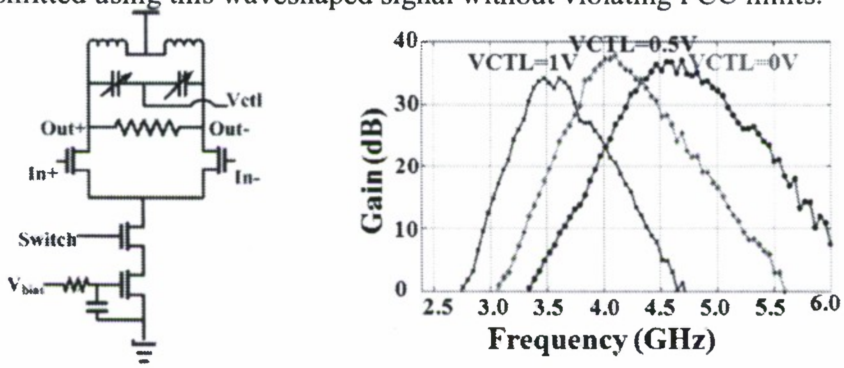
The basic requirements for such a network node are straightforward. The node should be low in cost, essentially disposable. The node should contain a bi-directional transceiver and a backend processor capable of computation and control. Most importantly, the node should operate at power levels on the order of microwatts, to enable deployment with an ultra-thin battery or harvesting power from the environment. Significant efforts have been made by others to achieve these goals. These have failed due to the difficulty of regulating low power, low duty cycle communication. In this project, we overcome this limitation by focusing on low duty cycle UWB communication and exploiting a natural biological phenomenon of Pulse Coupled Oscillators (PCOs) as characterized mathematically in [1], in our network design to provide a low power, low complexity method of regulating node to node communication.

Significant Accomplishments:

Over the past 18 months we have focused our work on three primary areas, design of an ultra-low power, duty cycleable transceiver front end, design of timing and synchronization circuits, and implementation of a low power processor in 90nm CMOS. Although we have also worked on development of power supply circuits, antenna prototypes, and communication protocols, these have not been our primary accomplishments and are not discussed here in the interest of brevity.

Transceiver Front End: Since the original proposal, we have made significant improvements to this design, resulting in a record low power, highly efficient, FCC compatible channel interface that demonstrates good interference rejection and enables transmissions up to 3 meters. The measured results of this system are reported in [2], but I will highlight them here.

The improved front end design utilizes a dual band transmission scheme not proposed in the original proposal. This new scheme enables 30dB separation between the timing pulses and data pulses, significantly reducing error probability, with little cost in area or power. This is due to the design of tunable transceiver circuits which are able to easily switch between the two transmission and receive bands. Figure 1 shows a diagram of the tunable receiver stage with the measured frequency characteristic showing excellent band isolation. Figures 2 and 3 show the dual band transmitter design and the time domain output signal of the transmitter measured at the receiver. Another improvement to our design, which is apparent in figures 2 and 3, is the addition of the use of wave shaping. In our original proposed design, we planned to simply switch the transmitter, however, this wastes transmission power in the sidelobes of the wideband signal and bumps the signal up against FCC compliance in the vicinity of the sidelobes. By using wave shaping, we confine the signal power more closely to the intended 500MHz transmission bands, and waste less transmission power while staying within FCC limits. Figure 4 shows a measured spectra from the transceiver for both the signal and synchronization bands, centered at 3.5GHz and 4.5GHz. It is clear that even more power could be transmitted using this waveshaped signal without violating FCC limits.



a.) b.)

Fig. 1. a.) Schematic of the Gain-stage of the Receiver circuit and b.) Measured gain of the circuit at different bias voltages (Vctl).

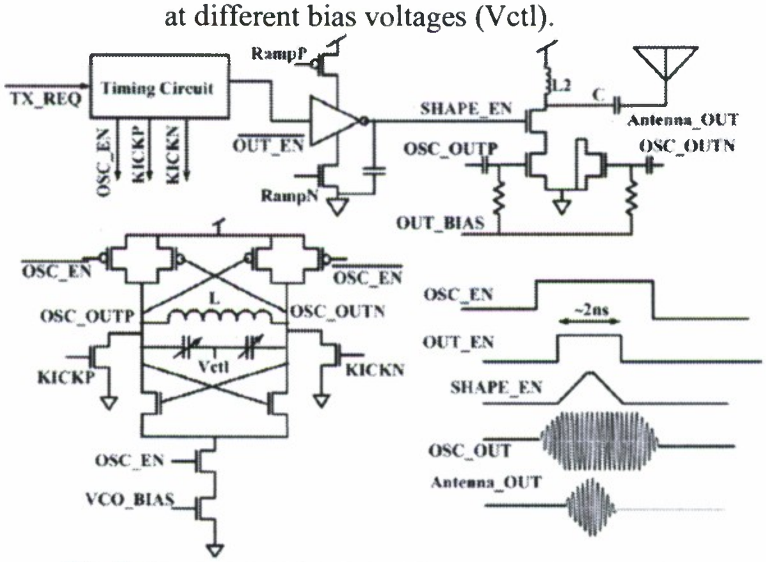


Fig. 2. Duty-Cycled LC-oscillator-based transmitter.

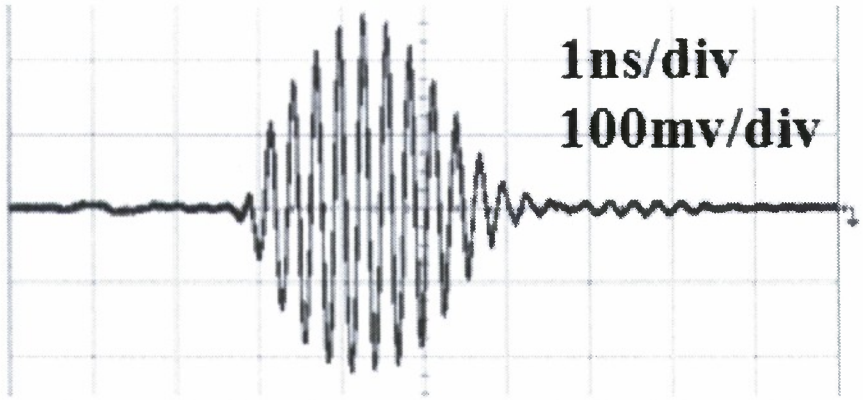


Fig. 3. Measured Transmitter Pulse shapes across a 50-ohm load, (horizontal axis is 1ns/div).

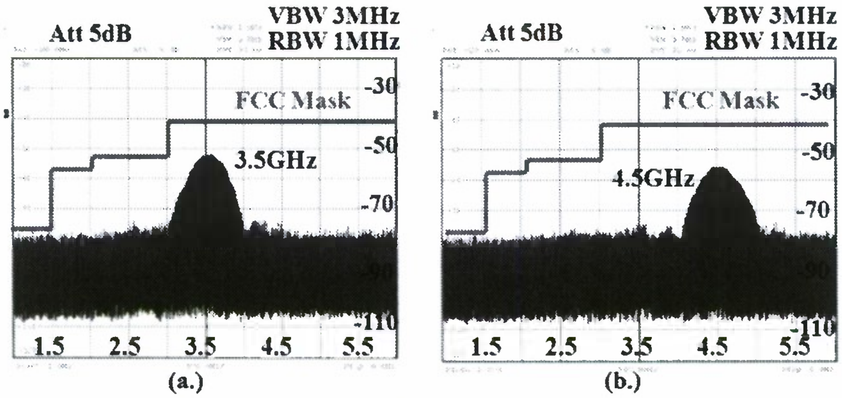
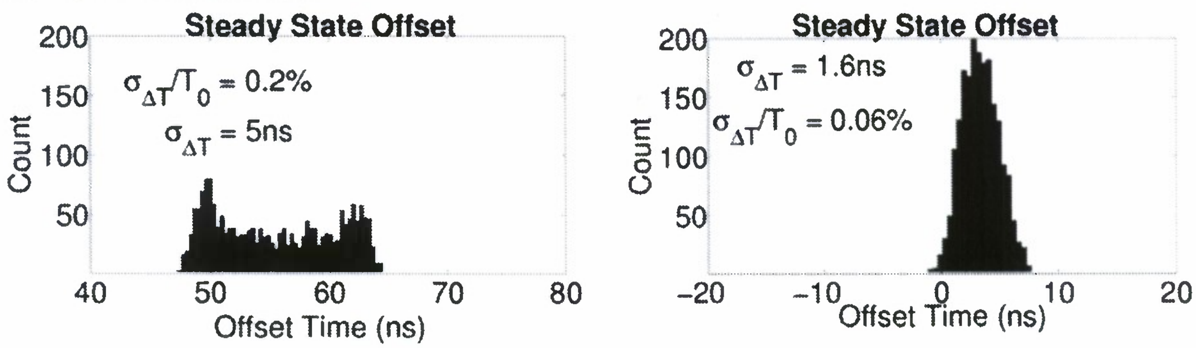


Fig. 4. Measured Transmission power spectrums @100Kbps with pulse-shaping i.e. triangular pulse shape for 3.5GHz and 4.5GHz bands

Finally one significant characteristic of this transmitter receiver pair, is it's ability to be aggressively duty cycled. Figure 3 clearly shows that 2ns pulses are easily achieved at the transmitter. We have also demonstrated detection of pulses at the receiver with an "RF on" window of as short at 3ns and BER better then 10^{-5}. These results are reported in detail in [2]. This is significant in that it will allow us to have a duty cycle window as short as 10ns, enabling duty cycling of up to 0.1% at 100KHz data rates using OOK modulation, as we proposed in our original proposal. The resulting power consumption of the front end circuits is 20uW with a sensitivity of -87dB at a BER of 10^{-5}. We can also boast a SIR of 50dB at 2.4GHz. These numbers are an order of magnitude improvement on the state of the art to the best of our knowledge.

Timing and Synchronization Circuits: Over the past year a large portion of our effort has been on the development of timing and synchronization blocks for regulation of network communications. We have made significant efforts in characterizing the PCO system, designing local oscillators and related blocks, and developing error reduction techniques and synchronization detection schemes to enable nodes to determine if they should proceed with communication. We have characterized the parameter space for synchronization of the network and have developed a set of rules governing required coupling strengths, transmission limits, and jitter limits for the nodes in the network. We have recently submitted a paper currently under review that details these findings. In addition, we have demonstrated synchronization of 3 nodes in a network. Figure 5 shows the relative offsets measured between 3 nodes synchronized to a low jitter leader node. Using sub-optimal designs, which can be significantly improved for jitter performance, we were able to demonstrate standard deviations in timing uncertainly of less than 5ns. We have determined, however, that our initial coupled oscillator designs based upon thresholded relaxation oscillators, exhibited too much timing uncertainly, and are currently in the process of fabricating an improved version that will enable us to synchronize a larger network and transmit data.



(a) (b)

Fig. 5 Measured statistics of relative offset timing between oscillators inthe PCO network. (a) node1 vs node2 (b) node1 vs node3

In addition to this work on synchronization we have developed two hardware implementable algorithms for important node tasks to improve performance. First, we have developed a method for detecting within the node if a node has been synchronized to the network so that communication can proceed. Second, we have developed a scheme to reinforce synchronization spike reception so that a single local error in reception of a coupling spike from the network does not corrupt timing. We have demonstrated both algorithms in hardware using an FPGA test setup and are currently in the process of writing a paper detailing these new methods.

Major Milestones Worked On:

- Synchronization with fully integrated CMOS electronics, demonstration of cycle-to-cycle jitter of less than 10ns for a 150KHz pulse rate (FY 2009) accomplished
- Duty cycled power <50μW for full system (FY 2009) accomplished
- 3 nodes synchronization with <1% jitter (FY 2010) accomplished
- Transmission conformance to FCC UWB standards under 802.15.4a (FY 2010) accomplished

Publications:

- X. Wang, R. Dokania, and A. Apsel, "Implementation of a Global Clocking Scheme for ULP Radio Networks", Proceedings of the International Conference on Circuits and Systems, Taipei, Taiwan, May 2009
- A. Apsel, R.Dokania, X. Wang, "Ultra-Low Power Radios for Ad-Hoc Networks", Proceedings of the International Conference on Circuits and Systems, Taipei, Taiwan, May 2009 (Invited)
- R. Dokania, X. Wang, S. Tallur, C. Dorta-Quinones, A. Apsel, "An Ultra-Low-Power Dual-Band UWB Impulse Radio," IEEE Transactions on Circuits and Systems II, accepted for publication, March 2010.
- R. Dokania, X. Wang, C. Dorta-Quinones, W. Godycki, S. Tallur and A. Apsel, "A 6μW, 100Kbps, 3-5GHz, UWB Impulse Radio Transmitter", accepted International Symposium on Low Power Electronics and Design (ISLPED), Austin, TX, August 2010.

- X. Wang, R. Dokania, A. Apsel, "PCO Based Synchronization for Ad-Hoc Duty-Cycled Impulse Radio Sensor Networks", Submitted to special issue on cognitive sensor networks of IEEE Sensors Journal.

Lessons Learned:

Going forward, we have learned several things that have informed our future research. Primarily, we have learned that our designs of several pieces of the timing block had significant flaws. This was a result of two factors. First, we trusted our design tools to give good estimations of the noise in these circuits from which we could determine jitter characteristics. In fact, these tools rely heavily on linear approximations of circuit behavior, and the non-linearities in these particular circuits, due to their unique low frequency, low power behavior, excited responses not well characterized by the tool. Second, we did not provision in our design for this level of inaccuracy in the models by providing more knobs in the circuit that could be tuned or changed after the fact. Since realizing these two problems, we have improved our characterization tool, and understand the regime in which our noise models cannot be relied upon and we have added some additional tunability. Both of these tasks are accomplished in the next generation design which we recently sent for fabrication.

Recommendations for a Path Forward:

As we proceed with our project, we believe that we are progressing well along our initial path, and have left some room for improvements in design and mitigation of unforeseen pitfalls. While we still believe that our initial basis for design of a network of radios using PCO synchronization is sound, there are several things that could be improved as we move forward. We recommend adding the following to our initial and continuing approach to this project.

- Continued examination of the impact of jitter on network synchronization and better ways to characterize jitter in non-linear circuits.
- Investigation of hardware solutions to improve interference rejection for in-band interferers.
- Working to develop protocols for network communication and antenna designs.

References:

[1] R. E. Mirollo and S. H. Strogatz, "Synchronization of pulse-coupled biological oscillators," SIAM J. Appl. Math., vol. 50, no. 6, pp. 1645–1662, Dec. 1990.

[2] R. Dokania, X. Wang, S. Tallur, C. Dorta-Quinones, A. Apsel, "An Ultra-Low-Power Dual-Band UWB Impulse Radio," IEEE Transactions on Circuits and Systems II, accepted for publication, March,2010.