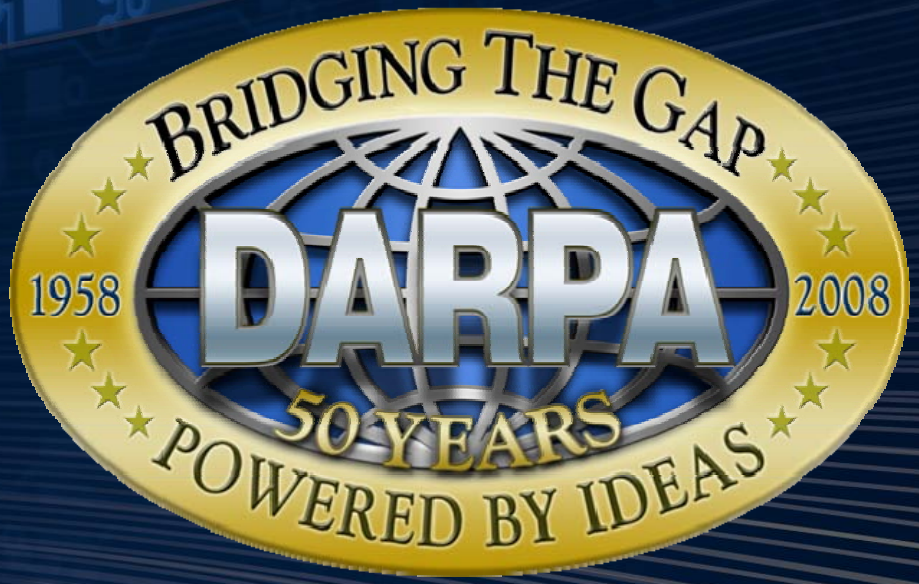
“Advanced Silicon Technology Foundry Access Strategy for DoD Research”



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DARPA MTO Office

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Statement of Problem & Goals

- **DoD researchers require reliable access to state of the art on-shore silicon foundry technologies**

- **Today's access options for SOA technologies are inadequate**
  - **DoD researchers risk falling behind other parts of the world where research access is easier**

- **TODAY's GOAL: get input from DoD research community as input for helping DARPA develop a reliable access plan**
  - **Important distinction between projects requiring "trusted" flows and those that do not**
  - **Willing to accept partial or incomplete design kits for SOA technologies**

Some Recent Access Examples

- **TEAM Program**
  - **TAPO access (90 nm CMOS & 130 nm BiCMOS)**
  - **Advanced Si-based RF research**

- **Rad-Hard-By-Design Program**
  - **TAPO access for 90 nm CMOS**
  - **“special” access to 45 nm SOI CMOS**

- **DARPA Seedlings**
  - **Cost effective TAPO access to 90 nm CMOS and 130 nm BiCMOS**

- **FCRP Program (SRC/DARPA funded)**
  - **Cost effective TAPO access to 90 nm CMOS and 130 nm BiCMOS**

- **Trust Program**
  - **MOSIS access(90nm CMOS)**

DARPA TEAM PROGRAM:

60 GHz RF-CMOS Rx (TEAM; UCB)

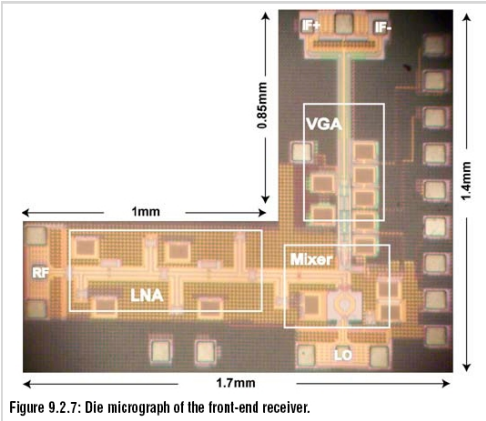
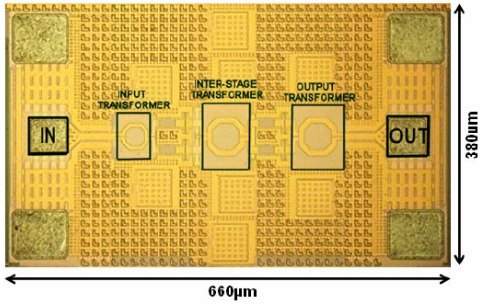


Figure 9.2.7: Die micrograph of the front-end receiver.

90 nm RF-CMOS

G_{Pwr}= -8 to +55dB
NF = 6.2 dB
P_{1dB}(in) = -26 dB
Pwr = 24 mW
V_{dd} = 1V

Transformer coupled Si-CMOS PA (TEAM; UCB)

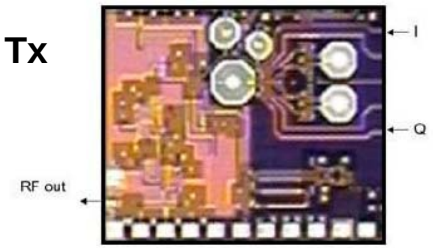


90 nm RF-CMOS

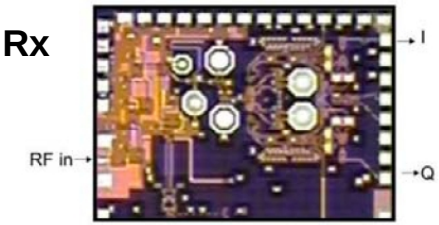
V_{dd} = 1 V
P_{1dB} = +9 dB
P_{Sat} = +12.3 dB
Area = 660 x 380 um^2
PAE = 8.8%

60 GHz RF-CMOS Radio (TEAM; GTech)

Tx



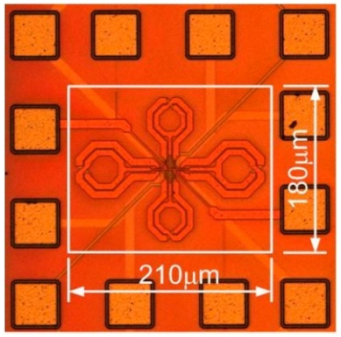
Rx



90 nm RF-CMOS

TP = 7 Gb/s (QPSK)
TP = 15 Gb/s (16QAMM)
Pwr = 200 mW

324 GHz RF-CMOS Oscillator (TEAM; UCLA)



90 nm RF-CMOS

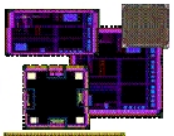
Linear superposition of four phase-shifted fundamentals generating output at $4\omega_0$

Pwr = -41 dB

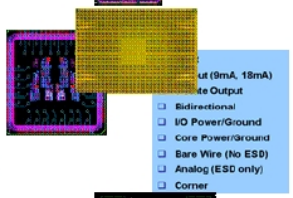
Rad-Hard-By-Design Program

90 nm RHBD Library Development

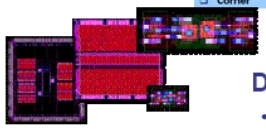
Standard Cell Libraries
- 1014 Cells
- Low Power & High Speed Variants



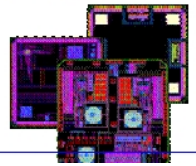
I/O Libraries
- 500MHz LVDS
- C4
- Wirebond
- 2.5V, 3.3V tolerant



SRAM
- 1Mrad
- 500Krad
- 6 Types
- Generator in work



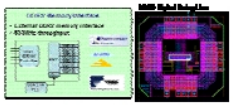
PLL
- Clock
- SERDES
- DDR2



ASIC Design Flow

Development Step	Data Included
Synthesis	• Liberty Format Files (.lib) • Synopsys Data Base File (.db)
Simulation	• Verilog simulation models • VHDL VITAL simulation models • Cadence schematics
Placement & Routing	• Cell physical geometry • Cell frame views • Cell timing views • Cell power views • Technology file
Verification	• Cell SPICE netlist • Verification decks version
Support Data	• Cell Datasheets • Models & Designs rules version

DDR 1 & 2 Interface
- High bandwidth external storage interface



SERDES
- 10Gbit/sec Ethernet
- Supports XAUI & PCI Express

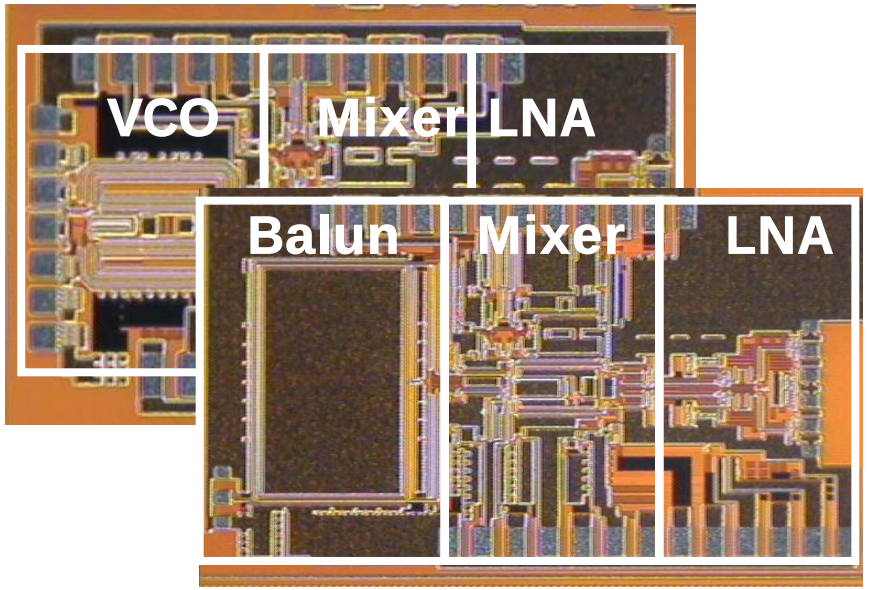
45 nm SOI exploration

Space System Applications

Examples

Dr. Charles Sodini (MIT): Receiver Systems for Active and Passive Millimeter-Wave Imaging (FCRP)

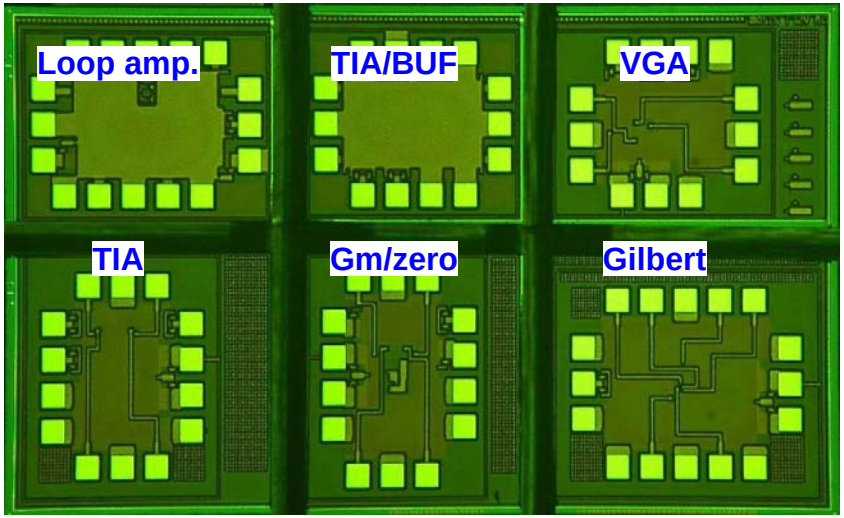
Technology: SiGe BiCMOS 8HP

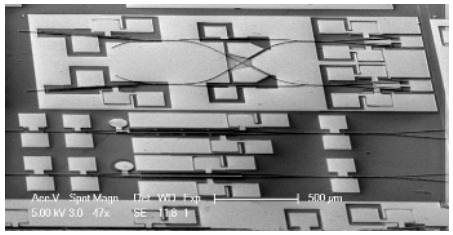


	LNA	Mixer/IF Amp	VCO	Accumulative
Gain	18-26 dB	20-26 dB		35-46 dB
Noise	4.9-6.0 dB	12-14 dB	-93 dBc/Hz	8-9.9 dB
Power	55 mW	67 mW	73 mW	195 mW

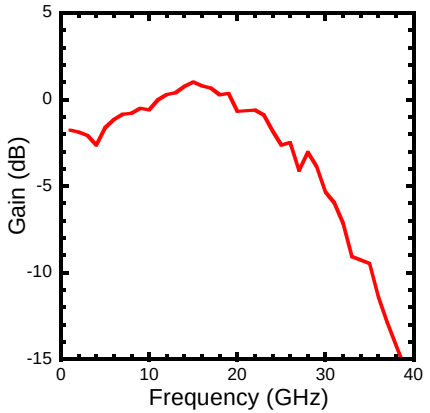
Dr. Mark Rodwell (UCSB): Optical PFLL: Optical Phase-Frequency Locking (DARPA PHOR-FRONT)

Technology: SiGe BiCMOS 7HP





Measured TIA Gain



Current DARPA Program IC Foundry Enablement

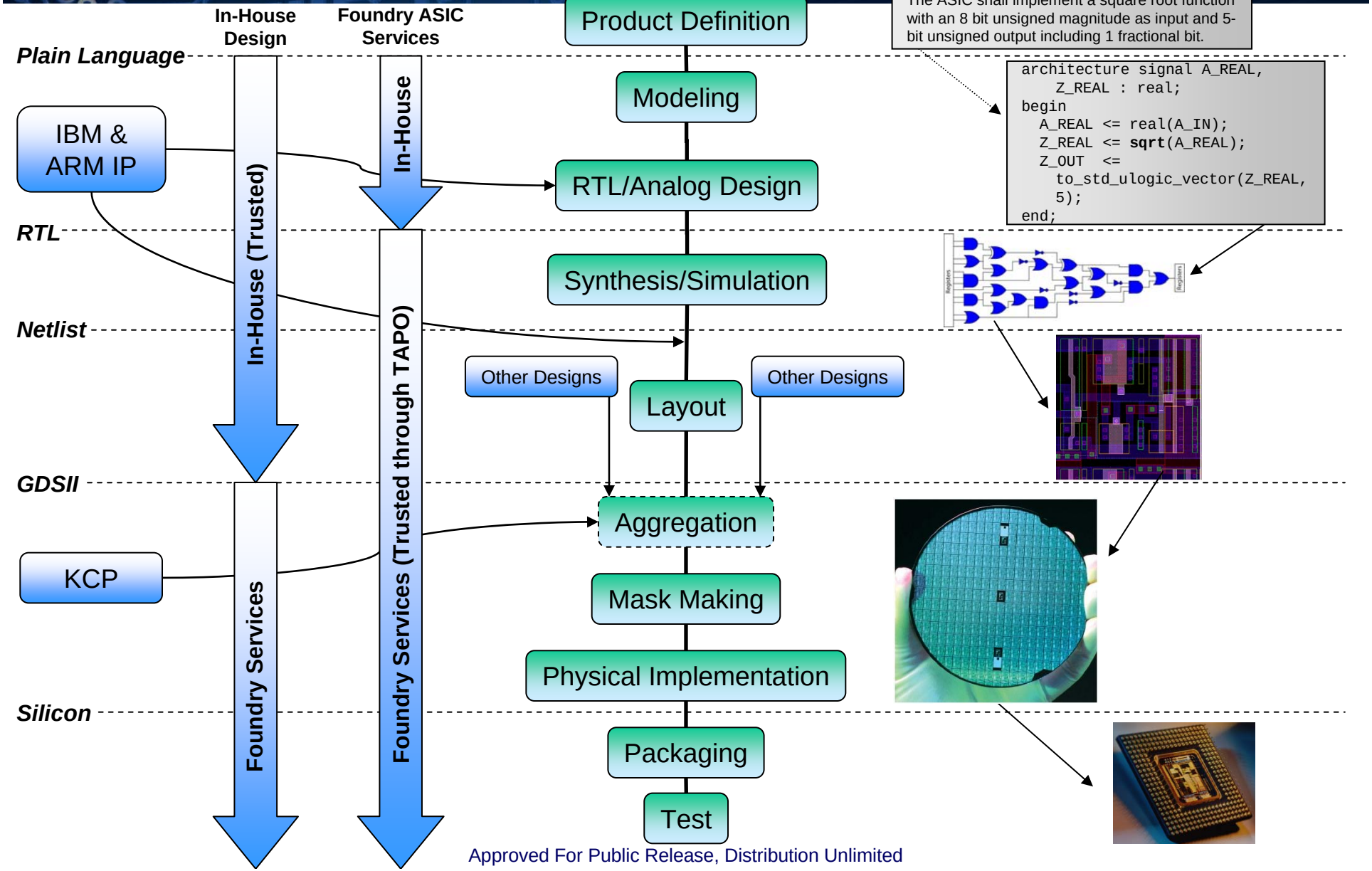
Saverio Fazzari

Outline

- Requirements
  - Projects need cost effective and reliable technology access for IC fabrication
  - Multiple process node support desired

- **Primary options**
  - **TAPO**
    - **DOD sponsored IBM access with cost**
    - **Limited runs & limited SOA technology**
  - **MOSIS**
    - **Large MPW schedule**
    - **Costs & limited SOA technology**
  - **Custom Foundry relationships**
    - **Large access to specific foundry technologies**
    - **Costly for PI to maintain relationship; limited PI pool**

IC Design Flow and TAPO



TAPO MPW Runs

FY09 MPW Program Schedule

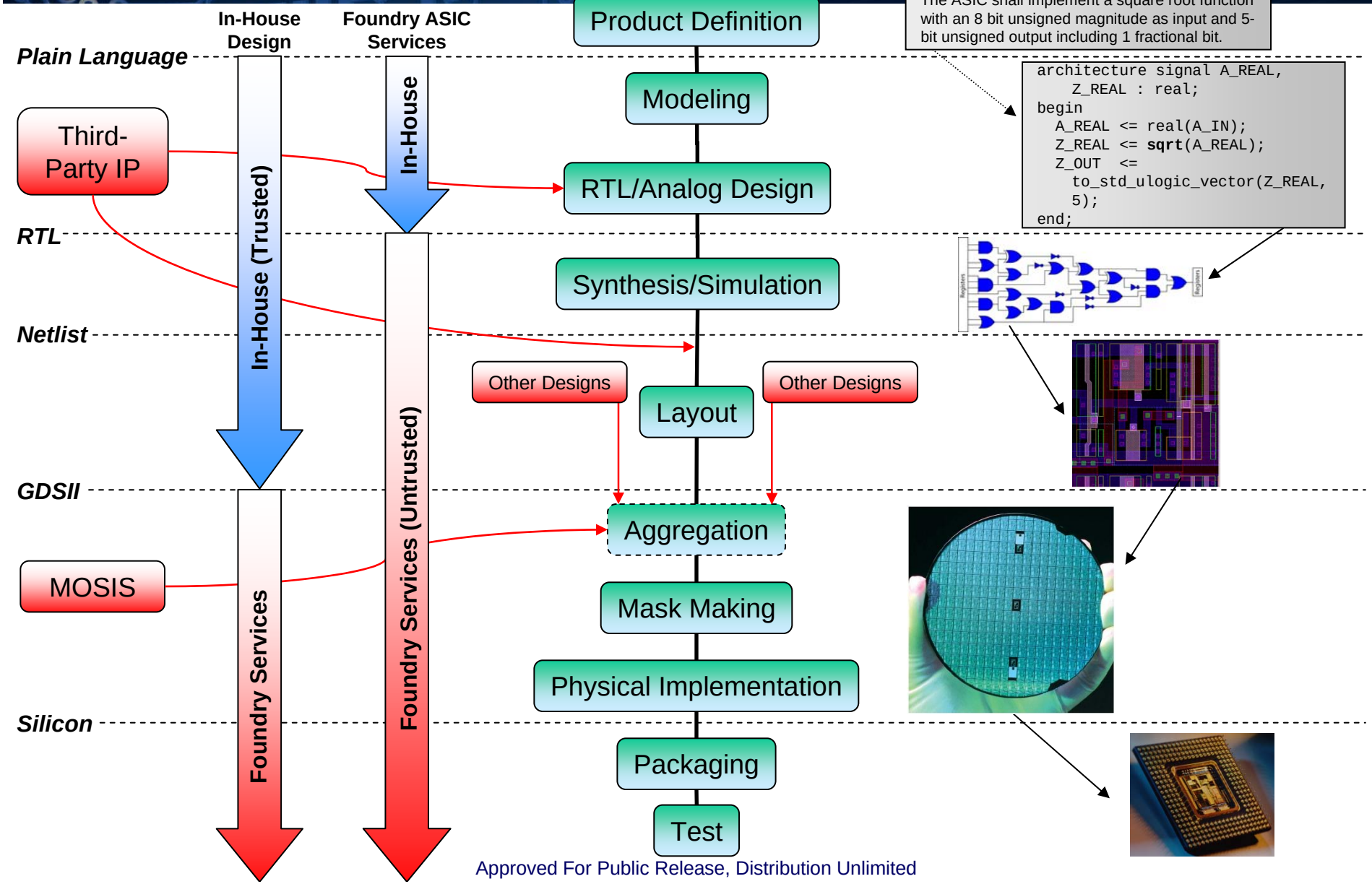
as of September 9, 2008

Technology		Quarter 1			Quarter 2			Quarter 3			Quarter 4		
		Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep
8HP	130nm	10/01/08 8HP09A		12/08/08 8HP09B		02/09/09 8HP09C				06/08/09 8HP 09D			09/08/09 8HP09E
8RF	130nm		11/03/08 8RF09A				03/09/09 8RF09B		05/26/09 8RF 09C			08/10/09 8RF09D	
9SF	90nm			12/01/08 9SF09A				04/06/09 9SF09B			07/13/09 9SF09C		
7HP	180nm	10/27/2008 7HP09A						04/20/09 7HP 09B					
9LP	90nm								05/04/09 9LP09A				
10SF	65nm					02/23/09 10SF09A*							

* Fully Customer-Funded Run (Taxi-Run)

There have been advanced runs including 45 nm SOI (12S0)

IC Design Flow With MOSIS



MOSIS MPW INFO

AMIS

- **The AMIS fabrication schedule includes MPW runs in the following processes: 1.5 µm CMOS, 0.7 µm high voltage CMOS, 0.5 µm CMOS, and 0.35 µm high voltage CMOS.**

austriamicrosystems

- **The austriamicrosystems fabrication schedule offered by MOSIS include 0.35 µm CMOS, high voltage CMOS, and SiGe BiCMOS processes.**

IBM Fabrication Schedule

- **The technologies included in the IBM MPW fabrication schedule range from 45 nanometer to 0.25 µm in CMOS, and from 0.13 µm to 0.50 µm in SiGe BiCMOS.**

TSMC Fabrication Schedule

- **Multiproject wafer (MPW) runs available through TSMC include 0.35 µm CMOS, 0.25 µm CMOS, 0.18 µm CMOS, and 0.13 µm CMOS.**

Info from www.mosis.com