Chip-Scale Energy and Power… and Heat

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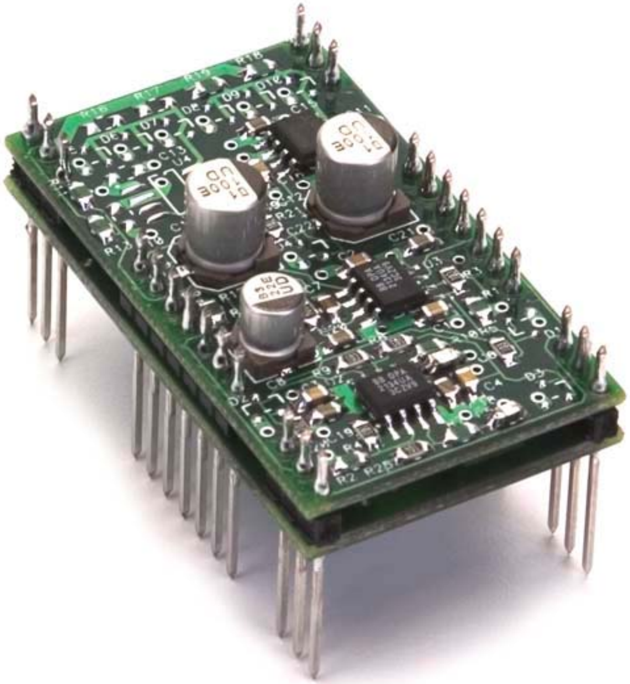
Getting the Heat Out

Dr. Thomas Kenny
DARPA/MTO
March 4, 2009

MICROSYSTEMS TECHNOLOGY OFFICE



Exciting Technologies

Exciting Technologies

Packed into Tiny Systems

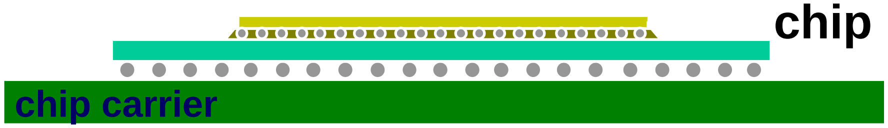
Exciting Technologies

Packed into Tiny Systems

Generating a lot of Heat!

Microelectronics Packaging Today

- Best modern technology in the electronics layer

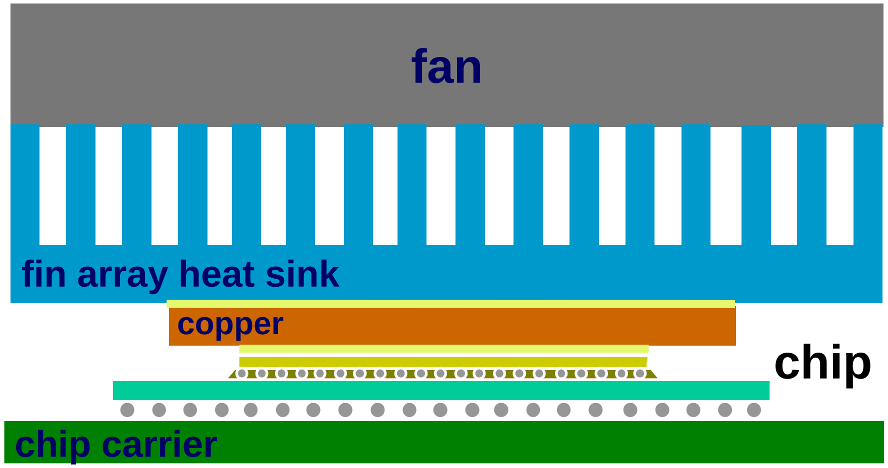


Microelectronics Packaging Today

- **Best modern technology in the electronics layer**

Ancient "technology" in the thermal layer

(side view)



Microelectronics Packaging Today

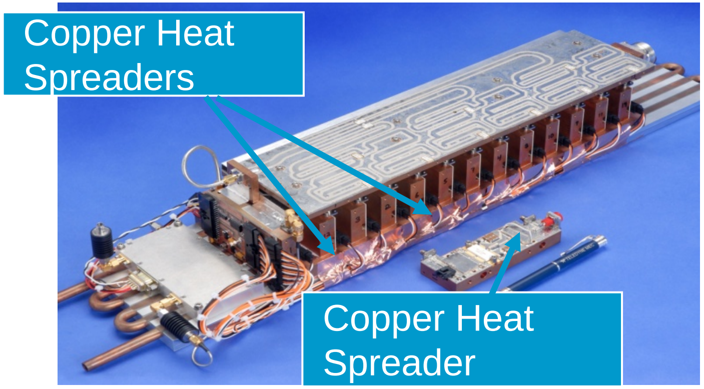
The growing size of the thermal solution is a source of :

- Mechanical failure problems
- Weight problems
- System size for multi-processor systems (servers)
- Significant added cost
- Reliability problems (fan)
- Crowding away the power conditioning elements

Things are bad in the commercial sector, and MUCH WORSE in the DoD…

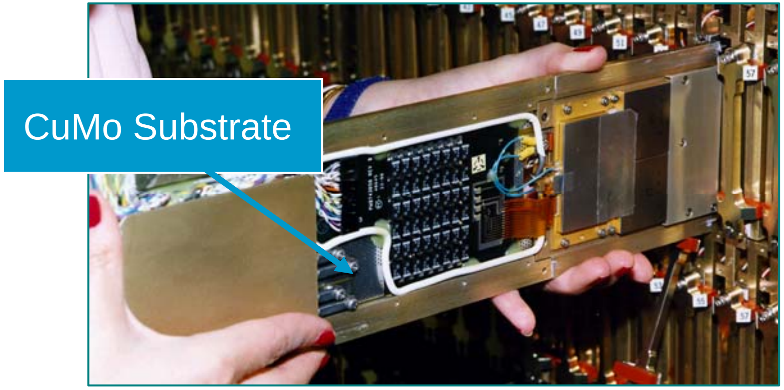
Examples of DoD Systems Constrained by Thermal Management

Teledyne's ALQ-99
TWT Replacement Module



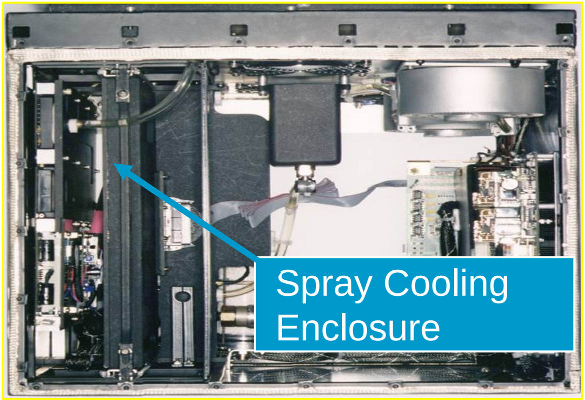
Solid Copper Spreaders used on High-G Platforms add Significant Weight to Avionics

Raytheon's High Power Density Phased Arrays



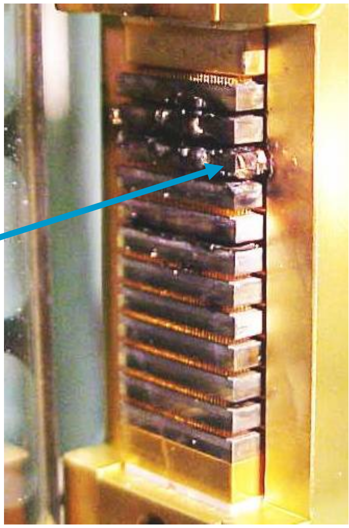
CuMo MCM Substrates Prevent Further Power Scaling in Array Radar Systems

Cray J90 Airborne Computer



Large, Heavy, Complex Facilities for Spray Cooling

Diode Laser Bar
Thermal Overload



Solder Interface Imposes High Assembly Temperature or High Thermal Resistance

DARPA Approach to Thermal Management Challenges

Industry :
Facing Increased Performance Requirements from DoD
Describing Increased Thermal Management Challenges

Metrics
Constraints
PIs and Transition Partners

Academia
(Focus Center Research Program) :
Device and Fabrication Challenges ‘ from Industry and ITRS
Crazy Ideas, Patient Students

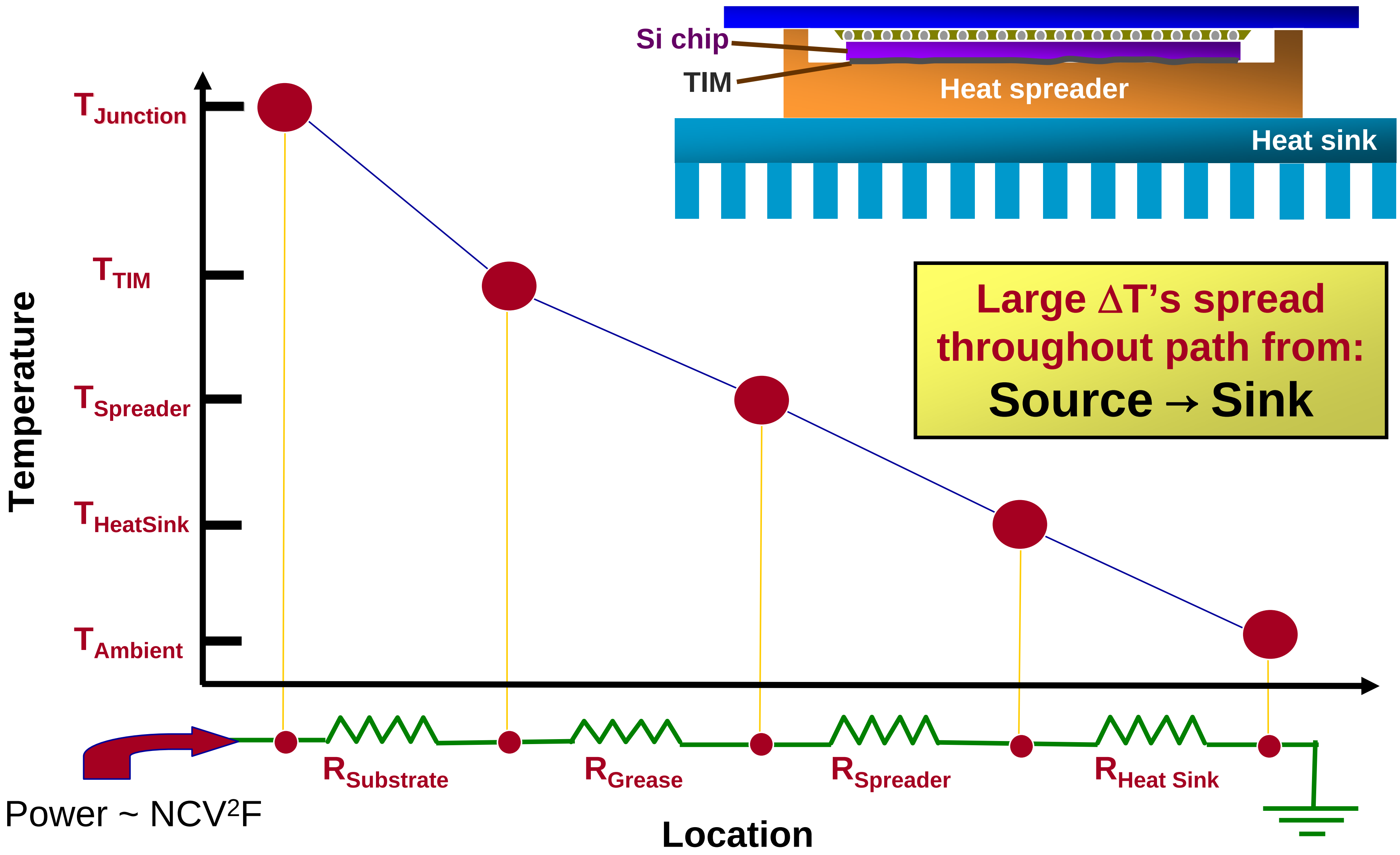
Concepts
Prototypes

Academia
(N/MEMS S&T Fundamentals) :
Materials and Nanostructure Challenges from Industrial partners
Crazy Ideas, Patient Students

New Materials
New Physics

DARPA Thermal Management Programs

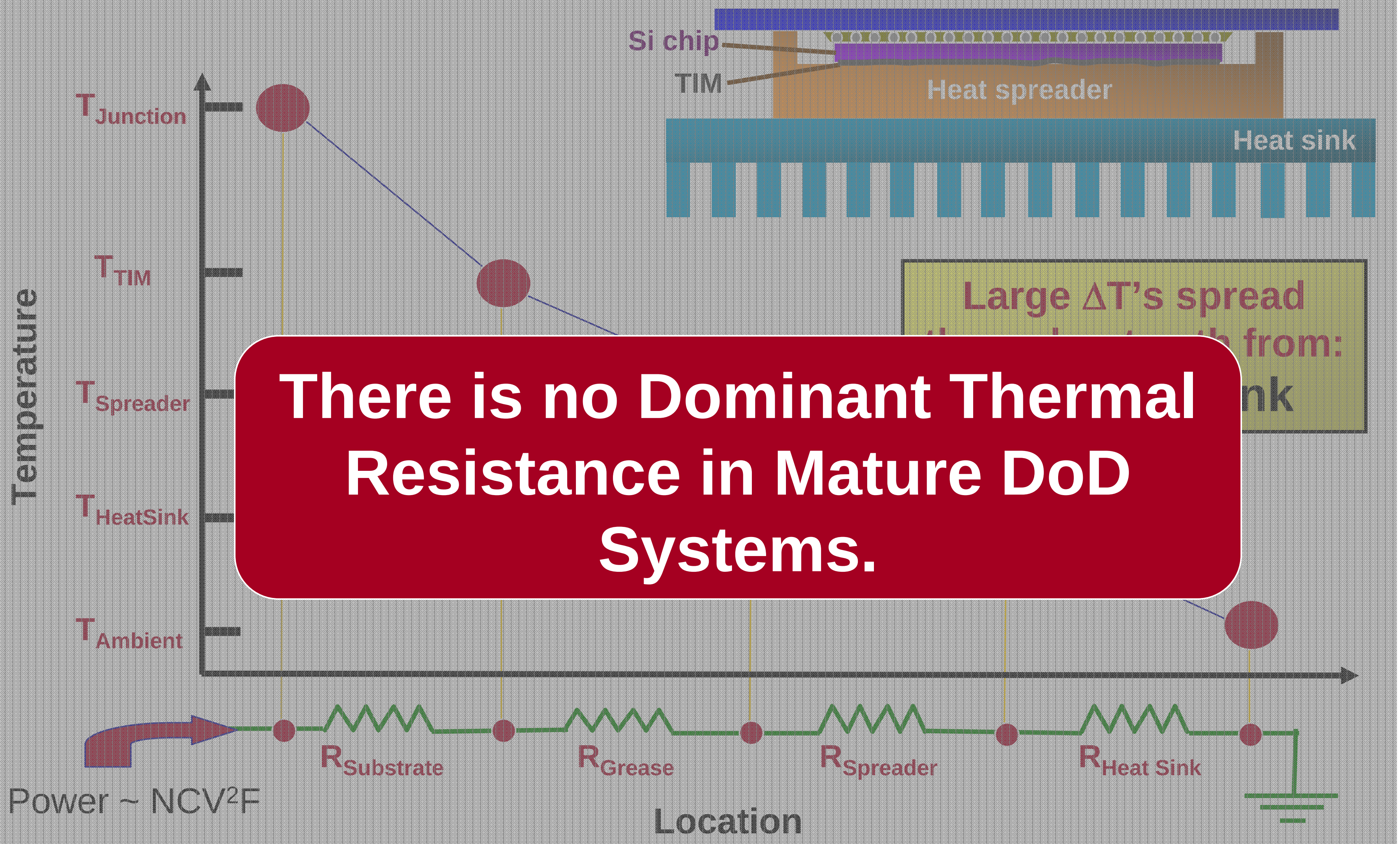
Thermal Resistance Breakdown
Where is the Problem?



Large ΔT's spread throughout path from:

Source → Sink

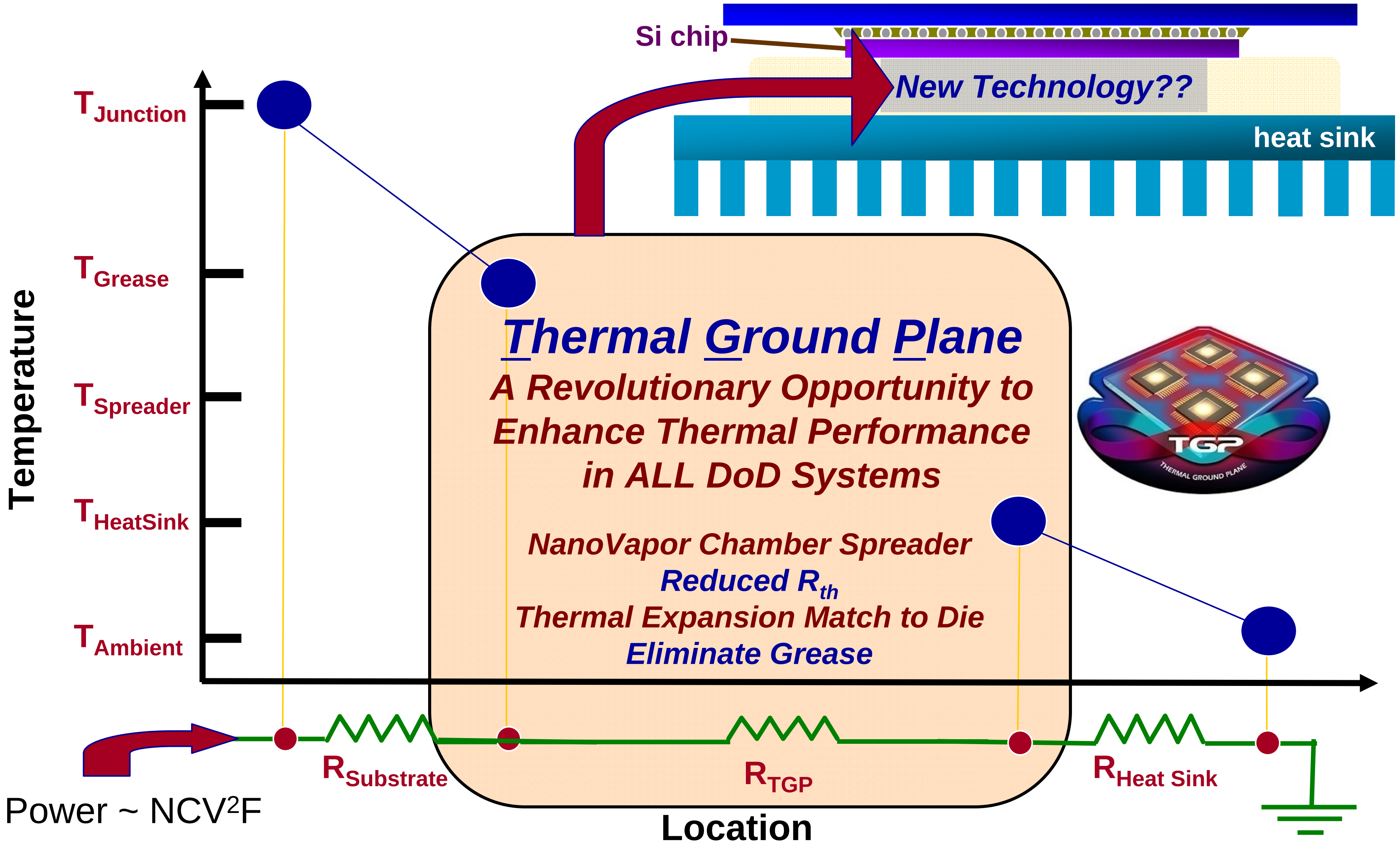
Thermal Resistance Breakdown
Where is the Problem?



Large ΔT's spread … from: … nk

There is no Dominant Thermal Resistance in Mature DoD Systems.

Thermal Ground Plane (TGP)



***T**hermal **G**round **P**lane*

A Revolutionary Opportunity to Enhance Thermal Performance in ALL DoD Systems

NanoVapor Chamber Spreader

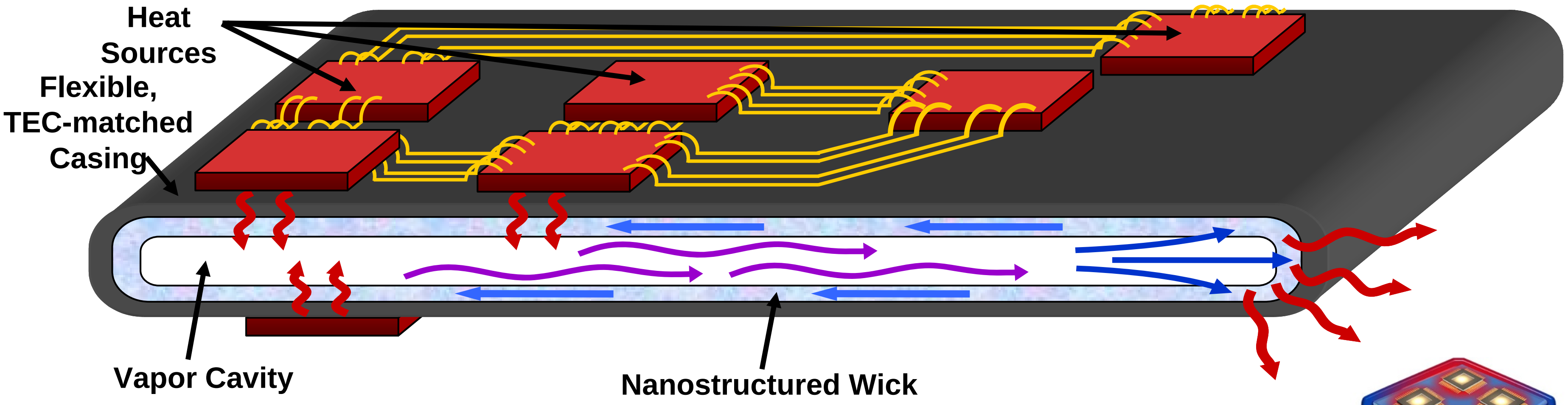
Reduced R_{th}

Thermal Expansion Match to Die

Eliminate Grease

Thermal Ground Plane (TGP)

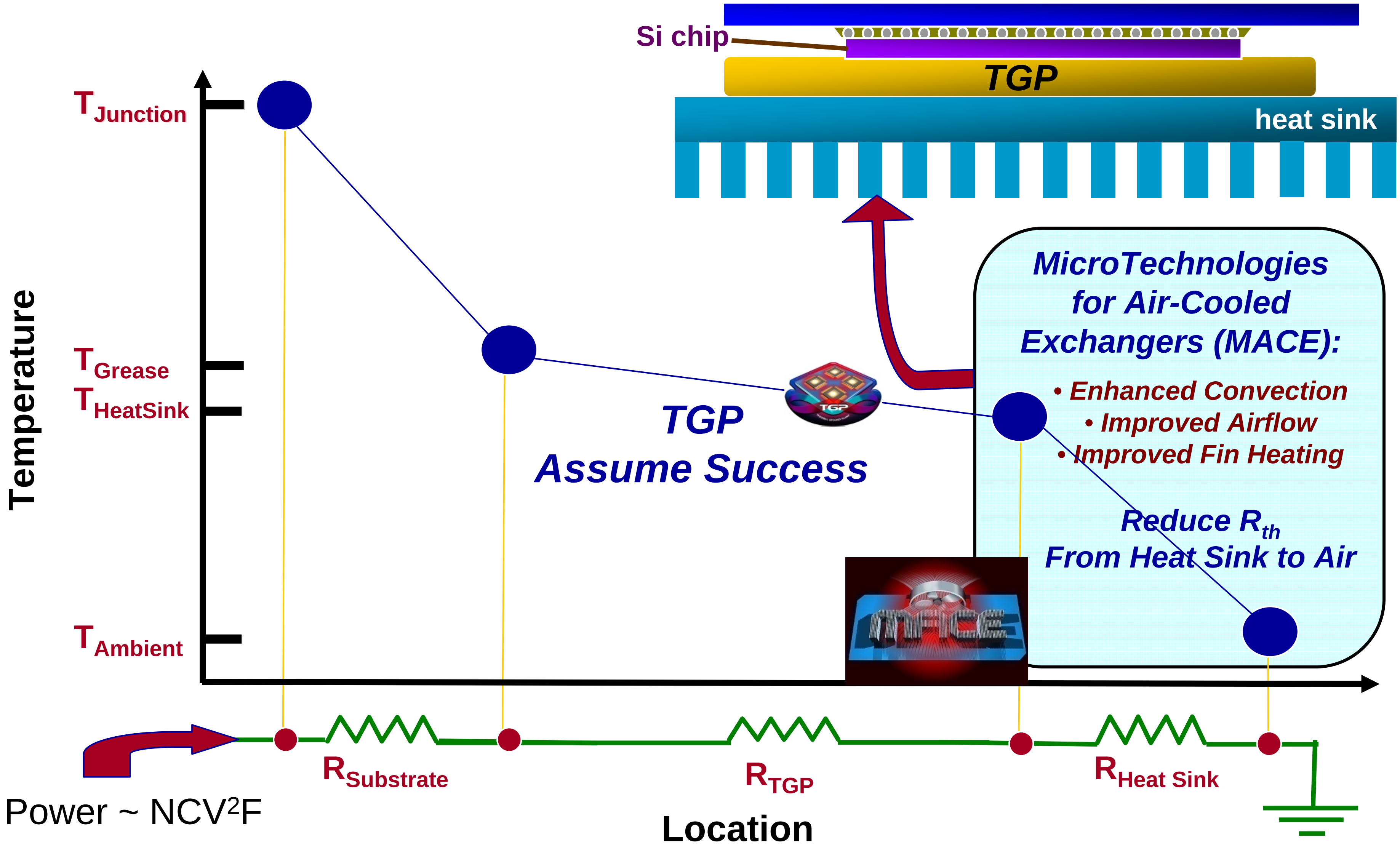
***TGP Program Vision* :** **A new 2-D, thin, lightweight MCM substrate incorporating modern and nanostructured materials to achieve vastly superior thermal conduction & possessing all mechanical properties necessary for hard-mounting ICs.**



- Extreme lateral thermal conduction, 100X above current MCM substrates
- Large 2-D area, <1 mm thick, Operation up to 20g
- Nanostructured wick for enhanced heat transfer and fluid transport
- Structural, flexible, thin, & light-weight materials that match the TEC of Si, GaAs, or GaN
- 2-phase heat transfer to eliminate load-driven thermal non-uniformity across substrate

Program Kickoff 1/08

A New Thermal Opportunity



TGP
Assume Success

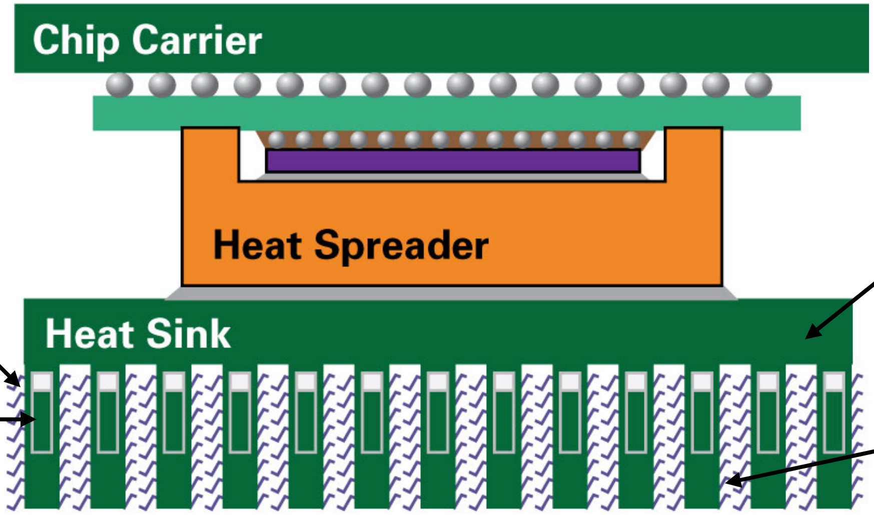
MicroTechnologies for Air-Cooled Exchangers (MACE):

- *Enhanced Convection*
- *Improved Airflow*
- *Improved Fin Heating*

Reduce R_{th}
From Heat Sink to Air

Microtechnologies for Air Cooled Exchangers (MACE)

***MACE Program Vision* :** **Develop new technologies to enhance the performance of heat sinks by reducing thermal resistance and airflow resistance. MACE will enable lighter, more compact systems with better thermal performance. MACE complements the Thermal Ground Plane (TGP) program.**



Nano-textured fins to enhance convection surface area & turbulence.

Micro-pump integrated micro-channel heat sink.

High conductivity, low density material (graphene /Cu, graphite /Al, etc). TGP could go here.

MEMS flaps, jets, other ideas to enhance airflow throughout heat sink

MACE Goals:

- **Reduction in Thermal Resistance from Heat Sink to Air**
- **Reduction in Airflow Resistance through Heat Sink**
- **Use of Direct Air Cooling in Dense High-Power Systems**
- **Reduced Power Consumption in Cooling Systems**

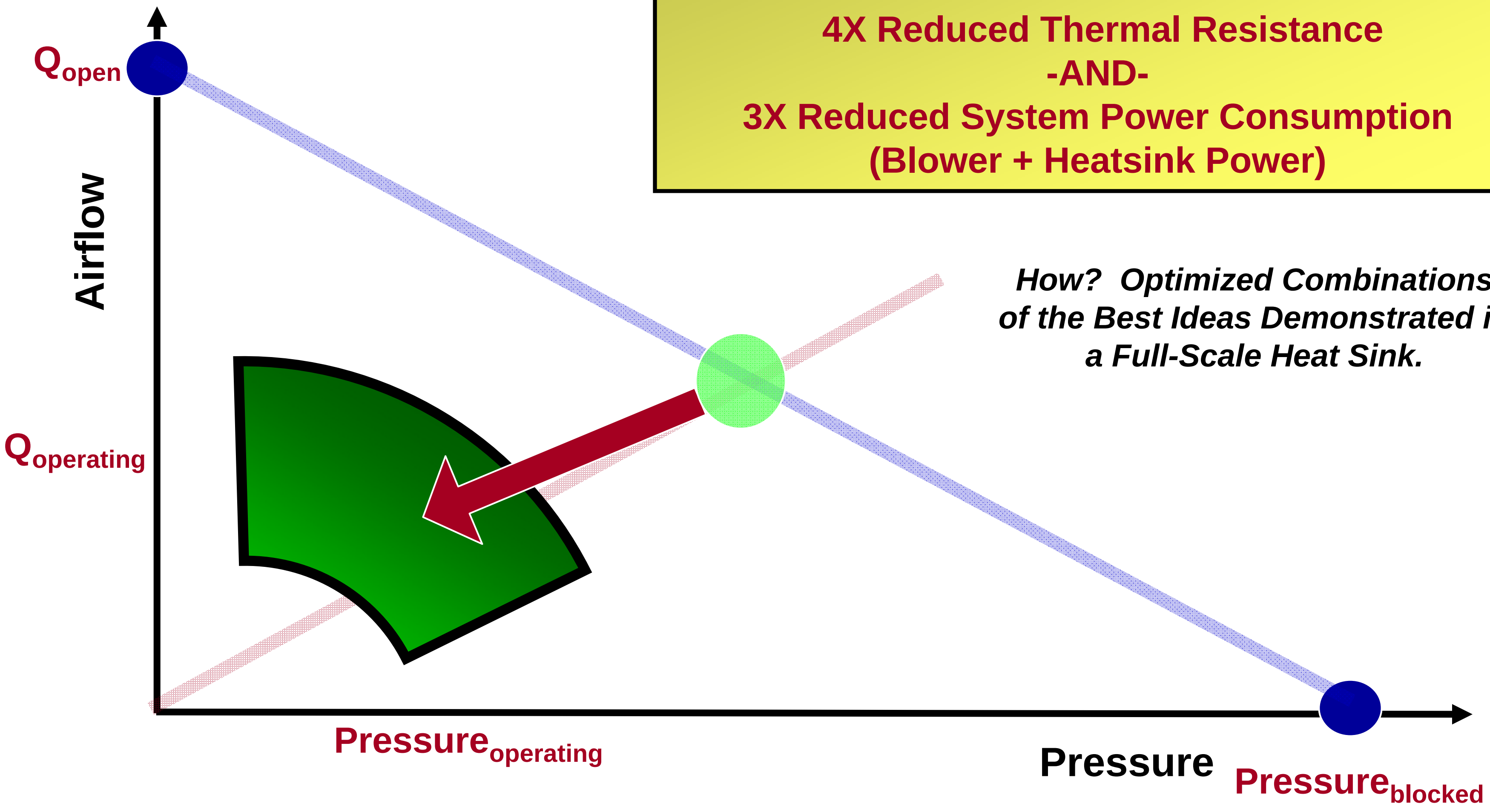
Program Kickoff 1/09.

MACE Program Goals

MACE Goals :

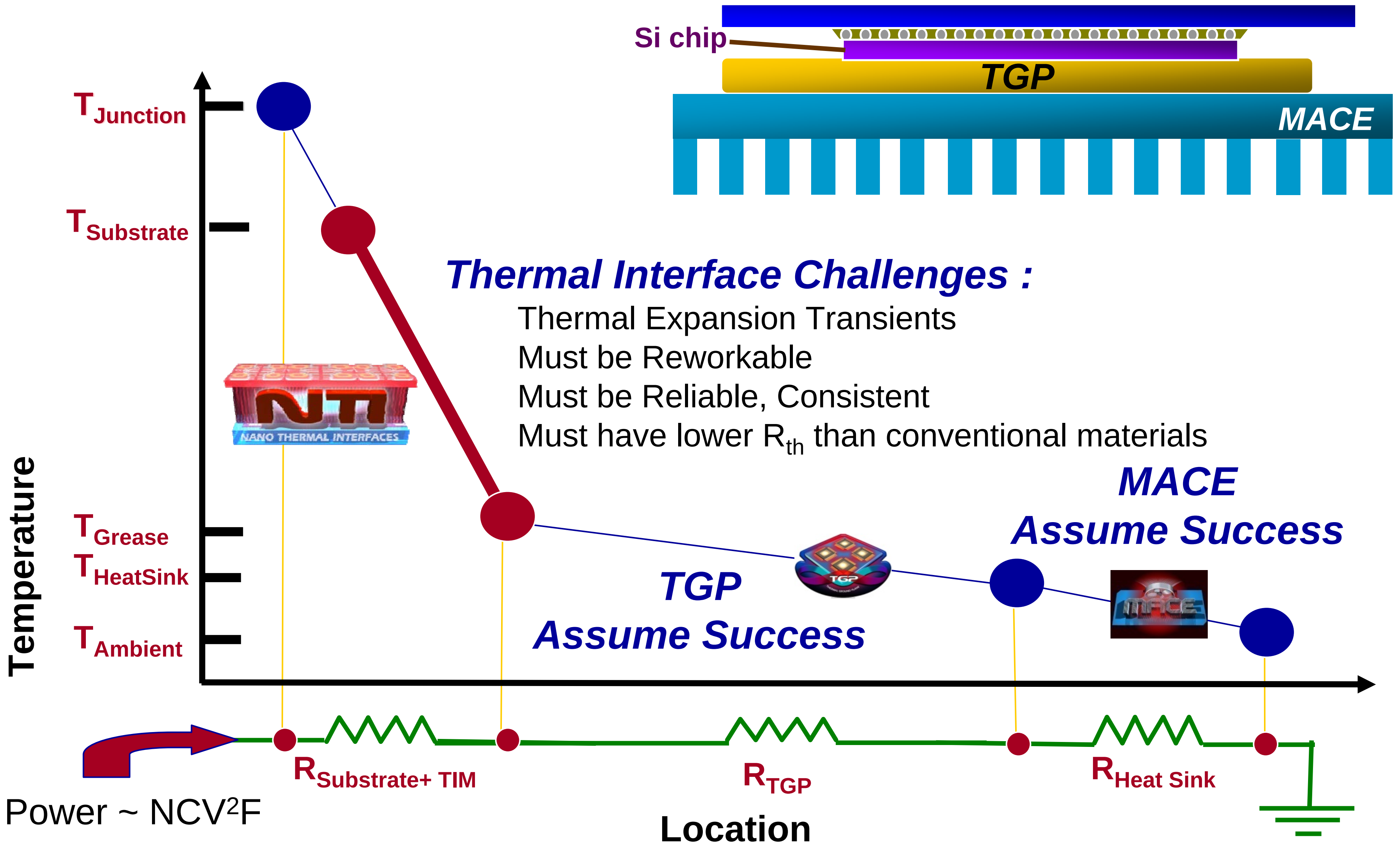
Enable New System Operating Points
At Better Performance and Lower Power

4X Reduced Thermal Resistance
-AND-
3X Reduced System Power Consumption
(Blower + Heatsink Power)



How? Optimized Combinations of the Best Ideas Demonstrated in a Full-Scale Heat Sink.

The Next Thermal Opportunity



Thermal Interface Challenges :

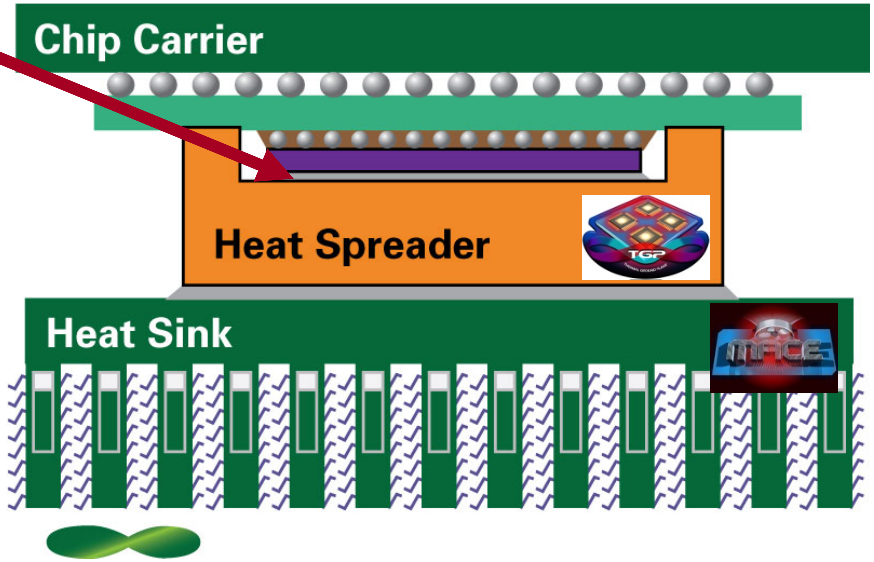
- Thermal Expansion Transients
- Must be Reworkable
- Must be Reliable, Consistent
- Must have lower R_{th} than conventional materials

MACE
Assume Success

TGP
Assume Success

NanoThermal Interfaces (NTI)

Thermal Interface materials (TIM):



Resistance of thermal interface materials – emerging bottleneck in thermal management of all DoD systems.

Success in TGP and MACE will shift focus to this layer.

Existing solutions (epoxy, grease, In, Solder) Not Doing the Job!

TIM Must Haves :

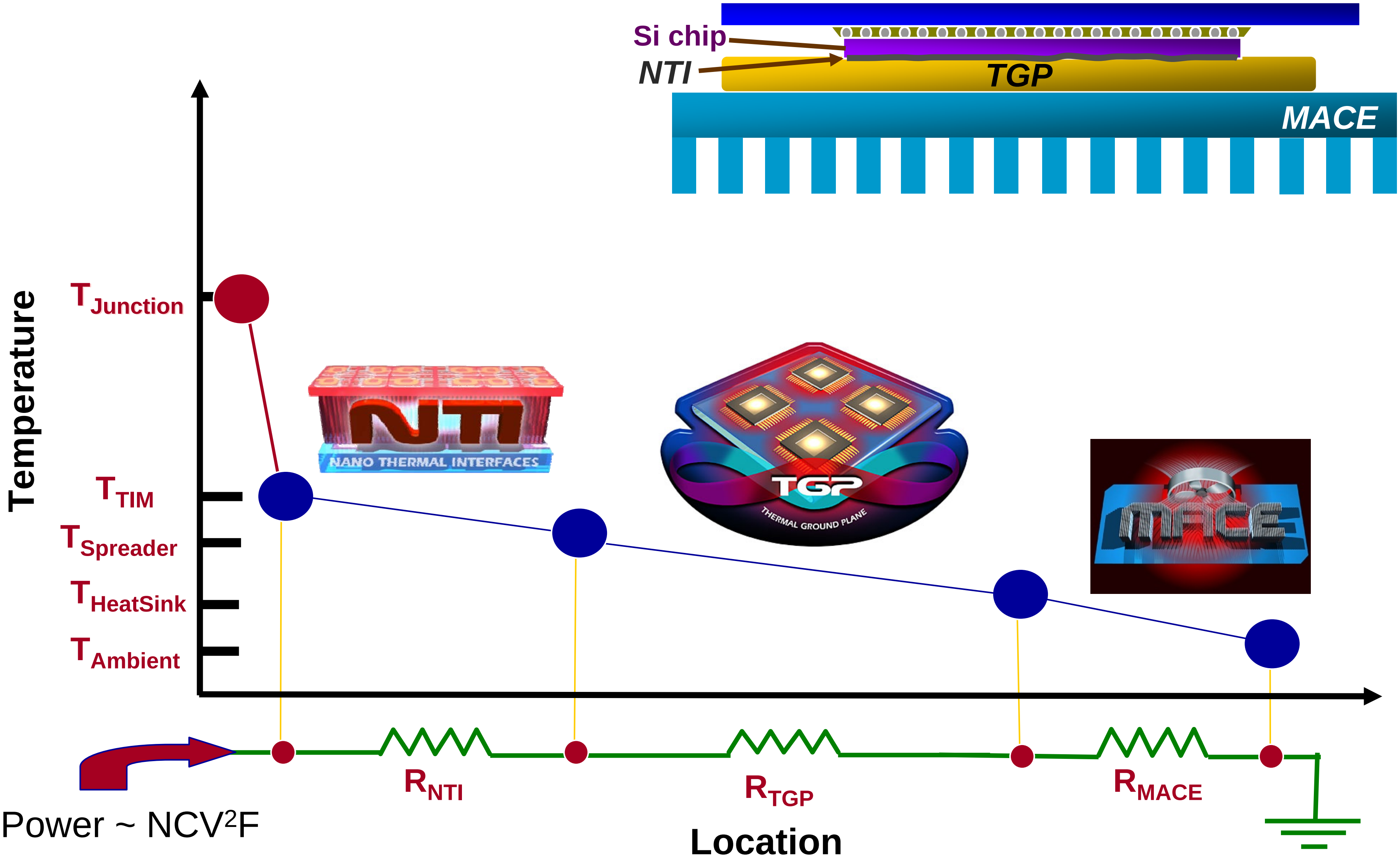
- **Lower Thermal Resistance (10 W/m•K typical. 5x reductions would be valuable)**
- **Easily Reworkable (Chips Fail)**
- **Allow Lateral Shear (chips get hot before the rest of the system)**
- **Long-Term Reliability and Consistency from Chip to Chip**

Opportunities :

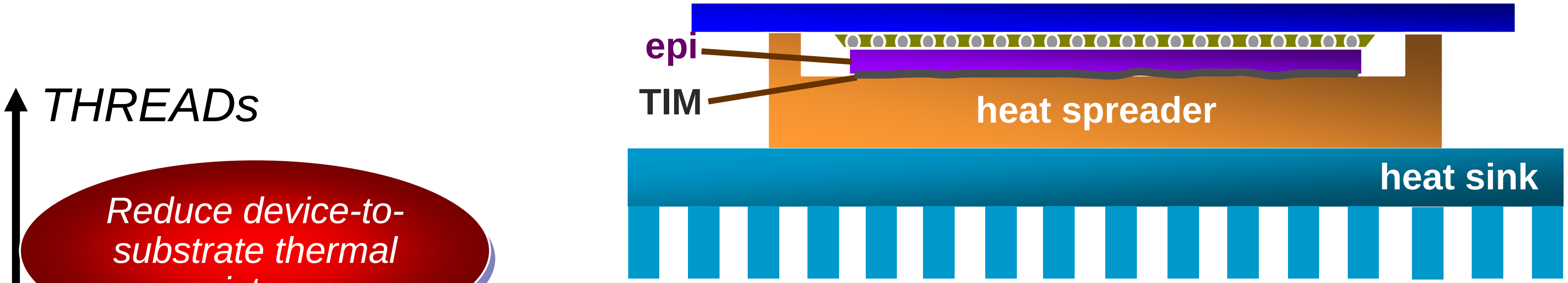
- ***Nanotube/Nanowire materials may be able to meet this challenge***
- ***Preliminary work in NSF, ONR, DARPA (MARCO), etc is promising***

Program Kickoff 4/09.

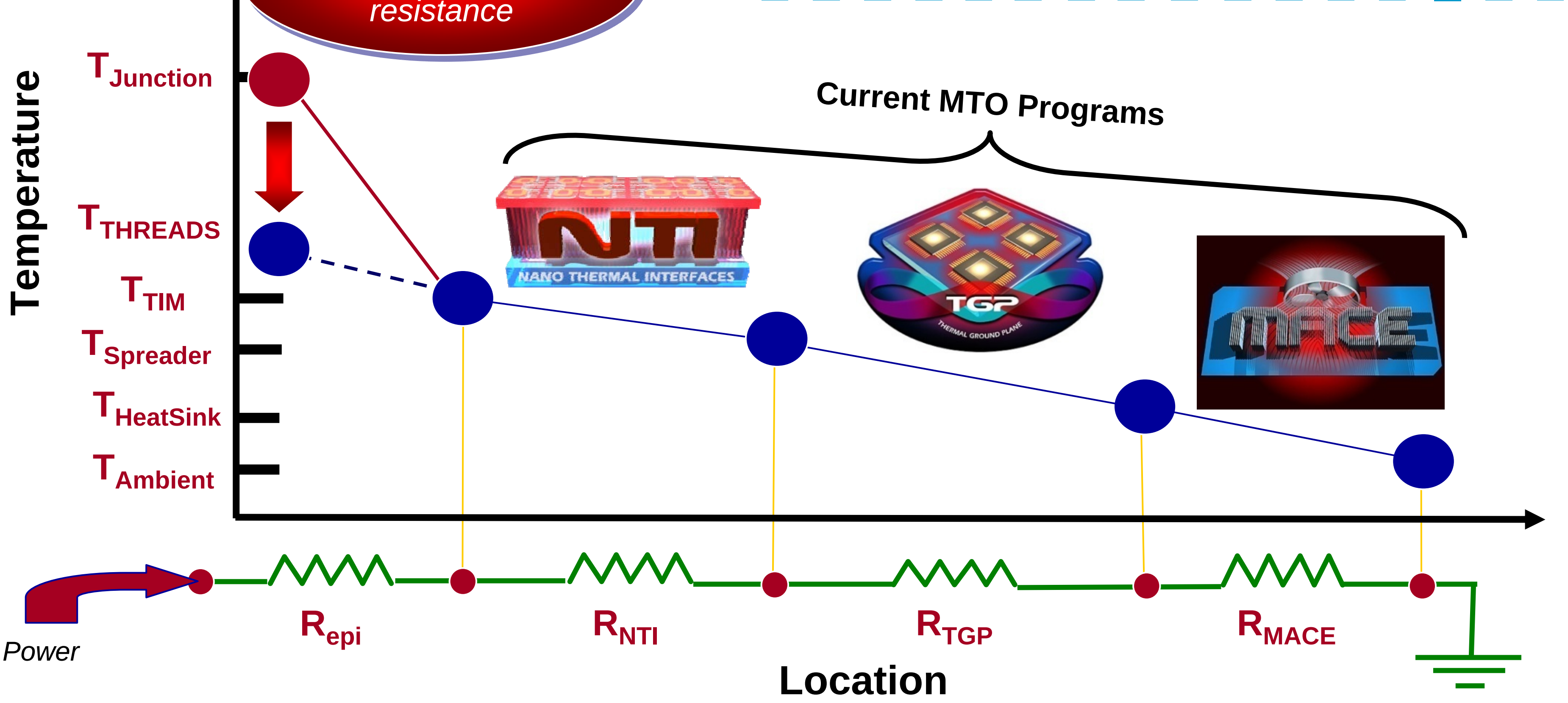
Thermal Management Portfolio



Technologies for Heat Removal from Electronics at the Device Scale (THREADS)



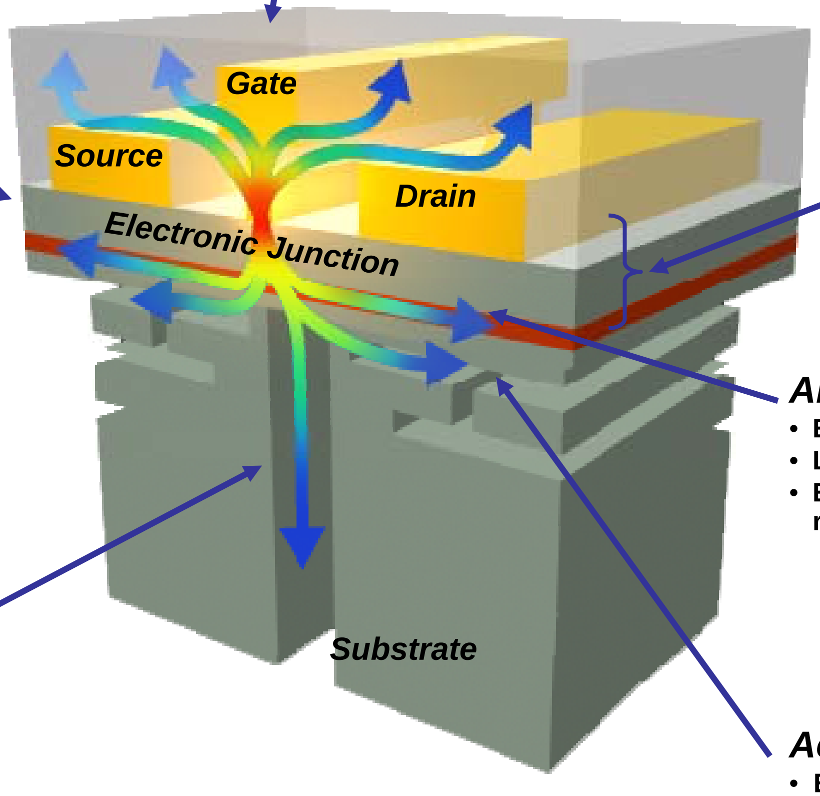
Reduce device-to-substrate thermal resistance



Technologies for Heat Removal from Electronics at the Device Scale (THREADS)

High Thermal Conductivity Over-layer for Heat Removal from Topside of Devices

- High thermal conductivity in deposited material
- Conformal coverage with no gaps



~ 1µm thickness

High Thermal Conductivity Substrates

- Integrate lattice-mismatched heat spreaders
- Eliminate thermal interface resistance
- Match coefficient of thermal expansion of electronic material

Embedded Thermal Vias

- Micro-machined vias within ~1 micron of junction
- High thermal conductivity conformal fill materials
- Low coupling resistance for junction-to-thermal via, thermal via-to-heat sink

Anisotropic Heat Transport

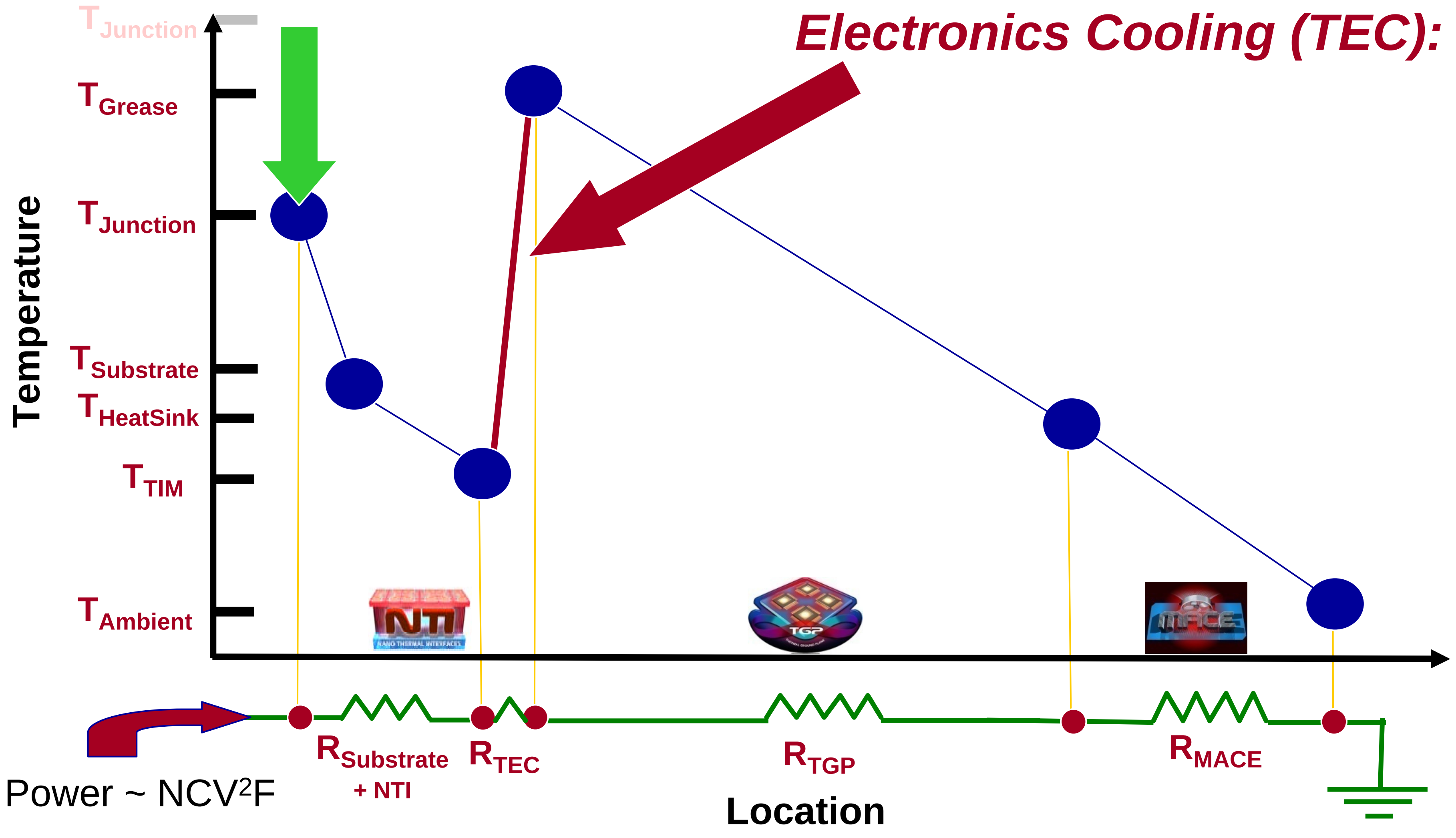
- Efficient nanoscale phonon channel
- Long LO phonon lifetime (3ps)
- Extremely low electrical contact resistance

Active Liquid Cooling

- Eliminate impact on device electrical properties due to time varying dielectric constant of liquid

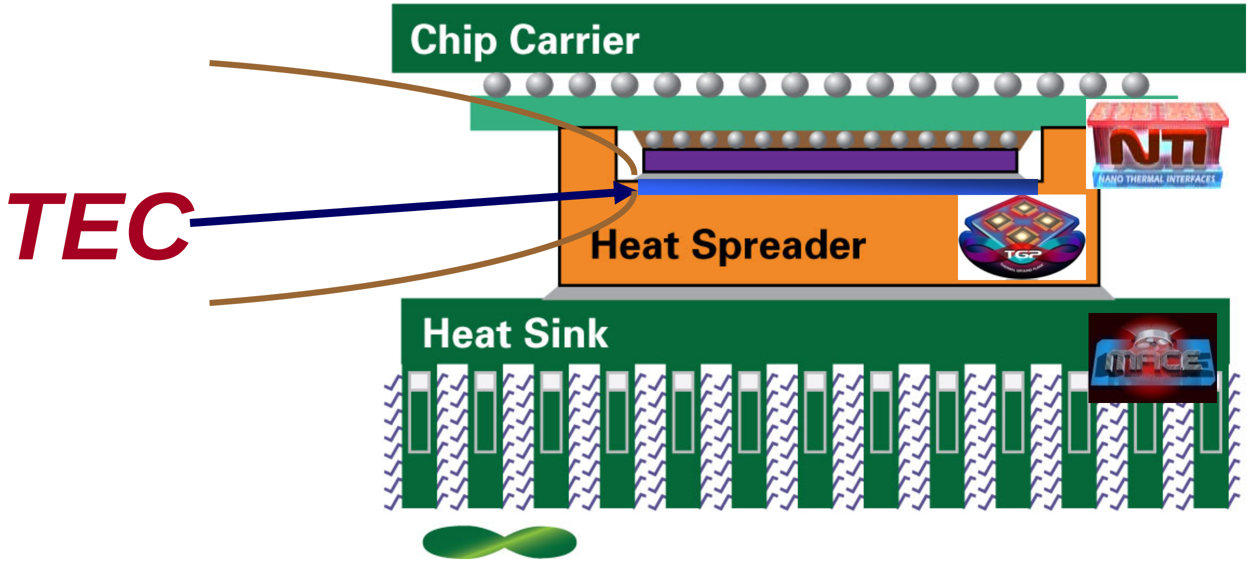
Thermoelectrics for Electronics Cooling (TEC)

Thermoelectrics for Electronics Cooling (TEC):



Thermoelectrics for Electronics Cooling (TEC)

TEC Vision : **Enable greater power utilization margins in electronic materials while also increasing device reliability. Integrate TEC design with NTI, TGP, and MACE.**



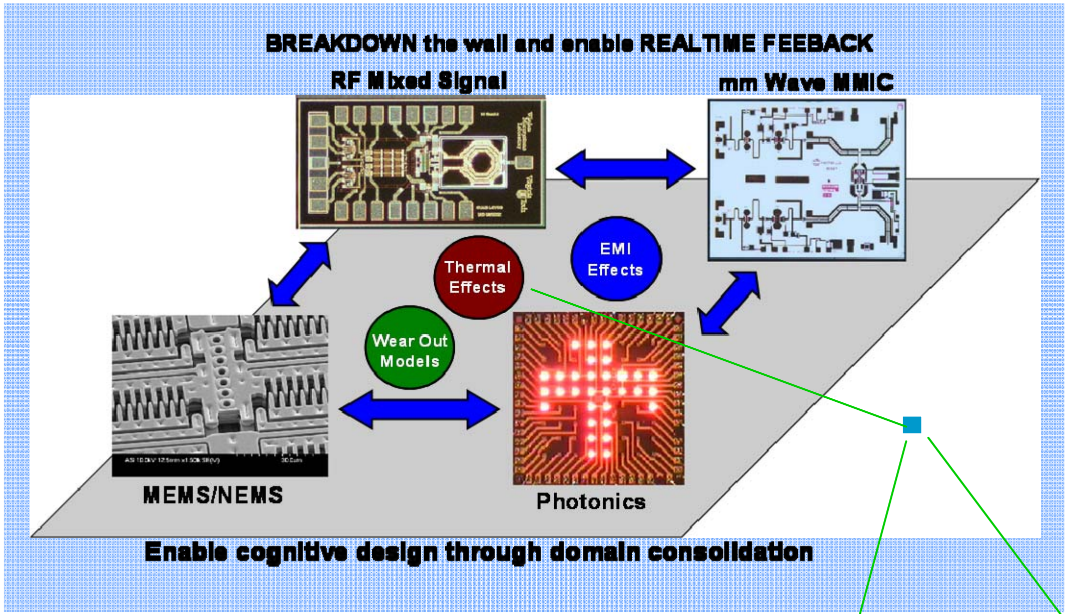
TEC Goals:

- **Build complete modules with all interfaces that demonstrate TEC benefits**
- **Reduce delta T of junction temperature for electronic devices**
- **Further increase electronic device power**
- **Increase device reliability**
- **Incorporate system with NTI, TGP, MACE designs for optimal thermal management system**

METACAD and DANTE Visions

- **METACAD – Cognitive Design Support for Complex Systems**
- **DANTE – Integrated Thermal + Electrical IC Design Support**

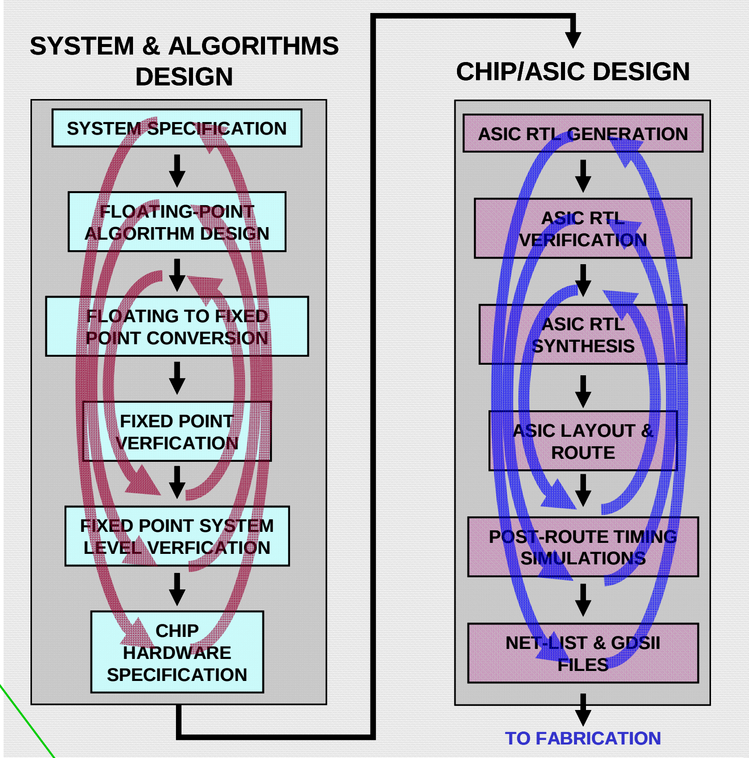
METACAD



Key Technologies

- NeoCAD/PAC/3DIC & Beyond
- Human/Machine Interaction Algorithms (Cognition)
- Models: Architecture, & Physical (Electrical, Thermal, Mechanical)

DANTE



SYSTEM & ALGORITHMS DESIGN

- SYSTEM SPECIFICATION
- FLOATING-POINT ALGORITHM DESIGN
- FLOATING TO FIXED POINT CONVERSION
- FIXED POINT VERFICATION
- FIXED POINT SYSTEM LEVEL VERFICATION
- CHIP HARDWARE SPECIFICATION

CHIP/ASIC DESIGN

- ASIC RTL GENERATION
- ASIC RTL VERIFICATION
- ASIC RTL SYNTHESIS
- ASIC LAYOUT & ROUTE
- POST-ROUTE TIMING SIMULATIONS
- NET-LIST & GDSII FILES

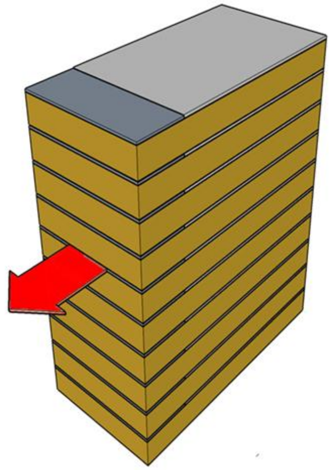
TO FABRICATION

Key Technologies

-Models: Architecture & Thermal

-Multi-Physics Interactions included

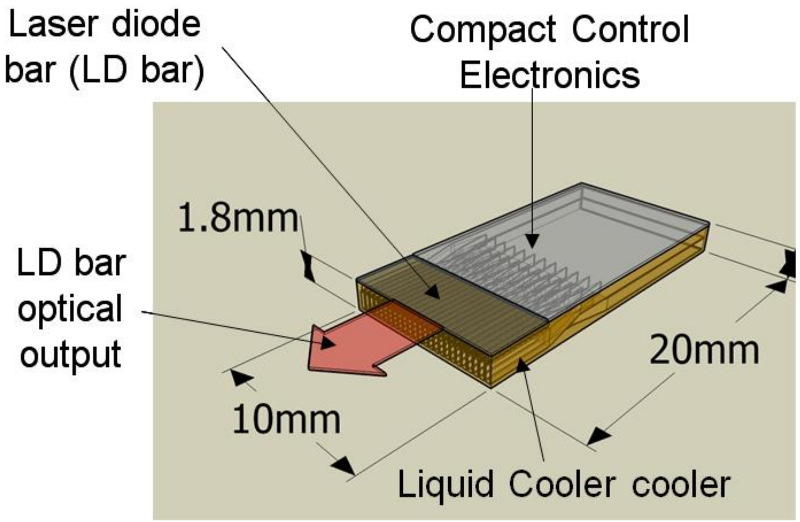
Direct Cooling of High Flux Laser Diode Elements



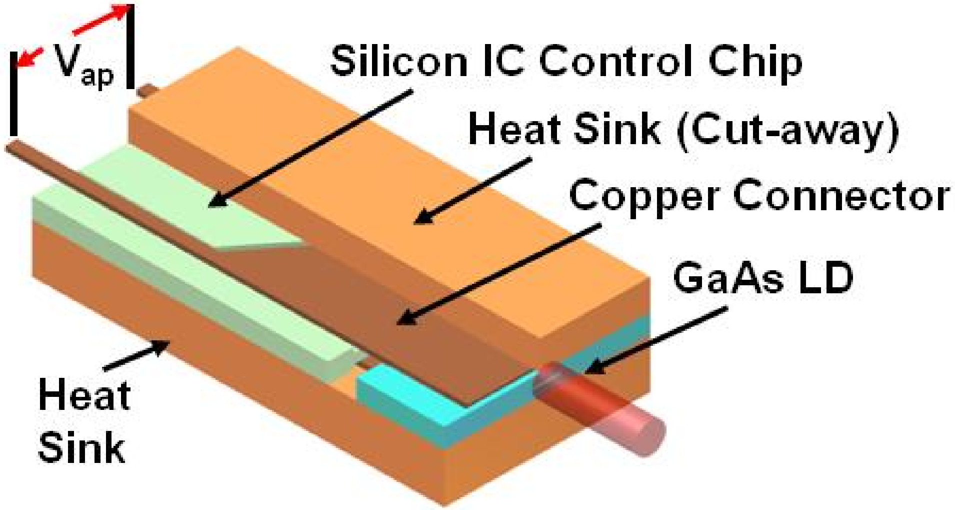
LDA Stack

Advantages include:

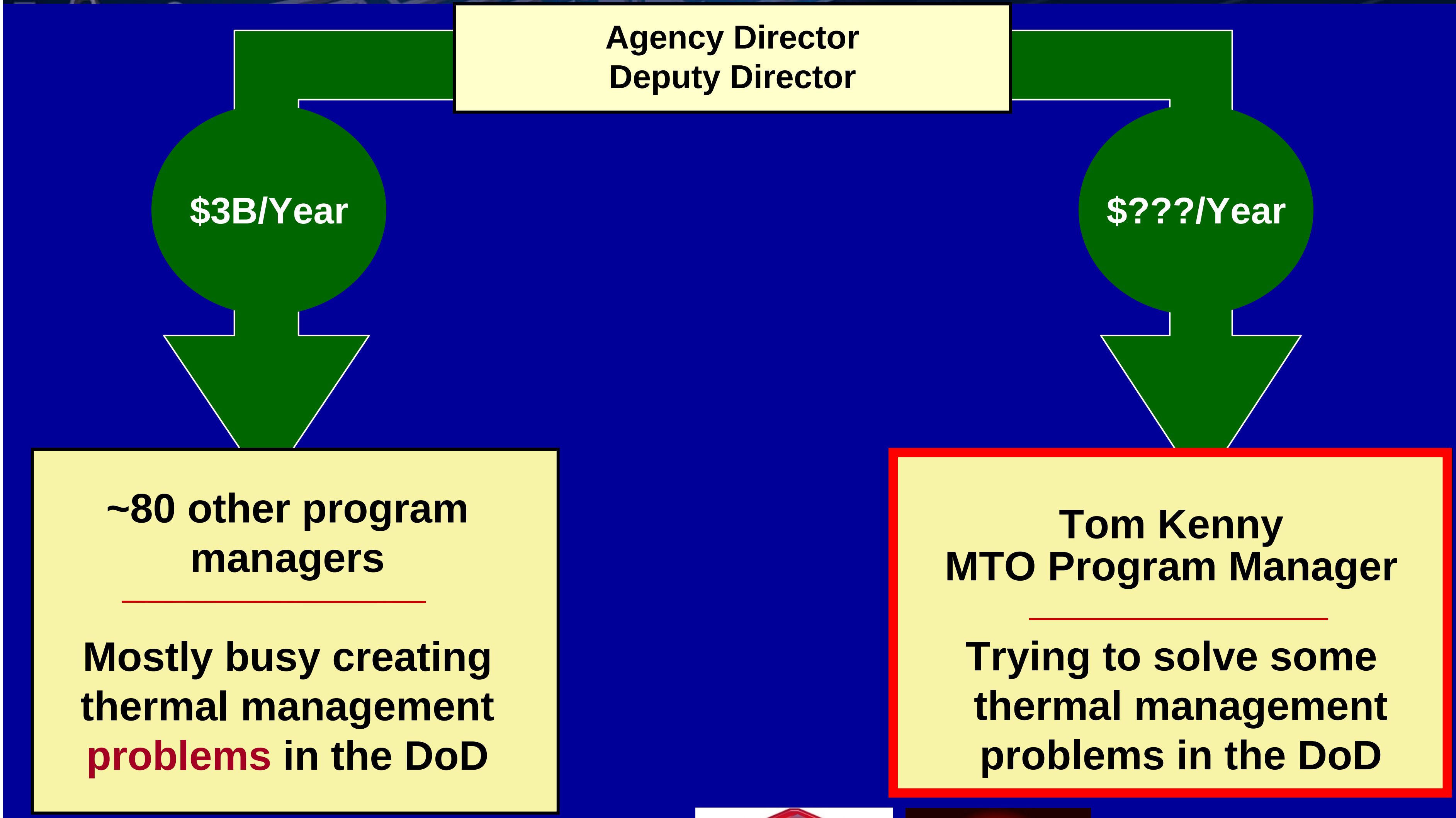
- **Laser diode protection at the single emitter level**
  - Intelligent protection is easier on a single emitter level
  - Enable control of current to each LD
  - Path to phased array LDAs and 3-4X higher power on target
- **35K lower facet temperature resulting in 10X longer life or**
- **5X improvement in performance resulting in ~1,000 Watts/cm-bar**



Single bar on 1.8 mm thick cooler



DARPA Organization



Agency Director
Deputy Director

$3B/Year

$???/Year

~80 other program managers

Mostly busy creating thermal management problems in the DoD

Tom Kenny
MTO Program Manager

Trying to solve some thermal management problems in the DoD

TGP
THERMAL GROUND PLANE

MACE

NTI
NANO THERMAL INTERFACES

???


MICROSYSTEMS TECHNOLOGY OFFICE
MTO
DARPA
SYMPOSIUM
BUILDING THE FUTURE
FROM THE INSIDE OUT