



Rump Session: Advanced Silicon Technology Foundry Access Options for DoD Research

Prof. Ken Shepard

Columbia University

The views and opinions presented by the invited speakers are their own
and should not be interpreted as representing the official views of DARPA or DoD

Approved For Public Release, Distribution Unlimited

Report Documentation Page				Form Approved OMB No. 0704-0188	
Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.					
1. REPORT DATE MAR 2009		2. REPORT TYPE		3. DATES COVERED 00-00-2009 to 00-00-2009	
4. TITLE AND SUBTITLE Daunting challenge of fab access for U. S. universities				5a. CONTRACT NUMBER	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S)				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Columbia University in the City of New York, Department of Electrical Engineering, 2960 Broadway, New York, NY, 10027-6902				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)				10. SPONSOR/MONITOR'S ACRONYM(S)	
				11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited					
13. SUPPLEMENTARY NOTES MTO (DARPA Microsystems Technology Office) Symposium, 2009, Mar 2-5, San Jose, CA. U.S. Government or Federal Rights License					
14. ABSTRACT					
15. SUBJECT TERMS					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT Same as Report (SAR)	18. NUMBER OF PAGES 8	19a. NAME OF RESPONSIBLE PERSON
a. REPORT unclassified	b. ABSTRACT unclassified	c. THIS PAGE unclassified			

A red-tinted, high-contrast image of a microchip circuit board, showing various components and traces. The text is overlaid on this image.

Daunting challenge of fab access for U. S. universities

Ken Shepard
Department of Electrical Engineering
Columbia University



Approved For Public Release, Distribution Unlimited

Requirements

- **U. S. universities must have access to semiconductor processing technologies to validate designs and innovate**
- **General needs require access to:**
 - General CMOS technology nodes
 - Bleeding edge technology to explore latest issues: variability, highest frequency performance
 - More general CMOS node to explore mixed technologies and alternate applications
 - Specialized needs to SiGe, MEMS
- **In some cases, in which large systems are explored, large silicon areas are required**

Fabrication alternatives for U. S. universities

5 mm x 5 mm 0.13 μ m CMOS

- **MOSIS**

- \$72,500 for university pricing (TSMC)

- **Europractice**

- 27,400 Euros (\$34,689) (UMC)

- **TAPO with 1/3 pricing (on DoD funded programs only)**

- \$43,000 (IBM)

- **CMP**

- 33,250 Euros (\$42,106) (STM)

MOSIS has a 5 mm x 5 mm minimum. Both CMP and Europractice allow smaller dice to be fabricated with almost linear cost scaling.

Fabrication alternatives for U. S. universities

12 mm² 65-nm CMOS

- **MOSIS**

- \$99,000 (IBM)

- **Europpractice**

- Not available.

- **TAPO with 1/3 pricing (on DoD funded programs only)**

- ~ \$60,000 (IBM)

- **CMP**

- 93,000 Euros (\$117,900) (STM)

MOSIS has a 12 mm² minimum. CMP allows smaller dice to be fabricated with almost linear cost scaling.

Other programs

- **SRC offers a match for MOSIS fabricated runs but this is capped at \$24K. Must be an SRC GRC-funded project. Very limited funds. Also, revised minimums and pricing (for SRC projects only)**
 - IBM 130nm (8RF-DM) (min) 4 sq mm \$10K
 - Europractice: \$3790 (but only a 2.3 mm² block); CMP: \$11,557
 - IBM 90nm (9SF, 9RF/LP) (min) 4 sq mm \$25K
 - Europractice: \$9160 (but only a 3.5 mm² block); CMP: \$25,327
 - IBM 65nm (10SF, 10LP) (min) 4 sq mm \$48K
 - Europractice: Not available; CMP: \$48,127
- **Both UMC and TSMC offer free shuttle runs to U. S. universities on a limited basis.**
 - Complex relationship with the foundries with sticky IP arrangements and lots of trips to Taiwan.
- **Some U. S. faculty with ties to China are getting free fab through SMIC (Shanghai), which offers technologies down to 65-nm CMOS**



OFFICE OF THE
COMPTROLLER
IN THE CITY OF NEW YORK

Approved For Public Release, Distribution Unlimited

International competitive landscape

- Taiwanese universities have almost “all you can eat” access to TSMC and UMC foundry.
- Chinese universities have a similar relationship with SMIC, many involved with large government “competitiveness” projects – “replacement” for Intel microprocessor
- European Union subsidizes Europractice, but until recently, U. S. has had almost the same access as Europeans (this may change).

Opportunities...

- TAPO program is fully funded for U. S. universities participating in DoD-funded (or DARPA-funded) research on a vetted basis.
- Are there opportunities to leverage the Albany Nanotech facility? NYS has already invested billions in this enterprise.
- Bottom line: There needs to be a solution here that is on a par with our Asian competitors.