

---

RELIABLE  
COMPUTER  
ARCHITECTURES

MURI Review  
June 8, 2002

---

Bruce Jacob

---

University of  
Maryland

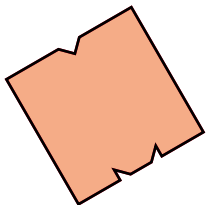
---

# **EFFECTS OF MICROWAVES**

## **Robust Computer Architectures**

**Prof. Bruce Jacob**

**Electrical & Computer Engineering**  
**University of Maryland, College Park**



UNIVERSITY OF MARYLAND

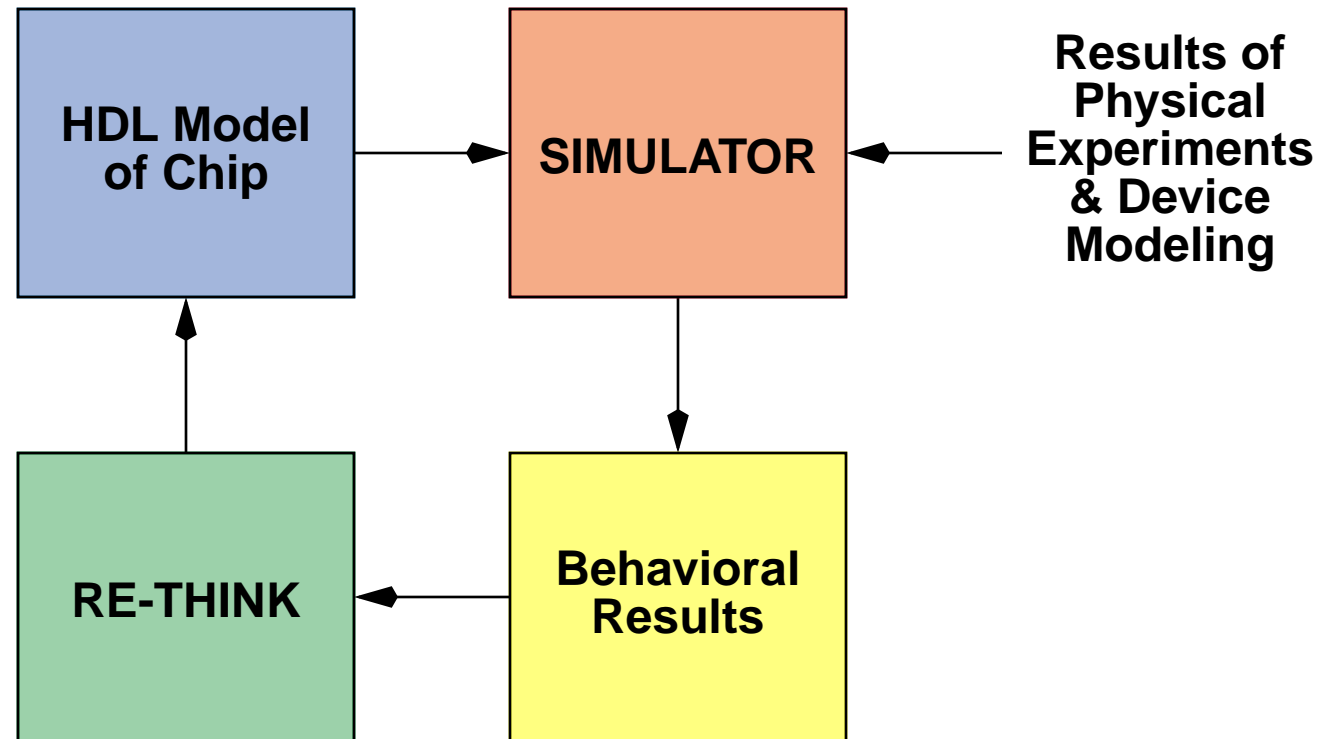
# Report Documentation Page

Form Approved  
OMB No. 0704-0188

Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

1. REPORT DATE <b>JUL 2006</b>		2. REPORT TYPE <b>N/A</b>		3. DATES COVERED <b>-</b>	
4. TITLE AND SUBTITLE <b>EFFECTS OF MICROWAVES Robust Computer Architectures</b>				5a. CONTRACT NUMBER	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S)				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) <b>Electrical &amp; Computer Engineering University of Maryland, College Park</b>				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)				10. SPONSOR/MONITOR'S ACRONYM(S)	
				11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT <b>Approved for public release, distribution unlimited</b>					
13. SUPPLEMENTARY NOTES <b>The original document contains color images.</b>					
14. ABSTRACT					
15. SUBJECT TERMS					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT <b>unclassified</b>	b. ABSTRACT <b>unclassified</b>	c. THIS PAGE <b>unclassified</b>			

# System Modeling



***WHEN systems fail, HOW do they fail?***

**We use this information  
to develop & test reliable architectures**

# Tasks (Talk Outline)

## ACCOMPLISHED

- Verilog models of two bootable microprocessors (simple/advanced)
- Initial work on robust architectures (reliability studies, draft floorplan)

## IN PROGRESS

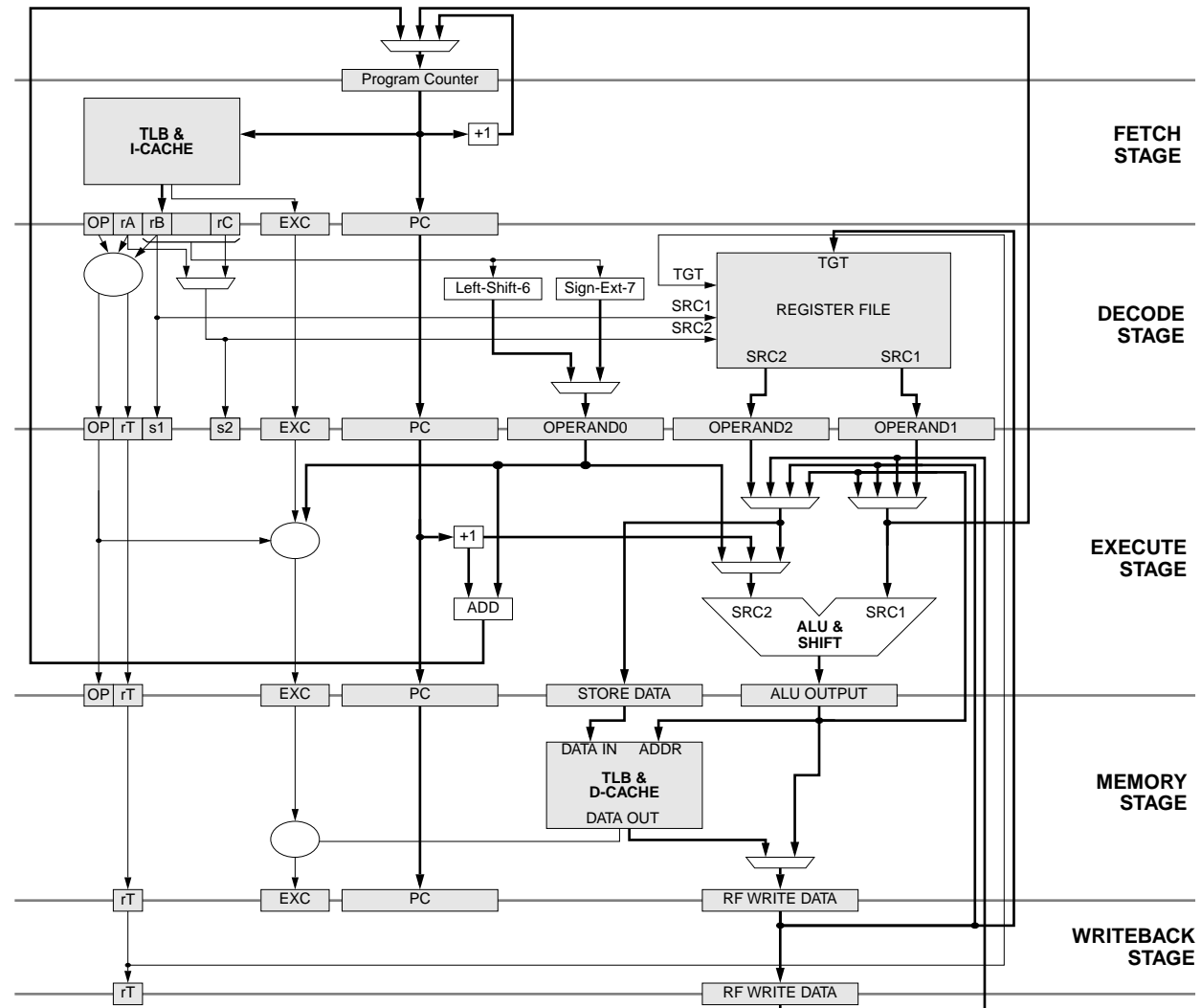
- Verilog model of microprocessor with hardware checkpoint/repair

## FUTURE WORK

- Fabricate and test physical designs
- Enhanced Verilog and SPICE software

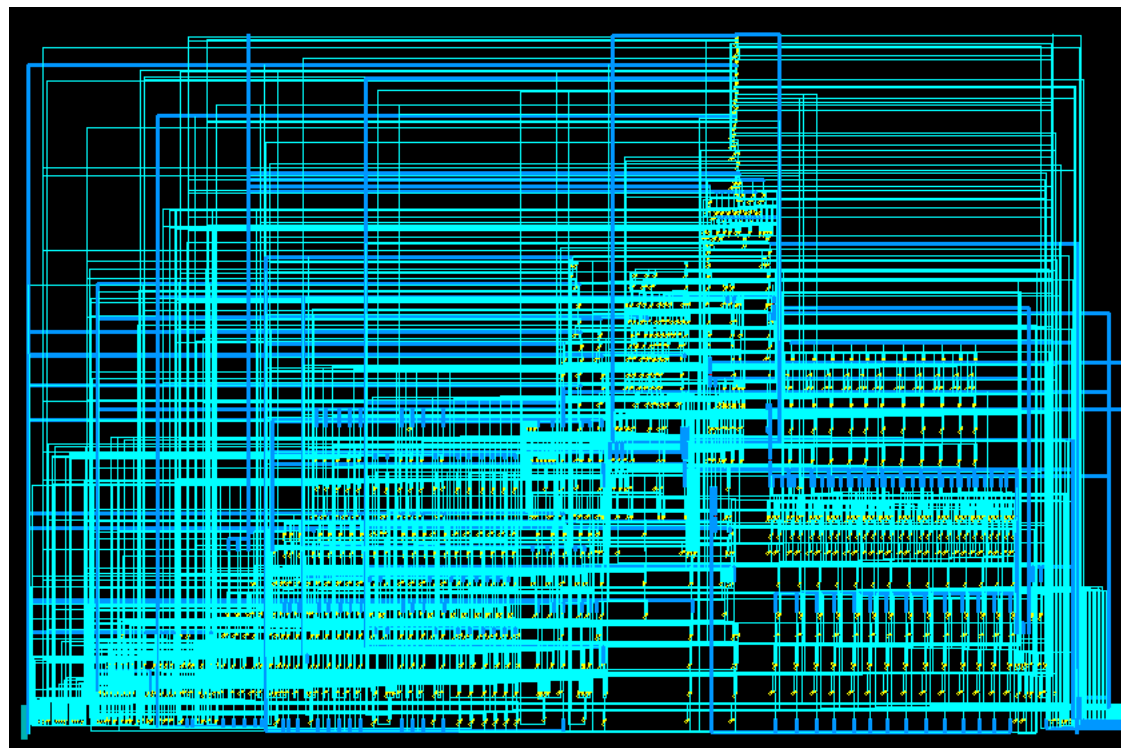
# Processor Model: simple

## Single-Issue, In-Order, Five-Stage Pipeline



# Processor Model: simple

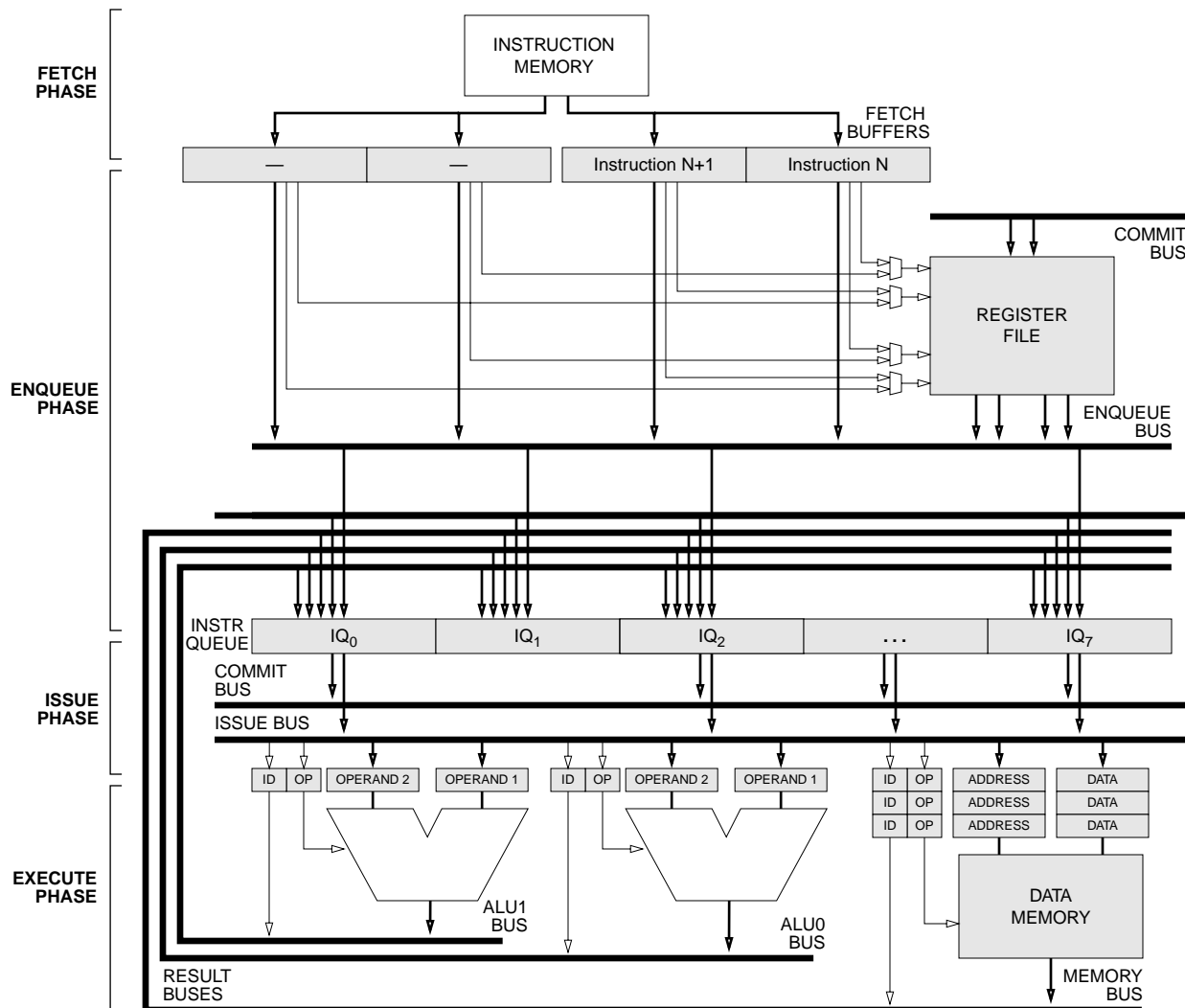
## Single-Issue, In-Order, Five-Stage Pipeline



**16-bit processor core**  
**Handles interrupts precisely**

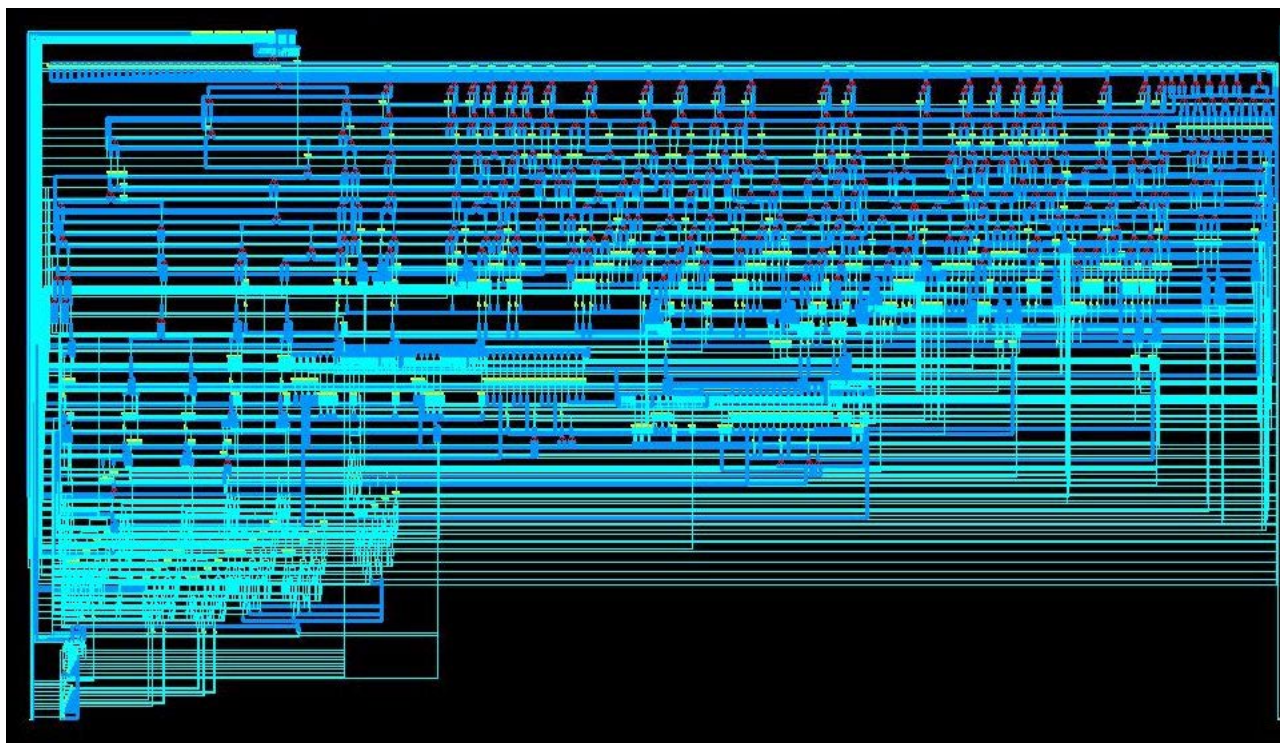
# Processor Model: advanced

## High-Performance Out-of-Order Core



# Processor Model: advanced

## PowerPC ISA with AltiVec SIMD Unit

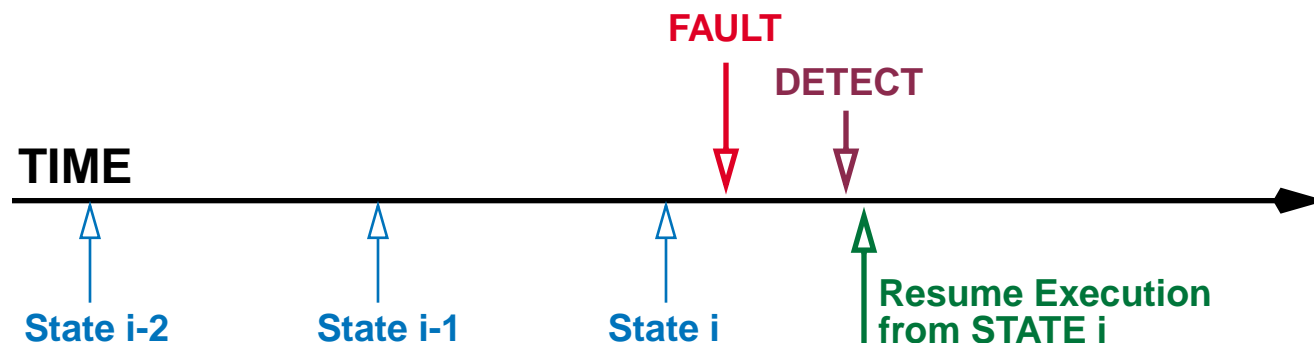


**Design & layout of core in progress  
(AltiVec multiplier above)**

# Robust Architectures

## INITIAL STUDY: Assume the Worst Case

### Checkpoint/Repair ...



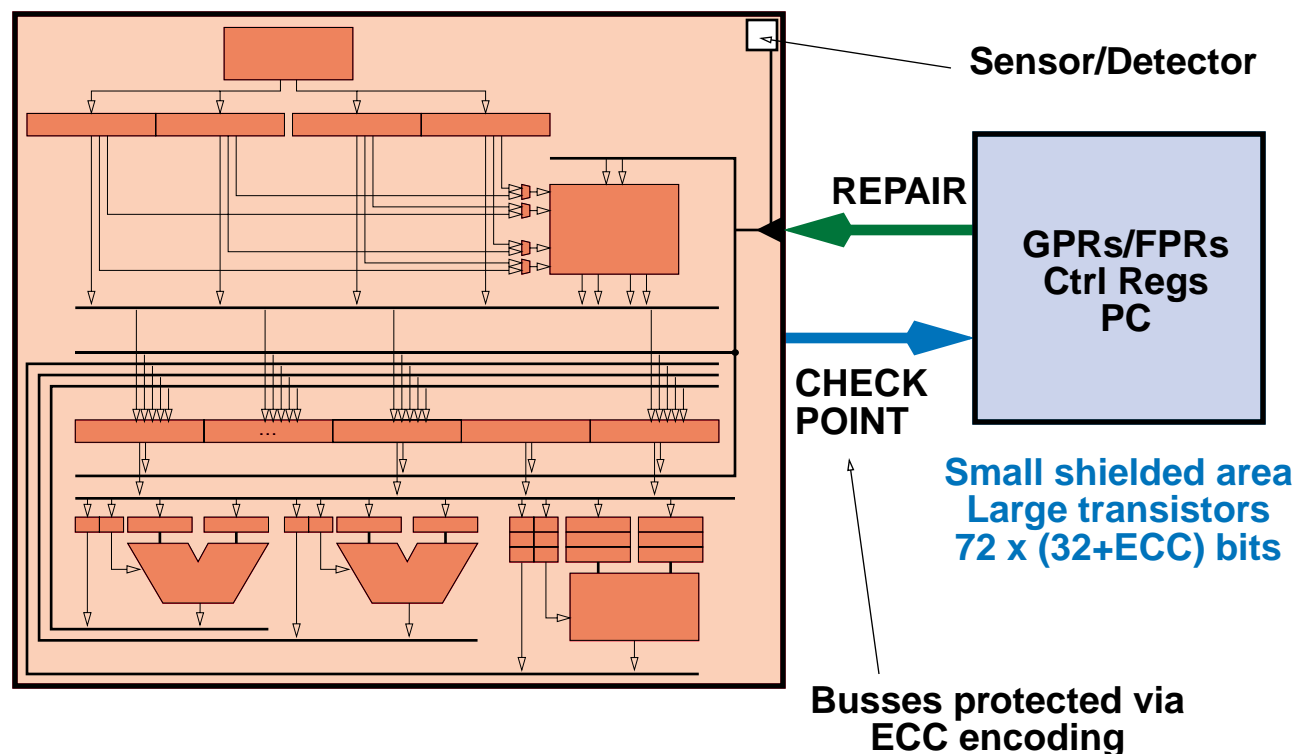
### CHECKPOINT:

Periodically save **KNOWN-GOOD STATE**

In case of **FAULT**, **REPAIR** to last saved state

# Robust Architectures

## INITIAL STUDY: Assume the Worst Case

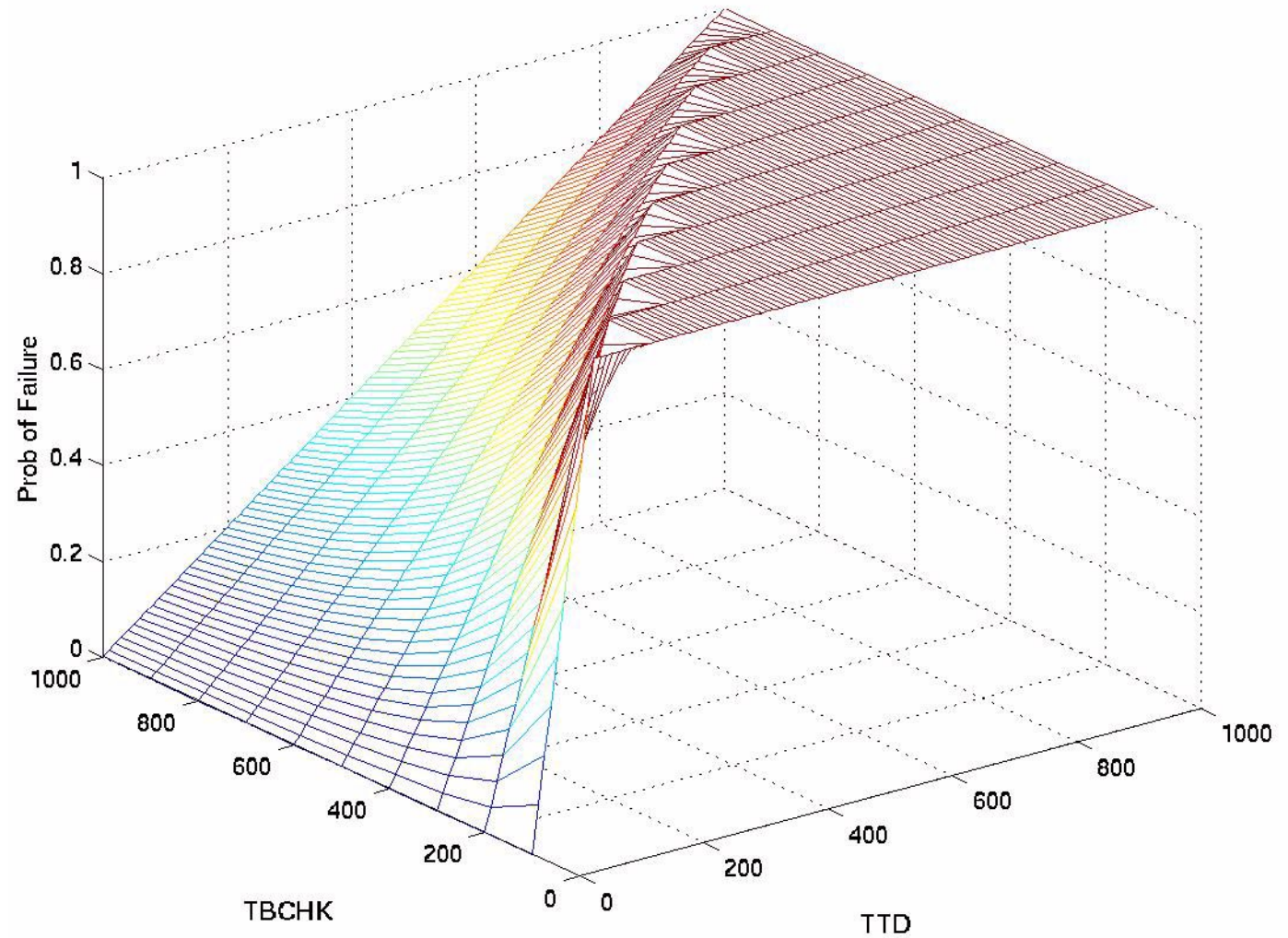


Implementation can be single- or multi-chip

# Robust Architectures

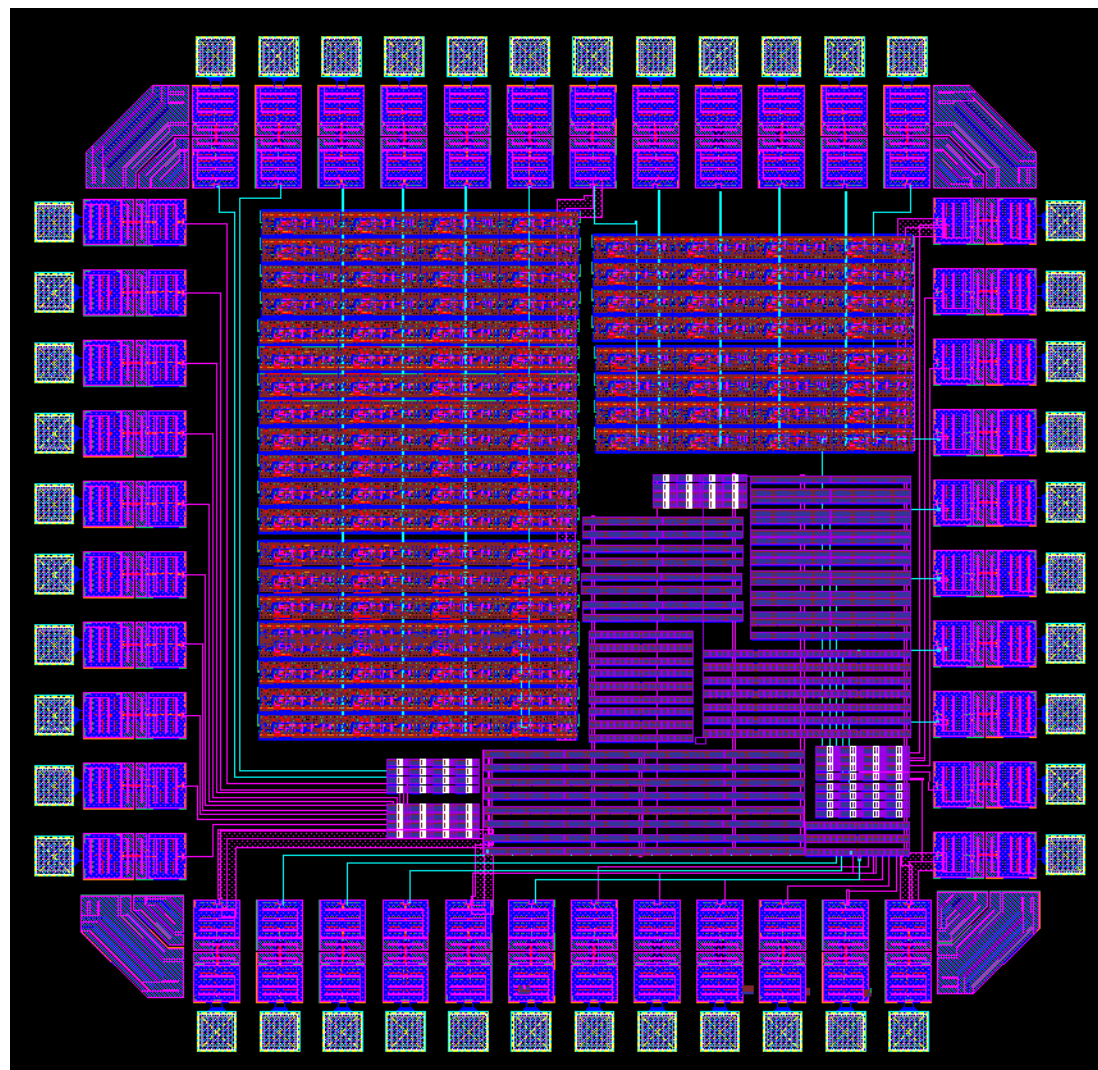


# Robust Architectures



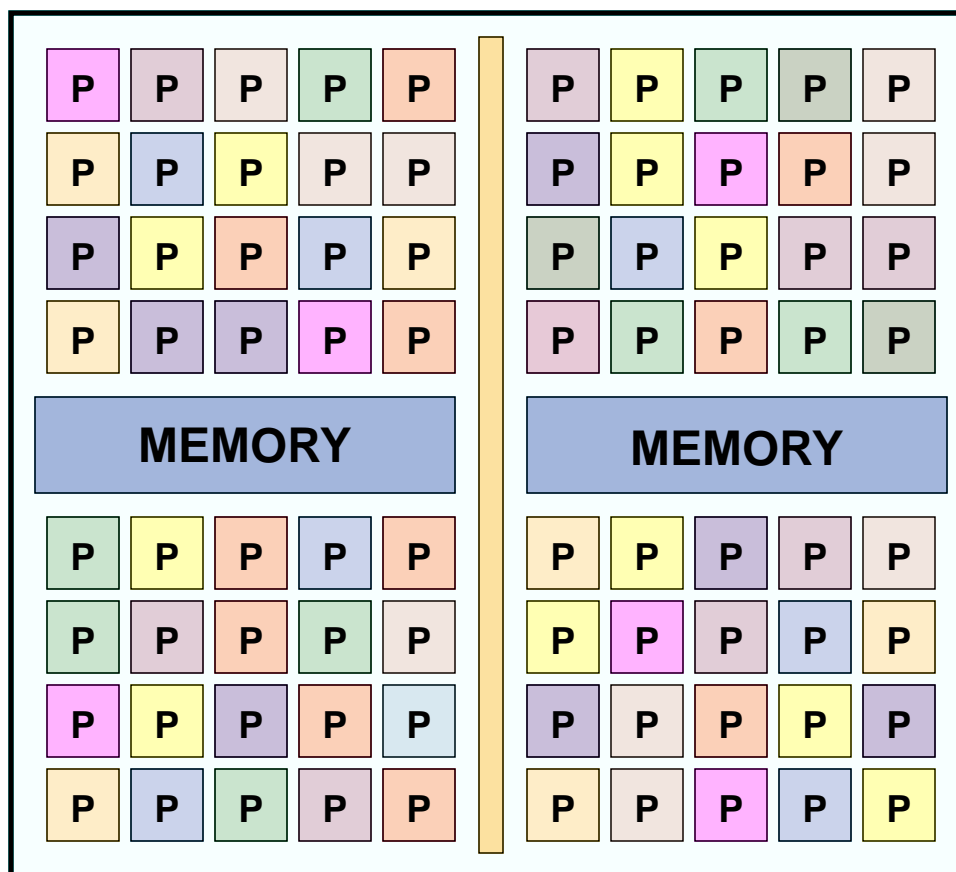
# Robust Architectures

## Initial Floorplan (simple CPU + safestore)



# Globally Asynchronous

**ASSUMPTION: Clock Net is Weak Point**



**Processing elements generate local clocks  
Synchronize at inter-node communication**

# Future Work

## Synthesize, Fabricate, Test Canonical Forms

- **Clock trees**
- **Busses (w/ and w/o ECC)**
- **Memories (w/ and w/o ECC)**
- **Arithmetic/Logic Units**

**Incorporate Drift-Diffusion into CAD tools  
(more accurate SPICE/Verilog modeling)**

# Participants

Profs. **Bruce Jacob & Neil Goldsman, UMCP**

A host of grad students:

- Azadeh Davoodi, Cagdas Dirik,  
Amol Gole, Samuel Rodriguez,  
Ohm Tuaycharoen (**Architecture**)
- Akin Akturk, Zeynep Dilli,  
Tejas Chitnis (**Microelectronics**)

