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(CR&D)**

**Task Order 0036: Physical and Chemical Processes of Operating
Electronic Devices**

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Universal Technology Corporation

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Final Report

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14. ABSTRACT This research in support of the Air Force Research Laboratory, Materials and Manufacturing Directorate was conducted at Wright-Patterson AFB, Ohio from 12 July 2005 through 25 August 2006. Models were developed to validate physical and chemical processes that occur during the operation of wide bandgap electronic devices. Efforts have focused on AlGaIn/GaN HEMT devices, and on aspects of the problem which impact device reliability estimates, such as internal temperature profiles, charge trapping, and electric fields. The bulk of the effort has relied on utilizing commercial electro-thermal and thermal finite element simulators, and details of the practical use of two of these simulators is discussed.						
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Part I: Introduction and scope of report.

This task was started to develop models of processes that occur in wide-bandgap semiconductor devices during operation, with the goal to influence predictions of lifetime and reliability of devices in realistic operating conditions and so accelerate the insertion of new electronic devices. Work has focused on AlGaN/GaN HEMT devices specifically, as these devices represent a large market and are being rushed to commercialization without full knowledge of failure mechanisms or assured long term reliability. These HEMTs are promising for very high power DC and high frequency devices (radar and long range communication).

The task had started with an extensive literature search to determine the extent of existing AlGaN/GaN HEMT modeling and experimental progress, as detailed in Appendix A. Device modeling was done in the finite element simulator DESSIS, as discussed in part II. The initial aim was to fit experimental data for device operation using material parameters from in house measurements and the open literature whenever this data exists and by adjustment to fit the experimental data when it does not. This resulted in a basic but working model of DC operation of the AlGaN/GaN HEMT before degradation that has been extended as detailed in part III to accommodate traps, show transients, show the effect of a field plate, and include hot electron effects.

To more accurately model device heating due to the substrate, a 3D thermal model was built in ANSYS. This can be incorporated in the DESSIS code to a first approximation as an effective thermal resistance as discussed in section F of part III, or the simulations can be loosely coupled as discussed in part IV for more accurate results that reveal that device heating is sensitive to bias, and not just the total power dissipated in the device.

Some brief evaluations of micro Raman for in-house AlGaN/GaN devices were conducted as discussed in part VI, observing an expected reduction in the Raman frequency with increasing temperature and an unexpected optical transparency after anneal of one metal ohmic stack. Micro Raman is a very useful high-power device characterization tool, and has been demonstrated by others to be able to measure stress and temperature to $\sim 1 \mu\text{m}$ resolution on AlGaN and GaN, while no signal is expected over continuous metal.

Part II: Device Modeling in DESSIS:

DESSIS (by Integrated Systems Engineering) [1] is a physics-based finite element simulator that has been the workhorse for PACE modeling during this effort. Sentaurus Device (also called Sdevice) will replace DESSIS and is backward compatible, except for at least one known difference in command interpretation, as will be discussed. Briefly, in either program a device is broken up into elements with specified material properties, such as dielectric constant, thermal conductivity, electron/hole mobility as a function of electric field, dopant density, etc. It should be pointed out that DESSIS is not first-principles or atomistic. Material properties are not determined within DESSIS, but must be specified by the user.

Mark Yannuzzi (AFRL/SNDM) supplied an early version of the parameter files for GaN, AlN, and AlGaIn that were used for early simulations discussed here, but the later ones use new parameter files developed as part of this task.

The bulk of the parameters were extracted directly from literature. Some are highly dependent on the device and must be adjusted to the particular wafer/device for best results. Others were instead fitted to literature, either because the exact data needed was not found, or in most cases because DESSIS only allows certain functional forms for parameters and sometimes a different functional form exists in the literature. All sources are given for parameters used within the parameter file when data is extracted from the literature.

In addition to the parameter (.par) files, DESSIS requires a DESSIS command (.cmd) file, and boundary (.bnd) /command files for the device geometry. All of my work uses the MDRAW program for the geometry. Common names are DatexMaterials.par (in DESSIS) or Sdevice.par (in Sentaurus Device) for the main parameter file, and xxx.par for the materials dependent parameter files, where xxx includes the material as identification, dessis_des.cmd for the DESSIS command file, and mdraw_mdr.cmd and mdraw_mdr.bnd for the MDRAW files. The main parameter file always must completely specify all important material parameters either directly or by calling the appropriate parameter file for all regions/materials, or DESSIS will fill in missing information with default parameters, which are not usually realistic.

Complete parameter files for GaN, AlN, and AlGaIn are considered ITAR restricted material and are not supplied with this document. Requests for these files should go through Eric Heller (AFRL/MLPSM), Don Dorsey (AFRL/MLPSM), or Chris Bozada (AFRL/SNDD). Command and boundary files are also sensitive and requests should also go through Eric Heller, Don Dorsey or Chris Bozada.

Figure 1 shows an example top view of simplified device geometry, with physically important regions marked. The DESSIS structure is a 2D cut through the Source-Gate-Drain region as shown in figure 2. Figure 3 shows a “cartoon sketch” of device operation, with the point that the hottest and most electrically stressed region in a conventional device without a field plate is the pinch off region near the edge of the gate, as determined in the literature survey. Because of this, the particular structure shown by Fig. 2 was designed to mimic early in-house devices in particular in the region near the gate. The SiN tapers off because its thermal and electrical effects for the purposes of this simulation were not very important far from the gate, and source and drain metals are represented only by equipotential surfaces. Table I shows a listing of some of the more important and less obvious variables that are found in the parameter and command files

for HEMT device operation that must be set in DESSIS and their effect on device performance.

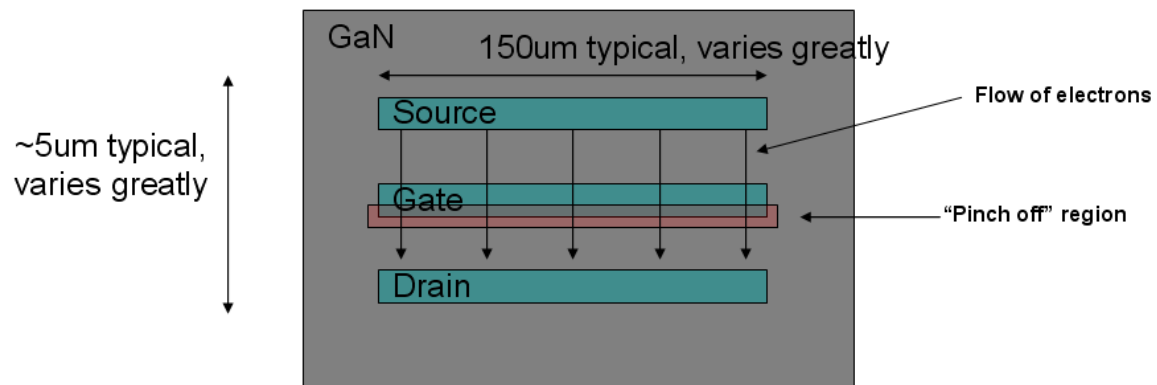


Figure 1: Simplified top view of a device, showing flow of electrons and the pinch off region.

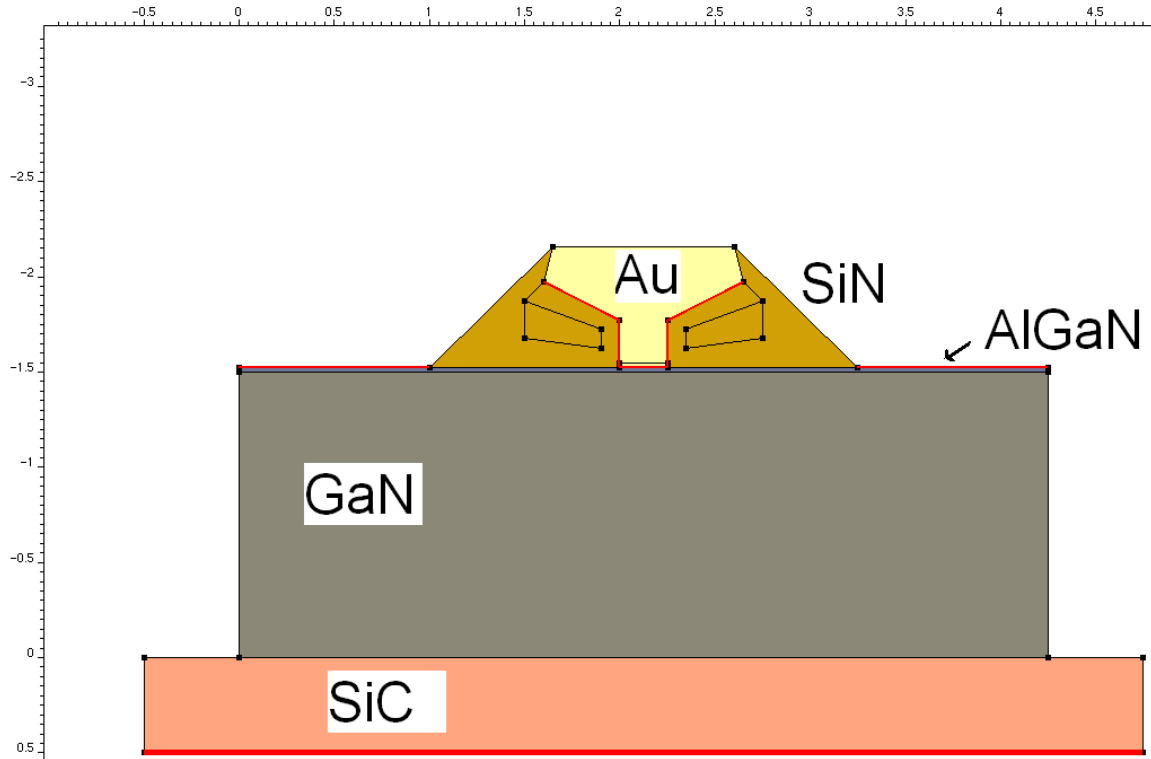


Figure 2: Simplified device geometry as input into the DESSIS software. Red shows electrical/thermal contacts. The AlGaN layer (purple) goes across the entire device, and is thin and hard to resolve in this image. A thin Ni layer is present between the Au and the AlGaN layer.

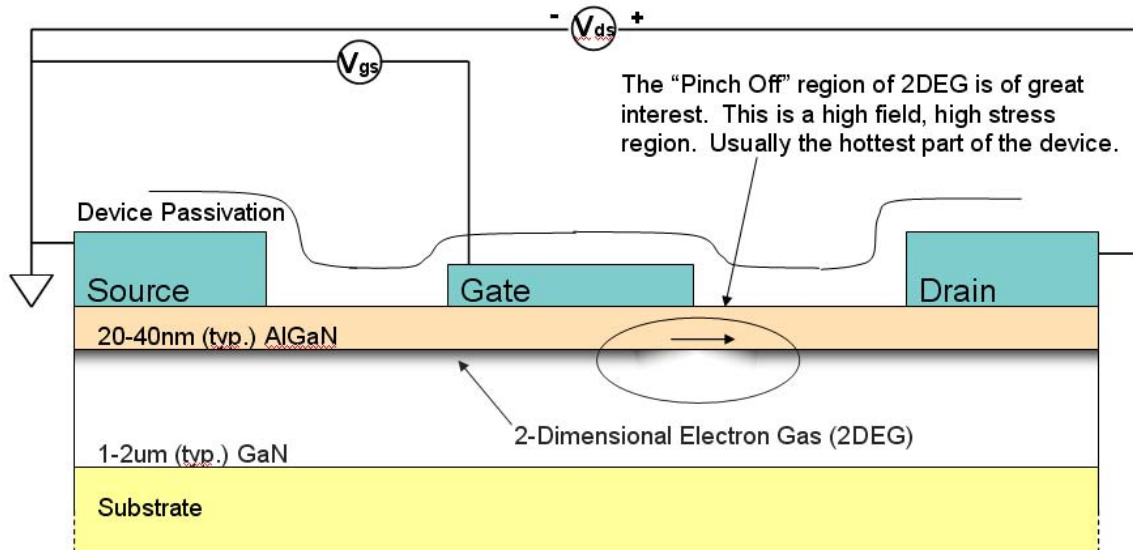


Figure 3: Side view of a cut into the device.

Table I: Major variables in the simulation and the effect on device performance.

Variable	Explanation	Effect on simulations
Command file		
Schottky Barrier Height	Ni/AlGa _N SBH, chosen from measurements in open literature.	Has direct effect on threshold voltage.
Source/Drain resistance	DESSIS allows resistance in Ohm* μm to be given. This can easily be determined from experiment but can vary significantly in practice over a wafer.	Affects low voltage (V_D) on-state resistance, less effect on current after saturation for reasonable resistances.
Thermal resistance of back contact	For most devices, thermal transport in the substrate requires a 3D simulation while the DESSIS license available for AFRL is 2D. To first order, the substrate can be treated as a fixed thermal resistance and calculated, although this breaks down at high power since thermal properties are temperature dependent and vary along the gate width. More rigorous treatment will be discussed and requires coupling a 3D thermal sim to the DESSIS sim.	Causes reduced mobility and less drain current at high power dissipation levels.
Air/AlGa _N or SiN/AlGa _N properties	Interface states at this interface expected to exist, even for passivated devices. Carrier density and device I-V current experimentally known to be affected by presence/absence of SiN, is direct evidence for this.	Depends on interface state properties.
Bulk Ga _N properties	Bulk states known to exist, C and Fe are intentionally put into Ga _N to make to semi-insulating. Without Fe or C, Ga _N typically n-type, attributed to from Si or O.	Can affect threshold voltage for any gate length. Affects sharpness of pinch-off as a function of V_G , especially for small gate length.
Fixed spontaneous and piezoelectric charge at AlGa _N /Ga _N interface (not to be confused with free charge)	Amount to expect is known theoretically for perfect crystalline material, and this value is typically used in the simulation. Charge amount may be reduced by damage.	Any change has a large affect on threshold voltage, and on-state current.

**Table I: Major variables in the simulation and the effect on device performance.
(Cont'd)**

Parameter file		
Dielectric constant	Self explanatory	Data assumed to be well known, variations not explored.
Index of Refraction	Self explanatory	Data assumed to be well known, variations not explored.
Heat capacity	Self explanatory	Data assumed to be well known, variations not explored.
Thermal conductivity	Self explanatory	Known within limits. Lower conductivity causes reduced mobility and less drain current at high power dissipation levels.
Bandgap	Self explanatory	Data assumed to be well known, variations not explored.
Effective Mass	Self explanatory	Data assumed to be well known for electrons, variations not explored.
Quantum Potential Parameters	The density gradient approach is used for 2DEG electron quantization in DESSIS. Schroedinger's equation is more accurate but numerically difficult. This is calibrated to Schroedinger's equation at zero bias voltage applied, to give a carrier density that spatially approximates the correct value. Can be turned on/off as needed.	Affects carrier density in 2DEG, energy level of carriers, position at interface. Will affect threshold voltage and fraction of carriers that see the AlGa _N mobility instead of the Ga _N one.
Energy Relaxation time (for Hydrodynamic simulations)	Exponential decay time constant for hot electron relaxation. Electrons assumed to have a temperature above the lattice temperature due to drift induced by electric fields. Long times increase the electron temperature and the number of hot electrons. Adds to computation time and reduces stability, can be turned on/off.	Complex effects. Must be used with care. Hot electron decay time is in practice a function of electron energy, so more complex than DESSIS assumes.

**Table I: Major variables in the simulation and the effect on device performance.
(Cont'd)**

Low field dependence (mobility)	Mobility when fields, dopants, etc. are not a factor. This is best characterized as the 2DEG mobility, not the bulk mobility. This is the mobility as measured by the Hall effect, as long as scattering by dopants are not a significant factor. Directly affects 2DEG sheet resistance, and can be calibrated this way.	Effects both low voltage (V_D) on-state resistance, and lesser effect on high V_D drain current.
High field dependence (mobility)	Mobility known to drop at high fields, characterized in open literature as a function of field and temperature. At very high fields, carrier velocity saturates.	Causes reduced carrier mobility at any drain voltages over $\sim 1V$.
Doping dependence (mobility)	Mobility known to degrade with dopant concentration. Characterized in open literature. DESSIS allows traps to contribute to degradation, Sdevice does not.	Depends on implementation.

Part III: Findings in DESSIS.

A. Fit to basic HEMT

Figure 4 shows the agreement seen between DESSIS (solid line) and experiment (dots). This is for a model calibrated to in-house data, Eric Heller (AFRL/MLPSM), Don Dorsey (AFRL/MLPSM), or Chris Bozada (AFRL/SNDD) can be reached for details. Of the parameters listed in Table I, all but three were set by values from the open literature, by results from other simulations (substrate thermal resistance), or by fitting to previous simulations. The three set by curve fitting are Source/Drain resistance, low field mobility, and bulk GaN trap density. Source/Drain resistance can vary greatly device to device, low field mobility can vary some as seen in 2DEG sheet resistance measurements, and bulk GaN trap density is not well known. GaN trap density was set throughout the entire GaN material, to represent the traps (C or Fe) introduced to make the material semi-insulating. It is expected that the density of these traps will vary, since in practice an attempt is made during growth to turn off the trap flux before the GaN deposition completes. In practice it is expected that some dopant is incorporated in the top layers of GaN, but less than in the bottom layers.

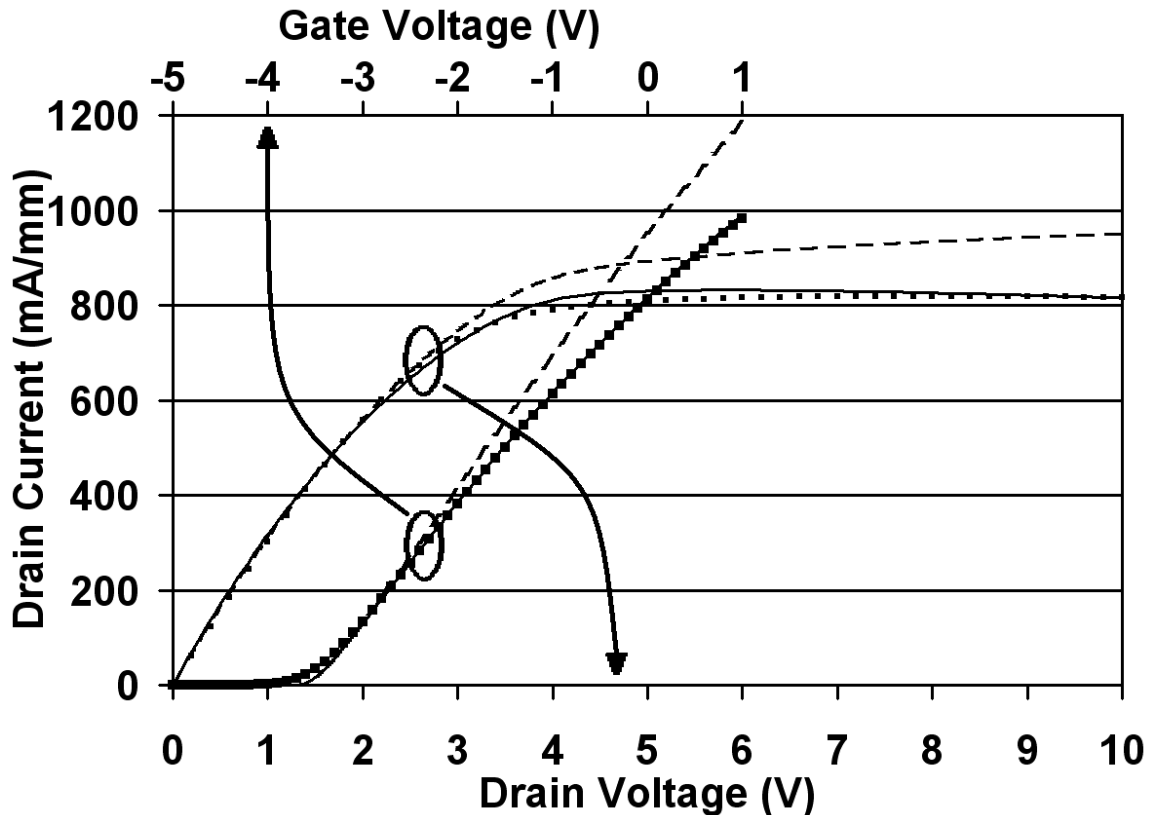


Figure 4: Experimental data (dots) compared with DESSIS output for an isothermal simulation (dotted line) with the device set to 300 K and one including temperature effects (solid line) with the substrate set to 300 K.

B. Effect of traps – position and energy varied.

To gauge the effect of traps, acceptor-like traps were put into DESSIS in the AlGaIn and GaN and the effect as a function of density, location, and the energy of the

trap, and steady-state DC I-V curves run. Band profiles were also run to gauge the impact of traps and assumptions about interface pinning mechanisms.

Traps were found to reduce I_D , especially at the knee, qualitatively in agreement with expectations from the literature [2]. Acceptor-like traps with energy near E_C do not completely fill, but those at mid gap or deeper were seen to fill completely. Because of this, Results for mid-gap traps were nearly identical to results for traps near E_V , as seen in Fig. 5. Trap filling profile is shown in Fig. 6. This may not be the case if traps were placed farther from the 2DEG than they were for this simulation. Also, this simulation was done with the SiN/AlGaIn interface rigidly pinned to $E_F = E_C - 0.9$ eV. This condition has been relaxed for later simulations, and this change will greatly affect the trap filling shown. With this change, it is expected that there will be a difference between trap filling of mid-gap traps and those near E_V .

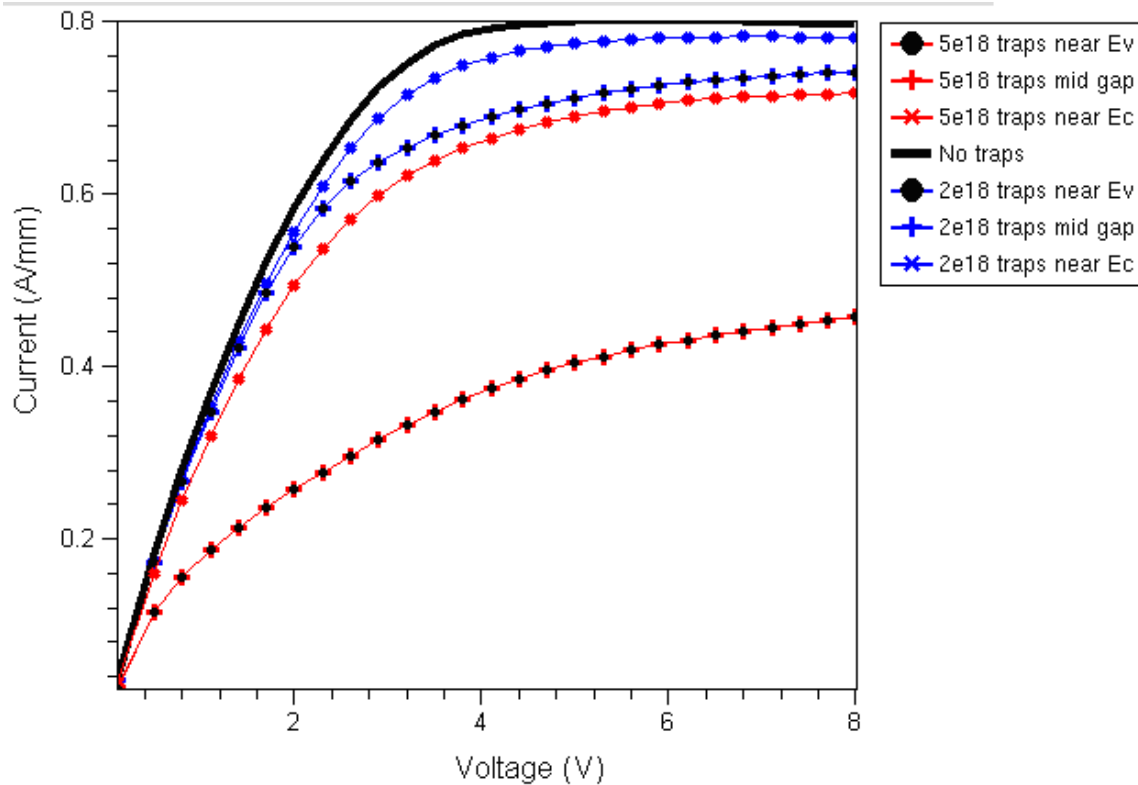


Figure 5: Effect of acceptor-like traps on DC I-V curves: Traps placed in the AlGaIn in the approximate location of the pinch-off region (drain edge of the gate). Density in units of cm^{-3} is varied, as well as the energy depth of the trap.

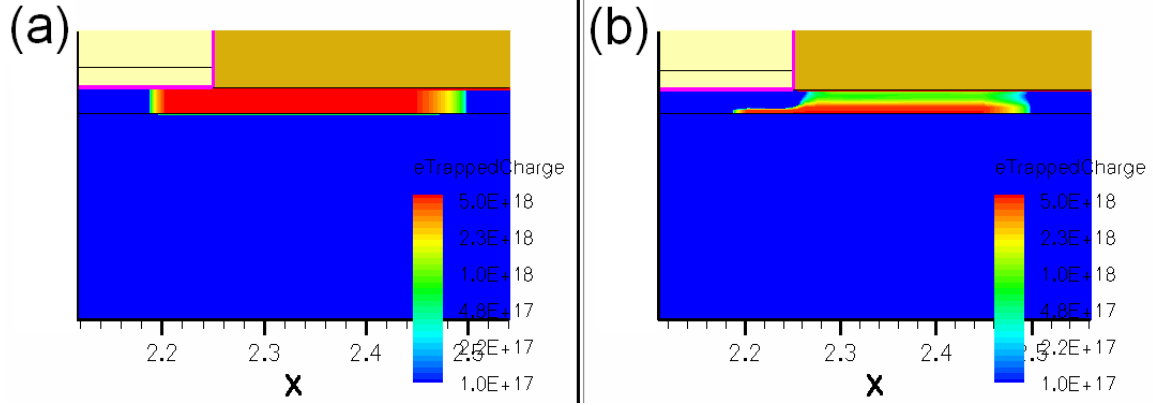


Figure 6: Predicted trap filling for mid gap traps (a) and for traps with energy near E_C (b). Traps were only available to fill in the AlGaIn region shown in red in (a). Yellow is gate metal, brown is SiN, Blue AlGaIn or GaN.

C. Transient current – Device heating.

Transient currents are observed in DC I-V curves when a stepwise change (or pulse) is applied to V_D or V_G ; drain current can in theory either initially overshoot and recover to a steady value or undershoot, with time constants ranging over many orders of magnitude. This effect has been attributed to gate lag, where a region near the gate acquires the gate potential over a characteristic time, delayed trap filling and unfilling, and thermal transients, as the device temperature changes to reflect the new steady state temperature profile expected for the new power dissipation. All of these have been reported in the open literature, more commonly gate lag [3] and trapping [4], than thermal transients [5].

A DESSIS simulation was carried out of the thermal heating transient, with no traps present in the AlGaIn, and a moderate number in the GaN which were very deep and so always expected to be occupied such that they did not contribute significantly to the transient effects. To be sure of this, the simulation was set up so that a self-consistent electro-thermal solution was found at $V_D=8V$ and $V_G=-4V$ where heating is negligible, then the electrical properties (traps states, etc.) were solved at $V_D=8V$ and $V_G=0V$, *without updating the thermal field*, then the thermal field allowed to approach the new steady-state as a function of time. A current transient was seen at nanosecond time scales, due to device heating at the pinch off region and in the sub- μm size region surrounding this region, as shown in the drain current (Fig. 7) and the thermal profile during the transient (Fig. 8). For unknown reasons, DESSIS was not very stable and the simulation could be carried out only to short times. Also, it was found that DESSIS would not run at all for the transient simulation without the Backward Euler option enabled in the math section (see the DESSIS manual, “Transient=BE” command).

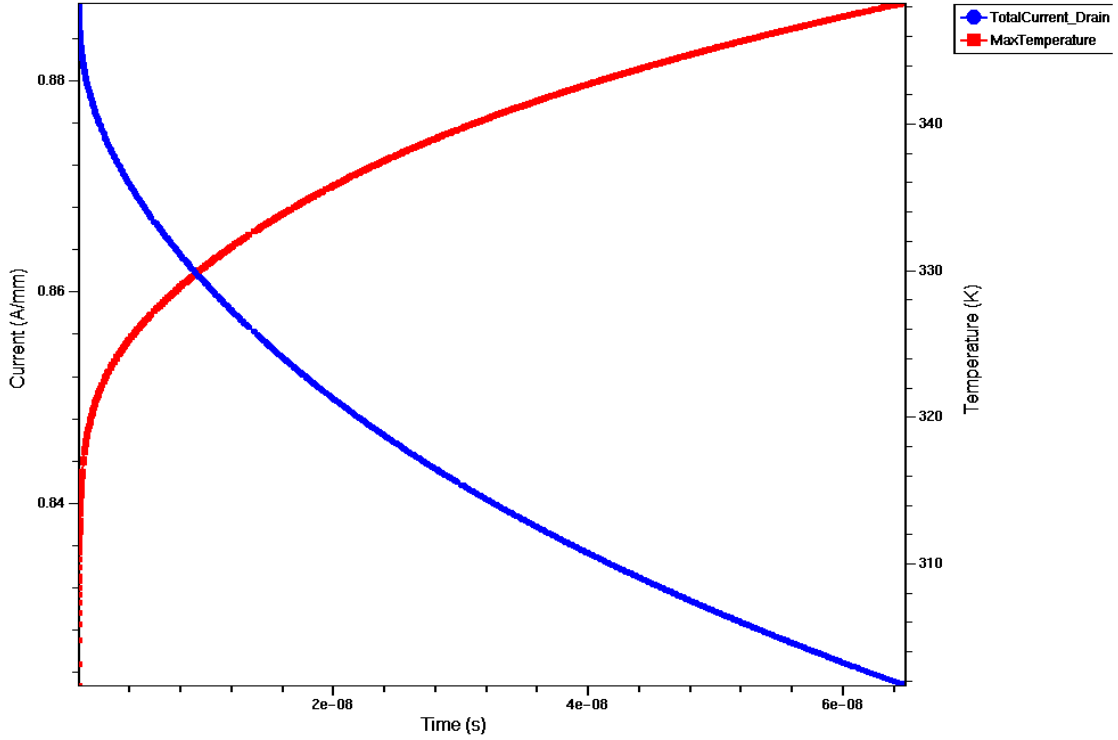


Figure 7: Drain current and temperature predicted as a function of time after device is turned on with $V_D=8V$ and $V_G=0V$ as $t=0$ from an off state with negligible heating at $V_D=8V$ and $V_G=-4V$.

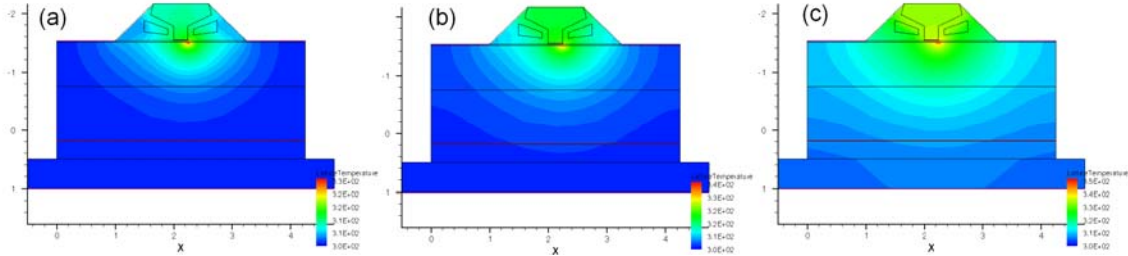


Figure 8: Thermal transient after 10ns (a), 20ns (b), and 60ns (c) of on-state operation.

D. Known Simulator issues.

A number of bugs and issues have been discovered in the course of building DESSIS simulations. This section will briefly mention the more significant of these that have caused issues with HEMT modeling during the course of this project, but will not go into issues of convergence, solution accuracy, etc. While not discussed, the user should be careful to make sure the mesh is appropriate for the problem, that all physical effects incorporated in the device simulation have appropriate parameters specified, that the solution has converged, that the accuracy of solution requested is appropriate, and that any new physical effects are carefully tested by for example running simulations of limiting cases.

1. Mobility at the edge of a heterointerface

DESSIS calculates mobility along nodes between cells as a function of field, temperature, doping density, etc. Where there is a heterointerface, there will also be a boundary between cells and a discontinuous mobility, as the value changes from one material to another. By default, DESSIS uses one mobility value at this interface, which of course cannot be right for both the AlGa_N and the Ga_N side of the interface. While there is an option to calculate two values at the interface, this is not used because it has caused convergence issues when enabled. With this option disabled, DESSIS appears to calculate the mobility for a given node as some average computed from dopant concentration, field, temperature, material, etc. at that node and the nearest neighboring ones, so that the mobility at the interface and the neighboring nodes above and below are affected by the presence of the interface, but the nodes beyond this have the expected bulk-like values. Ordinarily, this would contribute to a small error, but in the AlGa_N/Ga_N HEMT the 2DEG is confined at this interface and so the fraction of the current affected can be significant, unless the cell height of at least two calls to either side of the interface are made extremely small as is done for more recent simulations.

This effect should be considered whenever mobility changes discontinuously near the 2DEG. For example, if mobility is made doping dependent in the DESSIS parameter file then simulations involving rapid changes in the dopant density within the 2DEG or placing delta doped layers there should be done with care.

2. Approximations arising from Hydrodynamic simulations

Drift-diffusion is the simplest and most straightforward way to simulate device physics, see section 4.2.2 of the DESSIS version 10.0 manual [1]. However, this is not sufficient for simulations where hot electrons are a necessary part of the physics. Hot electrons will fill traps with levels far above the Quasi Fermi Potential (QFP) that would remain empty otherwise (as explained in a later section), can trigger degradation mechanisms, and can distort the high field region of the device when the energy relaxation time of the electrons, (tau_w)_ele in the DESSIS parameter file, is great enough that the relaxation length is sufficiently large that electrons do not come to steady state with their local environment [6]. This is expected for example when the relaxation length approaches the size over which the driving fields in the device change substantially, which for example was roughly between 0.15 ps and 1.0 ps relaxation time for one simulation of an AlGa_N HEMT with standard dimensions run recently.

It should be noted that this implementation is a rough approximation of reality. The hot electron lifetime should be a function of energy and not a single value. Also, DESSIS assumes a Fermi or Boltzmann distribution of electron energies with no maximum cutoff energy. However, in reality it is impossible for an electron to gain more energy than the potential of the most negative terminal of the device, without processes such as Auger recombination. A recent simulation with a long electron lifetime (meaning a high electron cutoff energy) and Auger processes turned off showed charging of the floating substrate of some 30V negative relative to the most negative terminal of the device. This was due to a tiny fraction of extremely hot electrons reaching the substrate and getting trapped, and was not expected to be physical. The effect on drain current can be seen in Fig. 9, this charging had a significant effect on device current because the high

substrate potential set up a field that depleted the 2DEG significantly from what was the case without this charging effect present.

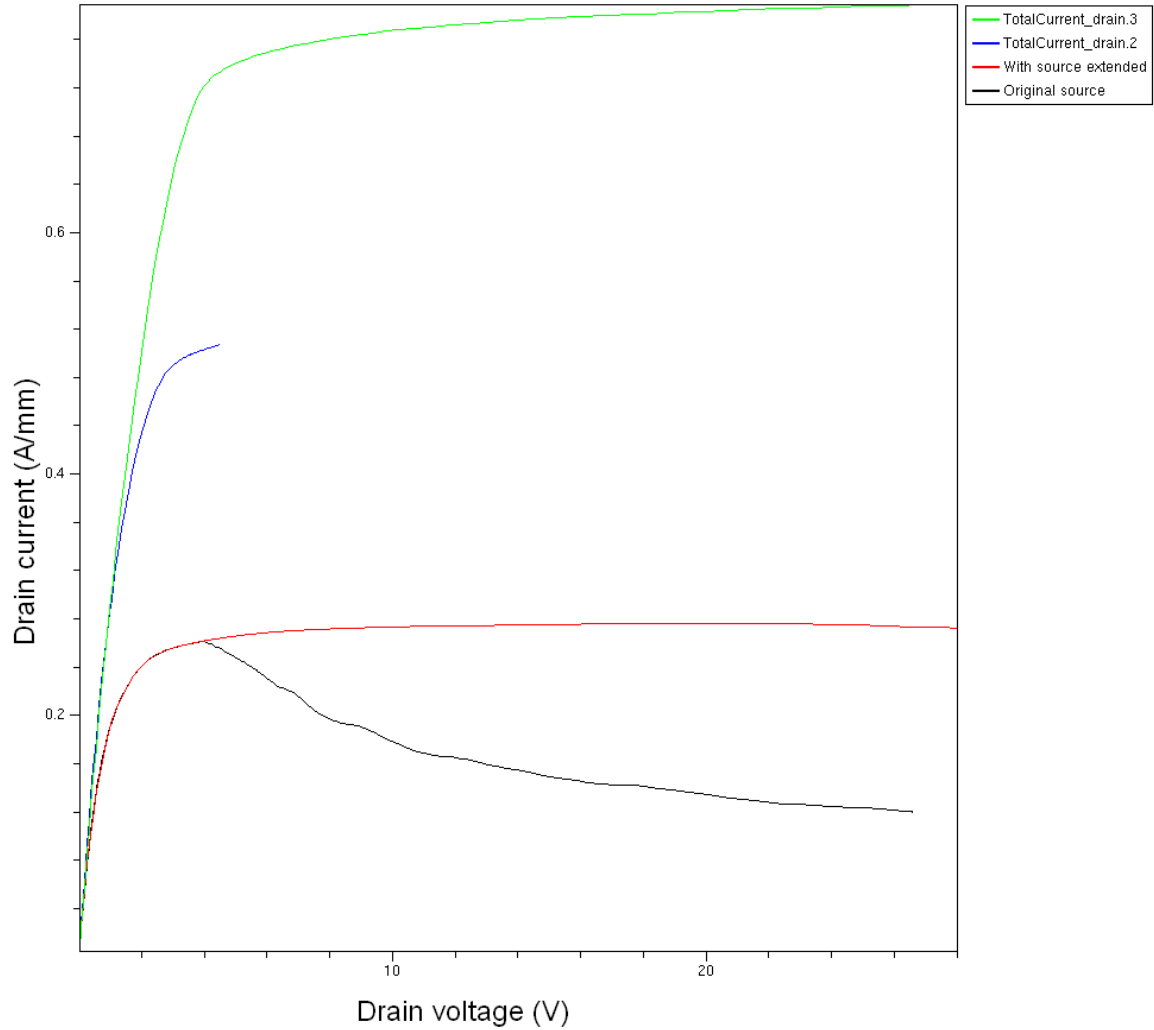


Figure 9: Drain current before (black) and after (red) extending the source contact to ground the epi/SiC interface, showing the difference that charging of the GaN makes in Hydrodynamic simulations. The GaN substrate charged to a potential of $\sim -30V$ due to an approximation made in the DESSIS implementation of Hydrodynamic simulations in the black curve.

3. Electron density and Quasi Fermi Potential

DESSIS computes Quasi Fermi Potential (QFP) for the purpose of calculating electron density, trap occupation, etc. The DESSIS and the Sentaurus Device manual as of this time specify that QFP (E_{Fn}) under Boltzmann statistics is determined by the value that satisfies the following relation for density of electrons,

$$n = N_C \exp\left(\frac{E_{F_n} - E_C}{kT}\right),$$

where the density of states is

$$N_C(T_e) = N_C 300 \times \left(\frac{T_e}{300}\right)^{\frac{3}{2}} \text{cm}^{-3}$$

More complex but analogous equations describe Fermi statistics. For Hydrodynamic simulations, where there is an electron temperature and a separate lattice temperature, the correct equations would use the electron temperature. However, the QFP reported out by the program uses the lattice temperature in both equations (despite the appearance of T_e in the quoted equation). Discussions with Sentaurus technical support (Nelson Braga) indicate that DESSIS calculates a QFP with the electron temperature and another with the lattice temperature, and only reports out the second. However, they are both used internally where appropriate.

4. Errors in hydrodynamic simulations

In general, mobility must degrade as average electron velocity increases. There are two choices that can be made for the electron mobility as a function of field. The first choice is that the mobility can degrade by the same equations as it does in Drift-Diffusion (DD), as a function of the electric field or the gradient of the QFP (4.2.2 and 8.8 of the DESSIS manual). The second is that the mobility can degrade based on the electron temperature (8.8.7 of the DESSIS manual) derived from the Hydrodynamic equations (4.2.4 of the DESSIS manual).

For the first option, mobility comes out far too low in the high field regions near the 2DEG when running a Hydro enabled simulation, and this appears to arise because of the way that QFP is computed in these regions. Under Drift-Diffusion at small and moderate biases, and in regions where the 2DEG density is not changing rapidly parallel to the AlGaIn/GaN interface, the component of the gradient of the QFP parallel to this interface is very close to the value of the electric field parallel to the interface. Perpendicular to the interface, the gradient of the QFP is small. Since there is very little current flowing perpendicular to the interface, this makes sense. So the total gradient of the QFP is close to the value of the driving force. Under Hydro, the QFP is computed differently, and there is a large gradient of the QFP perpendicular to the AlGaIn/GaN interface. However, as is expected from charge balance, there is still almost no current flowing in this direction! The result is that the total value of the gradient of the QFP is too great and the mobility is computed to be a factor of several smaller than it should be. The origin of this issue is unknown, but running hydrodynamic simulations with this form of high-field mobility degradation should be avoided until it is resolved.

E. Field plate.

Field plate (FP) simulations have been done which show the effect on the device with/without the plate at various voltages and for two different FP thicknesses. The plate is seen in simulation to cause some 2DEG depletion under it but otherwise do very little until a critical drain voltage is reached that causes the 2DEG under the plate to deplete. This happens because the 2DEG on the drain side of the gate tracks the drain voltage, while the FP is connected to the gate or source and does not. The voltage difference increases the electric field until the displacement charge reaches a value high enough to deplete the 2DEG. As this point local 2DEG resistance under the FP increases to the point that a significant voltage drop develops across the 2DEG and the FP acts to insulate the pinch-off region at the drain side of the gate from additional fields. For sufficiently high fields, a new pinch-off region will develop at the end of the FP in addition to the existing one at the end of the gate. These simulations were done on proprietary structures and requests for further details have to go through Eric Heller, Don Dorsey or Chris Bozada.

F. Thermal steady state.

DESSIS can do both isothermal simulations and simulations where “lattice heating” is allowed. This is separate from “electron heating” discussed in the Hydrodynamic section, and either or both can be enabled independently in DESSIS. Lattice heating slows the simulation greatly and requires that temperature dependent thermal conductivities are specified and that proper thermal boundary conditions be put in place. However, heat changes device behavior (mainly because mobility goes down with temperature) and is also a factor in almost any device degradation process. Thermal management is made more critical for AlGaIn/GaN power HEMTs because of the high temperatures these devices can reach, with junction temperatures several hundred degrees above ambient.

DESSIS allows thermal conductivity to be expressed as a power law fit to local temperature in degrees K. Over the range of interest for device modeling, this is sufficient to express known conductivities well for all materials used in a HEMT, even though conductivity as a function of temperature is often expressed in other forms. Boundary conditions must be treated more carefully, however. The top of the HEMT in a test stand is typically exposed to air, and it can reasonably be assumed that no heat flows through this boundary. To simulate the thermal properties of the substrate requires a 3 dimensional (3D) simulator to handle the substrate and in some cases also the test stand, since the gate-gate spacing (25-50 μm typ.) and the gate width (100-500 μm typ.) are both on the order of the substrate thickness (100-350 μm typ.). The current DESSIS and Sdevice licenses only allow 2D simulations, so a proper treatment using this software is impossible. Fortunately, the electrical part of the problem can usually be simulated by 2D since the gate width (100-400 μm typ.) is far greater than the epilayer thickness of (1-2 μm typ.) and any other dimensions in the problem with a great effect on the electrical properties such as S-D spacing, gate length, etc. The gate edge is an exception since it cannot be treated in this fashion but fortunately it is only a small part of the total width. Also, such issues as impedance along the gate, source, and drain widths complicate the picture, but appear to be small for low frequency analysis. The approach chosen for simple thermal analysis was to simulate the thermal problem in 3D and to reduce the

thermal properties of the substrate into a “thermal resistance” that can be incorporated into the 2D electro-thermal DESSIS simulations of the epilayers.

DESSIS allows the thermal resistance of a thermal and/or electrical contact to be specified in ($\text{cm}^2\text{K/W}$), but forces each contact, or any set of contacts referred to by the same name, to be at one uniform temperature. So, the simplest approach is to lump the entire substrate into one thermal resistance, and to specify this thermal resistance in DESSIS for the contact to the bottom of the epilayers, which are then at one temperature. A 3D thermal only simulation is run, where the device heating is assumed to be along the gate, a reasonable approximation in pinch-off device operation. Fig. 10 shows a typical thermal profile at the epi/SiC interface under the gate, and $2\text{ }\mu\text{m}$ away from this along the epi/SiC interface. It can be seen that there is a modest $\sim 1\text{-}4$ degree difference in this direction over a distance scale relevant to the electrical properties (S-G and G-D spacings are typically $\sim 2\text{ }\mu\text{m}$). The DESSIS simulation described assumes a slice in this direction, so this is the level of error introduced by assuming the bottom of the epilayers are at one temperature. However, the temperature varies by $\sim 20\text{ }^\circ\text{C}$ from gate center to gate edge, and so the temperature of the gate also varies by about this amount from center (hottest) to edge. Depending on the purpose of the simulation, typically the peak or the average temperature rise of the epi/SiC interface above ambient is divided by the power dissipation assumed in the simulation to give the thermal resistance of the substrate, which can be used as the substrate resistance in the DESSIS simulations to give the peak or typical thermal profile of the epilayers respectively. Peak temperature was used to derive Fig. 11. It should be noted that the thermal conductivity of the SiC substrate is temperature dependent, but DESSIS does not allow the thermal resistance to be given as a function of the power dissipation or the local lattice temperature. This will create an error that must be considered. This error is usually small, but can be large if for example the thermal resistance is computed at ambient temperature, but then used at $200\text{ }^\circ\text{C}$. It is best of course to run the substrate thermal simulation with appropriate temperatures for the device of interest. A later section will discuss a more elaborate thermal model built for publication which addresses all of these approximations.

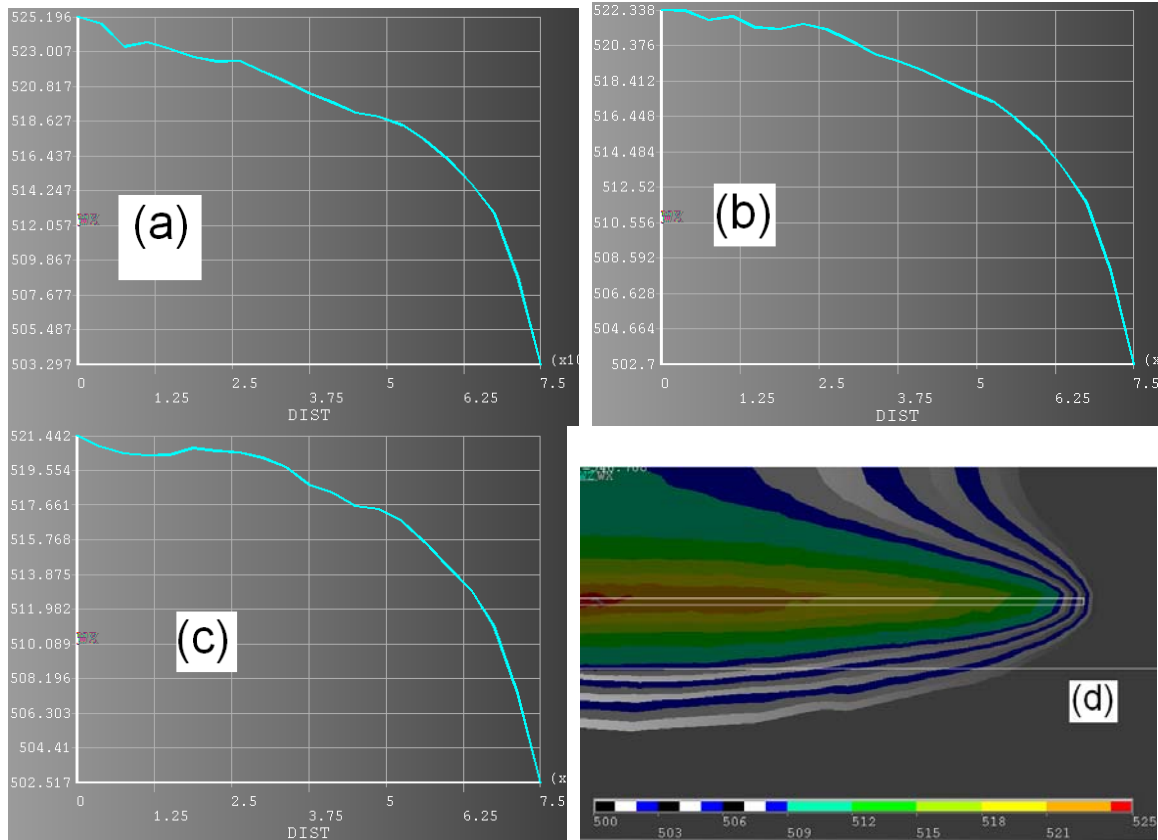


Figure 10: ANSYS [7] thermal simulation of the SiC substrate, with 473 K (200 °C) substrate base temperature, for a 2x150 test structure with 40 μm gate pitch.

In Figure 10, simulation runs from the center of the gate to the gate edge (0.075 mm), symmetry gives the other half of the gate. Part (a) is directly under the gate, at the epi/SiC interface and (b) is 2 μm away in the direction toward the other gate, also running parallel to the gate at this same interface. (c) is the same as (b) but 2 μm away from the second gate instead of toward it. As expected, the line profile (c) looks very similar to (b) but slightly cooler. (d) shows the temperature in the plane of the epi/SiC interface. Line fluctuations in all parts are due to the nature of the meshing, which was not fully optimized. This problem has since been fixed, by changing from the default ANSYS mesh based on tetragonal elements to one that uses tetragonal elements far from the device and rectangular ones with high aspect ratios near the gates, where temperature changes very slowly as a function of distance parallel to the gate width but rapidly in the other two dimensions. Device power was 5.07 W/mm.

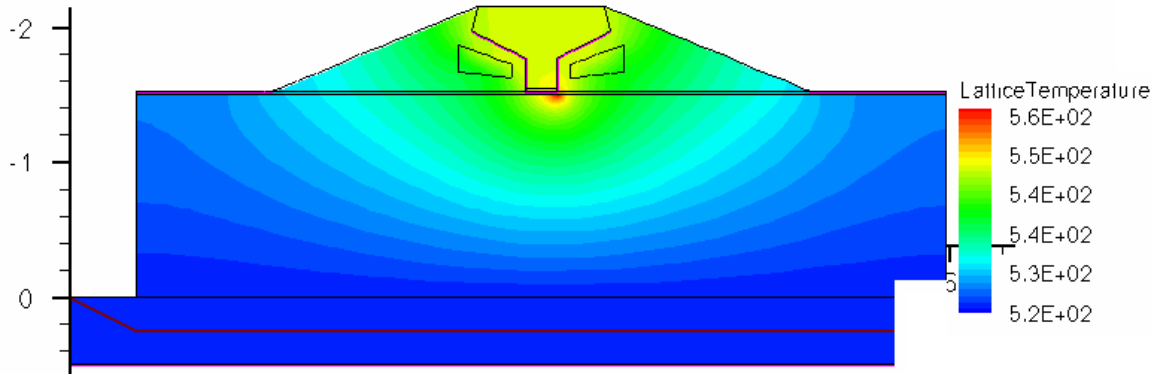


Figure 11: Based on the peak temperature, a DESSIS model of the epilayers looks like this.

In Figure 11, a small portion of the SiC substrate is included but does not affect the simulation. The gate is the standard Au/Ni mushroom gate and S/D metals are not in the simulation, except as electrical boundary conditions. The D side of the gate (to the right) contains the pinch-off region and the simulated hot spot.

G. Hot electrons.

The basics and some effects of hot electrons were discussed in the Hydrodynamic section, with regard to practical issues running Hydro that the user must be aware of. This section will focus on some of the effects of hot electrons when they are implemented correctly. Specifically, trap charging and degradation are the biggest effects seen so far. Electrons in DESSIS are assumed to momentum scatter efficiently, but energy loss is modeled as happening at a rate proportional to

$$\left. \frac{dW_n}{dt} \right|_{\text{coll}} = -H_n - \frac{W_n - W_{n0}}{\tau_{en}}$$

where W_n is the energy density of the electrons ($N * 3/2 kT_e$) with their elevated electron temperature T_e , W_{n0} is the energy density of an equivalent population of thermalized electrons at the lattice temperature T_L , τ is the hot electron lifetime (τ_w)_{ele} in the parameter file (see the simulator issue section for important information on this parameter), and H_n is a term for recombination heating, usually not a significant contributor. Due to the efficient momentum scattering, hot electrons scatter and travel in all directions, and fill traps as seen in Fig. 12. The net effect is a reduction in the 2DEG density when deep traps are significant.

Hot electrons are also expected to play an active role in device degradation, and a lot of this has gone into the work of Martha Gallivan from the Georgia Institute of Technology, June and July 2006. This work is well summarized by her report.

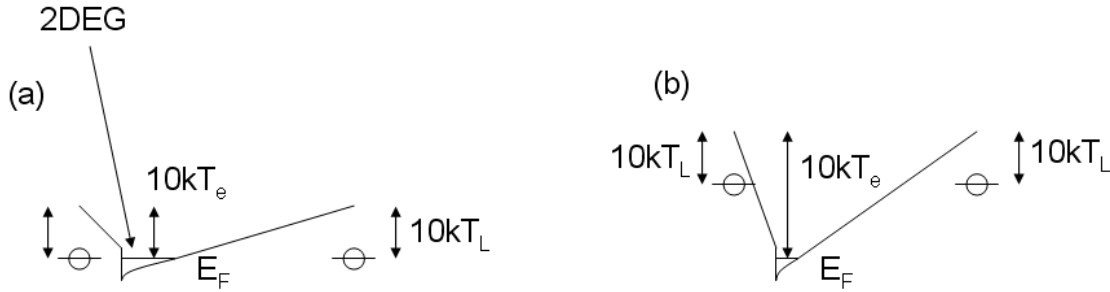


Figure 12: Main mechanism for trap charging.

In Figure 12, (a) shows traps in steady state drift-diffusion, where $T_e = T_L$. Those traps at 50% occupation are at the same energy as the Fermi level in the 2DEG, and the energy barrier is of course the same for an electron going from the 2DEG to the trap as going the other way. Traps may exist above and below E_F , of course, but only one level is shown for clarity. Part (b) shows the situation when $T_e > T_L$. The “effective” barrier is still the same value of $10 kT$ for both paths, but not the actual energy barrier, because electrons thermalize to the local lattice temperature when trapped. Hot holes can exist as well and follow an analogous process.

H. DESSIS vs. Sentaurus Device

As mentioned in the intro, Synopsys no longer supports DESSIS, and have positioned Sentaurus Device (Sdevice) as a replacement that should simulate legacy DESSIS code “as is”. AFRL currently has access to run both codes, but without support for bug fixes and upgrades, DESSIS is already inadequate for Hydro and will continue to be marginalized.

Two differences have so far been seen between the two simulators. One is that by adding the command “add2totaldoping” to the trap statement in the command line, traps in DESSIS can degrade mobility through the scattering caused by the point charge of a charged trap. DESSIS adds the trap density to the dopant density and the total is fed into the dopant sensitive parameterization of the mobility. This was imperfect, because DESSIS assumed that all traps caused this degradation, regardless of their charge state, so that neutral traps would contribute to the same mobility degradation as charged ones. Sdevice, however, does not support the “add2totaldoping” command. This means simply that any simulations with this command behave differently on the two simulators, and a large correction must be made to most of my simulations to get agreement.

The other difference discovered so far is that the trap field “DeepLevels” that is used in mdraw and commonly referenced in the DESSIS/Sdevice command file behaves slightly differently. Setting the density of DeepLevels traps to zero in the DESSIS command file will turn off the field. Setting this to zero in Sdevice does not, although setting a value low enough to be ignorable such as 1 cm^{-3} works.

At this point, simulations tested between the two programs agree well, so this should be the only other difference for those parts of the physics used by my models so far. As a practical point, DESSIS simulations by default use a parameter file name “Datexmaterials.par” and Sdevice uses “Sdevice.par” by default.

IV. Refined thermal model:

Previously, it was discussed that the substrate cannot be put into DESSIS accurately for typical device dimensions because it requires a 3D treatment but DESSIS at AFRL currently is restricted to 2D. A basic thermal model has been discussed for accounting for the substrate that works reasonably for most purposes, especially at small and moderate power densities.

A more elaborate thermal model has been built with a far more accurate treatment, addressing all of the approximations discussed previously. This model has been cleared and sent for publication and the following section draws heavily on the text generated in the upcoming publication. Temperatures for various points within a device were determined as a function of biasing conditions, substrate thickness and temperature, number of fingers, and gate length and pitch. Comparisons with simpler models were made, showing that a purely thermal finite element approach is expected to work for some thermal resistance determinations, but not when device bias or gate length is changed. As a practical application, this thermal modeling shows that life test results of industry-relevant devices can be significantly affected by the exact testing technique used.

Experimental techniques such as Raman spectroscopy, IR thermal imaging, photoluminescence and application of liquid crystals have been used with some success but are limited by either spatial or temperature resolution [8-11], and can have difficulty measuring the hottest part of the junction, which is often obscured by the gate metal. Thermal modeling circumvents some of these issues. Several efforts have modeled the device and substrate with the assumption that the thermal dissipation can be modeled as a constant power emitter of some characteristic length and width along the gate edge [12-14], and other efforts have modeled the two-dimensional thermal profile within the HEMT to gain a better understanding of local variations [15, 16]. In this work, we couple an electro-thermal model of HEMT operation with a three dimensional thermal model of the substrate. We find that the thermal resistance varies significantly within the device and as a function of bias, where thermal resistance is defined for this work as the temperature difference between one point in the device structure and another per W/mm power dissipation within the entire device structure, and power is expressed as power per unit gate length. Specifically, we find that the device thermal resistance can vary significantly with the biasing conditions used in a life test, significantly impacting the computed activation energy of failure modes and therefore the extrapolated operating lifetime.

The structure was simulated as two regions. Region 1 is the HEMT epitaxy, up to and including the AlN interlayer, and Region 2 the substrate, assumed to be SiC. Region 1 was modeled using the 2D electrothermal device simulator ISE-DESSIS [1], with major thermal model parameters given in Table II. DESSIS provides accurate modeling of device heating, as heat is self-consistently generated within the device. This is primarily from Joule heating within the entire 2DEG layer and especially at the gate edge. Region 2 was modeled thermally with the 3D ANSYS [7] simulator, and the two joined via the interface between the substrate and the AlN interlayer. The model was verified and calibrated by simulating $2 \times 150 \mu\text{m}$ test devices with $4.0 \mu\text{m}$ source-drain spacing, $40 \mu\text{m}$ gate-gate spacing and $0.22 \mu\text{m}$ gate length as measured by TEM. The GaN layer was grown by MOCVD on $\sim 350 \mu\text{m}$ thick SiC substrates, and the gate is a Ni/Au mushroom-

gate structure. Eric Heller (AFRL/MLPSM), Don Dorsey (AFRL/MLPSM), or Chris Bozada (AFRL/SNDD) can be reached for additional details. Figure 4 from Part III of this report shows comparison between experiment (dots) and this model (solid lines), assuming the base of the substrate is held at 300 K. The disagreement is probably from bulk or surface traps near the gate [2], which were not incorporated in this model. A more complete description will be published in the future. In addition, we have tested thermal resistance predictions of our model against the published measurements of M. Kuball et al. based on their stated device dimensions [17], and find agreement as shown in Table III. The thermal conductivity of SiC and GaN are not known with precision [18], and are the largest sources of error in this work. We believe that modeling is useful to illuminate trends in thermal resistance with changing device parameters, but at this time absolute numbers for a given device geometry require calibration and verification with experiment.

Fig. 13 shows comparison of our model to an analytical model of the substrate and epilayers developed for AlGaIn/GaN devices by A. M. Darwish et al. [13], and seen in their work to fit well to their finite element simulations of the same volume. Some analytic models exist prior to this work [19], but most assume the substrate has the same thermal conductivity as the epilayers, not valid for AlGaIn/GaN devices on SiC, sapphire, or Si. Fig. 13 (a) and (b) show that their analytical model agrees well with our results over a range of substrate thicknesses and gate widths. However, as shown in Fig. 13 (c), it does not correctly capture the effect of changing gate length. The root cause is that their models both assume that power dissipation is distributed evenly over the area of the gate/semiconductor interface, such that a greater gate length increases this area and necessarily decreases the total thermal resistance. It is known that a more detailed treatment will predict a different heating profile, and our electro-thermal modeling produces heating through power dissipation that is primarily near the edge of the gate on the drain side, and not over the entire length of the gate, in a region that does not necessarily increase in area as the gate length increases. In our model, gate length has only a very weak effect on thermal resistance for this simulated device.

Thermal profiles and cross sections of a typical device are shown in Fig. 14. Power dissipation will vary with device parameters, but in this example was 6.43 W/mm at the hottest point in the device (gate center of the two middle fingers), 8.08 W/mm at the edge of an outer finger, and 6.79 W/mm average. This power dissipation variation is due to the temperature variation along the fingers as shown in Fig. 14 (c) and primarily due to the temperature effect on electron mobility that is assumed to vary based on a fit to Monte Carlo simulations [20]. This power variation moderately reduces the thermal resistance of the hottest point in the HEMT, since more power dissipates in the ends of the farthest out fingers and less in the center. The effect is about 3% in the largest device we studied (Fig. 14) and less in smaller devices, as compared to a simulated device with the same total dissipated power but no variation finger to finger or along the gate width. While this effect is included in this work and may be important for other reasons, its effect on the thermal resistance will be negligible in most cases. Ohmic losses along the source and drain contacts as current flows parallel to the gate may have a significant effect but were not included in the model. Contact source/drain resistances are assumed to be constant with temperature as temperature dependence of this parameter is observed to be weak at device operating temperatures [21]. The thermal conductivity of the

source/drain metals are not expected to affect the thermal resistance much [13], and this was not included in the thermal model.

Table IV shows thermal resistance of the hottest point in the device (in Region 1 close to the drain-side corner of the gate at the AlGaIn/GaN interface), and the thermal resistance of Region 2. As expected, thermal resistance increases with reduced gate pitch and with higher substrate temperatures due to the decreasing thermal conductivities of the materials with increasing temperature. The thermal resistance of the substrate (Region 2) increases as gate bias becomes less negative primarily because of the extra drain current and device heating and its effect on bulk thermal resistivity. However, this change in gate bias *decreases* the thermal resistance of Region 1. This is because as the gate swings to more positive voltages for a given drain bias and the device necessarily heats up, the resistance of and the current across the 2DEG both increase significantly, increasing the fraction of the total power dissipated outside the pinch-off region such that the temperature of the pinch off region increases less relative to what would otherwise be expected. Many traditional models for thermal resistance do not take this into account [13, 19, 21], and assume that the heat is dissipated uniformly along the gate.

These subtle thermal considerations can have a significant impact on life test results. For example, the effective thermal resistance at regions of the 2DEG far from the pinch-off region, such as the source/drain pads, may increase as the thermal resistance at the gate edge decreases. This is an important point to consider when changing gate bias during life testing; our simulations show that when gate bias is adjusted to get the same power at different substrate temperatures, the *biggest temperature rise can be at the source/drain region* instead of near the gate, and so accurate temperature modeling requires accounting for heat dissipation *as a function of gate bias*. In another example, an 8×400 , $25 \mu\text{m}$ gate pitch device as shown in Table IV with 450K substrate temperature has a simulated power consumption of 4.61 W/mm at $V_G=0$ and $V_D=10$. The hottest point of the device is simulated to be 634 K for simulated thermal resistance of 39.9 K mm/W. At 430K, the device will require $V_G=-0.232$ to achieve the same power and the new thermal resistance will be 37.7 K mm/W, and the drop in temperature in the device at the hottest region in the device is not 20K but instead is modeled as shown in Fig. 15 (a) as 30.1K. If instead, we had changed V_D to preserve the same power, the map of temperature changes looks like Fig. 15 (b), with the hottest point decreasing in temperature by 32.2K. Models that don't account for the origin of heat in a device will not distinguish between Figs. 15 (a) and (b). The difference in temperatures is only a modest 2.1K and would not be detected by many experimental thermal measurement techniques [8, 9]. However, this represents 10% of the substrate temperature change that was made and this will affect the predicted Arrhenius activation energy and greatly change the extrapolated lifetime prediction for a device. To illustrate, Singhal et al. [22] measure an activation energy of 1.7eV for degradation of a GaN HEMT based on a set of life tests, and predict a MTTF at a junction temperature of 150 °C based on life test junction temperatures from 200 to 310 °C. We don't have the detail required to simulate junction temperatures based on their devices, but even a 5% change in this E_a will change MTTF by about a factor of 2 when extrapolating lifetime from 310 °C to 150 °C. This bias effect is especially sensitive to conditions that change the ratio of power dissipated in the pinch off region to that dissipated in the rest of the device, such as 2DEG sheet and contact resistance, and the drain bias chosen for the experiment.

In conclusion, an electro-thermal model has been built of multi-finger AlGaIn/GaN HEMT device operation that includes heat spreading in the substrate. We find that the variation in the power dissipated in the device along the gate width has an effect on the thermal resistance that can be neglected in most cases. We find that our approach makes very different thermal resistance predictions as the gate length or as the device bias is varied than models that assume the heat dissipation is along the entire length of the gate. In particular the equivalent thermal resistance is seen to vary with applied bias so that it is not sufficient for some applications such as life testing to model the heat source as a uniform source along the area of the gate, if device biases are changed significantly during the test.

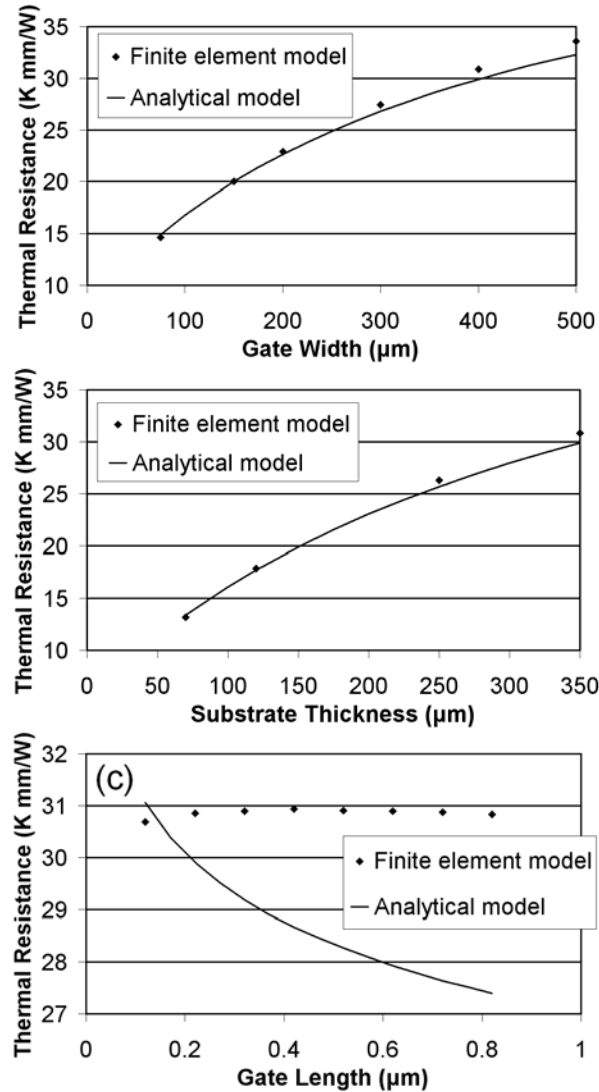


Figure13. Comparison of an analytical model [13] with a simplified version of our model, showing sensitivity to substrate thickness (a), gate width (b), and gate length (c). Both models assumed 400 μm gate fingers except as reported in (a), and 25 μm Gate-Gate spacing. Specifically, to facilitate comparison both models assume thermal conductivities fixed to the 300 K values reported in Table II and assume an infinite number of fingers.

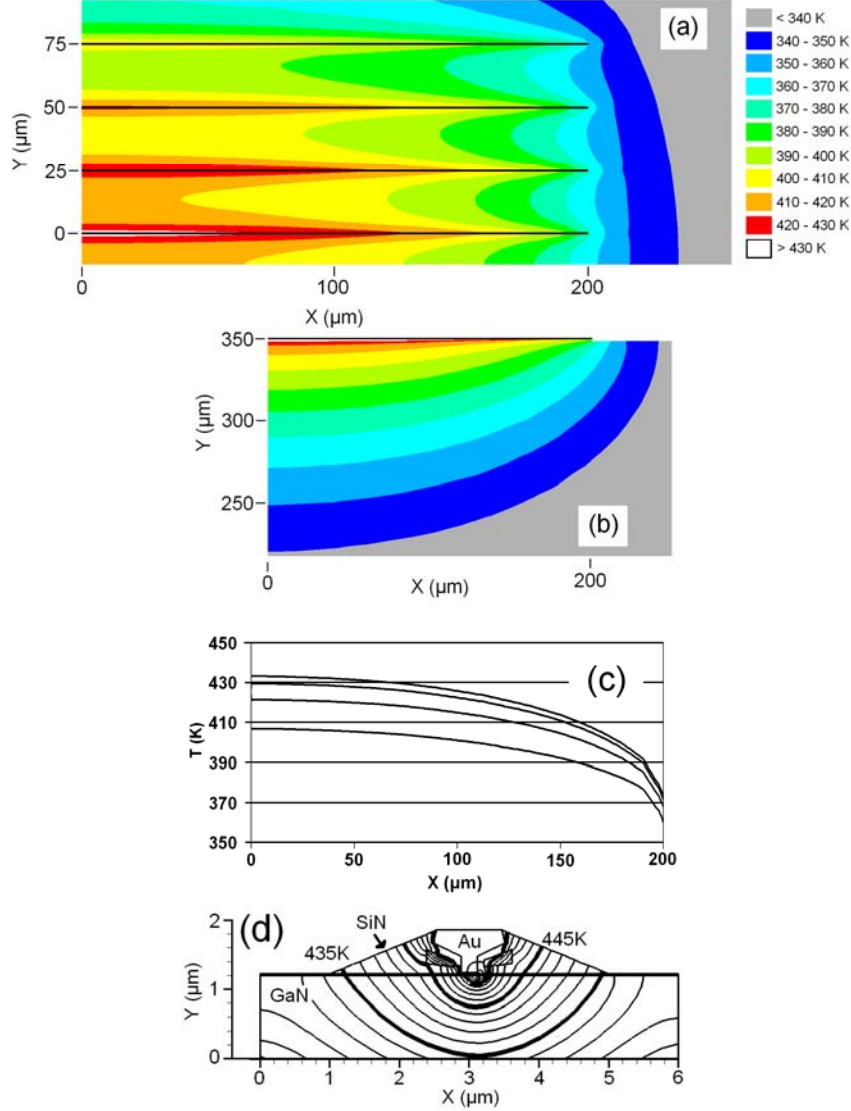


Figure 14. Temperature at the Region 1/Region 2 interface (a), and in a cross-section through a central finger and partway into the substrate (b), for an $8 \times 400 \mu\text{m}$ device with $L_G = 0.22 \mu\text{m}$ and $25 \mu\text{m}$ gate spacing running at $V_D=0\text{V}$ and $V_G=10\text{V}$, and temperature at the bottom of the substrate of 300 K . Gate regions illustrated as black lines. Due to symmetry, only half of the fingers and half of their length are shown. The GaN was $1.2 \mu\text{m}$ thick and the SiC substrate $350 \mu\text{m}$. Other parameters are as given in Table II. Temperature variation along the fingers (c), from center to edge at the top of Region 2. A contour plot of Region 1 at the hottest point (d) shows that the extent that the hot spot is localized. A 20 nm Ni layer is present between the Au and the 21 nm thick $\text{Al}_{0.27}\text{Ga}_{0.73}\text{N}$ layer. Divisions go from 427 K (outermost) to 465 K (innermost) with 2 K intervals, with thicker divisions at 435 , 445 and 455 K . The temperature changes rapidly at the hottest point and reaches 468 K , near the drain edge of the gate. Source/drain ohmics are present where the SiN passivation tapers off, but are not included in the thermal analysis.

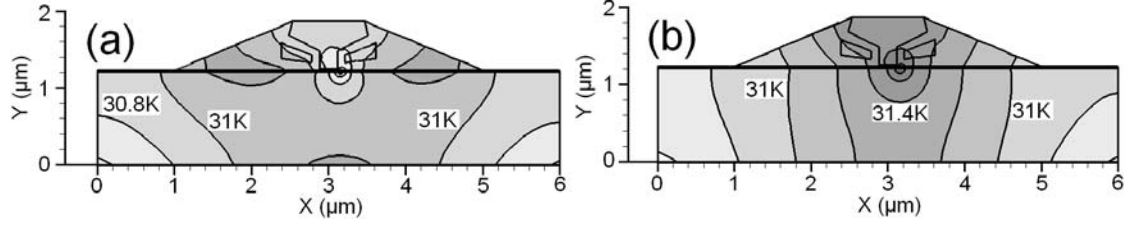


Figure 15. Temperature reduction in Region 1 predicted in a constant power life test where the substrate temperature has been reduced from 450 to 430 K. Constant power is achieved by adjusting V_G (a) or V_D (b). The greatest difference is seen in the behavior of the hottest spot, under the gate. Contours are at 0.2 K intervals.

Table II. Main parameters used in thermal device modeling, unless otherwise stated.

Parameter	Value
κ_{GaN} ^[23]	$2.67\text{--}4.25 \times 10^{-3} T + 3.0 \times 10^{-6} T^2 \text{ W cm}^{-1} \text{ K}^{-1}$
κ_{SiC} ^[24]	$3.87 * (T/293)^{-1.49} \text{ W cm}^{-1} \text{ K}^{-1}$
κ_{AlGaIn} ^[25]	$0.3 \text{ W cm}^{-1} \text{ K}^{-1}$
κ_{SiN} ^[1]	$0.185 \text{ W cm}^{-1} \text{ K}^{-1}$
C_{BD} ^[26]	$8.33 \times 10^4 \text{ W cm}^{-2} \text{ K}^{-1}$
κ_{Ni} ^[27]	$1.33\text{--}1.72 \times 10^{-3} T + 9.9 \times 10^{-7} T^2 \text{ W cm}^{-1} \text{ K}^{-1}$
κ_{Au} ^[27]	$3.36\text{--}6.4 \times 10^{-4} T \text{ W cm}^{-1} \text{ K}^{-1}$

C_{BD} is the surface conductivity of the AlN buffer layer.

Table III. Model predictions vs. M. Kuball et al. [17]. To simulate micro-Raman temperature measurements, our thermal resistance is based on the average temperature over the surface region from the gate edge to a point 1 μm from the gate edge. Data in units of K mm/W.

	1 $\times$ 200	4 $\times$ 250 50 μm gate pitch	8 $\times$ 250 25 μm gate pitch	4 $\times$ 500 50 μm gate pitch	8 $\times$ 500 25 μm gate pitch
M. Kuball et al. K_{exp}	6.4	7.4	14.8	12.9	17.5
M. Kuball et al. K_{sim}	5.8	9.4	15.6	11.2	19.3
This work K_{sim}	6.3	9.7	15.1	11.2	18.2

Table IV. Device thermal resistance (R_{TH}) from the base of the substrate to the hottest point of the buffer/SiC interface (labeled Region 2) and R_{TH} from this point to the hottest point of the device (labeled Region 1) as a function of component geometry and thermal assumptions. Total thermal resistance is of course the sum of these. Thermal resistance reported is based on variations of a device with 0.22 μm gates in a 8×400 structure with 25 μm gate pitch, 1.2 μm GaN, 350 μm SiC, 300 K substrate, thermal conductivity for SiC based on [24] and GaN based on [23] . Other parameters are as given in Table II.

Varied parameter	R_{TH} at $V_G=-2$ and $V_D=10$	R_{TH} at $V_G=0$ and $V_D=10$
	(K mm/W)	(K mm/W)
	Region 2/Region 1	Region 2/Region 1
8×400 , 25 μm gate pitch	17.3/6.8	19.6/5.5
4×400 , 25 μm gate pitch	11.5/6.6	12.7/5.4
2×400 , 25 μm gate pitch	7.5/6.6	8.0/5.3
4×400 , 50 μm gate pitch	9.5/6.6	10.4/5.4
2×400 , 50 μm gate pitch	6.8/6.5	7.3/5.3
2×150 , 50 μm gate pitch	5.5/6.5	5.7/5.2
300 K substrate base	17.3/6.8	19.6/5.5
350 K substrate base	21.6/7.1	24.2/5.7
400 K substrate base	26.1/7.4	29.0/5.8
450 K substrate base	30.9/7.6	34.0/5.9
120 μm SiC	11.9/6.6	13.0/5.4

V: Micro Raman

Micro Raman is a technique where laser light is focused down on a small region of typically 1 μm size and a small fraction interacts with phonons in the substance, red-shifting or blue-shifting the light in energy based on the phonon energy and whether a phonon was created or consumed. It is very well known that micro Raman can be used to measure local temperature; temperature affects the ratio of red-shifted light (the Stokes peak) to blue-shifted light (Anti-Stokes), the width of the lines, and the amount of shift observed (called the Raman frequency). Using micro-Raman to measure temperature in GaN is well documented, especially the change in Raman frequency, and can give temperature profiles to $\sim 1\ \mu\text{m}$ accuracy [8, 17, 28, 29]

Two small studies were done with micro Raman using David Liptak's system (AFRL/MLBP). The first involved heating an unannealed Ohmic stack to $\sim 600\ \text{C}$ for ~ 15 minutes to watch the anneal process. Fig. 16 shows before and after anneal for the 4 different ohmic metals present on the mask. This is not the typical anneal process for an Ohmic stack, but was the maximum temperature attainable in the sample holder used. The Raman peak for the E2 mode was observed to redshift with temperature as expected, although the precise temperature of the sample was unknown and so a quantitative comparison was not possible. The second study was followup on accidental observation of signal penetration through the metal. The E2 and A1 Raman peaks for GaN could be seen through the fourth Ohmic metal composition (shown in Fig. 17), but not through the other three. This suggests that this technique is of some value for determining if an Ohmic stack is continuous or if it is thin enough in spots to allow light to penetrate.

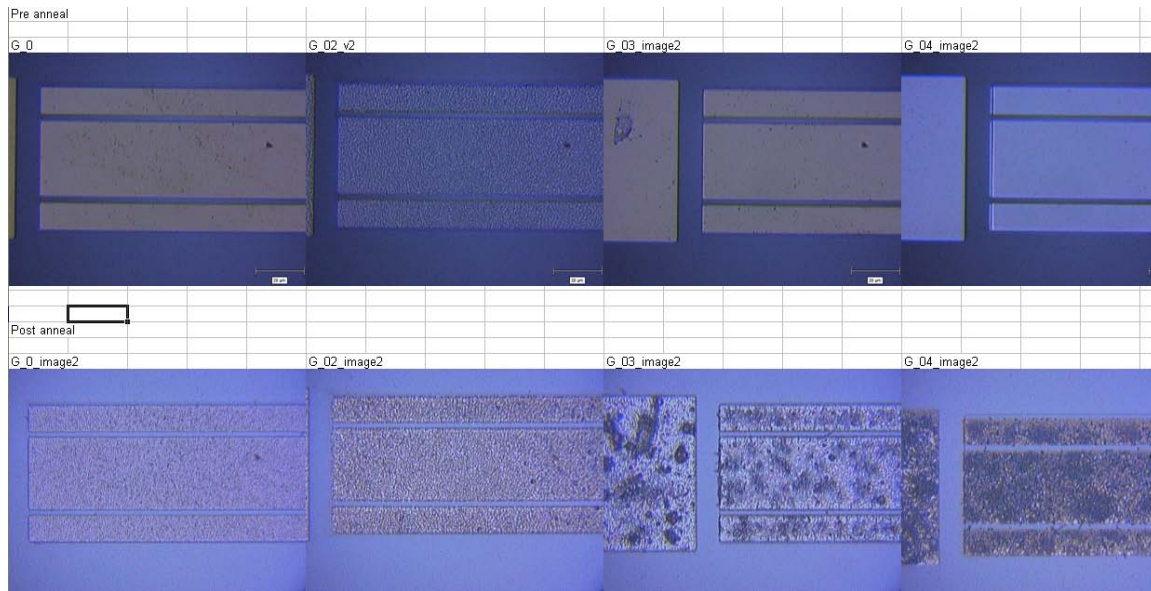


Figure 16: Pre anneal (top) and post anneal (bottom) for four different ohmic metallizations on AlGaIn/GaN. SiN and Gate metal are not present. 10 SCCM Ar was flowing.

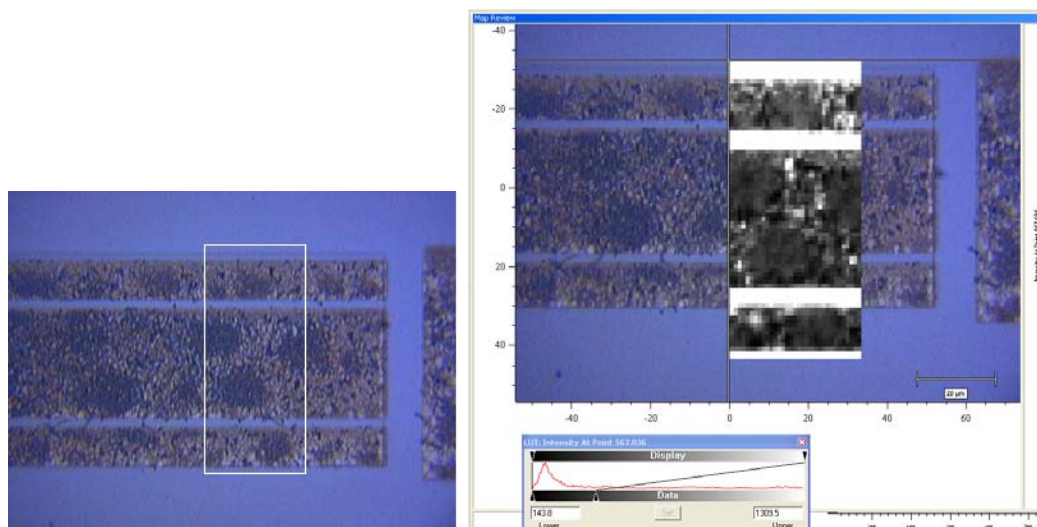


Figure 17: Two optical microscope images of the same region. The second has a Raman E2 mode peak height map overlaid on top. One metal allowed Raman signal to penetrate as shown, while the others did not.

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Appendix A:

Literature review: Deep traps in HEMT structures and findings.

Literature survey of the following topics was done. The goal was to get the Physics right in the planned AlGaIn/GaN HEMT device model; it was obvious that traps are very important to the physics of the device operation, yet poorly understood. No searches are completely exhaustive but should offer a good background for the following topics. While important questions remain unanswered, the literature helped to reduce the range of possibilities.

First, papers were binned into the following categories.

To address the important questions listed below, these papers were then binned according to the questions they address.

- A. Is the surface pinned and if so where?
- B. Where and what energy are the traps located? Intrinsic or hot electron generated ones...
- C. What biasing schemes exist to look for traps, activation energies, etc?

1. Models and theory useful for AlGaIn/GaN device simulation:

There has been a lot of work done, but so far a model for hot electron damage in AlGaIn/GaN HEMTs has apparently not been done.

Y Chang et al., Semicond. Sci. Technol. **20**, 188 (2005). Hong Kong Polytechnic. Simulation of AlGaIn/GaN HEMT as a fn of T. 1-D solution to Poisson and Schrödinger's equations. **Summarizes the spontaneous and piezoelectric effects as fn of T.** Their simulation shows radical reduction of n_s with T, down by 58% when going from 300K to 600K. This prediction seems to be at odds with established research.

John Albrecht et al., IEEE Trans on Elect Devices **47**, 2031 (2000). WPAFB. Gradual channel approximation. Includes S/D regions. Heating included as a thermal resistance and applied to entire channel uniformly. Uses an analytic approximation to $v(E)$ given by Monte Carlo simulations. **Simulated E, V, n_s parallel to channel shown.**

Y. Wang et al., Superlattices and Microstructures. **36**, 869 (2004). China.

Simple model solving Poisson and Schrödinger's equations in 1D. Neglects S and D resistance. **Might be useful as a cross check to early DESSIS simulation results.**

John Albrecht et al., JAP **83**, 4777 (1998). Then at U of Minnesota.

Bulk GaN Monte Carlo simulations. Low field mobility as fn of T from 300-600K and ionized impurity concentrations from 10^{16} to 10^{18} cm⁻³. Also drift velocity as fn of E.

Analytic forms given for these. Also fields to 500kV/cm for 300-600K temperature.

Analytic functions given. Will be different from the HEMT case because of different density of states, charge separation, etc. **Useful as a cross check to DESSIS results in certain limits.**

G. Meneghesso et al., IEEE Trans on Elect Devices **51**, 1554 (2004). U of Padova and U of Modena, Italy and U of CA.

Similar to our plans for expt guided modeling, but didn't look into any damage effects or models. Investigated drain current dispersion in 10-100us timescale. 0.3eV comes from T dependence of gate turn on. Numerical device simulations with traps placed at the ungated AlGaIn surface (virtual gate model). Find that traps there with energy level placed 0.3eV above E_v match their experimental data qualitatively. Believe that charging happens because the negative polarization charge at the surface attracts holes (charging happens by carrier capture/emission). Use both gate and drain pulsing methods. Decent details given on exact experimental technique. See also G. Verzellesi, ... G. Meneghesso et al., IEEE IEDM Tech. Dig. 28.5.1, 689 (2002). U of Padova, U of Modena Italy and U of CA.

W. Saito et al., IEEE Trans on Elect Devices **52**, 159 (2005).

Field plate structure and benefits modeled and tested. Experiment done with devices on same wafer with and without FP. Find high gate leakage at high V_D and a low V_{BR} to be correlated experimentally. Not sure if passivation is the same in the experiment for FP vs. no FP devices.

L. S. Yu et al., APL **73**, 238 (1998). U. of Calif., and Epitronics.

Measured Ti and Ni Schottky barriers on GaN and Al_{0.15}Ga_{0.85}N by I-V, C-V and photocurrent techniques.

2. Interfaces, atomic distribution, substrate effects (very incomplete search):

S. Gokden, Physica E **23**, 114 (2004). Bahkesir U. in Turkey.

Compares experimental mobility vs. T by Hall effect in the AlGaIn/GaN 2DEG to refine theory of roughness and fit certain roughness parameters.

L. Bergman et al., Mat. Res. Soc. Symp. **719**, 185 (2002). U of Idaho

PL of various AlGaIn mole fractions; $x=0, 0.12, 0.22, 0.5, 0.7$.

N. D. Jager et al., Mat. Res. Soc. Symp. **719**, 359 (2002). Germany and CA.

Roughness of cleaved surfaces in GaAs by STM. Can see p-n junctions and individual charged dopant atoms. Technique is best when the surface state density is low but traps might be seen directly this way.

A. P. Zhang et al., Journal of Electronic Materials **32**, 388 (2003). GE and Cornell

Finds that high counts of surface depressions on AlGaIn/GaN HEMTs as seen by AFM and optical defect mapping on SiC can affect gain collapse.

S. Arulkumaran et al., APL **81**, 3073 (2002).

Compare sapphire and SiC AlGaIn/GaN HEMTs. Find more traps in the sapphire ones by looking at light's effect and also a 120Hz "AC hysteresis" measurement that shows a signal similar to current slump. AC hysteresis: Probably pure AC compared to pure DC V_D signal, but it is not entirely clear.

S. Arulkumaran et al., APL **84**, 613 (2004). Nagoya inst of tech., Japan

Compare SiO_2 , SiN, and SiON passivation. SiON might be a good compromise with acceptable DC characteristics and decent V_{BR} .

S. Arulkumaran et al., APL **85**, 5745 (2004). Nagoya inst of tech., Japan

i-GaN capping layer seen to eliminate most trapping regardless of passivation.

O. Ambacher et al., JAP **85**, 3222 (1999). EE Dept. Of Cornell

Have mobility and n_s *mobility vs. interface roughness of the AlGaIn/GaN interface.

Experimental data is in this paper and for theory they reference R. Oberhuber et al., APL **73**, 818 (1998). They also characterize 2DEG density vs. Al content, for Ga and N face growth.

3. Experimental degradation processes (non trap):

A. Sozza et al., Microelectronics and Reliability **44**, 1369 (2004). France/Italy/Germany. Storage and DC life tests done on ohmic and Schottky contacts to $x=.24$ AlGaIn. Tested a Pt/Au and Pt/Ti/Pt/Au Schottky and Ti/Al and Ti/Al/Ni/Au for the ohmic. **They see some contact degradation, both gate and ohmic.** Tests from 300-380C and up to ~500 hours. **Hot electron stressing done on HEMTs**, seem to indicate that temperature is needed to cause degradation (DC current drop). This contradicts some other reports.

B. S. Kang ... R. C. Fitch et al., JVST B **22** 2635 (2004)

Comparison of Ti/Al/Ni/Au to Ti/Al/Ir/Au on same wafer with device characteristics to 550 C, permanent thermal damage is contact metal dependent. See also R. C. Fitch et al., JVST B **22**, 619 (2004) for additional details. Lower contact resistance, better g_m , better V_{BR} seen for Ir. Many devices studied and statistics shown.

J. A. Chisholm et al., Computational Materials Science **22**, 73 (2001).

They find the energy needed to inject a Au, Ni, or Ti atom under N and Ga rich conditions. Find that Ti especially can require a low 1.2eV amount of energy to move into GaN under annealing conditions and acts as a donor. Note that energy for Ti in AlGaIn is not discussed here.

4. Experimental degradation processes (traps likely):

Y. C. Chou et al., Microelectronics and Reliability **44**, 1033 (2004).

Authors stresses a AlGa_N/Ga_N HEMT at 240C for 48h with device running at $I_D=500\text{mA/mm}$ and $V_D=10\text{V}$. They estimate the junction $T=\text{ambient } T + 150\text{C}$. They saw 50% degradation in I_{max} and G_{mp} , but STEM imaging showed no difference between stressed and virgin devices for the Pt/Au gate or the Ti/Al/Pt/Au ohmics. A word of caution: This group seems to assume the thermal resistance is not a fn of T.

C. Tedesco et al., Quality and Reliability Engineering International **9**, 371 (1993). Italy. Unpassivated AlGaAs/GaAs HEMTs. Two tests done **at room temperature**. 1) High vs. low gate reverse current at same power dissipation. 2) same V_D but varying V_G . Find that high V_G and not dissipated power is important for these devices. Show effect of tests on g_m , I_D , parasitic resistance.

Hyungtak Kim et al., Microelectronics and Reliability **43**, 823 (2003). Cornell U. Look into hot electron effects on $x=0.3$ AlGa_N/Ga_N power HFETs with Si_N passivation. Pulsed I-V and DLTS done on hot electron stressed devices and thermally stressed devices. As for C. Tedesco on AlGaAs/GaAs devices, hot electrons from high positive V_D and negative V_G causes the damage and not the power dissipation alone. Stress effects on gate leakage and subthreshold current I_D shown. **I-DLTS done on before/after stress devices, shows creation of a new peak with 1.08eV activation energy after hot electron stress on a SiN passivated sapphire substrate device.**

D. S. Green et al., Journal of Crystal Growth **272**, 285 (2004). RFMD.

Impact of Al_N nucleation. Find that Al_N nucleation temperature affects edge dislocation density and RF dispersion. Also affects device properties differently after operating for an extended time at elevated temperature.

F. Rampazzo et al., Microelectronics and Reliability **44**, 1375 (2004)

This group finds that hot electron degradation will partially recover with several days room temperature storage. **So measuring the devices at a reproducible time is critical. Also find much more hot electron degradation with unpassivated devices than with passivated ones, this argues that the hot electron effect is a near or on surface effect.**

D. K. Sahoo et al., IEEE Trans on Elect. Devices., **50**, 1163 (2003).

Group compared Si_N passivated AlGa_N/Ga_N MODFETs under different stresses.

Channel on with moderate V_D , and channel pinched off with high V_G and high reverse gate current stress. V_D is apparently not reported for the second test.

R. Pierobon, G. Meneghesso et al., ASDAM 2004, The Fifth International Conference on Advanced Semi. Devices and Systems, p. 143, October 17-21. Italy/France.

Compare hot e stress on passivated and unpassivated devices and discuss storage at RT, elevated temperature, and light exposure – seen to recover the devices.

5. Other measurement techniques for traps:

Besides the obvious, the following are explored as interesting possibilities. At a minimum, light exposure needs to be controlled and may serve as a valuable diagnostic technique.

N. D. Jager et al., Mat. Res. Soc. Symp. **719**, 359 (2002). Germany and CA.

Roughness of cleaved surfaces in GaAs by STM. Can see p-n junctions and individual charged dopant atoms. Technique is best when the surface state density is low but traps might be seen directly this way.

D. Sahoo et al., IEEE Trans on Elect Devices **50**, 1163 (2003). India.
 Authors see increase in $1/f$ (flicker) noise at some biases with hot electron stress that they attribute to increased trap creation near channel. Specifically, if hot electrons just filled states and did not create new ones, then the $1/f$ noise would not be expected to increase. Authors also perform hot electron stress and high gate reverse current stress on devices and compare results. However, A. Curutchet et al., Microelectronics and Reliability **43**, 1713 (2003) from France/UK see worse $1/f$ performance for a sample grown on SiC than for one on Sapphire, opposite the expected behavior. This will need to be looked into before using this technique.

A. Paccagnella et al., Electronics letters **28**, 2107 (1992).
 Gives some theory behind analysis of $g_m(f)$ as a tool to characterize deep levels.

P. B. Klein et al., JAP **88**, 2843 (2000). NRL.
 Detailed study of light on reversing the current collapse. Quantify both intensity and wavelength of light needed. They find two trap energies (turn on at $\sim 1.80\text{eV}$ and 2.85eV light), and determine photo-capture cross sections and densities in a GaN MESFET. Klein has several more papers in this topic, for example, P. B. Klein, JAP **92**, 5498 (2002) where they find “complete” restoration of I_D with light exposure. Only 175uJ/cm^2 of 400nm light will excite most of their 2.85eV turn-on traps. However, some traps have much smaller cross sections and require more light.

R. Vetury et al., IEEE Trans on Elect Devices **48**, 560 (2001). U of California.
 Virtual gate proposed between gate and drain based on effect of passivation and lateral extension of the gate field along the surface. Time constant of seconds. Finds that 2.7eV light won't affect the traps but 325nm (3.8eV) light does. Speculates that holes must be generated in the semiconductor that are swept into the traps, since 2.7eV light does not excite them. However G. Meneghesso's ones at only 0.3eV above E_V might function as described by this author.

P. De Wolf et al., JVST B **18**, 361 (2000). IMEC in Belgium.
 Review of several SPM techniques with focus on capabilities for carrier and dopant profiling. Mentions that STM imaging of dopant atoms (N. D. Jager et al.) probably requires a surface where the intrinsic surface states are outside the bandgap. Discussion of STM for imaging pn junctions in surfaces known to have a high density of surface states (UHV cleaved Si).

A Cavallini, Microelectronic Engineering **73**, 954 (2004). Italy.
 Current DLTS (I-DLTS) used and discussed for AlAsAs/GaAs structures. I-DLTS can be used without the need for a FAT-FET or diode structure. Also see A. Cavallini et al., JAP **94**, 5297 (2003).

R. Mosca et al., Superlattices and Microstructures **36** 425 (2004). Italy.
 Current DLTS used on a AlGaIn/GaN HEMT with $1\mu\text{m}$ gate length (width not given) with SiN passivation. Authors find an irregularity in their data that seems to show that thermal history is important in a way they could not determine.

A. Vertiatchikh et al., Electronics letters **38**, 388 (2002).
 Current DLTS done on $x=0.3$ AlGaIn/GaN HEMTs shows reduction of trap signal and elimination of one peak from a trap level with SiN passivation. Argues for near-surface traps. Uncertain what their device size is.

O. Mitrofanov et al., APL **84**, 422 (2004). Bell Labs.

They do a careful analysis of channel current transients for GaN capped $x=0.34$ AlGaIn/GaN HEMTs. Are able to see two well defined recovery times of $\sim 1.0\mu s$ and $175\mu s$ for certain device conditions. For the fast process they see Poole-Frenkel (PF) emission (activation energy is reduced by $E^{0.5}$, where E is the E field). Find that the trap capture process is not thermally activated, but the emission process is. **Based on PF emission, the fast process traps must be near the gate edge, either in the barrier or on the surface.**

S. Nozaki et al., APL **78**, 2896 (2001). U of Calif and HRL Labs in Calif.

I-DLTS done on AlGaIn/GaN MODFET. Find 0.28eV , but note that by analysis of trap and detrapping times find that **this is not the trap responsible for room temperature trapping**. The 0.28eV trap is expected by extrapolation to have 0.5ms time constant but a 0.5s and 15s time constant are actually seen.

A. Hierro, ... S. A. Ringel et al., Phys. Stat. Sol (b) **228**, 937 (2001). Ohio State U.

Use DLTS and **DLOS (Deep Level Optical Spectroscopy)** in MOVPE n-GaN that has been characterized by TEM and EBIC (Electron Beam Induced Current microscopy). Find a defect at $E_C-2.64$ believed related to threading dislocations. Also see A. Hierro et al., APL **76**, 3064 (2000), where traps at $E_C-E_T=0.58-0.62, 1.35, 2.57-2.64, 3.22\text{eV}$ are seen in GaN by using a combination of DLTS and DLOS.

A. Chantre et al., Phys. Rev. B **23**, 5335 (1981). France.

Early paper on DLOS. Looks like the first.

6. Other topics and decent review articles:

Cole Litton and collaborators – Good GaN, AlGaIn survey and characterization plan. Survey of defects seen/expected in GaN, those expected in AlGaIn, defect creation and DLTS of Schottkys. $x=0.41$ AlGaIn photodiodes have been seen by PL to have defects 0.567 and 0.274eV below E_C , these probably correlate to 0.61eV and 0.234eV defects in GaN.

E. Kohn et al., IEEE Trans. On Microwave Theory and Techniques **51**, 634 (2003).

Review article on thermal and electronic transients. Compares a traditional AlGaIn/GaN HEMT, an InGaIn channel FET, and an AlGaIn/GaN double barrier structure, they find that the transient effects can be largely eliminated. Speculation for the double barrier structure is that the band structure is different so that the large surface charge expected in traditional HEMTs is not present.

O. Ambacher et al., Journ. Of Phys.: Cond. Matt., **14**, 3399 (2002). Germany, Italy, USA. AlGaIn, InGaIn, AlInN characterization. Nonlinear behavior of electric polarization as a fn of x . Also same for lattice constant, bond lengths, etc. Also discusses QW confinement energy, stark effects, n_s , E_F position relative to the first bound level as a fn of x .

S. L. Delage and C. Dua, Microelectronics and Reliability **43**, 1705 (2003).

Brief overview of some known failure mechanisms for AlGaIn/GaN HEMTs.

N.-Q. Zhang et al., IEEE IEDM Tech. Dig. 01-589, 25.5.1 (2001), U of Ca.

They find that a bilayer of SiO_2 (under the gate only) on SiN (everywhere) can produce a device with kV breakdown and low current slump.

J. K. Gillespie, R. C. Fitch et al., IEEE Electron Device Lett., **23**, 505 (2002). WPAFB.

Sc₂O₃ and MgO on AlGa_N/Ga_N HEMTs. Find that these passivations can result in higher power devices compared to Si₃N₄ passivation. Also Sc₂O₃ in particular ages well under DC stress. MgO needs care due to water absorption.

C. B. Soh et al., Journ. Of Phys.: Cond. Matt., **16**, 6305 (2004). Singapore.

DLTS on MOCVD Ga_N. Growth on various substrates to affect bulk dislocation densities. Find a level at $E_C - E_T \sim 0.18$ and 0.24-0.27 believed associated with screw dislocations, one at 0.59-0.63 believed associated with edge dislocations, 0.37-0.40 believed related to a Si containing point defect.

P. Muret et al., Superlattices and Microstructures, **36** 435 (2004). France.

Use DLTS based on Fourier transform technique to find deep levels in MOCVD Ga_N but show that using a different technique, **HR-DLTS, gives different trap energies than DLTS did** and more complicated trapping behavior, **with a given trap likely having several charge states and levels**. HR-DLTS is essentially DLTS done over both time and temperature with a complex fitting algorithm.

J. K. Gillespie, R. C. Fitch et al., Solid State Electronics **47**, 1859 (2003). WPAFB.

Good statistics – many MBE grown devices tested and compared, shows good uniformity can be achieved over a wafer.

D. Zuhang et al., Materials Science and Eng. R **48**, 1 (2005). Kansas State U.

More than you want to know about Ga_N, Al_N, SiC wet etching.

Prime questions for HEMT modeling:

A. Is the surface pinned and if so where? Based on the literature, pinning is unknown and probably device dependent. Certainly changes with passivation/unpassivation of devices. Density of pinning sites is expected to be lower for Si₃N₄ than for unpassivated.

G. Meneghesso et al., IEEE Trans on Elect Devices **51**, 1554 (2004).

Believe unpassivated $x=0.35$ MOCVD AlGa_N surface of AlGa_N/Ga_N HEMT grown on semi-insulating SiC to be pinned 0.3eV above E_v . 0.3eV comes from activation energy they measured.

J. P. Ibbetson et al., APL **77** 250 (2000). U. of California.

They argue that the surface must be pinned at about 1.65eV below E_C by at least $1.1 \times 10^{13} \text{ cm}^{-2}$ states. This pinning properly fits calculated 2DEG density based on band structure theory to Hall measurements of 2DEG density for various thicknesses of unpassivated $x=0.34$ AlGa_N/Ga_N structures

T. Hashizume et al., JVST B **19**, 1675 (2001). Hokkaido U. of Japan

Tested MBE vs MOVPE Ga_N and different passivations and find that the surface Fermi level can be affected by $\sim 1\text{eV}$ based on passivation or lack thereof and surface preparation. Si₃N₄ on MOVPE n-Ga_N was pinned at $E_v + 2.8\text{eV}$ (though if the surface state density is low then this pinning level will be sensitive to band profiles).

B. Where and what energy are the traps located? Intrinsic or hot electron generated ones... Looks like intrinsic traps are probably near/on the surface, near the gate or towards the drain side of the gate.

G. Meneghesso et al., IEEE Trans on Elect Devices **51**, 1554 (2004).
Believe unpassivated $x=0.35$ MOCVD AlGaIn/GaN HEMT grown on semi-insulating SiC to be pinned at surface.

W. Saito et al., IEEE Trans on Elect Devices **52**, 159 (2005).
Find a field plate is effective, this argues for traps or conductive states above the channel.
Not sure if the passivation in this work is the same for FP vs. no FP devices.

A. Vertiatchikh et al., Electronics letters **38**, 388 (2002).
Current DLTS done on $x=0.3$ AlGaIn/GaN HEMTs shows reduction of trap signal at 1.43eV and elimination of one peak from a trap level with SiN passivation. **Argues for near-surface traps.**

J. P. Ibbetson et al., APL **77** 250 (2000). U. of California.
They argue that the surface must be pinned at about 1.65eV below E_C by at least $1.1 \times 10^{13} \text{ cm}^{-2}$ states. This pinning properly fits calculated 2DEG density based on band structure theory to Hall measurements of 2DEG density for various thicknesses of unpassivated $x=0.34$ AlGaIn/GaN structures. **However, a pinned surface may argue against this as the site of hot electron traps as this surface might be hard to move.**

O. Mitrofanov et al., APL **82**, 4361 (2003). Bell Labs.
Si doping of unpassivated GaN capped AlGaIn/GaN HEMTs is seen to significantly reduce RF dispersion as seen by short gate turn on pulsing. **As Si doping is in the top 20Å of the device, argues that traps must be near this area to be affected.** Dispersion is immeasurable in selected devices.

O. Mitrofanov et al., APL **84**, 422 (2004). Bell Labs.
They do an interesting analysis of channel current transients for GaN capped $x=0.34$ AlGaIn/GaN HEMTs. Are able to see two well defined recovery times of $\sim 1.0 \mu\text{s}$ and $175 \mu\text{s}$ for certain device conditions. For the fast process they see Poole-Frenkel (PF) emission (activation energy is reduced by $E^{0.5}$, where E is the E field). Find that the trap capture process is not thermally activated, but the emission process is. **Based on PF emission and the need for a high E field to witness this effect, the fast process traps must be near the gate edge, either in the barrier or on the surface.**

P. B. Klein et al., Electronics Letters **37**, 661 (2001).
Analysis of a MBE AlGaIn/GaN HEMT, MOCVD AlGaIn/GaN HEMT, and GaN MESFET. PL spectra look very similar with similar activation energies of about 1.8 and 2.85eV for 2 traps. As activation energy would be expected to vary with alloy composition this **argues for traps in bulk GaN.**

C. What biasing schemes exist to look for traps, activation energies, etc? (Note: my author list is certainly not exhaustive)

- a. “Gate turn on”: Pulse V_G briefly onto the on state with constant V_D on device.
Can vary T and/or pulse width. Very sensitive test to look for current slump.
Devices biased this way are sensitive to hot electron filling of traps.
G. Meneghesso et al., IEEE Trans on Elect Devices **51**, 1554 (2004).
O. Mitrofanov et al., APL **82**, 4361 (2003).
E. Kohn et al., IEEE Trans. On Microwave Theory and Techniques **51**, 634 (2003).
- b. “Gate turn off”: Can supply brief off pulses to gate. Small I_{SD} seen during pulse
will be greater than steady state off current. Heating effects will probably
complicate the data however!
G. Meneghesso et al., IEEE Trans on Elect Devices **51**, 1554 (2004).
O. Mitrofanov et al., APL **84**, 422 (2004). - They look at the transient after removing the
gate pulse.
- c. “Drain turn on”: Pulse V_D briefly from 0 to an on state with constant V_G on
device.
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